MITIGATION OF RANDOM AND DETERMINISTIC NOISE IN MIXED SIGNAL SYSTEMS WITH EXAMPLES IN FREQUENCY SYNTHESIZER SYSTEMS

by

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Abstract

RF frequency synthesizer systems are prevalent in today's electronics. In a synthesizer there is a sensitive analog oscillator that may be affected by two different types of noise.

The first is random noise injection from active devices. This results in phase noise in the synthesizer's spectrum. The second noise source is deterministic. A digital frequency divider with high-amplitude switching is an example of such a deterministic source. This noise enters the system through various forms of electric or magnetic field coupling and manifests itself as spurs or pulling. Both forms of noise can adversely affect system performance.

We will first summarize methods for reducing noise. These already known steps have to do with layout techniques, device geometry, and general synthesizer topologies. Then we will show ways to isolate noisy interfering circuits from the sensitive analog systems. Finally, we present some considerations for reducing the effects of random noise.

A power supply filter can improve the effects of deterministic noise such as undesired signals on the supply line. We show several ways to improve the rejection of high frequency supply noise (characterized by the power supply rejection ratio or PSRR) through the design of a voltage regulator. The emphasis is on new techniques for obtaining good PSRR at S-band frequencies and above.

To validate the techniques, we designed a regulator in Peregrine Semiconductor's .25µm ULTRA CMOS Silicon on Sapphire process. It produces a 2.5V output with an input ranging from 2.6V to 5V and has a maximum current sourcing of 70mA. The regulator's low drop out performance is 60mV with no load and it achieves a power supply ripple reduction of 29.8 dB at 500 MHz.

To address random noise in synthesizers, the thesis provides preliminary investigation of an oscillator topology change that has been proposed in the literature. This proposed change reduces the phase noise of the oscillator within the overall system. A differential cross-coupled design is the usual topology of choice, but it is not optimal for noise performance. We investigate current noise injection in the traditional design and present an updated design that uses a differential Colpitts oscillator as an alternative to classic cross-coupled designs.

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Chapter 1 - Introduction

Modern day electronics exist in a mixed signal environment. This environment comes from the need to have high-speed, high-amplitude digital circuitry in close proximity to precision analog circuitry. Addressing the adverse effects of digital noise on this analog circuitry is the main purpose of this thesis. However, the analog circuitry is also affected in a negative way by another noise source. Random noise is also everywhere in modern day electronics. It exists in circuits due to resistance and the non-idealities in the operation of active devices.

We will use a synthesizer as an example of a mixed signal environment plagued by these two noise sources. However, the discussion presented can be applied to nearly all mixed signal systems.

The overall system performance improves by reducing noise. The noise sources cause many unwanted effects such as VCO pulling, jitter, spurs, and increased phase noise spectrums. Noise can come from many different places in a complex RFIC environment. These sources fall into two categories, which we shall label as deterministic and random.

1.1 Noise Types and Considerations

There are two main types of noise sources. The first is deterministic noise. A deterministic noise source is another circuit that may interfere with the analog circuits. This source usually presents itself as a disturbance on the supply or ground lines. This can be the case when a single supply shares connection to both a sensitive voltage controlled oscillator and a high amplitude frequency divider. This noise source can contribute to spurs seen in oscillator spectrums.

The second noise source type is random noise. Thermal noise is an example of a random noise source. Thermal noise is a result of electrons producing heat as they collide or become mobile. 1/f noise is another type of random noise. 1/f noise is caused by traps or defects in the lattice structure in active deices [1]. This noise source results in an elevated phase noise spectrum. It is necessary to reduce the effects of noise in order to improve system performance. The following two subsections discuss the two noise sources in more detail.

1.1.1 Deterministic Noise

Deterministic noise sources can be detrimental to the power supply voltage. When the supply is not clean, the desired circuitry can experience unwanted results such as spurs in oscillators caused by frequency modulation or a mixing operation (shown in Figure 1). Digital circuitry is an example of such a deterministic noise source. The spurs seen at the output of an analog oscillator surround the carrier signal at offsets equal to the frequency of the high speed switching. Figure 1 shows a case of deterministic noise as it affects the supply of a PFD/CP (Phase Frequency Detector and Charge Pump).

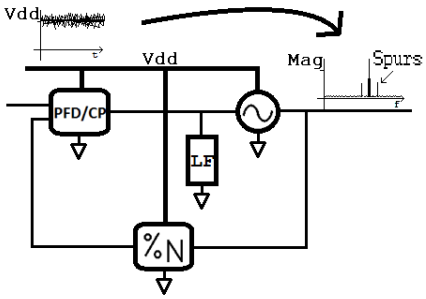

Figure 1: Deterministic interference caused by high-amplitude switching of the digital frequency divider.

As the divider switches between Vdd and ground, the supply must source more or less current. This non-ideal supply cannot make this change instantaneously. When the supply sources more current, the voltage on the supply will drop. Thus, the supply will be modulated with a frequency equal to the frequency of switching. Figure 2 illustrates how a large inverter like one found in pad driver circuits can disrupt a supply voltage in this way.

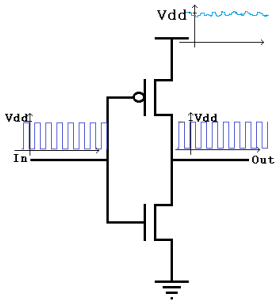

Figure 2: A large digital inverter like one that would be found in an exponential horn can cause a significant power supply disturbance.

In order to reduce the noise that is produced by high amplitude digital circuitry, a bypass capacitor can be added to the supply line. However, this digital circuitry is most likely on an integrated circuit. Capacitors on an integrated circuit consume too much space. Therefore, the value of the capacitor is limited by its small size.

The other option for the addition of a bypass capacitor is to place the capacitor off-chip. As Figure 3 shows, the off-chip capacitor is plagued by parasitic inductances.

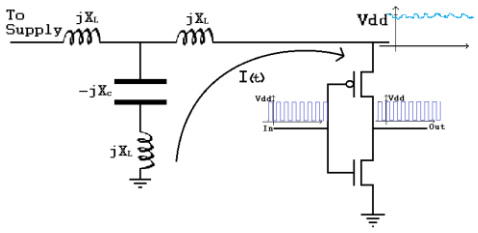

Figure 3: Putting a bypass capacitor off-chip does not suppress the high frequency disturbance on the supply line because of the significant amount of parasitic inductive reactance.

The inductive reactance of the bond wires and the printed circuit boards interfere with the capacitors ability to suppress high frequencies. The off-chip bypass capacitor that was meant to suppress this high frequency noise now looks like an inductance that does not suppress high frequencies to the integrated circuit. This problem may be solved by using on-chip voltage regulators and is the motivation for the main research discussed in this thesis.

1.1.2 Random Noise

Random Noise is a problem in all circuit devices. The resistance or restriction of electrons/holes mobility creates heat or thermal noise. This thermal noise is well known and is characterized by the resistance in every non-ideal device. The equations below (1) show its mathematical model [2].

$$v_{noise}^2 = 4kTR\ (V^2Hz^{-1}) \qquad i_{noise}^2 = \sqrt{4kTR}\ (A^2Hz^{-1}) \qquad (1)$$

Where k is the Boltzmann constant, T is temperature in Kelvin of the substrate, and R is the resistance in the devise. This i^2_{noise} can be added to the small signal model of a FET as in Figure 4 [1].

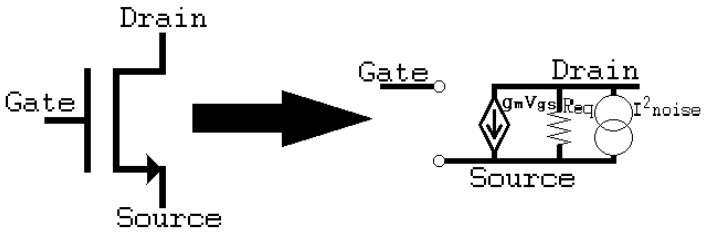

Figure 4: Noise model of a NFET.

In addition, the presents of imperfections in fabrication creates traps in the lattice structure. These traps restrict the transfer of electrons across the energy band gap [1]. This interaction of traps creates 1/f noise especially in transmitter [1]. Because FETs and Diodes have parasitic resistances and bandgaps with mobile carriers, they produce thermal and 1/f noise. Moreover, the noise of different devices varies within a given process. For example, the NFETs were found to have higher noise levels than the PFETs. In addition, small channel devices have worse performance then large channel devices [1].

The noise that devices produce, cause phase noise in the sensitive charge pump (CP) and VCO control portions of synthesizers (shown in Figure 5) [3].

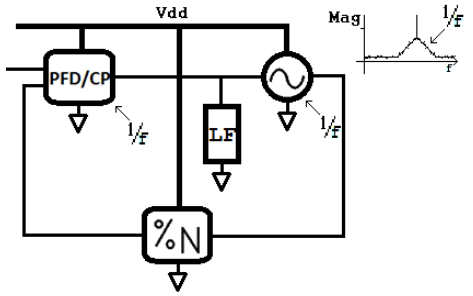

Figure 5: A synthesizer with an output spectrum.

1.2 Layout Issues

As previously discussed, this thesis will focus on the problem with power supply noise and its reduction through on-chip regulators with good high frequency PSRR performance. However, the power supply is not the only mechanism for which noise is spread through an integrated circuit. Many considerations in noise performance relate to the physical layout of the circuits, devices and metal layers. This section will cover the current state of the art in layout noise considerations as well as some electromagnetic theory issues.

When designing a layout on an integrated circuit it is important to consider radio frequency issues. Some of the issues I will discuss are; coupling, crosstalk, Faraday loops/cages, ground loops, and supply/ground bounce.

1.2.1 Mixed Signal Circuit Example

Figure 6 shows a schematic of a synthesizer with a modulator and power amplifier. Coupling is everywhere in such a radio frequency integrated circuit (RFIC).

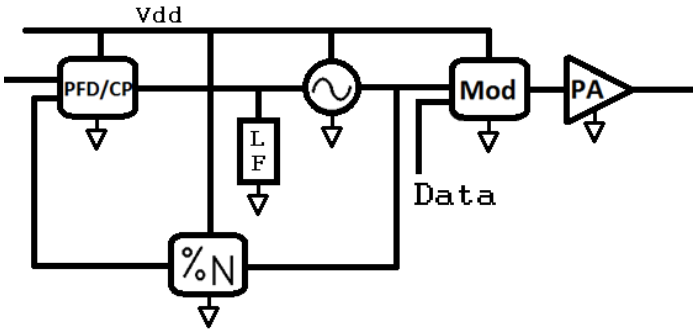

Figure 6: The full synthesizer with the modulator and the power amplifier on the output.

The oscillator and power amplifiers both have inductors. These inductors interact causing data-dependant frequency pulling in the oscillator. The digital divider couples to the analog circuitry through the supply, but can also couple through traces. These traces may be in close proximity and share some charge. There are also many places where a strong signal is radiated in a synthesizer. Sensitive signal areas such as the loop filter are very receptive to strong signals. These “transmitters” and “receivers” are often a path of deterministic noise propagation.

1.2.2 Coupling/ Crosstalk

Crosstalk between digital and analog signals can occur from either magnetic field coupling or electric field coupling in an IC layout. In addition, crosstalk can occur when analog and digital signals share the same V_{dd} and/or ground pins and associated bond wires. These subsections overview magnetic and electric field coupling.

Magnetic Coupling

Magnetic coupling is an issue in RFICs due to the use of inductors in RF designs. On an integrated circuit, there may be multiple inductors in a close area. These inductors produce magnetic fields through the air and substrate. Figure 7 shows magnetic fields from one inductor passing through another circuit's inductors producing a voltage in the second inductor.

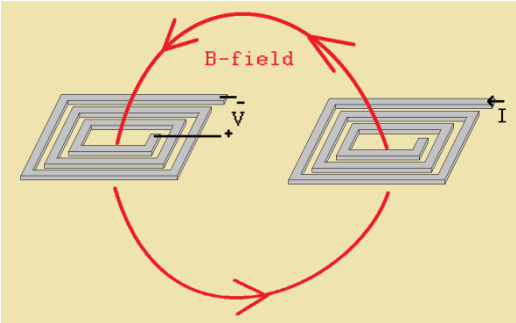

Figure 7: B-field coupling between inductors on an Integrated Circuit.

The two inductors interact like the windings of a transformer. If the inductor on the right in Figure 7 were a power amplifier, it would produce a strong magnetic field. The inductor on the left might be within a sensitive analog oscillator. The strong magnetic field created by the power amplifier will induce a voltage and current in the windings of the analog oscillator possibly leading to significant frequency perturbations. This can be quantified by the equation for mutual inductance (2). Equation (2) is for a current carrying wire s distance away from a loop of wire that is l long and w wide. Dimensions are shown in Figure 8 [4].

$$M = \frac{\mu_0 l}{2\pi} \ln \frac{s+w}{s} \qquad (2)\ [4]$$

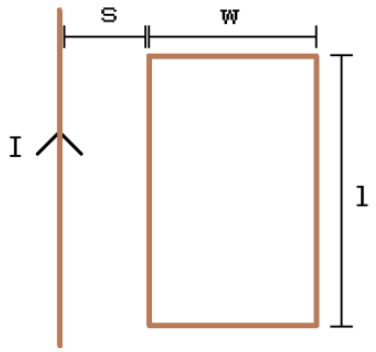

Figure 8: A current carrying wire close to a wire loop [4].

A few things can be done to reduce the interaction of inductors on an integrated circuit. Often an analog oscillator is created with two inductors with one inductor on each side of a differential output. These inductors can be wound in opposite directions. This "counter winding" results in a cancelation of the induced voltages in the received inductor.

In addition, the mutual inductance between inductors is inversely proportional to their separation. By increasing the distance between the inductors, the coupling between them decreases.

There are also several ways to shield or isolate the inductors [5]. By placing a grounded shield under the inductor, the penetration of both magnetic and electric fields into the substrate can be reduced [5]. However, solid shielding often reduces the inductance and Q or quality factor of the inductor [5] by introducing opposing currents in the shield. This reduction in Q may have an even worse effect on the system performance then the magnetic coupling. Reference [5] shows how a patterned ground shield can be used with reduced negative effects to reduce electric field penetration into the substrate.

Magnetic field coupling can also occur between inductors and analog circuitry that does not intentionally use inductors. Figure 9 shows a power amplifier's inductor that would produce a magnetic field. This magnetic field would pass through the analog circuitry on the left in Figure 9.

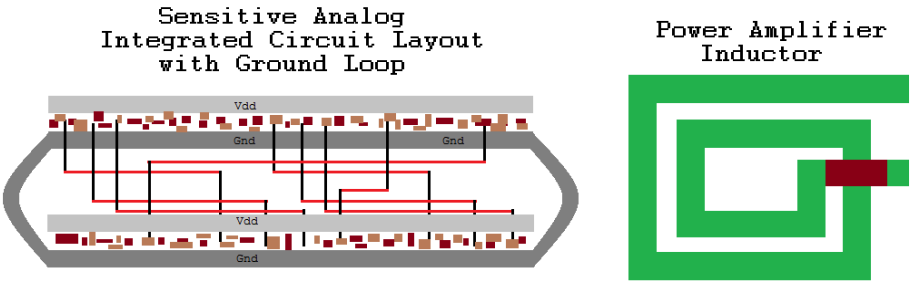

Figure 9: The right shows an inductor on an IC that is radiating a b-field. The picture on the left shows an example of a Faraday loop that would be adversely affected by the inductors B-field radiation.

The illustration on the left in Figure 9 presents an example of a Faraday loop. In the layout process, it is easy to unintentionally make these loops. In the same way as the two-inductor example above, the inductors B-field will pass through the Faraday loop producing a voltage in and inducing a current through the loop. The best solution to this interference problem is to break the loop on one side as shown in Figure 10.

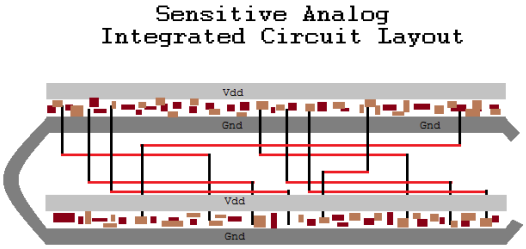

Figure 10: Shown is a layout of an analog circuit with no loop.

Capacitive Coupling

Magnetic field coupling is not the only type of coupling. Electric fields may also present a problem.

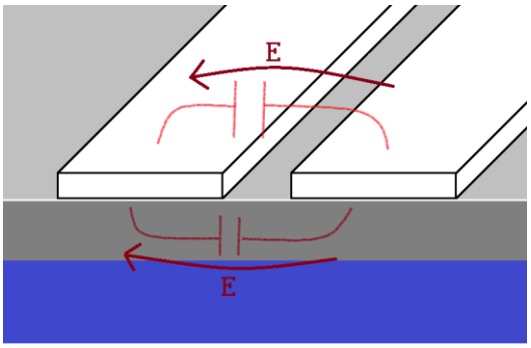

Figure 11: When two traces are very close together on an Integrated Circuit, there are electric fields and hence parasitic capacitance formed between the two lines.

When two lines are very close together the electric (and magnetic) fields between the lines, act as an electric bridge. For example, lines that are close together can be seen as the plates of a capacitor. This situation is illustrated in Figures 11 and 12.

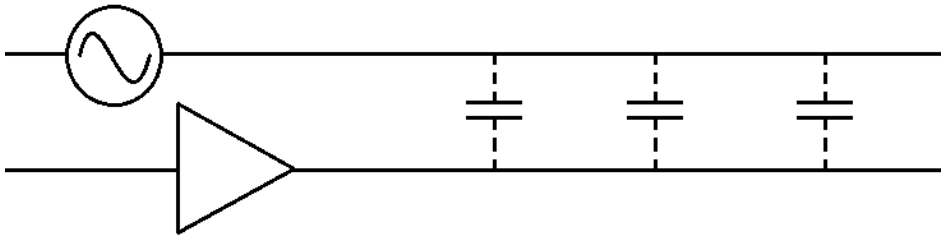

Figure 12: Shown is a schematic of an analog oscillator's output that was routed in close proximity to a power amplifier's output.

Depending on the frequency of the signals, the capacitive reactance between the lines may be sufficiently small to allow substantial high frequency currents to flow. The signals on these lines would then interfere with each other.

Capacitive coupling does not only happen above the substrate. Below the traces, the oxide forms a capacitor from the trace to the substrate. The substrate is resistive in standard silicon processes. This resistance can be quite low and characterized by (3).

$$R = \rho \times \frac{L}{A} \qquad (3)$$

Rho (ρ) is the resistivity of the material L is the length of the area and A is the area.

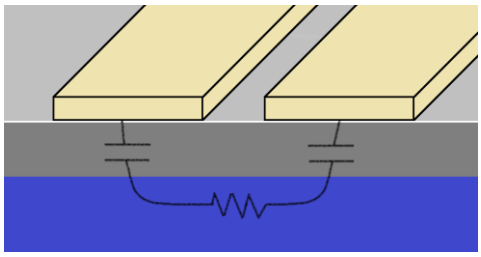

Figure 13: The capacitive coupling through the substrate.

The resistivity of silicon makes the resistance in the model small, as shown in Figure 13. This resistance is small compared with the capacitive reactance that is formed directly beneath the traces. Equation (4) for the parasitic capacitance is shown below.

$$Xc = \frac{d}{2\pi \times f \times \in \times A} \qquad (4)$$

However, a silicon on insulator processes such as Peregrine Ultra CMOS SOS has a high resistivity substrate. This high resistance isolates the two capacitances shown in Figure 13, but does not eliminate the problem. A capacitance will still exist through the substrate as shown in Figure 14. This capacitance is, in general, larger than the capacitance shown above in the substrate in Figure 11.

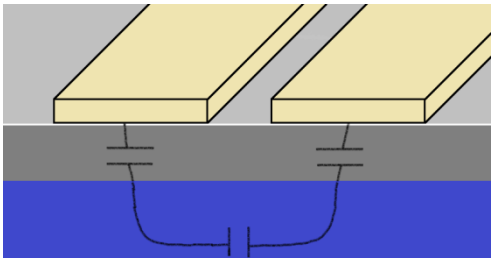

Figure 14: Insulative substrates have series capacitance

1.2.3 Supply/Ground Bounce

Supply/ground bounce comes from the fact that an inductive bond wire separates the ground and V_{dd} on the chip from the ground and V_{dd} off-chip. This inductor may have a changing current (e.g. created by a high amplitude frequency divider) passing through it. If a designer is not careful, the voltage produced may be added to the desired analog signals in a sensitive area such as the loop filter control voltage.

Figure 15 shows the typical case where the loop filter is left off-chip so the values can be fine-tuned. The voltage across the loop filter is labeled V_f, and the actual control voltage seen by the oscillator is V_c.

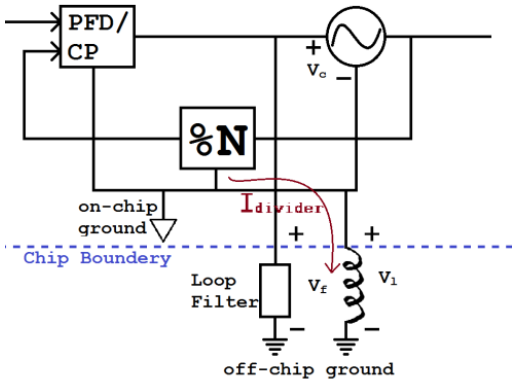

Figure 15: This schematic shows the difference between an on-chip ground and an off-chip ground.

The current through the divider's ground path changes as it switches. However, the current cannot change instantly through the bond wire and this creates a difference in voltage between the two grounds. This difference is shown in (5) as V_i. By applying KVL (5).

$$V_l = V_f - V_c \qquad (5)$$

Thus, the divider changes the voltage on the oscillator's input relative to the loop filter's ground. This is referred to as ground bounce.

A first solution to this problem would be to separate the on-chip grounds. The ground does not have to be shared between the oscillator and the divider as Figure 16 shows. Now there is a noisy digital ground and a quiet analog ground.

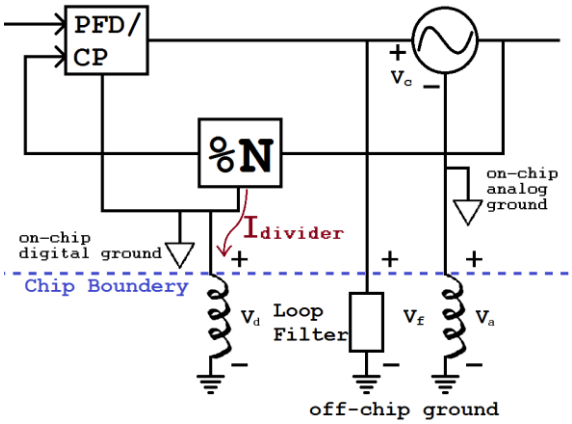

Figure 16: The ground lines can be separated to have a noisy digital ground and a quiet analog ground.

1.3 Prior Work

The research described in this thesis concentrates on isolating each sensitive subsystem in a synthesizer by supplying each with an independent power supply. This can be achieved by constructing on-chip voltage regulators with good supply isolation.

1.3.1 Regulator Specifications

Since the purpose is to use the regulator to improve the performance of a synthesizer system, we compiled a few important design specifications. These specifications where based on performance reported for other voltage regulator research found in the literature together with our research goal of providing good PSRR at S-band frequencies. The design specifications are shown in Table 1.

Table 1: Regulator Specification Table

Specification	Value
PSRR	< -30dB @2GHz
Output voltage	2.5V +/-50mV
Input voltage	3.0-7.0V
Current sourcing	10-100mA
Drop out voltage	< 0.5V
Supply Filtering f_c	150 kHz

In [6] a power supply rejection of -40dB is achieved. However, this -40dB is only characterized at 10MHz [6]. Reference [7] shows a dropout voltage of .3V. This specification is difficult to achieve but the frequency synthesizer system will work fine with a dropout of 0.5V. The process recommends a supply voltage in the 2.5V range so the supply to the regulator will be at least 0.5V above. The research uses a supply filter with the regulator. Without the supply filter, the PSRR is not well controlled into the GHz range as seen in [8]. The frequency corner of the filter is set to a few decades before the bandwidth of the operational amplifier.

1.3.2 Device Noise Research

The most important specification in a regulator is the PSRR. However, adding more circuitry to the overall system increases the number of devices that creates more random noise. Our goal is to keep this noise to a minimum by using appropriate devices and circuit design techniques.

Much is known about SOI device noise from the research already conducted at other institutions [1], [9]. The considerations that are found in [1] were taken into account as the testing circuits in this paper were being designed. This section will discuss several of the important results for device noise characterization.

When considering the biasing of a FET it is important to know that the FET's noise performance is not constant across all V_{ds} conditions [1]. As the V_{ds} value increases the 1/f spectrum may increase significantly [1]. In addition, the noise performance changes with modes or region of operation. The results found indicate that the active vs. triode region of operation do not have constant noise performance [1]. In the Peregrine process, there are many different types of devices. The process provides N and P type FETs with low, medium, and high thresholds. The NFETs were found to be worse than the PFETS in noise performance [1]. The 1/f performance is better with high thresholds then with low [1].

Chapter 2 - Regulator

Voltage Regulators are used to isolate a circuit from a ripple or disturbance on the supply line [10], [11], [12], [13]. Regulators typically have three main parts, the reference, the feedback, and the pass transistor. Figure 17 shows an example of a traditional regulator topology.

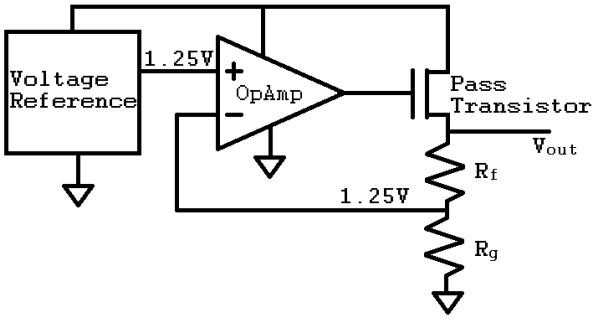

Figure 17: Classic regulator topology

A reference is often constructed using a diode with a constant current provided by a current mirror. Since the voltage across the diode does not change if the current is kept constant, it makes a good voltage reference. These current mirror diode structures are referred to as a bandgap reference. There are many different configurations of bandgap references [14], [15], [16], and [17]. Some of these bandgap references have elaborate current mirrors, utilize an operational amplifier, or have temperature compensation [14]. All the bandgap references have the goal of maintaining a constant output voltage across all operating conditions. This output voltage is typically 1.25V.

The feedback section is constructed with an operational amplifier and two feedback resistors. The operational amplifier takes the reference into its positive terminal. It can then step up that voltage to the desired output voltage (V_{out}) by controlling the pass transistor's conductance. The operational amplifier must have high gain to maintain a constant output and a high bandwidth to keep the high frequency supply ripple from modulating the output.

The final stage in a regulators design is the pass transistor. The pass transistor's output could be configured in different ways [18]. The purpose of this stage is to source the desired

current to the load while providing a good control for the operational amplifier. To source the desired current the transistor must usually be quite large. One way to configure the output is to use a simple NFET source follower [17]. In the source follower case, the transistor might just be the buffer transistor on the output of the operational amplifier. However, this configuration does not produce the best drop out performance [17]. To achieve a better performance, the pass transistor can be designed as a PFET in a common-source configuration.

The traditional regulator architecture of Figure 17 is good for many applications. However, the power supply rejection ratio (PSRR) is often only characterized to the low MHz range because of its poor performance in the GHz range. [19] [6] are good examples of such a case where the PSRR is not characterized into the GHz range.

Many of today's modern synthesized electronics such as Bluetooth and wireless LAN operate in the 2.4GHz range. For this reason, it is important to improve the PSRR performance through S-Band.

The traditional regulator only has good PSRR within the bandwidth of the operational amplifier. To address the problem a supply filter is added to the traditional design to suppress frequencies above the bandwidth of the operational amplifier. This general technique has been reported in such papers as [6], but to-date, there has been limited study and optimization of PSRR performance at S-Band frequencies. Figure 18 below shows how these filters are added to a traditional regulator design.

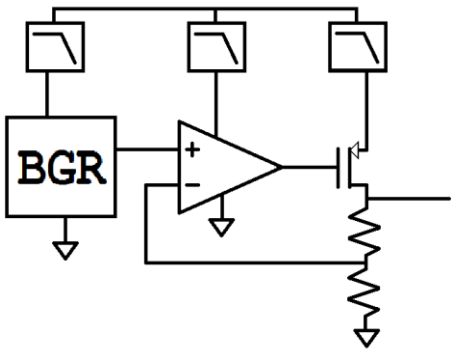

Figure 18: Supply filtering each stage of the regulator reducing the high frequency pass-through.

The supply filters can now reduce the high frequency interference on the supply line before it is allowed to affect the regulator stages. This new regulator can be used in an environment that has S-Band signals. An example of such a system is the synthesizer in Figure 19.

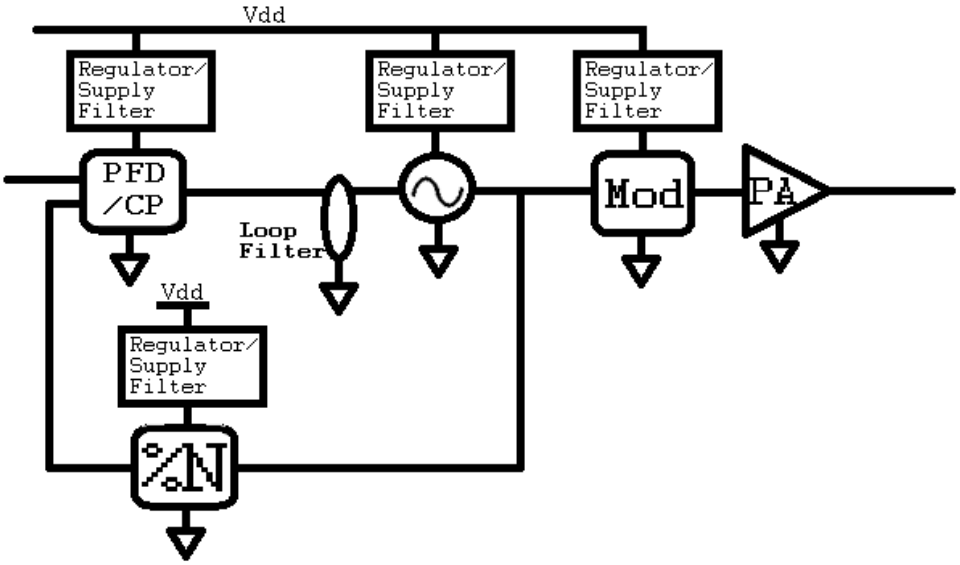

Figure 19: General layout of a synthesizer with added regulators and supply filtering.

The rest of this chapter presents the implementation considerations for designing a voltage regulator as a tool in mixed signal environments. We will discuss some regulator architectures and schematics. Finally, we will present some of the regulator simulations and final testing.

2.1 Regulator Architecture and Schematics

The following subsections present engineering tradeoffs in the design. Size is a main constraint in most integrated circuit designs [7]. While this issue is not a big problem in the research stage, it is important in the industry [7]. Current sourcing specification is also a large factor influencing design size in almost every case.

The first subsection discusses the supply filter. The second subsection shows the many tradeoffs considered in the output stage. The output stage consists of a supply filter feeding a pass transistor in the low drop out (LDO) configuration. The final subsection illustrates the need

for a steady quiet reference voltage. This voltage reference is traditionally a Bandgap reference. The bandgap reference is implemented in this research but with a somewhat complex temperature compensated design. Device noise is also an issue that is critical in band gap reference design and will considered.

2.1.1 Filtering

In an effort to isolate sensitive circuitry from supply noise, a supply filter is typically used [7]. The simplest supply filter is a bypass capacitor. While this method works reasonably well for suppressing high frequency noise on a PCB, it is not the ideal solution for all cases. In the case of an integrated circuit design, it is not possible to get a large value capacitor on-chip in a sufficiently small area. These on-chip capacitors also do not have the best Q or quality factor. This means that the capacitor will start to pass some high frequencies as the series impedance becomes more resistive. Figure 20 shows the small valued capacitor and its series resistance.

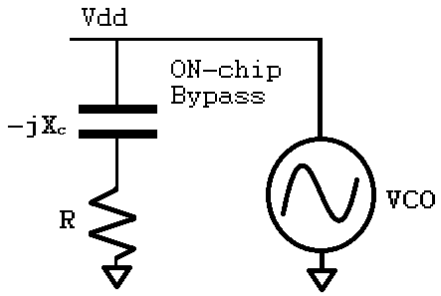

Figure 20: A bypass capacitor with series resistance on-chip filtering an oscillator.

Active RC Supply Filtering

There are better ways to filter the supply. A RC low pass filter can be used to filter the supply on-chip Figure 21.

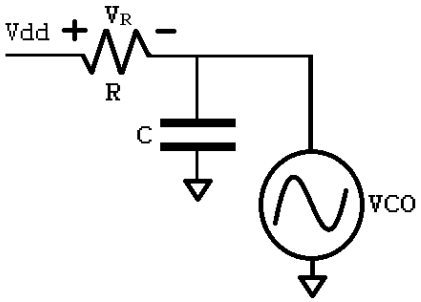

Figure 21: Simple RC low pass filter.

As shown in Figure 22 and (8), source follower is added to a simple RC filter. Without the transistor, there would be a significant voltage drop across the series resistance. Figure 22 shows the final design of the supply filter.

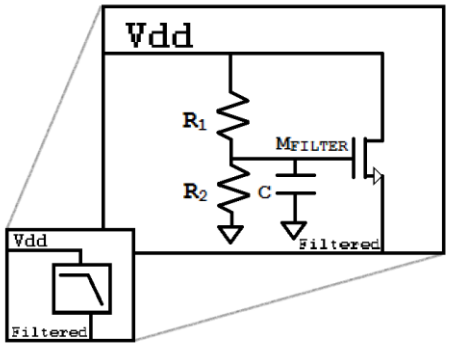

Figure 22: A simple supply filter can provide supply isolation in an integrated circuit.

In the voltage regulator application, this method allows you to set the bandwidth of the filter to a low enough value to reject frequencies above those not addressed by the operational amplifier feedback system. The low pass frequency corner is set to be two decades before the operational amplifier's gain bandwidth product. The gain bandwidth product is the point where the amplifier's gain drops to unity. Below this point, the gain of the feedback system suppresses any unwanted noise. The low pass filter's cut off frequency is set in such a place to reject the noise that the feedback control system is not able to attenuate. The cut off frequency is given by (8)

$$f_c = \frac{1}{2\pi \times R_1 || R_2 \times (C + C_{gate})} \quad (8)$$

In our regulator, a separate supply filter will be added to each stage of the regulator. Giving each stage, its own supply filter reduces the feedback paths in the system. Each filter is specifically sized to source the current that stage needs to optimize area consumption on-chip. The filter that supplies the output stage will have to be scaled for different current sourcing applications. In addition, the source follower used in the filter that sources the output stage improves the dropout voltage performance because it can be constructed using an intrinsic device. This intrinsic device has a threshold of 0 volts and can therefore operate with a very small drain source voltage. This optimizes the headroom for the pass transistor stage.

2.1.2 Pass Transistor

The drop out voltage of the regulator is also a key design performance measure. If a regulator has a low drop out voltage then the regulator's supply voltage can drop very close to the regulators output voltage. For example, if someone is designing a 2.0 V regulator. The regulator will maintain the 2.0V output until the supply voltage (V_{dd}) drops down to 2.3V. This means the dropout voltage performance is 0.3 V. The drop out voltage is mainly affected by the pass transistor's configuration.

There are two main configurations that can be used at the output stage [17] (Figure 23).

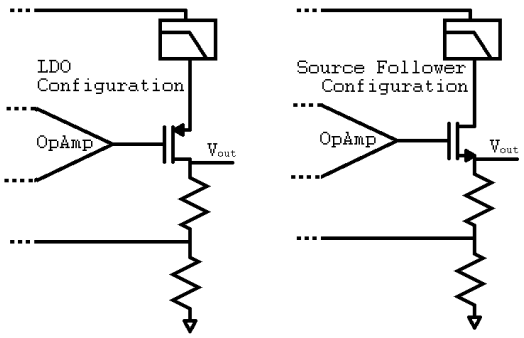

Figure 23: The output stage of the regulator with the LDO configuration on the left and the source follower configuration on the right.

One configuration is the source follower and the other is called the LDO. These two configurations both have advantages. The source follower is the classic output stage to use. In [17] a source follower configuration was found to have better line regulation. An LDO was found to have better load regulation [17]. The source follower configuration has a major flaw. The impedance seen from the filter side (or the drain of the FET) is a very high impedance node. This results in the source follower not having high gain. This low gain results in poor voltage drop out performance.

The LDO configuration is designed to keep the drop out as low as possible. In the LDO configuration, the pass transistor is in a common drain configuration shown by Figure 23. Since the device is a PFET and its gate voltage can be lower than the output voltage with this configuration, the voltage drop out performance is much better. For this design, the specification was for the regulator to output a voltage that was 0.5 volts lower than the minimum supply voltage. For this reason, this regulator design uses the LDO configuration.

In the design of the voltage regulator, a dominant tradeoff is physical size to the current sourcing performance. This tradeoff mostly depends on the pass transistor implementation in the output stage of the regulator. In the output stage, two transistors must source the output current. Both the transistor in the supply filter and the output pass transistor are scaled by the amount of current the regulator needs to source. This relation is set by the I_d equation (9) where the drain current must be about 5% higher than the most current the regulator will have to source plus the current through the divider of the feedback loop.

$$I_d = K' \frac{W}{L} (V_{overdrive})^2 \qquad (9)$$

This 5% is just for error margin due to shifting thresholds.

The pass transistor is also the output load of the operational amplifier. For stability of the amplifier, the pass transistor cannot be too large. The size of the output transistor is directly related to the amount of capacitance seen from the gate. If the value of this capacitance is too large, the control feedback loop may become unstable. However, there is a solution to this problem. The capacitance as seen from the gate of a transistor is proportional to Width × Length. However, the current (9) is directly related to width but inversely related to the length. On the other hand, using the minimum length may not be the best solution.

The equation (9) above shows the long channel model for current through a FET. The equation for a small channel FET is somewhat more complicated and less ideal than the long channel case. The FET will no longer be considered a long channel devise if the length is small. This is yet another trade off in the considerations surrounding the design of this very important output stage. The devices that have larger lengths can be modeled using the long channel equation (9). These long channel devices produce less 1/f noise if used with high V_{ds} values then a small channel device used with a high V_{ds} [1].

2.1.3 Bandgap Reference

Shown on the right in Figure 24 is the core of the Bandgap Reference (BGR). Mostly it is an elaborate current mirror, which has the purpose of establishing an equal current through each diode in the circuit. The final stage is just a current source fed into a resister of value R×K and a very large diode. If the final leg were to be only a resister, the circuit would form a regulator, but the regulator would be very temperature dependant [14]. If the temperature increased then the output voltage of the regulator would also increase. This relative relationship is referred to as PTAT or proportional to absolute temperature. A diode's voltage change has the opposite relationship with temperature. The relationship between the voltage across a diode and its temperature is CTAT or complimentary to actual temperature. Therefore, in adding the diode, if done correctly, the output voltage becomes no longer temperature dependant.

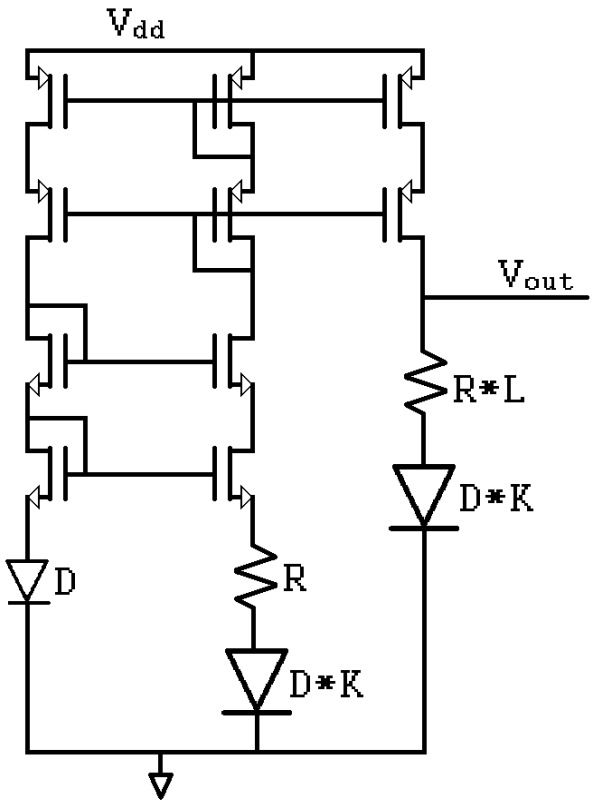

Figure 24: Band Gap reference core.

However, these PTAT and CTAT relationships are not perfectly linear. This relationship is illustrated in Figure 25 [15].

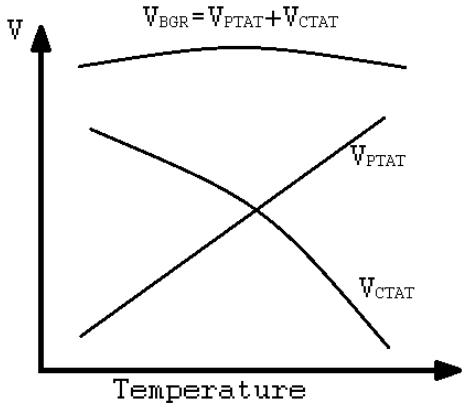

Figure 25: Relationship between V_{BGR}, V_{PTAT}, and V_{CTAT} [15].

The resultant curve has a trend that decreases either side of the midpoint. Equation (11) demonstrates how the PTAT and CTAT can be aligned for a maximally flat temperature relationship at a specific temperature range.

$$V_{ref} = V_{D3} + \frac{nk \times \ln K \times V_T \times T \times L}{q} \qquad (11)\ [14]$$

L is the factor that the final stage resistor must be larger than the resistor in the second stage or the reference. K is the factor that the second two diodes must be larger than the diode in the first leg.

2.1.4 Simple BGR based Regulator

An early, simple regulator was implemented in an effort to create a design that did not require the use of an operational amplifier. This schematic Figure 26 shows the total circuit design.

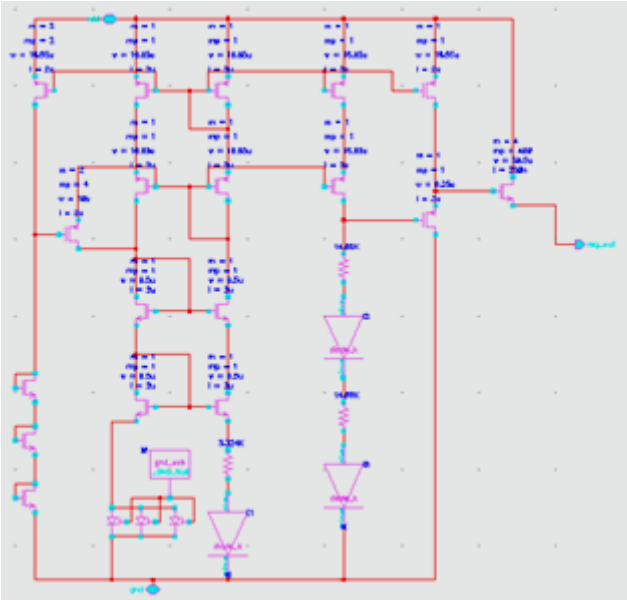

Figure 26: The initial design of the bandgap reference with a standalone output stage.

Note the addition of an extra resistor and diode in the third stage. This was added to raise the BGR output voltage to 2.5V. The addition on the far left is the start up circuit [14]. This circuit's only purpose is to ensure that the current mirror flows current. Moreover, if the circuit starts up properly the start up circuit has no effect on the function of the BGR. The final addition to the core is the two output FETs. The last output FET is a standard source follower so that the BGR can provide 20 to 100mA to the circuitry

A PFET source follower was also added before this output FET to step up the output slightly this accomplishes two goals. The first goal is to lower the input voltage required to turn on the BGR's 2.5 V output. The second goal is to regain the voltage lost in the V_{gs} drop on the source follower output FET. Again, in this early design stage the output of this circuit is meant to be run independently. For the final design, the gain stage is unneeded due to the final feedback system as well as the construction of the final output stage.

The three graphs below in Figures 27-29 show the temperature independence of the simple regulator. The graphs show input Voltage (x-axis) vs. the output voltage (y-axis). The simulation was run at 23 degrees C, 65 degrees C, and 100 degrees C. As you can see from the graphs, there is a difference of less than 10mV between the three.

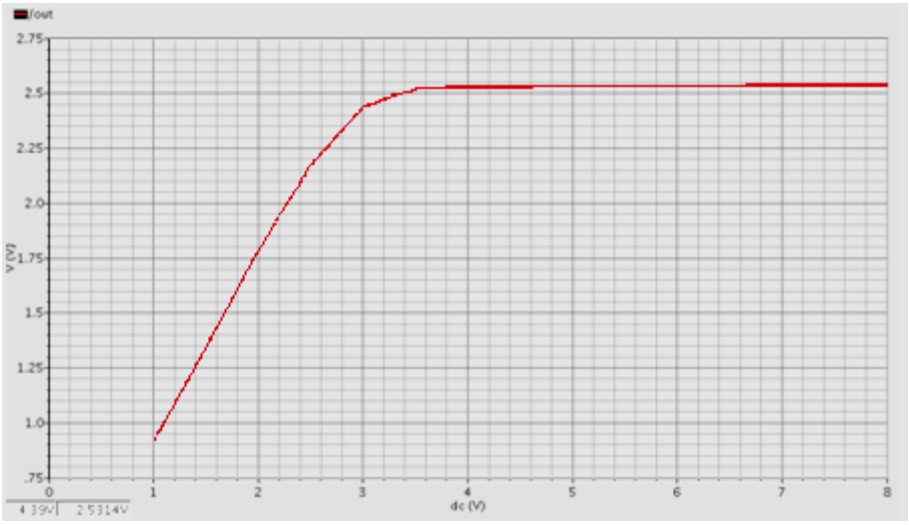

Figure 27: Output voltage simulation at 65 degrees C

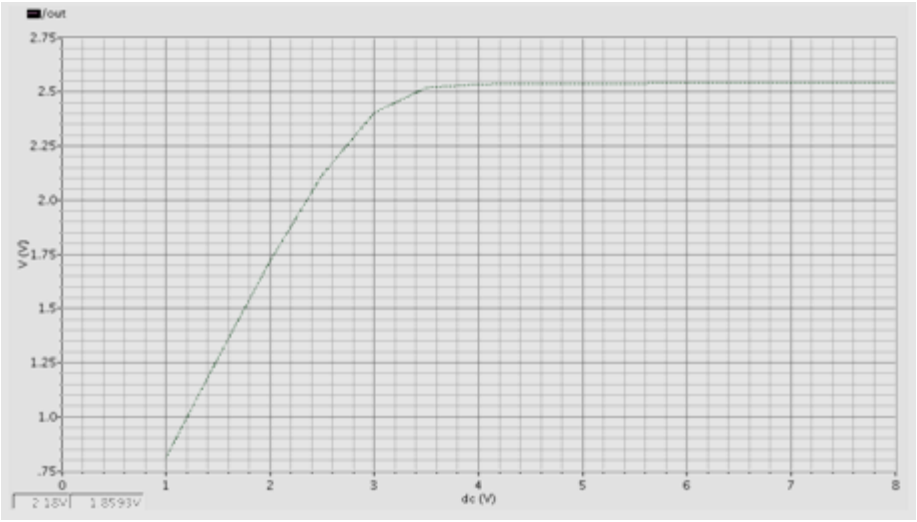

Figure 28: Output voltage simulation at 23 degrees C

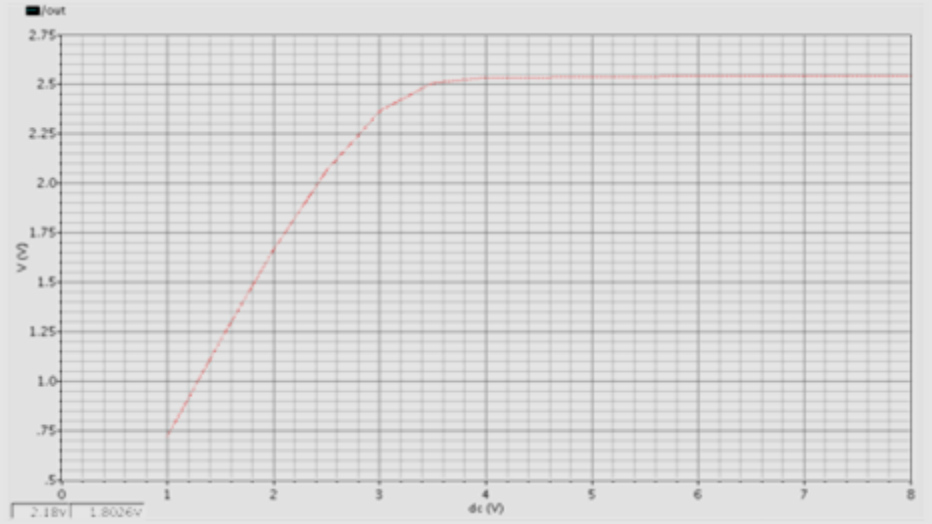

Figure 29: Output voltage simulation at 100 degrees C

The startup circuit has a small draw back that can be somewhat reduced by over sizing the main start up circuit transistor. This effect manifests itself as an increase in the output voltage at high input voltages. Figure 30 shows the effect of the startup circuitry on the high input voltages.

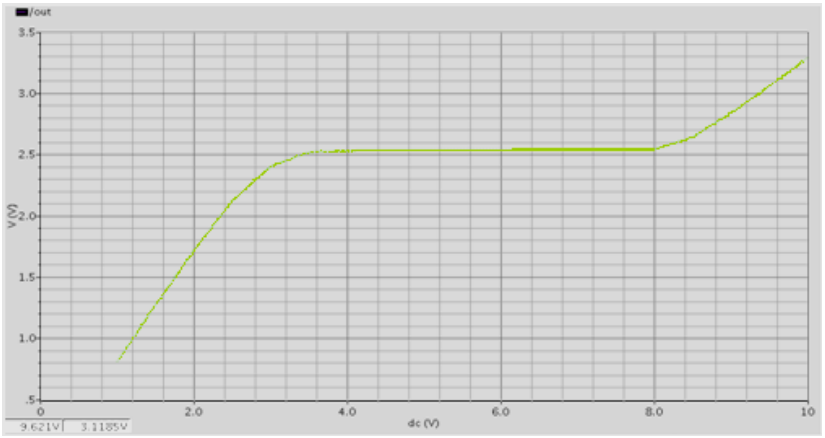

Figure 30: The simulated output plot of the band gap reference.

2.1.5 Noise Considerations

Device noise is the most important issue associated with the band gap reference. The noise at the output of the band gap reference will be amplified by the closed loop gain and seen at the output of the regulator. The device noise comes from the resistors, diodes, and FETs. In

this design, it is necessary to have NEFTs but not in the output leg, this will help in isolating the noisy NFETs. The sizes of the devices are very dependent on the current that is chosen to use through each leg. The channel lengths can be made large when it is possible. Diodes are believed to be the source of most of the noise in the band gap reference. The diode in the first leg of the BRG is the base line is small. The second two legs have to have a diode that is a factor of K larger making those quite large devices. These devices create a significant noise source on the output of the BGR. This is especially the case in the Peregrine process where they are implemented in ultra thin silicon, as opposed to more traditional vertical diode structures. In the following chapter, we will show the effects of this device noise on the final regulator. The next chapter also presents the testing procedure and results for the final regulator.

2.1.6 Full BGR with Operation amplifier and Filtering

For the final design of the voltage regulator, a more traditional regulator architecture was adopted. The simple regulator design suffered from process tolerances changes of voltages of the output transistors. The design shown in Figure 31 shows the final topology of the regulator utilizing a feedback operational amplifier control system.

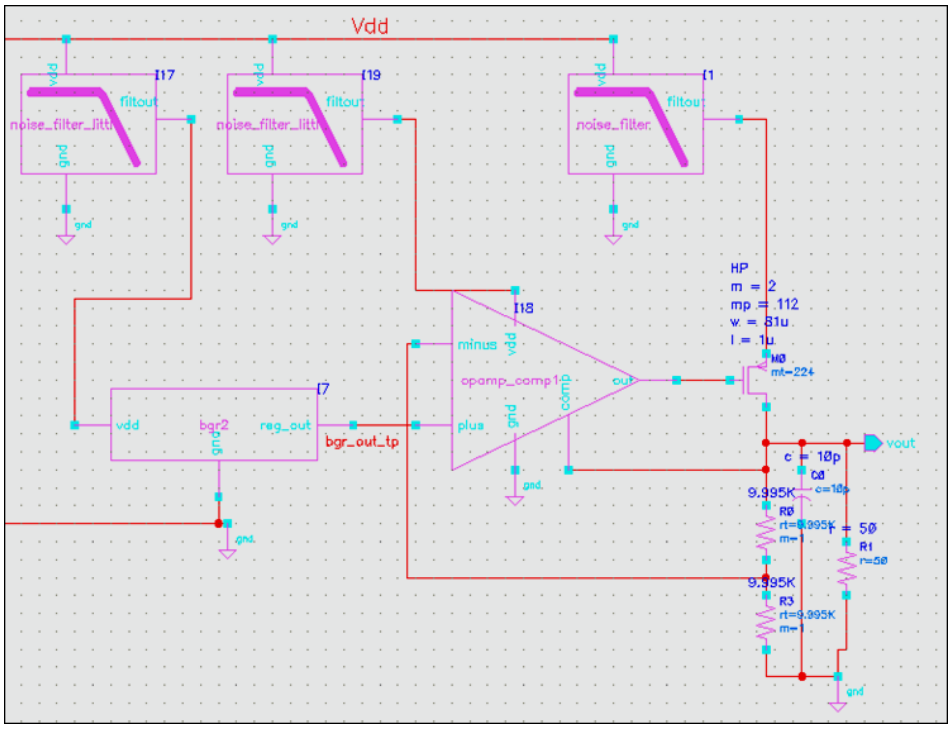

Figure 31: Final top-level regulator design.

The operational amplifier feeds into a PFET pass transistor sized to source 70mA. A compensation line is fed from the output into the operational amplifier to maintain stability. Figures 32-34 show the final designs of each individual block.

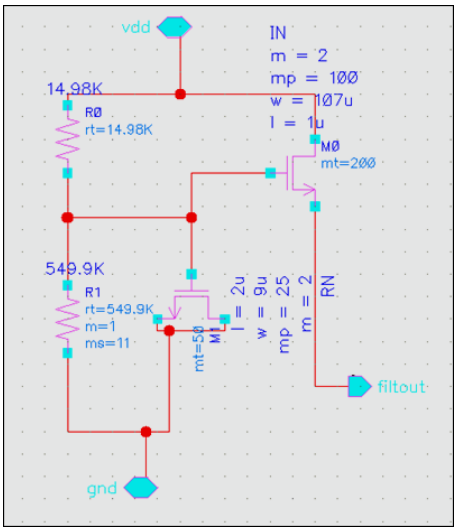

Figure 32: Final supply filter design.

The filter shown in Figure 32 was implemented with a resistive voltage divider to set the biasing of the NFET source follower. The resistors as combined in parallel form a low pass filter with the MOSFET capacitor. This filter's corner frequency was set to 150 kHz. The goal was to achieve at least 20dB of attenuation at 1 GHz. However, the voltage divider formed by the C_{ds} capacitors (Figure 50) and the output capacitance (shown in Figure 31) made this attenuation less than 20dB. The output capacitor's size is limited due to the integrated circuit process used. Figure 31 shows that a supply filter sources each stage of the regulator.

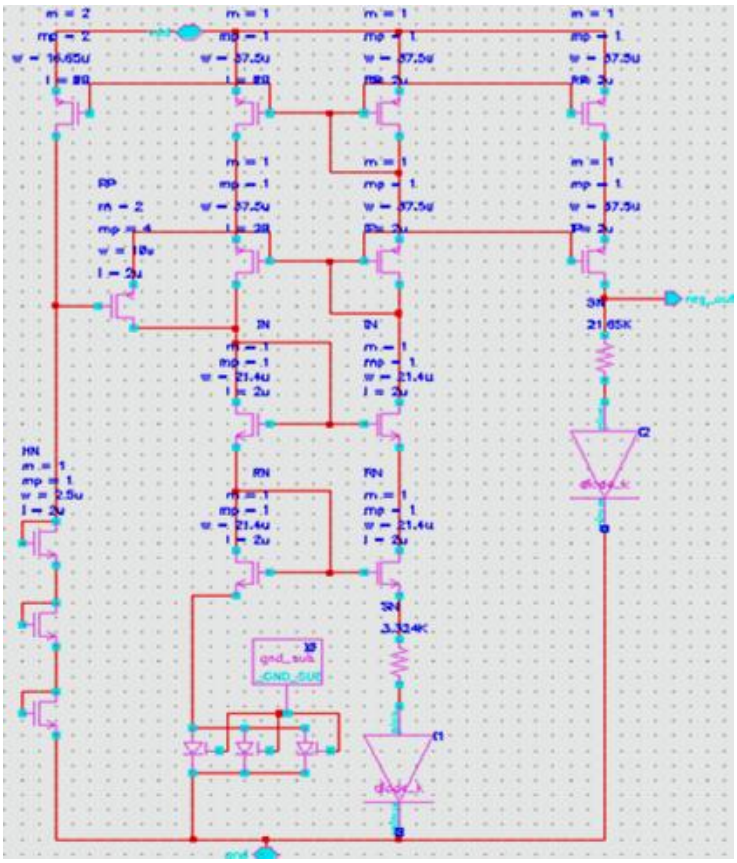

Figure 33: Final Band Gap Reference Design.

Figure 33 shows the final schematic of the BGR. The band gap reference mirrors the design presented above in section 2.1.3. The design starts with the current. Current is chosen from analyzing the diode in the first stage of the core of Figure 24. The current needs to be set to a linear region of the diode's log-current versus voltage relationship. This current is held constant through the cascoded mirror structure. The mirrored current is fed into a larger diode and resistor. This diode must be sized larger than the first diode. The voltage across the resistor and large diode matches the voltage across the smaller first diode. The difference in diode voltages therefore occurs across the resistor, creating a PTAT current reference. The final stage provides temperature compensation (as discussed above) and outputs a stable 1.25 V reference. This voltage reference is fed into the positive input of an operational amplifier shown in Figure 34.

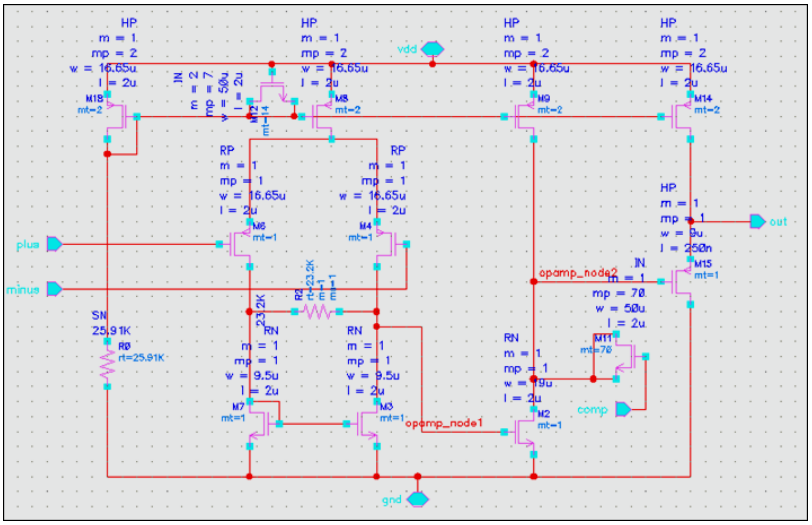

Figure 34: Final operational amplifier design.

The operational amplifier has a standard differential input stage with an active load. Then a gain stage is followed by a source follower output. Stability was achieved by compensating with a MOS capacitor from the output of the regulator back to the opamp_node2 shown in Figure 34.

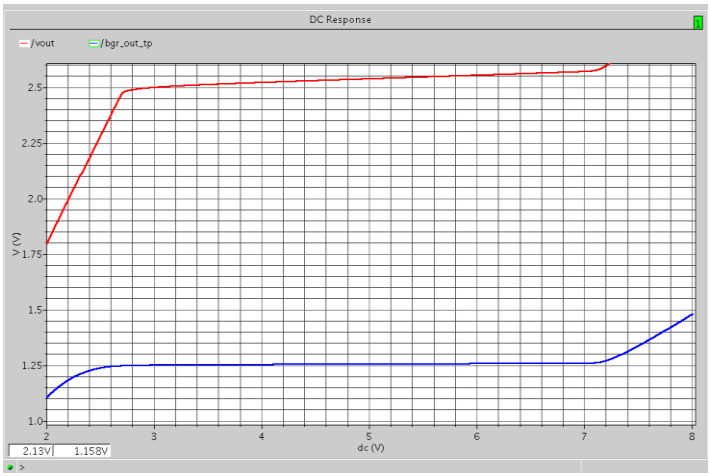

Figure 35: Output Voltage simulation of final design.

Figure 35 shows the output voltage of the BGR in blue and the regulator in red verses the input voltage. In this simulation, the regulator was sourcing 10mA.

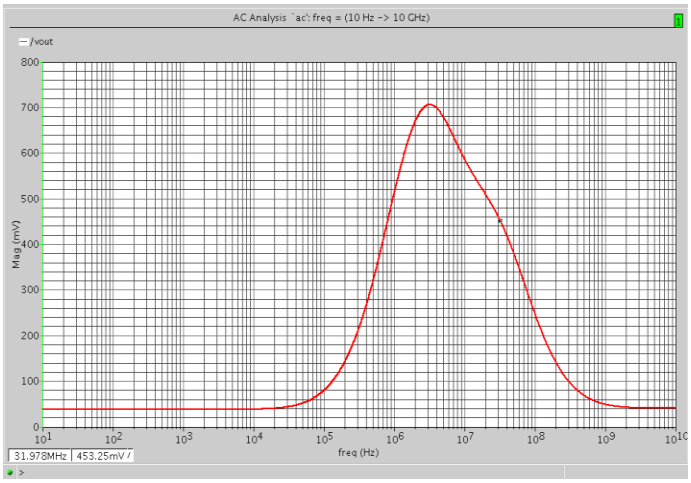

Figure 36: Supply rejection simulation.

Figure 36 shows the supply rejection of the final regulator. For this simulation, a 1 V ac sweep was applied to the V_{dd} line and output is plotted. The layout of the voltage regulator is shown in Figure 37.

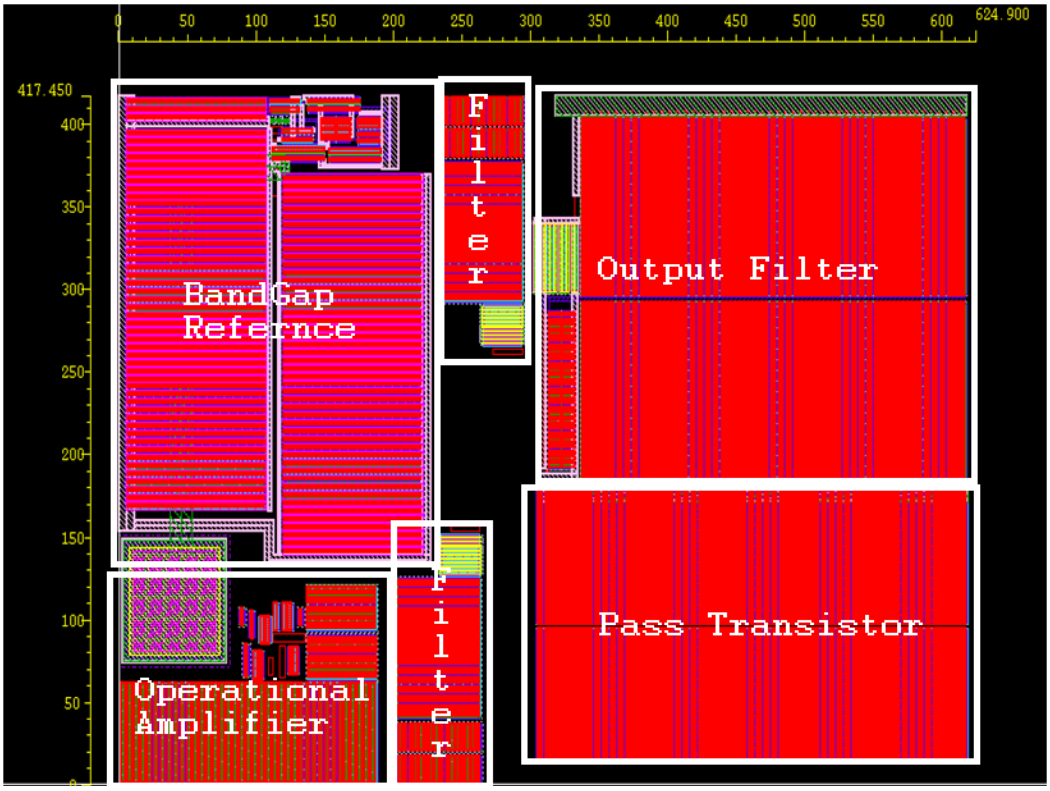

Figure 37: Layout of voltage regulator.

Chapter 3 - Regulator Performance Testing

The regulator was fabricated through Peregrine Semiconductor and ball bonded into a plastic package for testing. Figure 38 shows the packaged device and associated pin out.

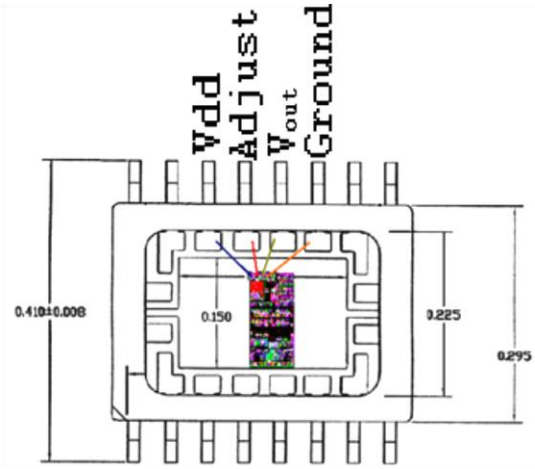

Figure 38: The bonding diagram and pin out for the Regulator for ball bonding.

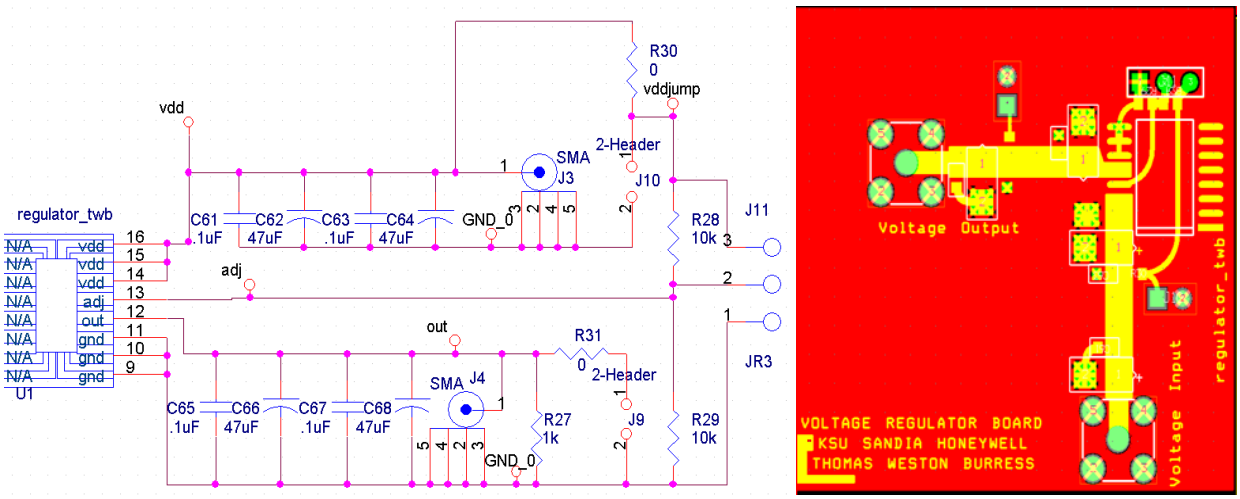

Figure 39: Schematic and layout of the PCB board fabricated for testing.

Figure 39 shows the schematic and layout of the PCB test board. This test board is equipped to do simple DC tests as well as radio frequency noise and ripple analysis. Multiple locations for bypass capacitors are added to the board to check stability and characterize the value, and distance from chip of capacitances needed. SMA connectors and 50 Ω traces are needed for high frequency noise and ripple analysis. There is an adjust line where the output

voltage of the regulator can be set. This can be done by adding fixed resisters off-chip or by applying a DC voltage to the optional header. Loads can be applied using a fixed surface mount resistor on the PCB, through the SMA connector, or using an on-chip FET that can be accessed by probing the IC. This on chip FET is large in order to simulate the effects of an on-chip load.

3.1 Regulator Performance

The following plots show the base voltage regulator performance. Each of the plots where measured using an Agilent 34405A DMM and HP E3616A power supply. These six plots each show multiple regulators from the same run. A few regulators where tested each time to verify accuracy of the measurements and to identify any discrepancies over process tolerances.

Figure 40 shows how the voltage output behaves with increasing input voltage. From this data, the drop out voltage of 0.5V was verified.

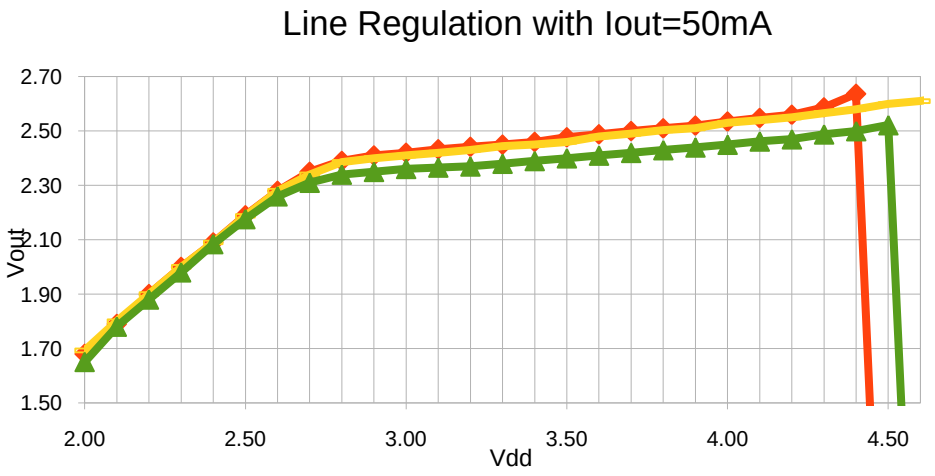

Figure 40: Plot of changing input voltage with respect to the output voltage under 50 Ω load conditions.

Figure 41 shows the line regulation of the regulator under unloaded conditions.

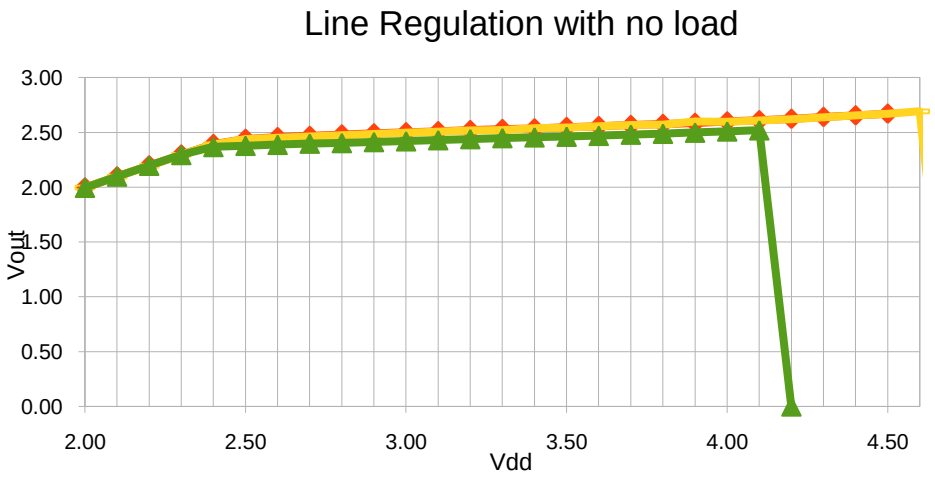

Figure 41: Plot of changing input voltage with respect to the output voltage under un-loaded conditions.

For Figure 42 the load was changed and the output voltage was monitored to find the maximum current the regulator can source without allowing the voltage of the output dropping below tolerance. The minimum load resistance from this data was found to be 75Ω. This current is the current sourced by the regulator to the load. From this plot, a maximum current that the regulator can source is found to be about 70 mA.

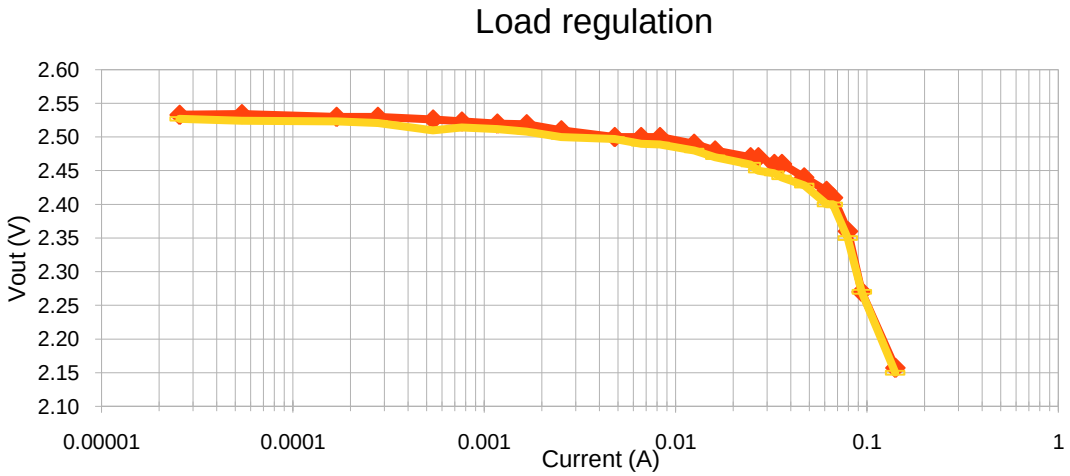

Figure 42: Plot of output current sourced verses the output voltage as current out increases.

Plots in Figure 43-44 show how the current drawn from the supply reacts when the input voltage is increased.

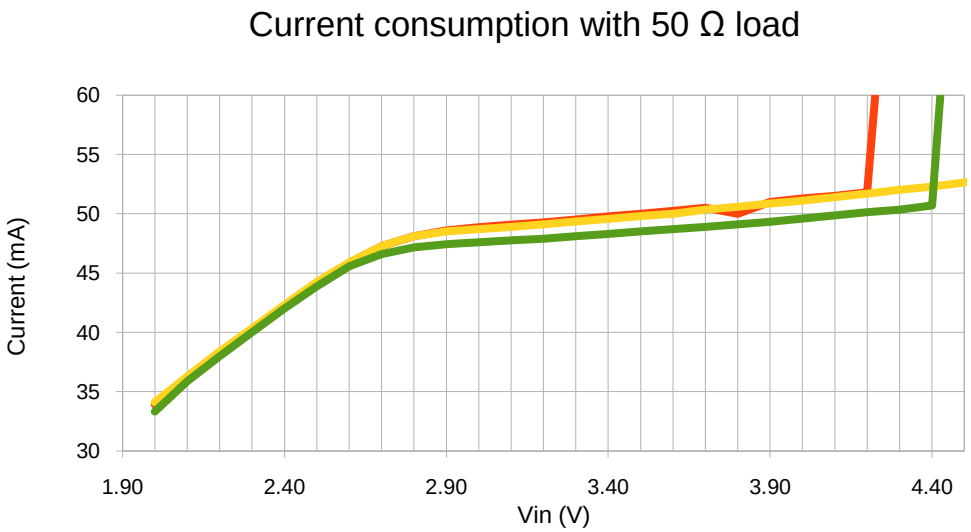

Figure 43: Plot of a swept input voltage with respect to current drawn from the supply under a 50 Ω load condition.

Under loaded conditions, the regulator performed as expected until the current spikes at approximately 4.1V. This spike in current is a result of the ESD pad structure. The ESD pad uses an HN clamp and this clamp is trying to protect the circuit from high voltages. However, the effects of these clamps prevented the characterization of the regulator at higher voltages.

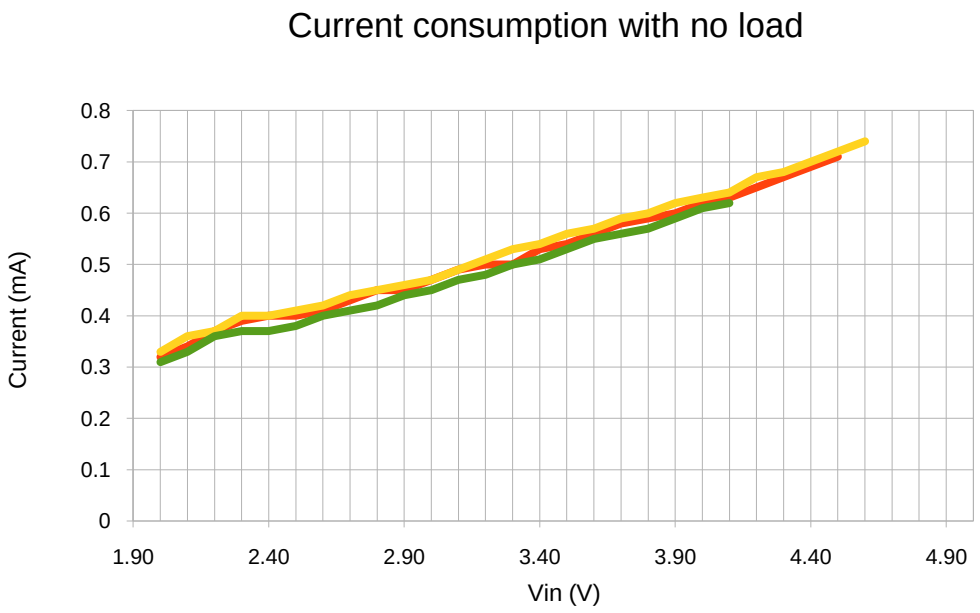

Figure 44: Plot of a swept input voltage with respect to current drawn from the supply under un-loaded conditions.

Figure 44 shows the quiescent current is approximately 0.5mA and there is a fairly linear relationship between the current and the input voltage when the output is left unloaded.

3.2 Noise Measurements

The first and most important test relevant to this research discussed in this section is noise testing. The BGR was found to be producing a significant amount of 1/f noise as well as an elevated thermal noise floor. Figure 45 shows the plotted results of this measurement.

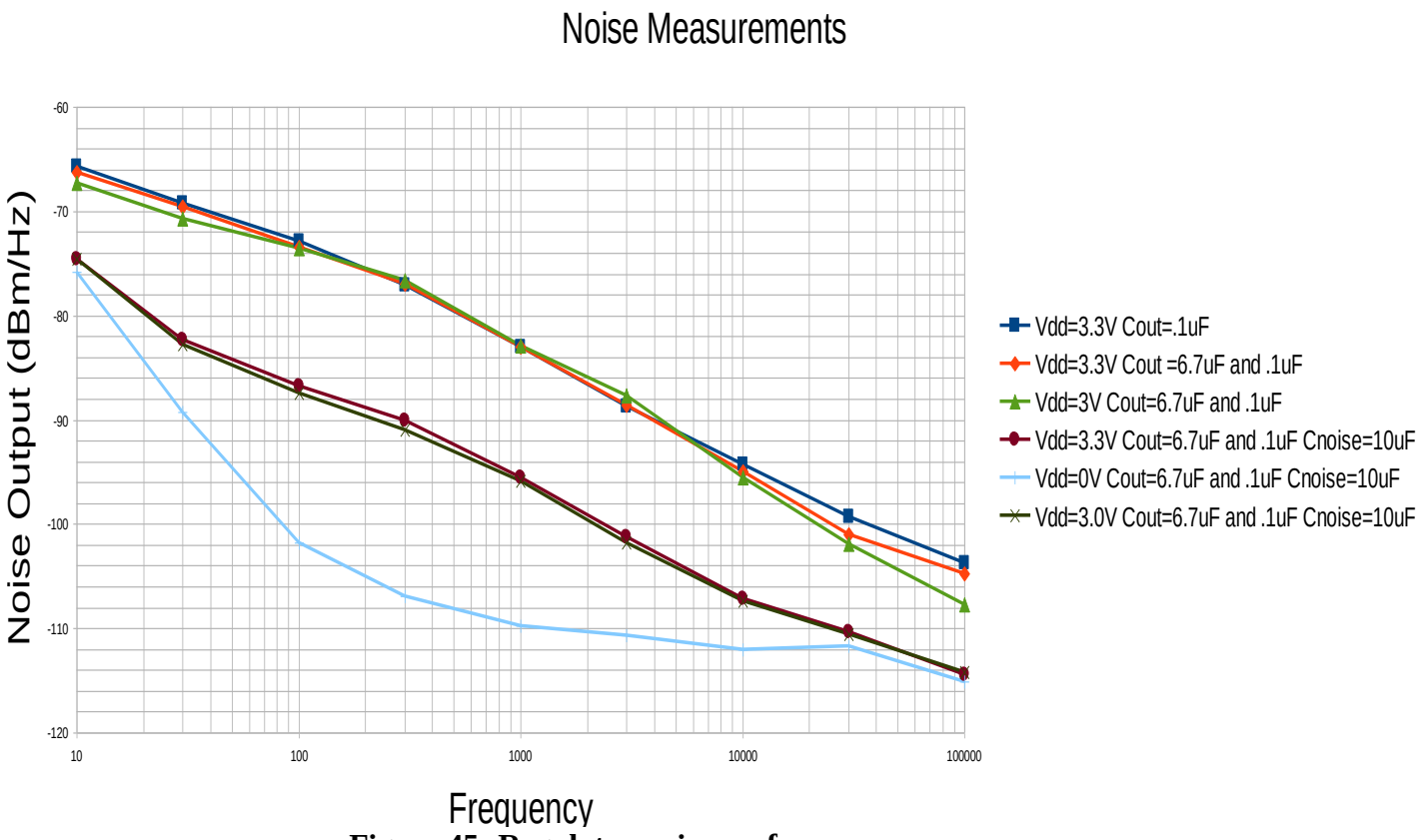

Figure 45: Regulator noise performance.

The output noise of the regulator with different capacitive bypassing is displayed. The cyan plot shows the noise limit of the spectrum analyzer, as the regulator was unpowered in this case. The blue line shows the noise level with a minimum 0.1µF output bypass capacitance. The next two plots show little improvement by adding a 6.7 µF to the output (red) and reducing the input voltage level (green). The final to plots (dark green and brown) where achieved by adding a capacitor to ground at the output of the band gap reference as shown in Figure 46.

We accomplished this by using an IC probe to attach to a pad on-chip. These two plots (dark green 3.0V V_{in} and brown 3.3V V_{in}) with the C_{noise} capacitor show very similar results and reduce the noise level by 13dB.

All of the points where taken on a HP 3588A Spectrum analyzer, using the setup shown in Figure 47. A pre-amplifier is used to increase the noise level so that the points can be read above the noise levels of the spectrum analyzer. The noise levels shown are adjusted for the preamps gain.

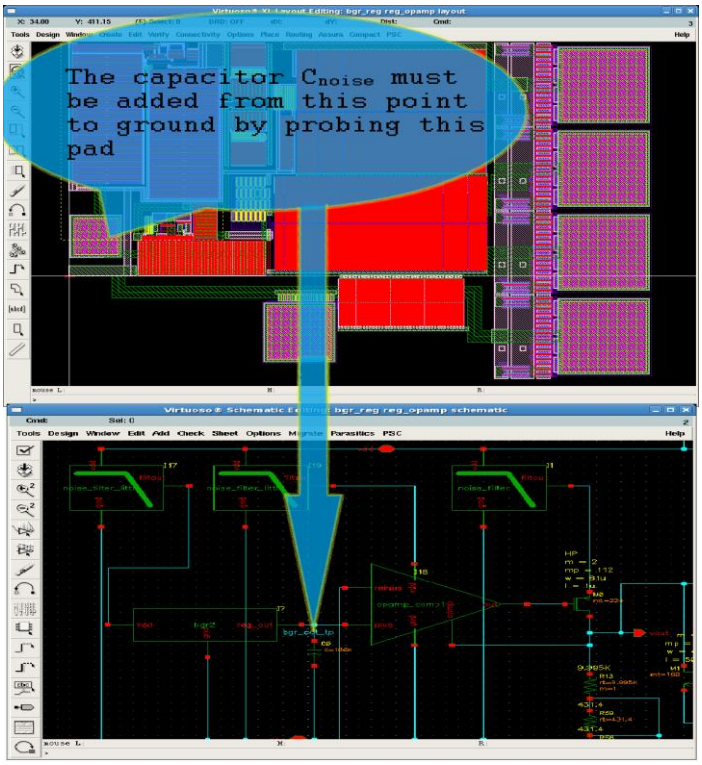

Figure 46: Image shows that the capacitor Cnoise must be added by probing a probe pad. This will quiet the noise being produced by the BGR

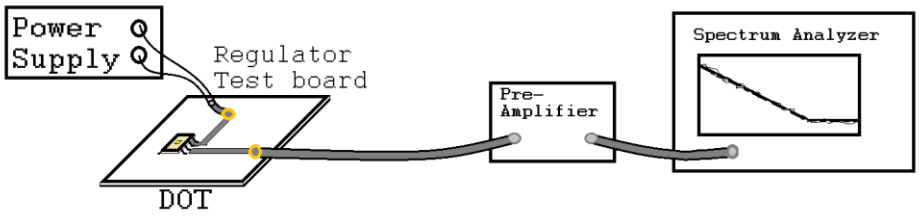

Figure 47: Test setup for noise measurements.

3.3 Supply Noise Reduction

Since the purpose of the regulator is to suppress the noise on the supply, a supply noise reduction analysis is done. Figure 48-49 show the S_{21} plot of the regulator from input to output.

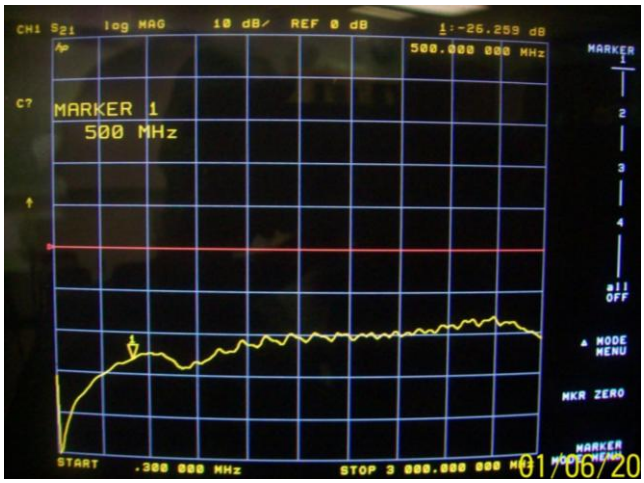

Figure 48: Ripple rejection with a 50 Ω load.

In Figure 48, the output of the regulator was loaded with a 50 Ω resistor. The ripple rejection is 25dB @ 500MHz. More importantly, the rejection is 21dB @ 1.5GHz and 19dB @ 2.4GHz.

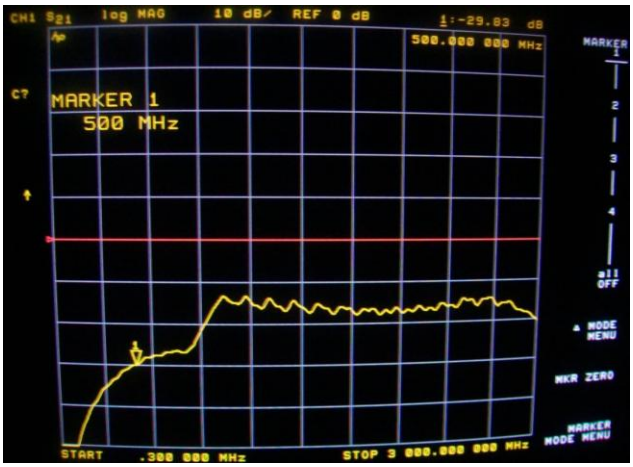

Figure 49: Ripple rejection with no load.

In Figure 49, the output of the regulator was left un-loaded. The ripple rejection is 29.8dB @ 500MHz. In the desired S-band frequency range, the rejection is found to be 16dB @ 1.5GHz and 15dB @ 2.4GHz. The loaded levels are lower in the upper frequencies due to the voltage divider formed between the large C_{ds} Capacitors (shown in Figure 50) and the load resistor. A comparison of this regulator's PSRR and Gupta, May 2005 [6] is shown in Table 2.

Table 2: Benchmark for PSRR

Research	@ 10MHz	@500MHz	@2.4GHz
Gupta, May 2005 [6]	40dB	Not reported	Not reported
PSRR (KSU Regulator)	>50dB	25dB	19dB

These measurements were found to be about 10dB less than the expected values because of noise sneak paths through the output's supply filter stage that were not fully modeled in simulation.

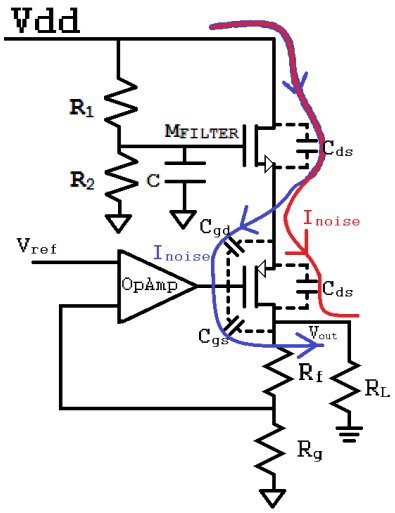

Figure 50: The output of the regulator and the noise sneak paths.

The setup for these tests include an RF DC coupler, a HP E3616A power supply, Agilent 34405A DMM, and the HP 8753C network analyzer. The test setup is shown in Figure 51.

Figure 51: Test setup for ripple rejection plots.

3.4 Temperature Characterization

A very important specification in linear regulators is the resistance to voltage change over changing temperature. BGR regulators are often constructed with temperature compensation [15]. Below are three plots that show the temperature characteristics of the tested regulator. Since the BGR was designed to have an output voltage that is resilient to changes in temperature, the regulator also takes on this property. Figure 52 shows the regulation at elevated temperatures. Figure 53 shows a composite of high temperature measurements with a decreasing temperature curve. Finally, Figure 54 shows a plot of the regulators trend with increasing input voltage at a temperature of 80K.

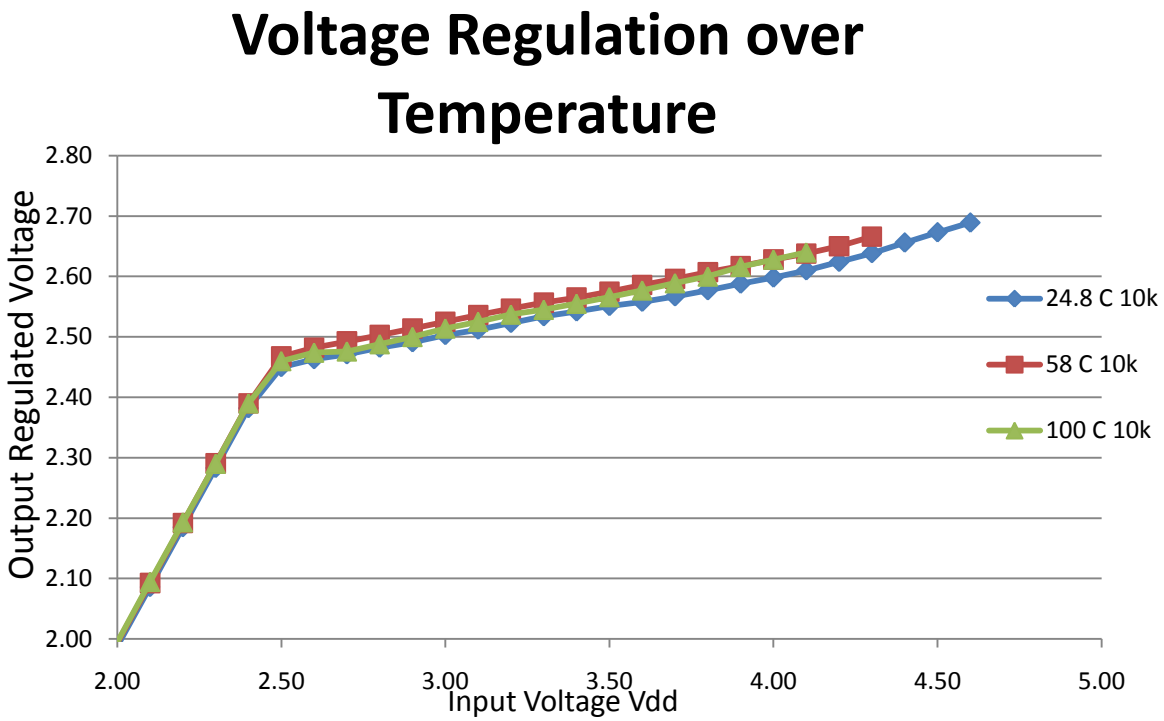

Figure 52: Line regulation over elevated temperatures sweeping the input voltage.

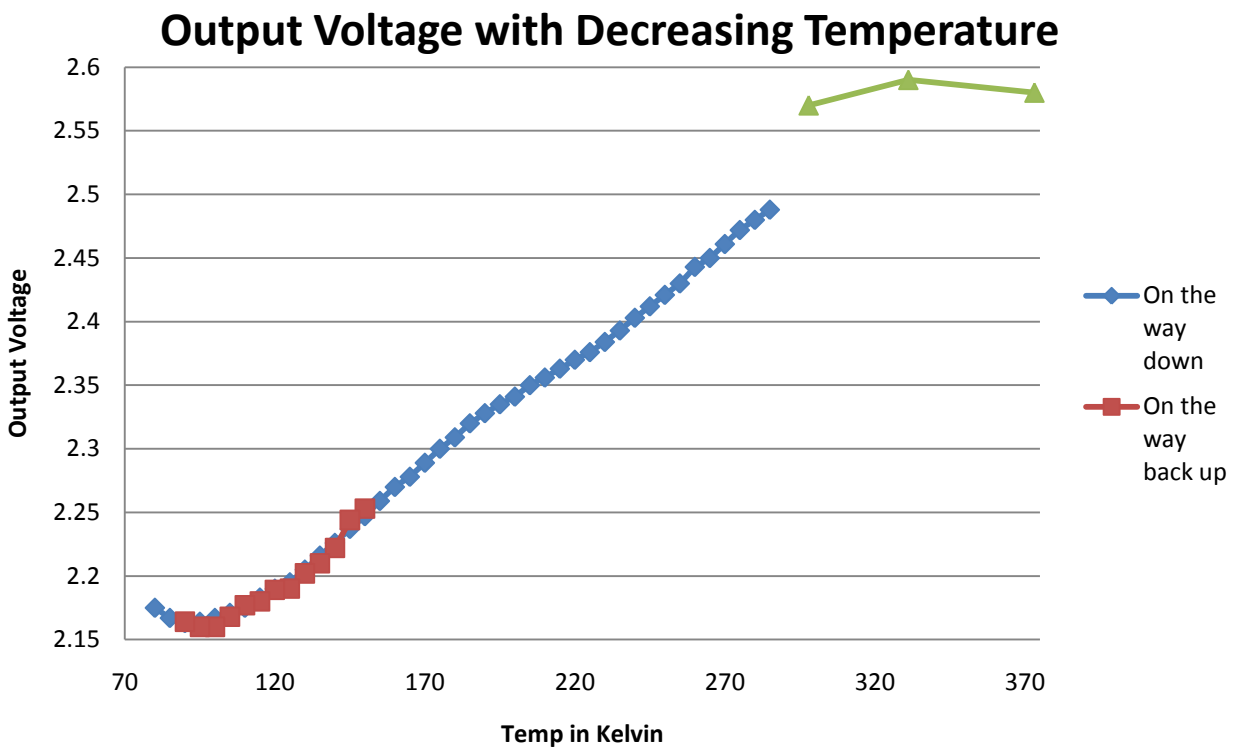

Figure 53: Temperature curve composite.

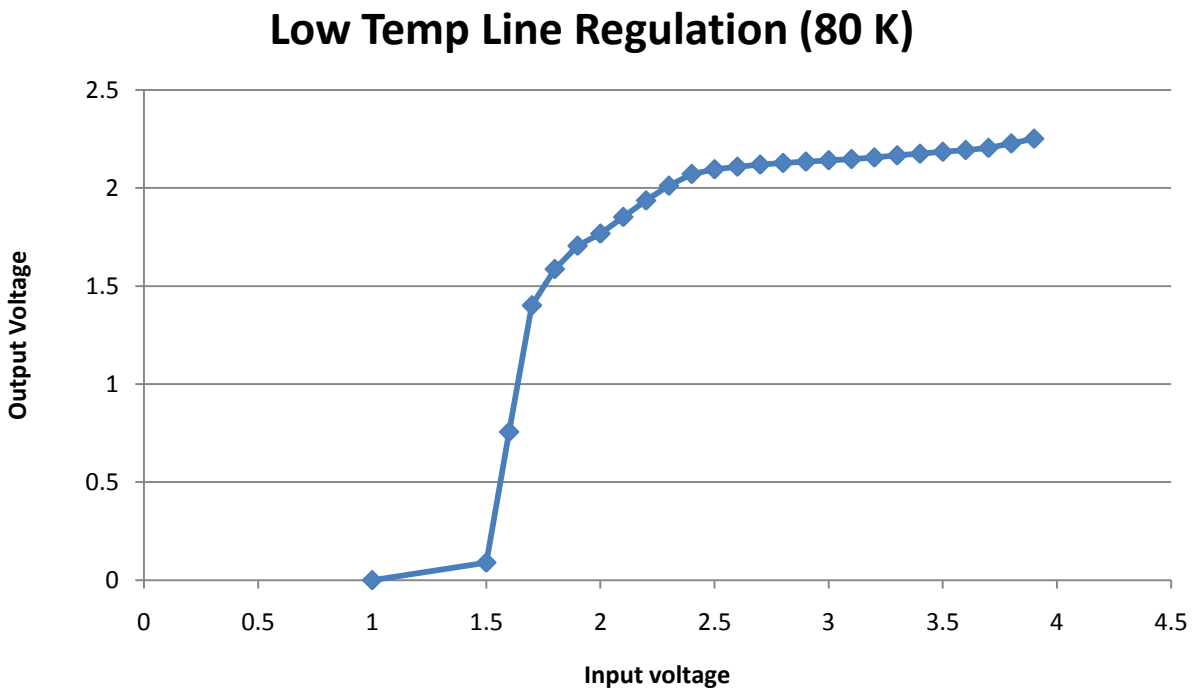

Figure 54: Plot of low temperature line regulation.

Chapter 4 - Synthesizer/VCO

A synthesizer has many different sensitive areas where noise can become an issue. Reference [3] shows how the charge pump can cause phase noise in synthesizers. In addition, in sections 1.1 and 1.2.1 we discussed how power amplifiers and digital frequency dividers contribute to the noise problem. Noise on the supply causes oscillators to have jitter on the output [20], [21]. The analog oscillator is not only affected by these deterministic noise sources on the supply. Like the charge pump, the oscillator affects the noise level with the random noise in its own devices.

Tail current biasing is a very common way to bias and analog oscillator in a synthesizer system. As suggested by Thomas Lee in [22] the tail current approach is not the ideal bias solution to produce an oscillator with low phase noise. In the paper, he postulates that the tail current injects a noise voltage into the oscillator. He also demonstrates a few simulations that indicate that using both N and P FET cross coupled FETs will reduce the phase noise by making the device (or Waveform) more symmetric.

4.1 Topology Choices

When considering the oscillator the first order of business is picking a topology. There are many things to consider on the subject of topology [23]. The first group presented will be the cross-coupled case. The cross-coupled FET oscillator is the most common in integrated circuit synthesizers systems. This is probably why there are so many variations on this design. I will take you through them and present the issues with each. The other topology I would like to present is the Colpitts, which is normally a single ended structure. The Colpitts oscillator is a classic design and may be a greatly overlooked solution to the topology question [23]. The Colpitts oscillator can also be constructed in a way that allows for a differential output.

4.1.1 Cross Coupled

The cross-coupled oscillator is used in numerous designs. The oscillator shown in Figure 55 is the simplest topology of this cross-coupled group. This oscillator uses cross-coupled NFETS as well as a NFET tail current source. This current source is configured in the classic current mirror configuration. As discussed in section 1.1.2 the NFETS have poor noise

performance. The tail current on this design is injecting this noise in to the oscillator's core. The whole structure could be made from the PFETs that have better noise performance.

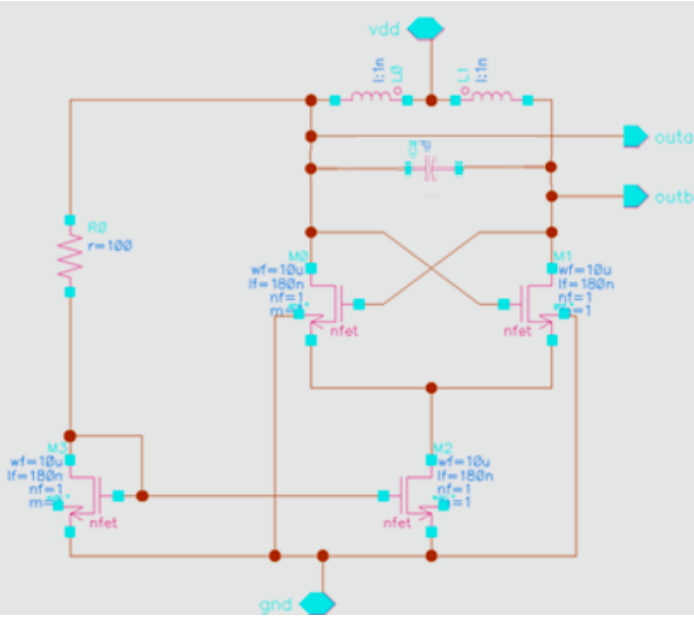

Figure 55: Cross-coupled NFET VCO topology.

Figure 56 shows how the oscillator can be configured in the complimentary cross-coupled configuration. Reference [22] shows that the addition of the cross-coupled PFETs makes the waveform more symmetric and therefore improves the phase noise. However, the addition of more devices into this configuration along with using a tail current source may not produce much improvement in performance due to the additional noise sources.

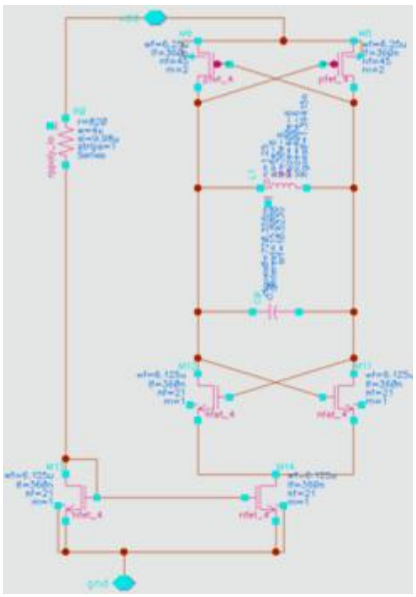

Figure 56: Complimentary cross-coupled topology with NFET tail current.

Figure 57 shows the same configuration as above but with a PFET current source. The 1/f device noise from the PFET is still being injected into the oscillator core. However, this design may show an improvement due to PFETs having better 1/f performance [1].

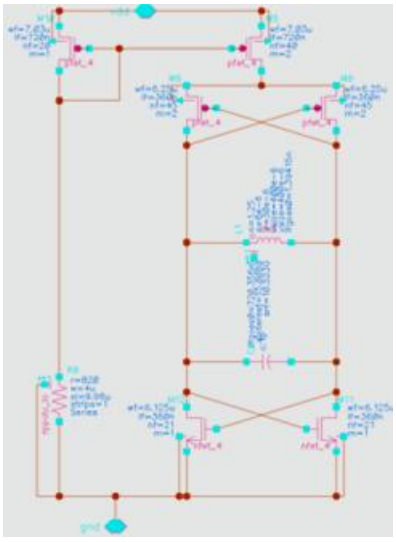

Figure 57: Complimentary cross-coupled topology with PFET tail current.

Figure 58 shows alternate biasing of a cross-coupled NFET configuration. We suggest that this configuration may have better performance than the oscillators discussed previously in this subsection. This configuration has fewer devices that produce 1/f noise. In addition the use

of the tail current mirror is replaced with a resistor bias and tail resistors. This biasing change eliminates the current mirrors injection of 1/f noise into the oscillator core.

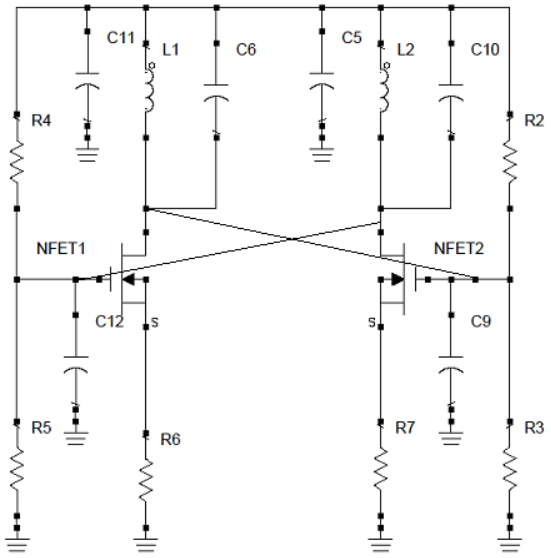

Figure 58: Proposed alternate biased cross-coupled design.

4.1.2 Differential Colpitts Oscillator

Figure 59 shows the classic design of a Colpitts Oscillator. This design does not use a tail current that would inject noise but uses a resistor bias and a capacitive feedback.

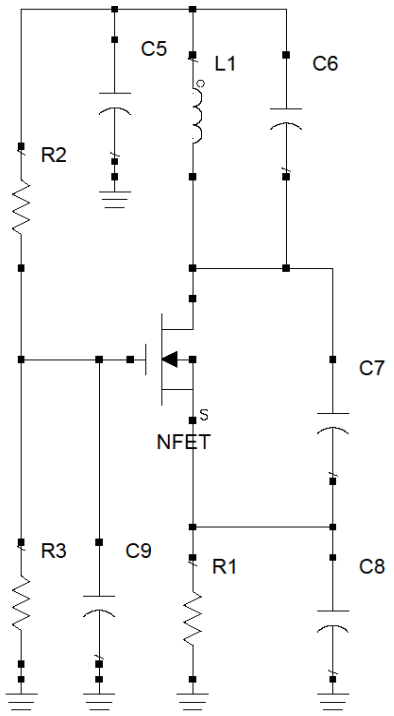

Figure 59: Above is the schematic of the traditional Colpitts oscillator.

In a synthesizer design, it is sometimes necessary to have a differential output to the oscillator. These outputs are used for I and Q modulators. Figure 60 shows a proposed differential Colpitts oscillator with a capacitive tie to combine the differential legs.

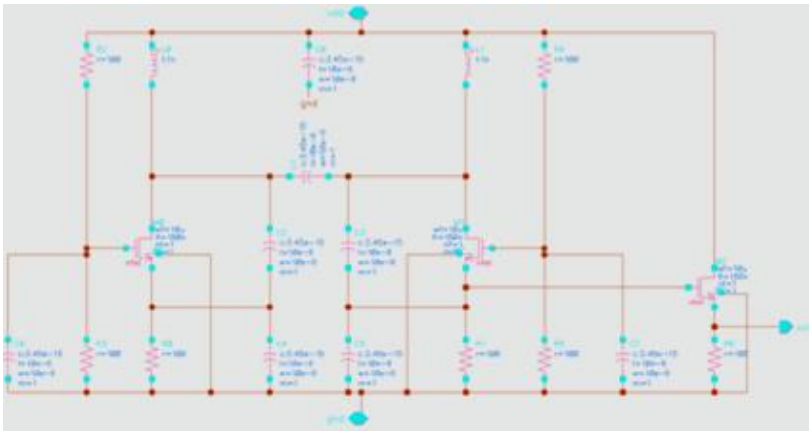

Figure 60: The schematic pictured above is the proposed differential Colpitts oscillator.

4.1.3 Preliminary Oscillator Explorations

The Colpitts oscillator is the classic oscillator design. In the previous section, the oscillators suffer from noise injection issues. It is suggested by [22] that the Colpitts will not suffer from the same problems. In the cross-coupled oscillators, the noise is injected at the high to low transitions of the output waveform. The impulse sensitivity function (ISF) discussed in [22] indicates that the preferred location of noise injection is at the peaks of the oscillator's waveform. Figure 61 illustrates this desired behavior.

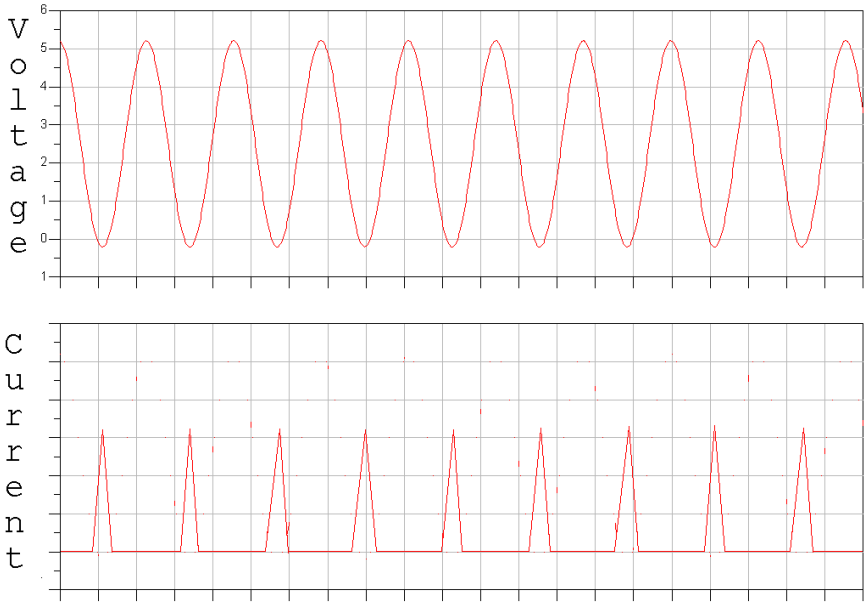

Figure 61: The output voltage as compared with the Current through the drain of the transistor [22].

The spikes in the current waveform occurring on the troughs or the peaks of the voltage waveform reduce the effect of noise on the phase. This effect is reduced because the transition from high to low is not does not experience this spike in noise [22].

A test of this theory a simulation was conducted using the set-up schematic shown in Figure 62.

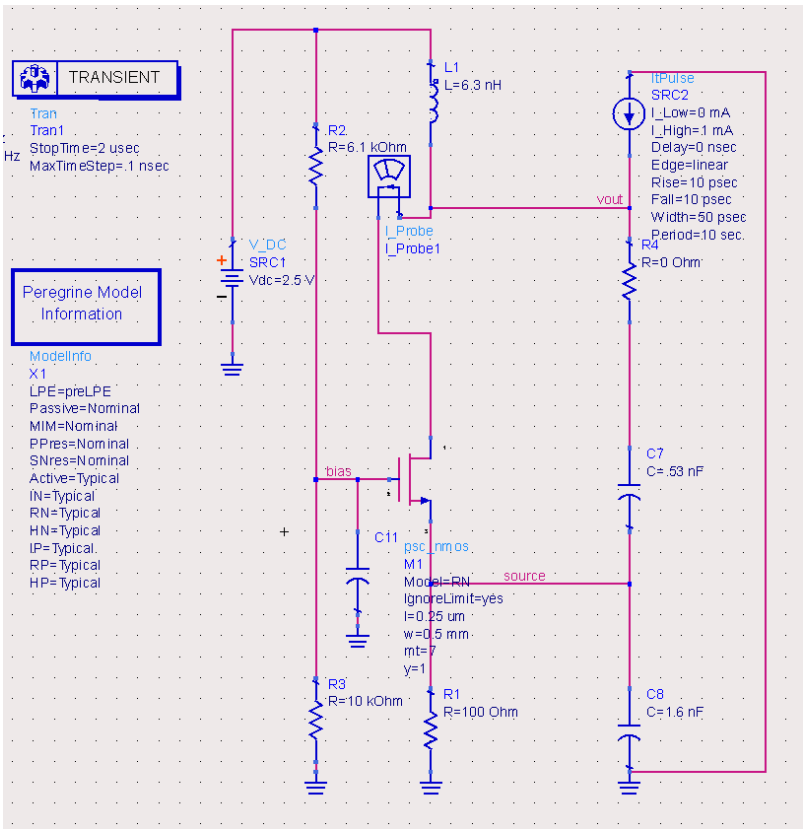

Figure 62: ADS schematic of Colpitts Oscillator

In the simulation, the current through the FET was sampled as well as the output voltage. In [22] it was suggested that the current spikes occur at the desired locations. However, the following Figure 63 shows an interesting discrepancy with this theory.

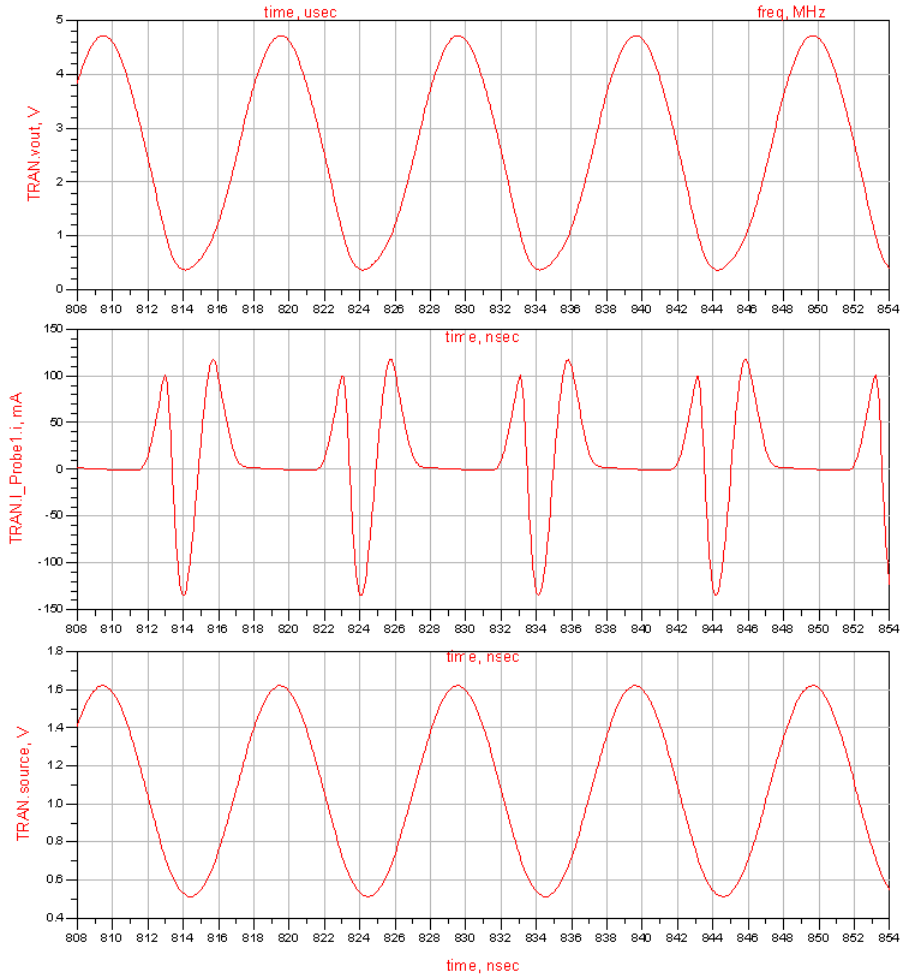

Figure 63: Output voltage at source and drain and current simulations for Colpitts Oscillator.

This simulation shows a current spike that starts to go positive. Then the FET of the oscillator switches the source and drain as the voltage on the drain drops below the gate voltage resulting in a negative current spike. This is not desired because the peak of the spike that is positive overlaps the transition point of the output voltage waveform. This is suggested by [22] to produce more phase noise in the oscillator. More investigation of how to create a more ideal narrow current spike is needed.

Chapter 5 - Conclusions

The voltage regulator is an effective way to improve the performance of a synthesizer system. By rejecting the interference through the supply line, the sensitive charge pump and oscillator will improve in performance. The regulator performed as well as or exceeded other regulators in the literature [6], [7], and [8]. The regulator was characterized and performed well into the S-band region where modern day synthesizers operate.

Integrated circuits designed to work into S-band have coupling issues. These issues can be quantified and reduced by proper layout techniques. Proper routing of traces and shielding techniques can effectively reduce the spread of unwanted noise.

The device noise can be reduced in sensitive areas by choosing proper devices, biasing, and topology. As shown in section 3.2 the noise can also be reduced by adding a capacitor at the output of the BGR.

VCOs have many different topologies. Discovering the VCO with the best performance will be the main continuation of this work. As suggested in section 4.1.3 the best approach in reducing the phase noise of oscillators may be to optimize the current waveforms of the Colpitts oscillator.

Chapter 6 - Future Work

A new regulator was fabricated in the Jazz Semiconductor process. The new regulator is expected to have better performance in PSRR as well as device noise do to increases in on-chip capacitances and use of improved diodes. This Jazz regulator needs to be tested and characterized.

All of the types of VCO's discussed above should be fabricated and tested to validate the theories discussed. This research on VCO's could be a useful for RFIC designers in the future. Simulation is not sufficient. This comparative analysis will need to be tested in the lab. The Jazz VCO fabrication run should include all VCO's in the following table.

Table 3: Future Jazz VCO Fabrication.

#	Topology	Biasing
1	Standard NFET cross-coupled	NFET tail current
2	Complimentary cross-coupled	NFET tail current
3	Complimentary cross-coupled	PFET tail current
4	N or PFET cross-coupled	Resistor biased and tail resistor
5	Single ended Colpitts Oscillator	Resistor biased and tail resistor
6	Differential Colpitts Osillator	Resistor biased and tail resistor

The #1 standard NFET cross-coupled design will provide a phase noise base line. The #2 complimentary cross-coupled design will investigate the symmetric waveform improvement of phase noise over the base line. Number 3 Complimentary cross-coupled design is intended to be compared to number 2 to illustrate the difference between using a NFET vs. a PFET tail current. The # 4 design is to be compared with the phase noise of the first three cross-coupled versions. Finally, #5 and #6 are an experiment to determine if the Colpitts may be a viable option. In addition, #5 and #6 are suggested to have the best phase noise performance [22], but the waveform issues found in section 4.1.3 must be addressed first.

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