ULTRA-LOW POWER ENERGY HARVESTING WIRELESS SENSOR NETWORK DESIGN

by

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Abstract

This thesis presents an energy harvesting wireless sensor network (EHWSN) architecture customized for use within a space suit. The contribution of this research spans both physical (PHY) layer energy harvesting transceiver design and appropriate medium access control (MAC) layer solutions. The EHWSN architecture consists of a star topology with two types of transceiver nodes: a powered Gateway Radio (GR) node and multiple energy harvesting (EH) Bio-Sensor Radio (BSR) nodes. A GR node works as a central controller to receive data from BSR nodes and manages the EHWSN via command packets; low power BSR nodes work to obtain biological signals, packetize the data and transmit it to the GR node.

To demonstrate the feasibility of an EHWSN at the PHY layer, a representative BSR node is designed and implemented. The BSR node is powered by a thermal energy harvesting system (TEHS) which exploits the difference between the temperatures of a space suit's cooling garment and the astronaut's body. It is shown that through appropriate control of the duty-cycle in transmission and receiving modes, it is possible for the transceiver to operate with less than 1mW power generated by the TEHS. A super capacitor, energy storage of TEHS, acts as an energy buffer between TEHS and power consuming units (processing units and transceiver radio). The super capacitor charges when a BSR node is in sleep mode and discharges when the node is active. The node switches from sleep mode to active mode whenever the super capacitor is fully charged. A voltage level monitor detects the system's energy level by measuring voltage across the super capacitor.

Since the power generated by the TEHS is extremely low(less than 1mW) and a BSR node consumes relatively high power (approximately 250mW) during active mode, a BSR node must work under an extremely low duty cycle (approximately 0.4%). This ultra-low duty cycle complicates MAC layer design because a BSR node must sleep for more than 99.6% of overall operation time. Another challenge for MAC layer design is the inability to predict when the BSR node awakens from sleep mode due to unpredictability of the harvested energy. Therefore, two feasible MAC layer designs, CSA (carrier sense ALOHA based)-MAC and GRI (gateway radio initialized)-MAC, are proposed in this thesis.

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Acknowledgements

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Chapter 1 - Introduction

1.1 Project Background

The physical and mental health of astronauts on a space mission is often challenged by the harsh operating environment. Various devices have been developed to track and predict astronaut's health status in order to both maximize their working efficiency as well as to ensure their safety [1]. Research for this thesis correlates to the NASA EPSCoR project (NNX11AM05A) whose primary goal is to study the feasibility and implement a customized low power and low data rate wireless sensor network (WSN) for use inside a space suit for biomedical application. The project is divided into five tasks.

Task 1 determines physiological signals that can predict astronaut's fatigue during space exploration mission and develop associated sensors to detect those physiological signals. Task 1 is a joint effort by Kinesiology department and ECE department to develop and utilize a collection of field tests in the form of an obstacle course in which individual tests mimic typical EVAs [2]. Field tasks include lifting weighted boxes, climbing ladders and stairs, and transporting weighted objects in a wheelbarrow (see Figure 1-1). For this task effort, commercial biomedical sensors (i.e., Delsys Trigno Electromyograph [3] and 3-aixs accelerometer) were placed on meaningful spots on the body (see Figure 1-2) to acquire data for further analysis.

Task 2 mainly focuses on testing and simulating the radio environment within a space suit. Associated tasks include measuring path loss inside a space suit with different transmission frequency range (315M, 433M, and 916M) and finding capable energy harvesting technologies that can be used inside the space suit to provide electrical energy to the transceiver node designed in Task 3.

Task3 is to develop an ultra-low power energy harvesting wireless sensor network (EHWSN) to obtain the biological signals identified by Task1 and transmit the data to space suit backpack

computer for further analysis. Besides, energy harvesting (EH) transceiver node used in the EHWSN is also designed in this task.

Task 4 is to create a compact package for the transceiver node designed in Task 3 and bio-sensors designed in Task 1.

Task 5 mainly focuses on public outreach.

Figure 1-1: Field Tasks [2]

Figure 1-2: Using commercial sensors to obtain EMG signals and ACC signals. [4]

1.2 Thesis Goals

The work in this thesis is primarily related to Task 3 of the project. The goals of this research include designing an energy harvesting system (EHS) which can be used within a spacesuit, developing an energy harvesting (EH) transceiver node which can work with an extremely low duty cycle ($\approx 0.4\%$), and presenting a feasible medium access control (MAC) layer design.

1.3 Understanding EHWSN

A wireless sensor network (WSN) is comprised of nodes that have processing units, sensors, antenna, power source, and radio frequency integrated circuit (RFIC) as radio transceivers [14]. WSN typically use battery power as a power source while EHWSN use an energy harvesting system (EHS) as a power source, converting energy from the environment to electrical energy to power the sensor nodes. Energy from environment can be converted into electrical energy using various energy harvesting (EH) techniques (see Table1-1). For example, photovoltaic cell that converts solar energy to electrical energy is most widely used in our daily life. Solar keyboard and solar calculator are two familiar applications of photovoltaic cell. Although the output power from the EHS is extremely low (uW~mW) and various over time, with the development of ultra low power electronics and energy storage techniques (e.g. low leakage super capacitor), EHWSN becomes reality and attracts more and more researchers' attentions [5] [6] [7]. However, according to literature, there are very few MAC layer designs which we can find suitable for the EHWSN especially for the piezoelectric or thermoelectric techniques based EHWSN.

EHWSN is used for this thesis because 1) batteries are forbidden inside space suits because of safety concerns, thereby preventing use of battery based WSN, 2) EHS does not require regular replacement, thereby reducing nodes' maintenance tasks, and 3) EHS is more environmentally friendly compared to batteries [6][8]. Preliminary study in [9] finds that thermoelectric generation is the most suitable EH method for using inside a spacesuit compared with other viable methods (piezoelectric and automatic watches), although the method has low output voltage ($\approx 100mV$) (solution for this drawback is shown in Section 2.2.3).

Table 1-1: Energy harvesting techniques and harvested power [28]

Harvesting techniques	Source	Efficiency	Harvested power
Photovoltaic	Ambient light	5 ~ 30%	$10\ \mathrm{uW/cm^2}$~$10\ \mathrm{mW/cm^2}$
Piezoelectric	Vibration/motion	1 ~ 10%	$4\ \mathrm{uW/cm^2}$~$100\ \mathrm{uW/cm^2}$
Thermoelectric	Thermal energy (human)	0.1~3%	$30\ \mathrm{uW/cm^2}$
Antennas	RF (cell phone)	50 %	$0.1\ \mathrm{uW/cm^2}$

1.4 EHWSN Design Overview

The EHWSN designed in this thesis follows a star topology, in which a gateway radio (GR) works as central node and multiple bio-sensors radio (BSR) work as sub nodes (see Figure 1-3). A subtle difference from traditional EHWSN in which all the nodes are EH nodes, is that the GR node in our EHWSN is powered by the backpack battery of space suit and thereby not energy constrained. Since BSR nodes powered by EHS are extremely power constrained, one major goal of our MAC layer design is to shift power consumption pressure from BSR nodes to GR node as much as possible, which is different from the constraints on existing MAC layer designs.

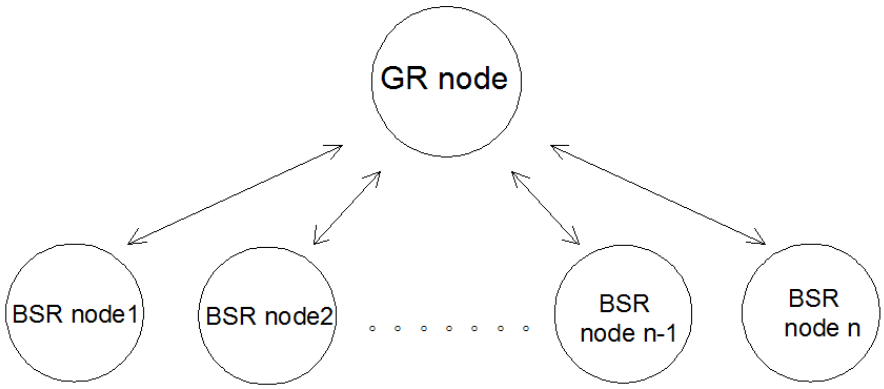

Figure 1-3: Overview of a Star Topology Network

1.5 Thesis Contributions and Organization

This thesis has following contributions:

First, we design a feasible thermal energy harvesting system (TEHS) that can be used within a spacesuit. Since a thermal electric generator (TEG) needs a temperature differential to generate electrical power, one approach is to exploit the difference between astronaut's body temperature and the cooling garment that is worn. However, the key challenge is to ensure that there is adequate physical contact between the TEG terminals and the body/cooling garment. A creative solution to this problem has been designed and implemented as discussed in Section 2.2.4.

Second, we design and implement a transceiver node that can operate in energy constrained environments. Specifically, the transceiver node works with extremely low duty cycle ($\approx$ 0.4%) by staying in sleep mode for most of the operational time. Analysis in Section 2.3.4 presents that power generates during sleep ($\approx$1mW) and power consumes ($\approx$250mW) during active modes. Both hardware and software design aspects of a transceiver node are discussed in Chapter 2. Additionally, at the end of Chapter 2, we illustrate a way to calculate maximum sampling rate which can be supported by our EH transceiver node. Based on the simulation results our system can achieve as high as 4.5Hz sampling rate by using current EH transceiver node, although the rate up to 300Hz may be feasible in the future as noted in the conclusion in section 4.2.

Finally, thanks to our special EHWSN construction with one power-unconstrained node (GR node) and multiple extremely power-constrained nodes (BSR nodes), very few existing media access control (MAC) layer design can be directly used in our system. Two feasible MAC layer designs CSA (carrier sense ALOHA based)-MAC and GRI (gateway radio initialized)-MAC, are present for our EHWSN in Chapter 3. Since the wake up time of EH transceiver node (BSR node) is unpredictable, both MAC layer designs are asynchronous designs in which BSR nodes have not to transmit data packets in fixed time slots. In CSA-MAC, if the channel is detected to be clear, a BSR node can transmit a packet whenever the node is ready and a GR node keep listening to the channel all the time. In GRI-MAC, a GR node always keeps transmitting beacons to inform an awake BSR node to transmit a data packet. Both MAC designs are modified from existing MAC layer designs to shift the power consumption pressure from power-constrained nodes (BSR node) to power-unconstrained node (GR node). The details of MAC layer design are provided in Chapter 3.

Chapter 2 - Physical (PHY) Layer

2.1 Overall Description of Hardware System

The hardware system of the energy harvesting wireless sensor network (EHWSN) studied in this thesis consists of two types of transceiver nodes: Bio-Sensor Radio (BSR) node and Gateway Radio (GR) node.

BSR Node

Multiple BSR nodes, which are placed on various locations on the human body to obtain different types of vital signals, are present in the EHWSN. After collecting biomedical signal, digitizing them, and converting the signals to data packets, BSR nodes send the packets to the GR node. A BSR node is comprised of two main parts (see Figure 2-1): a daughter board (DB) and K-State-NASA Body Area Network Development Board (KANDB), also known as the mother board (MB). Daughter board tasks include providing power to an entire BSR node, acquiring vital signals from human body, and being a part of the antenna as discussed in [9]; mother board tasks include converting and storing incoming data from daughter board, building and transmitting a data packet to GR node, managing power utilization, and responding to the incoming command packet from GR node. Major components on the BSR node are shown in Table 2-1.

Table 2-1: Part Name and Part Number

Daughter Board	
Part Name	**Part Number**
Accelerometer Sensor	ADXL330
Ultralow Voltage Step-up Converter	LTC3108
Super Capacitor	AVX BestCap (0050mF/5.5V)
Mother Board	
Part Name	**Part Number**
Field Programmable Gate Array (FPGA)	Actel-AGL1000
Microcontroller (uC)	ATmega 1284P
RF Micro-transceiver (RFIC)	K-State research IC

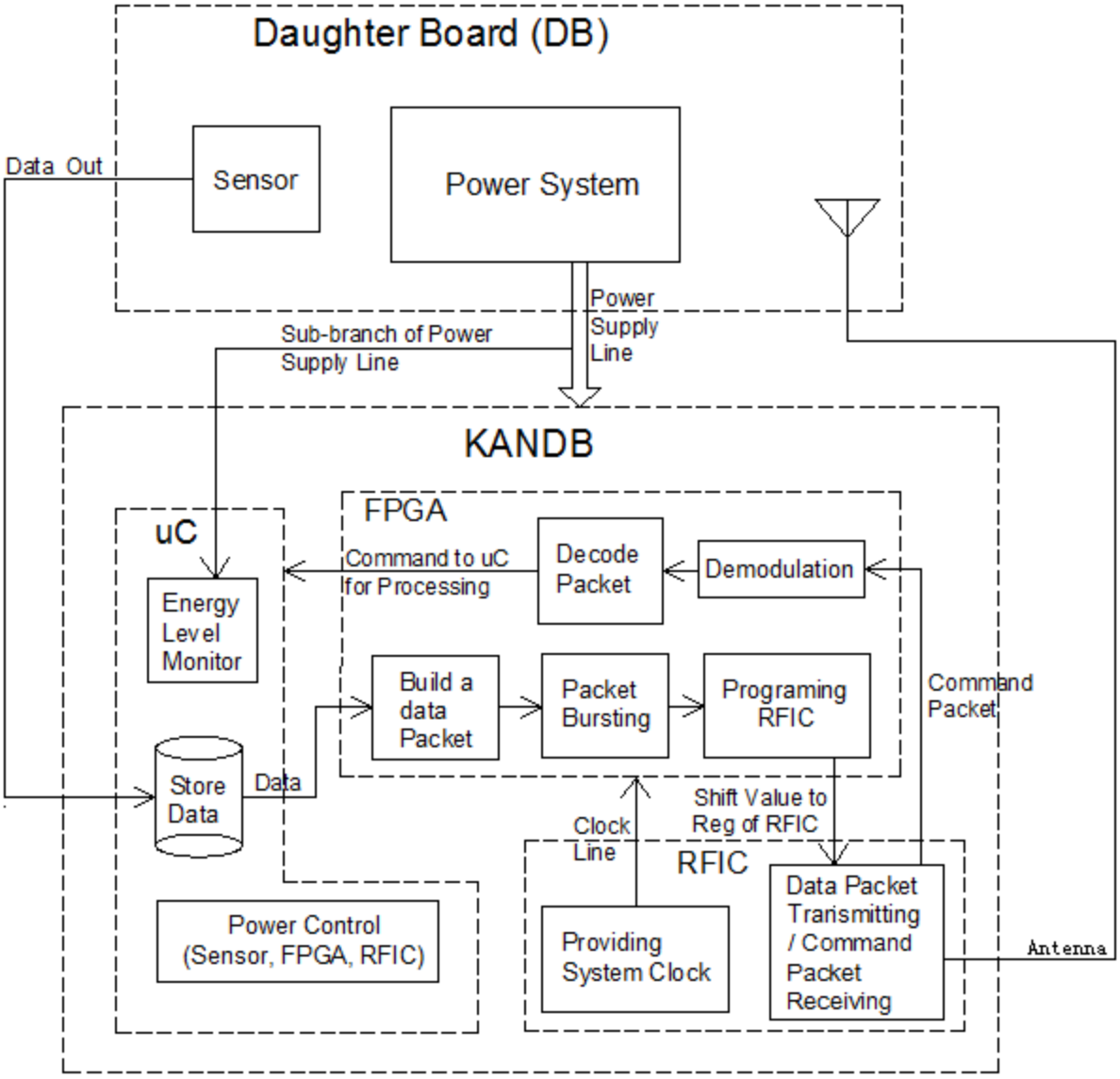

Figure 2-1: Block Diagram of a BSR Node

GR Node

Only one GR node is present in each EHWSN. The primary function of the GR node (see Figure 2-2) is to receive and decode data packets from BSR nodes and then transmit the data part to a computer in the backpack of a space suit. A GR node acts as the WSN organizer via command packets. It consists of a mother board only because the GR node is directly powered by the space suit's backpack and the node does not need to obtain vital signals.

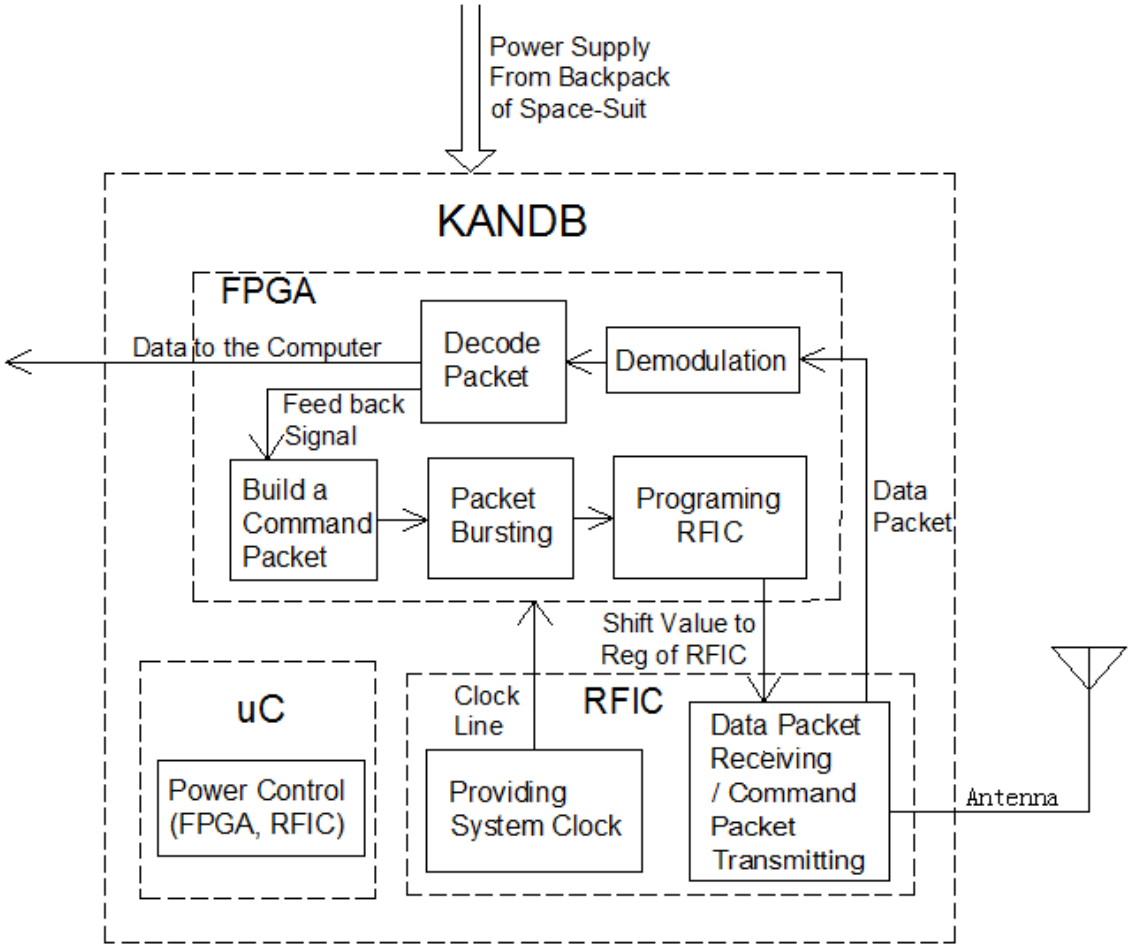

Figure 2-2: Block Diagram of a BSR Node

Since the BSR node and GR node have similar hardware and software design and EHWSN efficiency is limited by BSR node's performance, the remainder of this chapter primarily focuses on the BSR node. The daughter board is discussed first followed by a description of the mother board.

2.2 Daughter Board

2.2.1 Daughter Board Description

As mentioned, the daughter board has two main tasks: obtain vital signals from the human body using a built-in sensor and provide enough power to KANDB using the Energy Harvesting (EH) System. In addition, the daughter board contains antenna circuit as discussed in [9]. A top view of daughter board is shown in Figure 2-3 and a block diagram is shown in Figure2-4.

Figure 2-3: Daughter Board Top View

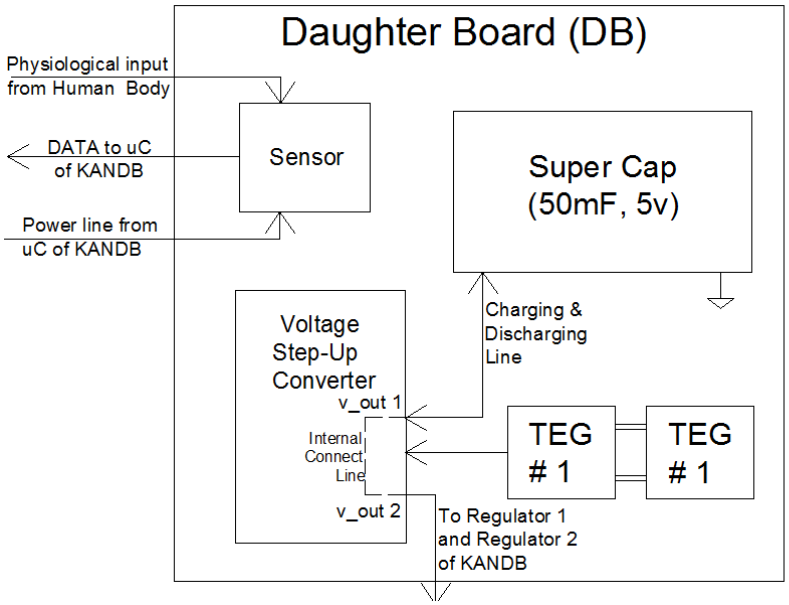

Figure 2-4: Daughter Board Block Diagram

2.2.2 Sensors

Various sensors are needed to monitor the health condition of an astronaut. Sensor types and their reasonable sampling rates are shown in Table 2-2.

Table 2-2: Sampling rate and number of sensors needed for an EHWSN within a spacesuit

Types of Sensor	Sampling Rate (samples/second)	units
Electromyography (EMG)	500	Multiple (TBD)
Electrocardiogram (ECG)	250	1
Respiration Rate Senor (RRS)	200	1
Pulse Oximeter (PO)	240	1
Accelerometer (ACC)	50 ~ 200	Multiple (TBD)

2.2.3 Thermal Energy Harvesting System

As shown in Figure 2-5, the Thermal Energy Harvesting System (TEHS), the core part of a daughter board, consists of a thermal electric generator (TEG), voltage step-up converter, and super cap (50mF).

When body temperature is applied to the "hot" side of a TEG and low temperature is applied to the "cold", the TEG can be used as an energy convertor to transfer thermal energy to electrical energy. Larger temperature difference between two sides of the TEG will produce higher output power [9]. Since the output voltage of TEGs is too low to be used (approximately 90 mV) to power the mother board directly, an ultralow-voltage step-up converter (UVSC) must be employed. UVSC can operate from inputs at least 20 mV and provide selectable output voltage (Vout) of 4.1V, or 5V [10]. The UVSC output (Vout1) connects with a super capacitor which acts as the energy storage element of this system. The energy condition is monitored by measuring voltage across the super capacitor using an A to D converter on the mother board and also within the UVSC on the daughter board. Different Vout settings have correspondingly different working ranges (see Table2-3). When Vout (voltage across the super capacitor) falls

below the working range, a switch in the UVSC turns off in order to shut down the mother board. For example, if Vout is set to 4.1V, the switch is turned off when voltage across the super capacitor falls below 3.7V. The switch is turned back on when voltage across the super capacitor rises above 3.8V. Therefore, voltage of the super capacitor must stay within working range to ensure smooth operation of the entire system. The mother board monitors the voltage to regulate the voltage and avoid this condition.

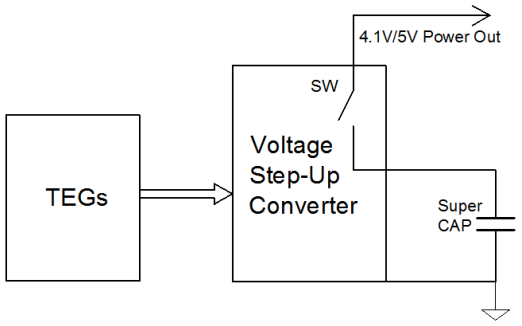

Figure 2-5: Thermal Energy Harvesting System

Table 2-3: Vout and its working range

Vout	Working Range
4.1V	3.8V ~ 4.1V
5.0V	4.6V ~ 5.0V

2.2.4 Testing Setup and Results

1. Charging Current with Power supply

Because duty cycle is limited by the ratio of charging current to the super capacitor with the mother board in sleep mode and discharging current consumed by mother board in active mode (see Section 2.3.4), charging current is the key parameter in order to evaluate the TEHS. To access the maximum charging current possibly with the UVSC, a power-supply with 100mV was used to mimic the TEG (see Figure 2-6). Because charging current is difficult to measure directly, the current was found by using Equation 2.2.4-1.

$$i = \frac{dv}{dt} \text{ C}, \qquad (2.2.4\text{-}1)$$

where v is the voltage across the super capacitor, t is the time of super capacitor charging, and C is the value of the super capacitor (50mF). After UVSC is powered by the power supply, super capacitor begins charging. t is recoded starting when 2V is observed at the testing point with steps of 0.2V and stops being recorded when the super capacitor is fully charged (5V). Measured results of v and t are shown in Figure 2-11. The charging current found using Equation 2.2.4-1 at different charging voltages is shown Figure 2-12.

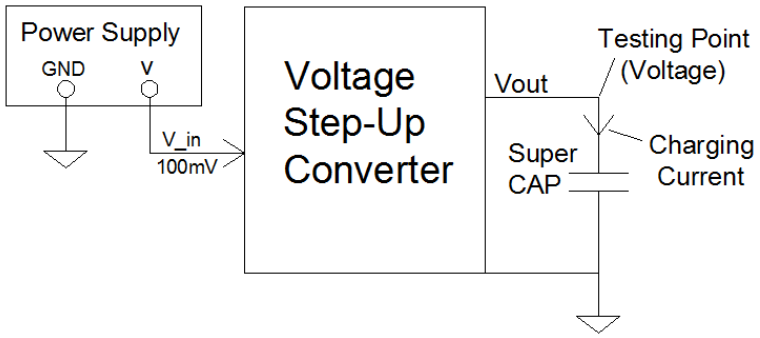

Figure 2-6: Measurement setup with power supply

2. Charging Current with TEGs

In this test, two paralleled TEGs are used as a power source to power the voltage step-up converter (see Figure 2-7). Since TEG needs temperature difference to create output power, the hot side of the TEG should touch the high temperature object (body skin) and the cold side should touch the low temperature object (ice bag). However, TEGs are located between mother board and daughter board (see Figure 2-8) made from thermal isolation material, thereby making TEGs impossible touching with high or low temperature object directly.

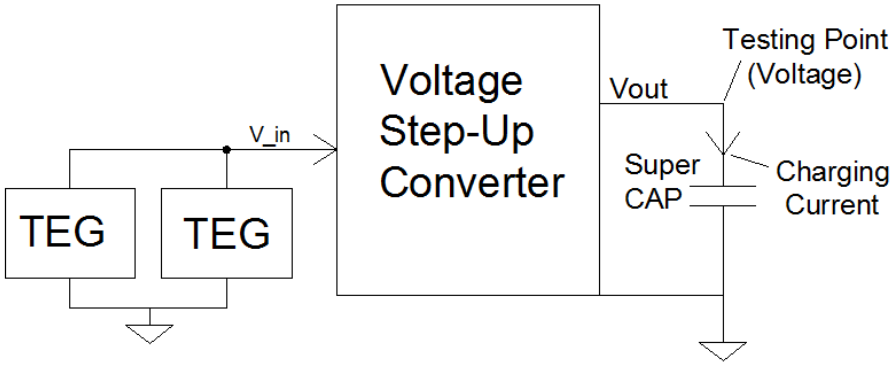

Figure 2-7: Measurement set up with TEGs

Figure 2-8: Combination of mother board and daughter board

A model designed to provide maximum thermal flow is shown in Figure 2-9. On one side, a 0.019 Inch thickness copper plate bent with U shape to bypass the mother board connects cold side of TEG with ice bag (25˚F); on the other side, thermal starting from arm (91˚F) going through another 0.076 Inch thickness copperplate and vias filled with thermal paste to the hot side of TEG. Since the copper is thermal conductor with very high thermal conductivity (401 W/(m K)) and is reasonable thick, very little temperature is changed when thermal flows through copperplate. A testing set up is shown in Figure 2-10. Measuring steps are similar as above and the measurement results are shown in Figure 2-11, and Figure 2-12. From the testing results we can see that, when testing with TEGs, it needs around 8 minutes to charge the super capacitor from 2V to 5V, and the average charging current is around 250uA. The testing with TEGs has better performance probably because the TEGs have lower output impedance than the power supply at the low voltages used.

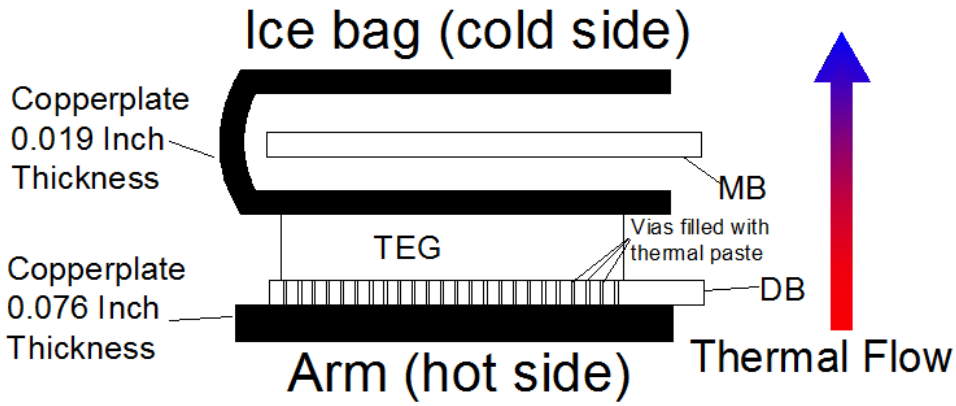

Figure 2-9: Testing set up model

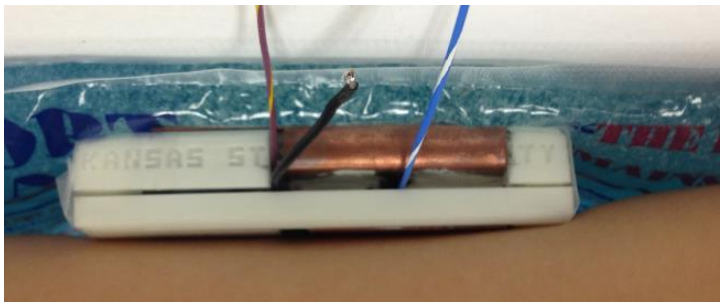

Figure 2-10: Real testing set up

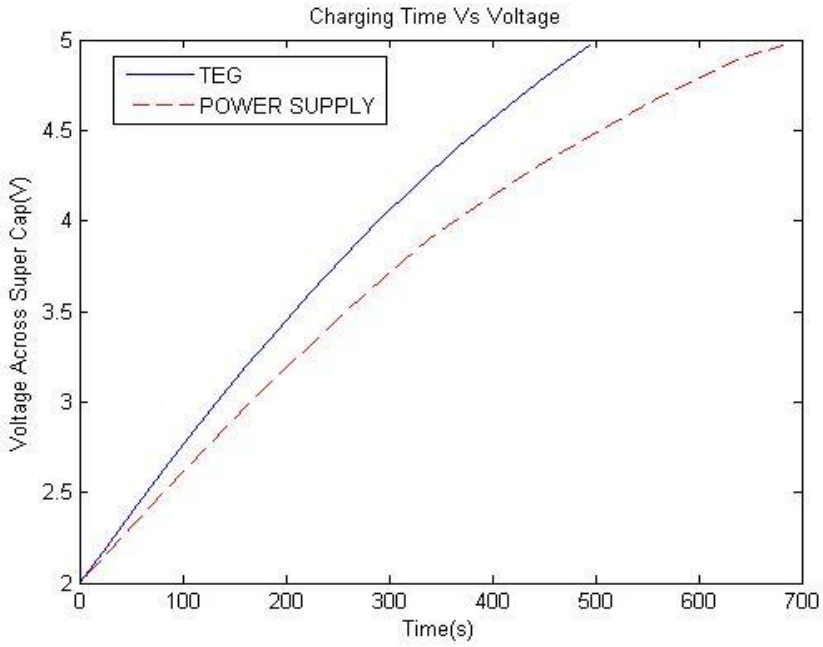

Figure 2-11: Charging time vs. Voltage across super capacitor (using 100mV power supply or TEG at input to step up converter)

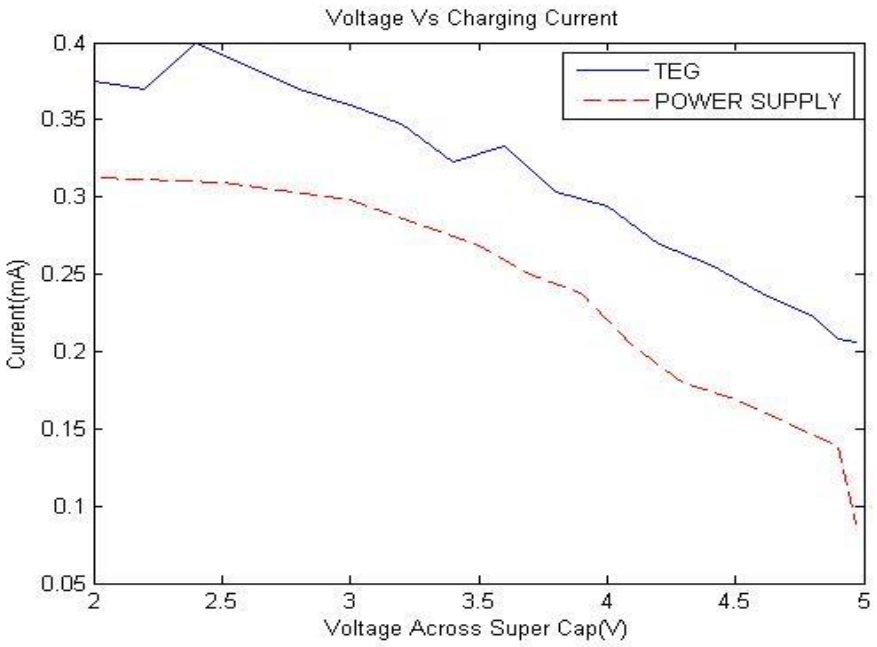

Figure 2-12: Charging current into super capacitor (using 100mV power supply vs. using TEGs)

3. TEHS Overall Output Power

To further assess the thermal energy harvesting output capabilities of the TEGs, a load resistor was placed across the super capacitor to determine average power available with 100% duty cycle operation (Figure 2-13). One of three conditions must happen when adjusting load resistor value: 1) the voltage across super capacitor decreases, indicating that load power is greater than TEHS overall output power; 2) the voltage increases, indicating that load power is less than TEHS overall output power; 3) the voltage remains stable, indicating that load power equals to TEHS overall output power. The resistor value which keeps the voltage remaining stable is recorded at Table 2-4 and the TEHS overall output power can be calculated by $P_{TEHS} = P_{load} = V^2/R_{load}$.

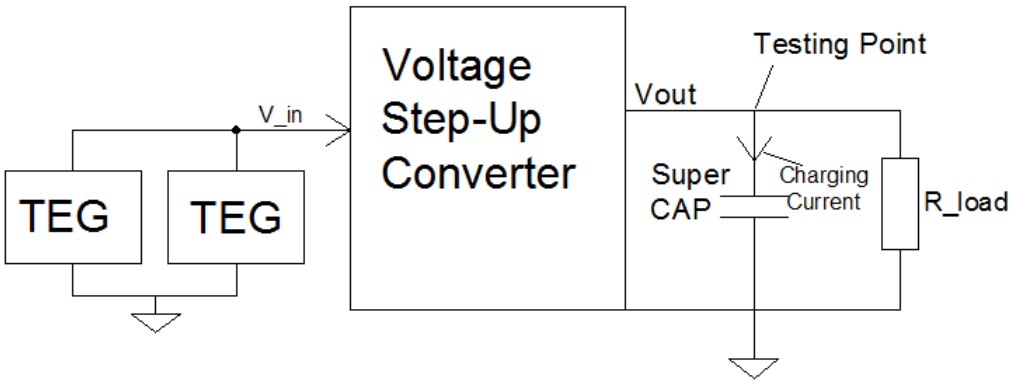

Figure 2-13: Output power measurement set up

Table 2-4: TEHS overall output power measurement

Load resistor (R_{load})	Voltage at testing point (V)	Load power (P_{load})	TEHS output power (P_{TEHS})
28kΩ	4.95V	0.87mW	0.87mW

Based on previous test results (with TEGs), the output power is about 0.94mW which is a little bit higher than P_{TEHS} measured in this test. Considering the temperature varies over time, this little error is acceptable. However, the temperature of ice bag is around -4℃, which must be lower than the temperature of cooling garment, so further test within a real space suit is needed to get more realistic P_{TEHS}.

2.3 K-State-NASA Body Area Network Development Board

2.3.1 Hardware Description of Mother Board

The mother board, shown in Figure2-14 (top view) and Figure2-15 (block diagram), mainly contains two regulators, a microcontroller (uC), a RFIC, and a field programmable gate array (FPGA).

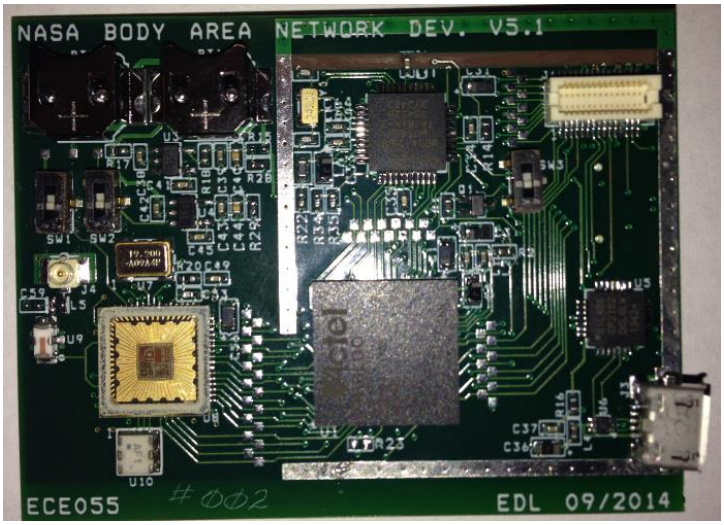

Figure 2-14: Top view of mother board

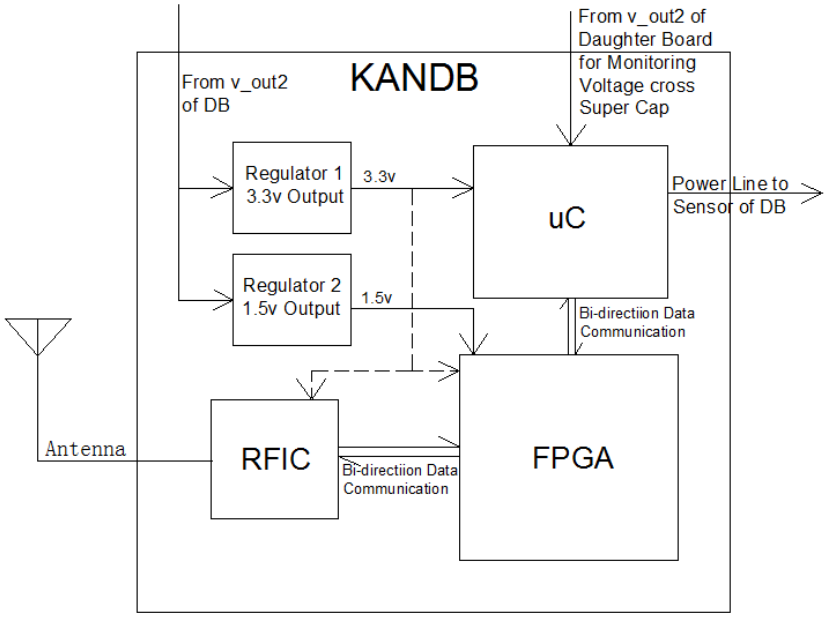

Figure 2-15: Block diagram of mother board

Regulators

Two regulators in the mother board work with input voltage range spans of 3.7V to 5.0V. Regulator 1 converts incoming voltage to 3.3 V to power the uC, the FPGA, and the RFIC. Regulator 2 converts incoming voltage to 1.5V to power the FPGA core logic. Both regulators contain an enable pin that can be used to activate or deactivate the output voltage. The 3.3V regulator is active constantly to power uC and draws a quiescent current of approximately 2uA [11]. The enable pin of the 1.5V regulator is controlled by the uC to power down the FPGA during sleep.

uC

Three main tasks of the uC include operating as a power manager, functioning as an analog to digital converter (ADC), and working as a data storage buffer. The uC can individually turn the power supply on or off for each component (Regulator2, RFIC, FPGA, and sensor) on a BSR node. When acting as a power manager, the uC places board in different types of modes (details in Section 2.3.2) according to the current energy level that it monitors by measuring the voltage across the super capacitor on the BSR daughter board. When acting as an ADC and a storage buffer, the uC converts input analog signals to 8-bit digital signals and then stores the digital signals in the data buffer, as described in Section 2.3.2.

FPGA

FPGA has four main functions: data processing, packet formation, bi-direction communication with uC, and RFIC programming to build or decode a data packet. See Section 2.3.2 for details for each function.

RFIC and Energy Detection

The RF integrated circuit (RFIC) is used to modulate and demodulate incoming data onto 433 MHz carrier. The FPGA controls the RFIC by setting value of the 61-bit programmable register (see Figure 2-17). When the RFIC is set to "receive" mode, three bits of the status register (see Figure 2-16) can be used as a received signal strength indicator (RSSI) to indicate the link quality.

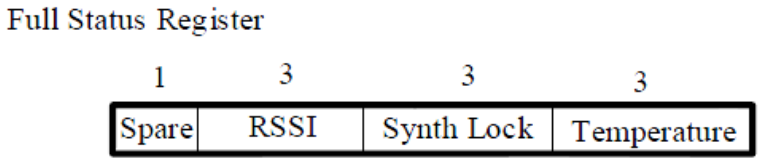

Figure 2-16: Status register fields

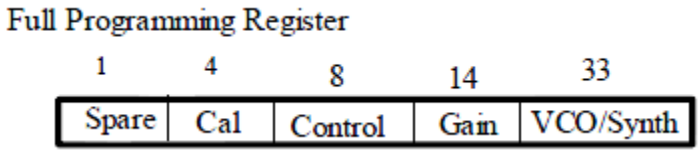

Figure 2-17: Programming register fields

2.3.2 Software Description of Mother Board

2.3.2.1 Transmission mode

The primary functions of the mother board software include controlling the active mode/sleep mode duty cycle, sampling sensor data, creating data packets, and controlling the RFIC to transmit and receive these packets. In transmit mode, the software operation is described in Figure 2-18.

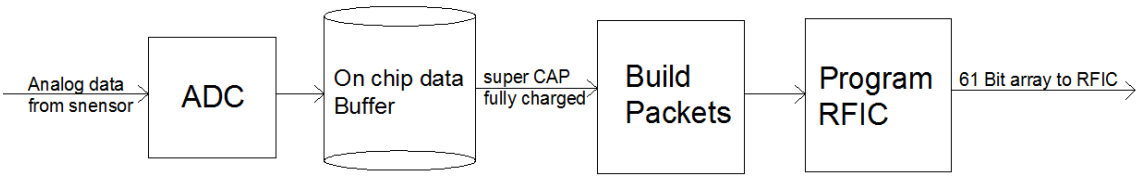

Figure 2-18: Software design overview for transmission mode

A. ADC and On-chip Data Buffer

Since packet size reduction and sufficient precision (precision = V_ref/2^{bits}) are goals, an 8-bit ADC (12mV precision with 3.3V reference voltage) is employed in this design. After one ADC conversion, an 8-bit byte is stored in the on-chip data buffer. For specific type of sensor, it needs

to take more than one value per sample time. For example, an accelerometer (ACC) sensor needs to obtain 3 values (x-axis, y-axis, and z-axis) per sample, thereby 3 bytes stored in the on-chip data buffer for each sample time. Maximum buffer size is set to 256 bytes. Buffer size could not be too large (e.g. over 300 bytes) because data must be transmitted within 0.4s or less due to working range of UVSC (see Table 2-3) and high Tx mode current consumption (51mA). Buffer size could not be too small (e.g. less than 50 bytes) in order to avoid transmit efficiency reduction due to packet having fixed preamble length and CRC bits. When the super capacitor is fully charged, uC sends data stored in the on-chip data buffer to FPGA via serial peripheral interface (SPI) for creating a packet.

B. Packet Creation and RFIC Programming

Packet formats

In wireless communication, data is most often transmitted in the form of packets. Two types of packets are used in this design: data packets (see Figure2-19) and command packets (see Figure 2-20). Each type is formatted to achieve good tradeoff between performance and data transmission efficiency when operating at extremely low power.

(1) Data Packet:

A data packet consists of:

- 4-byte sync word: "010101..." sequence and a "111" to indicate the end of the sync word
- 1-byte ID &Type: 6-bit ID that can define up to 64 BSR nodes and 2-bit type always ‘10’ for data packet
- 1-byte size: identifies the number of bytes in the "data" (up to 256)
- 4 to 256-byte data payload
- 4-byte CRC

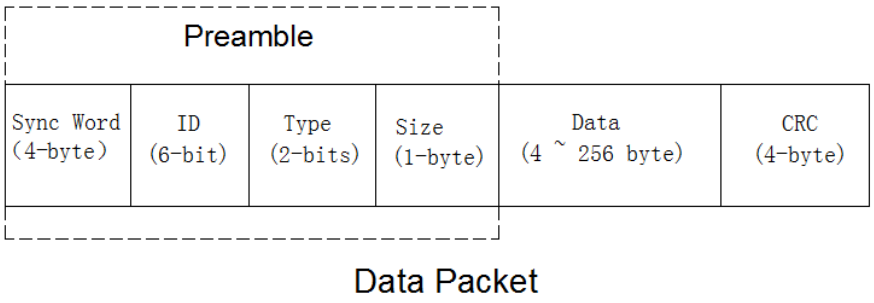

Figure 2-19: Data Packet

(2) Command Packet:

A command packet consists of:

- 4-byte sync word: "010101..." sequence and "111" to indicate the end of the sync word
- 1-byte ID & Type & Parity Check: 6-bit ID that can define up to 64 sensors, 1-bit type always '0' for command packet, and 1-bit parity check
- 1-byte command & Parity Check: 7-bit Command (up to 128 commands) and 1-bit parity check

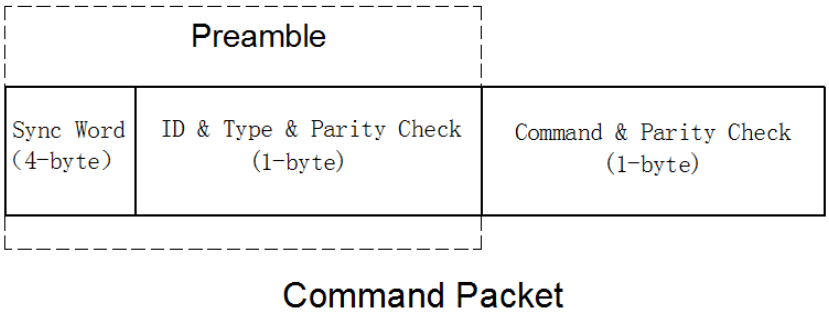

Figure 2-20: Command Packet

The "Sync Word" is a moderate length sequence of "0101..." ending with "111" to allow a receiver to synchronize to, confirm the incoming packet, and locate the beginning field. In [12] [13], extensive analyses have been done to decide the necessary length of sync word. Since multiple transmitters (BSR nodes) are used, the ID defines the "sending source" of the packet. Two types of packet are used in the system: one for transmitting data and another for transmitting command. "Type" determines whether a packet is a command packet or a data packet. If a packet is a data packet, the "Size" indicates the number of bytes of data (command packet is not well defined). "Data" stores data coming from on-chip data buffer. The last part of

data packet is Cyclic Redundancy Check (CRC). If a packet is a command packet, the command and parity check field are combined to minimize the packet size.

2.3.2.2 Receiving Mode

The software design of the receiving mode focuses on the processing of incoming data after the demodulation process is performed by the FPGA and is the subject of a parallel research project covering demodulation bit synchronization, and packet detection [13]. The primary functions of receiving mode software include synchronization of incoming data, detection of the sync word, and packet processing. An overview block diagram of the design is shown in Figure 2-21.

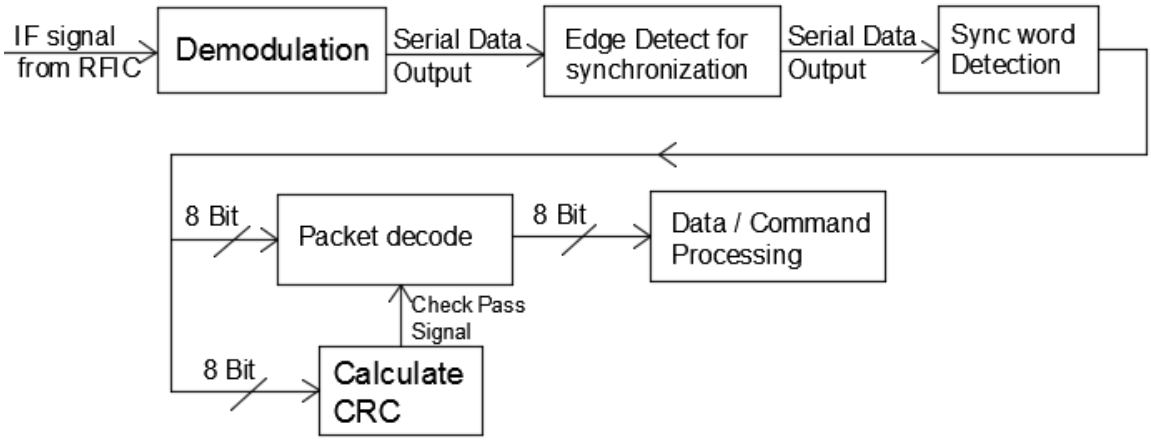

Figure 2-21 Block Diagram of Receive Design

Synchronization of incoming data

Due to limitations of the ultra-low power demodulation method used, data out of the demodulation step may be slightly distorted and with the incoming data rate increased, the distortion becomes more and more serious (see Figure 2-22 and Figure 2-23) [13].If incoming data is continuously sampled by the software design without taking corrective action, distortion accumulates and bit error occurs. Distortion accumulation is avoided by calibrating the start time of sampling whenever an edge (either positive of negative edge) of incoming data is detected (See 2-24). However, errors still occur if incoming data rate is high. Based on the test in [13], probability of error reception increases from 1% to 10% with incoming data rate changing from 10kbits/s to 30kbits/s. For this reason, the data rate used in this project is currently limited to 10kbits/s.

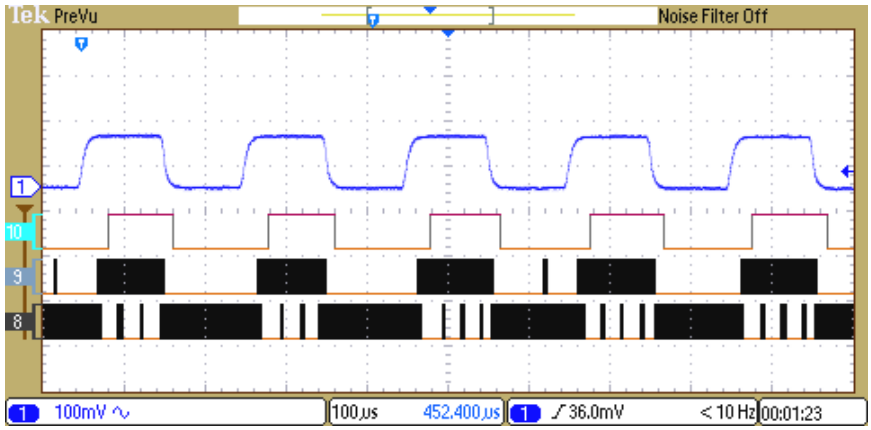

Figure 2-22: Demodulation test results with 10kbit/s incoming data rate (the top line shows the original incoming data and second line shows the data after demodulation) [13]

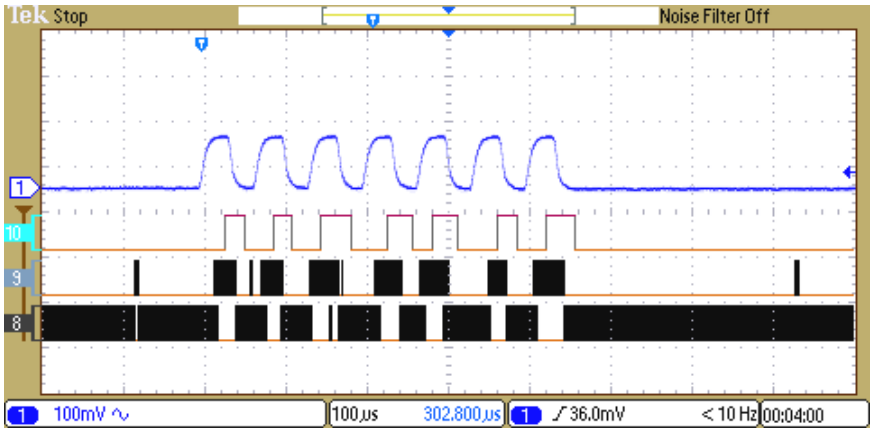

Figure 2-23: Demodulation test results with 30kbit/s incoming data rate (the top line shows the original incoming data and second line shows the data out from demodulation) [13]

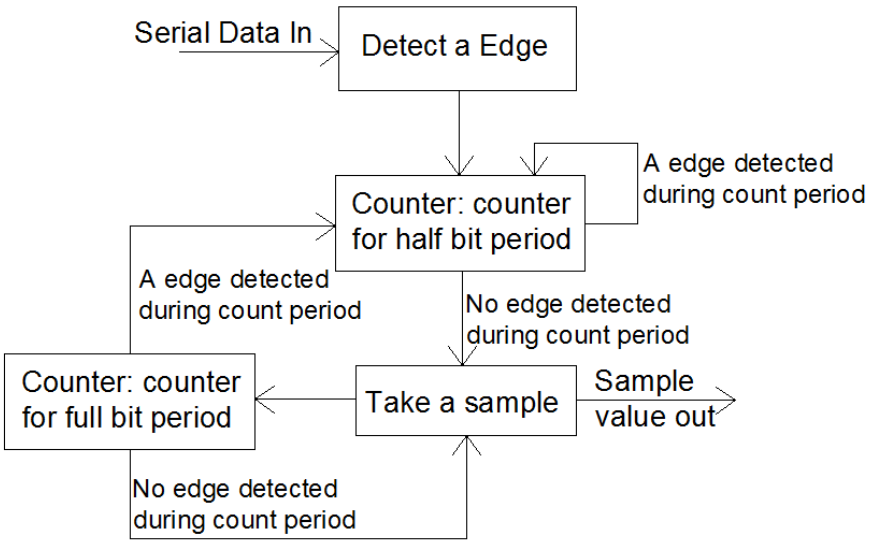

Figure 2-24: Block Diagram of Edge Detection Method

Detection of sync word

Two main steps detect the sync word:

- Verification that incoming data is a sync word
- Determination of the end of sync work

As discussed in Section 2.3.2 Packet format, a sync word has a long sequence of "0101…," allowing distinction between sync word and noise. When a pattern of "01" repeated eight times is detected, a sync word is assumed; then a pattern of "111" must be detected to indicate the end of sync word and begin data processing.

Packet processing

The incoming packet is decoded by following the order of the packet fields. The block diagram of packet processing is shown in Figure 2-25. First, the ID field is checked to ensure that the packet originates from the desired node. Then, by checking the "Type" of the packet, a determination must be made as to whether the packet is a command or a data packet. When a command packet is received and the packet passes parity check, the command will be further processed; when a data packet is received and passes CRC check, data reception is confirmed. When an incoming packet does not pass the check (parity or CRC check), the receiver node

transmits a Re-send command packet to the originating node inform it to re-transmit the previous packet.

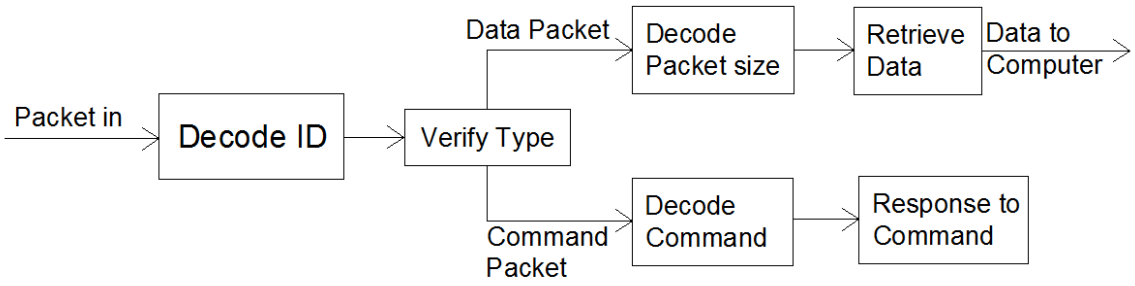

Figure 2-25: Block diagram of packet processing

Operation modes and duty cycle considerations

A BSR node operates in three modes: sleep mode (SM), data sampling mode (DSM), and active mode (AM) (Figure 2-26). During sleep mode, uC works in power-save mode with an external low frequency crystal controlled 32 KHz clock to minimize power use while maintaining accurate timing. All other components, including RFIC, Regulator2, and FPGA, are turned off. The current in sleep mode (I_S) is approximately 6 ~ 10uA (data sheet) and the period of SM (T_S) is around 1 over the sensor data sampling rate (f_{ds}). When SM is finished, the system immediately proceeds to DSM. The task of DSM is to convert analog signals from the daughter board to 8-bit data words and store the data in an on-chip buffer. In DSM, the microcontroller works with an 8MHz internal clock, and the current (I_{DS}) of the system increases to approximately 4 mA (data sheet). The period of DSM (T_{DS}) is very short (25~75 us) compared to the SM (approximately 1 second). When DSM is finished, the system returns to SM. The system proceeds to AM when the super capacitor is fully charged. During AM, the uC turns on the FPGA and RFIC in order to transmit (Tx) or receive (Rx) a packet as previously described. The period of AM (T_{am}) can be calculated by

$$T_{am} = L_{packet}\left(\frac{1}{f_{tx}}\right) + T_{Rx} \qquad (2.3.4\text{-}1)$$

where f_{tx} is transmit bit rate, L_{packet} is the packet length, and T_{Rx} is node listening time. If a BSR is a transmit-only node, the T_{Rx} would be zero. However, for the protocols discussed in Chapter 3, a non-zero T_{Rx} would be used.

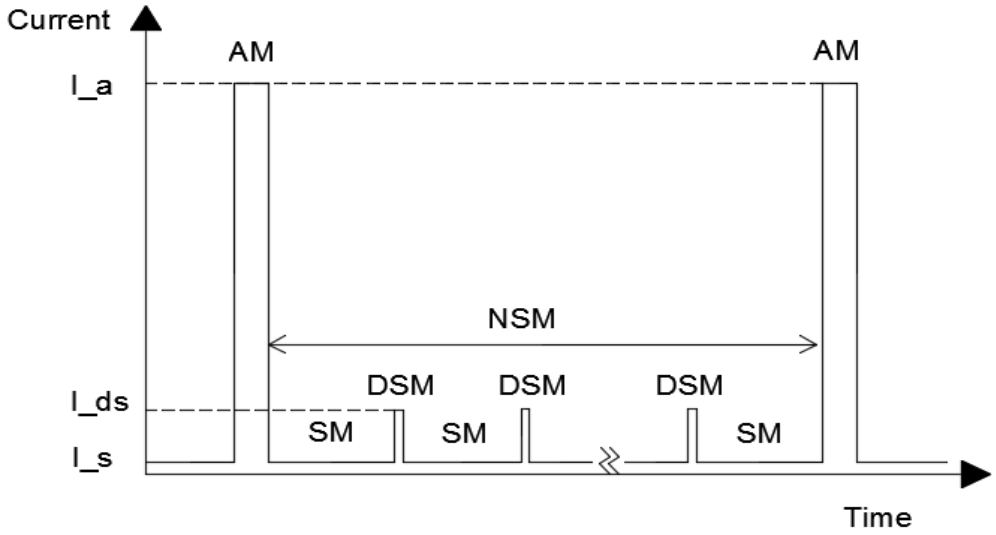

Figure 2-26: Time Sequence VS Current (SM: Sleep mode; DSM: Data Sampling mode; AM: Active mode; NSM: Nominal sleep mode)

Since the data sampling and active mode currents are much higher than the charging current to the energy harvesting storage capacitor, the most difficult part of design is achieving acceptable bio sensor data rate. To quantity this constraint, we next look at the current consumption level of the major components.

2.3.3 Testing Results and Analysis

1. Current consumption of different modes

Figure 2-27 depicts the measurement set up. Measured current consumptions for different modes are recorded in Table 2-5

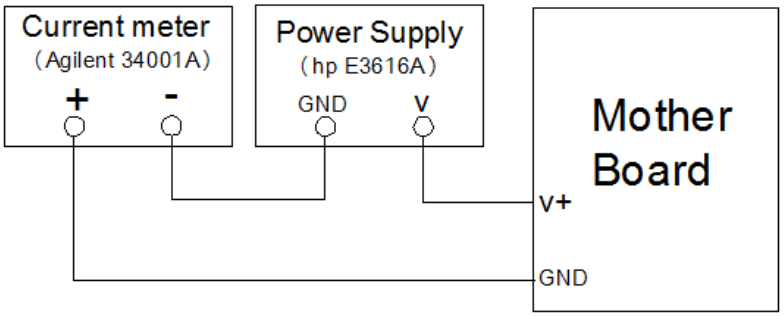

Figure 2-27: Current measurement set up

Table 2-5: Current measurement results

Mode Types	Components Turned on	Current (measurement)
sleep mode (SM)	uC(sleep),Regulator 1&2,	8uA
Data sampling mode(DSM)	uC(active), ACC sensor	4.7mA
Tx mode	uC(active), FPGA, RFIC, Regulator 1&2	51mA
Rx mode	uC(active), FPGA, RFIC, Regulator 1&2	30mA

2. Testing with combined mother board and daughter board

In this test, instead of a power supply, the daughter board was employed to power the mother board. A test point was put on the super capacitor to monitor the voltage changing when the mother board operated in different mode. Figure 2-28 shows that the tested voltage decreased when a BSR node ran in AM (Tx mode at this test) and increased with much slower rate when it returns to sleep mode. The packet transmission last 89.6 ms with 10kbits/s transmission rate and the voltage across the super capacitor drops approximately 98mV, from which the current consumption of packet transmission can be calculated to be 53.4mA.

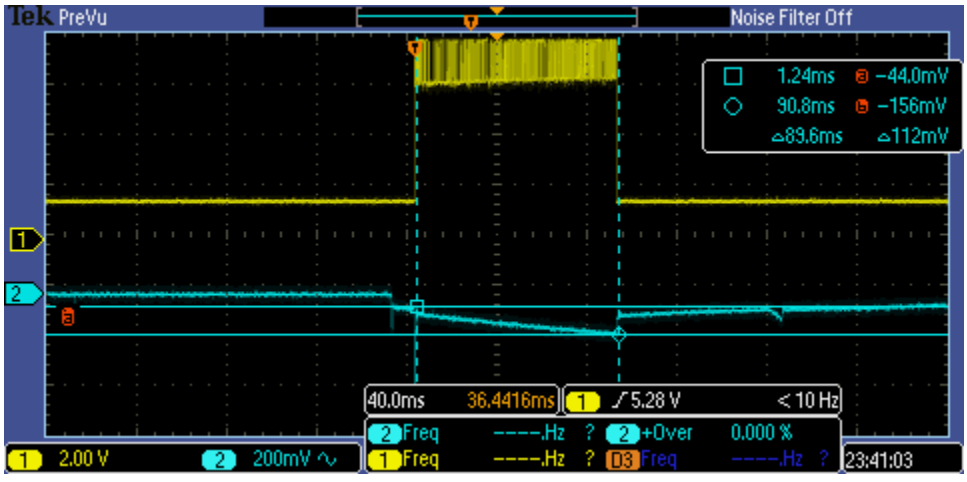

Figure 2-28: Combinational test output (top yellow signal shows a transmitted packet and the blue signal shows the voltage change across the super capacitor)

2.3.4 Duty Cycle Analysis

A. Duty Cycle Calculation

To simplify duty cycle calculation, SM and DSM can be combined as a Nominal Sleep Mode (NSM). The total time of the NSM (TTNSM) is $N(T_s + T_{ds}) \approx N T_s$, where N is the number of DSMs between two AM. The duty cycle is then calculated as

$$\text{Duty Cycle} = \frac{T_{am}}{N(T_s+T_{ds})+T_{am}} \approx \frac{T_{am}}{NT_s}, (T_s \gg T_{ds},\ NT_s \gg T_{am}) \quad (2.3.4\text{-}1)$$

To find the period of active mode (T_{am}), Equation (2.2.4-1) can be written as

$$dt = \frac{dv}{i} C \quad (2.3.4\text{-}2)$$

where dv is the voltage difference ($\Delta V_{discharge}$) before and after AM mode, i is the AM current (I_{am}), C is the value of the super capacitor (50mF), and *dt* is the discharging time of the super capacitor equaled to the period of AM (T_{am}):

$$T_{am} = \frac{\Delta V_{discharge}}{I_{am}} C \quad (2.3.4\text{-}3)$$

Similarly, the total time of NSM (NTs) can be written as

$$N\ Ts = \frac{\Delta V_{charge}}{I_{charge}} C \quad (2.3.4\text{-}4)$$

where ΔV_{charge} is the voltage difference before moving into NSM and after leaving NSM to AM, and I_{charge} is the charging current of the super capacitor during NSM. The super capacitor must be fully charged before moving into AM in order to compromise the power consumed during AM. Therefore,

$$\Delta V_{charge} = \Delta V_{discharge} \quad (2.3.4\text{-}5)$$

When Equations (2.3.4-3), (2.3.4-4), and (2.3.4-5) are combined, the new expression of duty cycle is

$$\text{Duty Cycle} = \frac{T_{am}}{N\ T_s} = \boxed{\frac{I_{charge}}{I_{am}}} \quad (2.3.4\text{-}6)$$

When supply current comes out from the daughter board (I_{DB}), it splits into two branches: one branch goes to the mother board to maintain NSM (I_{NSM}) and another one goes to charge the super capacitor (I_{charge}) (Figure 2-29).

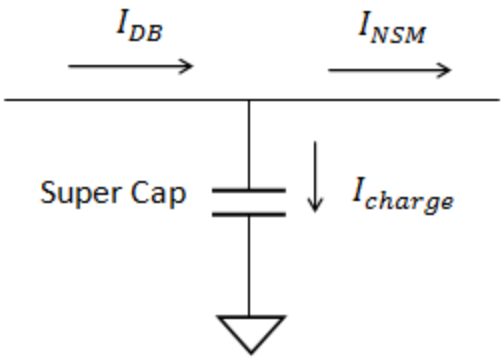

Figure 2-29: Current flow during NSM

According to Figure 2-29,

$$I_{charge} = I_{DB} - I_{NSM} \tag{2.3.4-7}$$

where I_{NSM} can be calculated by

$$I_{NSM} = \frac{I_s T_s + I_{ds} T_{ds}}{T_s + T_{ds}} \approx \frac{I_s T_s + I_{ds} T_{ds}}{T_s} = I_s + I_{ds} T_{ds} \left(\frac{1}{T_s}\right) \tag{2.3.4-8}$$

Because the SM period equals to the time between two DSMs ($T_s = 1/f_{ds}$), Equation (2.3.4-6) can be written as

$$I_{NSM} = I_s + I_{ds} T_{ds} f_{ds} \tag{2.3.4-9}$$

B. Maximum Data Sampling Rate Analysis without Rx Mode

The maximum data sampling rate (MDSR), which defines the maximum data that can be taken during TTNSM and successfully be transmitted during AM, is an indicator of system capability. According to Equations (2.3.4-9) and (2.3.4-7), when the data sampling rate (f_{ds}) is increased, I_{charge} is decreased. Therefore, the harvested energy ($E_{harvested}$) decreased with fixed harvesting time. In addition, the energy consumed ($E_{consumed}$) during AM mode increased because more data obtained during TTNSM period required transmission. Because f_{ds} cannot be too high to make $E_{consumed}$ exceed $E_{harvested}$, f_{ds} was limited by the following inequality

$$E_{harvested} \geq E_{consumed} \tag{2.3.4-10}$$

Given an energy harvesting time ($N T_s = N\left(\frac{1}{f_{ds}}\right)$), an energy harvesting current (I_{charge}), and an EHS output voltage (V_{out}), the $E_{harvested}$ can be derived as

$$E_{harvested} = V_{out}(\mathrm{N}\,\mathrm{T_s})I_{charge} \quad (2.3.4\text{-}11)$$

When Equation (2.3.4-9) and Equation (2.3.4-7) were substituted into Equation (2.3.4-11), a new expression of $E_{harvested}$ was evolved. f_{ds} is shown as

$$E_{harvested} = V_{out}\mathrm{N}(\frac{I_{DB}-I_S}{f_{ds}} - \mathrm{I_{DS}T_{DS}}) \quad (2.3.4\text{-}12)$$

Because BSR nodes are power-constrained, ideal energy utilization uses all the energy to transmit data without wasting energy to listen to the channel. The expression of $\mathrm{E_{consumed}}$ under this ideal condition (without considering Rx mode) is shown as

$$\mathrm{E_{consumed}} = \mathrm{V_{in}T_{am}I_{am}} = V_{in}\mathrm{T_{tx}I_{tx}} \quad (2.3.4\text{-}13)$$

where $\mathrm{V_{in}}$ is input voltage of mother board that equals to V_{out}, $\mathrm{I_{tx}}$ is the Tx mode current consumption, and $\mathrm{T_{tx}}$ is the packet transmission time which can be calculated as

$$\mathrm{T_{tx}} = (L_{preamble} + L_{data})(\frac{1}{f_{tx}}) \quad (2.3.4\text{-}14)$$

where $\mathrm{L_{preamble}}$ is the length of preamble part (bits) of a packet and $\mathrm{L_{data}}$ is the length of data part (bits) of a packet. $\mathrm{L_{data}}$ is decided by the number of data sampled during TTNSM and calculated by

$$L_{data} = 8n\mathrm{N} \quad (2.3.4\text{-}15)$$

where n, which is variously based on the type of sensor, is the total number of data sampled during each DSM. For example, the accelerometer sensor at each DSM must obtain three data for x, y, and z axis, and ECG sensor obtains one data at each DSM. There is an 8 in Equation (2.3.4-15), because of the use of an 8-bit ADC. When Equations (2.3.4-15) and (2.3.4-14) are substituted into Equation (2.3.4-13), a new expression of $E_{consumed}$ can be written as

$$\mathrm{E_{consumed}} = \mathrm{V_{in}I_{tx}}(L_{preamble} + 8n\mathrm{N})(\frac{1}{f_{tx}}) \quad (2.3.4\text{-}16)$$

f_{ds} was then computed by substituting Equations (2.3.4-12) and (2.3.4-16) into inequality (2.3.4-10):

$$f_{ds} \leq \frac{(I_{BD}-I_S)Nf_{tx}}{I_{tx}(L_{preambel}+8nN)+Nf_{tx}\mathrm{I_{DS}T_{DS}}} \quad (2.3.4\text{-}17)$$

Therefore, the MDSR can be derived as

$$f_{ds\_max} = \frac{(I_{BD}-I_S)Nf_{tx}}{I_{tx}(L_{preambel}+8nN)+Nf_{tx}\mathrm{I_{DS}T_{DS}}} \quad (2.3.4\text{-}18)$$

In Equation (2.3.4-18), two variables, n and N, affect the maximum data sampling rate (MDSR). Figure 2-30 shows that, with the number of DSM during the total time of the NSM (TTNSM) increased (N), MDSR is increased and approaching to a fixed value. A BSR node with EMG sensor ($n = 1$) has 3 times higher MDSR than a BSR node with ACC sensor ($n = 3$) due to the single byte converted in the EMG sensor case.

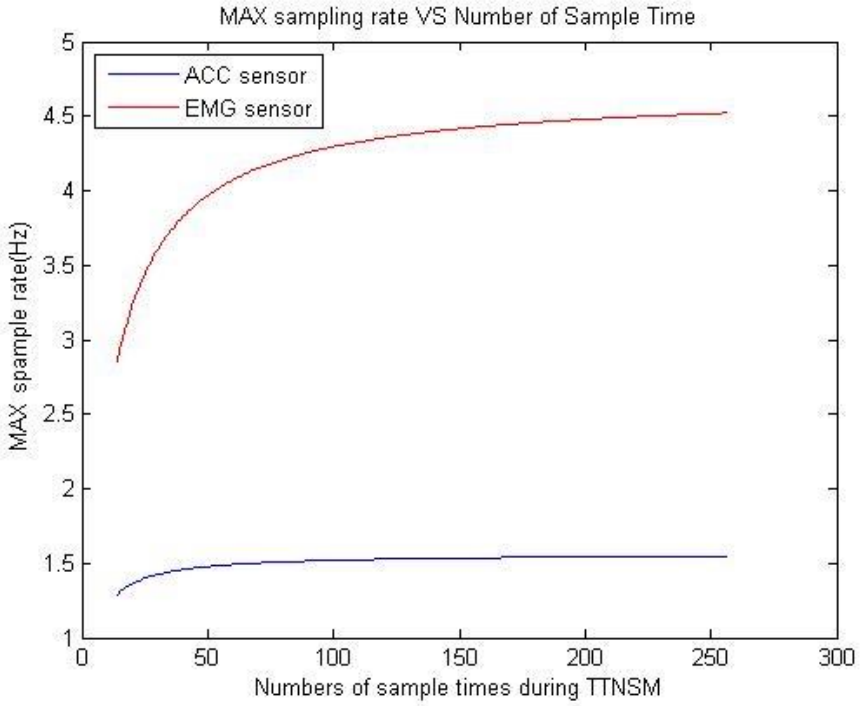

Figure 2-30: MDSR vs. Number of sample times during TTNSM
(ACC sensor and EMG sensor)

When the Rx mode was considered, a new expression of $E_{consumed}$ was derived as

$$E_{consumed} = V_{in}(T_{tx}I_{tx} + T_{rx}I_{rx}) \quad (2.3.4\text{-}19)$$

f_{ds} can be computed as

$$f_{ds} \leq \frac{(I_{BD}-I_S)N_{max}\, f_{tx}}{I_{tx}(L_{preambel}+8nN_{max})+f_{tx}(N_{max}I_{DS}T_{DS+}T_{rx}I_{rx})} \quad (2.3.4\text{-}20)$$

Therefore, the MDSR can be derived as

$$f_{ds\_max} = \frac{(I_{BD}-I_S)N_{max}\, f_{tx}}{I_{tx}(L_{preambel}+8nN_{max})+f_{tx}(N_{max}I_{DS}T_{DS+}T_{rx}I_{rx})} \quad (2.3.4\text{-}21)$$

Where N_{max} is the maximum sampling time during TTNSM and with fixed listening time N_{max} can be calculated as

$$\mathrm{N}_{\max} = \left(\frac{(E'_{harvested} - \mathrm{V}_{in}\mathrm{T}_{\mathrm{rx}}\mathrm{I}_{\mathrm{rx}})f_{tx}}{\mathrm{V}_{in}I_{tx}} - L_{preambel}\right)\left(\frac{1}{8n}\right) \qquad (2.3.4\text{-}22)$$

where $E'_{harvested}$ is the maximum energy can be harvested within the TEHS working range (see Table 2-3).

Figure 2-31 and Figure 2-32 show that with more time spending on Rx mode, MDSR becomes lower and lower. MDSR of sensors goes to zero when the listening time is 0.66 s, because all the harvesting energy are used to listen to the channel and no energy are used to transmit data. For a practical system, Figure 2-31 suggests that listening time should not exceed about 100ms. This is an important result relative to the design of MAC layer protocols in the following chapter.

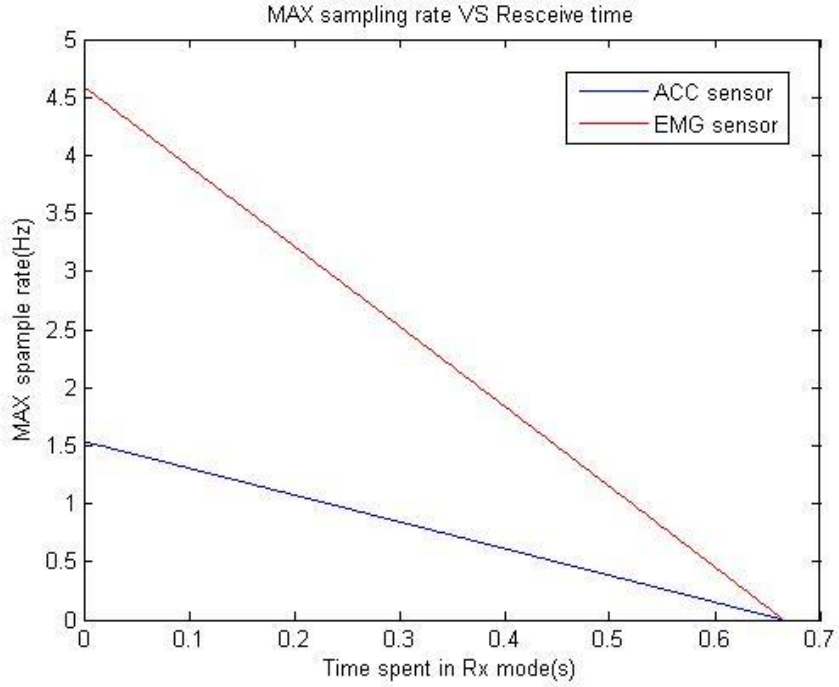

Figure 2-31: MDSR vs. Time spent in Rx modes (ACC sensor and EMG sensor)

2.3.5 Summary of PHY Layer Design

At the beginning of this chapter, we introduced two types of transceiver nodes of our star topology energy harvesting wireless sensor network (EHWSN): the bio-sensor radio (BSR) node and the gateway radio (GR) node. Then, we discussed the packet design and the modulation method employed. Finally, we tested the output power from energy harvesting system and

current consumption for different modes, and analyzed the maximum data sampling rate (MDSR) under different conditions. A summary of PHY layer design used in the calculations is shown in Table 2-6.

Table 2-6: PHY layer features summary

Network type	Star topology network
Node type	BSR node, GR node
Modulation method	FSK @ 10kbit/s
Carrier frequency	467MHz
Packet type	Data packet, Command packet
Packet size	Data packet: 13~269 bytes
	Command Packet: 6 bytes
Energy harvesting system output power	0.87mW
Current consumption (with 4.95V)	Sleep mode: 8uA
	Tx mode： 51mA
	Rx mode: 30mA
Maximum data sampling rate (without Rx mode)	ACC Sensor: 1.5Hz
	EMG Sensor: 4.5Hz
Maximum data sampling rate (with 100 ms Rx mode)	ACC Sensor: 1.3Hz
	EMG Sensor: 3.9Hz

Chapter 3 - Recent MAC Layer Protocol Survey and New MAC Protocol Layer Design

As demonstrated in Chapter 2, controlling the duty-cycle of wireless sensor nodes in the EH network facilitates low energy consumption. The MAC layer design for this WSN can be regarded as a duty-cycling MAC Protocol [21] [24]. The first portion of this chapter presents a survey of duty-cycling MAC layer design roughly categorized as synchronous (e.g. WiseMAC [15], S-MAC [16], T-MAC [17]) and asynchronous (e.g. B-MAC [18], X-MAC [19], RI-MAC [20], and RW-MAC [21]). Given the extreme energy constraints on energy and the cost of achieving synchrony, asynchronous MAC layer is the primary focus of this thesis.

In our EHWSN, as Bio-Sensor Radio (BSR) nodes are extremely power-constrained, their energy usage has to be reduced or even eliminated. It would be prudent to use almost all the energy stored by EHS for transmitting data. Gateway Radio (GR) node is a power-unconstrained node. Therefore, the primary goal of our MAC layer design is to shift energy consumption pressure from BSR nodes to the GR node as best as possible. Two asynchronous MAC protocol designs that fit the PHY layer design: Type I MAC Layer (CSA-MAC layer) and Type II MAC Layer (GRI-MAC Layer) are present in this chapter. Their properties (collision probability, overhearing time, and idle listening time) are analyzed via simulations.

3.1 Survey of Energy Efficient MAC Protocols

Currently, plenty of MAC layer designs for WSNs attempt to obtain high energy efficiency by duty-cycling each node in the WSNs [22]. Duty-cycling nodes between sleep mode and active mode can reduce unnecessary power consumption. The following section introduces background knowledge and describes several duty-cycling MAC layers.

3.1.1 Energy Considerations

Before individual MACs can be introduced, reasons for energy waste [22] [23] [24] in WSNs are demonstrated below:

- Packet Collision: Packet collision occurs when more than one packet is transmitted simultaneously or when only part of a packet overlaps with other packets during transmission (sees Figure 3-1). Packet collisions can be solved by re-transmitting the packet. This solution, however, will at least double the amount of energy utilized to transmit the packet.

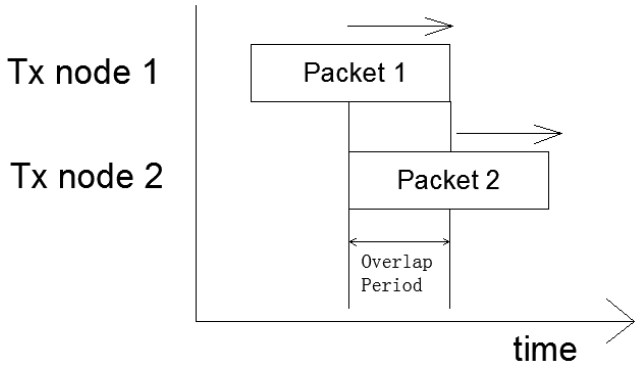

Figure 3-1: Packet Collision (part of packet overlaps)

- Idle Listening: Idle listening occurs when a node consumes energy in order to listen to the idle channel while waiting for possible traffic.
- Overhead: Energy is consumed by nodes sending the control packet before sending the data packet.
- Overhearing: A node may waste energy listening to a signal not destined for it.
- Overemitting: A node may transmit a packet to a receiver that is not ready to receive it.

3.1.2 MAC Layer for Duty-cycled WSNs

In order to prolong the life and increase energy efficiency of the sensor node, sensor nodes cycle between a sleep mode and an active mode. MAC protocols developed for this kind of duty-cycled WSNs can be categorized as synchronous or asynchronous [19] [22]. In synchronous WSNs, duty cycles of sender nodes are pre-scheduled by receiver nodes via synchronization information; in asynchronous WSNs, duty cycles of sender nodes are independent of receiver nodes' status.

A. Synchronized MAC Layer for Duty- cycled WSN

Synchronous MAC protocols specify the period of wake-up and sleep durations to reduce unnecessary time and energy wasted in idle listening. S-MAC is an example of this type of MAC protocol.

Sensor-MAC (S-MAC)

S-MAC [16] aims to establish low-duty-cycle operation to achieve high energy efficiency. All nodes in the network periodically sleep, wake up, receive/transmit data, and go back to sleep. To reduce control over-head, they use virtual cluster techniques [19] to make the neighboring nodes synchronize via exchange of schedule information. Therefore, the neighboring nodes can wake up at the same time. After exchanging synchronization information, the nodes will send Ready to Send-Clear to Send (RTS-CTS) packet at the end of a wake period to avoid data collision. The send-data will follow the successful exchange of RTS-CTS, which is shown in Figure 3-3. Since periodic sleep causes high latency, especially for multi-hop routing, adaptive listening is introduced to reduce latency. When a node hears a transmission of its neighbor, it wakes up at the end of the transmission to determine whether it is the next hop. If the node is the next-hop node, its neighbor could pass the data immediately instead of waiting until the next scheduled listening time.

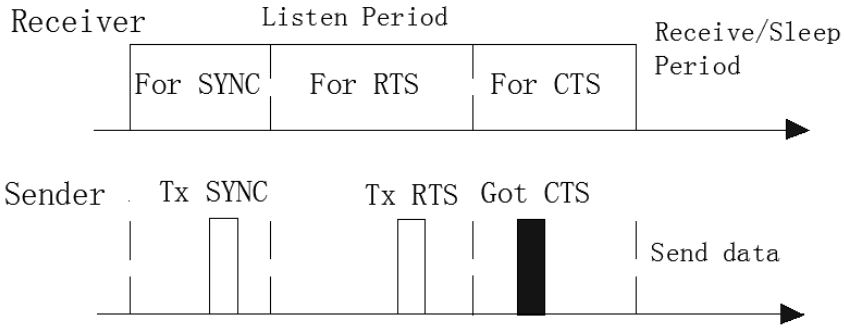

Figure 3-2: S-MAC Sender-Receiver Communication [16]

Advantages: Sleep schedules reduce energy waste caused by idle listening. Carrier sense is used to achieve collision avoidance.

Disadvantages: Adaptive listening causes idle listening and overhearing problems. Synchronization information exchange also increases power consumption due to control packet overhead.

Conclusion: For S-MAC, periods of sleep and awake are predefined and constant. Unfortunately, these periods do not fit our system because sleep period of BSR nodes is controlled by the energy monitor. Energy waste on the control packet overhead (sync information exchange, CTS/RTS) cannot be accommodated by the energy harvesting system that shoulders the burden of energy consumption.

B. Asynchronous MAC Layer for Duty- cycled WSN

The key advantage of Asynchronous MAC is that the sender and receiver can be completely decoupled in their duty cycles [25], thereby removing the energy used for exchanging synchronization information. Asynchronous MAC can be divided into two categories: sender-initiated MAC and receiver-initiated MAC.

a) Sender-Initiated MAC

Sender-initiated means the communication request starts from the sender side.

B-MAC

Berkeley Media Access Control (B-MAC) [18] is a Carrier Sense Multiple Access (CSMA) protocol for low-power WSNs. In order to avoid packet collision, the channel must be determined to be clear. This determination is referred to as Clear Channel Assessment (CCA). To realize CCA, B-MAC uses an outlier algorithm comprised of nodes that take five samples during the channel sampling period. The channel is declared to be busy if none of the five samples is outlier whose energy level is significantly below the noise floor. The channel is declared to be clear if outlier exists among the five samples.

Receiver node duty cycles its radio through periodic channel sampling, known as Low Power Listening (LPL). Once the receiver wakes up, it checks channel activity. If a preamble is detected, the receiver node stays awake to receive the incoming packet. Transmit nodes send the preamble long enough to match the interval. For example, if the channel is checked every 100ms, the preamble must be at least 100ms long for a node to wake up. The channel is also checked for activities to wake up the receiver node. The process of timing line is indicated in Figure 3-3.

Advantages: LPL reduces the power consumption caused by idle listening. B-MAC has better packet deliver rate, latency and energy consumption [18].

Disadvantages: A long preamble must be sent before the data is transmitted, consequently decreasing transmission efficiency and increasing power consumption.

Conclusion: In our system of interest, the transmit node (BSR) is an extremely power-constrained node. The long preamble consumes almost all the energy harvested in one sleep cycle before data transmission occurs. Therefore, the B-MAC is unsuitable for our WSN.

X-MAC

To avoid the overhearing, X-MAC [19] sends a series of short preambles instead of an entire long preamble used in B-MAC. For each short preamble, the target address is embedded, thereby allowing the receiver node to know whether or not it is the target node without having to wait until the end of the extended preamble. If the receiver node finds it is not the target node, it can

go back to sleep immediately to reduce energy cost due to overhearing; if the receiver node finds it is the target node, it sends an Acknowledge (ACK) packet to the transmit node. In X-MAC a short pause is inserted between short preambles to create a small window through which the sender node can listen to the media. If a sender node received ACK packet from the receiver, it stops sending the preamble and begins to send the data packet, as shown in Figure 3-3,

Advantages: Short preambles with embedded target ID solves the overhearing problem. X-MAC has much better performance than B-MAC from the standpoint of the energy usage.

Disadvantages: The series of short preamble transmission dominates power consumption.

Conclusion: X-MAC cannot be used for the system in this study because of reasons similar to B-MAC. Energy waste as a result of sending a series of short preambles is not feasible for BSR nodes**.**

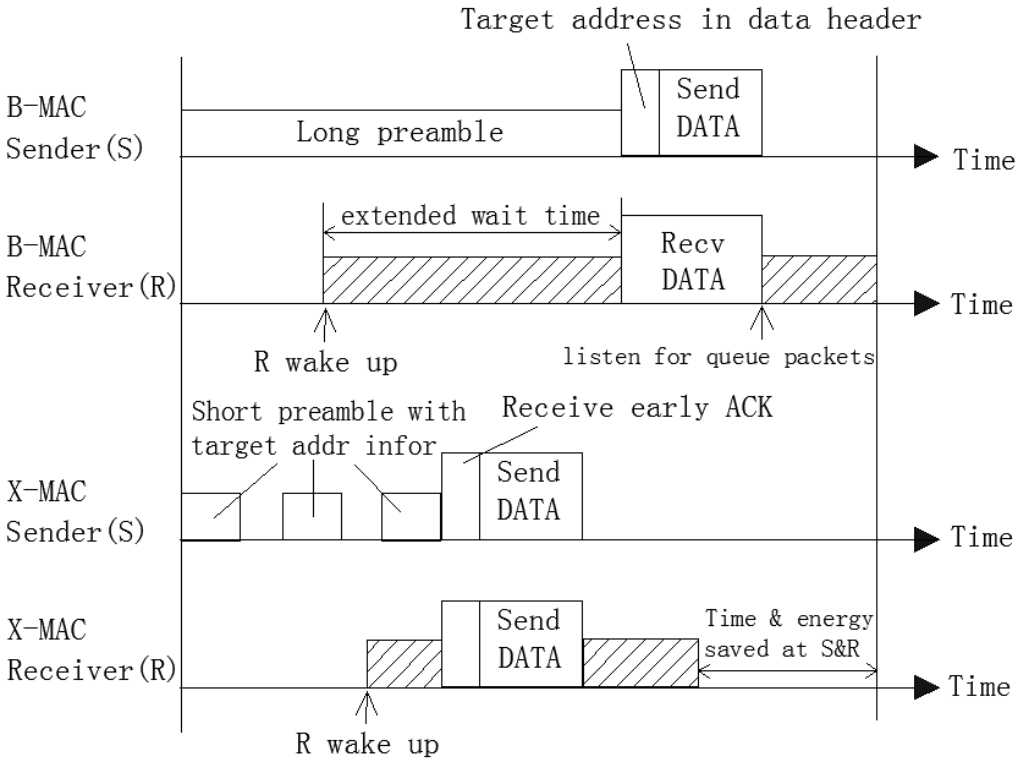

Figure 3-3: Comparison of time line between B-MAC and X-MAC [19]

b) Receiver-Initiated MAC

Receiver-initiated means the communication request starts from receiver side.

RI-MAC

In receiver-initiated MAC (RI-MAC) [20], a DATA frame transmission is initiated by the intended receiver node of the DATA. Each receiver node in RI-MAC periodically wakes up at its own time to turn on its radio and check channel status. If the channel is idle, the receiver node broadcasts a beacon to inform that it is ready to receive a DATA frame. For the sender, a node with pending data silently waits for a beacon from the receiver. When a sender node receives a beacon from the intended receiver, it immediately sends the DATA frame. When the transmission is complete, the sender will get an ACK from the receiver. If no DATA frame comes after a beacon is broadcast, the node goes to sleep, as shown in Figure3-4.

Advantages: Sender does not occupy the channel until the receiver is ready to receive, which handles a wide range of traffic loads more efficiently than B-MAC and X-MAC.

Disadvantages: Sender typically must idle listen for a long time to receive a beacon sent from the receiver.

Conclusion: A long idle listening time for the sender nodes (BSR nodes) is not feasible for our system.

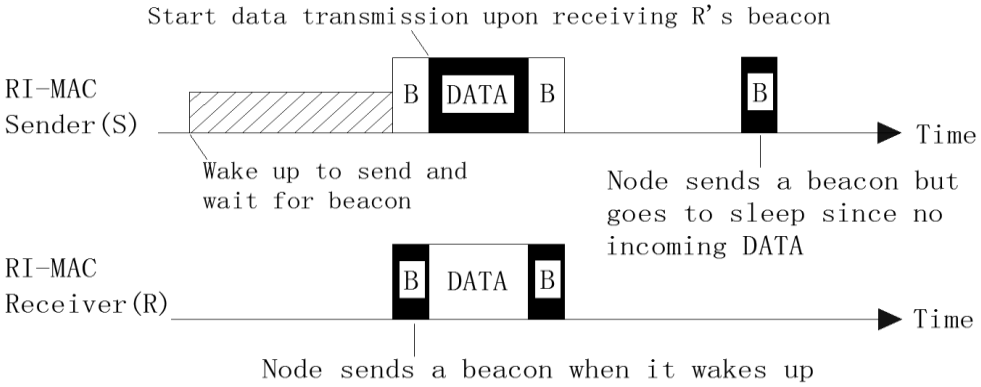

Figure 3-4: Time diagram of RI-MAC [20]

3.2 Type I MAC layer protocol design

3.2.1 Attributes

Extremely Low Duty Cycle:

According to the duty-cycle calculation in Section 2.4, our EH sensor node has only approximately 0.4% duty cycle that is limited by charging current (≈ 200uA) from the EH system and discharging current (≈50mA) for data transmission. In this MAC layer design, the sleep mode period of BSR node has to be maintained at least 250 times longer than the active mode period. For example, if a transmit node spends 300ms to transmit a packet, it must sleep approximately 1.25 minutes to recover its energy.

Single and Unpredictable Energy Source:

In our energy harvesting system, TEG is the only energy source. The TEG converts thermal energy (due to temperature difference) to electrical energy to power the mother-board. Therefore, when designing the MAC layer, the working range (see Table 2-3) of the system must be considered by measuring voltage across the super cap in the daughter board.

Star Topology Network:

Our network can be considered as a Single Cluster Star Topology Network (SASTN) that consists of one GR node and multiple BSR nodes (Figure3-5). In contrast to an ad hoc network, in which every node plays an equivalent role, the GR node is a power-unconstrained node (powered by the space suit) that works as central node to receive all data packets. BSR nodes are power-constrained nodes (powered by EH system) that work as sub-nodes to transmit data packets. During MAC protocol design, energy consumption must be shifted to the GR node as best as possible**.**

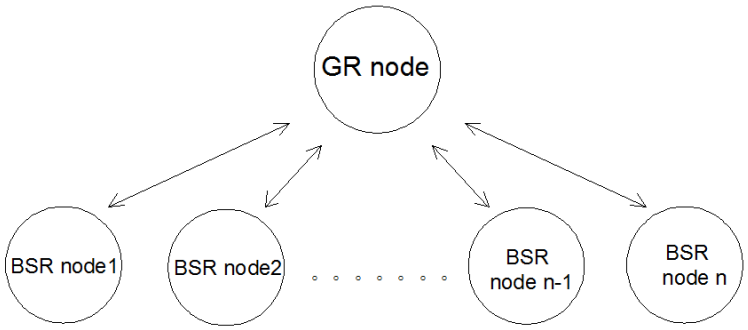

Figure 3-5: Overview of a Star Topology Network

3.2.2 CS-ALOHA Based MAC Layer Design

Along with the discussions in previous subsections, any proposed MAC protocol for our EHWSN must meet the following goals:

- Low latency for data transmission
- Simple control packet overhead
- Achieve highest sampling rate with current duty-cycle
- Shift power consumption pressure from BSR nodes to the GR node

We propose a CS-ALOHA based MAC protocol to meet these requirements.

3.2.2.1 Background

ALOHA Protocol

ALOHA protocol [26], a design for early satellite systems, allows each subscriber to transmit data whenever necessary. This design eliminates idle listening for the subscriber or the BSR node in our system. However, increasing numbers of nodes and length of packets may lead to more packet collisions.

Carrier Sense

Carrier sense (CS) means that each node in the network monitors channel status before information transmission, consequently greatly decreasing collision probability. In type I MAC protocol, CS was realized by the Channel Energy Detection method utilized by other protocols, including 802.15.4 [19]. In this method, each BSR node takes a sample of the channel and compares it to the noise floor. If the sample is above the pre-set threshold, the channel is considered to be busy; if the sample is below the pre-set threshold, the channel is considered to be idle.

Energy Level Monitor

Due to limitations of the TEHS, our system's working range is from 4.6V to 5.0V (voltage across the Super Capacitor, and see Table 2-3 for details). If the voltage drops below 4.6V, the power system unexpectedly shuts off the entire system. The energy status of this system can be monitored by checking voltage across the Super Capacitor. If the voltage is above 4.95V, the energy status is good for sending a data packet; if the voltage is below 4.65V, the energy status is poor (too close to the 4.6V) and the system is forced into sleep mode.

3.2.2.2 Design Description

CS-ALOHA based MAC is sender-initiated asynchronous MAC protocol that combines the CS method and the ALOHA protocol.

For the BSR node side, each node has distinct sleep-wake up periods. When a BSR node is ready to transmit a data packet, the node turns on its radio to sense the channel. If the channel is idle, the node transmits a data packet to the GR node; if the channel is busy, the node goes to sleep for a period equal to the longest data packet transmission time (data pay load part contains 256 bytes data) which is approximately 250ms with 10kbit/s transmission rate. The node then wakes up to sense the channel again. After the BSR node receives the ACK command from the GR node indicating correct reception of the data packet, the BSR node goes back to sleep for another sleep-sampling period. Sometimes, because of low energy level, the BSR node goes back to sleep mode without listening to the ACK command. The BSR node process is shown in Figure3-6.

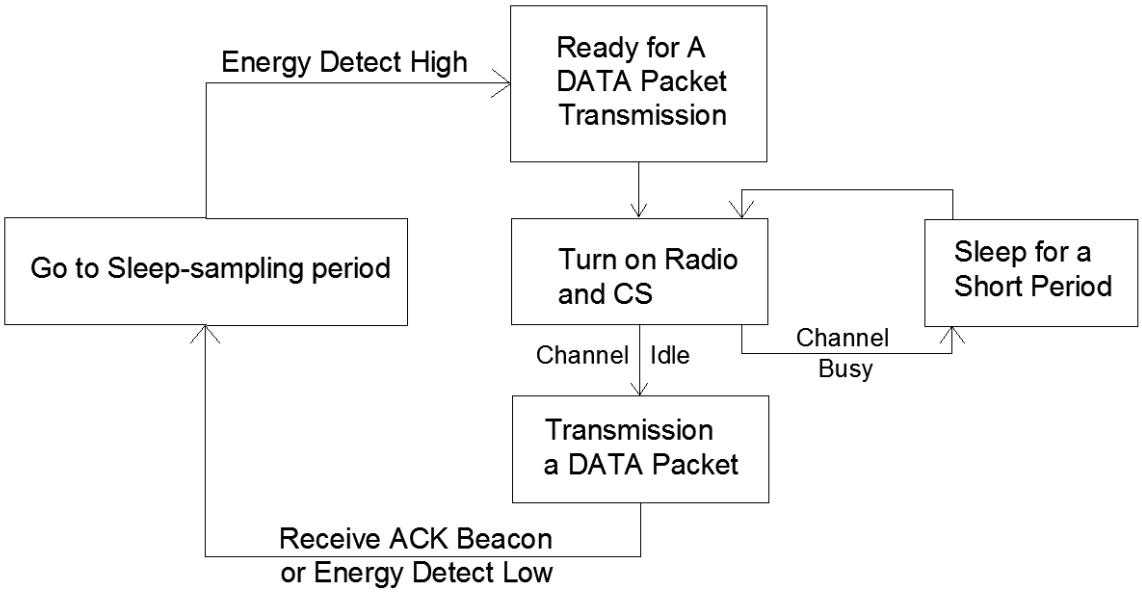

Figure 3-6: BSR Node Process

Because the GR node is a power unconstrained, it listens almost continuously in order to receive the data packet from BSR nodes, thereby making it possible for BSR nodes to transmit data packet whenever they are ready to do so. Therefore, BSR node does not need to transmit a long preamble or a series of short preamble in order to inform the receiver node that it is ready to transmit (see B-MAC and X-MAC). Although this design causes the GR node to experience idle listening, this design successfully shifts power consumption pressure from the BSR side to the GR side, thereby meeting the goals of this study. After correctly receiving the data packet (pass CRC checking), a GR node sends an ACK command packet to the BSR node to inform that the transmission is complete. After that, the GR node continues to listen to the channel. The BSR node process is shown in Figure3-7. A timing flow diagram is shown in Figure3-8.

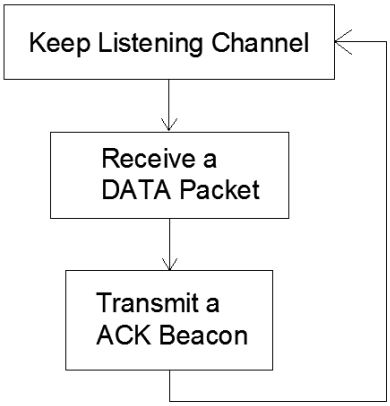

Figure 3-7: Receiver Node (GR node) Process

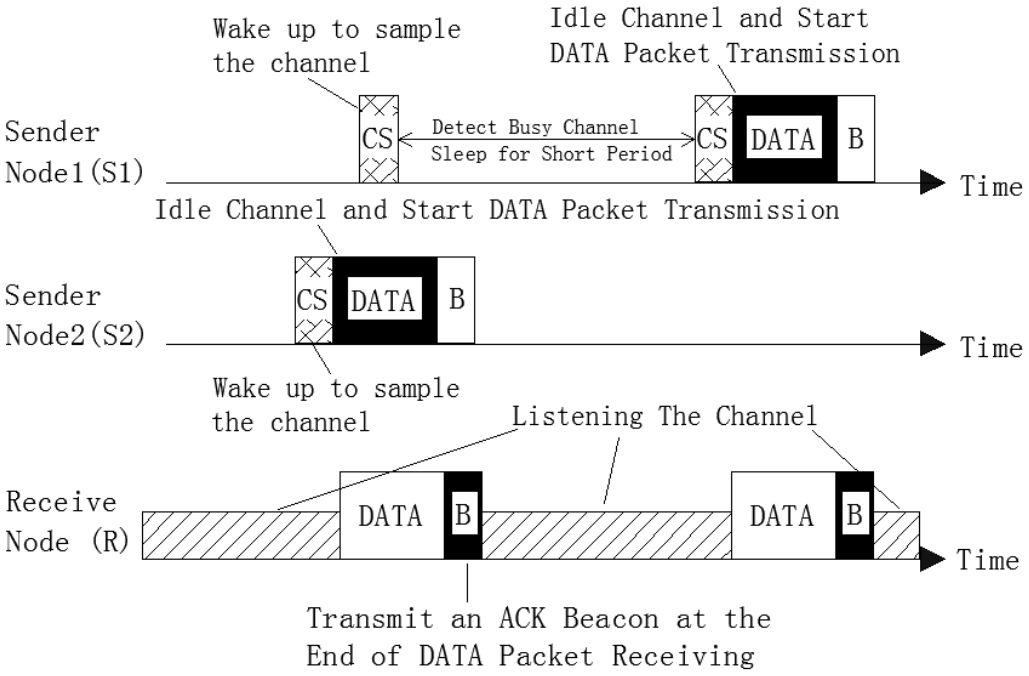

Figure 3-8: Timing Flow Diagram

3.2.3 Simulation and Analysis

WSN in this study is a single-hop network. A BSR node transmits a data packet directly to the GR node without going through intermediary nodes. Therefore there is no latency caused by multiple-hops which are common in ad hoc networks. A BSR node immediately transmits a data packet when the node is ready (high energy level). Therefore, no idle listening or overhearing issues exists in this MAC layer design.

Ideally, packet collision will not occur in this MAC layer design, because a BSR node ensures that the channel is clear before transmitting a data packet. Unfortunately, due to the hidden terminal problem, carrier sense (CS) step does not always work. Therefore, packet collision probability of this MAC layer without the CS step must be evaluated.

Without the CS step, CS-ALOHA MAC layer can be considered as a Pure ALOHA [26] scheme. The probability of that n packets generated by nodes during a given packet duration interval is assumed to be Poisson distributed, given by

$$\Pr(n) = (\lambda\tau)^n e^{-(\lambda\tau)}/n! \quad (3.2.3\text{-}1)$$

where, λ is the mean arrival rate (packet/second) calculated by Equation (3.2.3-2), and τ is the packet duration.

$$\lambda = \sum_{i=1}^{N}\left(\frac{1}{T_{cycle}}\right) \quad (3.2.3\text{-}2)$$

where, N is the number of BSR nodes and T_{cycle} is the average time of a sleep-wake up period. Here, we assume that T_{cycle} is the same across all BSRs. A BSR node transmits one packet within each T_{cycle}, thereby using $1/T_{cycle}$ to calculate mean arrival rate for one BSR node. λ increases with the number of BSR nodes.

A packet is assumed to be transmitted successfully if no other packets are transmitted during the given packet duration interval (τ) [26]. The probability that zero packet is generated (i.e., no collision) during this interval is given by

$$\Pr(0) = e^{-(\lambda\tau)} \quad (3.2.3\text{-}3)$$

Therefore, the probability of packet collision is given by

$$\Pr[\text{collsion}] = 1 - \Pr(0) \quad (3.2.3\text{-}4)$$

Figure 3-9 shows simulation results of packet collision probability with increasing number of BSR nodes.

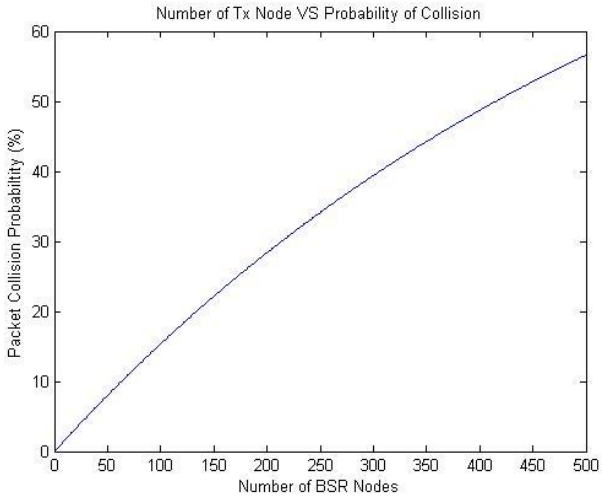

Figure 3-9: Packet Collision Probability vs. Number of BSR Nodes

After taking CS into consideration, the probability of packet collision can be derived by

$$\Pr[\text{collision}] = \left(1 - \mathrm{P}_{successful}\right)(1 - \Pr(0)) \qquad (3.2.3\text{-}4)$$

where $\mathrm{P}_{successful}$ is the probability that CS gives a correct decision whether the channel is clear or not. Figure 3-10 shows that, with $\mathrm{P}_{successful}$ increasing, the Pr [collision] is decreased.

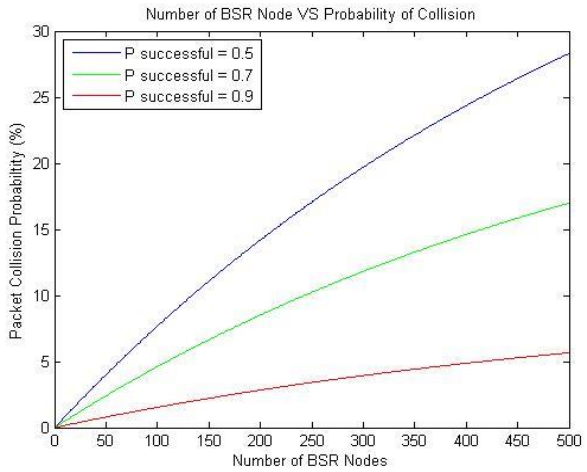

Figure 3-10: Packet Collision Probability vs. Number of BSR Nodes with CS

3.2.4 Design Drawbacks

Due to the special usage environment, concerns exist regarding whether or not all nodes will work within a space suit. A space suit consists of various layers, including multiple metallic layers which are radio opaque at Ultra High Frequency (UHF) [27]. All wireless signals, which are at UHF, can only be transmitted inside a space suit, and the signal is attenuated due to path loss and antenna mismatch loss. The signal becomes weaker as distance increases. For example, if a node located at the left wrist (14) (Figure 3-11) is transmitting a data packet, another node at the left ankle (10) may consider the data packet to be a noise and consequently detect an idle channel. In this case, packet collision is not avoided by sampling channel energy (CS), meaning that the Type I MAC layer has potential for undetected packet collisions.

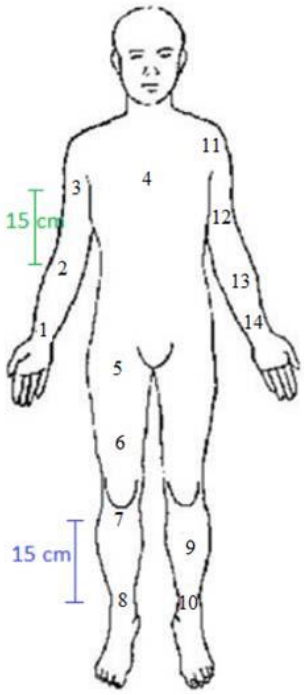

Figure 3-11: Radio locations for intra-suit wireless propagation [27]

3.3 Type II MAC layer protocol design

Type II MAC layer protocol is designed to eliminate packet collisions. A GR initiated based MAC (GRI-MAC) layer is proposed in this study as a Type II MAC layer design in order to use the GR node to control BSR nodes. BSR nodes transmit data packet only when they receive an indication from the GR node. Every data transmission initiated by the GR node can guarantee only one data packet transmission at a time, thereby eliminating the packet collision issue.

3.3.1 BSR Initiated Based MAC Layer Design

3.3.1.1 Definitions

Beacon: As shown in Figure 3-12, beacon contains sync word, ID, and Parity Check bit. Beacon transmits from GR node to BSR nodes to indicate the BSR node with identical ID in order to give a data packet transmission. Length of the beacon is calculated by Equation (3.3.1-1).

$$\text{Beacon Length} = B_{length} = \left(8n_{sync} + 8\right)\left(\frac{1}{f_{tx}}\right) \quad (3.3.1\text{-}1)$$

where, n_{sync} is the number of bytes of sync word, and f_{tx} is transmission rate. B_{length} is 3.2ms with 3 bytes sync word and 10kbit/s transmission rate.

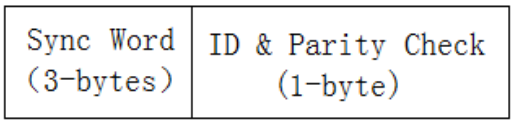

Figure 3-12: Beacon Frame

Beacon Gap: A time period between beacons is called beacon gap (BG). During BG, the GR node switches from transmit (TX) mode to receiving (RX) mode in order to detect channel status. BG must be long enough to determine if a data packet is coming or just an idle channel. BG length can be calculated as:

$$\text{Beacon Gap Length} = BG_{length} = \left(8n_{sync}\right)\left(\frac{\mathbf{1}}{\boldsymbol{f_{tx}}}\right) \quad (3.3.1\text{-}2)$$

where n_{sync} is the number of byte of sync word, and f_{tx} is the transmission rate. The current BG_{length} is 2.4ms with 3 bytes sync word and 10kbit/s transmission rate.

Minimum Listening Time: Minimum listening time (MLT) is the minimum time required for the BSR node to wake up to listen to the channel. MLT length must cover at least two lengths of beacon and one BG length to ensure that at least one entire beacon is detected. MLT can be calculated as:

$$MLT = 2B_{length} + BG_{length} \quad (3.3.1\text{-}3)$$

The current MLT is$(2 \times 3.2 + 3.6)ms = 10ms$

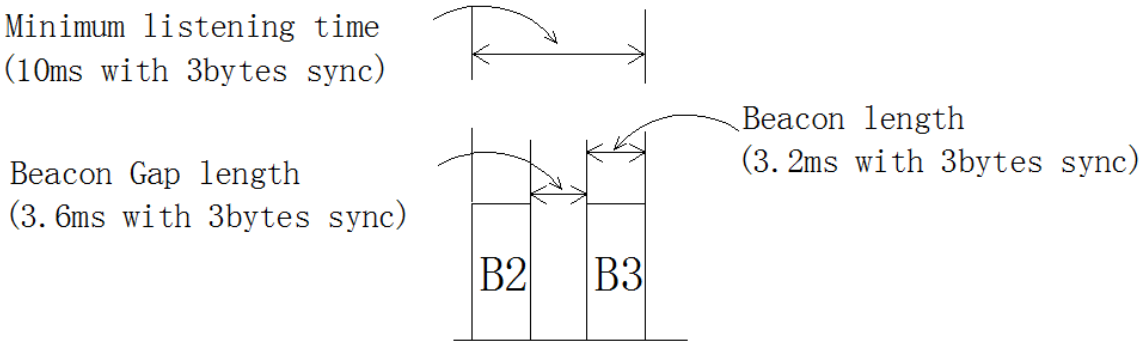

Figure 3-13: Concepts of GWRI-MAC Design

3.3.1.2 Design Description

GR based MAC (GRI-MAC) is a receiver-initiated asynchronous MAC protocol.

GR node process:

A GR node keeps the radio on in order to periodically broadcast beacon and detects channel. GR node's working process is shown in Figure 3-14. After broadcasting a beacon, a GR node switches from Tx mode to Rx mode with BG_{length} to detect any coming packet. If no packet is received during BG, the GR node switches to TX mode to broadcast a beacon with another ID. The GR node broadcasts beacons with pre-set order (ID number from 1 to n), and begins again when the beacon with the last ID number is sent. During a BG, if a GR node listens to an incoming data packet, the GR node continues in Rx mode until the entire packet is received. When data packet receiving is complete, the GR node sends an ACK command to intend BSR node to indicate a correct reception. Then, the GR node continues to broadcast beacon with next ID number.

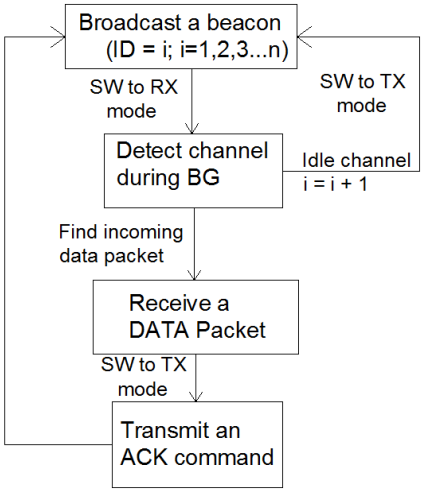

Figure 3-14: Working Process of GR node

BSR node process:

A BSR turns on its radio to listen to beacons whenever the node is ready to transmit a data packet. If no beacon is detected within MLT indicating, meaning that another BSR node data packet is being transmitted, the BSR turns to sleep mode for a short period equal to the longest data packet transmission time. After finding a beacon, a BSR node compares the beacon ID with its own ID in order to estimate time of detecting the intended beacon. If the time is greater than twice the Temperature Compensated Crystal Oscillator (TCXO) stabilized time (T_oscillation), the BSR node sleeps for the estimated time. Otherwise the BSR node extends its listening time to detect the intended beacon. When the intended beacon is found, the BSR node begins to transmit a data packet. If the BSR node receives an ACK command or detects a low energy level, it goes to a sleep-sampling period to wait for the next transmission cycle. The entire working process is shown in Figure 3-15.

Timing diagrams for various scenarios are shown in Figure 3-16, Figure 3-17, and Figure 3-18. Figure 3-16 demonstrates that BSR Node1 wakes up to listen to beacons while BSR Node3 transmits the data packet, thereby preventing Node1 from finding a beacon within MLT. After Node1 listens to the channel for MLT, it goes to sleep for a period (equal to the longest data packet transmission time) and then wakes up to detect the beacon again. BSR Node3 wakes up earlier than Node1 and finds a beacon with only one ID number ahead of the expected beacon. Therefore, Node3 extends its listening time until detecting the intended beacon.

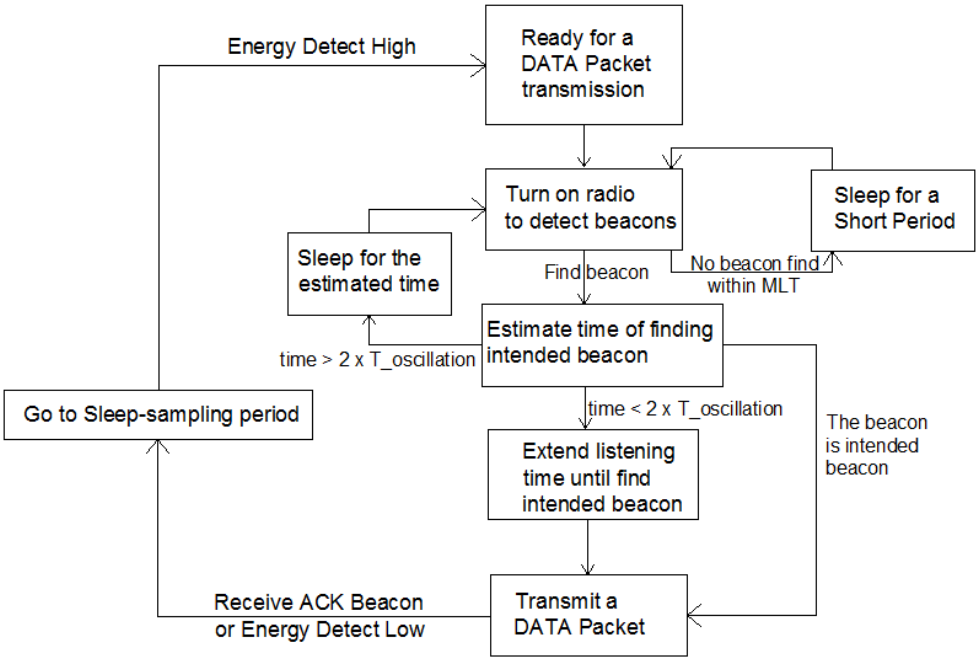

Figure 3-15: Working Process of BSR node

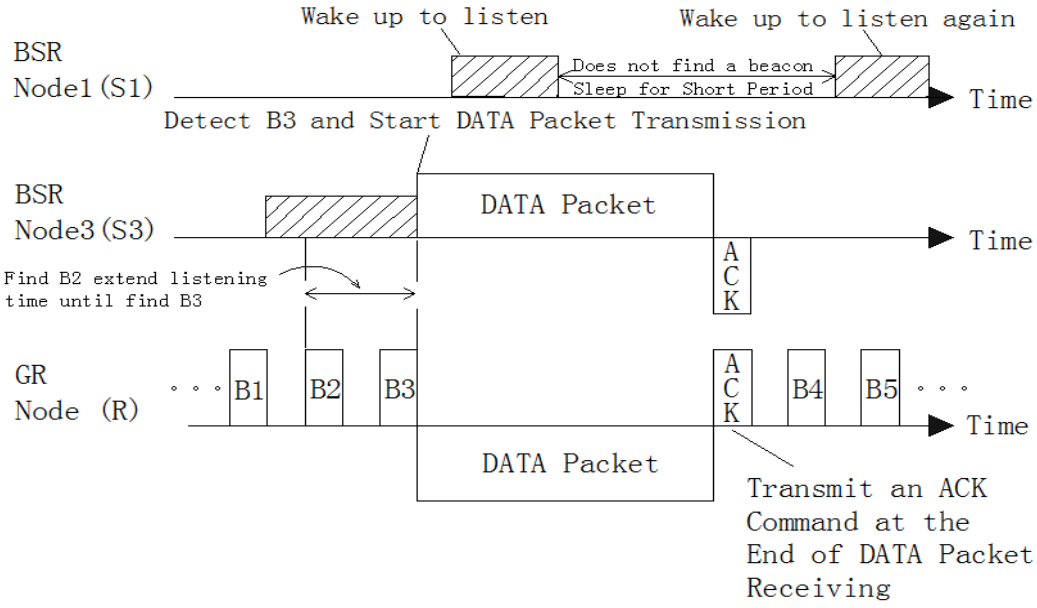

Figure 3-16: Timing Diagram of Scenario one

Figure 3-17 shows that, although BSR Node6 wakes up approximately one beacon time earlier than BSR Node3, Node3 transmits a data packet earlier because Node3 detects its intended beacon (with ID of Node3) before Node6 does. During data packet transmission of Node3, Node6 no longer finds beacons, so it goes to sleep for a short period (equal to the longest data packet transmission time) and then wakes up to detect the beacon again.

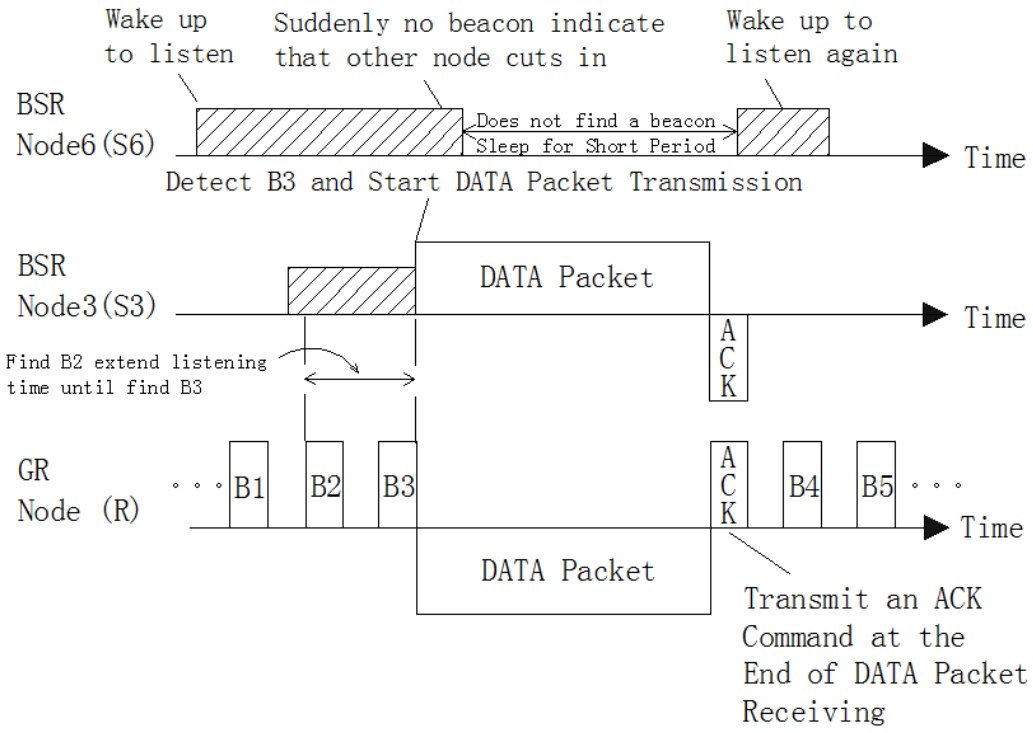

Figure 3-17: Timing Diagram of Scenario two

Figure 3-18 illustrates that, BSR Node15 wakes up to detect beacon with the ID of Node2. After estimating that the time of receiving beacon with ID of Node15 is longer than twice of TCXO stabilized time, Node15 goes to sleep for an estimated time and wakes up approximately one beacon ahead of its intended beacon. If another BSR node does a data packet transmission during Node15 sleep time, the intended beacon for Node15 will be delayed. In this case that intended beacon is delayed, node15 wakes up to detect a beacon and re-estimates another sleep time.

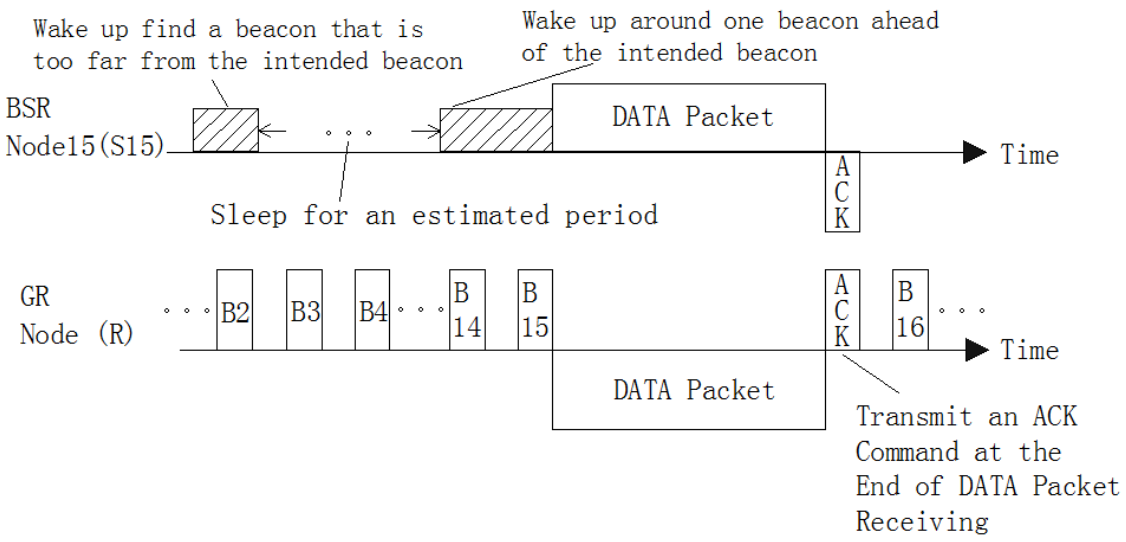

Figure 3-18: Timing Diagram of Scenario three

3.3.2 Simulation and Analysis

Although GRI-MAC layer design eliminates packet collision and increases system reliability, the design incurs extra energy costs due to idle listening and overhearing. Average listening time (ALT) for individual BSR nodes must be quantified, consequently identifying the corresponding max-sampling rate by using Equation 2.3.6-18.

Average listening time:

ALT is the average time that a BSR node listens to find its intended beacon. The BSR node process (Section 3.3.1) shows that the listening time for a BSR node has three possible conditions: detect intended beacon within MLT (Figure 3-19), detect intended beacon in extended listening time (estimated sleep time < 2xT_oscillation) (Figure 3-20), and detect intended beacon in the next wake-up time (Figure 3-21). ALT can be calculated by the following Equation (3.3.2-1):

$$\boldsymbol{ALT} = \sum_{\mathbf{i=1}}^{\mathbf{3}} \boldsymbol{T}(\boldsymbol{i})\,\boldsymbol{Pr}(\boldsymbol{i}) = \boldsymbol{T}(\mathbf{1})\,\mathbf{Pr}(\mathbf{1}) + \boldsymbol{T}(\mathbf{2})\,\mathbf{Pr}(\mathbf{2}) + \boldsymbol{T}(\mathbf{3})\,\mathbf{Pr}(\mathbf{3}) \qquad (3.3.2\text{-}1)$$

where $\boldsymbol{T}(\boldsymbol{i})$ is the listening time for each condition and $\boldsymbol{Pr}(\boldsymbol{i})$ is the probability for each condition.

In the first condition, the intended beacon can be found at the beginning of MLT or at the end of MLT. Therefore, $\boldsymbol{T(1)}$ must be a random number located within $[B_{length}, 2B_{length} + BG_{length}]$; $\boldsymbol{T(1)}$'s expectation value is $1.5B_{length} + 0.5BG_{length}$. The $\mathbf{Pr(1)}$ is 1/N, where N is the number of BSR nodes.

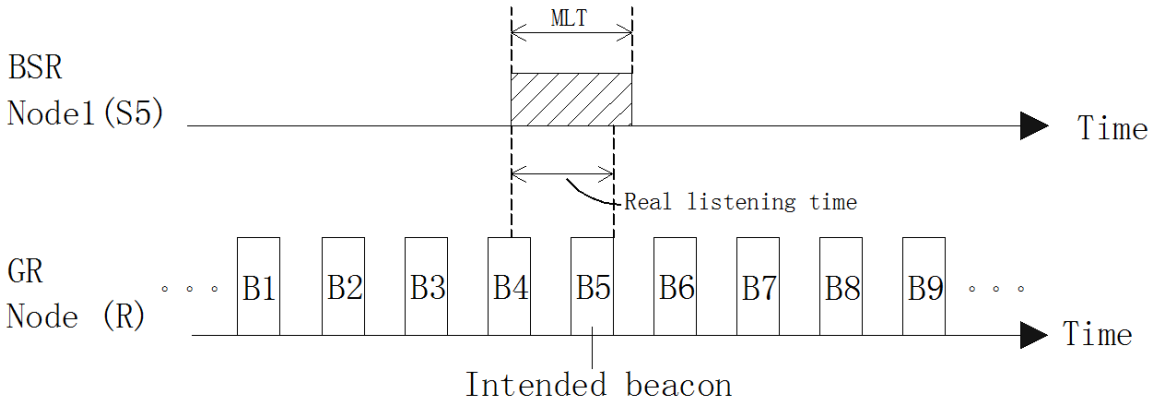

Figure 3-19: Condition 1: Detect intended beacon within MLT

In the second condition, $\boldsymbol{T(2)}\,\mathbf{Pr(2)}$ can be calculated by the following equation:

$$\boldsymbol{T(2)}\,\mathbf{Pr(2)} = \left(\frac{\mathbf{1}}{\boldsymbol{e}}\right)\sum_{\boldsymbol{i=1}}^{\boldsymbol{e}}\left(MLT + \boldsymbol{i}\left(B_{length} + BG_{length}\right)\right)\left(\frac{\boldsymbol{e}}{\boldsymbol{N}}\right) \qquad (3.3.2\text{-}2)$$

where *e* indicates the maximum number difference between detected beacon and intended beacon under condition 2. After MLT, if the beacon number extends by 1, listening time extends by $\left(B_{length} + BG_{length}\right)$. $\left(\frac{\boldsymbol{e}}{\boldsymbol{N}}\right)$ reflecting the probability of the second condition.

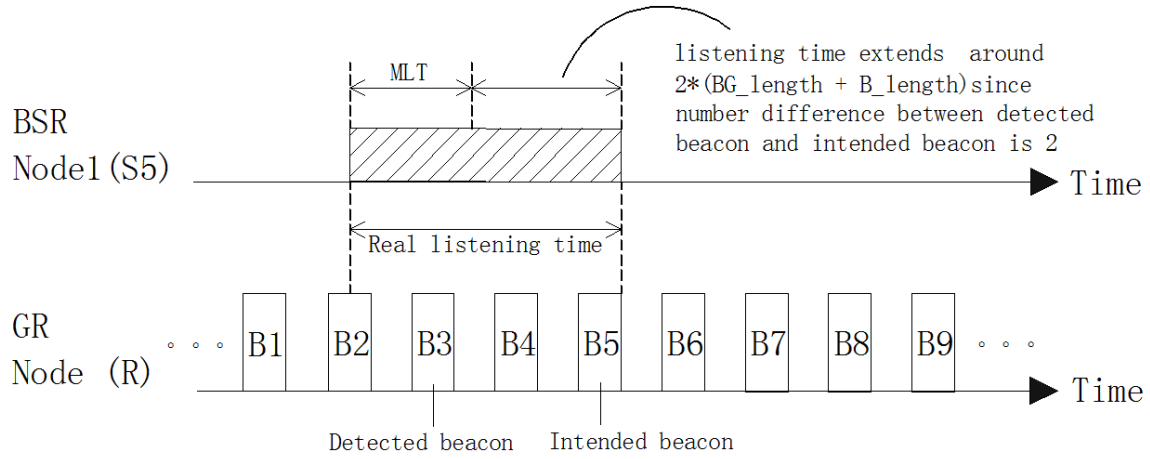

Figure 3-20: Condition 2: Detect intended beacon in extended listening time (Estimated sleep time < 2xT_oscillation)

In the third condition, the listening time, $\boldsymbol{T(3)}$, is approximately 2 MLT. The probability of the third condition,$\mathbf{Pr(3)}$ is$\left(\frac{\boldsymbol{N-e-1}}{\boldsymbol{N}}\right)$.

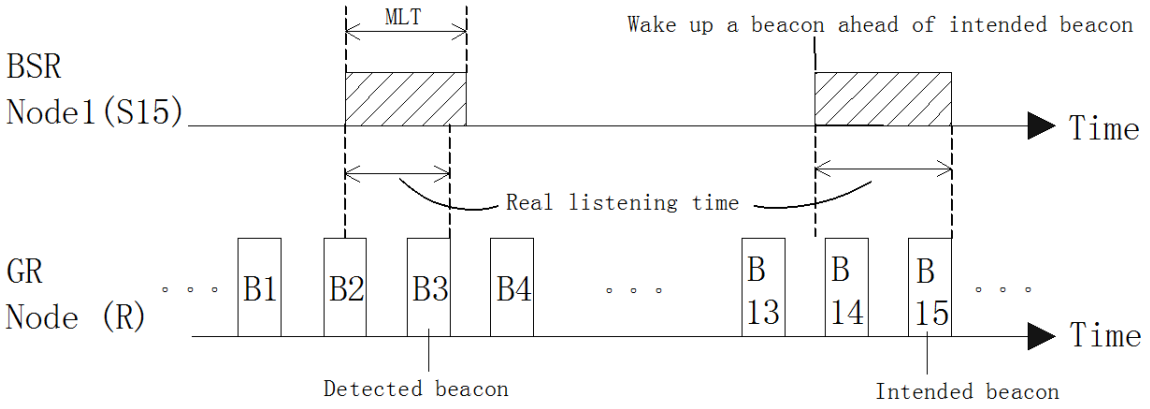

Figure 3-21: Condition 2: Detect intended beacon in next waking-up time (Estimated sleep time < 2xT_oscillation)

Assuming T_oscillation is 10ms, a simulation result of ALT vs. Number of BSR nodes is shown in Figure 3-22. ALT converges to 18ms because Condition 3 will dominate ALT calculation with an increasing number of BSR nodes. From Figure 2-31 we can easily find the maximum data

sampling rate of our system working under current MAC layer design (time spent in Rx mode is 18ms).

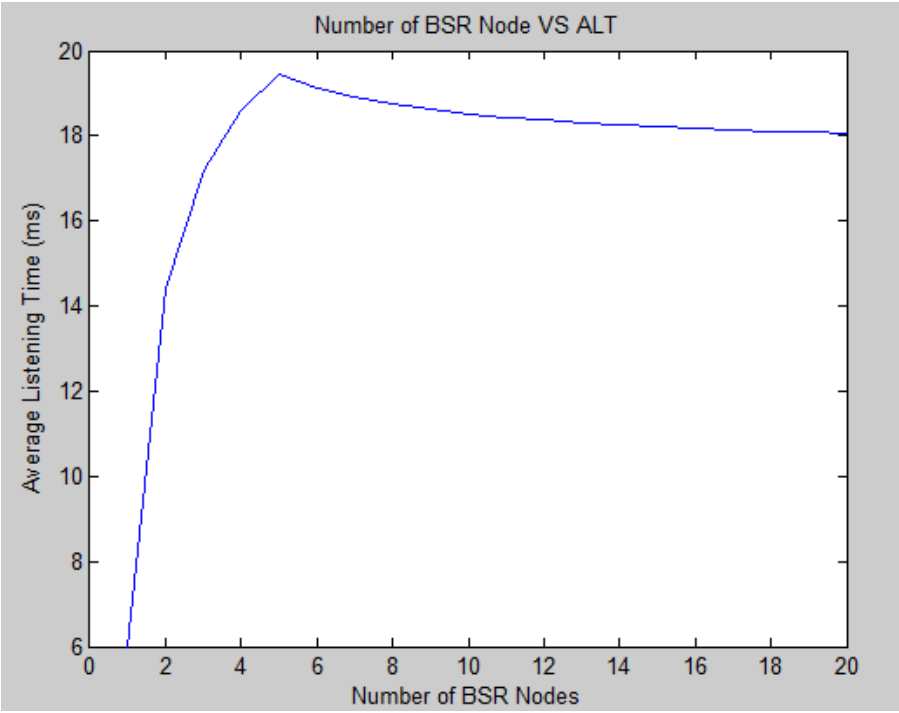

Figure 3-22: ALT vs. Number of BSR nodes

3.3.3 Design Drawbacks

This design contains three primary drawbacks:

- **Idle listening:** BSR nodes must wake up for a period in order to listen to their beacons before transmitting a data packet. Although the period is short and the wasted energy is affordable, the BSR nodes must prolong sleep time in order to recover the extra energy cost.
- **Overhearing:** A BSR node likely listens to the beacons with IDs of other BSR nodes.

- **Latency:** Because of an increasing number of nodes, a BSR node requires longer time waiting for its intended beacon (a node will turn to sleep mode first and turn back to Rx mode if the waiting time is too long), thereby increasing the latency between packet transmissions.

3.4 Conclusions

In this chapter, we provided a survey of energy efficient MAC protocols and proposed two MAC layer designs which fit the EHWSN of interest in this thesis. CS-ALOHA MAC layer design has high energy utilization and GRI-MAC layer design has high reliability. A summary of these two MAC layer performance metrics designs is presented in Table 3-1.

Table 3-1: Summary of Metric of CSA-MAC and GRI-MAC

	CS-ALOHA MAC	**GRI-MAC**
Packet collision	YES	NO
Idle listening	NO	YES
Overhearing	NO	YES
Overemitting	NO	NO
Overhead	YES	YES
Latency	NO	YES
Energy utilization	Higher	Lower
Reliable	Lower	Higher
Average listening time	0	18ms
MDSR (EMG sensor)	$\approx 4.5Hz$	$\approx 4.3Hz$

Chapter 4 - Conclusion and Future Work

4.1 Summary

Energy harvesting wireless sensor networks (EHWSNs) have gained popularity recently due to their independence from utility power [5], longer transceiver node lifetime, and safety in special environments (e.g., inside space suits). This thesis, which discusses both physical layer and medium access control (MAC) layer design, demonstrates EHWSN design inside a space suit. The EHWSN in this thesis considered a star topology network, including multiple bio-sensor radio (BSR) nodes and one gateway radio (GR) node. A GR node acts as a central node to receive data packets sent by BSR nodes and organize the network. The gateway node is assumed to be power-unconstrained.

The wireless sensor network (WSN) in this research is considered as an EHWSN because all BSR nodes are powered by thermal energy harvesting system (TEHS) which provides very low output power ($\approx 1mW$). An experiment is conducted to replicate real thermal-energy flow in the proposed hardware to estimate output power during practical use. The measurement result (output power = 0.87mW) is a key parameter to calculate the BSR node duty cycle.

Another key parameter for duty cycle calculation is BSR node-consumed power under various modes of operation. A functional BSR node with transmit (Tx) mode and receive (Rx) mode was implemented to measure power consumption under real situations. Based on the measurements, Tx mode consumes approximately 250mW, Rx mode consumes approximately 150mW, and duty cycle is calculated to be approximately 0.4%. Results of duty cycle calculation and maximum data sampling rate (MDSR) analysis based on measurements provided guidance for the MAC layer design.

A survey was conducted to obtain a broad outline for existing MAC layer designs. After considering previous analysis and modifying existing MAC layers, two MAC layer designs, CSA (Carrier Sense ALOHA) -MAC layer and GRI (gateway radio initiated)-MAC layer, were presented. CSA-MAC layer and GRI-MAC layer designs which shift power consumption pressure from BSR nodes to the GR node are feasible for our extremely low duty cycle EHWSN. CSA-MAC layer has a little bit higher maximum data sampling rate and GRI-MAC is more reliable.

4.2 Future Work

Due to the extremely low duty cycle ($\leq 0.4\%$) and low Tx rate (10kbit/s), MDSR in this system is only 1.5Hz~ 4.5Hz, which is far less than biosensor signal sampling rate requirement (Table 2-2). Two aspects including TEHS and Tx rate must be improved in order to realize higher MDSR. Current TEHS having only 0.87mW overall output power is designed for using only two parallel thermal electrical generators (TEGs) and more than two-thirds of harvested energy is wasted in ultra-low voltage step-up converter (UVSC). In order to increase TEHS output power, a new structure with more TEGs must be designed and a new USVC must be found. Tx rate is limited primarily by the current demodulation method. As link budget studies suggest significant link margin exist within the envisioned space suit application [27], new methods can be employed to achieve higher Tx rate. If we can increase the Tx rate from 10kbit/s to 1Mbit/s without changing anything else of this system, MDSR can reach as high as 300Hz which will meet almost all the biosensor signals sampling rate requirements. Obtained MDSR value currently is based primarily on calculation and simulation results. In order to obtain more accurate MDSR of EHWSN under real situation, the two types of MAC layer designs proposed in Chapter 3 should be implemented and tested.

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Appendix A - Table of Acronyms

ALT	Average Listening Time
ADC	Analog To Digital Converter
ALT	Average Listening Time
AM	Active Mode
BG	Beacon Gap
B-MAC	Berkeley Media Access Control
BSR	Bio-Sensor Radio
CSA	Carrier Sense ALOHA Based
CCA	Clear Channel Assessment
CRC	Cyclic Redundancy Check
CS	Carrier Sense
CS	Channel Energy
CSMA	Carrier Sense Multiple Access
DB	Daughter Board
DSM	Data Sampling Mode
ECG	Electrocardiogram
EH	Energy Harvesting
EHS	Energy Harvesting System
EHWSN	Energy Harvesting Wireless Sensor Network
EMG	Electromyography
FPGA	Field Programmable Gate Array
GND	Ground
GR	Gateway Radio
GRI	Gateway Radio Initialized
GRI-MAC	GR Initiated Based MAC
KANDB	K-State-NASA Body Area Network Development Board
LPL	Low Power Listening
MAC	Medium Access Control
MB	Mother Board
MDSR	Maximum Data Sampling Rate
MLT	Minimum Listening Time
NSM	Nominal Sleep Mode
PHY	Physical
PO	Pulse Oximeter
RFIC	Radio Frequency Integrated Circuit
RI-MAC	Receiver-Initiated MAC

RRS	Respiration Rate Senor
RSSI	Received Signal Strength Indicator
RTS-CTS	Ready To Send-Clear To Send
RX	Receiving
SASTN	Single Cluster Star Topology Network
SM	Sleep Mode
SPI	Serial Peripheral Interface
TCXO	Temperature Compensated Crystal Oscillator
TEG	Thermal Electric Generator
TEHS	Thermal Energy Harvesting System
TTNSM	total time of the NSM
TX	Transmit
UHF	Ultra High Frequency
UVSC	Ultralow-Voltage Step-Up Converter
Vout	Output Voltage
WSN	Wireless Sensor Network