NOISE CHARACTERIZATION OF TRANSISTORS IN 0.25µm AND 0.5µm SILICON-ON-SAPPHIRE PROCESSES

by

KEITH BURTON ALBERS

B.S., Kansas State University, 2008

A THESIS

submitted in partial fulfillment of the

requirements for the degree

MASTER OF SCIENCE

Department of Electrical and Computer Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2010

Approved by:

Major Professor
Dr. William B. Kuhn

ABSTRACT

A technique for measuring and characterizing transistor noise is presented. The primary goal of the measurements is to locate the 1/f noise corner for select transistors in Silicon-on-Sapphire processes. Additionally, the magnitude of the background channel noise of each transistor is measured. With this data, integrated circuit (IC) engineers will have a qualitative and quantitative resource for selecting transistors in designs with low noise requirements.

During tests, transistor noise behavioral change is investigated over varying channel lengths, device type (N-type and P-type), threshold voltage, and bias voltage levels. Noise improvements for increased channel lengths from minimal, 1.0μm, and 4.0μm are measured. Transistors with medium and high threshold voltages are tested for comparison of their noise performance. The bias voltages are chosen to represent typical design values used in practice, with approximately 400 mV overdrive and a drain-to-source voltage range of 0.5 to 3.0V.

The transistors subjected to tests are custom designed in Peregrine's 0.5μm (FC) and 0.25μm (GC) Silicon-on-Sapphire (SOS) processes. In order to allow channel current noise to dominate over other circuit noise, the transistors have extraordinarily large aspect ratios (~2500 - 5000).

The transistor noise produced is amplified and measured over a frequency range of 1kHz - 100MHz. This range allows the measurement of each device's low and high frequency noise spectrum and resulting noise corner.

Table of Contents

List of Figures

List of Tables

Acknowledgements

I would like to thank Dr. William B. Kuhn for his seemingly unlimited wisdom, enthusiasm, and support for this research and throughout my time as a graduate student at Kansas State University. His commitment as a mentor and a friend made this research possible. I would also like to thank my graduate committee, Dr. Don Gruenbacher and Dr. Andrew Rys, for dedicating their time and thoughts.

I would also like to thank Honeywell KCP and Sandia National Laboratories for this opportunity and their support. Finally, I would like to thank our integrated circuit foundry, Peregrine Semiconductor, for allowing us to publish our results.

CHAPTER 1 - Introduction

1.1. What's so Important About 1/f Noise?

The demand for smaller and faster devices over the years has pushed integrated circuit (IC) processes to astonishingly small sizes. Although this trend has its benefits, miniaturization of the transistor imposes inherent complications when designing low noise circuits. To make matters worse, standard IC supply voltages have remained the same for reasons of compatibility with existing systems. This can result in even more complications such as noise performance and device lifetime.

Although many IC designers couldn't care less about a transistor producing -100 dBm/Hz at 10 kHz, someone designing a frequency synthesizer might cringe at this when thinking of what it might do to their phase noise. When it comes to circuits like this , minimal noise power spectral density (PSD) is the name of the game. Many components throughout these systems contribute to the total noise. One of the most fundamental of these is transistors and their associated noise spectrum, namely the frequency of their 1/f noise corner.

A specific example were 1/f noise characteristics play a vital role in system performance is the charge pump in a divide-by-N synthesizer as seen in Figure 1-1. Accompanying the diagram are illustrations of noise spectrums throughout the circuit.

The synthesizer works by trying to match the phase of a `desired output phase Θ_f, once divided by N, with a reference phase Θ_r. Any output phase deviation (i.e. $\Theta_r \neq \Theta_f$) is detected by the phase-frequency detector (PFD) which commands the charge pumps (CP) to source or sync current pulses to or from the loop filter. This then applies the appropriate voltage and resulting frequency and phase changes at the voltage-controlled oscillator (VCO).

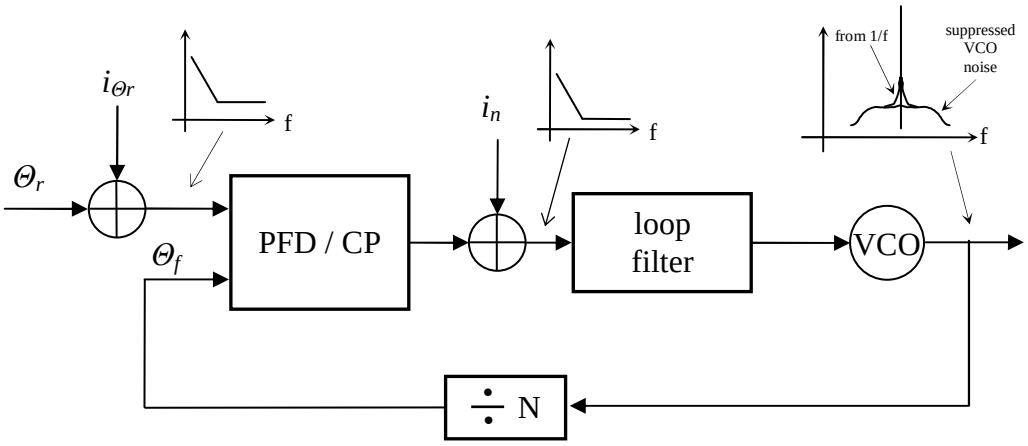


Figure 1-1: Result of phase noise in a divide-by-N synthesizer.

The problem here arises from the noise associated with the charge pump current pulses, shown as the injection of i_n, which ultimately causes jitter in the output frequency/phase. Jitter in the VCO frequency/phase is another concern, but is normally suppressed by the loop. Unfortunately, the transfer function from i_n to the VCO output phase noise is the same as that from the reference to the output (modified by the phase-detector constant), such that i_n directly modulates the VCO phase. Although the magnitude of this noise is usually low, it is noticeable close to the carrier due to its 1/f

nature. To make matters worse, the 1/f noise associated with the reference phase coming into the PFD also contributes to the overall phase noise.

So what does this mean in terms of overall system performance? The figure on the following page illustrates how a poor 1/f noise corner can contribute to the phase noise and degradation of a system. Shown is a case of *reciprocal mixing* in which a smaller signal is drowned out due to the presence of a large interferer.

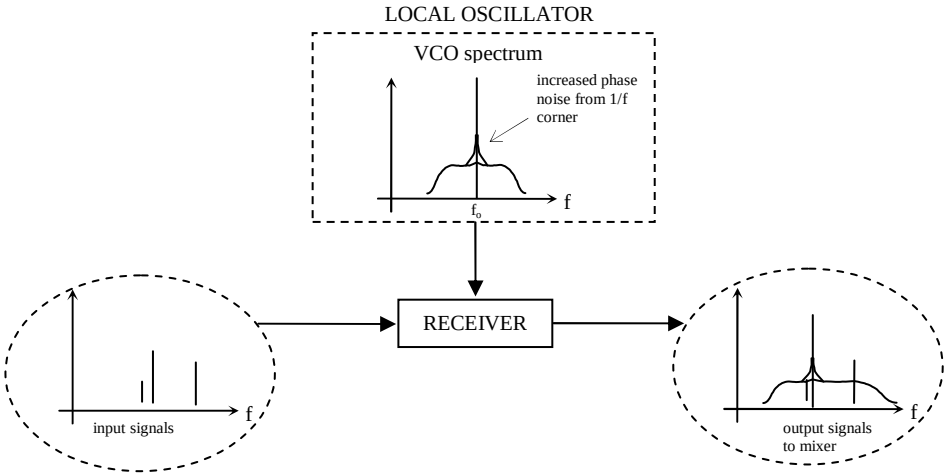


Figure 1-2: Degradation of channel resolution due to 1/f noise performance.

Issues similar to this become paramount in systems where a decent SNR could make all the difference for signal detection. Ultimately, the transistor noise is in part responsible for the overall signal to noise ratio at a device's output.

1.2. Previous Work

There have been many publications on MOSFET 1/f noise, mostly concentrating on its origins and how to develop more accurate simulations for analysis purposes [1] – [6]. Although this knowledge is beneficial, it is not immediately useful to an IC engineer who

needs to know specific noise values or simply which transistor will perform best for them in a specific process.

The target of this thesis is to characterize the noise performance of Peregrine Semiconductor's 0.5μm (FC) and 0.25μm (GC) processes. In doing so, the identification of the 1/f noise corner, along with the background device channel noise, will enable the approximation of noise levels at any desired frequency (Section 2.3).

Studies in [7] investigate 1/f noise for weak, moderate, and strong inversion of Peregrine's Silicon-on-Sapphire FC process. The research provides data for noise variations over increasing nFET and pFET channel lengths, but failed to go to high enough frequencies to identify the noise corner. Additionally, the experiments do not cover the noise variations witnessed here in Chapter 5 for varying parameters (e.g. drain-to-source voltage). Lastly, the background channel noise magnitude is not reported. With that said, their experimental setup does offer a good starting point for the work conducted here, and was leveraged in this work.

1.3. Thesis Outline

Chapter 2 begins with a brief overview of device physics and transistor operation to introduce common terminology used throughout the remainder of the thesis. It then introduces different types of noise sources found in circuits. Since the main focus is the 1/f noise spectrum of transistors, the majority of this chapter concerns the origins of 1/f noise in semiconductors as described by today's leading theories. Chapter 2 then discusses the parameters chosen to vary during testing, and their expected behavioral changes on noise.

Chapter 3 covers the design of the tested transistors fabricated in Peregrine's 0.5μm and 0.25μm SOS processes. Discussions include how to ensure the measured noise is the channel noise produced by a tested transistor and not additive circuit noise from the experimental setup.

In Chapter 4, the noise measurement setup is elaborated. The topics covered include basic circuit topography and methodology for collecting the noise data.

The acquired noise data is presented and analyzed in Chapter 5. The analysis characterizes each transistor offered in the two IC processes on a noise performance basis. This includes broadband noise levels and the 1/f noise corner for each device over the varied parameters.

Conclusions of this research are in Chapter 6 along with some implications of the results. An appendix is included in this thesis to summarize the equations in the previous chapters.

CHAPTER 2 – Noise Theory

2.1 A Brief Review of Transistor Operation

Throughout this document various terms will be used in reference to transistors. It is therefore beneficial to provide a brief overview of them. Figure 2-1 illustrates the two basic types of devices offered in the targeted Silicon-on-Sapphire IC process.

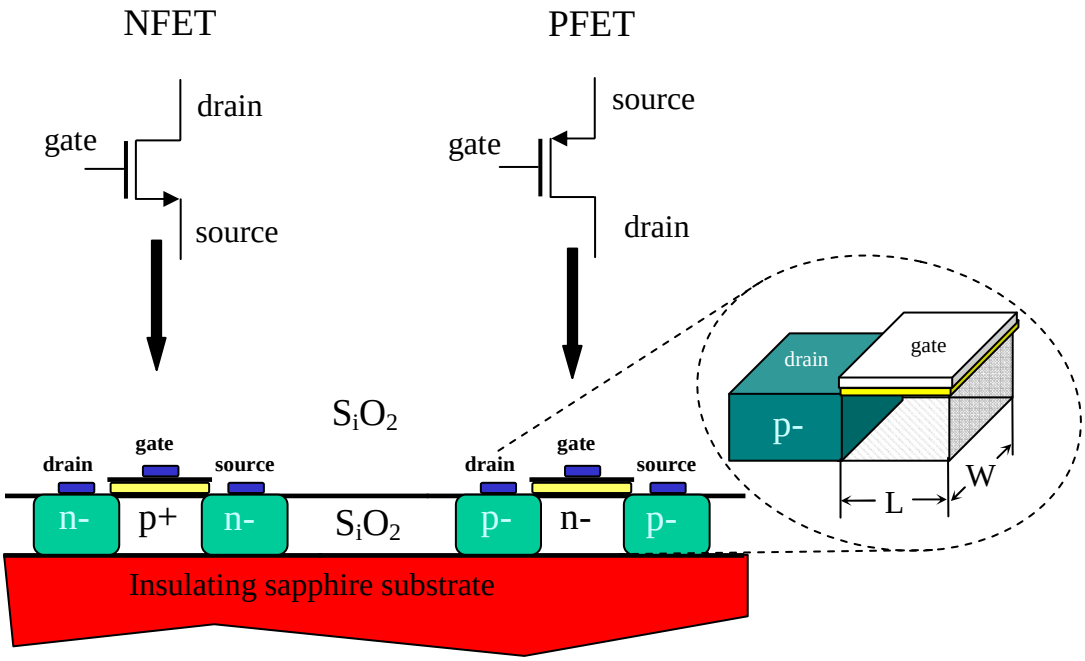


Figure 2-1: Transistor schematic symbol and corresponding IC layout.

Shown in Figure 2-1 are fully-depleted N-channel and P-channel transistors with their respective doping patterns. It should be noted the typical substrate in CMOS processes is S_iO_2, however an insulating sapphire substrate is used in the processes

concerned here. This substrate is *fully insulating*, which virtually eliminates the danger of latch-up, while also increasing performance by reduction of parasitic capacitances.

Device operation begins with forming a channel in the region under the gate, of design specified length (L) and width (W), by applying a gate-to-source voltage (V_{GS}). The conductivity of the induced channel depends on how far V_{GS} has surpassed a device specific *threshold* voltage (V_{th}). The amount of V_{GS} needed to form a channel is dependant upon the doping concentration of a particular device. This study considers both medium and high threshold transistors of both types for Peregrine Semiconductor's 0.25µm and 0.5µm processes. The table shown below summarizes the naming conventions used for both processes.

Table 2-1: Threshold naming conventions for 0.25µm and 0.5µm processes.

	Process	
Type-Threshold	**0.25µm (GC)**	**0.5µm (FC)**
N-medium	RN	NL
N-high	HN	RN
P-medium	RP	PL
P-high	HP	RP

This threshold potential is the point where either negative or positive charge carriers, depending on device type, are attracted from the source region. Once the channel is formed, application of a drain-to-source (V_{DS}) voltage allows current to flow through the channel. The magnitude of V_{DS} relative to the *overdrive* voltage (V_{GS}-V_{th}) determines if the device is operating in the saturation (active) or triode (linear) regions. Once the

transistor dimensions and overdrive are defined, the *transconductance* of a device is found (for low overdrive voltages up to a few tenths of a volt) as

$$g_m = \frac{\mu C_{OX} W}{L}(V_{GS} - V_{th}). \tag{1}$$

Figure 2-2 demonstrates an N-type transistor for both regions of operation with their respective equations for DC current.

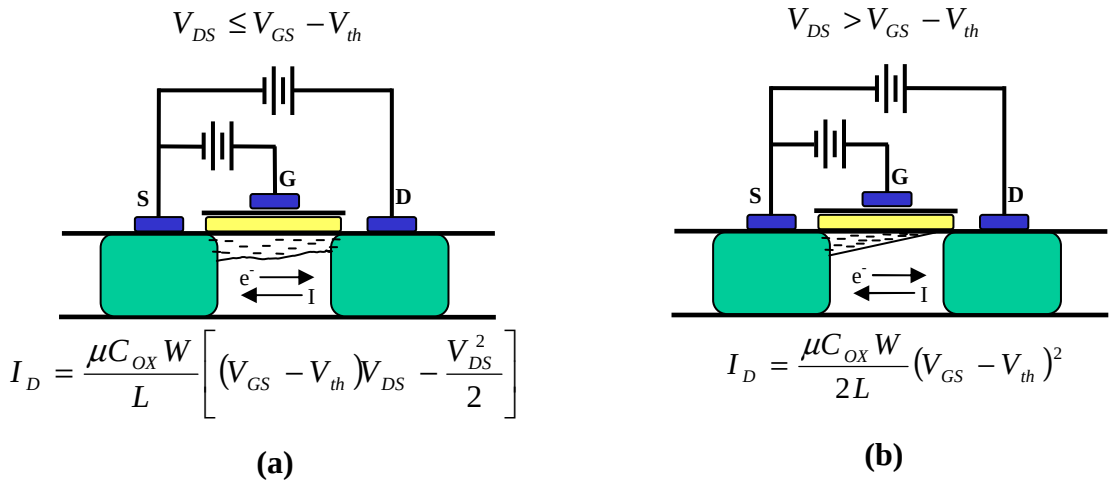


Figure 2-2: Device operating in triode (a) and saturation (b) regions.

The segment of the channel in Figure 2-2(b) which is *pinched* off is what distinguishes a device as being saturated. Here, saturation implies that increasing V_{DS} beyond the point where the channel is pinched-off has little effect on the devices current (i.e. I_D is no longer linearly related to V_{DS} as in triode region). As V_{DS} increases further, the pinched off point of the channel continues to recede towards the source. The graph below in Figure 2-3 exemplifies typical drain current (I_D) versus V_{DS} voltage.

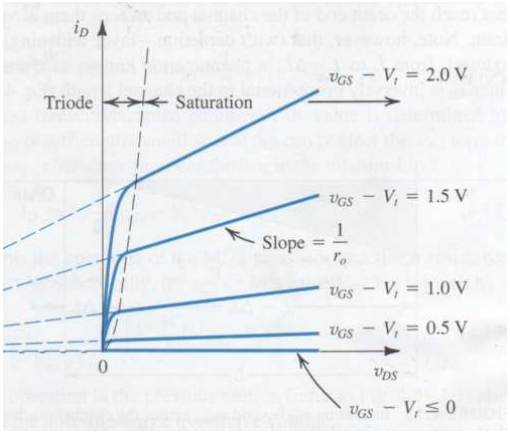


Figure 2-3: Typical transistor drain current versus V_{DS} curves [Sedra and Smith].

An important characteristic of the I_D curves, especially for sub-micron devices, is their slope in the saturation region whose inverse defines the drain-to-souce resistance (r_o) of a particular device. This resistance (not captured by the simplified equations in in Figure 2-2(b)) results from channel length modulation as V_{DS} varies and plays an important role in calculating the current, as well as the noise produced by a transistor (Section 3.1).

2.2 Noise: Types and Origins

When someone hears the word *noise* it is usually associated with something undesired. In the world of electrical circuits, this definition is often not far off from the truth. It is fundamental and unavoidable as it is experienced in virtually every component that dissipates power; from passive devices, such as resistors, to active devices. Although noise is not a primary concern to many circuits, it can cause real problems to small-signal and highly sensitive circuits as described in Chapter 1. As with any problem in engineering, in order to mitigate something, it must first be understood.

The most fundamental of all noise sources is thermal noise and is in any medium with resistance capable of dissipating energy. The amount of available noise power in a given system is

$$P = kTB \quad (W) \tag{1}$$

where

k	Boltzmann's constant $1.38\text{x}10^{-23}$ (J/K);
T	temperature (K);
B	noise bandwidth (Hz).

The expression in (1) relates energy on a particle level with a given temperature over some equivalent bandwidth. In most cases, the noise is described on a "per-Hertz" basis which yields a noise power spectral density (PSD). When considering the transference of (1) to another system through a medium's resistance (R), the rms noise voltage or current PSD can be given as

$$v_{therm}^2 = 4kTR \quad \left(V^2 Hz^{-1}\right) \quad or \quad i_{therm}^2 = 4kTR^{-1} \quad \left(A^2 Hz^{-1}\right) \tag{2}$$

In (2), the multiplication by four appears when considering the transfer of power from one system to another whose mediums have the same resistance and are in thermodynamic equilibrium [8].

A standard way to schematically represent noise is by a voltage source in series with a medium's resistance as in Figure 2-4 (a). Alternatively, the Norton equivalent is shown in Figure 2-4 (b).

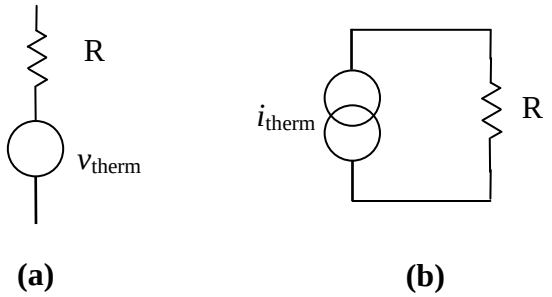


Figure 2-4: Circuit equivalent voltage (a) and current (b) noise sources.

As charged particles travel, they randomly collide with one another or with barriers of their medium. This drift of charged particles causes random, uniformly distributed fluctuations in current, and thus voltage, which are frequency independent giving thermal noise its more common name of *white* or *broadband* noise. As a point of reference, a 1kΩ resistor would yield approximately 4.0 nV/√Hz noise voltage.

The majority of the remaining types of sources usually involve solid-state physical devices, such as diodes or transistors. The specific types associated here are known as *shot* and *flicker* (1/f), and *generation-recombination* (g-r) noise. These sources are usually side effects of defects in the manufacturing process or inherent in the nature of the movement of charged particles through semiconductors.

2.3 Noise in Transistors

There are three main types of noise in transistors; background channel or broadband, 1/f, and generation-recombination noise. The term *background channel* noise can be thought of as the noise floor of transistors. Since the additional noise mechanisms typically create noise mainly at lower frequencies, the combination of these sources creates a *noise corner* at their intersection whose identity in transistors is a primary goal

in this research. It is therefore important to know what causes each noise type and what sort of parameters promote behavioral changes in them. Figure 2-5 illustrates the common definition of a device's noise corner. Explanation of the difference between the theoretical and actual observed background channel noise will come later in this section.

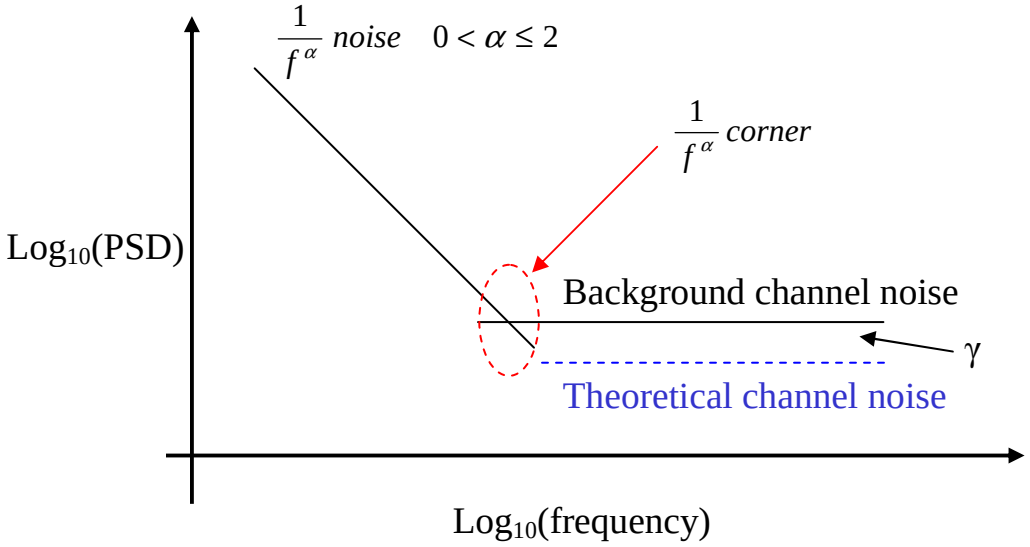


Figure 2-5: Transistor noise power spectral density and noise corner.

2.3.1 Transistor Broadband Noise

As a first step in the analysis of transistor noise, one must specify its region of operation. For purposes of this research, and as commonly seen in most RFIC circuits, transistor noise will be analyzed in the saturation region. The standard diagram of a transistor in saturation is illustrated in Figure 2-6.

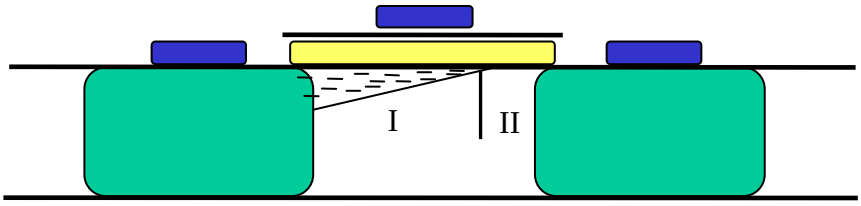


Figure 2-6: Device operating in saturation.

The channel in Figure 2-6 has two distinct regions. On the left (region I) is the effective channel length while the right hand region is the modulated pinch-off region. It is shown in [9] the only region which contributes to transistor thermal noise is region II.

The left-hand, or *gradual*, region is comprised of excess charges as a result of the electric field created by gate biasing. When under the influence of a V_{DS} voltage these charged particles experience collisions as partially described by thermal noise. An expression for broadband noise is given in [9], [10], and [11]. According to [10], while in moderate saturation, the effective channel length of the transistor is much greater than the mean free path of the traveling particle. Here, *mean free path* defines the average distance a charge particle travels without any collisions. Under these conditions, particles have regular collisions with the semiconductor lattice and other carriers as with thermal noise. It is then no surprise the gradual channel region is responsible for the background current noise, whose PSD is given as

$$S_W(f) = i_{ch}^2 = 4\gamma kTg_m \qquad (A^2 Hz^{-1}) \tag{3}$$

where

γ bias dependant noise factor;

g_m conductance of channel (S).

The noise-factor γ takes into account increased charge density and motion due to gate and V_{DS} voltage, respectively [10]. This distinguishes it from standard thermal noise voltage equations. Typical values of γ for larger channel length transistors are approximately 2/3 for moderate to strong channel inversions. It is important to note that γ is usually associated with g_{do}, which gives the transconductance of the channel with zero V_{DS} voltage, instead of g_m. In essence, g_{do} establishes a more traditional relation of (3) to thermal noise since there is no transverse electric field and the random collisions of particles are due to diffusion. For distinction, γ will be replaced with γ′ in this thesis due to non-zero V_{DS} voltages. The ratio of g_m to g_{do} can be approximated as one for longer effective channel lengths. However, the ratio begins to decrease as the channel lengths become shorter and as overdrive voltages increase [11], [12].

As V_{DS} voltage increases, the gradual channel shortens. At the point where the length of this region becomes less then the mean free path, the noise PSD described in (3) begins to fall apart. Under these conditions, the charged particles start experiencing less scattering and the noise tends towards a *shot noise* resemblance. This behavior describes discrete emission and capture of charged particles between two terminals through a medium, without considering collisions, in the presence of an electric field [11]. The time it takes to deposit this charge between the terminals is random and non-uniform, giving rise to its broadband nature [13]. The well known equation for shot noise and is expressed as

$$i_{n,shot}^2 = 2qI_{DC} \qquad (A^2Hz^{-1}) \tag{4}$$

where

q particle charge 1.602 x 10^{-19} (C);

I_{DC} dc current (A).

Since shot noise, like γ', is broadband, its effects can be incorporated with the measurement of the background channel noise through γ'.

2.3.2 Generation-Recombination Noise

A well known mechanism of noise experienced in semiconductors is known as generation-recombination (G-R) noise. This source is generally less discussed in research literature due to its typical low levels of total noise contribution when compared to 1/f noise (Section 2.3.2). The act of generation-recombination is simply the generation of electron-hole pairs and their eventual annihilation through recombination. The image in Figure 2-7 illustrates this process through examination of the electronic band structure.

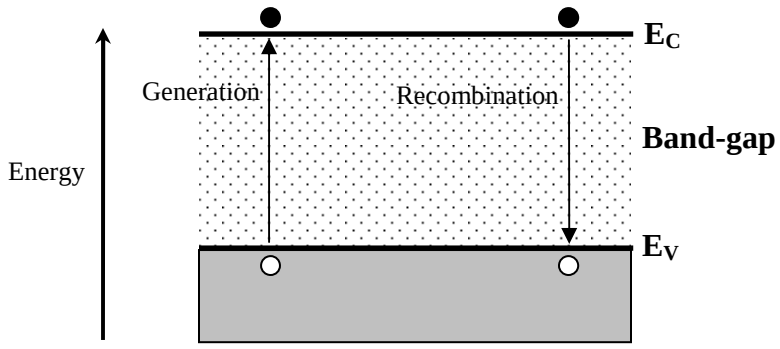


Figure 2-7: Direct generation-recombination in a semiconductor.

What Figure 2-7 describes is known as *direct recombination* where free electrons are generated and pass into the conduction band (E_C) or recombine by filling an available hole in the valence band (E_V). In order to do this, the electrons must acquire or lose enough energy to jump the band-gap to the respective bands. Typical mechanisms

responsible for this are kinetic energy transfer through particle collisions or the absorption of energy given off by an annihilation local to another electron [14].

Specifically for silicon semiconductors, this direct recombination is not probable due to differences in electron-hole momentums. Instead, *indirect* recombination occurs as shown in Figure 2-8 [14]. Here, defects from the fabrication process create *traps* in the band-gap at specific energy levels (E_t). These traps interact with free carriers through their capture, hold, and release over certain time intervals.

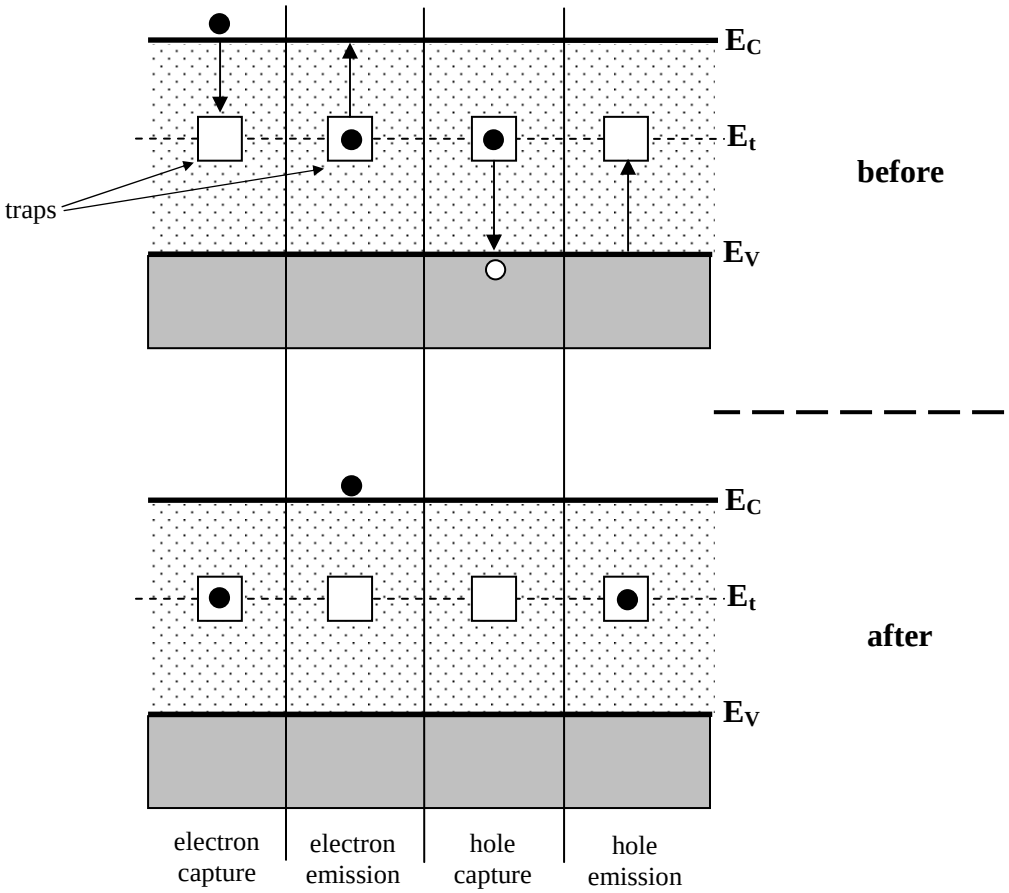


Figure 2-8: Indirect generation-recombination of carriers with traps associated with silicon semiconductors.

The specific time incorporated with the capture-hold-release nature of the traps causes carrier number fluctuations giving rise to a $1/f^{\alpha}$ nature of the noise. According to [15] and [16], α has a range of approximately $0<\alpha<2$ with a tendency towards $1/f^2$ at higher frequencies. Also shown in [16] is a noise plateau at lower frequencies which may suggest G-R saturation conditions.

What governs the ease and amount at which carriers can interact with traps is their energy, trap density, and the positions of trap energy levels in the band-gap. If a strong transverse electric field is present across the source and drain of a transistor, the energy of the charges increases creating *hot electrons* or *hot holes*. The more energy a carrier attains, the more readily it can surpass potential barriers and tunnel to traps at higher energy states. Additionally, if a large gate bias voltage is present, a higher probability of trap interaction exists through increased number of carriers in the channel.

Due to the target of this thesis, the qualitative explanation above on what creates and affects the magnitude of G-R noise is considered sufficient. For more depth on the subject, the reader should see documents referenced in this section.

2.3.3 Transistor 1/f Noise

The final noise source experienced is the 1/f noise behavior of transistors. Like G-R noise, 1/f noise is attributed to traps caused by defects during fabrication. What distinguishes 1/f noise from G-R noise is its magnitude and where the defects occur. At the S_i-S_iO_2 interface, a large number of localized energy states exist due to the abrupt discontinuity of the lattice structure giving rise to their common name of *interface* traps [1] - [3], [5]. This simply states the amount of energy needed for particles to tunnel and

interact with traps is less, resulting in the more dominant 1/f noise. Once again, the amount of 1/f noise is related to how strong a particular device is driven into saturation through the strength of the transverse E-field.

A well accepted expression developed in [5] captures the afore mentioned noise dependencies with

$$S_f(f) = \frac{q^2 kTN_t}{2C_{OX}^2 WL\alpha f} \tag{5}$$

where

N_t	trap density ($eV^{-1}cm^{-3}$);
C_{OX}	gate oxide capacitance (F);
W,L	width and length of gate (μm);
α	tunneling constant.

2.4 Parameters for Varying Noise Levels

The purpose of the previous section was to introduce what causes transistor channel noise and what changes might affect its magnitude. As discussed, the level of all noise sources relies on the amount of charges present in the channel (i.e. gate bias voltage through g_m). Also, all types of noise are at least somewhat dependant on V_{DS} voltage. With regards to testing, providing the ability to vary both transistor bias voltages to see behavioral changes in noise would prove desirable. Allowable V_{GS} and V_{DS} voltage ranges of up to nominally 3 V for both device types provide suitable test sweeps for both parameters. However to lesson the number of measurements, V_{GS} overdrive is limited to a typical design value of approximately 400 mV. This helps ensure the compatibility of g_m with g_{do} (Section 2.3.1)

The amount of noise produced by transistors is also proportional to channel area under the gate. This implies the need for multiple test devices with different channel lengths and/or widths. Since typical RFIC designs use channel lengths of 2.0 μm or less, varying the lengths from minimal, 1.0 μm, and 4.0 μm would provide a good test sample set. Also, keeping the aspect ratio constant eliminates noise changes through g_m, allowing the testing of channel length versus noise only. It is with these ideas for altering noise levels that the design of the measurement setup and specific transistors can now be discussed.

CHAPTER 3 – Measurement Setup

3.1 Considerations of the Measurement Setup

The topics covered in chapter two indicated what parameters to vary for viewing possible transistor noise level changes. The task now at hand is how to apply these variables and how to amplify the transistor's noise for measurement. As a first step, the channel noise must dominate all other sources before it can be amplified. Analysis of how to ensure this begins by applying basic noise principles as in the figure shown below.

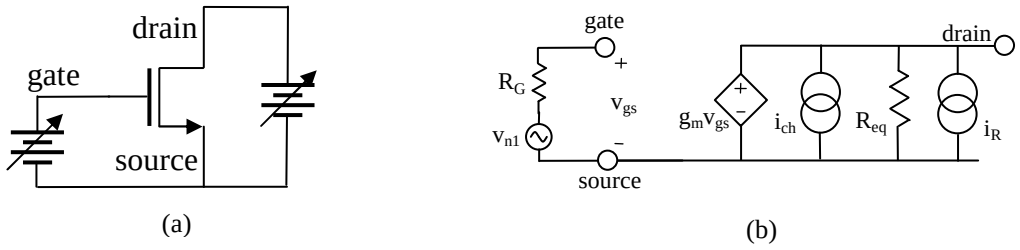


Figure 3-1: Biased test device (a) and its small-signal model (b).

Shown in Figure 3-1 is an example of a voltage biased device (a) and the corresponding noise sources located in its small-signal model (b). The variable voltage sources in (a) represent batteries connected to potentiometers with known resistances. It should be noted that in (b) the potentiometer noise source across V_{DS} has been omitted for reasons discussed later. The components i_{ch} and i_R correspond to the noise sources of the transistor and output resistance R_{eq}, respectively. When these sources are driven through

the R_{eq}, they develop a noise voltage at the drain terminal. Applying the proper equations for broadband noise discussed in the previous chapter reveals a total output voltage noise of

$$v_o^2 = \left(-g_m R_{eq}\sqrt{4kTR_G}\right)^2 + \left(g_m R_{eq}\sqrt{4kTg_m^{-1}\gamma'}\right)^2 + \left(R_{eq}\sqrt{4kTR_{eq}^{-1}}\right)^2 \qquad \left[V^2Hz^{-1}\right]. \qquad (6)$$

The terms in (6), starting from the left, are as follows: the amplified thermal noise of R_G, device current noise times R_{eq}, and the thermal noise of R_{eq}. The resistance R_{eq} represents the parallel equivalent of the load resistance and the output resistance of the transistor, r_o. The resistance R_G comes from the gate biasing potentiometer. The term of interest in (6) is the second. In order to make it dominate, two constraints arise.

1) $g_m^{-1} >> R_G$
2) $g_m >> R_{eq}^{-1}$

Unfortunately, these constraints contradict the direction of g_m. A solution for this is to follow constraint two by making g_m greater than the expected $1/R_{eq}$ and to modify the circuit to attenuate the gate-resistance noise. The conductance of $1/R_{eq}$ is approximately 0.02 S due to the expected 50 Ω input impedance of following amplifiers, so that g_m must exceed 20 mA/V. Constraint one can be alleviated by adding a large shunt capacitor to ground at the gate to short the noise contribution from R_G.

3.2 Amplifying the Transistor Noise

The analysis of the previous section enabled the transistor noise to dominate over all other noise sources exterior to the device. The bias circuit developed and shown in Figure 3-1(a) can now expand to the full transistor noise measurement circuit in Figure 3-2.

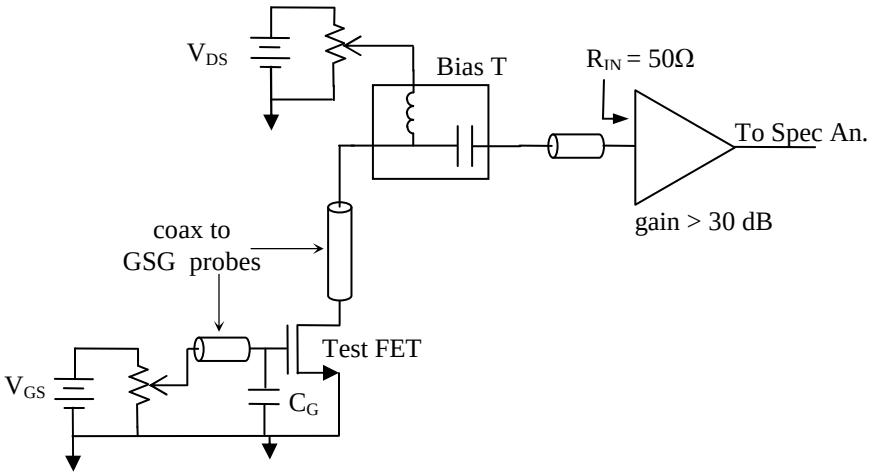


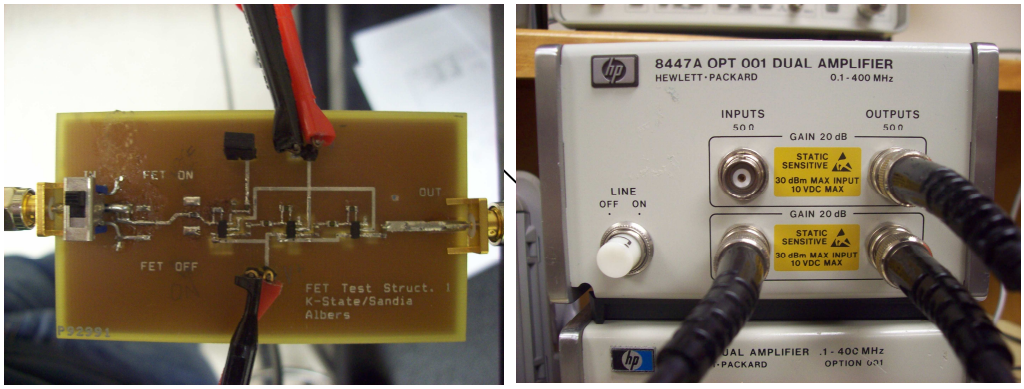
Figure 3-2: Transistor noise measurement setup.

Shown above are potentiometers used to provide desired device bias voltages. The voltage sources used are standard 9 V batteries since superfluous noise at these nodes is critical, and available supplies had strong noise/tones below 10 kHz. In order to separate the AC noise signal from the DC bias, a Bias-T was inserted prior to amplification. The measured lower corner frequency of the Bias-T was approximately 300 Hz when used in the measurement circuit, due to a large series capacitance. The Bias-T's internal inductor allows the exclusion of the noise produced by the V_{DS} potentiometer at high frequencies, but is insufficient to block frequencies below about 100 kHz. Although the potentiometer noise is therefore present at low frequencies, its total contribution is comparatively negligible.

The overall goal of Figure 3-2 is to amplify the transistor noise without adding substantial noise from the test circuit itself. Since the device background channel noise is the lowest measured noise level, it is the main focus of amplification. Recalling Equation (2) and using a g_m value of approximately 0.02 S at room temperature, the expected background channel noise voltage is approximately -170 dBm/Hz at the output terminal

of the transistor when driving into a 50 Ω load. Because this level is close to the -174 dBm/Hz room-temperature limit for amplifiers, a value of 0.04S was used in practice, yielding an expected background noise of -167 dBm/Hz. This magnitude still requires at least 30 dB to 40 dB or more of amplification to surpass the noise floor of an average spectrum analyzer.

To ease this gain requirement on a single amplifier over a frequency range of 1 kHz – 100 MHz, two amplifiers were used. A custom built PCB comprised of three LMV751 operational amplifiers in Figure 3-3 (a) provides approximately 65 dB of gain from 1kHz to 100 kHz. The schematic of its design is shown in Figure 3-4 on the following page. An HP8447A dual amplifier, shown in Figure 3-3 (b) supplies a suitable gain of 40 dB for the higher frequency measurements. These amplifiers were chosen for their gain and overall low noise contributions. The low frequency amplifier produces approximately 0.01 pA/Hz of input referred current noise at 1kHz offset which is negligible compared to the estimated device background current noise of 14 pA/Hz. For the high frequency measurements, the HP8447A contributes has an approximate 2 dB noise figure which is sufficiently small given the expected minimum channel noise of -167 dBm/Hz.



(a) **(b)**

Figure 3-3: Amplifiers used for low (a) and high (b) frequency noise measurements.

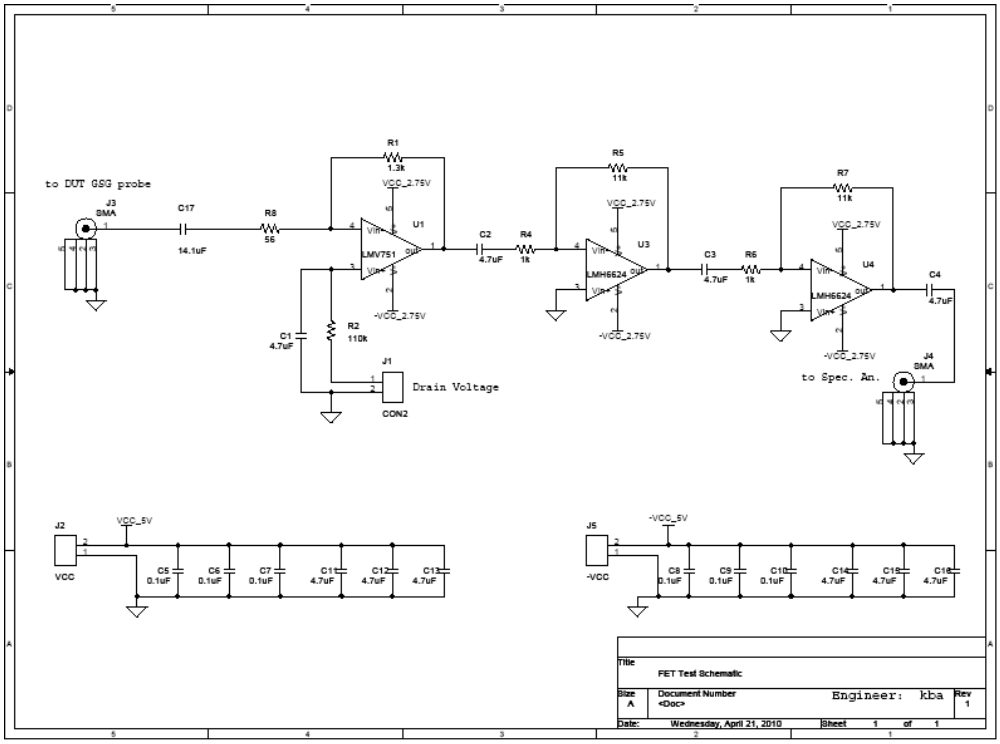


Figure 3-4: Schematic view of low frequency amplification board.

CHAPTER 4 – Transistor Design

4.1 Transistor Sizing

In order to achieve a transconductance value of approximately 0.04 mA/V while keeping overdrive voltages at or below ~400 mV, the fabricated transistors were designed with W/L ratios of approximately 2500 and 5000 for nFETs and pFETs, respectively. Because of on-chip space constraints, the 4.0 μm channel length P-type devices were limited to W/L of 2500, and were biased with twice the overdrive voltage as other devices. The images on the following page illustrate a portion of the fabricated transistor IC layouts. Shown in Figure 4-2 is a closer view of an 0.25μm HP transistor with its 150μm pitch ground-signal-ground (GSG) probes. The actual device is the red and blue patterned area. This pattern arises from the use of multiple fingers used to create the large width dimensions required without adding unwanted gate, source and drain resistance. The remaining colors correspond to different metal layers of the IC process.

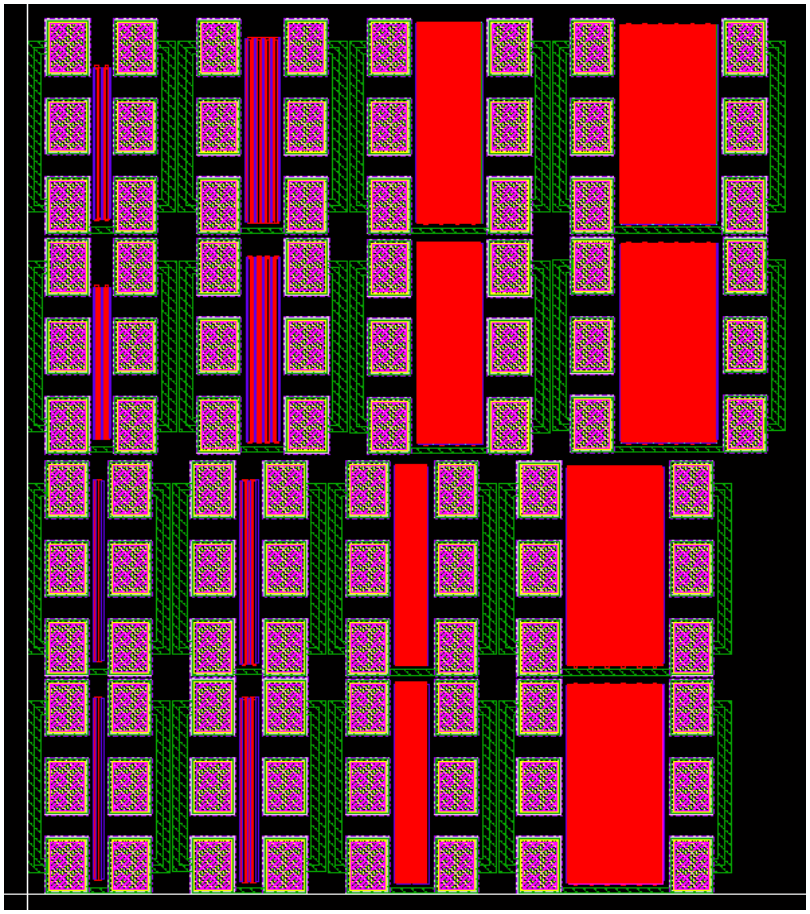


Figure 4-1: IC layout of P-type (rows: 1,2) and N-type (rows: 3,4) fabricated transistors.

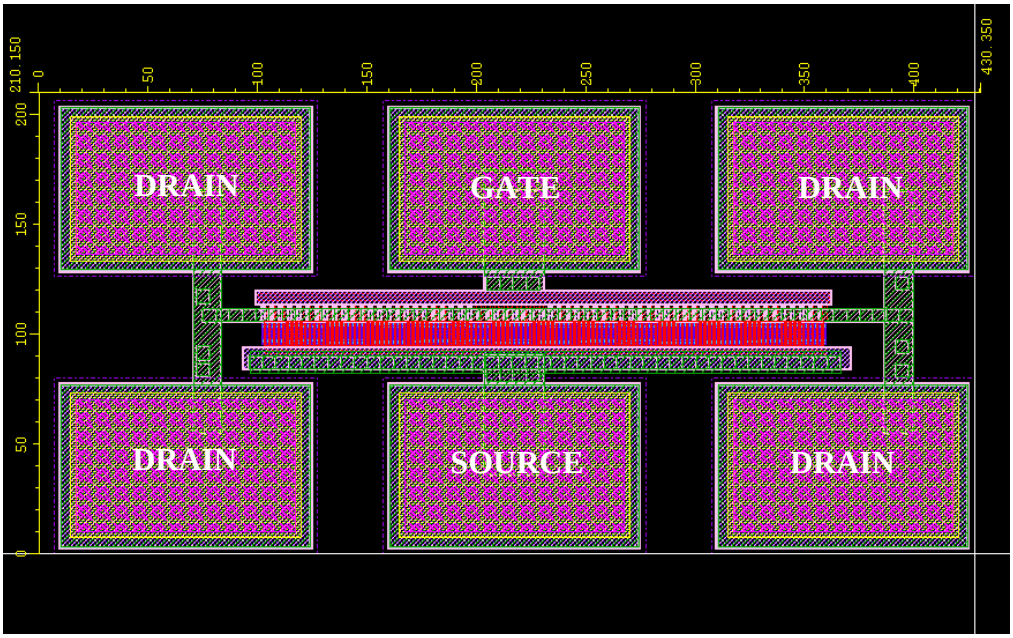


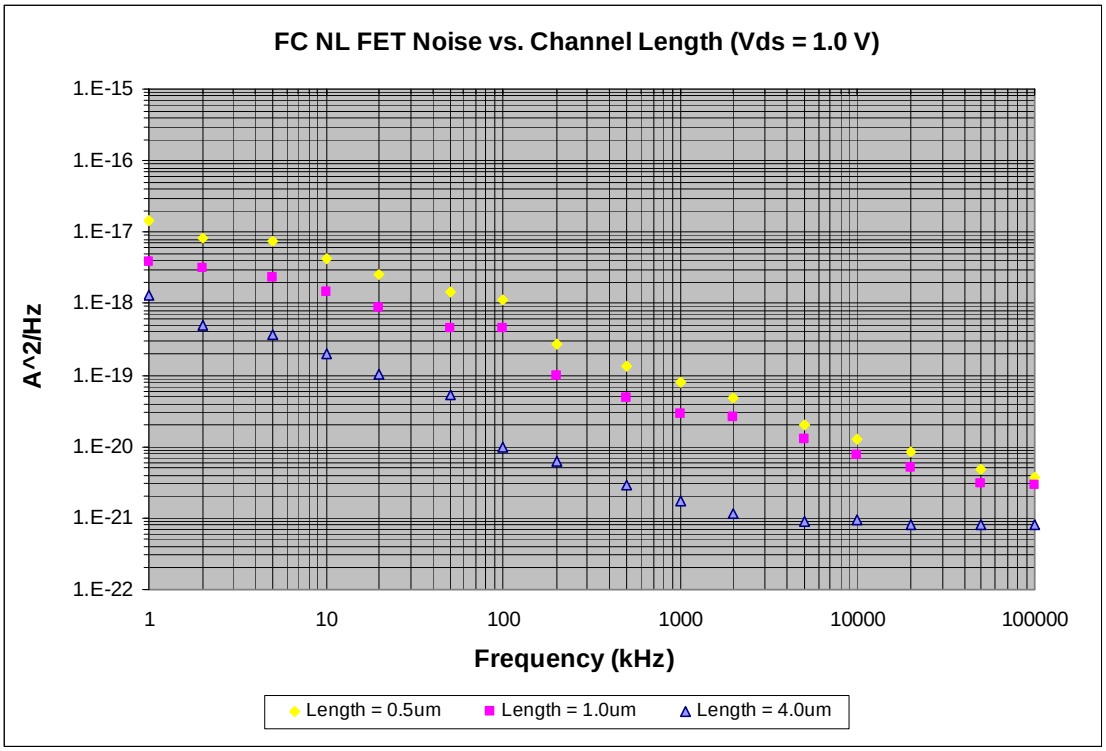
Figure 4-2: IC layout of 0.25µm HP transistor with probe pads.

CHAPTER 5 – Measurement Results

5.1 Presentation of Measured Data

The experimental data collected for variations in transistor channel noise ranged in frequency, V_{DS} voltage, and channel length. In order to efficiently present the results, two different styles of graphs were created. The first demonstrates the noise trends versus increasing frequency and channel length at a typical V_{DS} value of 1.0 V. The second graph shows noise variations versus frequency for a V_{DS} range of 0.5 – 3.0 V at 0.5 V increments. Through the presentation of these graphs and their general trends, estimated noise levels for the remaining transistors not shown can be extrapolated.

5.2 Measured Data Results for FC Process



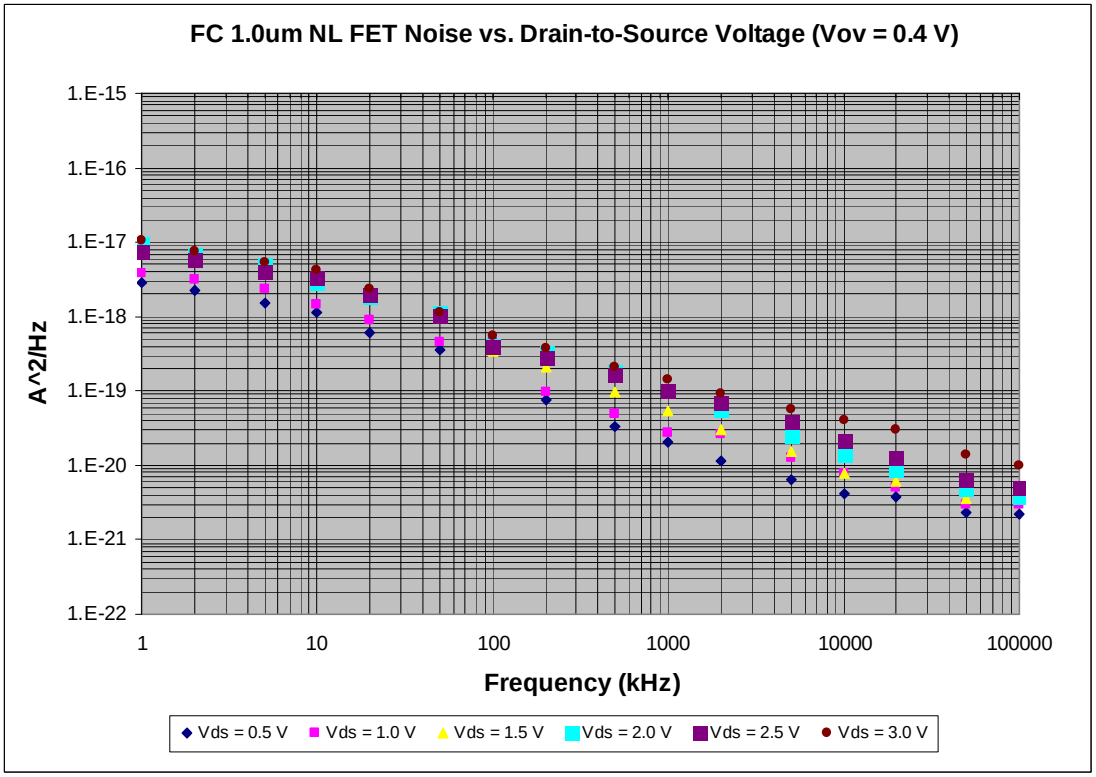
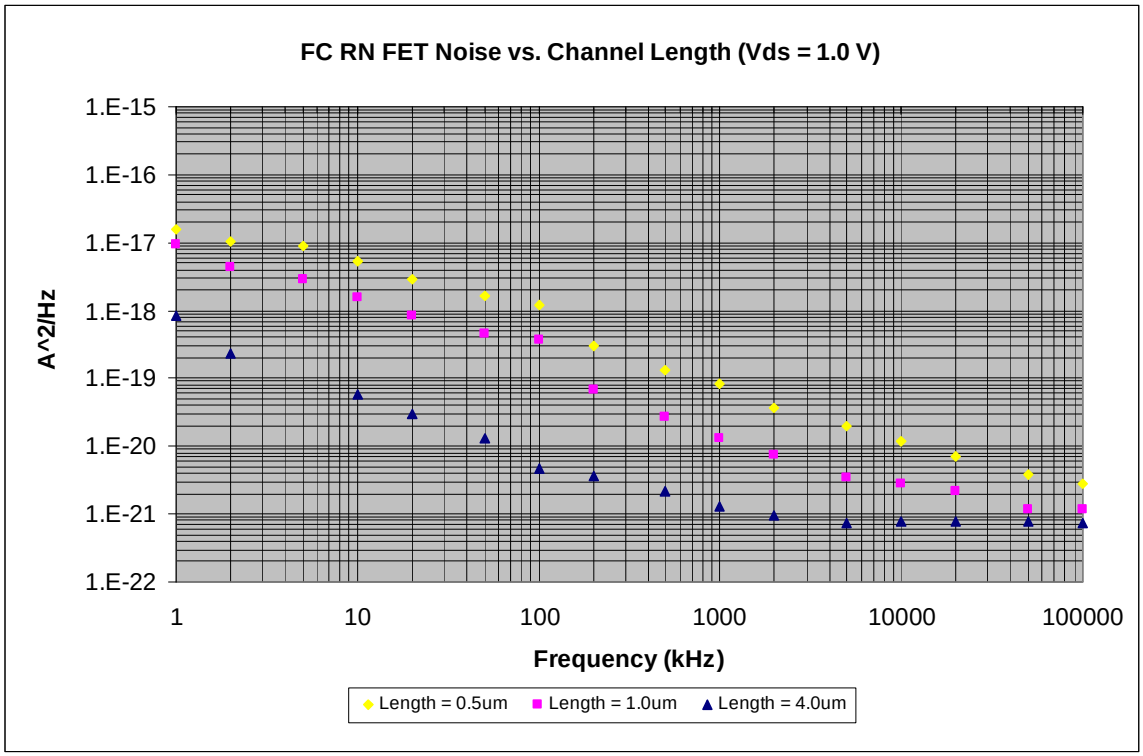


Figure 5-1: Measured noise of FC NL transistor.



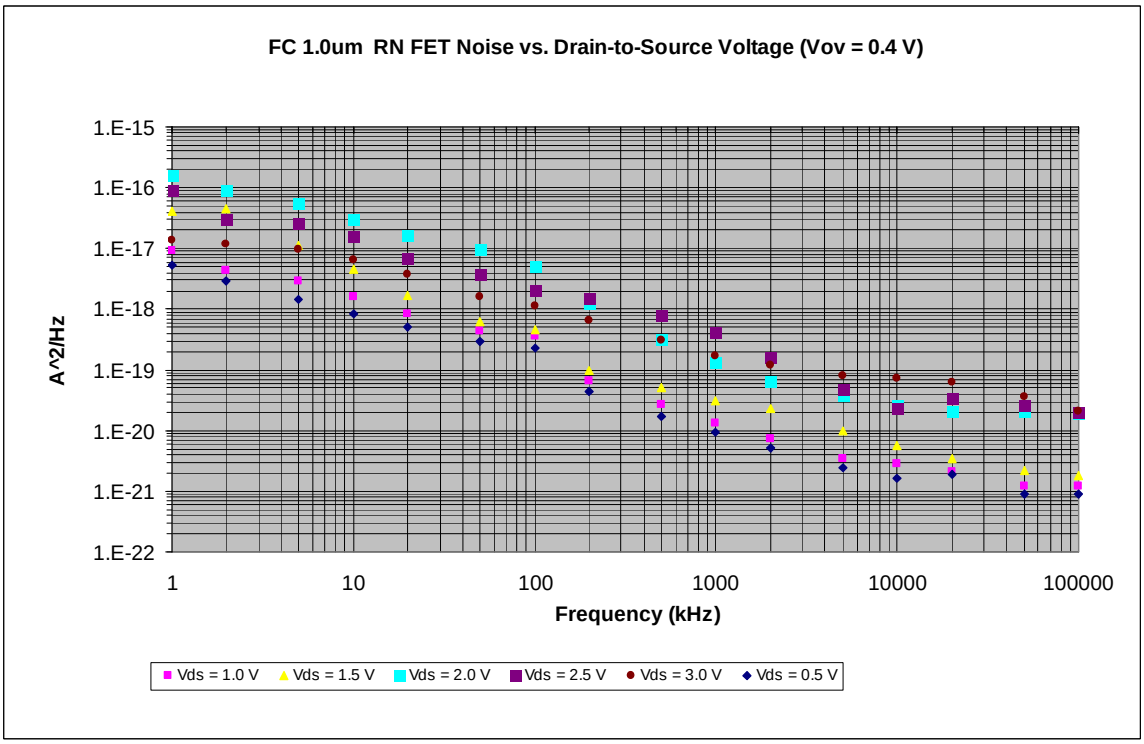
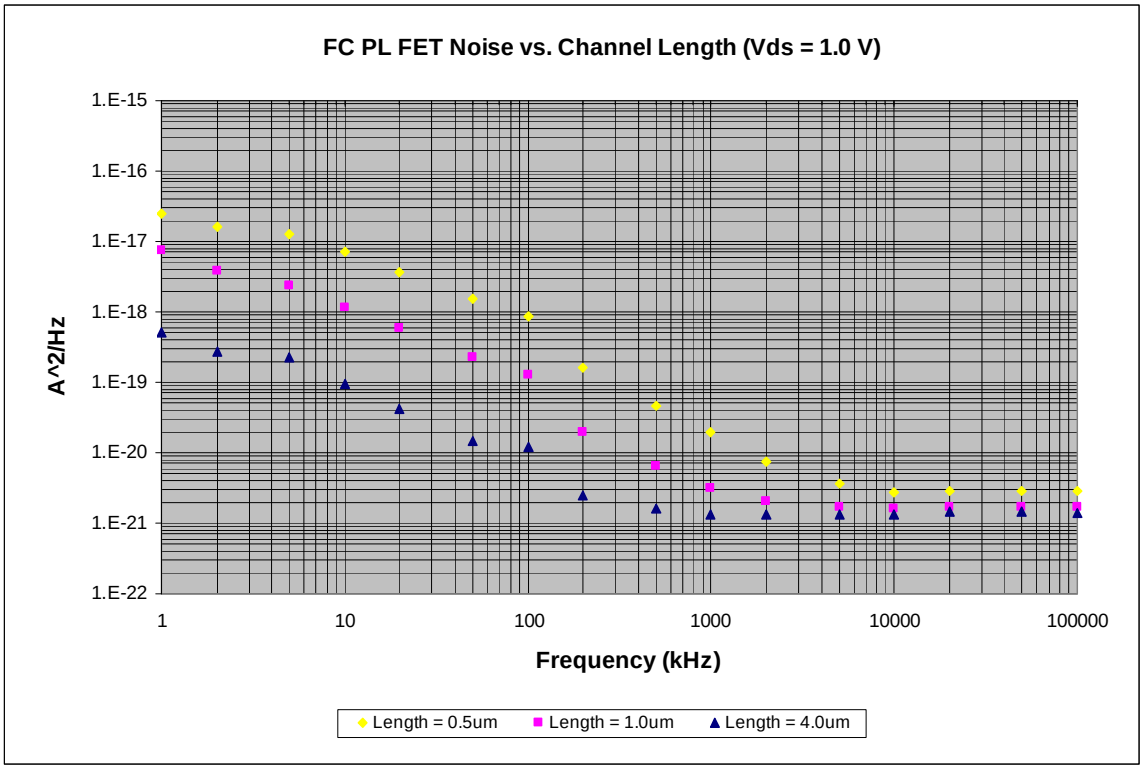


Figure 5-2: Measured noise of FC RN transistor.



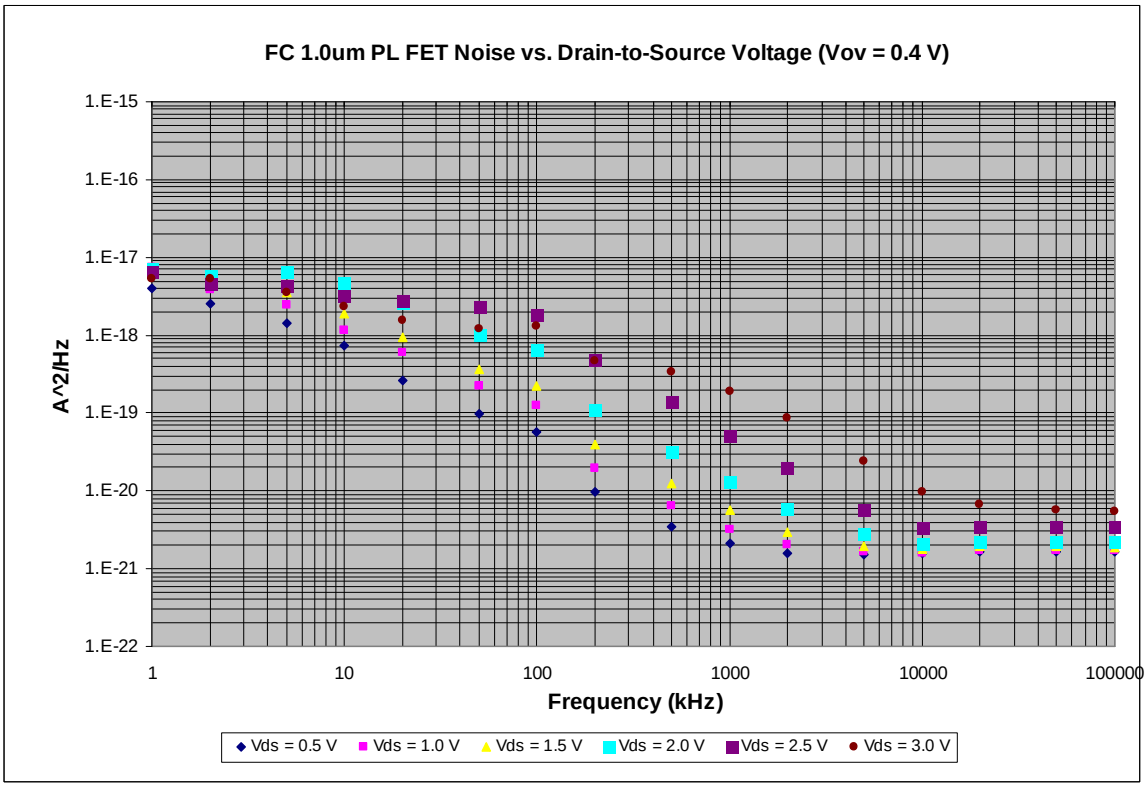


Figure 5-3: Measured noise of FC PL transistor.

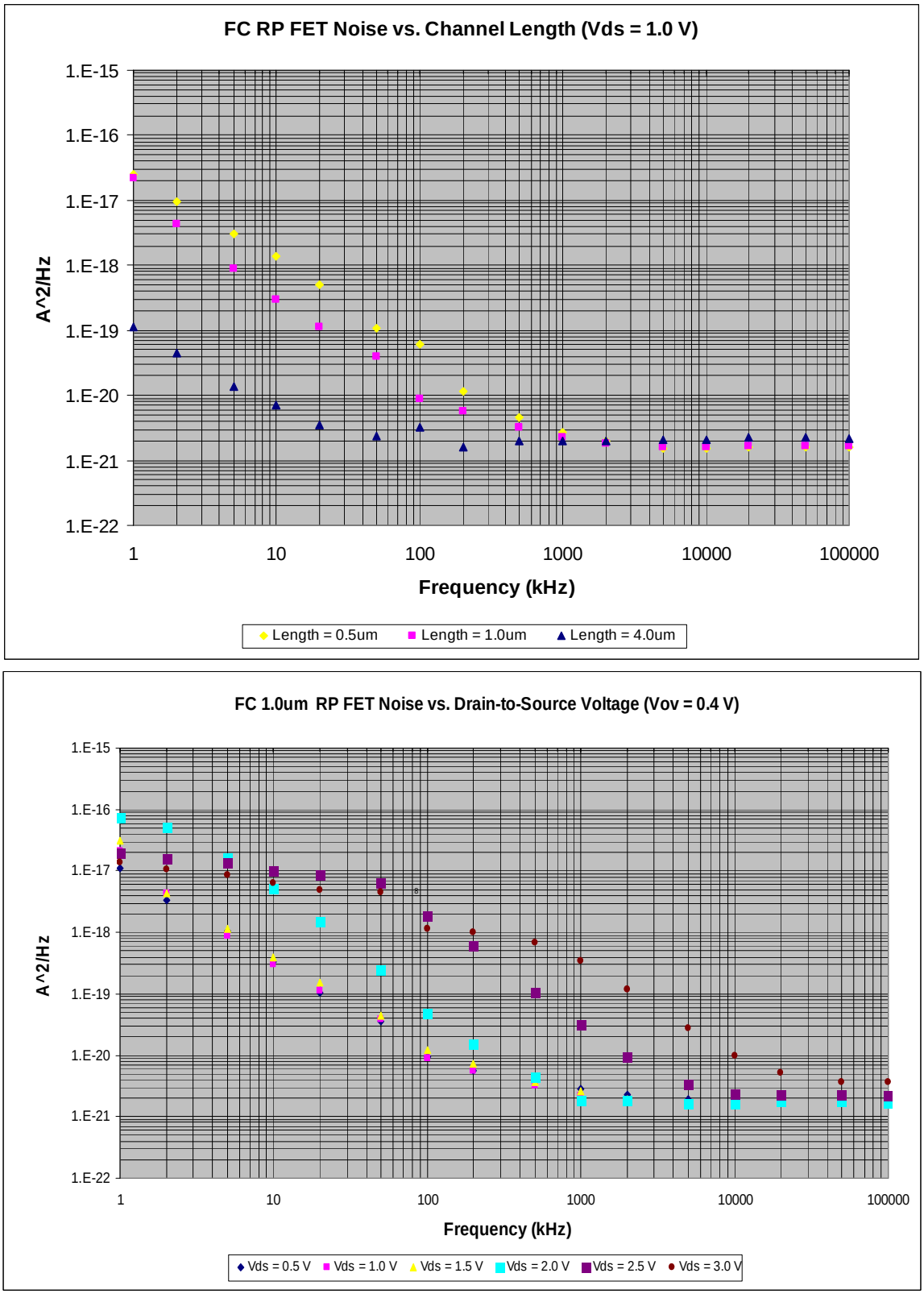


Figure 5-4: Measured noise of FC RP transistor.

5.3 Measured Data Results for GC Process

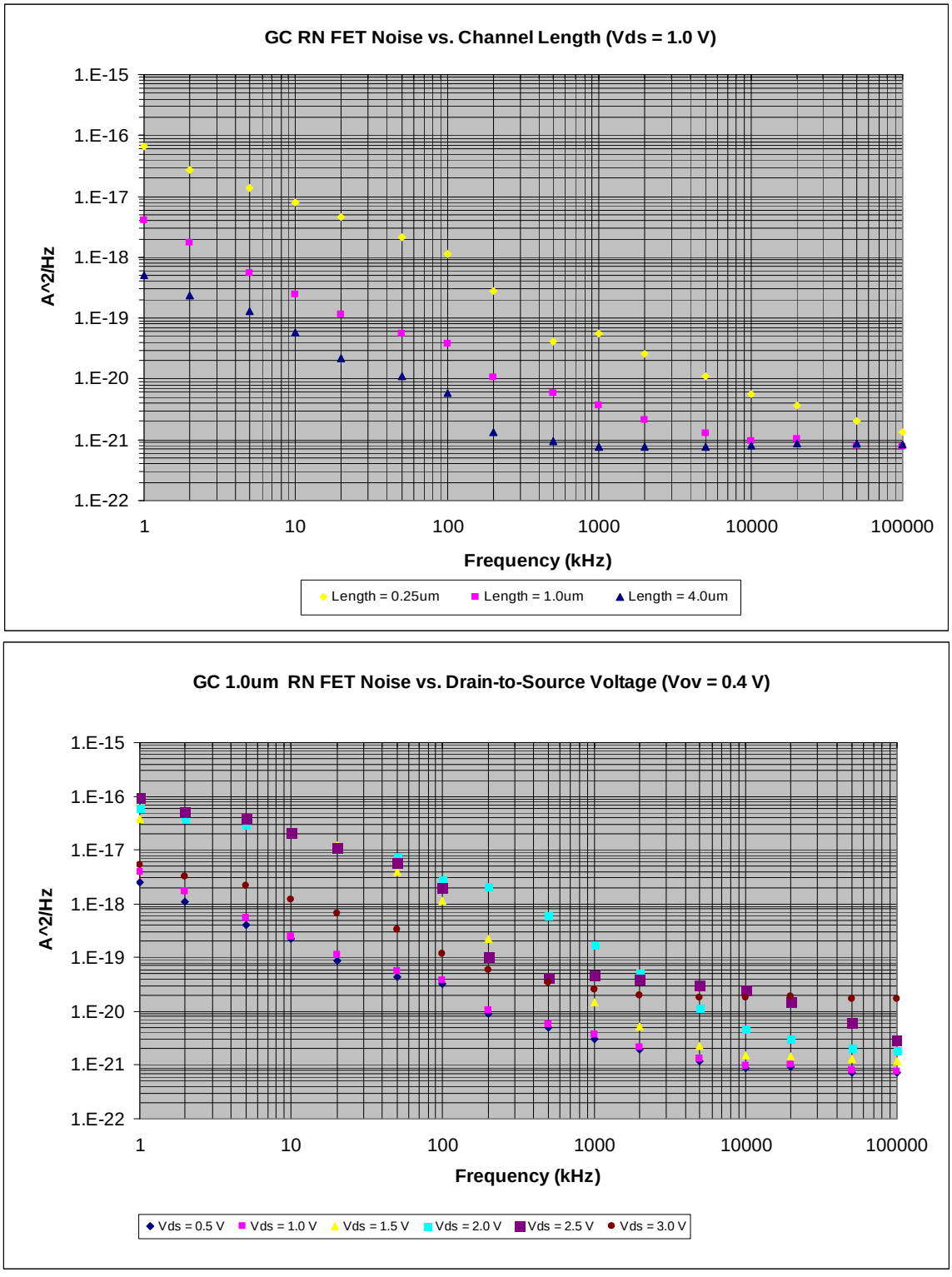


Figure 5-5: Measured noise of GC RN transistor.

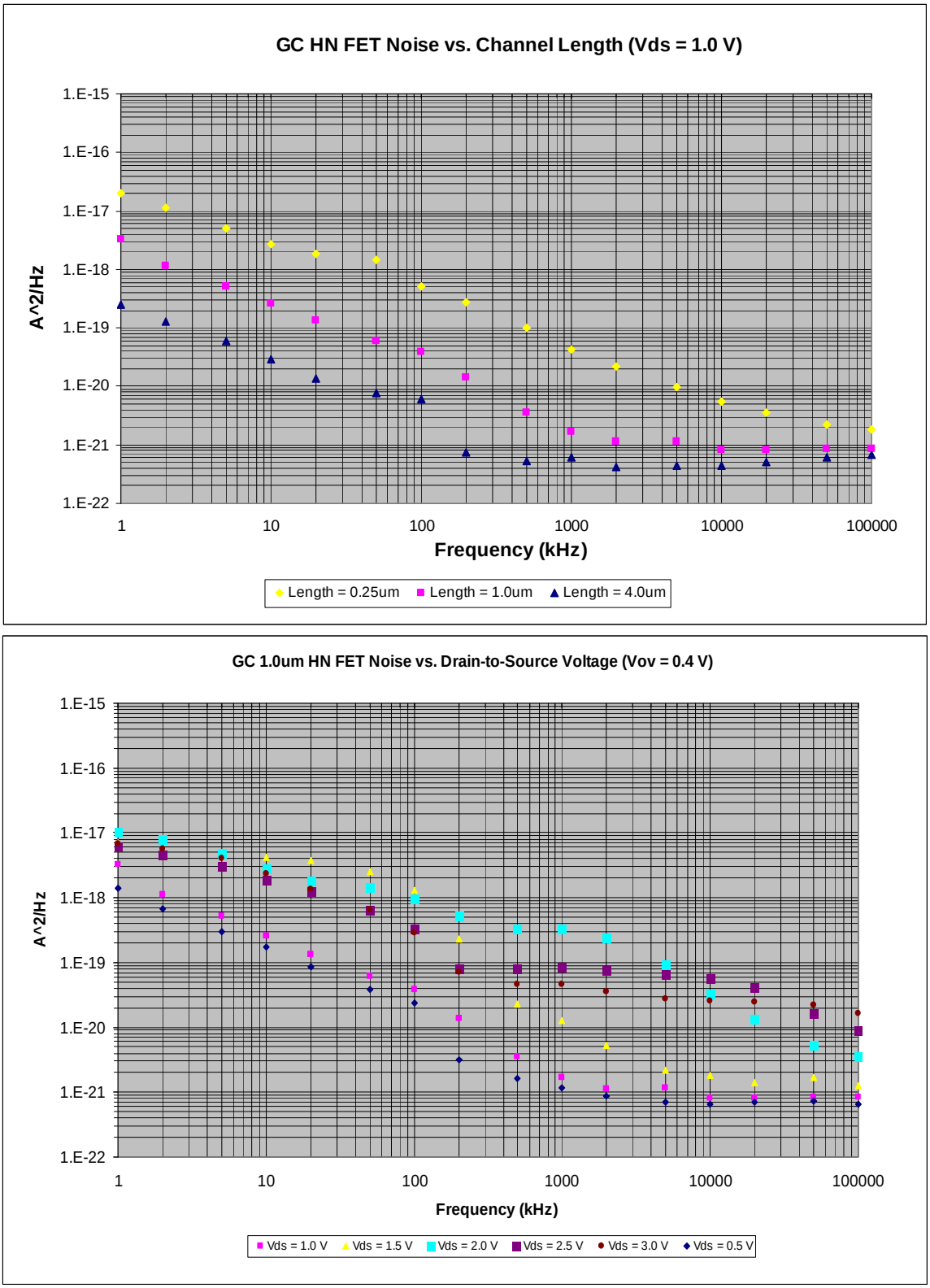


Figure 5-6: Measured noise of GC HN transistor.

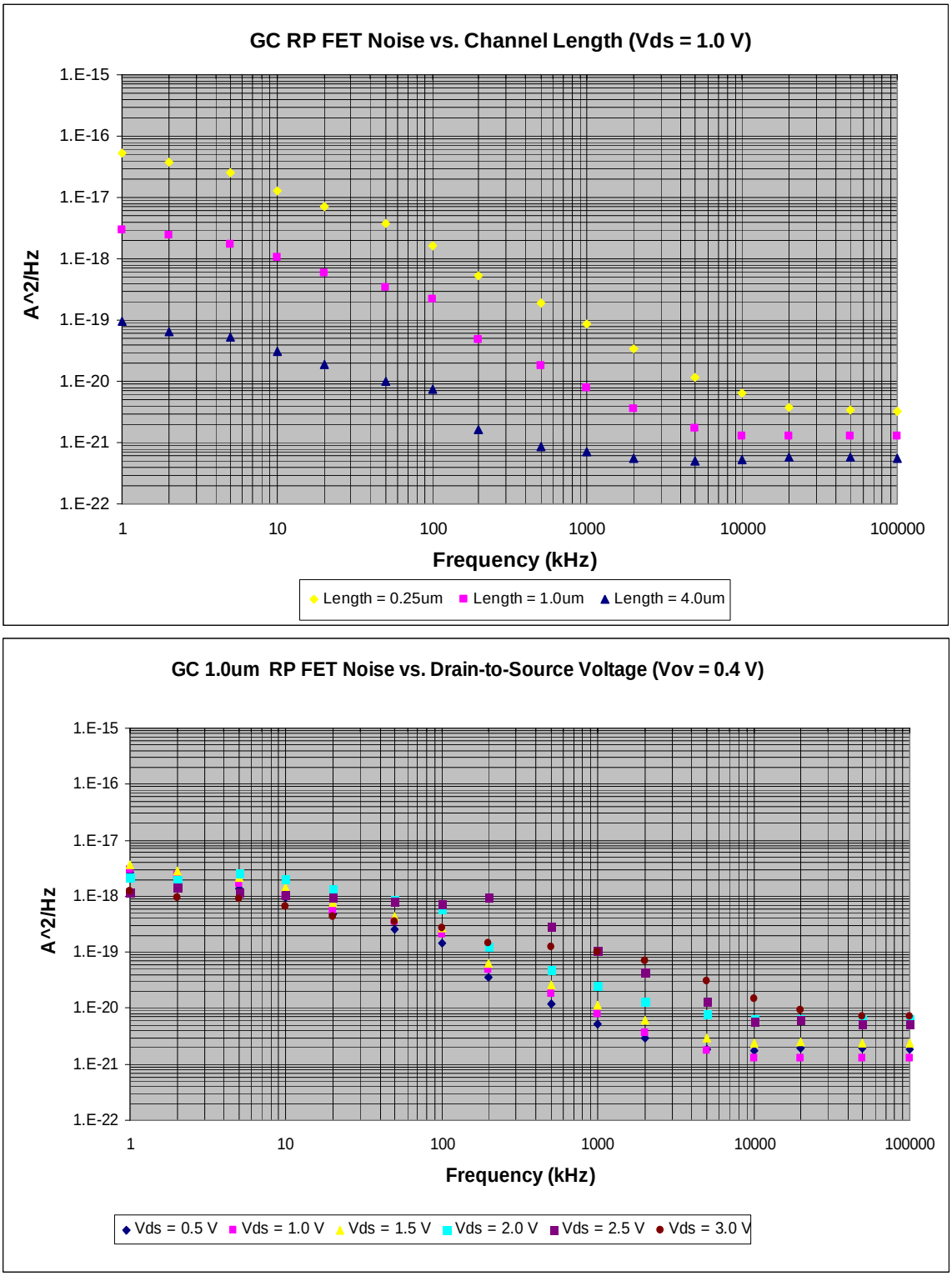


Figure 5-7: Measured noise of GC RP transistor.

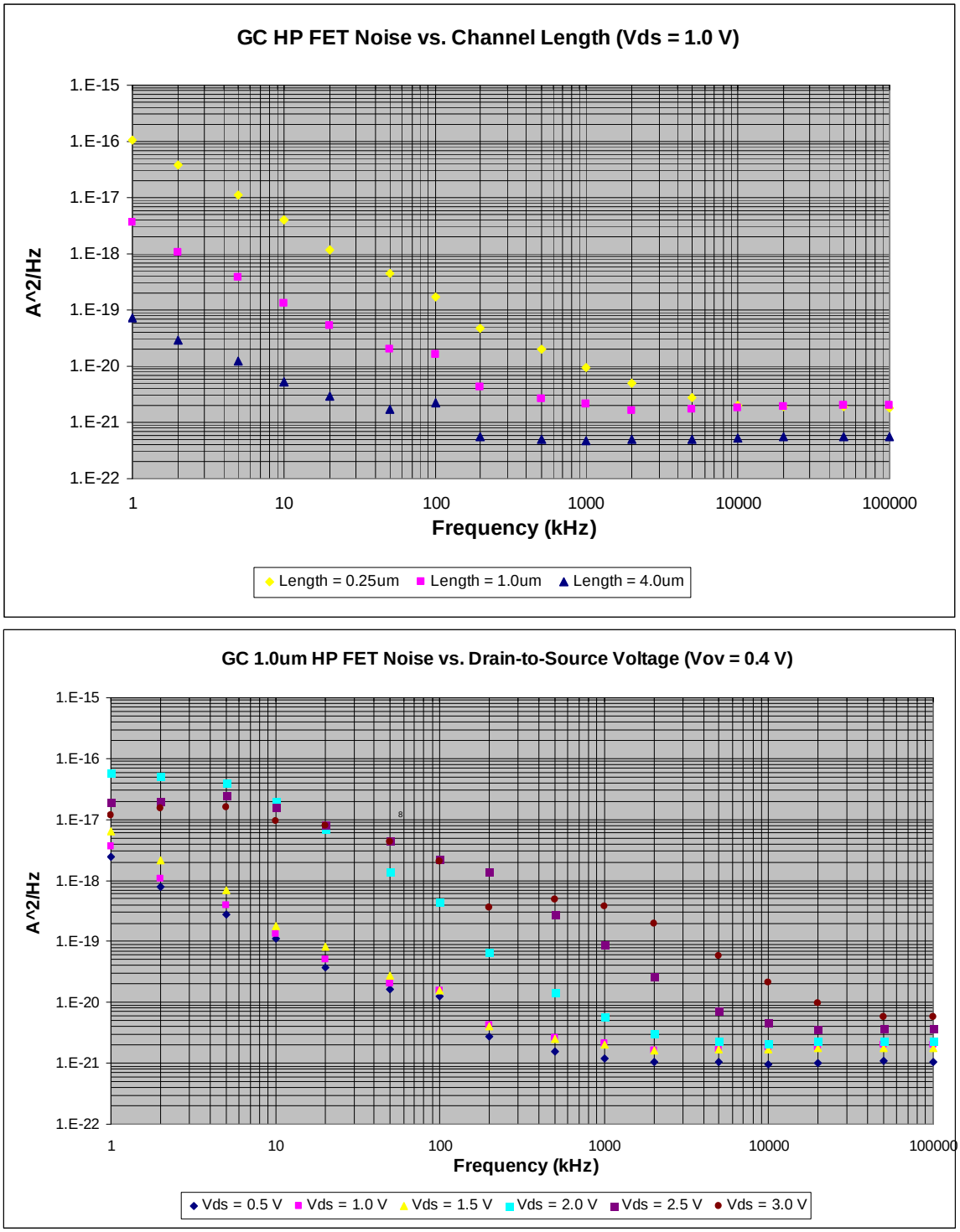


Figure 5-8: Measured noise of GC HP transistor.

5.4 Summary of Noise Measurements and Observed Trends

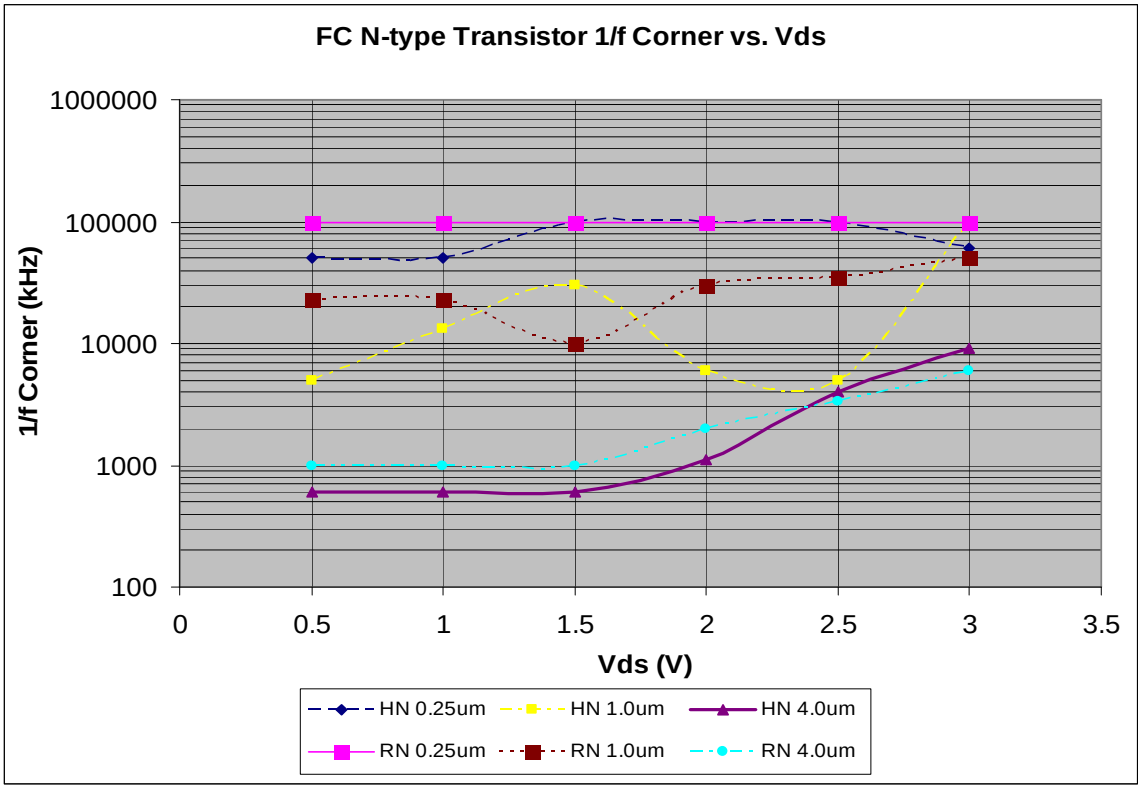
The plotted results above indicate the amount of noise produced is highly dependent upon on V_{DS} bias voltage, *especially* for smaller channel lengths. For nearly all devices, at least a 10 dB increase was observed in the 1/f spectrum for V_{DS} voltages beyond approximately 1.0 V and in some cases, the increase exceeds 20 dB. Transistors with larger channel lengths exhibited more resilience to increased V_{DS} voltage. This correlates with a suspected transverse electric field strength decrease as the channel length increases. An increase in channel length by 4X resulted in an average of approximately 10 dB less noise for frequencies below the noise corner. With this, the observed 1/f corners were reduced by approximately $1/10^{th}$ for each 4X increase.

On average, over all tested frequencies for devices of all channel lengths and types, higher threshold devices produced approximately 5 dB less noise than medium threshold devices. The probable cause of this affect is attributed to difference in the doping concentration of devices.

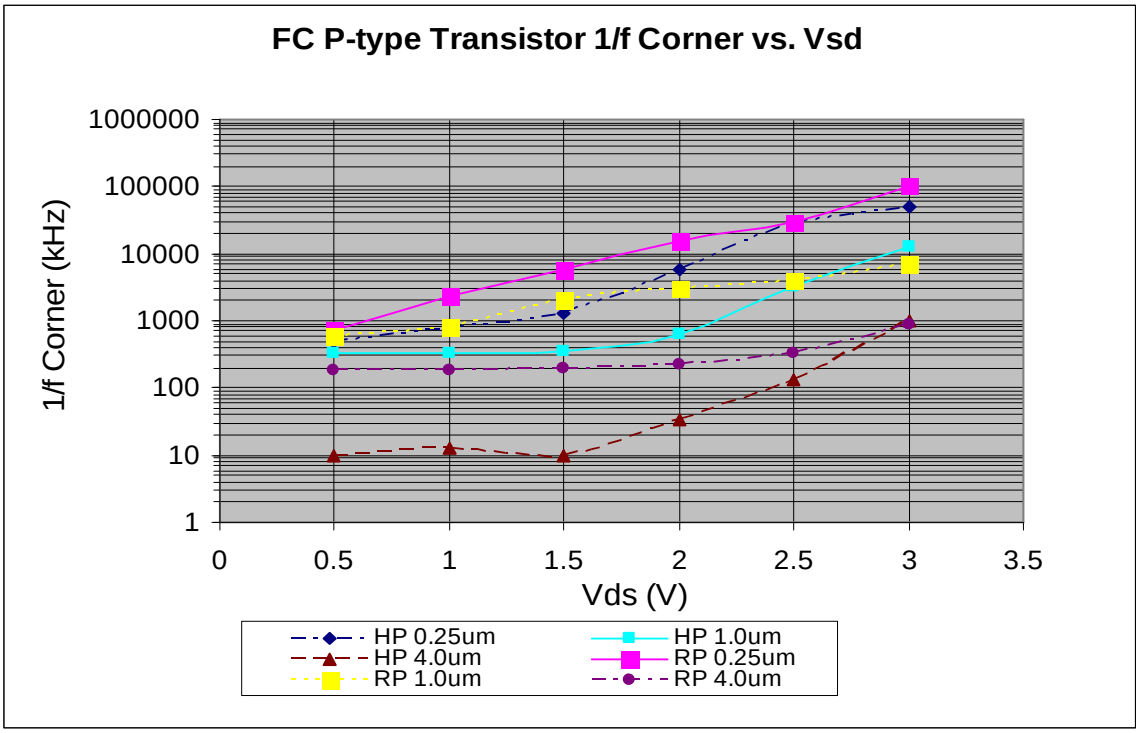
When comparing P-type versus N-type devices, the pFETs outperformed nFETs by an average of 10 dB at 1 V V_{DS}. At lower bias values, the two types of transistors perform similarly. However, the noise levels in the N-type transistors starts to increase significantly more than their P-type counterparts. This behavior can be attributed to the difference in attainable energy of charged particles (electron vs. hole) for a given electric field. As discussed in Chapter 2, the amount of energy a particle has determines the ease of interaction with oxide traps.

5.5 Device 1/f Noise Corners

One of the fundamental goals of this research is to characterize the available transistors with their noise corners. Regarding this, the corner of each transistor was estimated by finding the frequency where the noise increased by 3dB from the respective background channel noise floor at a given V_{DS} voltage. Figures 5-10 and 5-11 display the results of the corners found. It should be noted that devices with corners at or above 100 MHz were unattainable due interference of the FM broadcast band. Since the results are for qualitative purposes, no information is lost.

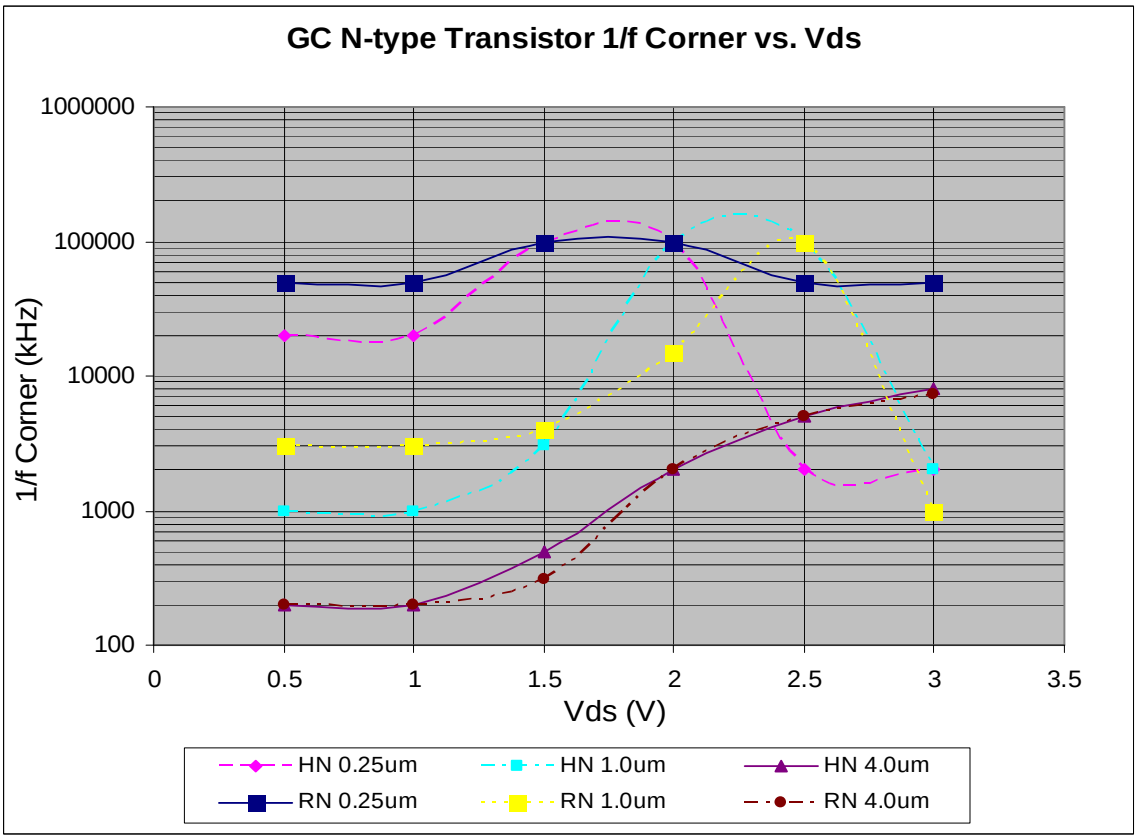


(a)

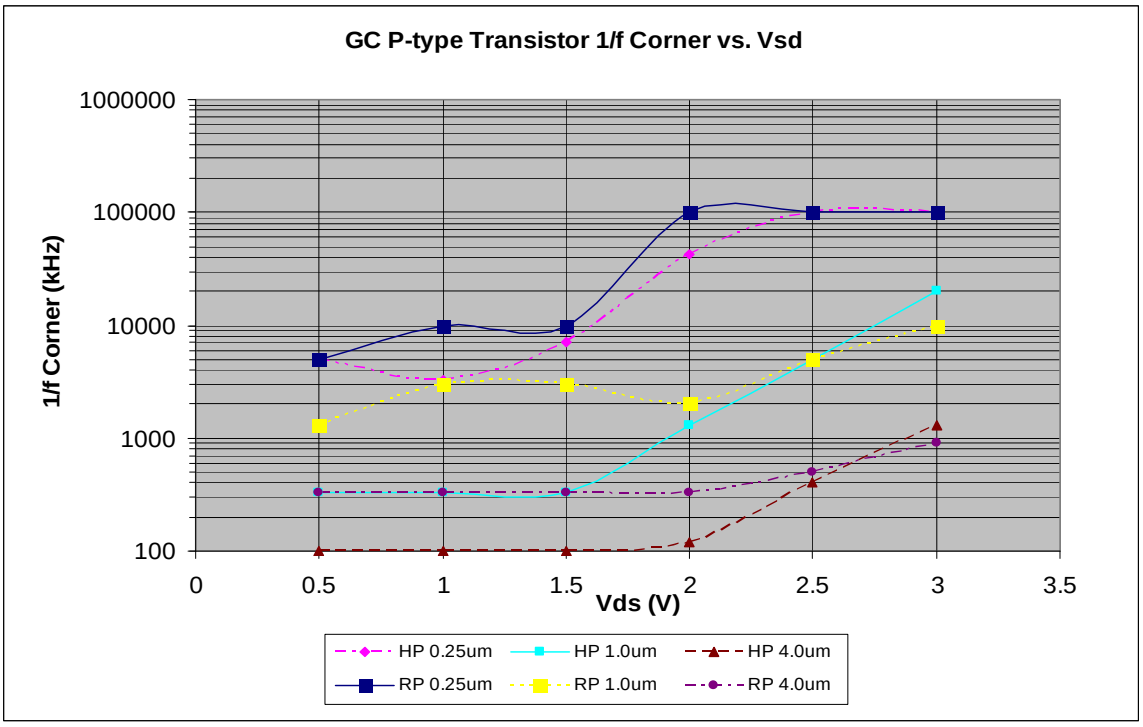


(b)

Figure 5-9: Estimated 1/f noise corners for N-type (a) and P-type (b) transistors in FC process.



(a)



(b)

Figure 5-10: Estimated 1/f noise corners for N-type (a) and P-type (b) transistors in GC process.

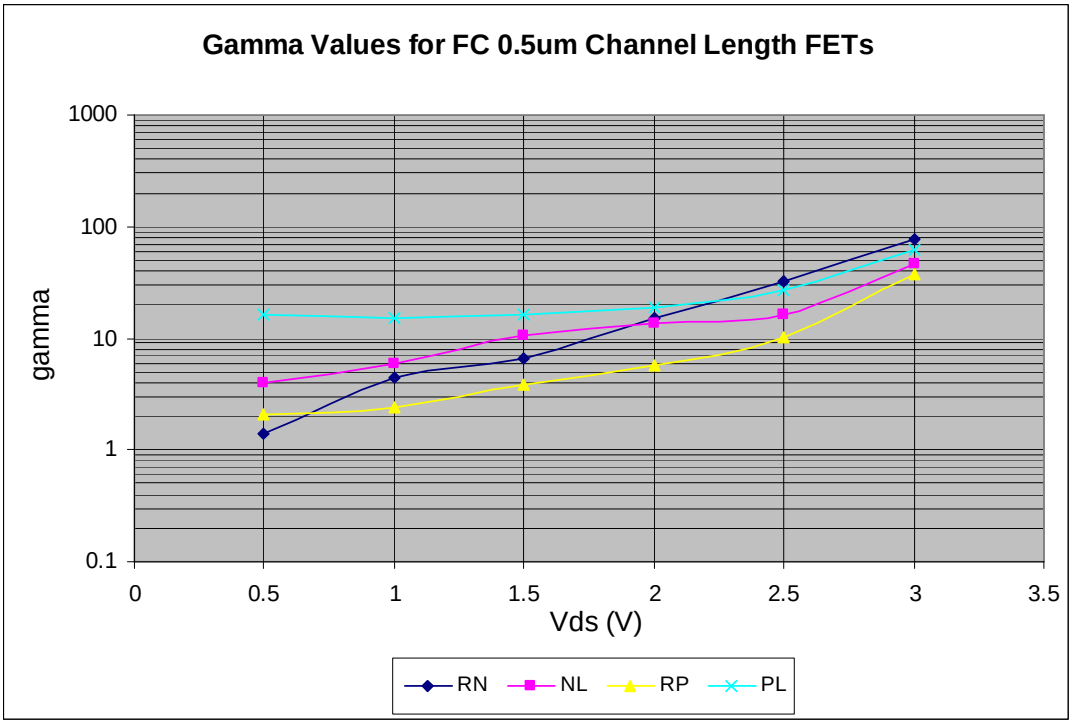
The trends observed in the noise corner plots signify low frequency noise is more susceptible to V_{DS} voltage increases than device background channel noise is. This is exemplified through increasing corner frequencies as V_{DS} voltage increases. For reasons discussed in Section 5.4, P-type transistors and longer channel length devices allow lower frequency corners.

The behavior of a decrease in corner frequency after a certain V_{DS} is reached is characteristic only to N-type devices. The exact cause of this is still under speculation, however likely suspects are effects, such as output resistance degradation and velocity saturation, experienced when devices approach their breakdown limits. It could also be possible that the interface states responsible for 1/f noise have become saturated at high V_{DS} values. Concurrently, the ever increasing energy of the carriers could now have

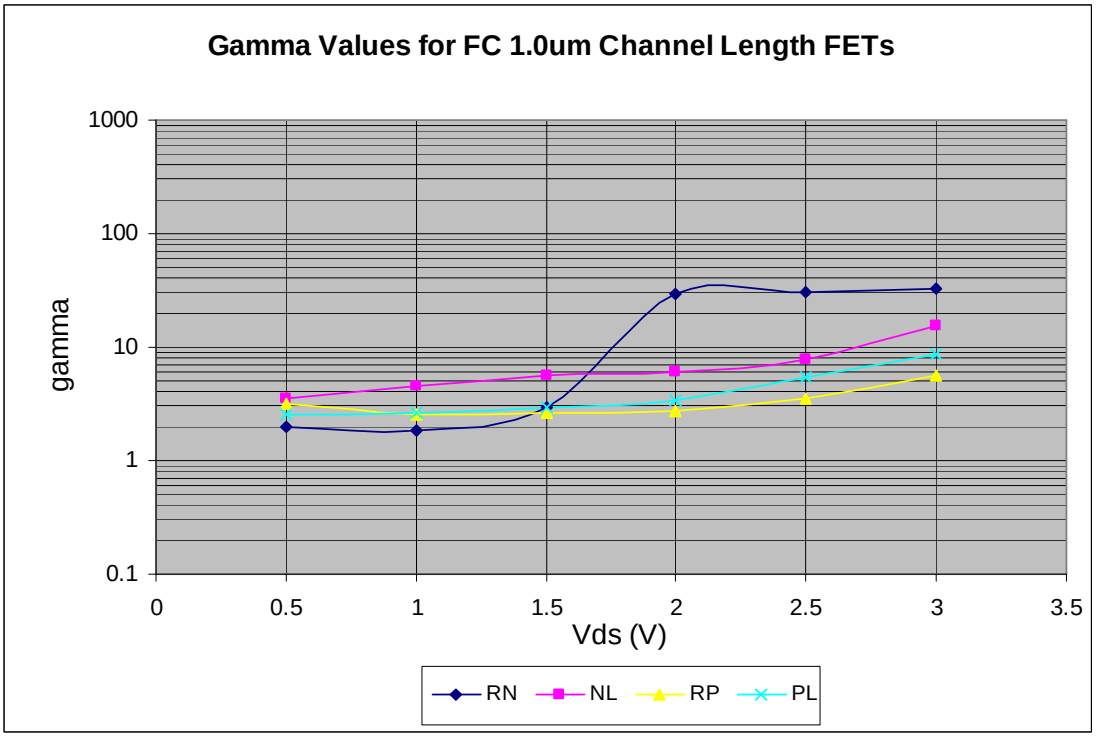
enough energy so that interactions with deeper traps more readily occur allowing G-R noise to surpass 1/f noise. Since the trends approximately match those seen in [17], this is likely the case.

5.6 Calculated Broadband Noise and γ′

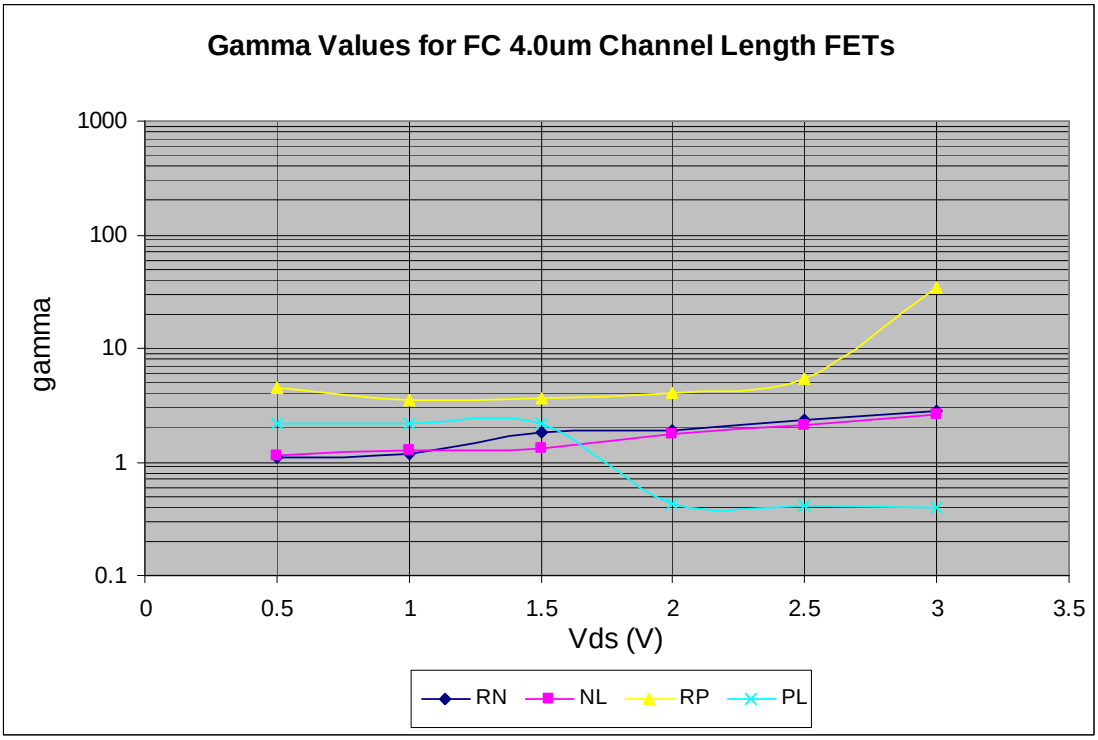
As a final measure in transistor noise performance, the value of γ′ was calculated. Recall this is a multiplicative factor on the long-channel device noise which compensates for additional channel noise experienced under the presence of a V_{DS} bias. The value of γ′ was calculated by taking the amount of noise measured at 100 MHz divided by the theoretical value of Equation 3. At a g_m of 0.04 mA/V with γ′ set to 1, Equation 3 is 6.40×10^{-22} A^2Hz^{-1}. Ideally, the measurements for γ′ should have been taken at > 100 MHz, however the FM broadcast band coupled with lack of a screen-room facility interfered with the background noise at these frequencies. The following graphs in Figures 5-11 and 5-12 represent the calculated values of γ′ versus V_{DS} voltage at 100 MHz for all the tested transistors and may therefore exceed the true value in some cases. In addition, it should be noted that g_m and g_{do} are likely not equal for the shorter channel devices due to the 400 mV overdrive used. Hence, smaller values of γ′ may be expected for lower overdrive designs.


Gamma Values for FC 0.5um Channel Length FETs
1000
100
10
1
0.1
gamma
0
0.5
1
1.5
2
2.5
3
3.5
Vds (V)
RN
NL
RP
PL

(a)

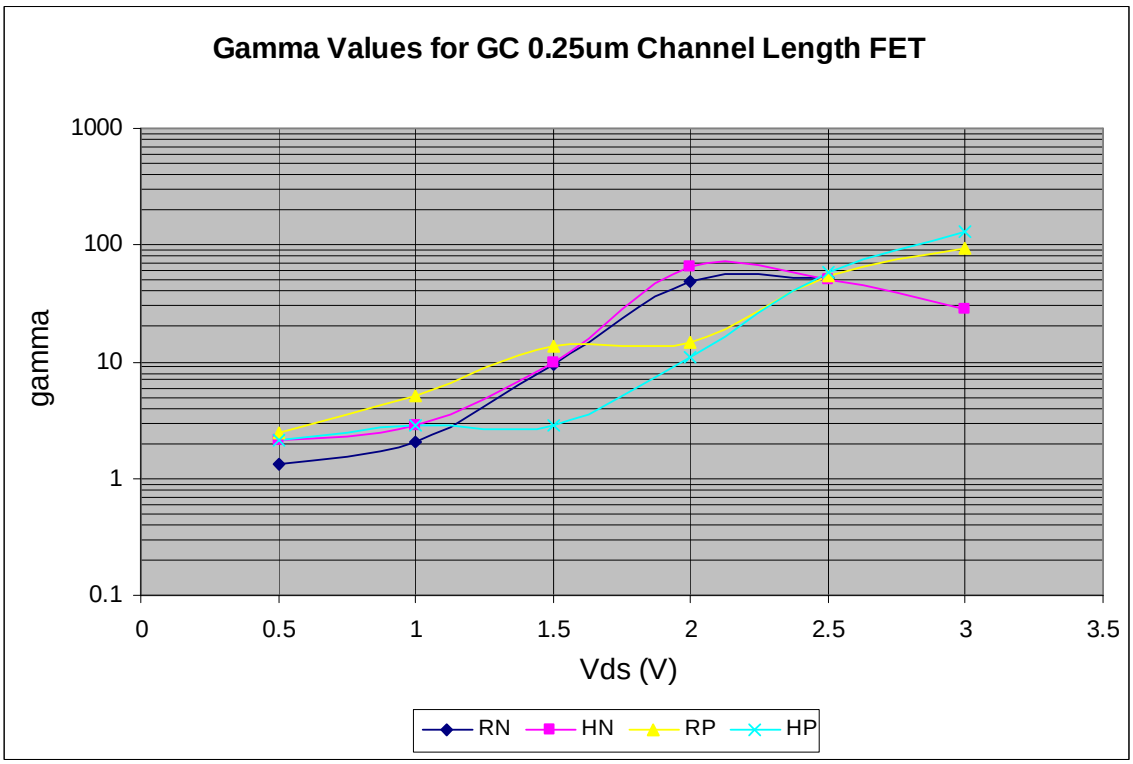

Gamma Values for FC 1.0um Channel Length FETs
1000
100
10
1
0.1
gamma
0
0.5
1
1.5
2
2.5
3
3.5
Vds (V)
RN
NL
RP
PL

(b)

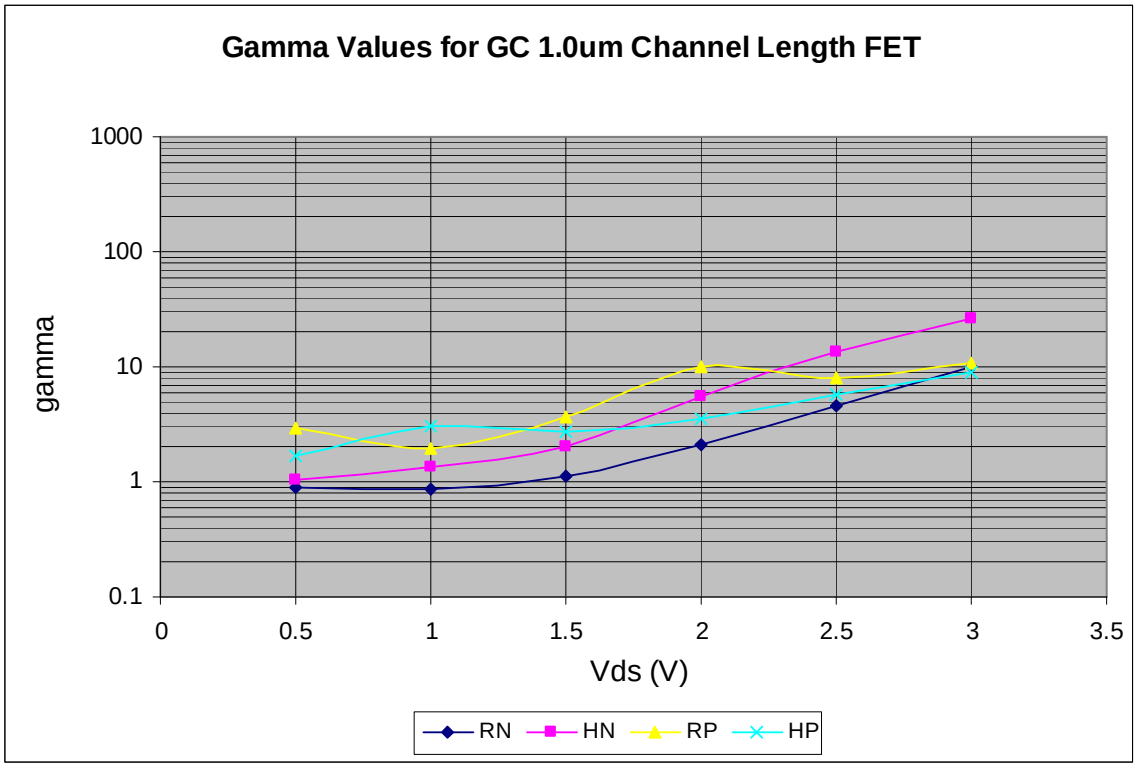


(c)

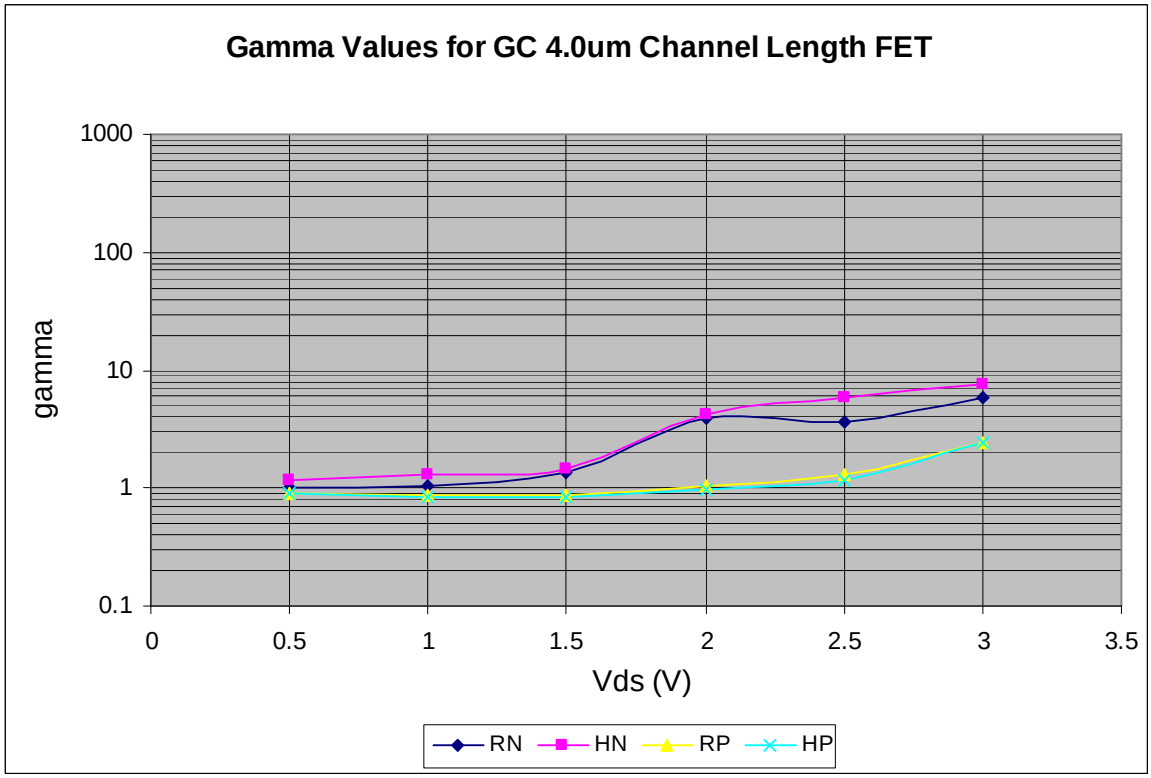
Figure 5-11: Calculated noise-factor versus V_{DS} voltage of 0.5µm (a), 1.0µm (b), and 4.0µm (c) transistors in FC process.



(a)



(b)



(c)

Figure 5-12: Calculated noise-factor versus V_{DS} voltage of 0.25µm (a), 1.0µm (b), and 4.0µm (c) transistors in GC process.

The graphs above approximately match the trends seen in [8] [9]. Specifically, the results found in Figure 5-11 (a) are found to differ only by a factor of 1.5. The differences in the γ' values are likely due to a maximum frequency measurement at 100 MHz here as opposed to 120 MHz in [8]. Additionally, higher gate biasing of the transistors in [8] produces lower gamma values.

As suspected, longer channel length devices produce smaller γ' and less noise increase for increases in V_{DS} voltage. This result confirms the amount of background channel noise is inversely proportional to the device area underneath the gate as shown in [3].

CHAPTER 6 – Conclusions

6.1 Conclusions

This thesis presents measured noise performance for transistors in 0.25 μm and 0.5 μm SOS processes. The tested devices for each process included medium and high thresholds with minimum, 1.0 μm, and 4.0 μm channel lengths. Gate bias voltages were selected to represent typical design overdrives of approximately 0.4 V while varying the drain-to-source voltage from 0.5 to 3.0 V. Test results show 1/f noise corner improvements of approximately one decade, or 10 dB less noise at low frequency, for each factor of four increase in channel length. The 1/f noise spectrum was found to

increase *dramatically* for V_{DS} voltage values past approximately 1 to 1.5 V for all tested transistors. With this, P-type and larger channel length devices proved to be less susceptible to increased V_{DS} voltages. Suspected causes are electron versus hole energy differences and decreased field strength through increased distance, respectively.

The noise factor increase, γ', was calculated for each transistor. As with the 1/f spectrum, the P-type transistors' broadband background noise showed greater resilience to increased V_{DS} voltages. Additional average noise improvements of approximately 5 dB were found over the tested frequency range for high threshold devices.

The characterization of the transistors conducted here indicates low noise circuit design preferences of P-type, high threshold devices operating well below maximum allowed V_{DS} for the process. Channel lengths should also be selected as large as circuit operating frequency will allow.

REFERENCES

[1] Daniel M. Fleetwood, Timothy L. Meisenheimer, John H. Scofield, "1/f Noise and Radiation Effects in MOS Devices," IEEE Trans. Elec. Dev., vol. 41, pp. 1953-1964, Nov. 1994.

[2] Hui Tian, Abbas El Gamal, "Analysis of 1/f Noise in Switched MOSFET Circuits," IEEE Transactions on Circuits and Systems-II, vol. 48, pp. 151-157, Feb. 2001.

[3] Chun Hu, G. P. Li, Eugene Worley, Joe White, "Consideration of Low-Frequency Noise in MOSFET's for Analog Performance," IEEE Electron Device Letters, vol. 17, pp. 552-554, Dec. 1996.

[4] L. K. J. Vandamme, Xiaosong Li, Dominique Rigaud, "1/f Noise in MOS Devices, Mobility or Number Fluctuations?," IEEE Transactions on Electron Devices, vol. 41, pp. 1936-1945, Nov. 1994.

[5] Ming-Horn Tsai, Tso-Ping Ma, "Effect of Radiation-Induced Interface Traps on 1/f Noise in MOSFET's," IEEE Transactions on Nuclear Science," vol. 39, pp. 2178-2185, Dec. 1992.

[6] Fan-Chi Hou, Gijs Bosman, Mark E. Law, "Simulation of Oxide Trapping Noise in Submicron n-Channel MOSFETs," IEEE Trans. Elec. Dev., vol. 50, Mar. 2003.

[7] M. N. Ericson, C. L. Britton, J. M. Rochelle, B. J. Blalock, D. M. Binkley, A. L. Winterberg, B. D. Williamson, "Flicker Noise Behavior of MOSFETs Fabricated in 0.5μm Fully Depleted (FD) Silicon-on-Sapphire (SOS) CMOS in Weak, Moderate, and Strong Inversion," IEEE Trans. Nucl. Sci., vol. 50, pp. 963-968, Aug. 2003.

[8] Henry W. Ott, "Noise Reduction Techniques in Electronic Systems," 2nd Edition, New York: John Wiley & Sons, Inc., 1988, pp. 228-241.

[9] Chih-Hung Chen, M. Jamal Deen, "Channel Noise Modeling in Deep Submicron MOSFETs," IEEE Transactions on Electron Devices, vol. 49, pp. 1484-1887, Aug. 2002.

[10] John. A. McNeill, "Noise in Short Channel MOSFETs," IEEE 2009 Custom Integrated Circuits Conference, pp. 567-572, 2009.

[11] Suharli Tedja, Jan Van der Spiegel, Hugh H. Williams, “Analytical and Experimental Studies of Thermal Noise in MOSFETs,” IEEE Transactions on Electron Devices,” vol. 41, pp. 2069-2075, Nov. 1994.

[12] Xin He, William B. Kuhn, “A 2.5-GHz Low-Power, High Dynamic Range, Self-Tuned Q-Enhanced LC Filter in SOI,” IEEE Journal of Solid-State Circuits, vol. 40, pp. 1618-1628, Aug. 2005.

[13] Kent H. Lundburg, “Noise Sources in Bulk CMOS.”

[14] S. M. Sze, “Semiconductor Devices, Physics and Technology,” 2nd Edition, USA: John Wiley & Sons, Inc., 2002, pp. 60-66.

[15] Saeed Mohammadi, Dimitris Pavlidis, “A Nonfundamental Theory of Low-Frequency Noise in Semiconductor Devices,” IEEE Transactions on Electron Devices, vol. 47, pp. 2009-2017, Nov. 2000.

[16] Leopoldo D. Yau, Chih-Tang Sah, “Theory and Experiments of Low-Frequency Generation-Recombination Noise in MOS Transistors,” IEEE Transactions on Electron Devices, vol. ED-16, pp. 170-177, Feb. 1969.