STUDY AND PERFORMANCE CHARACTERIZATION OF TWO KEY RF HARDWARE SUBSYSTEMS: MICROWAVE DIVIDE-BY-TWO FREQUENCY PRESCALERS AND LOW NOISE AMPLIFIERS

by

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Abstract

This thesis elaborates on the theory and art of the design of two key RF radio hardware subsystems: analog Frequency Dividers and Low Noise Amplifiers (LNAs). Specifically, the design and analysis of two Injection Locked Frequency Dividers (ILFDs), one Regenerative Frequency Divider (RFD), and two different LNAs are documented. In addition to deriving equations for various performance metrics and topology-specific optimization criterion, measurement data and software simulations are presented to quantify several parameters of interest. Also, a study of the design of LNAs is discussed, based on three "regimes:" impedance matching, transconductance-boosting, and active noise cancelling (ANC). For the ILFDs, a study of injection-locked synchronization and phase noise reduction is offered, based on previous works.

As the need for low power, high frequency radio devices continues to be driven by the mobile phone industry, Frequency Dividers that are used as prescalars in phase locked loop frequency synthesizers (PLLs) must too become capable of operation at higher frequencies while consuming little power. Not only should they be low power devices, but a wide "Locking Range" (LR) is also desired. The LR is the bandwidth of signals that a Frequency Divider is capable of dividing. As such, this thesis documents the design and analysis of two ILFDs: a Tail-ILFD and a Quench-ILFD. Both of these ILFDs are implemented on the same oscillator circuit, which consumes 2.28 mW, nominally. Measurements of the Tail and Quench-ILFDs' LRs are plotted, including one representing the Quench-ILFD operating at "very low" power. Also, an RFD is detailed in this thesis, which consumes 410 μW. This thesis documents Locking Ranges for the Tail and Quench-ILFDs of 12% and 3.7% of 6.4 GHz respectively, during nominal operation. In "very low" power mode, the Quench-ILFD has a LR of 4.8% while consuming 219.6 μW of power. For the RFD, simulations report a LR of 16.7% while consuming 410 μW.

Recently in 2011, a wideband LNA topology by Nozahi et al., which employs Partial Noise Cancelling (PNC) of the thermal noise generated by active devices, was presented and claimed to achieve a minimum and maximum NF of 1.4 dB and 1.7 dB (from 100 MHz to 2.3 GHz), while consuming 18 mW from a 1.8 V supply. This thesis details the theory, design, and

simulation results of a narrowband version of this PNC LNA. In order to compare the large-signal performance of this narrowband LNA to that of a well-known implementation, an LNA employing inductive source-degeneration (referred to as a "S-L LNA") is designed and analyzed through simulation. The PNC LNA operates at a frequency of 2.3 GHz while the S-L LNA operates at 2.8 GHz. Simulations report a NF of 1.76 dB for the PNC LNA and 2.3 dB for the S-L LNA, at their respective operating frequencies. Both LNAs consume roughly 15 mW of quiescent power from a 1.8 V supply.

Lastly, a case for the suspected design and layout faults, which caused fabricated versions of the RFD and two LNAs documented in this thesis to fail, is presented. First, measurements of the two LNAs are shown, which display the input impedance of the S-L LNA and the s_{21} responses for both. Then, general layout concerns are addressed, followed by topology-specific circuit design flaws.

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Acknowledgements

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I took Electronics II with Dr. Dyer, a class that set up my path into the world of RFIC design. As a student, Dr. Dyer not only answered all of my off-the-wall questions and encouraged my curiosity, but also spent countless hours after class with me helping to develop my intuition and knowledge regarding the field of electronic design. He was and is my main inspiration.

Dedication

First and foremost, I'd like to dedicate this work to my ever-loving parents, Sinaa Abdulamir and Imad Khamis. My mother, a mechanical engineer, and my father, a professor of statistics, always emphasized the importance of a strong education. Originally immigrating to the USA from Iraq in 1990, my parents witnessed their fair share of hardships, both culturally and financially. Despite raising 5 children on the meager "salary" of a Ph.D. graduate student, my parents always found the time to support me in my academic endeavors – whether that implied helping me with my homework during elementary school, or fiercely disciplining me when my performance was…less than satisfactory. After what seemed an eternity, my parents encouraged me to pursue electrical engineering upon graduation from high school, and never once doubted my abilities to overcome any challenge in my way. I can only hope that I've made my parents as proud as they have made me.

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I'd also like to dedicate this to my closest childhood homies: Ayman Al-Ashtal and Sam Gharaibeh. While I was still a young man, Ayman set an unwavering and unmatched example of what true courage, heart, respect, and intelligence is. I have never met anyone who is more genuine and fearless than he. I hope with all my heart that we meet again soon and get back to where we was. Sam taught me the importance of questioning everything I believe to be true and

re-evaluating deep, personal beliefs on the basis of what I believe to be right in my heart. Talented, witty, and the most emotionally-intelligent person I know – I hope Sam continues to provide me with the advice that has improved my life over the several years that I've known him. Without Sam's one-of-a-kind advice and unique, cosmic perspective on life, I would not be the happy person I am today. You guys are my brothers.

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Chapter 1 - Introduction

1.1 Objective

This thesis focuses on two critical subcircuits needed to implement low power, high frequency radio receivers: analog Injection-Locked Divide-by-2 Prescalars and Low Noise Amplifiers (LNAs). Chapter 1 explains the background and motivation that drive the need for LNAs and Frequency Dividers in modern radio applications. In chapter 2, prior art and current industry implementations for these two subsystems will be explained in terms of performance features and limitations. Chapter 3 elaborates the theory, analysis, design, simulation, and layout of (i) a "Quench" Injection-Locked Frequency Divider (ILFD), (ii) a "Tail" ILFD, and then (iii) a Regenerative Frequency Divider (RFD), also known as a "Miller Divider". Next, Chapter 4 reports the theory, analysis, design, simulation, and layout of (i) a Source-Inductor LNA (S-L LNA) and (ii) a Partial Noise-Cancelling LNA (PNC-LNA) based on the works of [1]. Finally, Chapter 5 concludes the document by summarizing and comparing the performance of the researched Frequency Divider and LNA topologies.

1.2 Background

1.2.1 Divide-by-2 Injection-Locked Frequency Dividers

ILFDs are extensively used in Phase-Locked-Loop (PLL) Frequency Synthesizers, or simply "PLLs". Ideally, a PLL provides a stable output frequency with minimized *phase noise*. PLL's are used in a variety of RFIC subsystems, for both transmit and receive operations. Figure 1.1 shows the architecture of a modern PLL implementation. A stable reference frequency is generated using a temperature-compensated crystal oscillator (TCXO). This signal is divided by some value *R*. A Phase-Frequency Detector (PFD) provides a signal proportional to the difference in phase (or frequency) between the reference signal and the output signal, after being

divided by both *P* and *N*, respectively. This signal drives the Charge Pump that provides the tuning voltage to a VCO. The loop filter (lowpass type) is necessary for stability and to control the dynamics and response time of the feedback system.

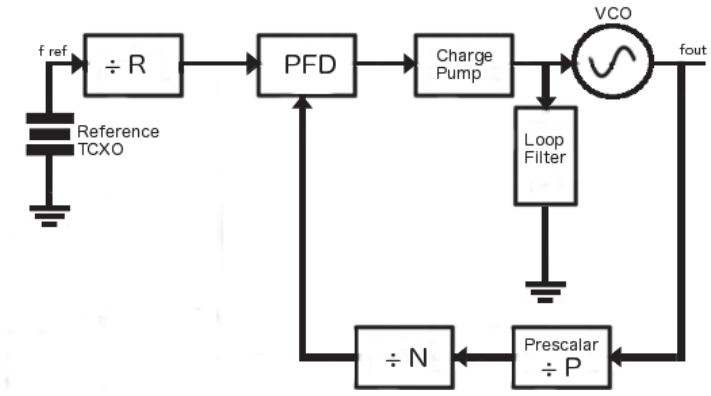

Figure 1.1 Modern PLL Architecture

The output frequency generated by such a PLL can be expressed as:

$$f_o = \left(\frac{f_{ref}}{R}\right)NP \tag{1.1}$$

and the minimum step size is:

$$f_{step} = \left(\frac{f_{ref}}{R}\right)P \tag{1.2}$$

As a result, the prescalar block is a determining factor of the range of frequencies that can be generated, unless a fractional-N architecture is used [3] [4].

The reason prescalars need to be used in the first place is because the digital circuitry that composes the divide-by-N block in Figure 1.1 is often too slow to process the higher GHz frequencies employed in newer wireless receivers. Using a prescalar subverts this issue, by providing the digital circuitry with a lower frequency input that can be properly divided. As a result, the development of ILFDs remains a strong subject of interest among RFIC researchers.

1.2.2 Low Noise Amplifiers

Low Noise Amplifiers serve as the first active stage for typical receiver architectures. The LNA and the passive circuitry that precedes it compose what is often referred to as the "front end" of a radio receiver. As the first active stage, the LNA determines many performance metrics of the entire radio system, such as the receiver sensitivity, out-of-band IIP3, and dynamic range. As mobile consumer technologies continue to support high-data and high-speed transmissions, it is paramount that these devices maintain sufficient operation in the context of these characterizations, while remaining low power. Unlike intermediate frequency (IF) amplifiers, buffer amplifiers, or chained amplifiers that typically appear in RF receivers, the design of LNAs requires input matching, gain boosting, noise cancelling, and frequency selective techniques in order to optimize receiver performance metrics, such as Noise Figure.

Noise Figure of Cascaded Systems

A receiver's *Noise Figure* (referred to as "F") is primarily established by the first stage in a cascaded network, if the gain of that stage is sufficiently large. H. T. Friis showed this in [2]. To illustrate this important point, consider Figure 1.2, which depicts a signal generator of voltage V_{in} with Thevenin impedance R_{source} and two cascaded 2-Port Networks (2PNs) with the second 2PN connected to a load:

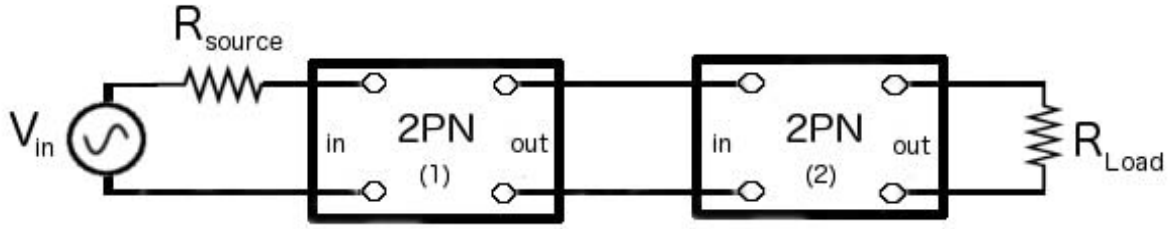

Figure 1.2 Signal source followed by two cascaded 2PNs and load impedance

In the context of communication circuits, the above figure represents a receiver front-end consisting of an antenna of impedance R_{source}, an LNA, followed by perhaps an amplifying, mixing, or filtering stage. $2PN_1$ represents the LNA and $2PN_2$ represents the next stage.

A voltage source, such as V_{in}, provides maximum power transfer to a load when the next stage's input impedance is *matched* to the source impedance, i.e. $R_{source} = R_{2PN,in}$. When this is true, the maximum available signal power can be described by:

$$P_{signal} = \frac{[V_{in}\left(\frac{R}{R+R}\right)]^2}{R} = \frac{{V_{in}}^2}{4R_{source}} = S_0 \quad (1.3)$$

where R indicates both the source impedance and the input impedance of $2PN_1$. Next, a signal source of Thevenin resistance R will produce thermal noise power of magnitude:

$$P_{noise} = kTB \quad (1.4)$$

delivered to a matched load, where k is Boltzmann's constant (1.38×10^{-23} J/ºK), T is the absolute temperature of the operating circuitry (typically 290 ºK in room-temperature, low power devices), and B is the *effective* bandwidth of the receiver system. This bandwidth is typically set by the off-chip BPF, the LNA, or both.

To illustrate a typical figure of a modern receiver, consider a Bluetooth device operating at 2.45 GHz, with a bandwidth of 245 MHz. For the signal and noise powers given here, the SNR can be defined as:

$$SNR_{input} = \frac{S_0}{kTB} \quad (1.5)$$

The noise power produced by the source impedance appears at the input terminals of $2PN_1$, which is amplified by the network's power gain G_1. Due to the internal circuitry that comprises $2PN_1$, additional noise will be introduced because of thermal effects from individual circuit elements. Considering this additional noise, the total available noise power at the output terminals of $2PN_1$ is:

$$P_{noise2PN1out} = F_1 G_1 kTB \quad (1.6)$$

where $F_1 \geq 1$ to account for the excess noise introduced. Similarly, the noise power that appears at the inputs of $2PN_2$ will also be amplified, this time by the gain of the second network G_2. Now the total noise power at the output terminals of $2PN_2$ can be expressed as:

$$P_{noise,2PN2out} = F_{12}\, G_1\, G_2 kTB \quad (1.7)$$

F_{12} represents the noise figure of the comprehensive system consisting of networks $2PN_1$ and $2PN_2$. However, as $2PN_2$ likely also contains thermal noise generating circuitry, it too will also have its own individual contribution to total available noise power at its output terminals. The noise power due solely to $2PN_2$ is:

$$P_{noise,2PN2} = (F_2 - 1)G_2kTB \tag{1.8}$$

Whereas the noise contribution due to the circuitry of $2PN_1$ is:

$$P_{noise,2PN1} = (F_1 - 1)G_1G_2kTB \tag{1.9}$$

Note that the $(F_i - 1)$ factor originates from the fact that the initial kTB noise was introduced by the signal source, which is subtracted out to obtain the noise contribution of only the 2PN of interest. Another observation from the above expressions is that the noise power of the first 2PN is amplified twice before appearing at the load. The noise power of the second 2PN is only amplified once. To illustrate the consequence of this fact on the total system noise figure, consider the expression for total available noise power at the output terminals of $2PN_2$, due to each stage's own contribution:

$$\begin{aligned} P_{noise,2PN2out} &= G_1G_2kTB + (F_1 - 1)G_1G_2kTB + (F_2 - 1)G_2kTB \\ &= G_1G_2kTB\left[1 + (F_1 - 1) + \frac{F_2 - 1}{G_1}\right] \\ &= G_1G_2kTB\left[F_1 + \frac{F_2 - 1}{G_1}\right] \end{aligned} \tag{1.10}$$

Equating this to (1.7) shows:

$$P_{noise,2PN2out} = G_1G_2kTB\left[F_1 + \frac{F_2 - 1}{G_1}\right] = F_{12}\,G_1\,G_2kTB \tag{1.11}$$

Dividing both sides by the similar terms shows that the noise figure describing the entire system of 2PNs results in:

$$F_{12} = F_1 + \frac{F_2 - 1}{G_1} \tag{1.12}$$

so that for a system of power-amplifying stages, the noise figure is dominated by the first stage, if it is of sufficient power gain G_1. Expanding this analysis to a chain of 3 2PNs would reveal:

$$F_{123} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} \tag{1.13}$$

Optimizing Circuit Noise Figure

To understand how to optimize the noise figure of a single stage such as F_1, consider the expression for the noise figure of a system composed of a signal source, one amplifying stage (such as an LNA), and a load impedance:

$$F = \frac{N_{out}}{N_{in} G} = \frac{N_{in} G + N_{sys}}{N_{in} G} = 1 + \frac{N_{sys}}{N_{in} G} \tag{1.14}$$

This suggests that for a low noise figure, the noise contribution from the stage's circuit should be minimized while keeping its power gain large in magnitude. The expression also implies a minimum theoretical noise figure of unity for a noise-less network, where all the noise power would have originated at the signal source.

Many different circuit-level techniques for the development of LNAs that optimize the above criterion have been researched and developed since the establishment of noise figure [5] [6]. In RF-tuned circuits, reactive components are used to provide matching and associated high-gain and low-noise paths for received signals. In wideband applications, where frequency-selective components are not usable, methods of noise figure improvement have begun to focus more on clever CMOS topologies, such as "noise cancellation" [1].

Both wideband and narrowband receivers can benefit from noise-cancellation architectures. Many methods of noise cancelling in FET circuits have been developed, using active coupling, differential circuits, and/or feedback to mitigate individual FET noise contribution [6] [8]. These circuits often employ g_m-boosting techniques and impedance matching as well. The study of LNA design techniques in this thesis focuses on adopting recently developed wideband noise cancellation circuits to narrowband LNAs to achieve good performance in terms of both noise figure and large-signal processing capabilities.

Chapter 2 - Background Theory and The State of The Art

2.1 Divide-by-2 Injection-Locked Frequency Dividers

The output frequencies needed in modern PLL circuits are well into the GHz range, which is too high for programmable digital dividers, thus the need for prescalars. In the past, a common approach has been to use a high-speed Source Coupled Logic (SCL) divide-by-2 circuit based on the D flip-flop architecture [7]. Figure 2.1 shows such a circuit:

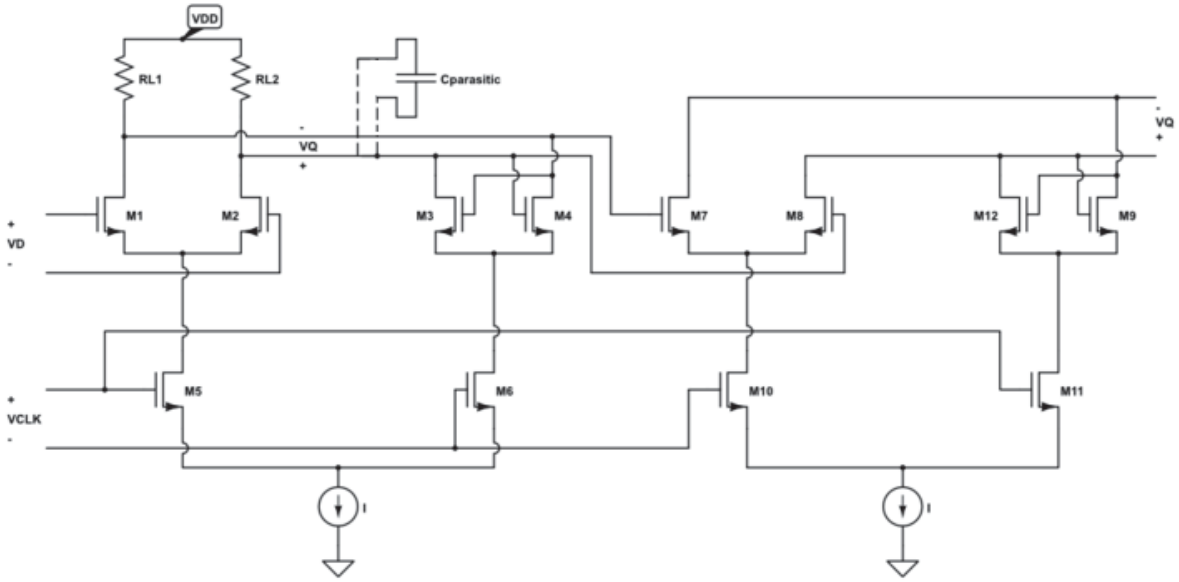

Figure 2.1 SCL Divide-by-2 Circuit

For the divider in figure 2.1, when V_{CLK} is positive, the first latch is transparent, and a differential voltage V_Q is established. FETs M_1 and M_2 form the "D" input. When V_{CLK} is negative, the cross-coupled pair formed by M_3 and M_4 latch the state and provides a fixed output to the second latch, which is now transparent. The maximum frequency this circuit can operate at is determined by:

$$\tau = \frac{C_{parasitic}}{\left(\frac{1}{R_L} - g_m\right)} \tag{2.1}$$

In current practice, f_{max} tends to be limited to ~3GHz, due to the parasitic capacitances illustrated in Figure 2.1. The capacitor $C_{parasitic}$ represents the capacitance formed by the differential lines that connect the drains of M_3 and M_4 to the drains of M_1 and M_2. Regardless of transistor sizing, $C_{parasitic}$ remains a result of the metal traces that provide these connections. In addition to this, R_{L1} and R_{L2} also introduce some parasitic capacitance at this node. High-valued resistors may be formed by connecting a number of N-well regions in the substrate through metal connections, and have a fixed resistance-per-length ratio. The resistors introduce a parasitic capacitance (that increases with increasing resistance), which limits the maximum value of the load impedance. The parasitic capacitance $C_{parasitic}$ and the limit on R_L imply that for a high f_{max}, g_m must be maximized. For this reason, this type of frequency divider is known for its high power consumption, which is another reason it is inferior to alternatives such as injection-locked architectures.

ILFDs work by forcing a free-running resonator to change its oscillation frequency by means of injecting signals at frequencies *near* the fundamental frequency of oscillation, directly into the resonator. Since the circuit is basically an oscillator, an inductor cancels parasitic capacitances, allowing the circuit to operate at significantly lower power than the SCL divider of Figure 2.1. Their primary disadvantage is a limited bandwidth of synchronization due to the oscillator's tuned load. Figure 2.2 can be used to understand the operation of a generic ILFD:

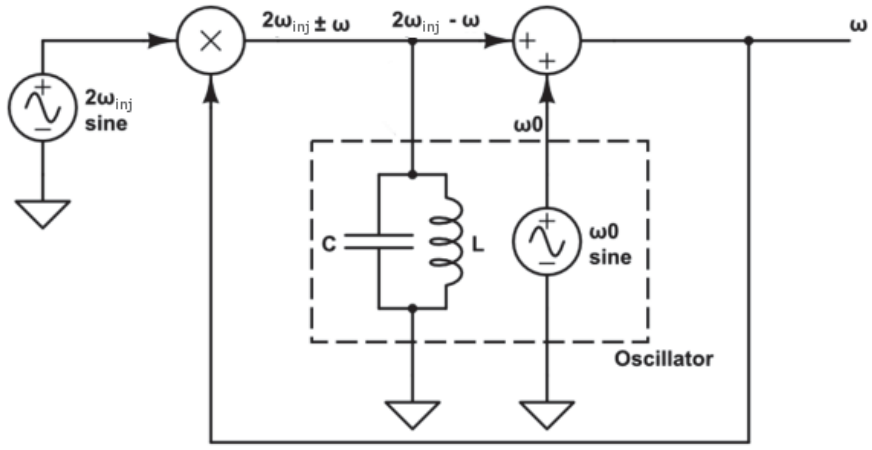

Figure 2.2 ILFD Block Diagram

The oscillator in Figure 2.2 has a fundamental frequency ω_o. As can be seen above, an ILFD works by mixing the input signal (at twice the desired output frequency), with the output of the oscillator, of frequency ω. The mixing product at $2\omega_{inj}$ - ω survives the filter, and reinforces the tank's oscillations at ω_o.

When the deviation of ω_{inj} from ω_o is small (i.e. within the linear region of a tuned load's $\partial\phi/\partial\omega$ relationship), the change in oscillation frequency from ω_o to ω_{inj} can be explained by the transient modification of the phase term of the sinusoidal output. In other words, this summing of the two signals in Figure 2.2 results in frequency modulation of the oscillator voltage. Using a phasor diagram to represent the frequencies and phase difference between the frequency-halved injection signal (at the output of the mixer in Figure 2.2) and the output oscillation, the locking of oscillators is mathematically treated in Chapter 3. The range of signal frequencies (centered around the fundamental frequency of the resonator), referred to as the "locking range," is dependent on the quality factors of the inductor and capacitor that make up the tank circuit. The quality factor (Q) is a metric of how much energy is lost during each cycle of oscillation, which also determines how long a resonant circuit will oscillate for a given input energy. The Q of the overall tank circuit is typically set by the on-chip inductor, and is given as:

$$Q_{LC} \approx Q_L = \frac{j\omega L}{R_{series}} \tag{2.2}$$

where R_{series} is the lumped resistances of the metal trace that forms the inductor, L is its inductance, and Q_L is its quality factor. Typically, capacitors implemented on-chip are of such high Q that the quality factor of the inductor dominates.

Two of the most popular ILFDs used as analog prescalars are the "Tail-ILFD" and the "Quench-ILFD."

2.1.1 "Tail-ILFDs"

Tail-ILFDs are so named because the input signal is applied to the gate of MOSFET that provides the tail current for a differential pair-based negative-resistance oscillator. To understand how mixing, filtering, and injection-locking processes take place in a Tail-ILFD, observe the following figure, which is a generic schematic of a Tail-ILFD implemented using a single-balanced mixer and a negative-resistance oscillator:

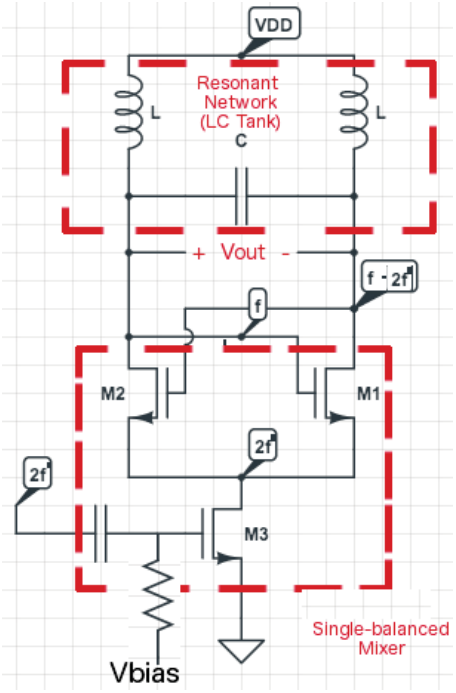

Figure 2.3 Generic Tail-ILFD

In Figure 2.3, the input signal is applied through an AC coupling capacitor directly to the gate of the current source FET, M_3. Because this FET is in a Common-Source amplifier configuration, this signal appears at the drain of M3 at a value of:

$$V_{DM3}(t) = V_{in}(t)A_v(t) \approx \frac{V_{in}(t)g_{m3}}{g_{m1}(t)} \tag{2.3}$$

where g_{m1} and g_{m3} are the transconductances of the M_1 and M_3, respectively. The transconductance g_{m1} is a function of time since its gate is tied to the output voltage of the oscillator. Next, the input signal at the source of M_1 is mixed with the oscillations of the tank, via

the cross-coupling of FETs M_1 and M_2. To illustrate how this qualifies as a mixing operation, Figure 2.4 depicts a simple switch-based mixer scheme: multiplying a sine wave at a frequency f_1 with a square wave at a frequency f_2.

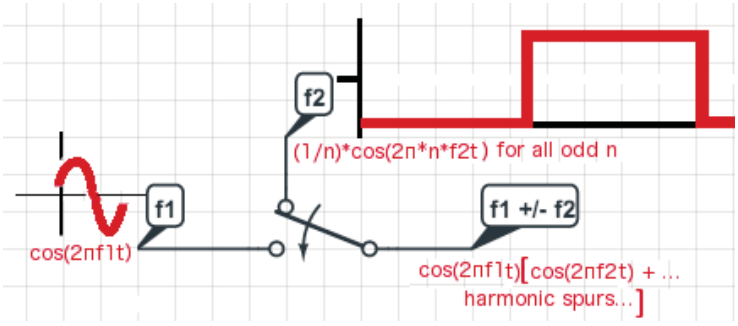

Figure 2.4 Switch-Based Single-balanced Mixer Scheme

It is well known that for a square-wave pulse train the Fourier series is:

$$s_{square}(t) = V_{os} + \frac{4}{\pi}\sum n\left[\frac{cos(2\pi(2n-1)ft)}{2n-1}\right]$$

$$= V_{os} + \frac{4}{\pi}(cos(2\pi ft) + \tfrac{1}{3}(cos(2\pi 3ft) + \tfrac{1}{5}(cos(2\pi 5ft) + \dots) \quad (2.4)$$

where V_{os} is a dc value if the square wave is unipolar as in Figure 2.4. It can be seen from the expansion above that a square pulse train in time is composed of the fundamental frequency (calculated as the inverse of the period of one square wave) and its odd harmonics. The following figure is a graphic representation of the frequency spectrum of such a signal:

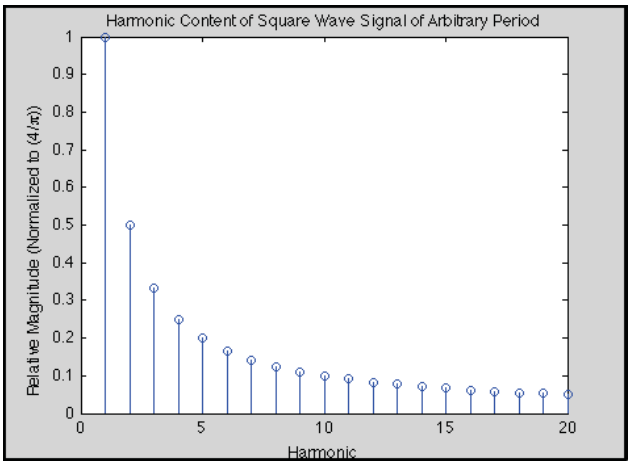

Figure 2.5 Frequency Spectrum of Arbitrary Square Wave

In the context of Figure 2.3, the switch is implemented by M_1 in Figure 2.3, one of the cross-coupled FETs that compose the negative resistance of the active oscillator. The square wave represents whether or not M_1's channel is open (magnitude of 1) or closed (magnitude of 0). An amplified version of the input signal at the Source of M_1 appears at M_1's Drain due to its Common Source (CS) configuration. The resultant signal is given by:

$$V_{DrainM1} = V_{DM3}(t)\left[\left(\frac{1}{2}\right) + \left(\frac{4}{\pi}\right)cos(2\pi f_2 t) + \tfrac{1}{3}cos(2\pi 3 f_2 t) + \tfrac{1}{5}cos(2\pi 5 f_2 t) + \cdots \right] \quad (2.5)$$

The signal injected into the tank contains not only the product of an ideal mixing operation of *2f* and *f*, but also all of the attenuated odd-numbered harmonic components of the switch-controlling square wave. However, due to the LC network at the node of the injecting signal, all of the higher-frequency components of the mixing operation are shorted to AC ground. Figure 2.6 illustrates the waveform discussed, without the detailed magnitude information.

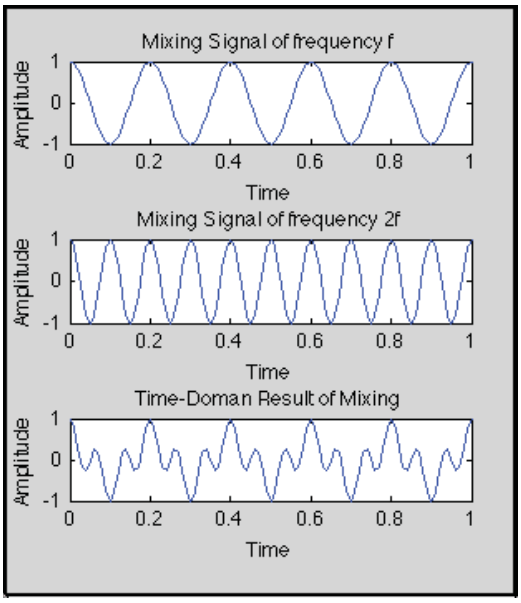

Figure 2.6 The Mixing of Two Signals

It is clear that the mixed signal, at the bottom of Figure 2.6, contains more than one frequency component. However the LC tank is tuned to the lower frequency component, selecting only the half-frequency of the *2f* input.

Ultimately, a Tail-ILFD operates by mixing a signal of twice the desired locking-frequency with the fundamental frequency of the oscillatory network, thus injecting a signal into the tank. If the quality factor of this network is such that the impedance of it at the frequency of the injected signal is sufficiently high, then phase-locked oscillation at this injected frequency can be sustained indefinitely. The phenomenon that controls the input magnitude required for "injection-locking" is explored in detail in Section 3.1, and a condition for locking is given that applies for both Tail and Quench-ILFDs.

2.1.2 "Quench" ILFDs

Quench-ILFDs are based on the same block-diagram level architecture depicted in Figure 2.1. The main difference between the two is where the input signal is applied to the circuit.

Quench-ILFDs are so named because the mixing operation is done by "quenching" the output terminals, i.e. momentarily connecting them via low impedance, as shown in Figure 2.7

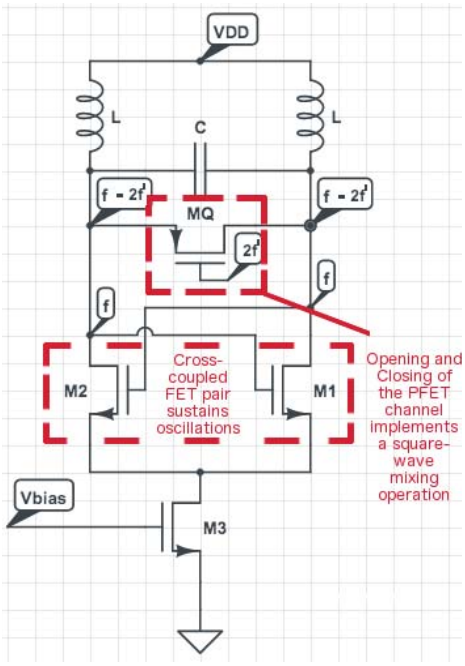

Figure 2.7 Generic Quench-ILFD

In a Quench-ILFD, the mixing operation is performed directly at the output terminals of the circuit, implemented by connecting a FET between these two terminals and applying the input signal to its gate in Figure 2.7. As the input signal drives the FET between states of triode and cutoff, the square-wave mixing signal appears on the Quench FET, M_Q. That is, a low voltage on M_Q's gate shorts M_1's drain to M_2's drain, which is a "multiply by zero." A high input voltage forces M_Q into cutoff, which is a "multiply by one." Other than this main difference, the Quench and Tail-ILFDs operate through essentially the same mechanisms.

While the means of synchronization of frequencies due to injection is not obvious upon inspection of a Tail-ILFD, seen in Figure 2.2, the placement of the "injection FET" M_Q offers some insight on how the injected signal, of roughly twice the frequency of the tank's resonant frequency, controls the instantaneous frequency of the oscillator. It also demonstrates the reduction in phase noise observed in all oscillators when they are injection-locked, including the

aforementioned Tail-ILFD. To illustrate this, Figure 2.8 displays the time domain waveforms of a Quench-ILFD:

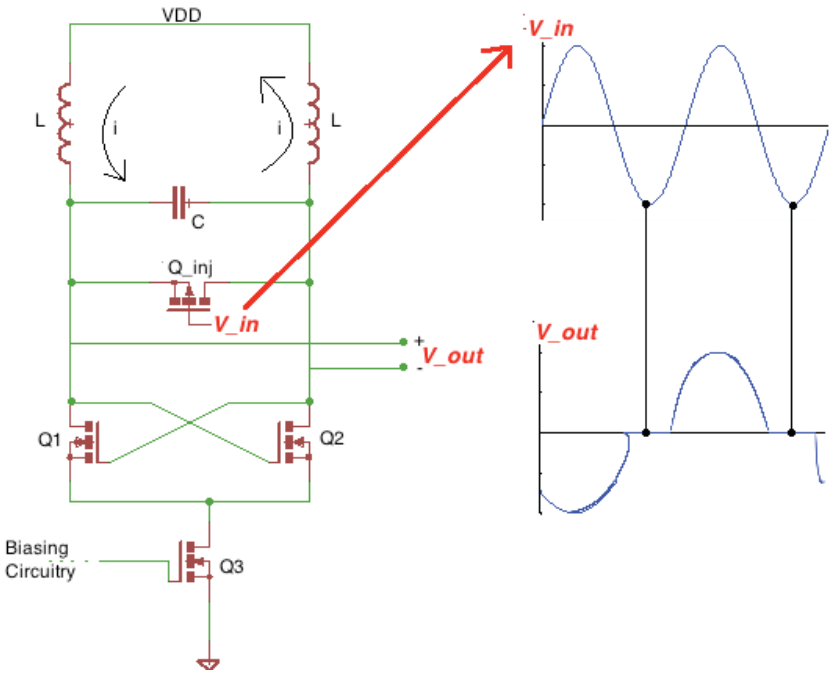

Figure 2.8 Transient Synchronization Mechanism of Quench-ILFD

The voltages on the gate of Q_{inj} and of the output oscillations are depicted on the right (not to scale). The outputs are shorted together (thus forcing a "zero-crossing" of the oscillation waveform) when the voltage on the gate of the pFET Q_{inj} is at its minimum value. Controlling the output's zero-crossings forces the oscillation frequency to be exactly half of V_{in}'s frequency and significantly reduces the jitter, relative to its free-running case. The reduction of phase noise in injection locked oscillators is elaborated in Chapter 3.

2.1.3 Regenerative ILFDs

Regenerative Frequency Dividers (RFDs) are similar in concept to the ILFDs discussed above, but differ in the fact that they do not have a free running oscillation. The block diagram of a Regenerative Frequency Divider is shown below:

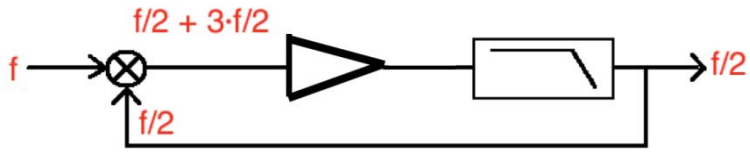

Figure 2.9 Regenerative Frequency Divider Block Diagram

Typical RFD implementations include the use of double-balanced mixers, followed directly by gain and filtering stages. The lowpass filter (LPF) is needed to provide mixer feedback at the desired locking frequency. It is important that the phase shift around the loop is an integer multiple of 2π, in order to satisfy the Barkhausen criterion of sustained oscillations.

The *Gilbert Cell* and MOSFET switches are popular topologies used to implement IC mixers. The mixing products are then filtered in order to obtain the desired locking frequency, which is then amplified and fed back to the mixer. In Figure 2.9 a lowpass filter is shown, although a bandpass LC tank may be considered to operate at higher frequency with less power, as is the case with ILFD designs. In this way, regenerative frequency division can occur, so long as there is an input excitation. Otherwise, free-running oscillations do not exist in an ideal RFD.

2.2 Low Noise Amplifiers

The noise figure of a LNA is mainly dependent on its input impedance match with the signal source (usually an antenna or crystal-based BPF), its power gain, and the noise generated by the LNA circuitry. As such, most LNA developments have emphasized improvements within these three categories. Specifically, this thesis summarizes LNA prior art in three specific regimes: (i) *Impedance Matching*, ensuring that the source and the LNA input are of the same resistive impedance, (ii) g_m*-Boosting*, or ways of increasing overall power gain, and (iii) *Active Noise Cancelling* (ANC) design, which employs the use of various circuit topologies that either fully or partially cancel the noise of the LNA itself.

2.2.1 Impedance Matching Techniques

Researched impedance-matching techniques are either wideband designs, which use resistive and active components, or narrowband designs, which use reactive components. Three wideband impedance matching designs are presented here: (i) Resistive termination matching, (ii) Source termination matching, and (iii) Shunt-Shunt resistive feedback matching.

Wideband Designs

Resistive termination

Resistive termination is the most straightforward approach to matching the LNA's input to any arbitrary source impedance. Observe the following figure, which demonstrates how this is accomplished:

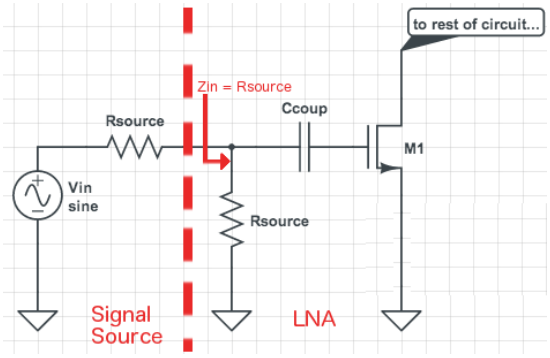

Figure 2.10 Resistive Input Termination

In the figure above, the signal source is shown on the left of the dashed line. It has internal impedance described by R_{source}, which is usually 50Ω in standard RF communication hardware. Matching is accomplished by connecting a resistance equal to R_{source} between ground and gate of M_1, through the use of a low-impedance reactance. Note that this is purely an AC connection, as the DC-blocking capacitor prevents the resistive termination from affecting the

bias points of the devices. The input to the LNA is on the right of the dashed line, and "looking" into the LNA's input reveals an impedance of:

$$Z_{in} = R_{source} // [\frac{1}{j\omega C_{coup}} + \frac{1}{j\omega C_{gateM_1}}] \quad (2.6)$$

Typically, the reactance due to the coupling capacitor in series with the gate and overlap capacitances of the amplifying transistor (M_1, here) is very high, since minimally sized transistors are used for high-frequency operation. Of course, the coupling capacitor adds very little reactance at high frequencies, by design. So, if:

$$X_{CgateM1} >> R_{source} \quad (2.7)$$

Then the input impedance of the LNA is approximately:

$$Z_{in} \approx R_{source} \quad (2.8)$$

leading to a matching of the impedances between the signal source and the LNA. However, this approach remains a last approach among RF design engineers, as it has a detrimental effect on the noise figure of the system. Observe the following figure, which is a noise model of a simple wideband, single-transistor LNA employing resistive input matching:

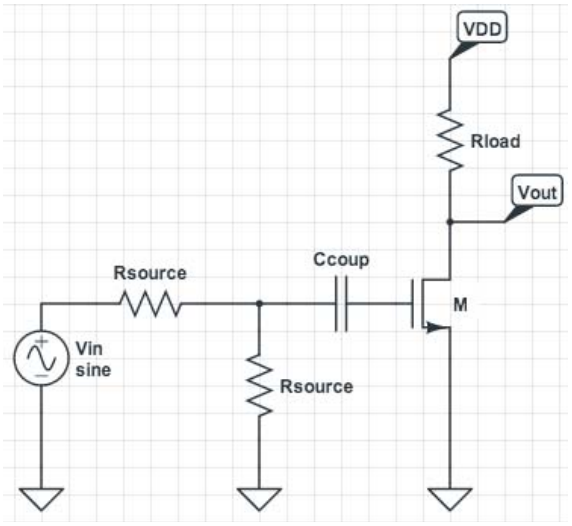

Figure 2.11 LNA Employing Resistive Input Termination

To analyze the noise figure of this topology, it is useful to replace the noisy components in the schematic with their appropriate noise models. Figure 2.12 below represents the models used for the thermal (or "Johnson") noise generated by any resistance *R*, and the thermal noise produced by a FET (of negligible source/drain impedance, high output impedance r_o, and ignoring flicker noise at high-frequency):

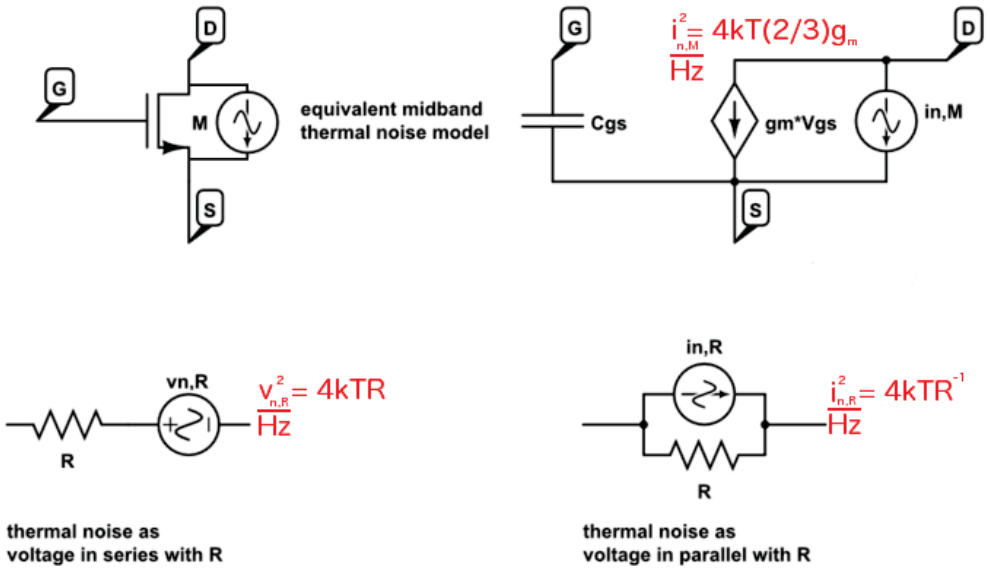

Figure 2.12 Simplified Noise Models for Resistance and MOSFET

As can be seen from Figure 2.12, the dominant noise source in a MOSFET at high frequencies is the thermal noise produced by the non-zero channel impedance, determined at the quiescent point of the transistor. This current spectral density is given as:

$$\left(i_{n,FET}\right)^2 = 4kT\left(\frac{2}{3}\right)g_m \tag{2.9}$$

which is given in units of A^2/Hz. The $(^2/_3)$ term is due to the pinch-off of the channel in the active mode of operation. The dominant noise source of any given resistance *R* is Johnson noise, and the current spectral density is:

$$\left(i_{n,R}\right)^2 = 4kT\left(\frac{1}{R}\right) \tag{2.10}$$

When needed, the voltage spectral density of a resistance may be used. The voltage spectral density, $(v_{n,R})^2$, is expressed in Figure 2.12, and is equal to $4kTR$. By replacing the components in Figure 2.11 with the appropriate models, the effect of each noise source on the output SNR can be determined. Figure 2.13 shows the overall noise model for the LNA:

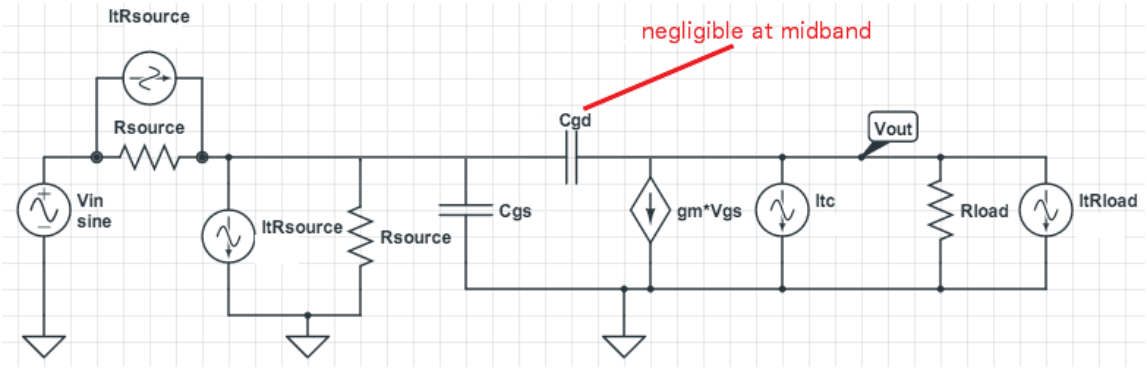

Figure 2.13 Simplified Noise Circuit of Resistive Termination LNA

To determine the Noise Figure for the circuit of Figure 2.11, the procedure is as follows: first, the output voltage (node V_{out} in the figure) that results from each noise current source is calculated. Next, the corresponding output power of each source's output voltage contribution is found using V^2/R_{load}, where all of the output power terms share the same R_{load} value. The total output noise power for the LNA is the sum of all these output power terms. By dividing the total output noise power by the output noise power that arises due to the source impedance only (R_s), the NF of any LNA can be analyzed. The noise figure can then be found from:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{Total\ Output\ Noise\ Power}{Output\ Noise\ Power\ due\ to\ Source} \tag{2.11}$$

Firstly, the output noise power due only to the source is a consequence of the real part of the source impedance and is equal to:

$$P_{out,source} = \left(\left(\left(\frac{1}{2}\right)i_n\right)^2 R_{source}\right)BG = \left(kTB\left(\frac{1}{R_{source}}\right)R_{source}\right)G = kTB[R_s R_L (g_m)^2] \tag{2.12}$$

where *B* is the effective bandwidth and *G* is the power gain of the LNA. Next, the noise due to the resistive-termination resistor is considered. Just like the signal source's internal resistance, the noise presented by this resistor is amplified by the LNA and is:

$$P_{out,R-term} = (\left(\left(\frac{1}{2}\right) i_n\right)^2 R_{source})BG = kTB[R_s R_L (g_m)^2] \quad (2.13)$$

As mentioned, the main source of noise in a FET device operating at a high frequency is due to the thermal noise in the induced channel, and gate noise is typically insignificant [14]. The noise current power spectral density generated is approximated as:

$$i_n^2 = 4kT\left(\frac{2}{3}\right) g_m \quad (2.14)$$

This energy is dissipated through the load R_{load} such that the output noise power within a bandwidth *B* due originating solely from the FET is:

$$P_{out,FET} = \left(\left(\frac{1}{2}\right) i_n\right)^2 R_{load} B = 4kTB\left(\frac{2}{3}\right) g_m R_{load} \quad (2.15)$$

This noise appears directly at the output and therefore isn't multiplied by the power gain of the LNA, *G*. Lastly, the load resistor presents some noise power at the output node of:

$$P_{out,Rload} = \frac{4kTB}{R_{load}} R_{load} = 4kTB \quad (2.16)$$

Solving (2.11) by substituting in terms of (2.12) - (2.16) gives an analytical result for the theoretical minimum noise figure for such an LNA:

$$F = kTB\frac{\left[2R_s R_{load} (g_m)^2 + 4\left(\frac{2}{3}\right) g_m R_{load} + 4\right]}{[kTBR_s R_{load} (g_m)^2]} \quad (2.17)$$

Expression (2.17) shows how a higher LNA power gain has a preferable effect on the noise figure, by minimizing the impact of noise due to the circuitry on the output SNR. This equation also demonstrates the negative impact of resistive-termination impedance matching. Introducing a resistive element at the input of the LNA in this fashion results in a minimum theoretical noise figure of 2, or 3 dB, since:

$$\lim_{G \to \infty}\{F\} = \lim_{g_m \to \infty}\{2 + \frac{4\left(\frac{2}{3}\right)}{R_s g_m} + \frac{4}{R_s R_{load} (g_m)^2}\} = 2 \quad (2.18)$$

when (2.18) is expressed by its decibel equivalent, the NF becomes:

$$10\log[F_{min}] = 10\log[2] = 3\ dB \tag{2.19}$$

This degradation of noise performance leaves much to be desired, and as expected more sophisticated topologies exist in order to eliminate this effect.

What follows for the remainder of this chapter are summaries of very similar analyses of several different LNA topologies that fall into the regimes outlined in the beginning of section 2.2 - not only for impedance matching LNAs, but for g_m-boosting and ANC LNAs as well. Note that some techniques improve performance in more than one regime. Also, these analyses are first order approximations of circuit behavior, since different IC processes will have different strengths and weaknesses in terms of gate oxide capacitance, substrate leakage, FET output impedances, electron and hole mobility, among a host of other process-based characteristics. Lastly, noise-less capacitors, midband operation, and exclusive use of long-channel device noise models are assumed in these analyses.

Source Termination

Source termination LNAs use an active device in order to set the input impedance, instead of a discrete resistor. The following figure is a noise model of a simple source termination Common-Gate (CG) LNA:

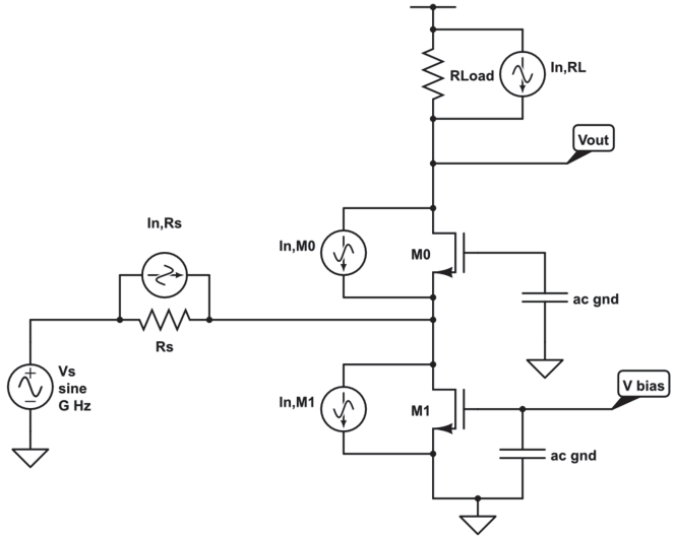

Figure 2.14 Simplified Noise Circuit of Source Termination CG LNA

Instead of simply placing a resistor of arbitrary value in shunt with the LNA's input, source termination establishes the input impedance by means of a FET. In this circuit, M_1 is a current source, which biases M_0, the amplifying transistor. At midband, the impedance looking into the LNA can be expressed as:

$$R_{in} = \left(\frac{1}{g_{m0}}\right) // \, r_{oM1} \approx \frac{1}{g_{m0}} \tag{2.20}$$

To obtain an impedance match, the transconductance of M_0 is set to:

$$g_{m0} = \frac{1}{R_s} = 20\ mS = 20\frac{mA}{V} \tag{2.21}$$

in a 50 Ω communication system. This is a limitation of this circuit – the maximum transconductance is set by the value of the source impedance. Since the input FET is in a CG configuration, the midband gain is estimated as:

$$A_v = \frac{V_{out}}{V_s} \approx g_{m0} R_L \tag{2.22}$$

For this particular LNA topology, the noise originating from R_s yields an output noise power of $kTBR_sR_L(g_{m,0})^2$. Due to the impedance matching condition, $R_s = (g_{m,0})^{-1}$, so the output noise power from R_s can be simplified as $kTBR_Lg_{m,0}$. The output noise power contributions due to

the FETs can be estimated as $kTB(^2/_3)R_L g_{m,0}$ and $kTB(^2/_3)R_L g_{m,1}$ for M_0 and M_1, respectively. The purely resistive load impedance contributes $4kTB$ of output noise power. The expression for the noise figure of this circuit based on these terms is:

$$F = \left(1 + \frac{2}{3}\right) + \frac{\frac{2}{3}g_{m,1}}{g_{m,0}} + \frac{4}{R_L g_{m,0}} \tag{2.23}$$

From (2.23), it can be seen that to optimize the noise performance for the LNA depicted in Figure 2.14, the transconductance of the tail FET M_1 should be kept as low as possible, and the load resistor should be chosen such that $R_L >> (4/g_{m,0})$. In the case where $g_{m,1}$ approaches zero and R_L approaches infinity, (2.23) yields a minimum theoretical noise figure of $^5/_3$, or 2.2 dB, for the simple source termination CG LNA topology.

Shunt-Shunt Resistive Feedback

Shunt-shunt resistive feedback LNAs use a feedback resistor R_F to establish an input impedance based on the LNA's closed-loop gain. The following figure is a noise model for a simplified Shunt-Shunt feedback LNA:

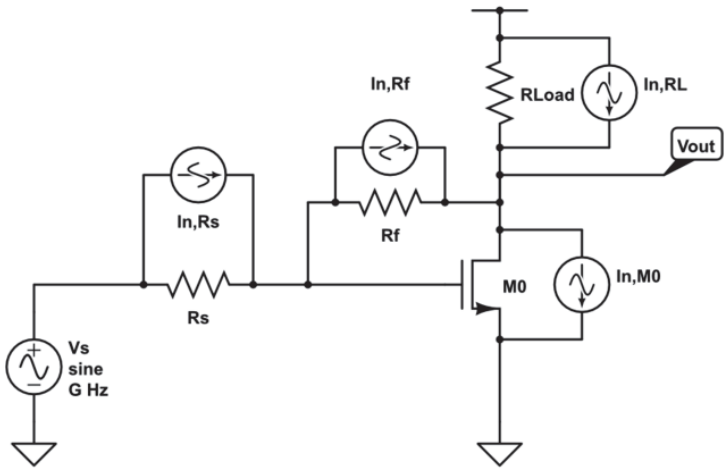

Figure 2.15 Simplified Noise Circuit of Shunt-Shunt Resistive Feedback LNA

When analyzed using feedback theory (where A is open-loop gain and ß is the feedback factor), it can be seen that the input impedance looking info this LNA is estimated to be:

$$R_{in} = \frac{A}{1+A\beta} \approx \frac{g_{mo}(R_F//R_L)}{[(1+g_{mo}(R_F//R_L))]} = \frac{1}{\frac{1}{R_S//R_L}+\frac{1}{g_{mo}}} \quad (2.24)$$

However, for the feedback mechanism to properly work, the load impedance R_L must be much larger than R_F, so that the output current is diverted back to the LNA's input node. So, when $R_F << R_L$, (2.24) becomes:

$$R_{in} = \frac{A}{1+A\beta} \approx \frac{1}{\frac{1}{R_F}+g_{mo}} \approx \frac{1}{g_{mo}} \quad (2.25)$$

It can be seen from (2.25) that this LNA also uses the transconductance of the amplifying transistor to set the input impedance. Due to the feedback mechanism, half of M_0's drain noise is cancelled, and the noise figure is:

$$F = 1 + R_s\left[\frac{1}{R_F}+\frac{1}{R_L}+\frac{2}{3}g_{m,0}\right] \quad (2.26)$$

To obtain an optimal noise figure here, the transconductance of M_0 should be matched to the inverse of the source impedance. In additon to this, R_s, R_F, and R_L should be chosen such that:

$$R_s << R_F << R_L \quad (2.27)$$

which, along with the impedance matching identity of $R_s = (g_{m,0})^{-1}$, results in the same theoretical minimum noise figure as for the source termination CG LNA: 2.2 dB. In [1], a shunt-shunt resistive feedback topology with a reduced NF of 1.7 dB (at 2.3 GHz) is realized through a technique of "noise cancellation." This topology, along with a cascode configuration (discussed later) and a tuned load, forms the basic topology for the PNC LNA studied in this thesis, discussed in Chapter 4.

Narrowband Designs

LC Matching Network

As many radios are designed for only one main frequency of operation, LC Matching Networks are often used to interface an LNA's typically high impedance to a lower source impedance, around a single center frequency. Ideally, these lossless components transform the input impedance to zero, at the resonant frequency of the LC network. This intends to provide full power transfer to the input of the LNA via resonance, and by properly designing the *Q* of the overall network, which includes *C*, *L*, and R_s, significant voltage gain can be obtained between the signal source and v_{gs} of the input FET, whose gate is in parallel with the capacitor of the matching network. The noise figure of this type of LNA is ideally 1, or 0 dB. In order to achieve such a low NF, the quality of the input RLC network at resonance must be very high, which depends on the quality of the inductor and the ratio of the capacitive reactance to R_s. To explain this dependence, observe Figure 2.16, which shows a noise model of a simple LC-matched common-source LNA.

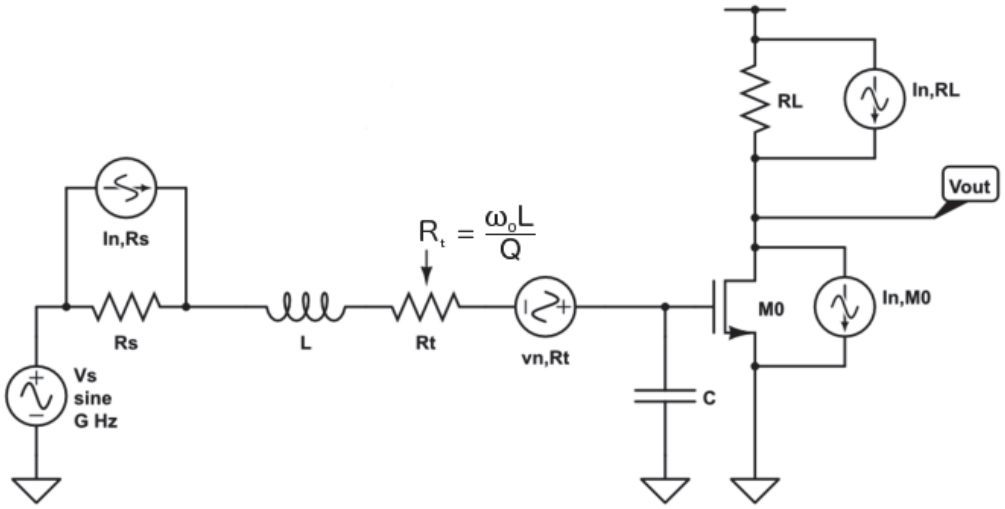

Figure 2.16 Simplified Noise Circuit of LNA employing LC Matching Network

In the circuit of Figure 2.16, an inductor appears in series with the source impedance and resonates with a capacitance in parallel with the input FET's gate, which represents M_0's parasitic capacitance and perhaps some explicit capacitance. While the capacitor is assumed to be noiseless, the noise of the inductor is represented as a thermal noise voltage originating from

the parasitic resistance of the inductor, R_t. R_t is the lumped resistance of the metal traces from which the inductor is fabricated, and at resonance is given as:

$$R_t = \frac{\omega_o L}{Q} \tag{2.28}$$

For an inductor of infinite Q, the noise current approaches zero. However, the resulting noise voltage $v_{n,Rt}$ is amplified to the output with the same gain as the noise from R_s. Ideally, this voltage gain is inversely proportional to ωCR_s, which is designed to be much less than one at ω_o. The resulting NF for this LNA is:

$$F = 1 + \frac{\omega_o L}{Q R_s} + \left(\omega_o C R_s + \frac{1}{Q}\right)^2 \left[\frac{\frac{2}{3}}{R_s g_{m,o}} + \frac{1}{R_s R_L (g_{m,o})^2}\right] \tag{2.29}$$

In the case where $\omega_o CR_s$ approaches zero and Q approaches infinity, (2.29) yields a theoretical minimum NF of 0 dB. In the case where $\omega_o CR_s$ approaches infinity, but Q is low enough that R_t is equal to R_s, the minimum theoretical NF becomes that of the resistive termination CS LNA: 3 dB. As the parasitic resistance of the inductor increases, the NF further degrades, regardless of the LNA's gain.

2.2.2 g_m-Boosting Techniques

Some g_m-boosting circuits are based on topologies that optimize signal gain, while still matching the signal source impedance. Two main types of g_m-boosting exist: (i) device coupling designs, and (ii) tuned-circuit designs.

Device Coupling Designs

Cascode Amplifier

A common cure to the Miller capacitance that plagues Common-Source (CS) amplifiers is to use a cascode configuration. A noise model of a simple cascode amplifier, with an LC input matching network, is shown in Figure 2.17. The Miller capacitance of M_0 (the input transistor) is now limited to:

$$C_{M0} = C_{G,M0}(1 + A_{V,M0}) = 2C_{G,M0} \tag{2.30}$$

where $C_{G,M0}$ is M_0's gate capacitance, and $A_{V,M0}$ is the voltage gain from the gate of M_0 to its drain. In (2.30), the transconductances of M_0 and M_1 are assumed to be equal, which results in $A_{V,M0}$ being equal to one.

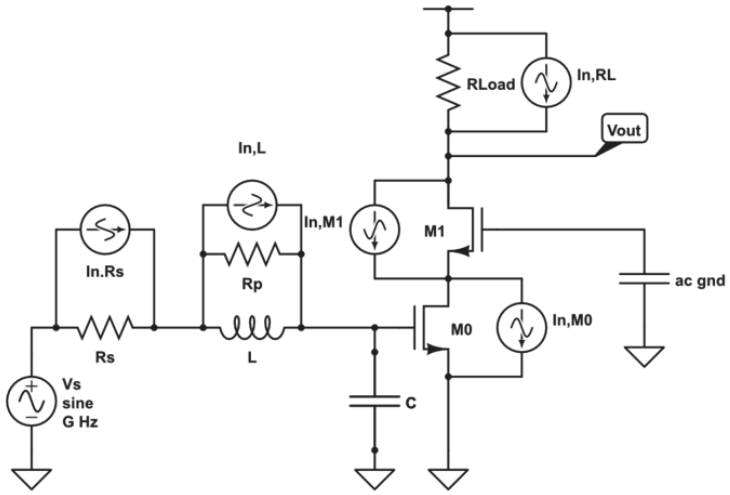

Figure 2.17 Simplified Noise Circuit of Cascode Amplifier

The noise current $i_{n,M1}$ generated by M_1 causes a voltage drop at its drain, the output terminal, of $-i_{n,M1}R_L$. The noise current is also injected into the source, and develops a source-gate voltage of $i_{n,M1}(1/g_{m,1})$, when $r_{o,M0}$ is sufficiently large. This voltage is amplified to the drain as $i_{n,M1}(1/g_{m,1})g_{m,1}R_L$, due to its common-gate (CG) configuration. This effectively cancels the thermal noise current generated by M_1. The resulting noise figure for this LNA is:

$$F = 1 + \frac{\omega_o L}{Q R_s} + \left(\omega_o C R_s + \frac{1}{Q}\right)^2 \left[\frac{\frac{2}{3}}{R_s g_{m,o}} + \frac{1}{R_s R_L (g_{m,o})^2}\right] \quad (2.31)$$

It can be seen that the NF expressed for this LNA in (2.31) is identical to the NF of the LC impedance-matched CS LNA, whose NF is expressed in (2.29). This is because the channel noise generated by M_1 is cancelled, due to the cascode configuration. In the case where $\omega_o C R_s$ approaches zero and Q approaches infinity, the theoretical NF for this LNA is 0 dB.

This circuit is an important circuit technique because high-frequency receivers often suffer from the Miller effect, and rely upon the cascode configuration to implement amplifying stages. Since the noise due to the cascode transistor M_1 is cancelled completely when matched to M_0, this technique can be used in a wide variety of designs.

Active Coupling

Figure 2.18 depicts the noise model for a simple LNA employing the use of active coupling g_m-boosting [8]:

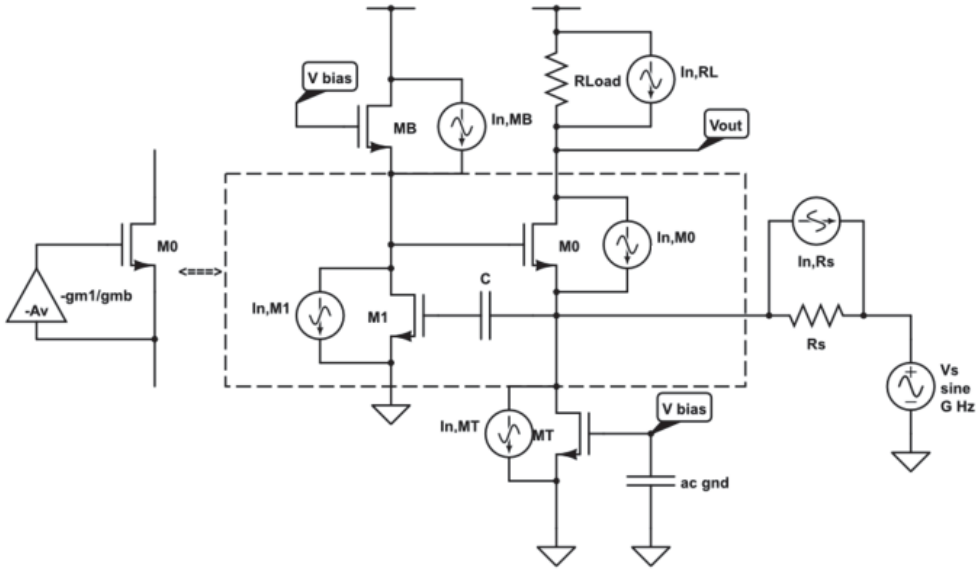

Figure 2.18 Simplified Noise Circuit of Active Coupled LNA

This LNA matches the input impedance via the source termination mechanism, using M_0, which is in common-gate (CG) configuration relative to V_s. M_T provides the bias current. The input signal is also fed to the gate of M_1, which is in a CS configuration. It can be seen in the figure above an amplified and inverted version of the input signal appears on the gate of M_0. When viewed from M_1's output, M_0 is in a CS configuration as well. Due to this active coupling, the effective transconductance of M_0 becomes $g_{m,0}(1+g_{m,1}/g_{m,B})$, while matching the impedances between the LNA and the signal source through M_0. Note that M_1's transconductance need not be equal to that of M_0.

The input impedance of this LNA is approximately $1/(2g_{m,0})$ when $(g_{m,1}/g_{m,B})$ is equal to one, due to the g_m-boosting employed through FETs M_1 and M_B. For impedance-matching, the transconductance of M_0 is set so that $1/(2g_{m,0}) = R_s$. This LNA has a gain of $g_{m,0}R_L$ with respect to the source V_s. Assuming $g_{m,0}R_s = (1/2)$ and $g_{m,1} = g_{m,B}$, the noise figure for this particular LNA is expressed as:

$$F = \left(1+\frac{1}{3}\right) + 2\left[\frac{g_{m,T}}{g_{m,0}} + \frac{\frac{4}{9}}{R_s g_{m,B}} + \frac{1}{g_{m,0}R_L}\right] \qquad (2.32)$$

Due to the active coupling, the noise figure contribution due to the input FET M_0 is only $(1/3)$, whereas in non-g_m-boosted applications source-termination results in NF contribution of $(2/3)$. However, (2.32) also shows that the NF contributions of all the other noise sources (besides that of R_s) are double what they would be without the g_m-boosting circuitry. In the case where $g_{m,0}R_L >> 2$ and $g_{m,1} = g_{m,B}$, the minimum theoretical NF is $4/3$, or 1.25 dB.

Reactive Designs

Common-Source Amplifier with Tuned Load

A common technique to achieve high gain and high output voltage-swing, while decreasing the noise contribution due to the load impedance, is to use a tank circuit as the load in a CS amplifier. As seen above, noise contributions due to capacitors and inductors (of high Q)

are negligible when compared to contributions due to resistors and active devices. Not only this, but since the impedance of an ideal inductor is 0Ω at dc, no biasing voltage is dropped over the tank circuit. Because a high quality tank stores its own energy, in the form of electric and magnetic field oscillations, the output voltage is actually able to swing higher than the supply voltage, without distorting the signal. Also, the tank is lossless, as there is no power lost to heat by these reactive devices. Indeed, using a tuned load is a wise approach to the design of any narrowband LNA. The noise model for a simple CS tuned load LNA is shown below:

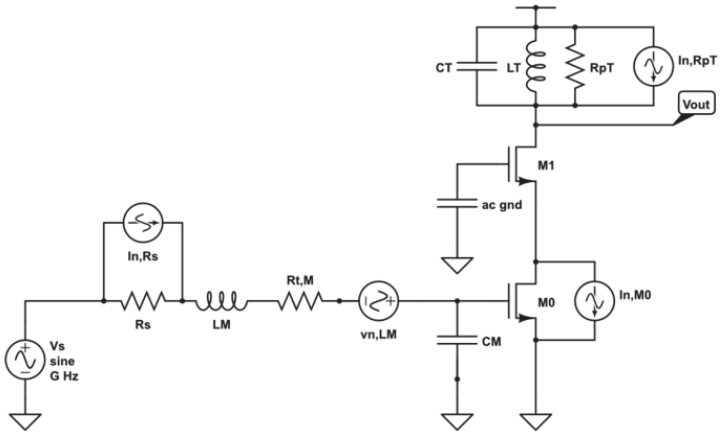

Figure 2.19 Simplified Noise Circuit of CS Tuned Load LNA

In the circuit of Figure 2.19, L_M and C_M implement the impedance matching. L_T and C_T compose the tank load. In the tank load, the noise current is attributed to the parallel equivalent resistance of the inductor L_T, where:

$$R_{p,T} = Q_T \omega_o L_T \tag{2.34}$$

The noise contribution due to (2.34) is inversely proportional to $(Q_T)^2$, whereas the noise contribution due to a resistive load has an effective Q of one. The noise figure for this LNA can be expressed as:

$$F = 1 + \frac{\omega_o L_M}{Q_M R_s} + \frac{\left(\omega_o C_M R_s + \frac{1}{Q_M}\right)^2}{R_s g_{m,o}} \left[\frac{2}{3} + \frac{1}{Q_T^2 g_{m,o} Q_T \omega_o L_T}\right] \tag{2.35}$$

The last term in (2.35) is due to the tuned load circuitry. As the quality factor of L_T increases, less noise voltage is generated, which is approximated as $\sqrt{(4kTB\omega_o L_T (Q_T)^{-1})}$. The $(\omega_o C_M R_S + 1/Q_M)$ term in the expression of (2.35) is the inverse of the quality factor of the input RLC network, and is designed to be much less than one at ω_o. This, along with assuming an infinite quality factors Q_M and Q_T, implies a theoretical minimum noise figure for this LNA of 0 dB at an input frequency of ω_o, regardless of the transconductance of M_0. This is because of the high gain associated with this type of reactive matching network, as well as the low-noise load. However, using a large transconductance value for the FETs M_0 and M_1 can further optimize the noise figure of this LNA in the case of finite Q factors.

Source-Inductor (S-L) Amplifier

The S-L amplifier is a heavily researched LNA, and is a great choice for narrowband receivers. It uses an inductor to resonate with the capacitance of an input FET, by placing the inductor in its source terminal. And by selecting the proper g_m for the FET, a real input impedance of arbitrary value can be generated. To understand this, refer to the following figure:

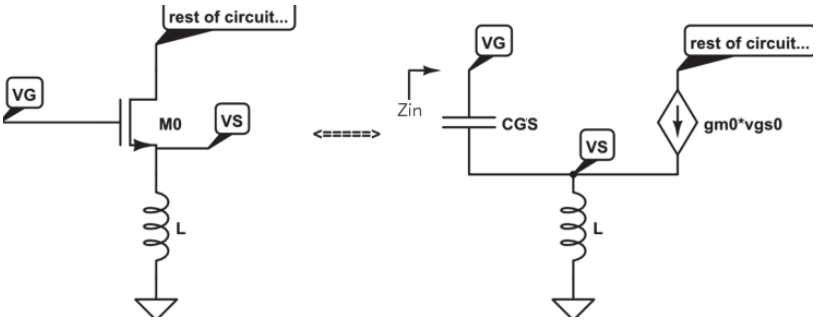

Figure 2.20 Input Impedance of FET with Source Inductance

For the network illustrated in Figure 2.20, it can be shown that Z_{in}, which is the complex impedance between the gate terminal and ground, is:

$$Z_{in} = j\left(\omega L - \frac{1}{\omega C_{gs}}\right) + \frac{g_{m,o}L}{C_{gs}} \tag{2.36}$$

Choosing an inductance value that resonates with the gate-source capacitance of the input FET sets the imaginary part of (2.36) equal to zero. Then, Z_{in} becomes:

$$Z_{in}|_{(\omega=\omega_o)} = \frac{g_{m,o}L}{C_{gs}} \tag{2.37}$$

which is a real value, implying resistive-only impedance at the LNA's operating frequency. Properly biasing the FET allows for matching to any arbitrary source resistance, through the control of its transconductance in conjunction with its aspect ratio that sets C_{gs}, and hence L.

The source-inductor technique for impedance matching, along with a tuned load impedance, can be used to implement a narrowband LNA with an impressive theoretical-minimum noise figure. The S-L LNA is a reliable topology that offers NFs as low as 1.2 dB [9]. Figure 2.21 shows the noise model for a simple S-L LNA.

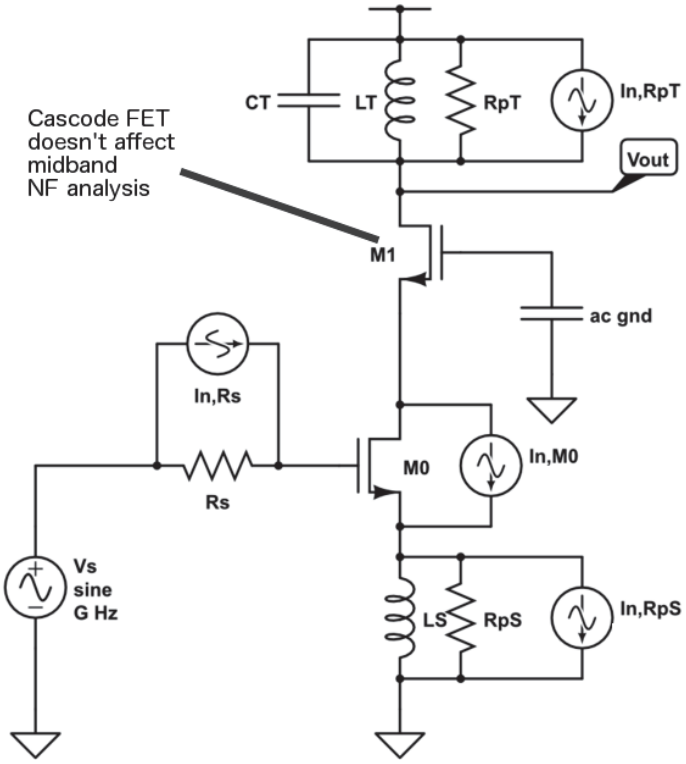

Figure 2.21 Simplified Noise Circuit of S-L LNA

A brief description of the noise cancelling mechanisms introduced by the source inductance is offered here: the inductor L_s, resonating with the internal gate-source capacitance in M_0, creates a high-impedance node at M_0's source terminal for signals of high frequency. Noise generated by M_0's channel can be modeled as thermal noise current being injected into the source terminal, coming out of the drain terminal. The high impedance at the source node established by L_s in parallel with C_{gs} causes the ac current to be dropped across the capacitance C_{gs} of the FET M_0. This causes a negative ac voltage drop across its gate-source junction, which in turn causes a decrease in the ac drain current, $g_{m0}v_{gs0}$. In this fashion, noise voltage (due exclusively to M_0 channel noise) at the drain of M_0 is effectively cancelled. This technique is essentially a narrowband implementation of *source degeneration.*

The noise figure for this LNA is:

$$F = 1 + \frac{(\omega_o C_{gs})^2\left[\left(R_s+\frac{\omega_o L_S}{Q_S}\right)^2+\left(\frac{R_s}{Q_S}\right)^2\right]\left[\sqrt{\left(2+\frac{\omega_o L_S}{R_s Q_S}\right)^2+\left(\frac{1}{Q_S}\right)^2}\right]}{g_{m,0}^2 R_s}\left[\frac{2}{3}g_{m,0}+\frac{1}{Q_S\omega_o L_S}+\frac{4}{Q_T^2(Q_T\omega_o L_T)}\right] \quad (2.38)$$

Observation of (2.38) implies that the noise figure has a dependence on the inverse square of the quality factors of the resonant circuits. In the case where Q_S approaches infinity, the added NF contribution is proportional to $(\omega_o C_{gs} R_s)^2$, which is the inverse of the quality factor of the input RLC network. However, this NF contribution is also proportional to $2/((g_{m,0})^2 R_s)$, an artifact of the fact that the LNA now presents a voltage divider of one half at its input. The choice of g_{m0} is dependent on the value of R_s, and must be sized appropriately for a proper match with the signal source to have the NF of (2.38). Later, in Chapter 4, the theory of operation and NF analysis for this LNA are further detailed. Also, expressions for voltage gain, Q-based input and output impedances, and maximum input power levels are derived.

2.2.3 Active Noise Cancelling Techniques

Active Noise Cancelling LNAs minimize the noise figure by actively cancelling the noise generated by the FETs in the circuit itself. Often, these noise-cancelling architectures also perform impedance matching or g_m-boosting. The two ANC LNAs presented in this document

are the (i) Common Gate – Common Source (CG-CS) LNA [6], and the (ii) Cross-Coupled (CC) LNA [14].

Common Gate – Common Source (CG-CS) LNA

To understand the operation of a CG-CS LNA, refer to the following figure, which is a noise model of a simple CG-CS LNA:

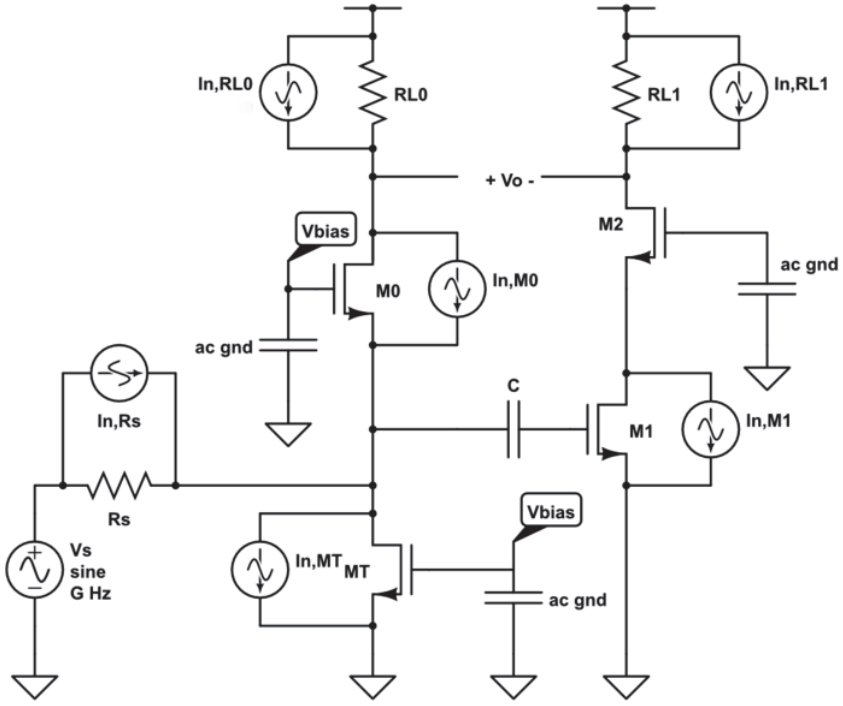

Figure 2.22 Simplified Noise Circuit CG-CS LNA

In the circuit of Figure 2.22, M_0 establishes the input impedance as $(g_{m0})^{-1}$, due to its source termination configuration. The output impedance of the tail FET M_T, as well as the reactance due to the gate of M_1, appear in parallel with $(g_{m0})^{-1}$, but are assumed to be of such high value that they are negligible when calculating the LNA's input impedance.

Single-ended to differential conversion is achieved by ac coupling the input signal, which is originally fed into the source terminal of M_0, to the gate of M_1, which is in a CS amplifier

configuration. Conversely, M_0 is in a CG configuration. If $g_{m0} = g_{m1}$ and $R_{L0} = R_{L1}$, then the output (taken differentially between the drains of M_0 and M_1) voltage due to some V_s is:

$$V_{out,diff} = \tfrac{1}{2}V_s(2g_mR_L) \tag{2.39}$$

And the voltage gain is:

$$A = \frac{V_{out,diff}}{V_s} = g_mR_L \tag{2.40}$$

In addition to single-ended-to-differential signal conversion, M_0's channel noise is fully cancelled. M_0's thermal noise current is injected *out* of the drain terminal (causing a negative voltage drop at the positive output terminal) and *into* the source terminal. This current injection to the input node of the LNA is amplified to the drain of M_0, as a positive voltage. When components are selected properly, the voltage at the drain due to the current injection into its source cancels one half of the noise voltage. The voltage at the positive output terminal due to these mechanisms results in:

$$V_{n,(+)} = -i_{n,m0}R_{L0} + \tfrac{1}{2}\frac{i_{n,m0}}{g_{m0}}g_{m0}R_{L0} = -\tfrac{1}{2}g_{m0}R_{L0} \tag{2.41}$$

The other half of the noise voltage due to M_0 is cancelled using M_1. The aforementioned source voltage at the LNA's input due to the channel noise of M_0 is also amplified by M_1, and appears at the negative output terminal. The voltage at the drain of M_1 due to the thermal noise of M_0 is:

$$V_{n,(-)} = -\tfrac{1}{2}\frac{i_{n,m0}}{g_{m0}}g_{m1}R_{L1} = -\tfrac{1}{2}g_{m0}R_{L0} \tag{2.42}$$

when perfect matching is assumed. Since the output is taken differentially, the total output noise voltage due to the channel noise of M_0 becomes:

$$V_{out} = V_+ - V_- = -\tfrac{1}{2}g_{m0}R_{L0} - (-\tfrac{1}{2}g_{m0}R_{L0}) = 0\ V \tag{2.43}$$

which implies full noise-cancellation of the thermal noise induced in the channel of M_0. For the full amplifier, only partial noise cancellation takes place, since M_1 has no similar feedback mechanism.

The noise figure for this LNA is:

$$F = \left(1 + \frac{2}{3}\right) + R_s\left[\frac{2}{3} g_{m,T} + \frac{1}{2R_L}\right] \tag{2.44}$$

The factor of ⅔ is due to the non-cancelled noise of M_1, which is matched to the FET providing the source-termination, M_0. From inspection of (2.44), an approach to minimizing the noise figure of this particular LNA would be to minimize the transconductance of the tail FET, M_T. The minimum theoretical NF produced by (2.44) is 2.2 dB.

Cross-Coupled (CC) LNA

The CC LNA is a fully differential common-gate amplifier that uses cross-coupling between a pair of amplifying transistors to fully cancel their thermal noise contributions. The coupling is done between the gate of one FET in the differential pair, and the source of the other. Figure 2.23 shows a noise model of a simple CC LNA, adapted from the capacitor cross-coupled common-gate LNA of [14]:

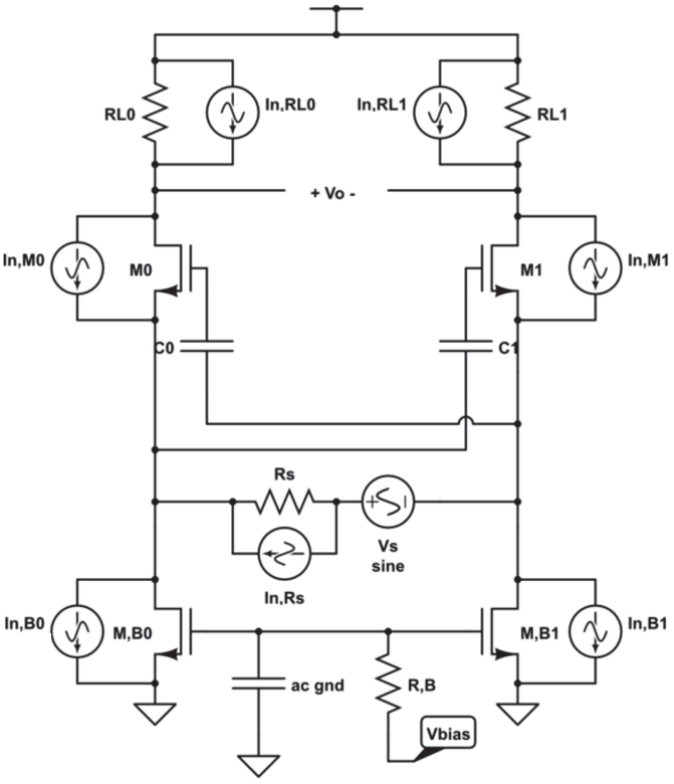

Figure 2.23 Simplified Noise Circuit CC LNA

Similar to the situation for the CG-CS LNA, half of the channel noise due to M_0 is cancelled due to its source-termination/common-gate configuration. The other half is cancelled by inverting and amplifying the noise voltage at the source of M_0, using M_1 in a common-source configuration, and then taking the output differentially. This is achieved using the cross-coupling capacitors C_0 and C_1, which act as bypass capacitors. M_1's configuration mirrors that of M_0, and its contribution to the output noise voltage is cancelled in an identical manner. Also, by providing an ac ground at the gate of the current sourcing FETs $M_{B,0}$ and $M_{B,1}$, the thermal noise contribution of R_B will not appear at the output. In this first-order anlaysis, the only noise sources that remain in this circuit are the source impedance R_s, the channel noise of the current source FETs, and the load impedances R_{L0} and R_{L1}. Assuming ideal matching between components, the noise figure for this LNA is expressed as:

$$F = 1 + \frac{4}{3}\left(\frac{g_{m,B}}{g_{m,0}}\right) + \frac{1}{g_{m,0}R_{L,0}} \tag{2.45}$$

When $g_{m,0}R_{L0} >> 1$, the dominant noise sources in this LNA are the current sourcing FETs, $M_{B,0}$ and $M_{B,1}$. Therefore, minimizing the ratio of their transconductance to that of the amplifying FETs optimizes the NF of (2.45). In the case where they are equal, the minimum theoretical NF is 3.67 dB. Therefore, the noise performance of this LNA would improve by fully or partially cancelling the noise due to these transistors. One method of decreasing the NF of (2.45) is to replace $M_{B,0}$ and $M_{B,1}$ with inductors that appear as high-impedance nodes at the operating frequencies, which is employed in [14]. Then the noise power contribution of the current source inductors becomes inversely proportional to the square of their quality factors, which are typically much greater than one. In [14], a NF of 2.97 dB at 6 GHz is reported.

Differential Partial Noise Cancelling LNA

This thesis documents the analysis, design, and simulation of a narrowband Partial Noise Cancelling (PNC) LNA. Adapted originally from the wideband implementation of [1], this PNC LNA uses NFET/PFET composite pairs and multiple-feedback paths in order to largely cancel

noise contributions from all the FETs in the circuit. The schematic for the PNC LNA designed and simulated in this thesis is shown in Figure 2.24.

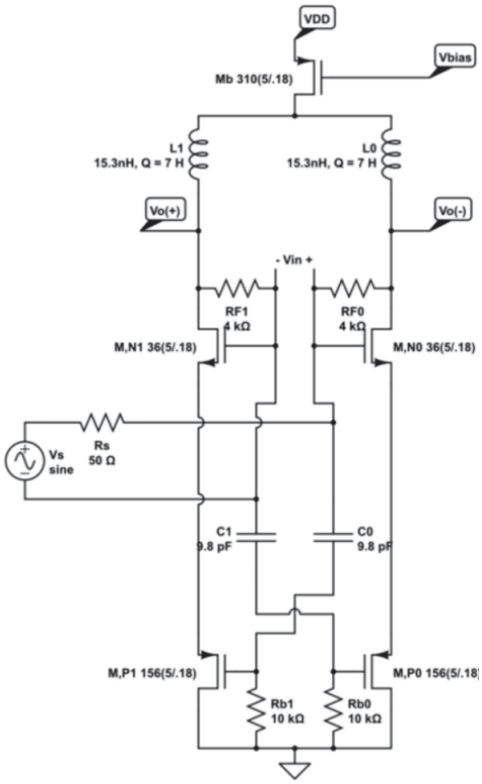

Figure 2.24 Schematic of narrowband PNC LNA

For the PNC LNA of Figure 2.24, the input FETs $M_{N,0}$ and $M_{N,1}$ are a differential pair of common-source configuration that each employ shunt-shunt feedback using resistors $R_{F,0}$ and $R_{F,1}$, as well as source-degeneration, via the pFETs $M_{P,0}$ and $M_{P,1}$. When the transconductances of all FETs are equal, half of the thermal noise contribution due to each nFET is cancelled because of the source-degeneration impedance of $(1/g_m)$. The other half is cancelled by cross-coupling the gates of the nFETs, which are provided output feedback, to the gates of the pFETs, which are in common-drain configurations. When all transconductances are equal, the voltage on the source of each pFET is half of its gate voltage. Using the corresponding nFET, which now appears as a CG amplifier to the signal at the pFET's source, the other half of the input

nFET's thermal noise is cancelled, since the output is taken differentially. However, since there is feedback back to the half-circuit from which the noise is generated, a small portion of the noise remains, hence the "partial" noise cancellation. The noise is due to the pFETs is partially cancelled in a similar manner. The reactive components compose a bandpass filter at the output that provide resonance at the frequency of operation and reject out-of-band signals. For proper operation, the parallel-equivalent impedance of the output filter should be much greater than R_F, in order for the current feedback mechanism to function. When the feedback resistance R_F is much greater than R_S, the minimum theoretical NF for the LNA of Figure 2.24 is .03 dB. The theory of operation, including NF analysis, is detailed in Chapter 4. For this PNC LNA, simulations report a NF of 1.76 dB while consuming 15 mW of dc power from a 1.8V supply.

2.3 LNA Large-Signal Performance

While noise figure is one of the most important figures of merit for an LNA, good receiver performance is also contingent on proper "large-signal" processing capabilities. "Large-signal" refers to received signals of sufficient power to cause the LNA circuitry to approach "compression" of the output signal. "Compression" refers to a decrease in the LNA power gain, which can directly lead to amplitude distortion and intermodulation distortion [15]. The metrics by which large-signal performance is characterized are based upon (i) the input power level that causes compression of the output, (ii) its "1dB Dynamic Range" (1dBDR), and lastly (iii) the 3rd Order Input and Output Intercept Points (IIP3 and OIP3).

2.3.1 Compression of LNAs

Due to real-world limitations set by power consumption and small-signal gain, the power gain of a LNA does not stay linear at large input power levels. As input power increases, the gain vs. input power of a LNA "rolls off" and significantly deviates from its ideally constant value. This phenomenon is known as "compression", and results from non-linear responses of the active devices along the signal path.

There are two main points where compression is possible. The first is the LNA's input node, where a strong enough signal can cause amplifying transistors to operate outside of their active regions, and at the output node, where the voltage can attempt to exceed the power supply voltage, or drop low enough to move the transistor out of the active region and into triode behavior. In both cases, amplitude distortion occurs. Figure 2.25 illustrates how these mechanisms affect LNA signal processing:

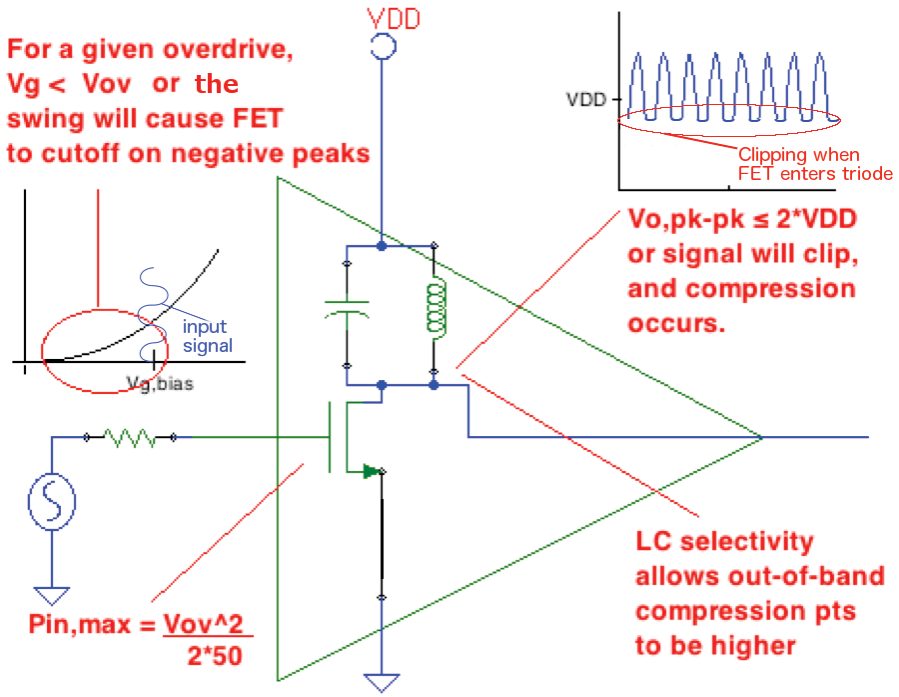

Figure 2.25 Input-Referred and Output-Referred Compression

Figure 2.25 above illustrates the ways compression can occur, at either the input or the output of the LNA. The peak voltage of the signal at the gate of the FET can't be greater than the overdrive voltage, or the device will enter cutoff. Therefore, for distortionless amplification, the input signal voltage is limited to:

$$V_{in,max} = V_{ov} \tag{2.46}$$

At input voltage levels above (2.46), compression at the input of the LNA occurs.

At the output, the signal voltage is limited by the supply voltage. For the LNA of Figure 2.25, the maximum distortionless output voltage is approximately:

$$V_{o,max} = VDD \tag{2.47}$$

So that the maximum output power without causing the LNA to compress is:

$$P_{o,max} = \frac{VDD^2}{2R_L} \tag{2.48}$$

The power levels at which compression causes the LNA gain to fall by 1 *dB* is referred to as $P_{c,i}$ and $P_{c,o}$: the input and output 1 dB compression point, respectively. $P_{c,o}$ is typically some fraction of the dc power consumption, between 0.01 and 0.5.

Compression due to these mechanisms can also occur because of *out-of-band* signals. In-band signals are of the same frequency as the operating frequency of a LNA, and out-of-band signals are of frequencies that are not within the passband of a narrowband LNA. For a wideband LNA, out-of-band signals refer to signals outside of the receiver's operating channel bandwidth. Proper LNA design requires that out-of-band compression point be insignificant when compared to the input compression point, which is attainable through proper filtering throughout the receiver frontend.

2.3.2 One-dB Dynamic Range

The 1dBDR of an LNA is the range of input signal power levels that experience less than 1 *dB* of compression while remaining above the sensitivity level, or noise floor. Mathematically, it is the difference between the "Sensitivity" power level and the input-referred 1 dB compression point, $P_{c,i}$. The sensitivity of a radio receiver refers to the lowest possible input power level that can be demodulated by the receiver in a reasonably error-free manner. In *dBm*, the sensitivity of a receiver system in a room temperature environment can be written mathematically as:

$$Sensitivity = \left(-174 + 10\log[B] + NF + \frac{C}{N_{min}}\right) dB_m \tag{2.49}$$

where B is the bandwidth of the received signal, NF is the noise figure of the receiver system in dB, C/N_{min} is the minimum signal-to-noise ratio required by the demodulator, and $-174\ dB_m$ represents the noise floor that exists at standard operating temperature, 290 ºK. The expression in (2.46) represents the "input-referred noise floor" of the overall receiver system, which is useful in determining the 1dBDR. The 1dBDR is:

$$1dBDR = [P_{c,i} - Sensitivity]\ dB \tag{2.50}$$

2.3.3 Third Order Input and Output Intercept Points

The IIP3 and OIP3 describe the input and output signal power levels where the distortion caused by spurious intermodulator emissions, a.k.a. IM products, are equal to the power level of the originally desired signal. This causes significant distortion that is a problem in places with very active spectrum environments, such as suburban locations. Typically, the IIP3 and OIP3 are 10 to 15 dB above the $P_{c,i}$ and $P_{c,o}$, respectively.

Chapter 3 - Frequency Dividers

3.1 Detailed Theory of Operation

3.1.1 Injection Locked Frequency Dividers

As explained in Chapter 2, ILFDs operate by synchronizing an oscillator to half the frequency of an injected signal. "Halving" the frequency of the injected signal is accomplished by mixing it with the output of the oscillator, and is described in detail in Section 2.1. This section details the conditions for locking and summarizes the reduction in oscillator phase noise relative to the free-running oscillator's noise spectrum.

Injection Locking

Injection locking works by changing the oscillation frequency of an already free-running oscillator by injecting signal energy directly into the resonator. The "free-running frequency" of the oscillator is denoted as ω_o, and for a tank circuit is given as:

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3.1}$$

Under certain conditions, the output of the oscillator can become synchronized, in frequency and phase, to the injected signal. When this happens, "locking" between the injected signal and the oscillator's output signal is said to have occurred. In order to explain this phenomenon, the derivation of the condition required for synchronization will be summarized, as adapted from the 1946 publication *"A Study of Locking Phenomena in Oscillators"* by Robert Adler [11].

An oscillator with a tuned load can be modeled as a tank circuit (composed of an inductor, capacitor, and an equivalent parallel resistance based on the quality factor of the inductor) in parallel with a negative admittance. Figure 3.1 shows a generic schematic of such a model. The effective quality factor Q of the full circuit is infinite, since any loss in power due to R_p is added back into the tank by the negative admittance, thus sustaining resonance indefinitely.

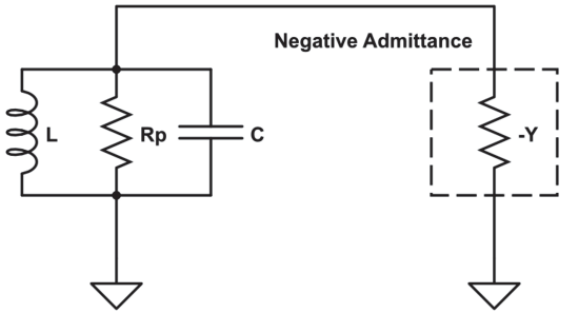

Figure 3.1 Model of Active Oscillator (after Adler)

If a current signal of frequency ω_{inj} is injected into the tank circuit, the voltage that develops due to the injection is the instantaneous output signal (of frequency ω) frequency-modulated with the arising beat note, $\Delta\omega$, as long as the following condition holds true:

$$\frac{\omega_o}{2Q_L} >> \Delta\omega_o \tag{3.2}$$

where Q_L is the quality factor of the inductor in its passive state. The beat notes $\Delta\omega$ and $\Delta\omega_o$ are defined as:

$$\Delta\omega = \omega - \omega_{inj} \tag{3.3}$$

$$\Delta\omega_o = \omega_o - \omega_{inj} \tag{3.4}$$

The condition of (3.2) implies that the injected signal should be close to the free-running oscillation frequency, and that a smaller value of Q_L corresponds to a wider locking range. Expressions (3.3) and (3.4) represent the frequencies of the beat notes that arise when an oscillator undergoing injecting is not yet locked. Expression (3.4) represents the situation where the instantaneous frequency of oscillation is the free-running frequency. According to [11], the spectrum of a non-synchronized oscillator undergoing injections contains ω_o and ω_{inj}, which produce the beat frequency of (3.4). Adler also reports that in reality, a lower *average* beat note is observed, such that the frequency of oscillation over one cycle shifts toward ω_{inj}. Lastly, Adler writes "we may think of ω as of a signal which is frequency modulated with the beat note $\Delta\omega$..." and also gives a phasor diagram used to represent phase and frequency of the

instantaneous beat note of (3.3) relative to the instantaneous output oscillation of frequency ω, and the injection signal of frequency ω_{inj}, which is shown in Figure 3.2. Any vector at rest represents a signal of frequency ω_{inj}. Relative to ω_{inj}, any rotating vector represents the angular beat frequency of (3.3).

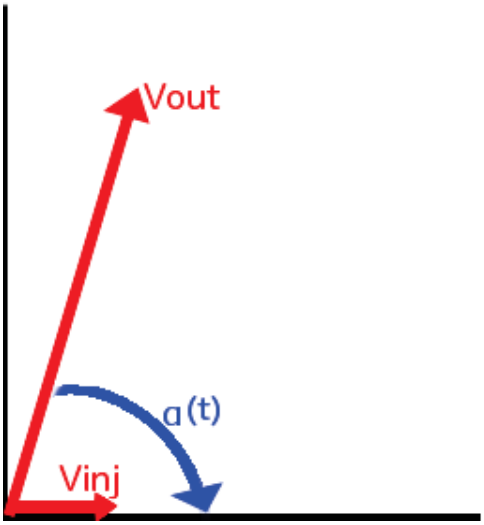

Figure 3.2 Phasor Diagram of Output Signal and Injection Signal (after Adler)

For the case where:

$$V_{inj} << V_{out} \tag{3.5}$$

the phase difference at any given time between the injection signal and the oscillator's output may be approximated as:

$$\phi = -\left(\frac{V_{inj}}{V_{out}}\right) sin(\alpha) \tag{3.6}$$

In [11], Adler explains that the oscillation voltage V_{out}, which is fed back into the mixer of Figure 2.2, is out of phase with the injection signal V_{inj}, and concludes that the instantaneous oscillation frequency exceeds ω_o "by an amount which will produce a lag equal to ϕ" relative to ω_o. Therefore, for a synchronized oscillator, the steady-state oscillation frequency is out of phase with the injection signal by a constant value that is dependent on the phase versus frequency relationship of a given resonator. Based on the phase versus frequency characteristic

of an LC tank circuit, Figure 3.3 is a plot of the phase difference between the injection signal and the steady-state oscillations versus the frequency of the injection signal. Using the linear portion of this curve, Adler derives the conditions necessary for injection locking.

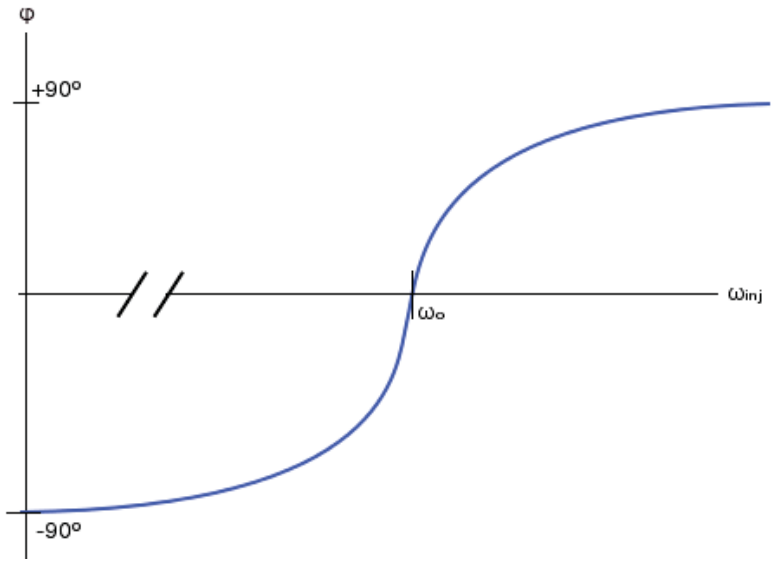

Figure 3.3 Phase between Input and Output Signals vs Injection Frequency (after Adler)

The curve in the plot of Figure 3.3 is centered on the fundamental frequency of the tank circuit, ω_o. For frequencies that are in the linear region of the above curve, the following term is defined [11]:

$$A = \frac{\partial \phi}{\partial t} = \frac{\partial \phi}{\Delta \omega_o} \tag{3.7}$$

so that:

$$\phi = A(\omega - \omega_o) \tag{3.8}$$

which is equivalent to:

$$\phi = A(\Delta\omega - \Delta\omega_o) \tag{3.9}$$

Setting the expressions (3.6) and (3.9) equal to one another, and replacing $\Delta\omega$ with $\partial\alpha/\partial t$, yields:

$$-\left(\frac{V_{inj}}{V_{out}}\right) sin(\alpha) = A[\frac{\partial \alpha}{\partial t} - \Delta\omega_o] \quad (3.10)$$

which is then rearranged for:

$$\frac{\partial \alpha}{\partial t} = -Bsin(\alpha) + \Delta\omega_o \quad (3.11)$$

where *B*, defined by [11] as the speed of the pull-in process, is:

$$B = (V_{inj} / V_{out})A^{-1} \ldots\ldots\ldots (3.12)$$

Using Figure 3.2 as a reference, it can be seen that locking between the oscillator's output and the injected signal will occur when the phase angle between their two corresponding vectors is a constant. Or, locking is contingent upon:

$$\frac{\partial \alpha}{\partial t} = 0 \quad (3.13)$$

Setting (3.12) equal to (3.13), and substituting *A* with $\partial\phi/\Delta\omega_o$ (where $\partial\phi \approx 2Q(\Delta\omega_o/\omega_o)$ for a tank circuit *and* small values of ϕ), reveals:

$$sin(\alpha) = 2Q\left(\frac{V_{out}}{V_{inj}}\right)\left(\frac{\Delta\omega_o}{\omega_o}\right) \quad (3.14)$$

and since $sin(\alpha)$ only assumes values between -1 and +1, the condition for locking is limited to:

$$\left| 2Q\left(\frac{V_{out}}{V_{inj}}\right)\left(\frac{\Delta\omega_o}{\omega_o}\right) \right| < 1 \quad (3.15)$$

which, solved for the ratio of the injected signal to the oscillation voltage, becomes:

$$\frac{V_{inj}}{V_{out}} > 2Q \left| \left(\frac{\Delta\omega_o}{\omega_o}\right) \right| \quad (3.16)$$

The expression of (3.16) gives the locking condition, in terms of injection voltage to output oscillation voltage, for an oscillator with an LC tuned load.

Reduction of Phase Noise

The phase noise of an oscillator is mitigated when under the conditions of injection locking to a low-noise source. Based on the works of [12], the effects on phase noise due to injection locking are summarized here.

The following model is used to analyze the phase noise of oscillator, under the conditions of an injected current at a "near-resonance":

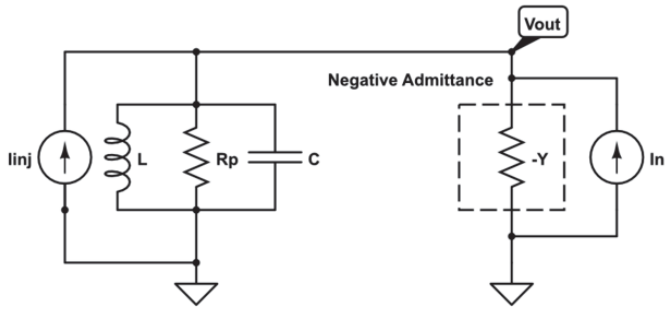

Figure 3.4 Model for Oscillator Phase Noise under Injection Locking (after Razavi)

In Figure 3.4, I_{inj} is the magnitude of the injected current, and I_n is the instantaneous thermal noise current of both the active device providing the negative admittance, and the noise generated in the tank circuit. Therefore, I_n represents the total amount of thermal noise current at the output of the oscillator.

As stated in the preceding section, the net Q of the oscillator is effectively infinite at its resonant frequency. This is because the power losses in R_p are cancelled out by the power generated by the negative resistance circuitry. According to [12], when no injection current is applied to the oscillator, the impedance of the tank circuit becomes the following function of frequency:

$$\left|\frac{V_{out}}{I_n}\right| = \frac{1}{|2(\omega_o - \omega_n)C|} \tag{3.17}$$

(3.17) dictates the noise-shape of the oscillator when no injection signal is applied, and reveals that the output voltage due to the broadband noise current reaches a maximum at ω_o, the resonant frequency of the tank circuit.

When a signal is injected at a frequency of ω_o and of peak current I_{inj}, [12] reports that the magnitude of the negative admittance's transconductance can be expressed as:

$$g_{m,-Y} = \frac{1}{R_p} - \frac{I_{inj}}{V_{env}} \tag{3.18}$$

where V_{env}, equal to $I_{out,pk}R_p$, represents the "envelope" of the output oscillations that arise due to the mixing process explained in the preceding section. Rearranging (3.18) reveals that the effective transconductance of the tank circuit is now:

$$g_{m,eff} = \frac{I_{inj}}{V_{env}} = \frac{1}{R_p} - g_{m,-Y} \tag{3.19}$$

which is the inverse of the impedance of the tank under the condition of an applied injection signal:

$$Z_n|_{\omega=\omega_{inj}} = \frac{V_{env}}{I_{inj}} \tag{3.20}$$

Replacing V_{env} of expression (3.20) with $I_{out,pk}R_p$ gives the following expression of the tank's impedance exclusively for signals within the locking bandwidth:

$$Z_n|_{\omega=\omega_{inj}} = \frac{I_{out,pk}R_p}{I_{inj}} \tag{3.21}$$

For frequencies that are within the locking range of an oscillator, the noise shape is no longer represented by the expression of (3.17), which reaches a maximum at the resonant frequency ω_o, but instead is established by the effective tank impedance, expressed in (3.20) and (3.21). If ω_{inj} falls outside of the locking bandwidth, the oscillator enters free-run operation, and the noise profile is dominated by (3.17). The following figure compares the phase noise when operating in the free-run mode and in injection-locked mode for a generic oscillator. Note the influence of a noisy injection source, representing a practical ILFD.

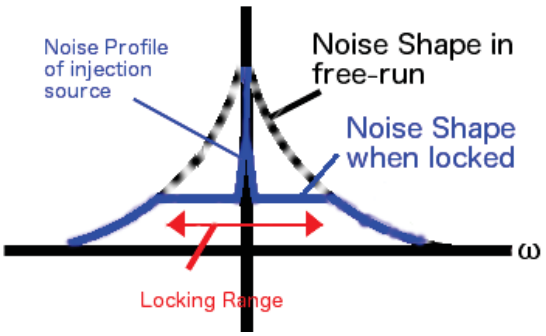

Figure 3.5 Oscillator Phase Noise in Free-Run and Injection-Locked Mode (after Razavi)

3.1.2 Regenerative Frequency Dividers

Regenerative frequency dividers are overviewed in Chapter 2. Figure 2.11 displays the block diagram of an ideal RFD consisting of a mixer, low pass filter (LPF), and an amplifier. A signal is injected into one terminal of the mixer, while a feedback loop consisting of an amplifier followed by a LPF drive the other input. The LPF provides the frequency selectivity and must not attenuate at frequencies that are roughly half of the frequency of the injected signal. In addition to satisfying the Barkhausen criterion for oscillation, the filter's phase must be such that feedback is in-phase. This positive feedback to the amplifier causes it to oscillate when an injected signal is applied, but only frequencies within the passband of the filter are sustained. As noted in Chapter 2, a bandpass filter (that introduces no phase shift) can also be used, especially at higher frequencies to save power. Since the filter's passband is "centered" around half the injected frequency, only these spectral elements can appear at the filter's output, which is then mixed with the injected signal. Because an ideal mixer provides an output signal whose frequency is the sum and different of the two input signals, its output will consists of the following frequencies:

$$\omega = \omega \pm \frac{\omega}{2} \tag{3.17}$$

And due to the LPF (or BPF), only ω - $\omega/2$ survives. In this manner, an RFD is able to lock and halve the frequency of any arbitrary injection signal.

3.2 CMOS Frequency Divider Implementations

3.2.1 Injection Locked Frequency Dividers

In order to directly compare the performance of a Tail-ILFD to a Quench-ILFD, a single oscillator circuit was used to implement both. The oscillator consisted of a cross-coupled negative-resistance oscillator with a tank circuit load. A schematic representing both implementations, using the same core oscillator circuitry, is shown in Figure 3.6. Applying the input signal to one injection FET and not the other enables one to compare their performance

under the same bias conditions and load. When testing with $V_{in,T}$, $V_{in,Q}$ is held high to keep M_Q in cutoff.

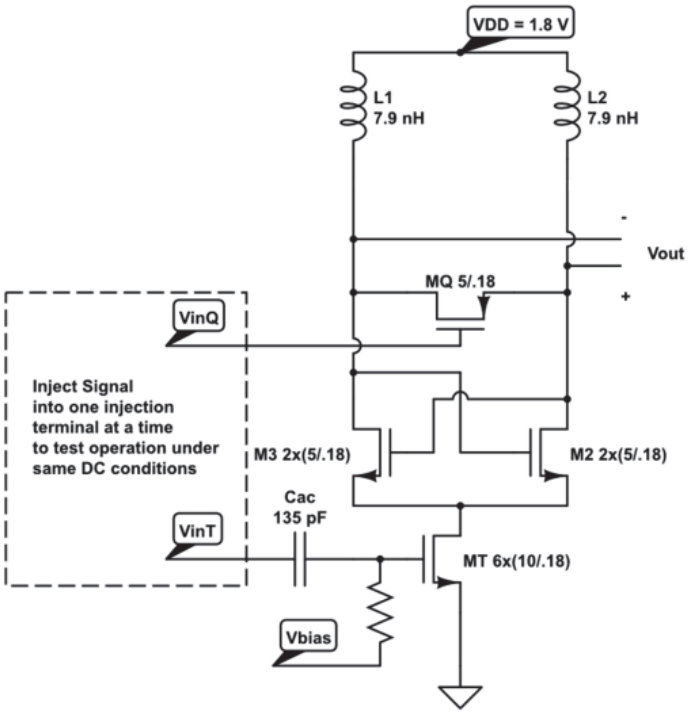

Figure 3.6 Schematic of Tail and Quench-ILFDs using Cadence ICFB

Tail Injection Mode Operation

To implement the Tail-ILFD of Figure 3.6, the injected signal is applied to the gate of M_T through a coupling capacitor, and appears via M_T's transconductance at the source nodes of M_2 and M_3 as a current of:

$$I_{inj} = g_{m,T} v_{gs,T} = g_{m,T} v_{in,T} \tag{3.22}$$

Note that *v* indicates the instantaneous value of a sinusoidal term. Here, $v_{in,T}$ is the injected signal at roughly twice the tank's fundamental frequency, as explained in section 2.1.1. FETs M_2, M_3, and M_T operate as a single-balanced mixer while L_1, L_2, and the net tank capacitance, suppressing the pre-divided injected signal at the mixer's output. The mixer's output terminals are the drains of M_2 and M_3, where the signal here results from superposition of the tank's fundamental oscillations and the voltage drop occurring from the injected current of

(3.22) into the tuned load. For injected current frequencies that satisfy (3.2), the half-circuit impedance of the load can be expressed as:

$$Z_n|_{\omega=\omega_{inj}} = R_p = Q_{L,1}(2\pi f L_1) \tag{3.23}$$

which results in:

$$V_{inj} = I_{inj}R_p = g_{m,T}v_{in,T}Q_{L,1}\left(2\pi\left(\frac{f_{inj}}{2}\right)L_1\right) \tag{3.24}$$

V_{inj} is the instantaneous voltage that is injected into the resonant circuit, as described in Figure 2.2. The frequency f_{inj} (in Hz) is the frequency of the input signal. When the conditions for locking set by (3.16) are met, the tank oscillates at exactly half the frequency of the injected signal source.

Quench Injection Locked Operation

The Quench FET M_Q of Figure 3.6 is placed in between the output terminals, and its gate is driven by the injection signal. In Quench operation, the injected signal is mixed directly with the drains of M_2 and M_3, by switching the impedance of M_Q between ~0Ω and ~ ∞Ω at a frequency that $2\omega_o$, where ω_o is the fundamental frequency of the tuned load. When on, M_Q operates in the triode region, and has a transient impedance of:

$$R_{M,Q} = \left[\mu_p C_{ox}\left(\frac{W}{L}\right)(v_{OV} - v_{DS})\right]^{-1} \tag{3.25}$$

For this type of Quench ILFD, [16] reports the locking range as:

$$\Delta\omega = \frac{I_{inj}}{V_{osc}C} \tag{3.26}$$

where C is the total tank capacitance, and is re-expressed in terms of the quality factor of the tank circuit [16]:

$$\omega\Delta = \frac{I_{inj}}{I_{dc}Q} \tag{3.27}$$

where I_{dc} is the dc current consumption. Lastly, [16] reports the following lock-in condition:

$$V_{inj,min} = \frac{\Delta\omega}{\omega_o L a_2} \tag{3.28}$$

where L is the tank inductance and a_2 is the second-order coefficient of a third-order nonlinear function describing the frequency response of the filter.

In the Quench mode of operation, (3.28) expresses the minimum injection signal voltage that will result in synchronization of the oscillator, for frequencies within the locking. Again, when the conditions for locking set by (3.16) are met, the tank oscillates at exactly half the frequency of the injected signal source.

Figure 3.7 shows the full circuit that was fabricated and measured.

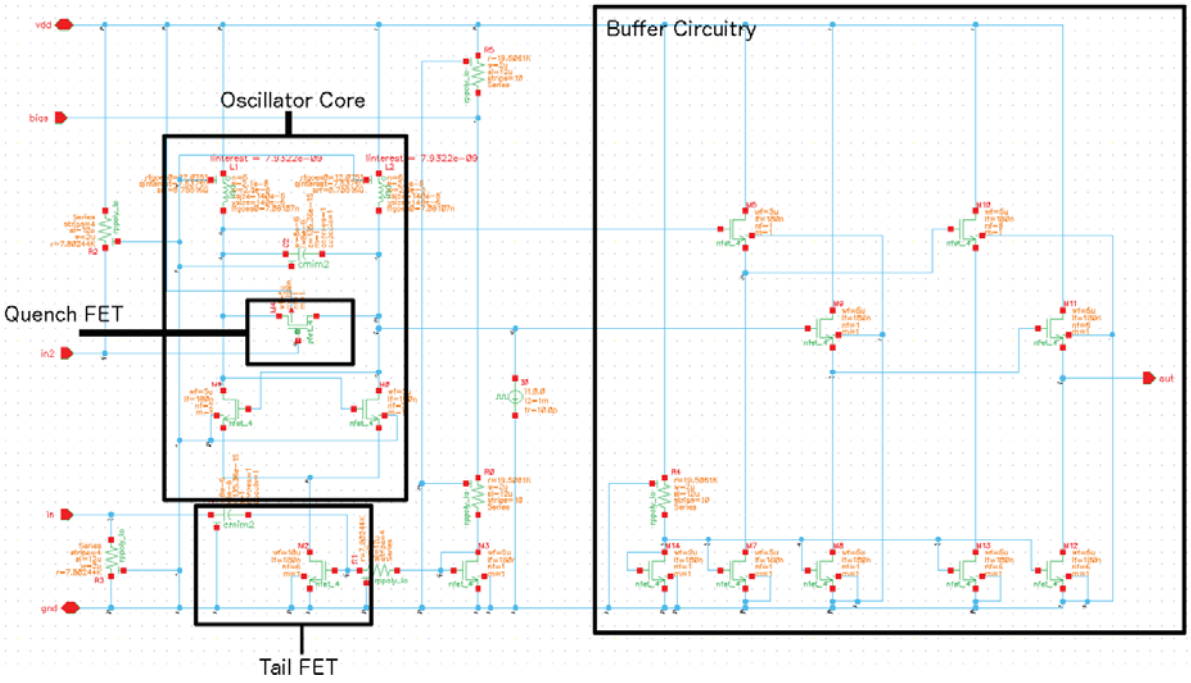

Figure 3.7 Schematic of Tail and Quench-ILFDs

The differential outputs connect to buffers, and only one buffer's output is available. This is sufficient in measuring the tank's output oscillation frequency while a high-frequency injection signal is applied to either M_T or M_Q. The layout is shown in Figure 3.8, annotated to show where probes make contact in order to carry out measurements. The three horizontal contacts that are labeled "Tail Site" and "Quench Site" are Ground-Signal-Ground (GSG) pads

and are used to apply ac signals to the gates of M_T and M_Q, respectively. The contact labeled "Bias Voltage Input" enables the control of overall power consumption of the core oscillator circuitry by changing the dc current through M_T, which also serves at the current supply for the oscillator core. This control mechanism is seen in Figure 3.7 – the bias voltage is applied to the current mirror that biases M_T's drain current. At nominal operation (i.e. Bias Voltage Input pin floating), the consumed dc power is 2.28 mW. The supply voltage *VDD* is 1.8 V and the oscillator core bias current I_{dc} is 1.27mA.

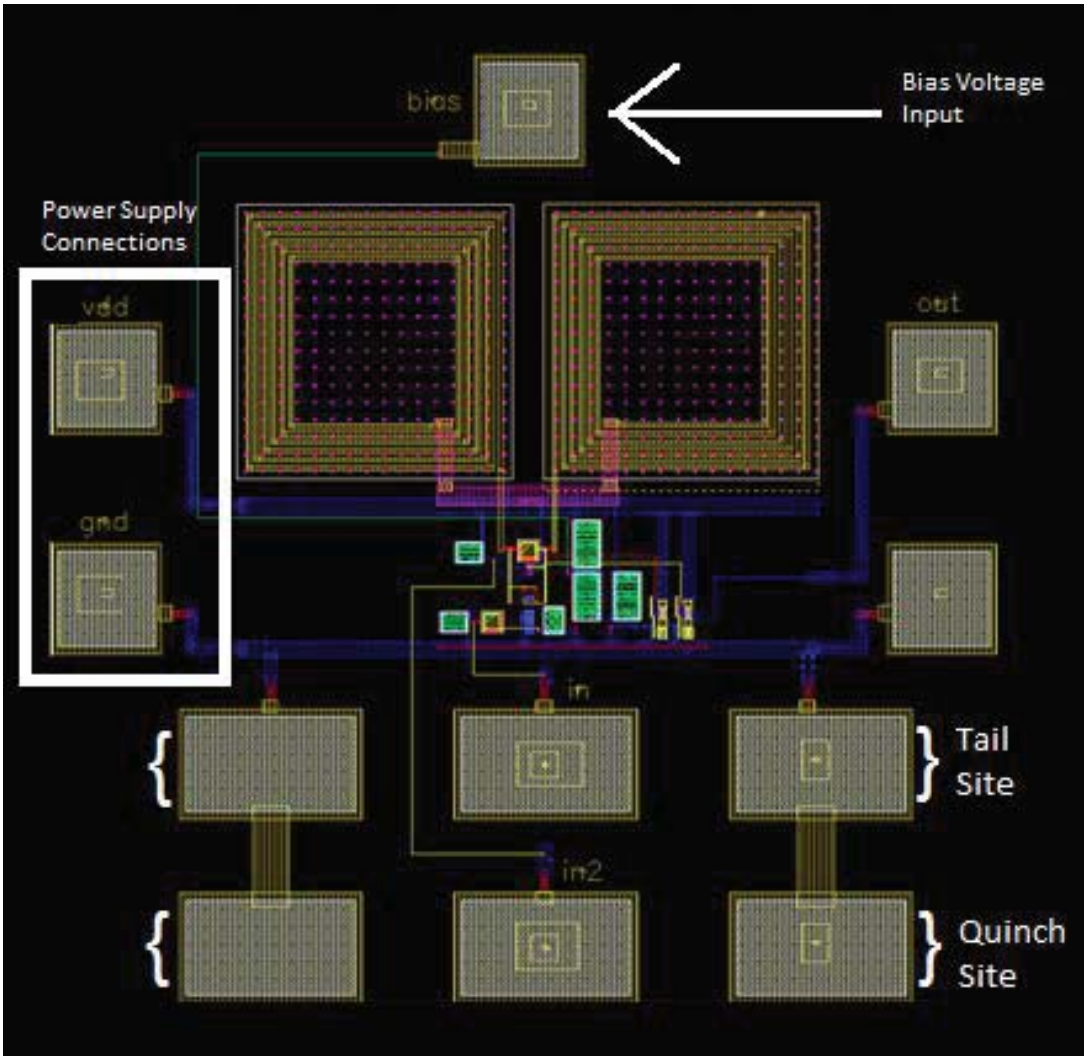

Figure 3.8 Tail and Quench-ILFD CMOS Layout Implementations

3.2.2 Regenerative Frequency Divider

To implement a low-power RFD, a Gilbert Cell mixer with a tuned load was chosen. Figure 3.9 is a simplified schematic representation of the implemented RFD.

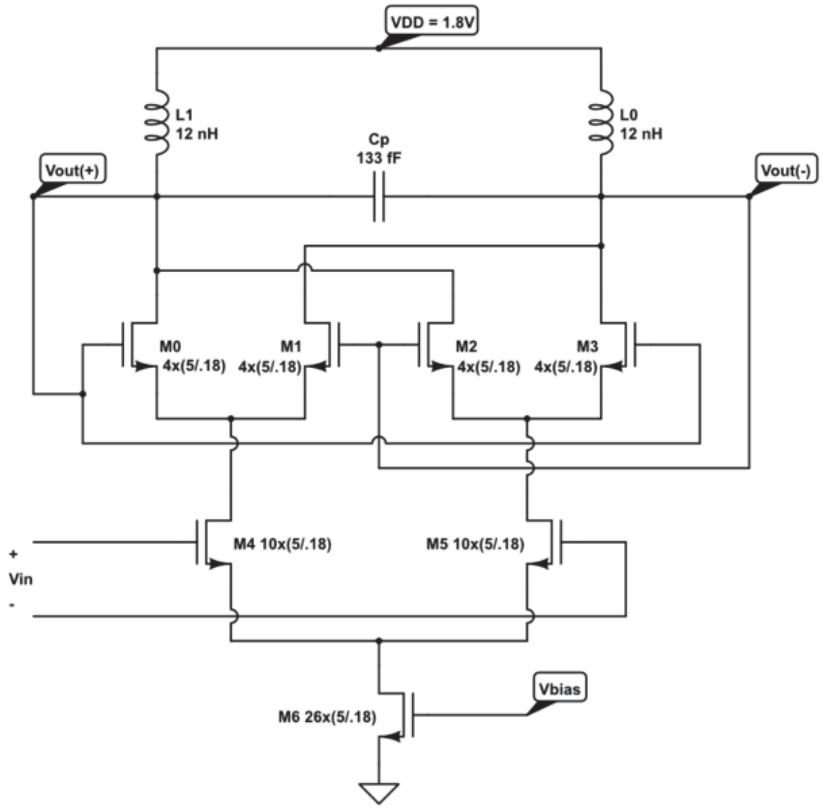

Figure 3.9 Implemented RFD Schematic

The circuit implements the block diagram of an RFD described in Figure 2.11. In the circuit of Figure 3.9, M_6 provides the dc current that drives the Gilbert Cell mixer implemented by FETs M_0 through M_5. FETs M_4 and M_5 are driven by a voltage source of twice the desired output frequency, which is mixed with the output tank oscillations. FETs M_0 through M_3 implement the other input of the mixer represented in Figure 2.11, and are provided feedback by connecting the gates of $M_{1,2}$ and $M_{0,3}$ to the negative output terminal and positive output terminal, respectively. Essentially, FETs M_0 through M_3 cause the transient gain seen by the V_{in}

input terminals to switch between $\pm A_v$, at a frequency dictated by the instantaneous output voltage of the oscillator. The magnitude of A_v is dependent on the frequency of the input signal f_{in}, and is equal to:

$$A_v = g_{m,5} Q_{L,0} 2\pi \left(\frac{fin}{2}\right) L_0 \tag{3.28}$$

A visualization of A_v through time provides a more intuitive understanding of the mixing and amplification within the Gilbert Cell mixer architecture. Observe Figure 3.10:

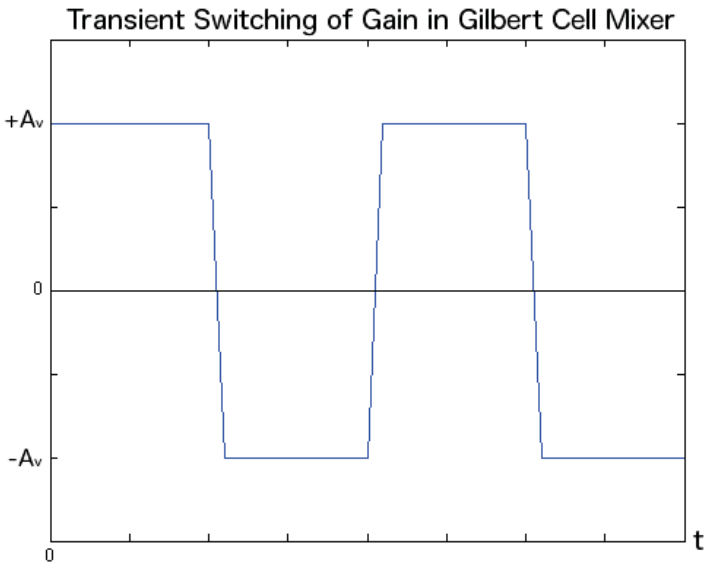

Figure 3.10 Transient Switching of Gain in Gilbert Cell Mixer

Lastly, the tuned load (consisting of L_0, L_1, and C_p) implements the filter of Figure 2.11. No explicit tank capacitance is used. Instead the inherent capacitances of the devices are employed to provide the needed tank capacitor. C_p is twice the parasitic capacitance at each output terminal $C_{p,out(+)}$ and $C_{p,out(-)}$, and for this schematic can be estimated as:

$$C_{p,out(+)} = C_{p,out(-)} \approx C_{G,M0} + C_{G,M3} + C_{DG,M2} + C_{DS,M2} \tag{3.29}$$

Using standard estimations for the terms in (3.29) yields:

$$C_{p,out(+)} = C_{ox} N_{fingers} [W_{M,0} L_{M,0} + W_{M,3} L_{M,3} + \left(\frac{2}{3}\right) W_{M,2} L_{M,2}] \quad (3.30)$$

Where $N_{fingers}$ and *(W*L)* is the same for all of the FETs represented in (3.30). Substituting the terms in (3.29) with the device geometries results in:

$$C_{p,out(+)} = C_{ox}(4)(5 \times .18)(2 + \frac{2}{3}) \approx 77\ fF \quad 3.31)$$

Figures 3.11 and 3.12 show the schematic view and layout view of the RFD as implemented in the CMOS process, respectively. The GSG pads that drive M_4 and M_5 appear at the right and left sides of Figure 3.11, and are both aligned vertically.

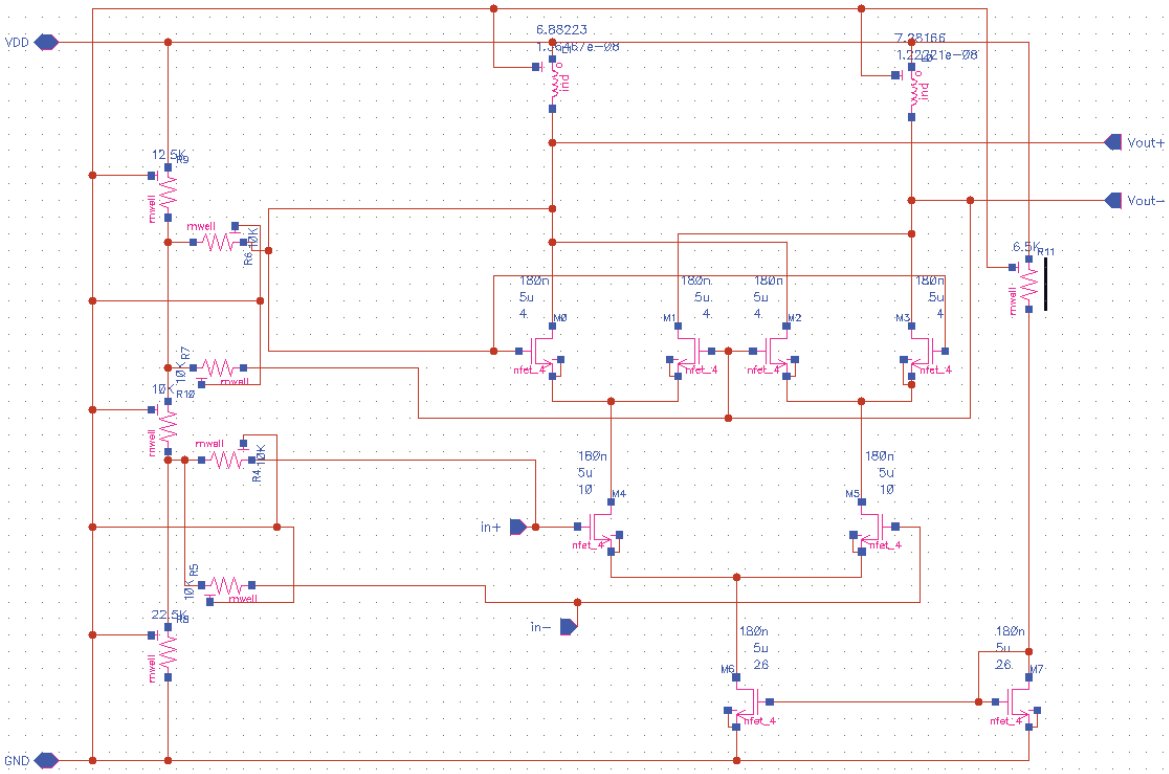

Figure 3.11 Schematic of RFD Implemented in ICFB

In order to measure the frequency of oscillation, a direction coupler was connected between the power supply and the node labeled "VDD" in Figure 3.11, and the output signal was viewed using a spectrum analyzer. Using a signal generator to feed the input with an arbitrary input power level and varying the frequency, the locking range is directly observed. When

synchronized, the output spectrum consists of half the injected signal only. When under injection but not synchronized, the output spectrum resembles a bandpass-filtered FM spectrum, as reported in [11].

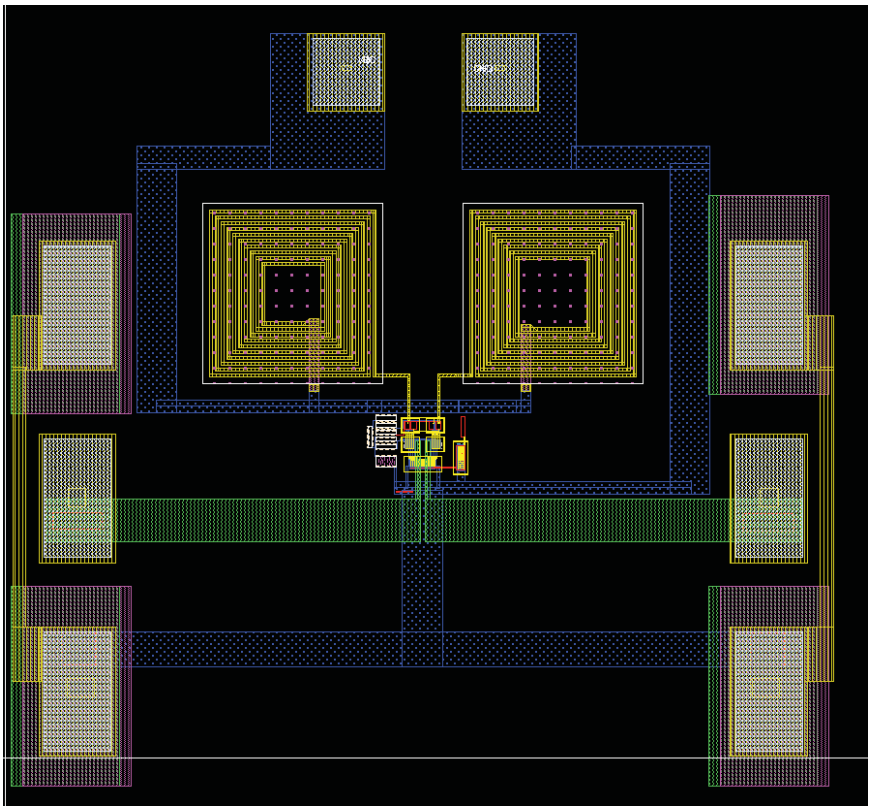

Figure 3.12 Layout of Implemented RFD

3.3 Performance of Frequency Dividers

For the implemented ILFD circuits, measurements of the dc power consumption and the locking range vs. input power are documented below. In addition, a measure of the phase noise of an ILFD is discussed, representing both Tail and Quench modes of operation. For the RFD, dc power consumption and the locking range are provided, as documented by simulations in Cadence Virtuoso.

3.3.1 Injection Locked Frequency Dividers

The following figure represents the measured oscillator current as a function of the voltage V_{BIAS} applied to the "Bias Voltage Input" in Figure 3.8. With no source applied to this node, i.e. the pin is left floating, the voltage at this pin is 1.18 V, and the nominal oscillator current is 1.27 mA.

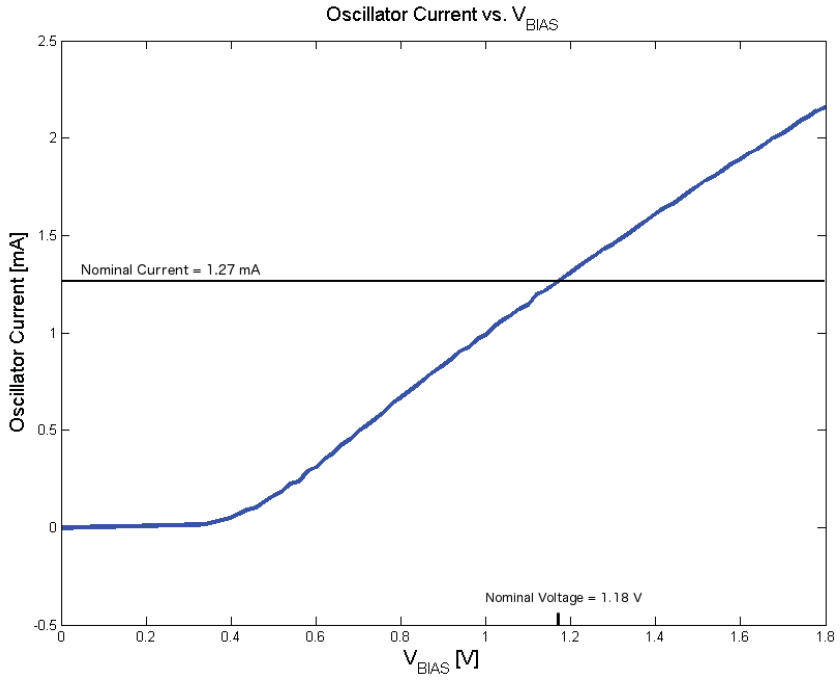

Figure 3.13 Oscillator Current as a Function of Applied V_{BIAS}

By varying the dc current that powers the oscillator, the locking performance at different levels of power consumption can be directly measured. However, because the Tail FET M_T is also the current source for the oscillator, its locking range was only measured at nominal power consumption. Otherwise, as the injection signal is superimposed on M_T's gate, the average bias current becomes a function of the applied input amplitude.

To quantify the "Locking Range" of an ILFD, a plot of the "Lock-in Power" versus frequency is generated, where the lock-in power is the power that is applied to the injection site

of the ILFD, in terms of dB_m. We note that this power level may be mapped to a voltage amplitude level to understand the expected behavior when the ILFD is used within an application specific IC. For this, a 0 dB_m "power" corresponds to an unloaded peak sinewave voltage of 0.63V.

The locking range refers to the range of frequencies of the injection signal that successfully result in injection-locked frequency division. The locking range varies depending on the value of the lock-in power, and tends to decrease as lock-in power decreases. For such a graph, the locking range is defined for any arbitrary lock-in power as the difference in frequency between the upper and lower intersects of the curve and the horizontal line defined by the given lock-in power. In this thesis, the lock-in power that establishes the locking range of interest is 0 dB_m. In the literature, the lock-in range is typically presented as a percentage of the operating frequency, i.e. exactly double the free-running frequency. When the lock-in power is too low to synchronize the oscillator, the output spectrum is observed to contain the free-running oscillation and sideband behavior resembling bandpass-filtered frequency modulation, as expected [11].

Tail-ILFD Locking Range Measurements

Figure 3.14 shows a plot of the lock-in power versus frequency for the Tail-ILFD:

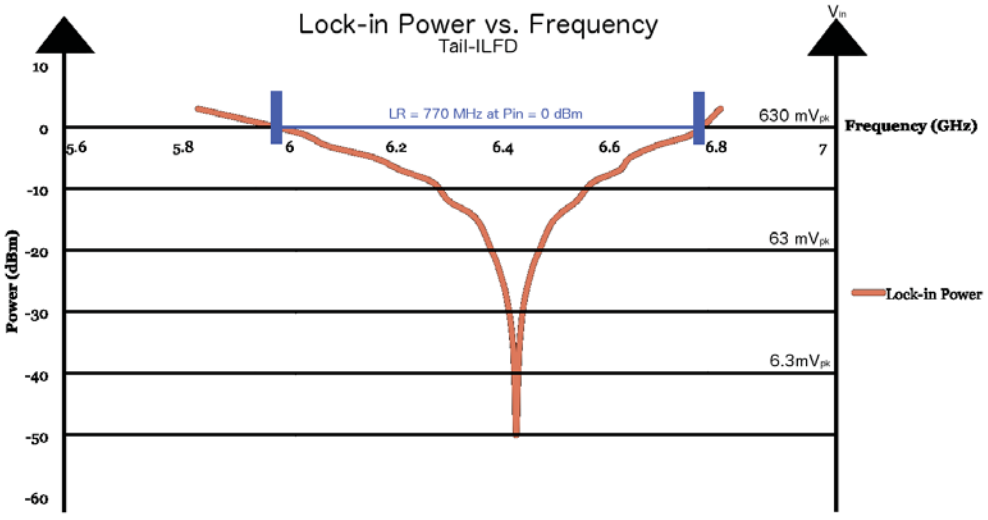

Figure 3.14 Lock-in Power vs. Input Frequency of Tail-ILFD at 2.28 mW dc

As seen in Figure 3.14, for a lock-in power of 0 dB_m (630 mV_{pk}), the locking range of the Tail-ILFD was measured as 770 MHz, with a free-running frequency of 6.4 GHz referred to the input. As a percentage, the locking range was 12%, while consuming a dc power of 2.28 mW.

By observing Figure 3.14, it can be seen that the lock-in range is mostly symmetrical about the free-running frequency for lock-in powers below -10 dB_m, corresponding to a 200 mV_{pk} input level. As the lock-in power increases to 0 dB_m, the curve deviates further in the direction of lower frequencies. This is believed to be due to the influence of parasitic capacitances present in the oscillator circuitry. In general, parasitic capacitances degrade the performance of active devices, and thus also the signal integrity, as the frequency of operation increases. Therefore, for large deviations from the free-running frequency, the parasitics introduced by the cross-coupled FETs and the output buffer are less pronounced at lower frequencies.

Quench-ILFD Locking Range Measurements

Two lock-in power versus frequency plots for the Quench-ILFD were generated, representing performance at both nominal power consumption and low power consumption. The first plot (Figure 3.15) represents locking range vs frequency of the Quench-ILFD at 2.28 mW (1.27 mA dc current), and the second (Figure 3.16) at 219.6 µW (122 µA dc current).

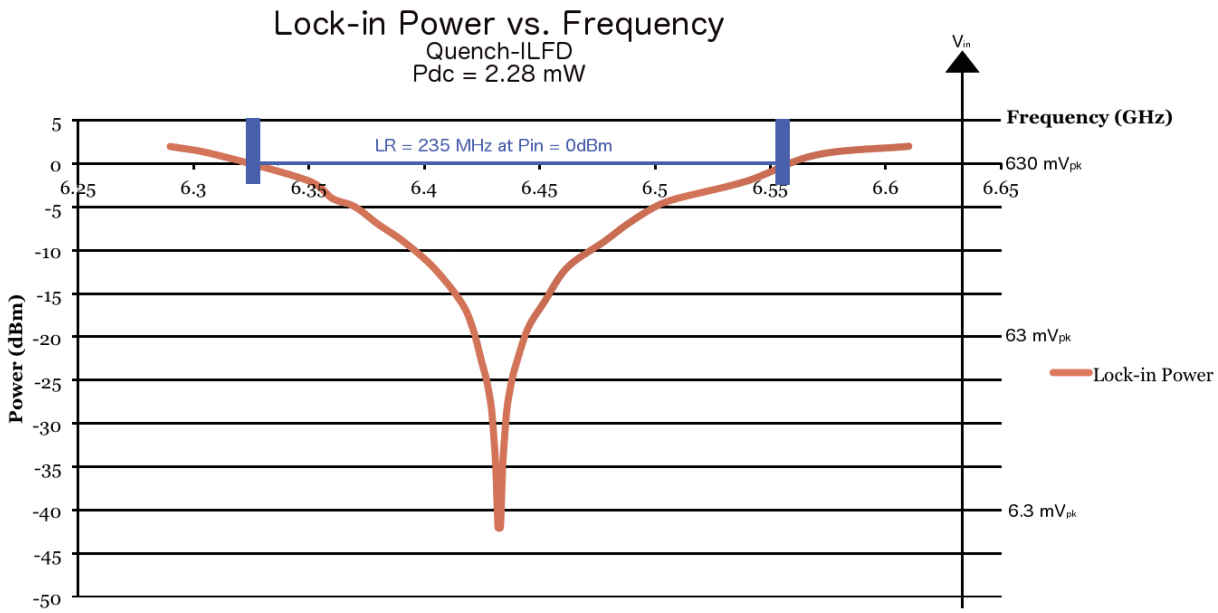

Figure 3.15 Lock-in Power vs. Input Frequency of Quench-ILFD at 2.28 mW dc

As seen in Figure 3.15, for a lock-in power of 0 dB_m, the locking range of the nominal-power Quench-ILFD was measured as 235 MHz, with a free-running input-referred frequency of 6.4 GHz. As a percentage, the locking range was 3.7%, while consuming a dc power of 2.28 mW.

As seen in Figure 3.16, for a lock-in power of 0 dB_m, the locking range of the low-power Quench-ILFD was measured as 307 MHz, with a free-running frequency of 6.4 GHz. As a percentage, the locking range was 4.8%, while consuming a dc power of 219.6 µW.

The results of Figures 3.15 and 3.16 suggest that the locking range of a Quench-ILFD is less than half that of a Tail-ILFD, for a given lock-in power. Also, Quench-ILFDs have an improved locking range when the oscillator circuitry is running at lower dc currents. And as lock-in power increases above -10 dB_m, the upper-bound of the lock-in power versus frequency curve deviates further from the operating frequency than the lower-bound. This asymmetry is contrary to the trend of the curve of Figure 3.14, where the locking range extends further for decreasing input frequencies for a Tail-ILFD.

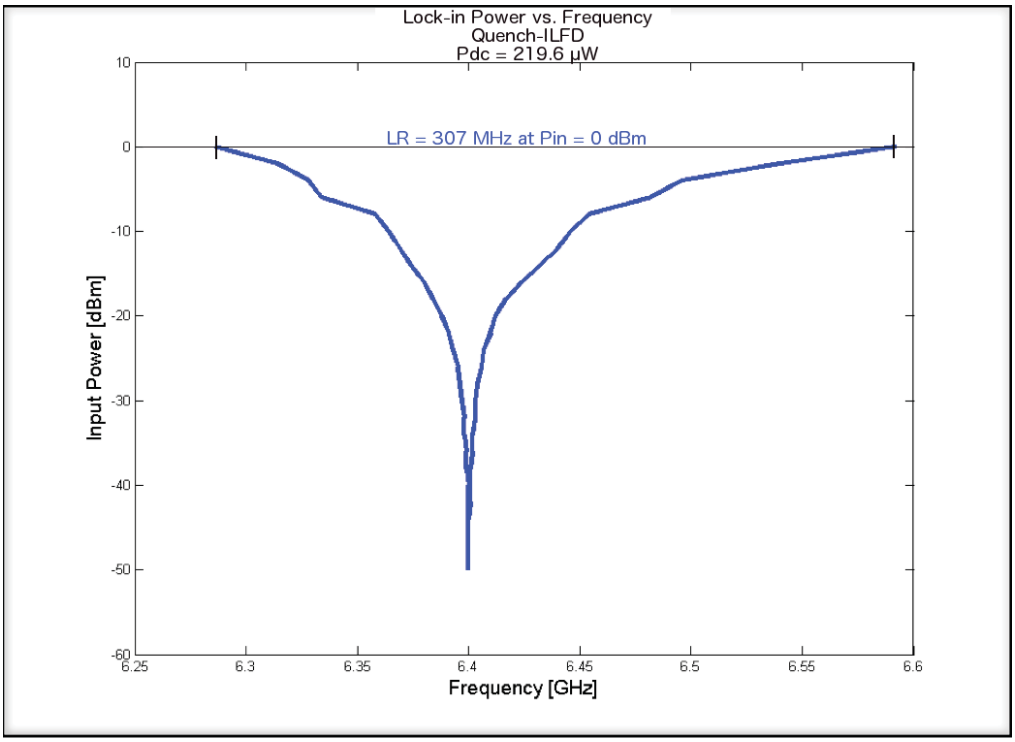

Figure 3.16 Lock-in Power vs. Input Frequency of Quench-ILFD at 219.6 µW DC

These observations can be understood by considering the operation of each injection FET, M_T and M_Q. M_T is biased in the active region, and the injection signal appears at the input of the mixer (as depicted in Figure 2.2) via the transconductance of M_T. Thus, the Tail-ILFD architecture has an inherent amplifying element, which effectively increases V_{inj}. This feature is lacking in the Quench-ILFD, since M_Q operates in the triode region. In Quench mode, V_{inj} does not see the same transconductance, and thus may have a smaller *effective* value for a given lock-in power, when compared the Tail-ILFD. Lastly, the impedance of the channel that connects the output terminals in Quench mode is dependent on the instantaneous value of the injection signal and the (W/L) ratio of M_Q, and thus limits high-frequency operation for a fixed lock-in power since a greater (W/L) ratio introduces greater parasitic capacitance directly at the output terminals.

The asymmetries of the locking ranges of both the Tail and Quench-ILFDs can also be explained in terms their effective values of V_{inj}. In Tail mode, V_{inj} is described by (3.24), and is

dependent on the value of $g_{m,T}$. As the frequency of operation increases, the effective value of $g_{m,T}$ decreases due to parasitics within M_T. As the frequency of operation decreases, $g_{m,T}$ becomes more "ideal." Thus, the curve of Figure 3.14 shifts further to the left for larger deviations from the operating frequency, defined by twice the free-running frequency. In Quench mode, the output oscillations degrade as the frequency of operation increases, due to parasitics within the circuitry. Therefore, the ratio of V_{inj} to the oscillator's voltage increases with frequency, and thus results in a higher modulation index for a given lock-in power. This need to overcome oscillation energy may also explain why the locking range of the Quench-ILFD is improved at lower power consumptions. If the ability to synchronize an oscillator's output is based on M_Q's ability to dissipate the energy between the terminals in its channel, then the locking range for a Quench-ILFD should increase as oscillator power decreases.

Phase Noise Measurements

Figure 3.17 is a photo of the spectrum analyzer as it was used to measure the phase noise of the ILFDs. Figure 3.17 shows the output spectrum and phase noise when locked to an input near its free-running frequency (i.e. $f_{inj} = 2f_{free}$).

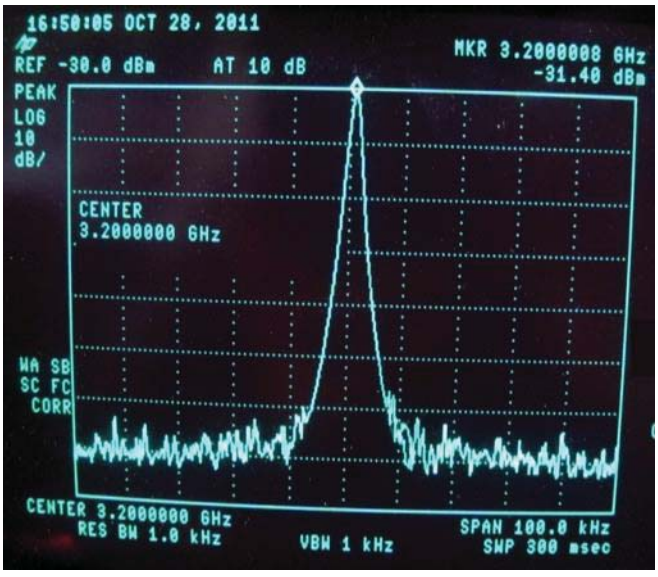

Figure 3.17 Output Spectrum and Phase Noise of locked ILFD

It should be noted that the phase noise of the ILFD is within the resolution of the spectrum analyzer. This gives the shape of the curve its smooth appearance, as it traces the passband of the resolution bandwidth (RBW) filter. With the RBW set to 1 kHz, the phase noise at 10 kHz offset can be calculated from Figure 3.16 as:

$$Phase\ Noise \leq -65\ dB_c - 10\log[RBW] = -95\ dB_c \tag{3.32}$$

The phase noise of the oscillator in injection-locked operation is no more than -*95* dB_c at a mere 10kHz offset from the fundamental frequency.

3.3.2 Regenerative Frequency Divider

Results for the RFD presented here are results of simulations in Cadence Virtuoso. This is because measurements of the RFD implemented in CMOS could not be carried out. This is currently believed to be due to issues with phase-shifters used in testing and hence an inability to drive the circuit with a satisfactory differential signal. Also, since the quality factor of the tank establishes its impedance for ac signals, the overall quality factor was degraded due to C_p, the tank capacitance for the RFD, being implemented using the parasitics of the feedback FETs. This is because of the assumption that the *Q* of the tank is equal to the quality factor of the inductor is based on capacitors of effectively infinite Q. When Metal-Insulator-Metal (MIM) caps are constructed, this is the case. However, this may not be true when using parasitic capacitances of active devices which are not well modeled.

The following figure shows the “testbench” setup used to simulate the behavior of the designed RFD:

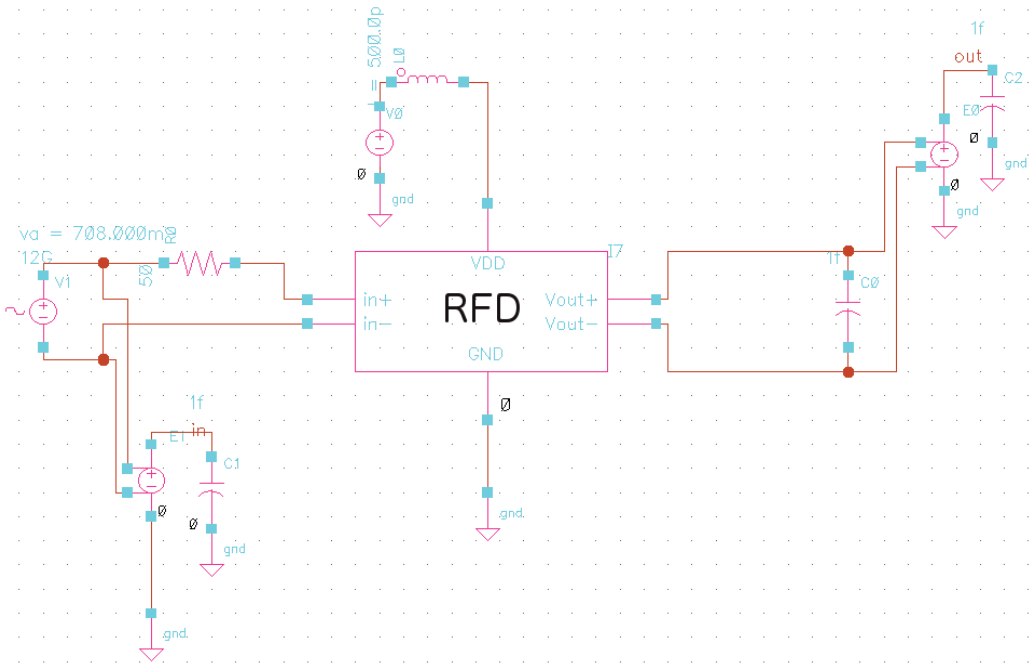

Figure 3.18 Testbench Setup used to Simulate RFD in Cadence ICFB

The simulated RFD of Figure 3.18 consumes 228 µA of dc current, at 410 µW. To simulate an input voltage equivalent to a real-world RF signal generator outputting 0 dB_m of power, the RFD is driven with a differential voltage of 630 mV with a source impedance of 50Ω. The locking range is determined using this model, and Figures 3.19 and 3.20 show the simulations used to determine the range of frequencies that can be synchronized to exactly half the frequency of the input signal.

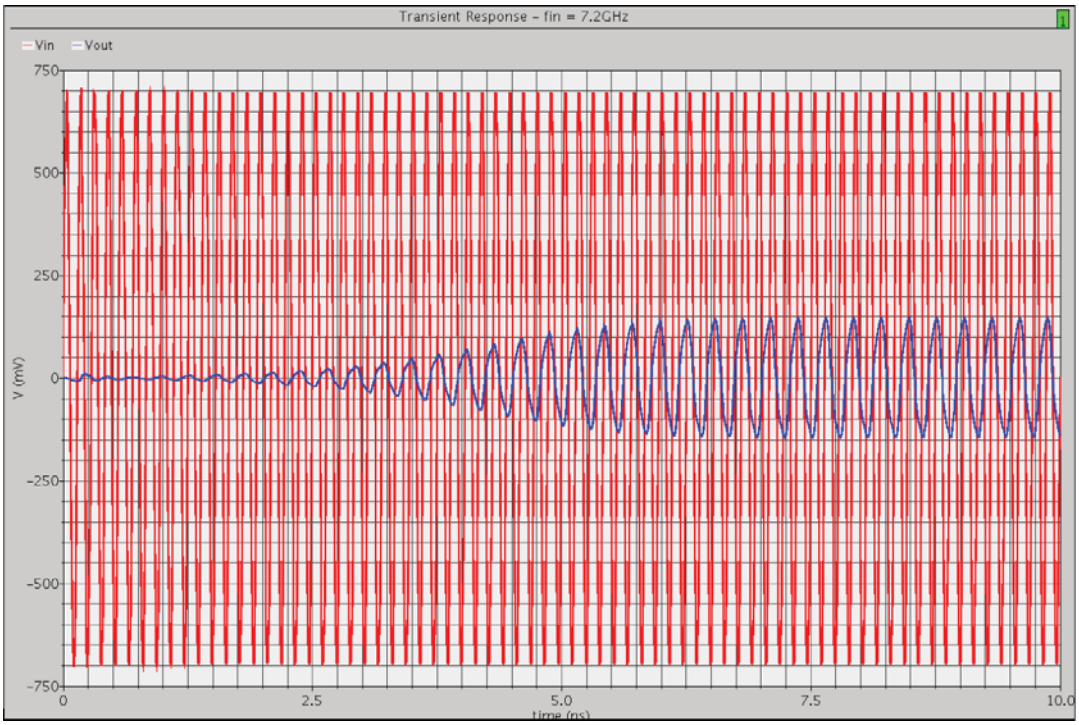

Figure 3.19 Simulation of Lower-Bound of Divisible Frequencies

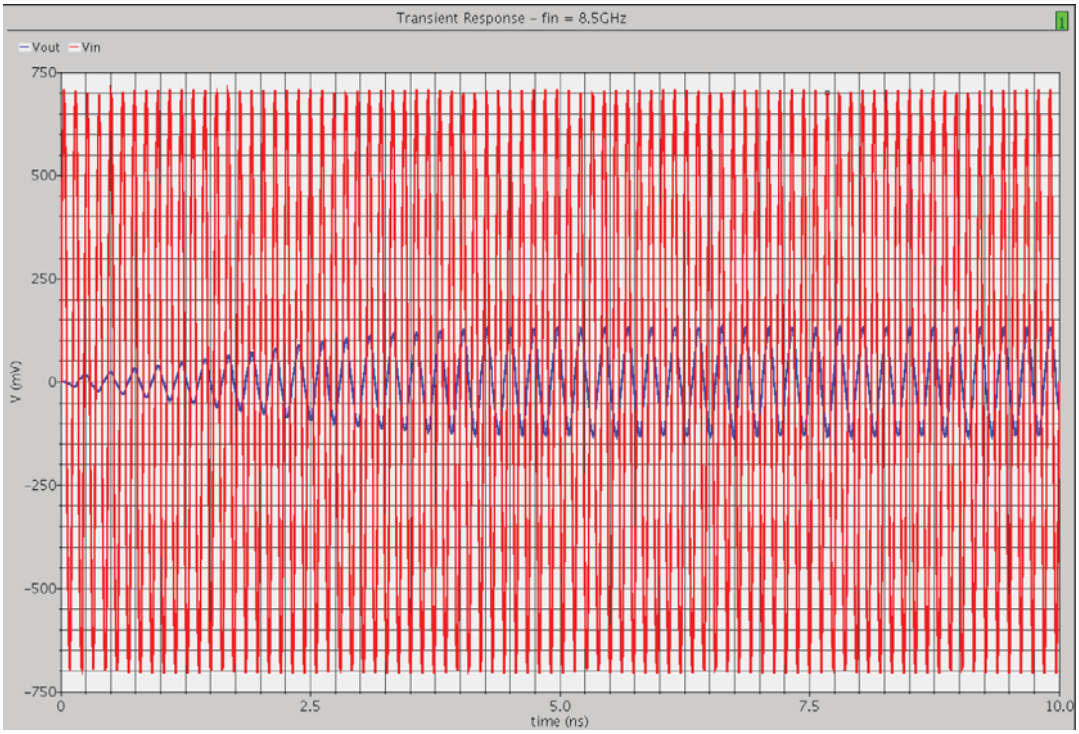

Figure 3.20 Simulation of Upper-Bound of Divisible Frequencies

From the frequencies observed in Figures 3.19 and 3.20, the range of divisible frequencies for the simulated RFD is equal to:

$$Range\ of\ Divisible\ Frequencies\ =\ (8.5 - 7.2)\ GHz\ =\ 1.3\ GHz \qquad (3.33)$$

Using the simulator to analyze the ac response of the RFD of Figure 3.9 reveals its resonant frequency, which can be used to estimate the free-running frequency for this divider. Note that the values on the vertical scale in Figure 3.21 do not indicate the magnitude of the output oscillation voltage, but rather give a description of the bandpass of the filter implemented in the RFD.

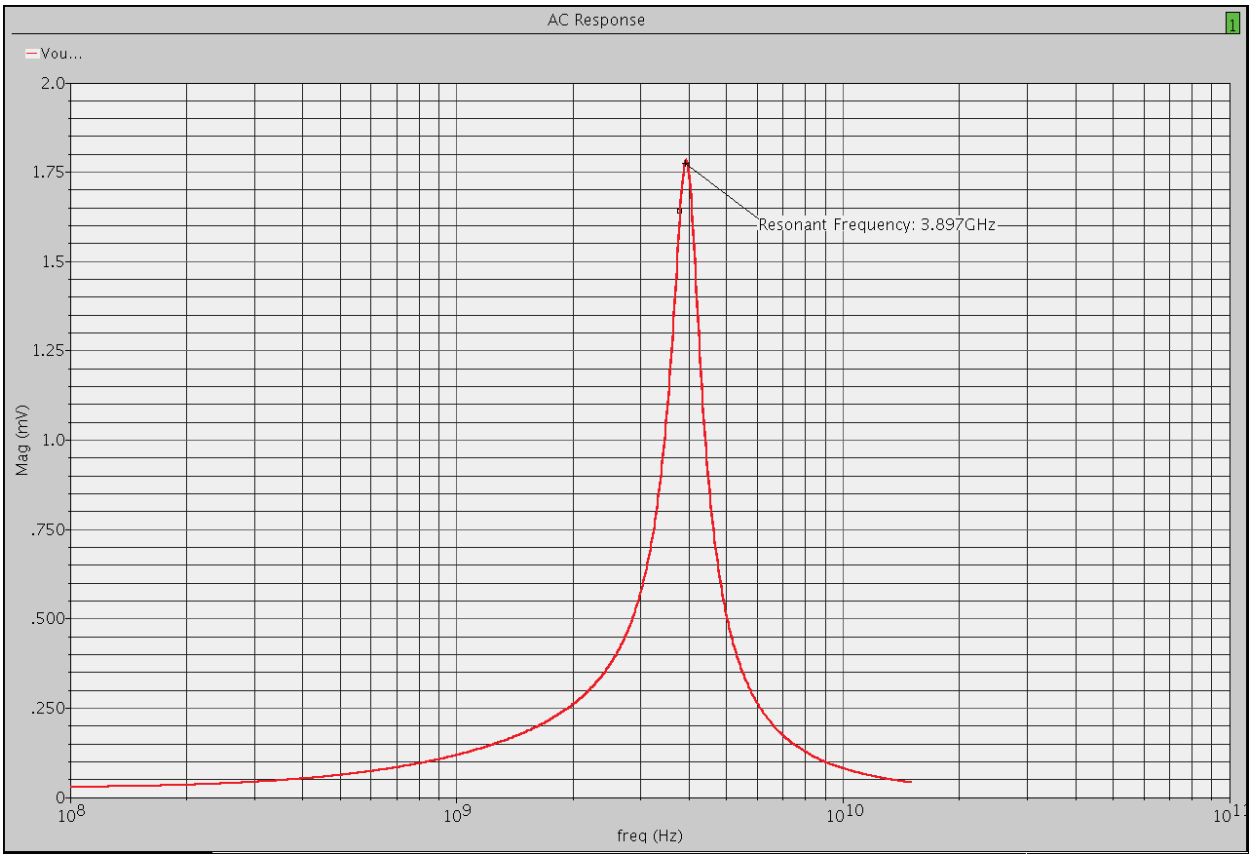

Figure 3.21 AC Response Simulation of RFD used to Determine Operating Frequency

Using 7.8 GHz as the frequency of operation for the RFD, its dividing range can be expressed as a percentage of 16.7%. Compared to the results obtained from Figure 3.13, it can be seen that simulations report that the range of the RFD is wider than that of the Tail-ILFD, while consuming much less power.

Chapter 4 - Low Noise Amplifiers

This thesis documents an LNA that is a modification of the Partial Noise Cancelling LNA presented in [1]. A simplified representation of the LNA presented in [1] is shown in Figure 4.1. A gain of 21 dB (over the range 2 to 2300 MHz), an IIP3 of -1.5 dB_m at 100 MHz, and a minimum and maximum noise figure (NF) of 1.4 and 1.7 dB (over the range 100 MHz to 2.3 GHz) are reported. The LNA consumes 18 mW of dc power, at a supply voltage of 1.8V and a dc current of 10 mA. Large-value coupling capacitors that connect the gates of $M_{N,1}$ and $M_{P,0}$, as well as the gates of $M_{N,0}$ and $M_{P,1}$ are not shown in Figure 4.1.

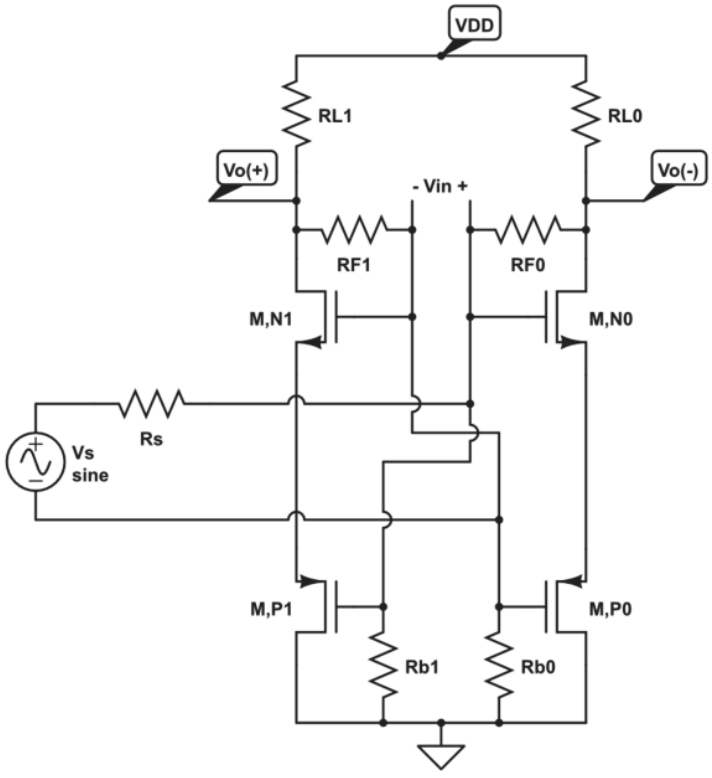

Figure 4.1 Simplified Schematic of LNA Presented in [1]

By replacing the resistors $R_{L,0}$ and $R_{L,1}$ of Figure 4.1 with a tuned load, a narrowband version of the above PNC LNA can be designed with the goal of improving the performance, especially relative to large out-of-band signals. Since the thermal noise contribution of a tuned load is inversely proportional to $(Q_L)^2$, whereas the quality factor of a resistive load is one, using a bandpass filter at the output should result in an improved NF. For all other conditions held equal, a high Q enhances the gain of the LNA, which (1.14) shows improves the NF. In addition to this, a tuned load allows the output voltage to swing beyond the supply voltage, due to the energy storing nature of the reactive elements. Increasing the swing of the output voltage should also improve the output-referred 1dB compression point ($P_{c,o}$) by decreasing the non-linearity at this node. Also, since the expressions for voltage (4.1) and power (4.2) of the IM products are:

$$v_{out,IM} = c_{IM}\left(v_{in,pk}\right)^3 \tag{4.1}$$

$$P_{out,IM} = 3P_{in} + C_{IM} \tag{4.2}$$

where c_{IM} is a constant based on the non-linearity of the output signal (and C_{IM} its decibel equivalent) , then increasing the swing of the output voltage should also result in increased IIP3 and OIP3 values, if the bias overdrive voltage of the input FET is sufficiently large. Lastly, because the tuned load also acts as a BPF, it should improve the out-of-band compression point, by attenuating such signals at the output. Simulation results for the designed narrowband PNC LNA are included in section 4.3, and are generated using Cadence Virtuoso. In this thesis we focus on the large signal handling issue.

In order to compare the performance of the narrowband PNC LNA, in terms of small and large signal processing, a cascode S-L (source-inductor) LNA was also designed, and simulation results are included in section 4.3.

4.1 Theory of Operation

4.1.1 Cascode Source-Inductor Low Noise Amplifier

Source-Inductor LNAs, discussed at the end of section 2.2.2, are essentially impedance-matched narrowband versions of a common-source (CS) amplifier employing source degeneration feedback as a means of cancelling the FET's channel noise. The inductor in the source terminal of the device is also made to resonate with the FET's parasitic, which results in an ideally real impedance between the FET's gate terminal and ground. The magnitude of the resistive input impedance is dependent on the transconductance of the FET and the inductance and capacitance values used. This mechanism thus enables impedance matching to any arbitrary source. Using a cascode configuration as well will mitigate Miller capacitance and increase the output impedance of the cascode FET, while having no effect on the midband NF. A generic schematic for the S-L LNA documented in this thesis is shown in Figure 4.2.

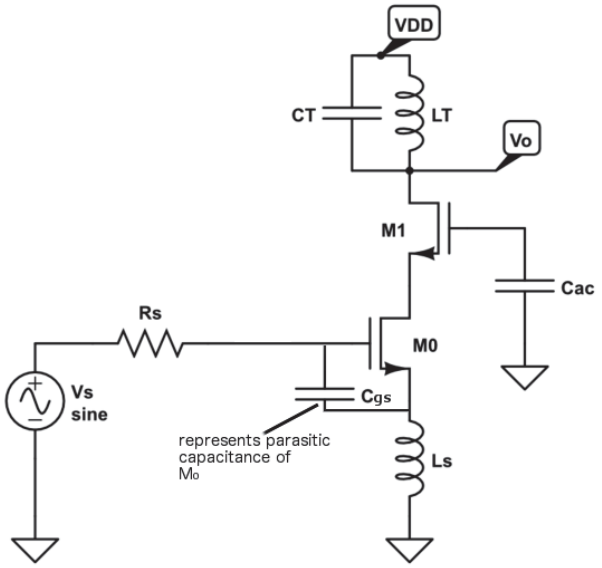

Figure 4.2 Generic Cascode S-L LNA Schematic

Small Signal Parameters

In the LNA of Figure 4.2, the parasitic capacitance of $C_{gs,0}$ resonates with the inductance L_s. The inductor L_S has some parasitic resistance at ω_o, described by its Q-factor Q_S. The small-signal model of Figure 4.3 is used to obtain the input impedance of the S-L LNA at resonance. In the figure, R_t represents the parasitic resistance of the traces that form L_s.

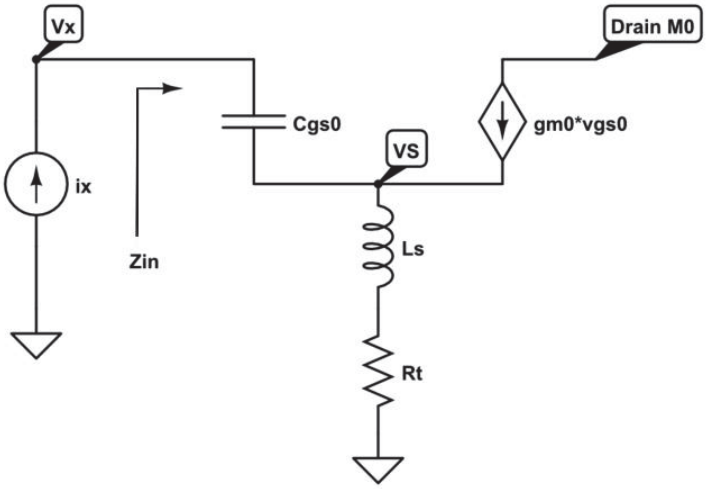

Figure 4.3 Small-Signal Model used to obtain Input Impedance and Voltage Gain

In Figure 4.3, a current i_x is applied to the gate of M_0 of the schematic in Figure 4.2. By determining the ratio of the resulting voltage v_x to i_x, the input impedance as a function of frequency is obtained. Solving the KVL expression for the loop that follows the input current i_x leads to:

$$v_x = i_x(j\omega C_{gs})^{-1} + (i_x + g_{m,0}v_{gs,0})[j\omega L_S + R_t] \tag{4.3}$$

where $R_t = \omega L_S/Q_S$. The voltage that develops due to i_x flowing through C_{gs} results in a v_{gs} of:

$$v_{gs,0} = i_x(j\omega C_{gs,0})^{-1} \tag{4.4}$$

Substituting $v_{gs,0}$ in (4.3) with that of (4.4) and rearranging terms gives:

$$v_x = i_x[(j\omega C_{gs,0}^{-1} + (1 + \frac{g_{m,0}}{j\omega C_{gs,0}})(j\omega L_S + R_t)] \tag{4.5}$$

The expression of (4.5) is used to obtain the input impedance as v_x/i_x at ω_o:

$$Z_{in}|_{\omega=\omega_o} = \frac{v_x}{i_x}|_{\omega=\omega_o} = \left(\frac{g_{m,o}L_S}{C_{gs,o}} + \frac{\omega_o L_S}{Q_S}\right) \tag{4.6}$$

As Q_S approaches infinity, the second and third terms of (4.6) approach zero. In this way, the transconductance $g_{m,0}$ can be used to theoretically match any arbitrary impedance.

The output impedance of the S-L LNA in Figure 4.2 can be approximated as:

$$Z_o = Q_T \omega L_T \tag{4.7}$$

Figure 4.3 can also be used to obtain an expression for the voltage gain of this S-L LNA. When Z_{in} of expression (4.6) is matched to R_s, v_x is equal to half of the signal source voltage, and the input current i_{in} in terms of R_s can be written as:

$$i_{in} = \frac{v_x}{Z_{in}} = \frac{\left(\frac{1}{2}\right)V_s\left[\left(R_s + \frac{\omega L_S}{Q_S}\right) - j\left(\frac{R_s}{Q_S}\right)\right]}{\left[\left(R_s + \frac{\omega L_S}{Q_S}\right)^2 + \left(\frac{R_s}{Q_S}\right)^2\right]} \tag{4.8}$$

The resulting $v_{gs,0}$ that develops across $C_{gs,0}$ is:

$$v_{gs,0} = \frac{\left(\frac{1}{2}\right)V_s(j\omega C_{gs,o})^{-1}\left[\left(R_s + \frac{\omega L_S}{Q_S}\right) - j\left(\frac{R_s}{Q_S}\right)\right]}{\left[\left(R_s + \frac{\omega L_S}{Q_S}\right)^2 + \left(\frac{R_s}{Q_S}\right)^2\right]} \tag{4.9}$$

Using (4.9) and the common approximation for the output voltage at resonance, the voltage gain with respect to the signal source is obtained as:

$$A_{V_s} = \frac{j\left(\frac{1}{2}\right)g_{m,o}Q_T\omega L_T(\omega C_{gs,o})^{-1}\left[\left(Rs + \frac{\omega LS}{QS}\right) - j\left(\frac{Rs}{QS}\right)\right]}{\left[\left(R_s + \frac{\omega L_S}{Q_S}\right)^2 + \left(\frac{R_s}{Q_S}\right)^2\right]} \tag{4.10}$$

The magnitude of the power gain of this LNA, as a product of the gain of (4.10) squared and the input impedance of (4.6) divided by the output impedance of (4.7), is:

$$G_p = \frac{\left(\frac{1}{4}\right)\left(\frac{g_{m,o}}{C_{gs,o}}\right)^2 Q_T\omega L_T\sqrt{\left[\left(R_s + \frac{\omega L_S}{Q_S}\right)^2 + \left(\frac{R_s}{Q_S}\right)^2\right]}}{\left[\left(R_s + \frac{\omega L_S}{Q_S}\right)^2 + \left(\frac{R_s}{Q_S}\right)^2\right]} \tag{4.11}$$

When Q_S approaches infinity, the power gain of (4.11) at resonance tends towards:

$$G_p = \left(\frac{1}{4}\right)\frac{g_{m,o}^2}{R_s(\omega_o C_{gs,o})^2} Q_T \omega_o L_T \tag{4.12}$$

Correspondingly, the voltage A_{Vs} of (4.10) tends towards:

$$A_{V_s} = \frac{j\left(\frac{1}{2}\right) g_{m,o} Q_T \omega_o L_T}{R_s \omega_o C_{gs,o}} \tag{4.13}$$

The term of $(R_s\omega_o C_{gs,0})^{-1}$ in expression (4.13) is the quality factor of the input RLC network composed of R_s, $C_{gs,0}$, and L_S. At ω_o, the term $(R_s\omega_o C_{gs,0})^{-1}$ should much greater than one, which is accomplished if $C_{gs,0}$ is sufficiently small that the reactance $X_{Cgs,0}$ is much greater than the source resistance R_s.

Noise Figure

Figure 4.4 shows the equivalent noise model for the S-L LNA and is used to obtain a first-order approximation of the noise figure. The noise power due to R_s is amplified to the output by the power gain described by (4.11), and can be written as:

$$P_{on,R_s} = kTB\frac{\left[R_s\left(\frac{g_{m,o}}{\omega_o C_{gs,o}}\right)^2 Q_T \omega_o L_T\right]}{\left[\sqrt{\left(2+\frac{\omega_o L_S}{Q_S}\right)^2 + (Q_S)^{-2}}\right]\left(\left(R_s + \frac{\omega_o L_S}{Q_S}\right)^2 + (R_s + Q_S)^2\right)} \tag{4.14}$$

Half of the thermal noise contribution due to the amplifying transistor M_0 is cancelled due to the inductive source degeneration and the matching identity of:

$$\frac{g_{m,o} L_S}{C_{gs,o}} = R_s \tag{4.15}$$

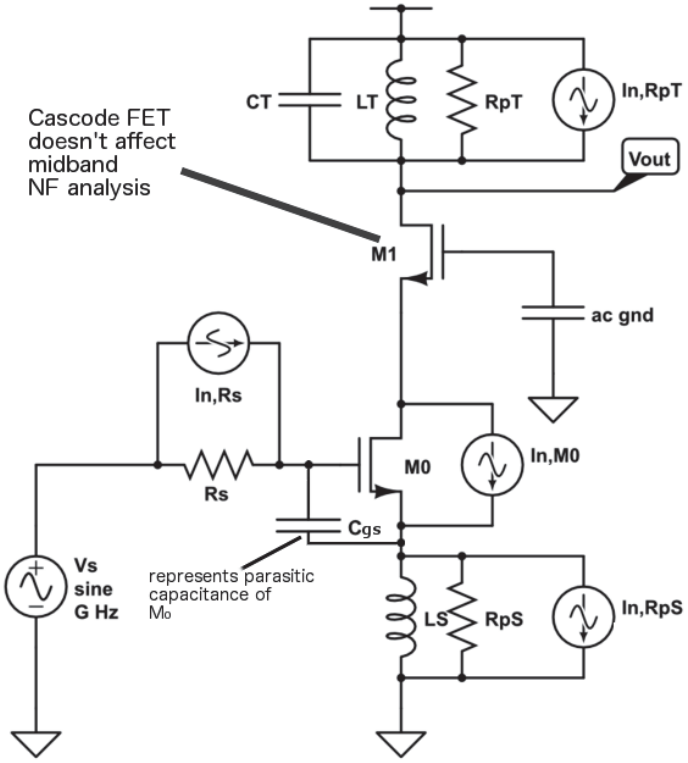

Figure 4.4 Thermal Noise Model of S-L LNA

When M_0's noise current $i_{n,M0}$ is injected *out of* the drain of M_0, it causes a negative output voltage of:

$$v_o = -i_{n,M0} Q_T \omega_o L_T \tag{4.16}$$

This same noise current is injected *into* the source terminal of M_0. It causes the following voltage v_x to develop:

$$v_x = i_{n,M0}[Z_{LC} \,//\, (\frac{1}{g_{m,o}}) \,] \tag{4.17}$$

where Z_{LsCgs} is the parallel-equivalent impedance of the LC network, which behaves as a tank circuit for signals at the source of M_0. At resonance, Z_{LsCgs} can be expressed as:

$$Z_{L_S C_{gs}} = Q' \omega_o L_S \tag{4.18}$$

where *Q'* is the composite quality factor of the RLC network. *Q'* is obtained as:

$$Q' = Q_S \,//\, \left(\frac{\left|X_{C_{gs,o}}\right|}{R_s}\right) \tag{4.19}$$

which is simplified for:

$$Q' = \left(\frac{1}{Q_S} + R_s \omega_o C_{gs,0}\right)^{-1} \tag{4.20}$$

Now, Z_{LsCgs} of (4.18) can be expressed as:

$$Z_{L_S C_{gs}} = \frac{\omega_o L_S}{\frac{1}{Q_S} + R_s \omega_o C_{gs,o}} \tag{4.21}$$

Assuming a high-quality L_S such that $(Q_S)^{-1} << R_s\omega_o C_{gs,0}$, the impedance of the resonant circuit described by (4.21) becomes:

$$Z_{L_S C_{gs}} = \frac{\omega_o L_S}{R_s \omega_o C_{gs,o}} \tag{4.22}$$

Given the matching condition of (4.15), Z_{LsCgs} can be written as:

$$Z_{L_S C_{gs}} = \frac{1}{g_{m,o}} \tag{4.23}$$

The impedance of (4.23) appears in parallel to the impedance looking into the source of M_0, which to a first-order is $1/g_{m,0}$. The resulting voltage at this terminal, according to (4.17), is now:

$$v_x = \frac{\left(\frac{1}{2}\right) i_{n,M0}}{g_{m,0}} \tag{4.24}$$

Because of the series resonance of C_{gs} and L_S, the gate terminal of M_0 is at ac ground at ω_o. Therefore, the voltage v_x of (4.24) is amplified to the output of the LNA via the common-gate mechanism of M_0. The output voltage due to summation of (4.16) and (4.24) is:

$$v_{on,M0} = -\left(\frac{1}{2}\right) i_{n,M0} Q_T \omega_o L_T \tag{4.25}$$

Expressed as a noise power, the thermal noise contribution to the output of this S-L LNA is:

$$P_{on,M0} = kTB\left[\left(\frac{2}{3}\right) g_{m,0} Q_T \omega_o L_T\right] \tag{4.26}$$

The inductor L_S introduces a noise current inversely proportional to the root of the parallel-equivalent impedance of L_s, and is expressed as:

$$i_{n,L_S} = \sqrt{\frac{4kTB}{Q_S \omega_o L_S}} \tag{4.27}$$

This current causes a voltage v_x at the source terminal of M_0 to develop of:

$$v_x = \frac{i_{n,L_S}}{2g_{m,o}} \tag{4.28}$$

The voltage of (4.28) appears at the output terminal of the LNA in the same manner as the noise voltage of (4.24) - through the common-gate configuration of M_0 relative to signals at its source terminal. Therefore, the output noise voltage due to L_S is:

$$v_{on,L_S} = \sqrt{\frac{4kTB}{Q_S \omega_o L_S}} \left(\left(\frac{1}{2}\right) Q_T \omega_o L_T\right) \tag{4.29}$$

and the corresponding output noise power contribution is:

$$P_{on,L_S} = kTB\left[\frac{Q_T \omega_o L_T}{Q_S \omega_o L_S}\right] \tag{4.30}$$

The last significant noise source is the parasitic resistance of the tank circuit load, which contributes the following noise power to the output:

$$P_{on,L_T} = kTB\left[\frac{4}{(Q_T)^2}\right] \tag{4.31}$$

Summing all of the noise power contributions of (4.14), (4.26), (4.30), and (4.31) gives the total output noise power of the S-L LNA of Figure 4.2. Then dividing the sum by (4.14), which is the noise power contribution due to R_s, and simplifying results in the following NF for this LNA:

$$F = 1 + \frac{(\omega_o C_{gs})^2\left[\left(R_s + \frac{\omega_o L_S}{Q_S}\right)^2 + \left(\frac{R_s}{Q_S}\right)^2\right]\sqrt{2 + \left(\frac{\omega_o L_S}{R_s Q_S}\right)^2 + \left(\frac{1}{Q_S}\right)^2}}{g_{m,o}^2 R_s}\left[\frac{2}{3} g_{m,0} + \frac{1}{Q_S \omega_o L_S} + \frac{4}{Q_T^2 (Q_T \omega_o L_T)}\right] \tag{4.32}$$

In the case where:

$$R_s >> \frac{\omega_o L_S}{Q_S} \tag{4.33}$$

the NF of (4.32) becomes:

$$F = 1 + \frac{2R_s(\omega_o C_{gs,0})^2}{g_{m,o}^2}\left[\frac{2}{3} g_{m,0} + \frac{1}{Q_S \omega_o L_S} + \frac{4}{Q_T^2 (Q_T \omega_o L_T)}\right] \tag{4.34}$$

It can be seen from (4.34) that the NF contribution of the circuitry composing the S-L LNA is inversely proportional to the quality factor of the input RLC network, given as:

$$Q_{L_S C_{gs}} = \frac{1}{R_s \omega_o C_{gs,o}} \tag{4.35}$$

As the quality factor of (4.35) increases, the theoretical minimum NF of this S-L LNA tends towards 0 dB.

Large Signal Parameters

At the input, compression occurs when $-v_{in,pk}$ is large enough to drive M_0 to cutoff when superimposed on its dc gate voltage, causing the instantaneous voltage $v_{GS,M0}$ to fall beneath the threshold voltage for the device, V_{th}. The dc voltage $V_{GS,M0} - V_{th}$ is defined as the overdrive voltage, v_{ov}. When $|-v_{in,pk}| \geq |v_{ov}|$, compression occurs, and the corresponding maximum input power that results in distortionless signal processing is:

$$P_{in,max} = \frac{(v_{ov})^2}{2R_{in}} = \frac{(V_{GS,Mo} - V_{th})^2}{2R_s} \tag{4.36}$$

At the output, compression occurs when the voltage attempts to exceed twice that of the supply, *VDD*. The maximum output voltage before compression occurs can therefore be written as:

$$v_{o,max} = 2VDD \tag{4.37}$$

This implies that the maximum input voltage that will result in distortionless signal processing, relative to output compression, is:

$$v_{in,max} = \frac{v_{o,max}}{A_v} = \frac{4VDD}{g_{m,o} Q_T \omega_o L_T (R_s \omega_o C_{gs,o})^{-1}} \tag{4.38}$$

Assuming high-quality inductors, the maximum input power corresponding to (4.38) is:

$$P_{in,max} = \frac{(v_{in,max})^2}{2R_{in}} = \frac{(4VDD)^2}{\frac{g_{m,o} L_S}{C_{gs,o}}} \tag{4.39}$$

In practice, the minimum between (107) and (110) sets $P_{in,max}$. Note that these powers are approximated with respect to the input terminal of the S-L LNA of Figure 4.2, not with respect to the source voltage V_s. When impedance matching applies, the maximum source voltage $V_{s,max}$ before compression is twice that of (109), since half is dropped across R_s.

4.1.2 Partial Noise Cancelling Low Noise Amplifier

The PNC LNA documented in this thesis is a narrowband version of the LNA presented in [1], and its generic schematic is shown in Figure 4.5. The pFET M_{bias} establishes the dc current, and its gate is connected to a current mirror. Due to the differential nature of this LNA, the noise of M_{bias} is cancelled because it appears at virtual ground. The tuned load is implemented by inductors L_0 and L_1, and they resonate with the parasitic capacitances of $M_{N,0}$ and $M_{N,1}$, and any loading present. In the CMOS implementation elaborated in the next section, some of this capacitance is also due to the buffers that follow the LNA. Resistors $R_{F,0}$ and $R_{F,1}$ provide shunt-feedback to $M_{N,0}$ and $M_{N,1}$, respectively, and are designed so that the differential input impedance is equal to $(1/g_{m,0} + 1/g_{m,1})$. Capacitors C_0 and C_1 cross-couple the pFETs and nFETs, which leads to partial noise cancelling of the all the active devices of Figure 4.3 through multiple feedback paths, explained later. Lastly, resistors R_{b0} and R_{b1} bias the pFETs $M_{P,0}$ and $M_{P,1}$.

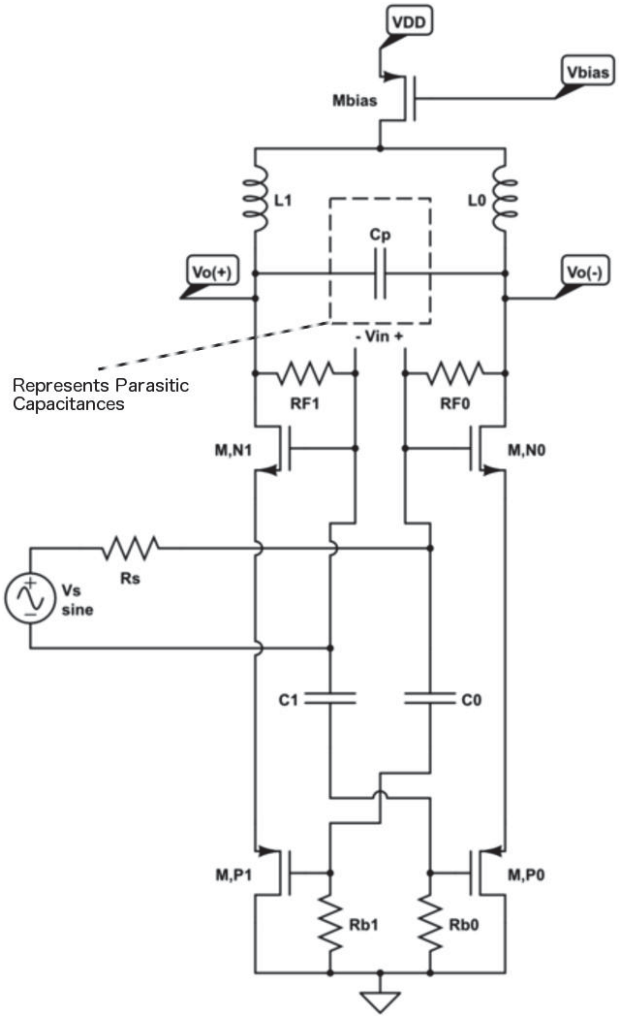

Figure 4.5 Generic Narrowband PNC LNA

Small Signal Parameters

The midband input impedance Z_{in} is obtained by analyzing the schematic in Figure 4.6, which represents the current-draw for the half-circuit model of the PNC LNA in Figure 4.5, assuming the capacitances of $M_{P,0}$ and $M_{P,1}$ are negligible (therefore not drawing current at midband frequencies). Analyzing Figure 4.6 results in the correct approximation for Z_{in} and its differential complement $Z_{in,diff}$. Note that the drain-source impedance r_o of the FETs are assumed to be large enough to have negligible effect on circuit behavior.

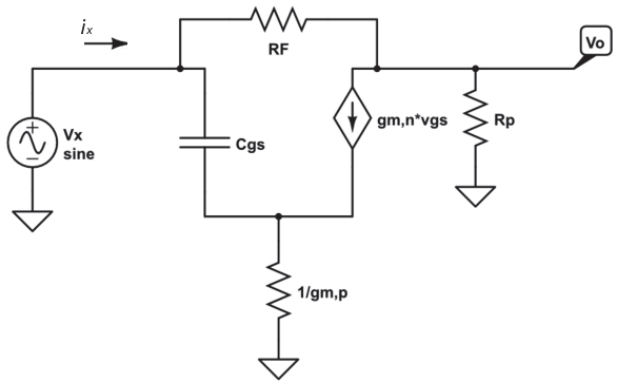

Figure 4.6 Half-Circuit Model of PNC LNA used to Determine Input Impedance

In Figure 4.6 , V_x is a test source applied to the half-circuit, which draws i_x current. R_p represents the equivalent impedance of the tuned load at resonance. R_F is the feedback resistor that appears on both input FETs. C_{gs}, represents the gate-source capacitance of the input FET, and is assumed to be negligible in this midband analysis. As mentioned previously, the capacitances of the cross-coupled pFETs are also considered negligible at midband. The impedance of $1/g_{m,p}$ represents the source-degeneration behavior due to the pFET that appears in series with the source terminal of the input nFET, as seen in Figure 4.6. Solving the KCL equation at the node labeled V_o reveals:

$$0 = V_o/R_p + g_{m,n}v_{gs} - ix \tag{4.40}$$

Assuming $V_o/R_p << g_{m,n}v_{gs}$ and rearranging (4.40) shows:

$$i_x = g_{m,n}v_{gs} \tag{4.41}$$

Since V_x appears between the gate terminal and ground, the gate voltage V_G is equal to V_x. Upon inspection of Figure 4.6, the source terminal's voltage V_S is equal to the product $(g_{m,n}v_{gs})(1/g_{m,p})$. Thus, v_{gs} can be written as:

$$v_{gs} = V_G - V_S = V_x - v_{gs}\left(\frac{g_{m,n}}{g_{m,p}}\right) \tag{4.42}$$

By setting the transconductances of all FETs equal, and rearranging (4.42), the following expression is used to replace the v_{gs} term in (4.41):

$$v_{gs} = \frac{V_x}{2} \tag{4.43}$$

Now, (4.41) becomes:

$$i_x = \frac{g_{m,n} V_x}{2} \tag{4.44}$$

which is manipulated to reveal the half-circuit input impedance at midband for this PNC LNA:

$$Z_{in} = \frac{V_x}{i_x} = \frac{2}{g_{m,n}} \tag{4.45}$$

Doubling this value reveals the differential input impedance at midband, $Z_{in,diff}$:

$$Z_{in,diff} = \frac{V_x}{i_x} = \frac{4}{g_{m,n}} \tag{4.46}$$

The expression of (4.45) discloses an inherent feature of the source-degeneration due to the series pFET. Setting $Z_{in,}$ to 50Ω implies that the transconductance of each FET must be:

$$g_{m,n} = \frac{2}{50\Omega} = 40\ mS \tag{4.47}$$

which is double what it would otherwise be in a topology not employing such source-degeneration. Since the power of the signal at the output is dependent on $(g_m)^2$, whereas the channel noise power of the FET is dependent on $(^2/_3)g_m$ (as shown in Figure 2.11), increasing g_m should imply a better noise figure.

The differential voltage gain for the LNA of Figure 4.5 is obtained by summing the differential voltage gain due to each individual input terminal. In classic differential topologies, this is not the case, since each output terminal is linearly dependent on only one input terminal. But due to the cross-coupling of the n and p FETs seen in Figure 4.5, the signal at each input terminal appears at the output terminal of the same polarity. Each pFET acts as a common-drain (CD) amplifier, also known as a source-follower. The source-follower operation imposes a fraction of the half-circuit input voltage on the source terminal of the other half-circuit nFET, whose gate is the input terminal of opposite polarity. Superposition allows the assumption that this input terminal is at ac ground, so that the nFET processes the signal at its source as a CG

amplifier. Therefore, each input terminal affects both output terminals, in such a way that the signal voltages sum at the output of the LNA. This process is outlined in Figure 4.7.

The half-circuit differential voltage gain (arbitrarily choosing $v_{in,(-)}$ as the input reference), can be expressed as:

$$A_{v_{\frac{1}{2}}diff} = \frac{v_{o,(+)} - v_{o,(-)}}{v_{in,(-)}} \tag{4.48}$$

which is split into:

$$A_{v_{\frac{1}{2}}diff} = \left(\frac{v_{o,(+)}}{v_{in,(-)}}\right) - \left(\frac{v_{o,(-)}}{v_{in,(-)}}\right) \tag{4.49}$$

The first term of (4.49) is determined by analyzing the half-circuit of Figure 4.4 to obtain (V_o/V_x). Resolving the KCL equation for node V_o, but substituting i_x with $((V_x-V_o)/R_F)$ shows:

$$0 = \frac{V_o}{R_p} + g_{m,n}v_{gs} + \frac{V_o - V_x}{R_F} \tag{4.50}$$

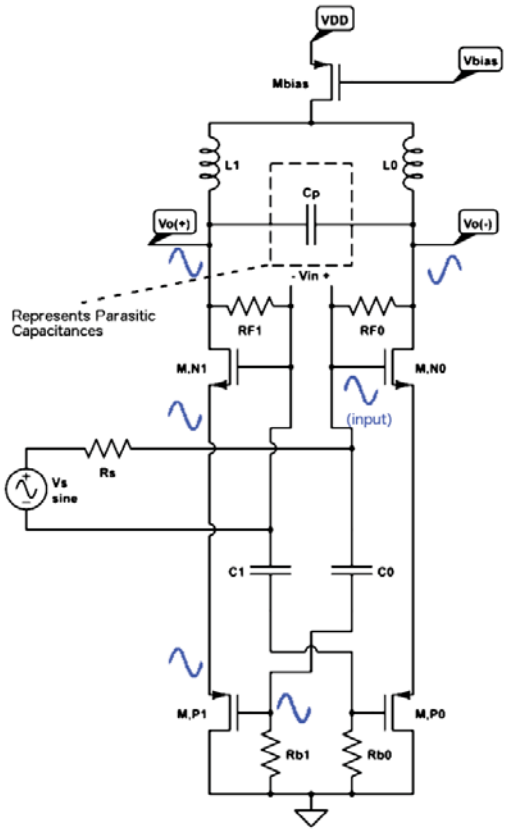

Figure 4.7 Differential Signals Paths for Half-Circuit PNC LNA

Manipulation of (4.50), using (4.43) for v_{gs}, and the condition that all transconductances are equal gives:

$$\frac{V_o}{V_x} = \frac{\left[1 - \frac{g_{m,n}R_F}{2}\right]}{\left[1 + \frac{R_F}{R_p}\right]} \tag{4.51}$$

Assuming $R_p >> R_F$ simplifies (4.51) to:

$$\frac{V_o}{V_x} = 1 - \frac{(g_{m,n}R_F)}{2} \tag{4.52}$$

Assuming $(g_{m,n}R_F / 2) >> 1$, the first term of (4.49) can be approximated as:

$$\frac{V_o}{V_x} = v_{o,(+)}/v_{in,(-)} \approx -\frac{g_{m,n}R_F}{2} \tag{4.53}$$

Determining the second term of (4.49) is done by analyzing the following small signal model to obtain $v_{o,(-)}/v_{in,(-)}$, shown in Figure 4.8.

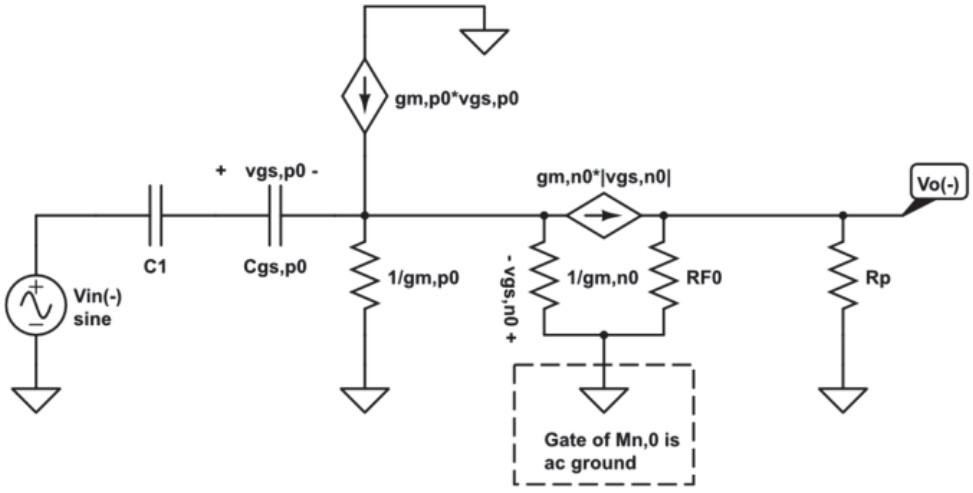

Figure 4.8 Small Signal Model to Obtain $v_{o,(-)} / v_{in,(-)}$ of PNC LNA

Assuming $R_p >> R_{F,0}$, the output voltage $V_{o,(-)}$ in the above figure can be expressed as:

$$V_{o,(-)} = g_{m,n1}|v_{gs,n1}|R_{F,1} \tag{4.54}$$

The voltage $v_{gs,n1}$ is the result of the current $g_{m,p0}v_{gs,p0}$ flowing through the equivalent impedance of $(1/g_{m,p0} \,//\, 1/g_{m,n0})$. Since $v_{gs,p0}$ is $v_{in,(-)}$ and $g_{m,p0} = g_{m,n0}$, (4.54) becomes:

$$V_{o,(-)} = g_{m,n1}\left(\frac{1}{2}\right)v_{in,(-)}R_{F,1} \tag{4.55}$$

which leads to:

$$\frac{V_{o,(-)}}{v_{in,(-)}} = \left(\frac{1}{2}\right)g_{m,n1}R_{F,1} \tag{4.56}$$

Expressing (4.49) as the difference of (4.53) and (4.56) and assuming perfect matching among the active devices gives the half-circuit differential voltage gain, $A_{v,1/2diff}$ as:

$$A_{v,\frac{1}{2}diff} = \left(\frac{V_{o,(+)}}{v_{in,(-)}}\right) - \left(\frac{V_{o,(-)}}{v_{in,(-)}}\right) = -\left(\frac{1}{2}\right)g_{m,n0}R_{F,0} - \left(\frac{1}{2}\right)g_{m,n1}R_{F,1} = -g_{m,n}R_F \tag{4.57}$$

Due to symmetry, the fully differential voltage gain $A_{v,diff}$ for this LNA can be expressed as:

$$A_{v,diff} = 2(|A_{v,\frac{1}{2}diff}|) = 2g_mR_F \tag{4.58}$$

When connected to a matched source, the gain of (4.58) halves to:

$$A_{V_s} = \frac{v_{o,diff}}{V_s} = g_mR_F \tag{4.59}$$

The differential output impedance $Z_{o,diff}$ of this PNC LNA is twice the output impedance of the half-circuit of Figure 4.6 and designing such that $R_F << R_p$ approximates $Z_{o,diff}$ as:

$$Z_{o,diff} = 2Z_{o,\frac{1}{2}} = 2(R_p//R_{F,0}) = 2R_F \tag{4.60}$$

Expressions (4.46), (4.59), and (4.60) express the approximate midband power gain of this PNC LNA with respect to V_s:

$$G_p = (A_{V_s})^2\left(\frac{Z_{in,diff}}{Z_{o,diff}}\right) = 8g_mR_F \tag{4.61}$$

Noise Figure

Figure 4.9 is the midband thermal noise model for the PNC LNA, and assumes a noiseless reactive load. Also, the noise originating from the resistors $R_{b,0}$ and $R_{b,1}$ have been omitted, since these noise current appear at virtual ground.

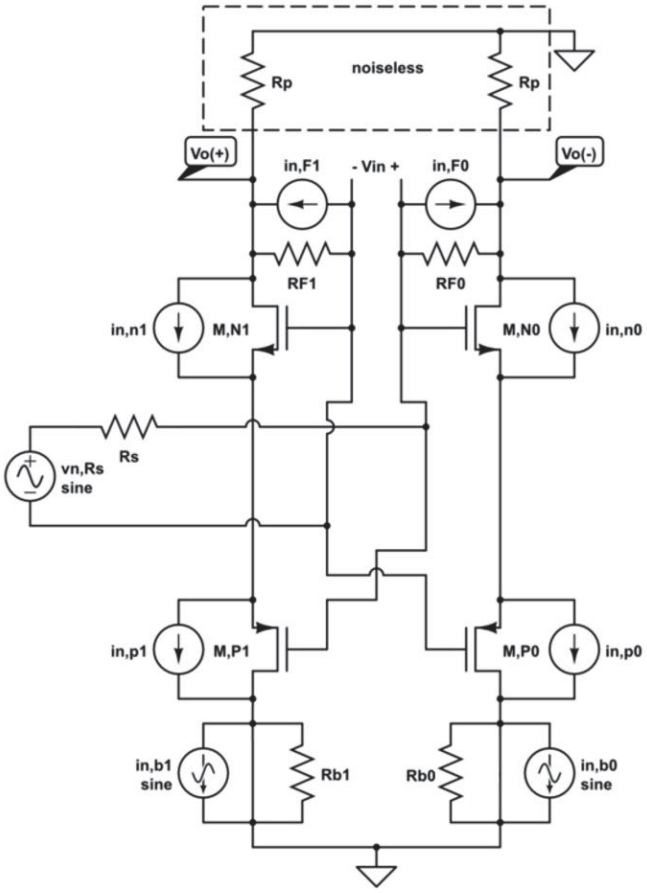

Figure 4.9 Midband Thermal Noise Model of PNC LNA

The transfer function of the noise voltage of the source impedance $v_{n,Rs}$ is identical to that of the source voltage V_s. So, the differential output noise voltage due to the R_s is:

$$v_{No,R_s} = \left(\frac{1}{2}\right) v_{n,R_s}(2g_m R_F) \tag{4.62}$$

which is dropped over the load described in (4.60). The corresponding output spectral noise power contribution is:

$$P_{No,R_s} = \frac{(v_{No,R_s})^2}{Z_{o,diff}} = 4kTR_s(R_F(g_m)^2) \tag{4.63}$$

The noise power contributions due to the nFETs $M_{N,0}$ and $M_{N,1}$ are identical, due to symmetry. To obtain these expressions, a similar approach to (4.49) is used: the differential

output noise voltage due to each nFET is determined, first by computing the noise voltage at the output terminal of opposite polarity, and then by computing the noise voltage at the output terminal of the same polarity. Figure 4.10 is useful in performing the former. A similar approach is used to determine the noise contributions due to the pFETs.

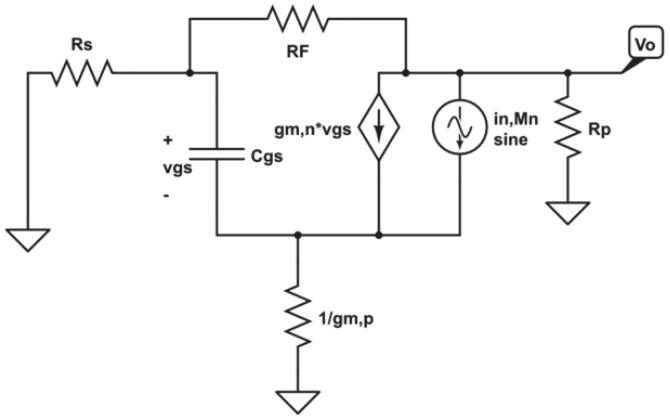

Figure 4.10 Half-Circuit Small Signal Model used to Obtain nFET Noise Contributions

Solving the KCL equation at the node labeled V_o results in:

$$0 = \frac{V_o}{R_p} + \frac{V_o - v_G}{R_F} + g_{m,n} v_{gs} + i_{n,Mn} \tag{4.64}$$

Next, solving and rearranging the KCL equations for the gate and source nodes in Figure 4.8 gives the following two expressions ((4.65) and (4.66), respectively):

$$v_G = V_o \left(\frac{R_s}{R_s + R_F}\right) \tag{4.65}$$

$$v_S = \left(\frac{1}{2}\right)\left[i_{n,Mn}\left(\frac{1}{g_{m,p}}\right) + V_o\left(\frac{R_s}{R_s + R_F}\right)\right] \tag{4.66}$$

which allows for v_{gs} of (4.64) to be expressed as:

$$v_{gs} = \left(\frac{1}{2}\right) V_o \left(\frac{R_s}{R_s + R_F}\right) \tag{4.67}$$

Now, assuming V_o/R_p is negligible and all FET transconductances equal, (4.64) can be rearranged as:

$$V_o\left[1 - \frac{R_s}{R_s + R_F} + \left(\frac{1}{2}\right) g_m (R_F // R_s)\right] = -\left(\frac{1}{2}\right) i_{n,Mn} R_F \tag{4.68}$$

Designing such that $R_F >> R_s$ allows:

$$V_o\left[1 + \left(\frac{1}{2}\right) g_m R_s\right] = -\left(\frac{1}{2}\right) i_{n,Mn} R_F \tag{4.69}$$

which reveals:

$$V_o = \frac{\left[-\left(\frac{1}{2}\right) i_{n,Mn} R_F\right]}{1 + \left(\frac{1}{2}\right) g_m R_s} \tag{4.70}$$

Due to the impedance matching condition of $2/g_m = R_s$, it is trivial to show $(^1/_2) g_m R_s = 1$. Now, (4.70) becomes:

$$V_o = -\left(\frac{1}{4}\right) i_{n,Mn} R_F \tag{4.71}$$

Where $i_{n,Mn}$ is the thermal channel noise current of the nFET under consideration. In this analysis, (4.71) expresses both the noise voltage at the positive output terminal due to $M_{N,1}$'s thermal noise and the noise voltage at the negative output terminal due to $M_{N,0}$'s thermal noise, due to symmetry.

Figure 4.11 is used to determine the output noise voltage of the nFETs that occurs due to the cross-coupling capacitors C_0 and C_1. In the figure, these capacitors are assumed to be short circuits, and the tuned load impedance R_p is considered to be an open circuit at midband operation. The node labeled v_N represents the source terminal of the cross-coupled pFET introducing the noise from the input nFET of the other half-circuit. This node is shared with the source terminal of the other input nFET. The voltage at this node is one-half of the voltage that is fed back from the other half-circuit's feedback resistor, R_F. The midband transfer function between the gate of $M_{N,0}$ (or $M_{N,1}$) to the source terminal of $M_{p,1}$ (or $M_{p,0}$), i.e. node v_N of Figure 4.9, is equivalent to a pFET CD amplifier with a load impedance of $^1/g_{m,n}$ and is written as:

$$\frac{v_{G,No}}{v_{S,P1}} = \frac{1}{1 + g_{m,p1}(g_{m,n1})^{-1}} = \frac{1}{2} \tag{4.72}$$

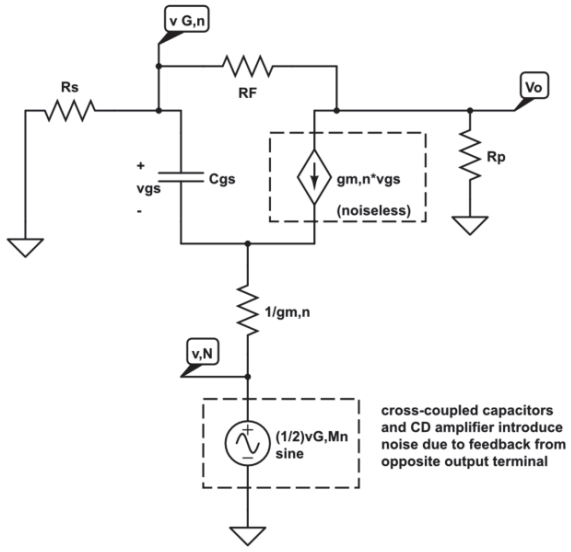

Figure 4.11 Second Half-Circuit Model used to Obtain nFET Noise Contributions

The voltage $v_{G,N0}$ is a portion of the output noise that appears at $v_{o,(-)}$ in Figure 4.7. Due to the presence of R_s, the gate terminal of each input resistor sees some impedance to ac ground. In the case where $R_p >> (R_F + R_s)$, the voltage $v_{G,N0}$ is the result of a voltage divider consisting of R_F and R_s:

$$v_{G,N0} = v_{o,(-)}\left[\frac{R_s}{R_s + R_{F,o}}\right] \tag{4.73}$$

Therefore, the voltage labeled v_N of the generic half-circuit in Figure 4.9 can be expressed as:

$$v_N = \left(\frac{1}{2}\right) v_{G,Mn} \tag{4.74}$$

Where $v_{G,N0}$, a fraction of $v_{o,(-)}$ as described in (4.71), is:

$$v_{G,N0} = -\left(\left(\frac{1}{4}\right) i_{n,Mn} R_F\right)\left[\frac{R_s}{R_s + R_{F,o}}\right] \tag{4.75}$$

Solving the KCL equation at the gate terminal in the generic half-circuit of Figure 4.9 resolves:

$$v_{G,n} = V_o\left(\frac{R_s}{R_s + R_F}\right) \tag{4.76}$$

Next, solving the KCL equation at the node labeled V_o gives:

$$V_o = -(R_s + R_F)(g_{m,n} v_{gs}) \tag{4.77}$$

v_{gs} can be expressed as the difference between the gate voltage of (4.76) and the voltage at the source terminal, noted in (4.74). This results in:

$$v_{gs} = \left(\frac{1}{2}\right)\left(v_{G,n} - v_N\right) \tag{4.78}$$

Expressing (4.77) in terms of (4.74), (4.76), and (4.78) gives the noise voltage of the output terminal (V_o node of Figure 4.9) due to noise originating from the channel of the input nFET of the same polarity, and is shown in (4.79):

$$V_o = v_{G,N0}\left[\frac{\left(\frac{1}{2}\right)(R_s + R_F)g_{m,n}}{1+\frac{(g_m R_s)}{2}}\right] = \left(\frac{1}{2}\right)\left[-\left(\frac{1}{4}\right) i_{n,Mn} R_F\right] \tag{4.79}$$

Where $i_{n,Mn}$ is the same as in expression (4.71). Since $v_N = (1/2)v_{G,N}$, the half-circuit transfer function between noise that appears at node v_N and the voltage V_o of Figure 4.9 can be written as:

$$\frac{V_o}{v_N} = \frac{\left[(R_s + R_F)g_{m,n}\right]}{\left[1 + \left(\frac{1}{2}\right)g_m R_s\right]} \tag{4.80}$$

Since the gate of the nFET is not at ac ground, but instead is fed back some portion of V_o of (4.79), its corresponding cross-coupling capacitor will transfer this fed back signal to the gate of the pFET of the half-circuit from which the noise voltage source in Figure 4.9 originates. A transfer function between V_o and the output terminal of opposite polarity can be obtained by solving the following:

$$\left(\frac{v_{G,n}}{V_o}\right)\left(\frac{v_N}{v_{G,Mn}}\right)\left(\frac{V_{o,opp}}{v_N}\right) = \frac{V_{o,opp}}{V_o} \tag{4.81}$$

Where $V_{o,opp}$ is the output terminal *not* represented in Figure 4.9. Solving for (4.81) results in:

$$\frac{V_{o,opp}}{V_o} = \left(\frac{1}{2}\right)\left(\frac{R_s}{R_s + R_F}\right)\left[\left(\frac{1}{2}\right)(R_s + R_F)g_m\right] \tag{4.82}$$

Since $(1/2)g_m R_s$ reduces to unity, (4.82) is simplified as:

$$\frac{V_{o,opp}}{V_o} = \left(\frac{1}{2}\right) \tag{4.83}$$

Superimposing $V_{o,opp}$ onto the voltage established in (4.71) for the half-circuit of Figure 4.7 gives the total noise voltage at the negative (or positive) output terminal due to the input FET M_0 (or M_1) as:

$$v_{o,(+)} = \left[-\left(\frac{1}{4}\right) i_{n,N0} R_F\right]\left(1 + \left(\frac{1}{2}\right)^2\right) \tag{4.84}$$

Simplifying the difference between (4.84) and (4.79) gives the differential output noise voltage due to either input nFET:

$$v_{on,diff} = -\left(\frac{3}{16}\right) i_{n,Mn} R_F \tag{4.85}$$

The noise due to the pFETs that appear in series with the input FETs is analyzed next. Similar to the process above, first Figure 4.11 will be used to determine the noise voltage that appears on the output terminal of the same half-circuit as the offending pFET. Next, the noise that appears on the opposite output terminal due to the feedback resistors R_F and the cross-coupling capacitors is calculated. Then, the portion of this voltage that appears back on the original output terminal of interest is determined and superimposed. Then, the differential output noise voltage due to each pFET can be known, due to symmetry.

Figure 4.11 can be used to obtain the output noise voltage $v_{o,(-)}$ (or $v_{o,(+)}$) due to $M_{p,0}$ (or $M_{p,1}$) by using a different noise term for v_N. The voltage that appears on this node is due to the pFET's channel noise current flowing through the equivalent impedance established by the source resistances of nFET/pFET pair combining in parallel. Assuming all FETs have matched transconductances, v_N is:

$$v_N = \left(\frac{1}{2}\right)\left(\frac{1}{g_m}\right) i_{n,Mp} \tag{4.86}$$

Due to the matching condition, (4.80) can be resolved to:

$$\frac{V_o}{v_N} = \left(\frac{1}{2}\right)\left[(R_s + R_F) g_{m,n}\right] \tag{4.87}$$

Which implies the half-circuit output noise voltage V_o is:

$$V_o = \left(\frac{1}{2}\right)^2 \left(\frac{1}{g_m}\right) i_{n,Mp}\left[(R_s + R_F) g_{m,n}\right] \tag{4.88}$$

Using the approximation of (4.83) gives the noise voltage that appears on the output terminal of opposite polarity, due the feedback and cross-coupling of the noise of (4.88):

$$V_{o,opp} = \left(\frac{1}{2}\right) V_o = \left(\frac{1}{2}\right)^3 \left(\frac{1}{g_m}\right) i_{n,Mp}\left[(R_s + R_F) g_{m,n}\right] \tag{4.89}$$

Since the voltage established in (4.89) is processed symmetrically as that of (4.88), a portion of it will also appear on the opposite output terminal, and will be superimposed on (4.88). This portion can be expressed using Figure 4.9, establishing the voltage for v_N:

$$\frac{v_N}{V_{o,opp}} = \left(\frac{1}{2}\right)\left[\frac{R_s}{R_s + R_F}\right] \tag{4.90}$$

Now, the total voltage of node V_o (due to (4.88) summed with noise originating in (4.90)) of Figure 4.9, can be written as V_o', using the transfer function of (4.87), as:

$$V_o' = V_o + v_N\left(\frac{V_o}{v_N}\right) = \left(\frac{5}{16}\right) i_{n,Mp}(R_s + R_F) \tag{4.91}$$

Subtracting (4.89) from (4.91) results in the differential output noise voltage due to each individual pFET:

$$v_{op,diff} = V_o' - V_{o,opp} = i_{n,Mp}(R_s + R_F)\left[\left(\frac{5}{16}\right) - \left(\frac{1}{2}\right)^3\right] \tag{4.92}$$

Applying the matching condition where $(g_m/2) = (1/R_s)$, assuming $R_F/R_s >> 1$, and considering $(1/18)$ of negligible consequence allows:

$$v_{op,diff} = \left(\frac{3}{16}\right) i_{n,Mp}(R_s + R_F) \tag{4.93}$$

The noise due to the feedback resistors $R_{F,0}$ and $R_{F,1}$ can be determined by analyzing the small-signal half-circuit in Figure 4.12. Within, the noise current due to R_F is shown, as well as the corresponding output terminal. First, the voltage V_o is found. Then, the voltage of the opposite output terminal $V_{o,opp}$ and the portion of this superimposed onto V_o are expressed. Then, the total differential output voltage due to the noise current of each individual feedback resistor is approximated.

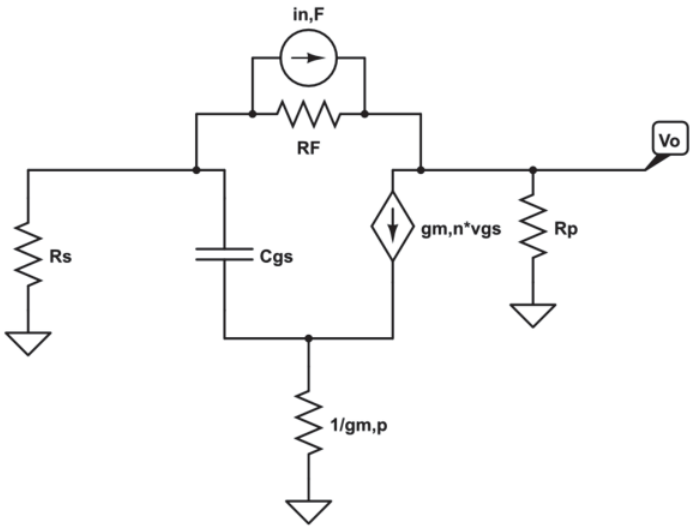

Figure 4.12 Small-Signal Model used to Determine Noise of Feedback Resistors

Solving KCL equations for the node labeled V_o, the gate terminal, and the source terminal result in the following three equations, respectively:

$$0 = -i_{n,F} + \frac{V_o + v_G}{R_F} + g_{m,n} v_{gs} \tag{4.94}$$

$$v_G = V_o \left[\frac{R_s}{R_s + R_F}\right] \tag{4.95}$$

$$v_S = \left(\frac{1}{2}\right) v_G \tag{4.96}$$

Expressing (4.94) in terms of (4.95) and (4.96) and assuming $R_s/R_F << 1$ results in:

$$V_o = i_{n,F} R_F \tag{4.97}$$

The output voltage of the opposite output terminal due to (4.97) is found by first finding the noise voltage v_N that appears at the source terminal of the input nFET of corresponding polarity. This voltage v_N is:

$$v_N = \left(\frac{1}{2}\right)\left(\frac{R_s}{R_s + R_F}\right) V_o \tag{4.98}$$

Using (4.87) and $(g_m R_s) = 2$ approximates the opposite output terminal's noise voltage due to (4.98) as:

$$V_{o,opp} = v_N\left[\left(\frac{1}{2}\right)\left[(R_s + R_F)g_m\right]\right] = \left(\frac{1}{2}\right) i_{n,F} R_F \tag{4.99}$$

Which causes an imposition (defined by (4.83)) onto V_o resulting in V_o':

$$V_o' = V_o + \left(\frac{1}{2}\right) V_{o,opp} = i_{n,F} R_F \left[1 + \left(\frac{1}{2}\right)^2\right] \tag{4.100}$$

The difference between (4.100) and (4.99) give the total differential output noise voltage due to each individual feedback resistor, described by R_F, as:

$$v_{oF,diff} = \left(\frac{3}{4}\right) i_{n,F} R_F \tag{4.101}$$

The noise figure may now be found in terms of the individual noise contributions from all noisy components of Figure 4.7. The total output noise due to both nFETs is:

$$P_{oN,M_n} = kTB\left[\left(\frac{3}{16}\right)^2 \left(\frac{8}{3}\right) g_{m,n} R_F\right] \tag{4.102}$$

The total output noise due to both pFETs is:

$$P_{oN,M_n} = kTB\left[\left(\frac{3}{16}\right)^2 \left(\frac{8}{3}\right) g_{m,n}(R_s + R_F)\right] \tag{4.103}$$

The total output noise due to the feedback resistors is:

$$P_{oN,R_F} = kTB\left[4\left(\frac{3}{4}\right)^2\right] \tag{4.104}$$

Lastly, the total output noise due to the source expressed in (4.63), can be simplified as:

$$P_{oN,R_s} = kTB\left[8 g_{m,n} R_F\right] \tag{4.105}$$

The total output noise current due to all the noisy elements, written as the sum of (4.102) through (4.105), is:

$$P_{oN,Tot} = kTB[8 g_{m,n} R_F + \left(\frac{3}{16}\right)^2 \left(\frac{8}{3}\right) g_{m,n} R_F + \left(\frac{3}{16}\right)^2 \left(\frac{8}{3}\right) g_{m,n}(R_s + R_F) + 4\left(\frac{3}{4}\right)^2] \tag{4.106}$$

The noise figure is calculated by dividing the total output noise power in (4.106) by the output noise power due only to the source in (4.105), and is expressed as:

$$F = \frac{8 g_{m,n} R_F + \left(\frac{3}{16}\right)^2 \left(\frac{8}{3}\right) g_{m,n} R_F + \left(\frac{3}{16}\right)^2 \left(\frac{8}{3}\right) g_{m,n}(R_s + R_F) + 4\left(\frac{3}{4}\right)^2}{8 g_{m,n} R_F} \tag{4.107}$$

The NF expressed in (4.107) becomes:

$$F = 1 + \frac{\left(\frac{s}{16}\right)^2\left(\frac{s}{s}\right)g_{m,n}R_F + \left(\frac{s}{16}\right)^2\left(\frac{s}{s}\right)g_{m,n}(R_s+R_F)+4\left(\frac{s}{4}\right)^2}{8g_{m,n}R_F} \tag{4.108}$$

Applying the matching identity of $2/g_m = R_s$ and simplifying results in:

$$F \approx \left(1 + \frac{171}{5248}\right) + \left[\frac{\left(\frac{9}{16}\right)}{g_m R_F}\right] \tag{4.109}$$

The expression of (4.109) represents the minimum theoretical midband noise figure for the PNC LNA of Figure 4.5. When $g_m R_F$ is much greater than one, the minimum NF is .03 dB. Note that the NF of (4.109) relies requires $R_F >> R_s$, and has ignored many second order effects in the FET models such as gate-source capacitance and series gate resistance so that higher NF values can be expected at high frequency.

Large Signal Parameters

As with the S-L LNA described in the previous section, the input FETs will begin to compress when they no longer operate in active mode. This happens when the instantaneous voltage on their gates, which are the sums of their respective dc bias voltages and ac input voltages, drops below the threshold voltage of the device, V_{th}. Due to the differential topology, only half of the LNA's input voltage $v_{in,diff}$ (not to be confused with V_s) is superimposed on each nFET's gate. Therefore, the maximum input voltage corresponds to when its peak value is equal to twice the overdrive voltage, which is identical on each nFET. This implies that the maximum input power before compression is:

$$P_{in,max} = \frac{(2v_{ov})^2}{z_{in}} = \frac{4(v_{ov})^2}{\frac{4}{g_m}} = \frac{2(v_{ov})^2}{R_s} = (v_{ov})^2 g_m \tag{4.110}$$

As with the S-L LNA of the previous section, compression will occur at the output when the output voltage attempts to exceed twice that of the supply, which is an improvement over the original design in [1]. Again, this is because of the energy storing mechanisms of a reactive load. When this is the case, the maximum input power to this LNA can be estimated as:

$$P_{in,max} = \frac{(\frac{v_{o,diff,max}}{A_{v,diff}})^2}{Z_{in,diff}} = \frac{(\frac{1}{4})(VDD)^2}{R_F} \quad (4.111)$$

In practice, the minimum between (4.110) and (4.111) sets the maximum input power before compression, and thus distortion of the output signal. Again, these powers are considered at the input terminals of the PNC LNA, not from the terminals between source voltage V_s and ground.

4.2 2.4-GHz CMOS Low Noise Amplifier Implementations

4.2.1 Source-Inductor Low Noise Amplifier

Figure 4.13 shows a simplified schematic of the S-L LNA that was implemented in the .180µ CMOS process. The tuned load consists of C_T, L_T, and the parasitic capacitances of the drain of M_1 and the buffers of the following stage (not shown) and resonates at ~2.4 GHz. C_{byp} provides on-chip bypass capacitance for the power supply, and C_{byp2} implements the ac ground node for the cascode transistor. L_s is the source inductor that resonates with the capacitance of the input FET M_0's gate-source capacitance.

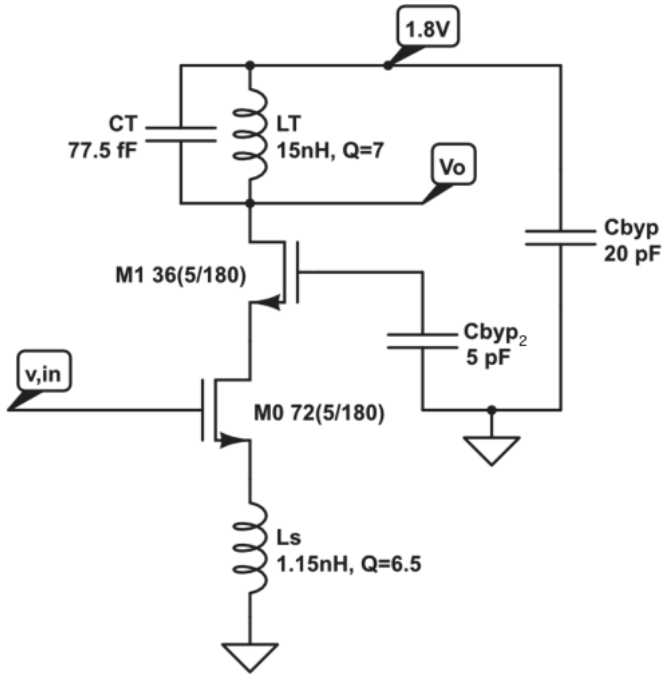

Figure 4.13 Simplified Schematic of Implemented S-L LNA

A schematic and layout of this S-L LNA, as implemented in Cadence Virtuoso ICFB, follow in Figures 4.14 and 4.15.

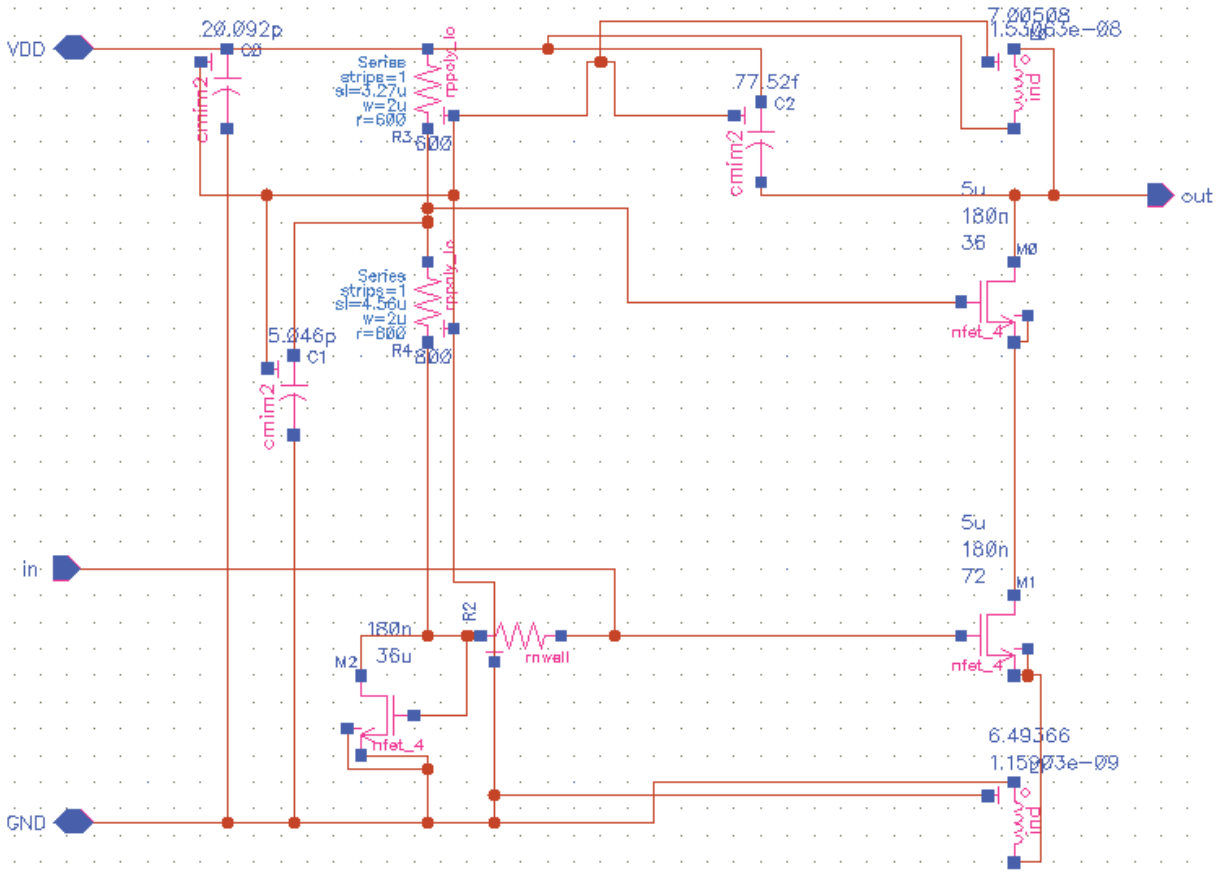

Figure 4.14 Schematic of Implemented S-L LNA using Cadence Virtuoso ICFB

Not shown in Figure 4.14 or 4.15 is the schematic/layout of the buffer stages that follow. These buffers were implemented in order to measure the output signals of both LNAs directly using a spectrum analyzer. In order to keep their input capacitance low, an exponential buffer chain was used, consisting of three stages. Simulation results included later in this thesis for both the S-L and PNC LNAs include the effect of loading from these buffers, which drive 50Ω load impedances. With a supply voltage VDD of 1.8V and a nominal dc current of 8mA, the S-L

LNA of Figure 4.12 consumes 14.4 mW of dc power. The schematic and layout of these buffers can be found in Appendix A.

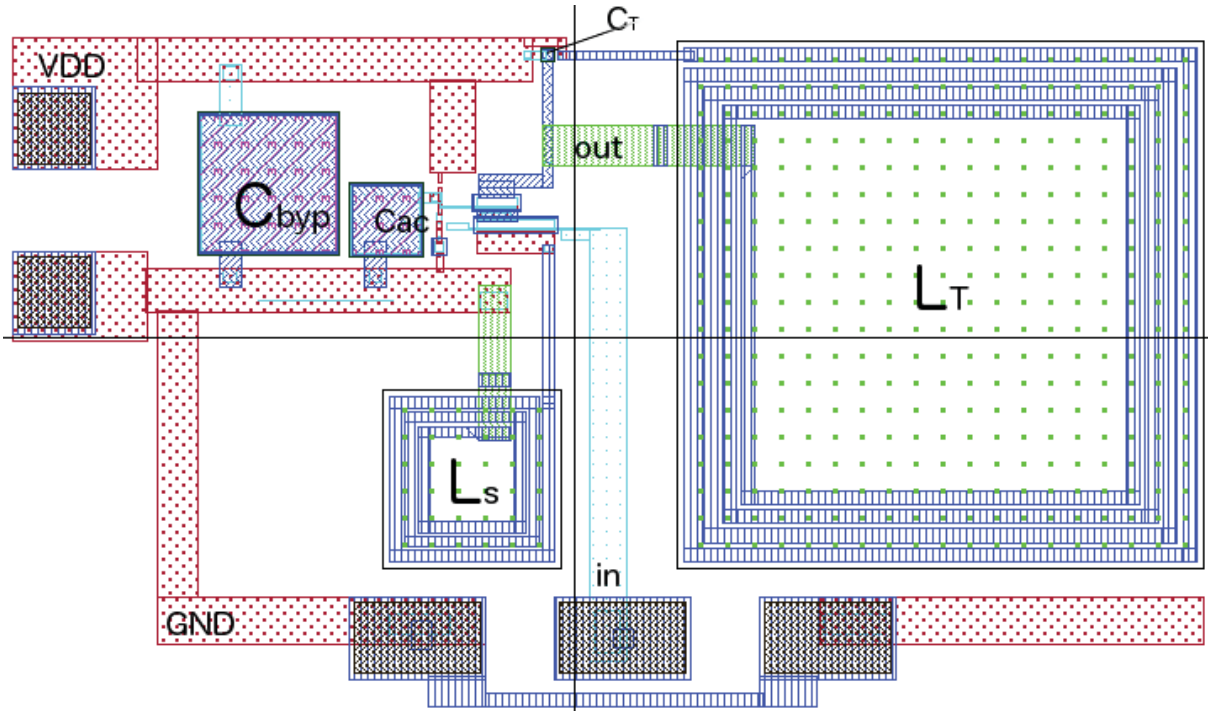

Figure 4.15 Annotated Layout of Implemented S-L LNA using Cadence Virtuoso ICFB

4.2.2 Partial Noise Cancelling Low Noise Amplifier

Figure 4.16 below shows a simplified schematic of the PNC LNA implemented in CMOS. The tuned load's inductance consists of L_0 and L_1, which are *15.3 nH* each with a quality factor of *7.0*, consistent with the S-L LNA implementations. These components resonate at ~2.4 GHz with the parasitic capacitances introduced by the nFETs $M_{N,0}$ and $M_{N,1}$, as well as the gate capacitance of the FETs acting as inputs to the buffers, which are not shown in Figure 4.16. The feedback resistors $R_{F,0}$ and $R_{F,1}$ are *4 kΩ* each and provide the feedback that allows the input to modify its input impedance. The cross-coupling capacitors C_0 and C_1 are *9.8 pF* each, and are intended to be low-impedance paths at ~2.4 GHz. The series pFETs $M_{P,0}$ and $M_{P,1}$ have

much wider than their nFET counterparts, since the ratio of the process transconductances is approximately 4 in the process used. These pFETs are biased into the active region using the *10 kΩ* resistors $R_{b,0}$ and $R_{b,1}$.

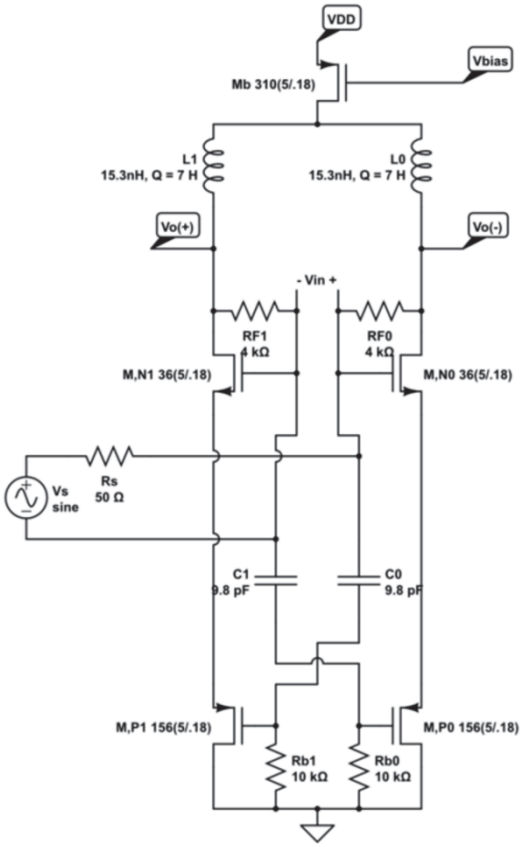

Figure 4.16 Simplified Schematic of Implemented PNC LNA

A detailed schematic and layout of this PNC LNA, as implemented in Cadence Virtuoso, follow in Figures 4.17 and 4.18.

As with the S-L LNA, not shown in Figure 4.17 or 4.18 is the schematic/layout of the buffer stages that follow. With a supply voltage VDD of 1.8V and a nominal dc current of 8.4mA, the PNC LNA of Figure 4.18 consumes 15.1 mW of dc power. The schematic and layout of the buffers can be found in Appendix A.

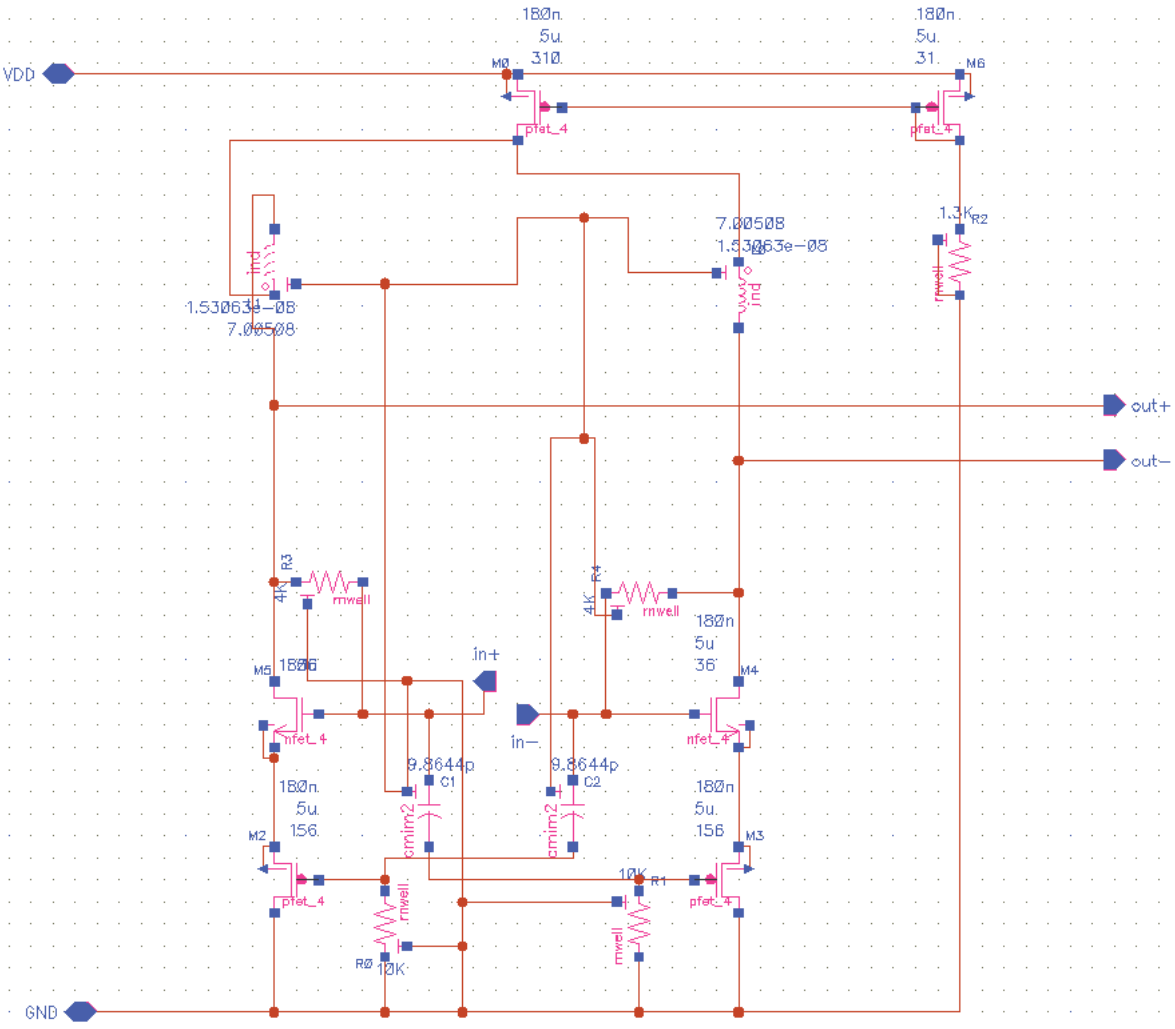

Figure 4.17 Schematic of Implemented PNC LNA using Cadence Virtuoso ICFB

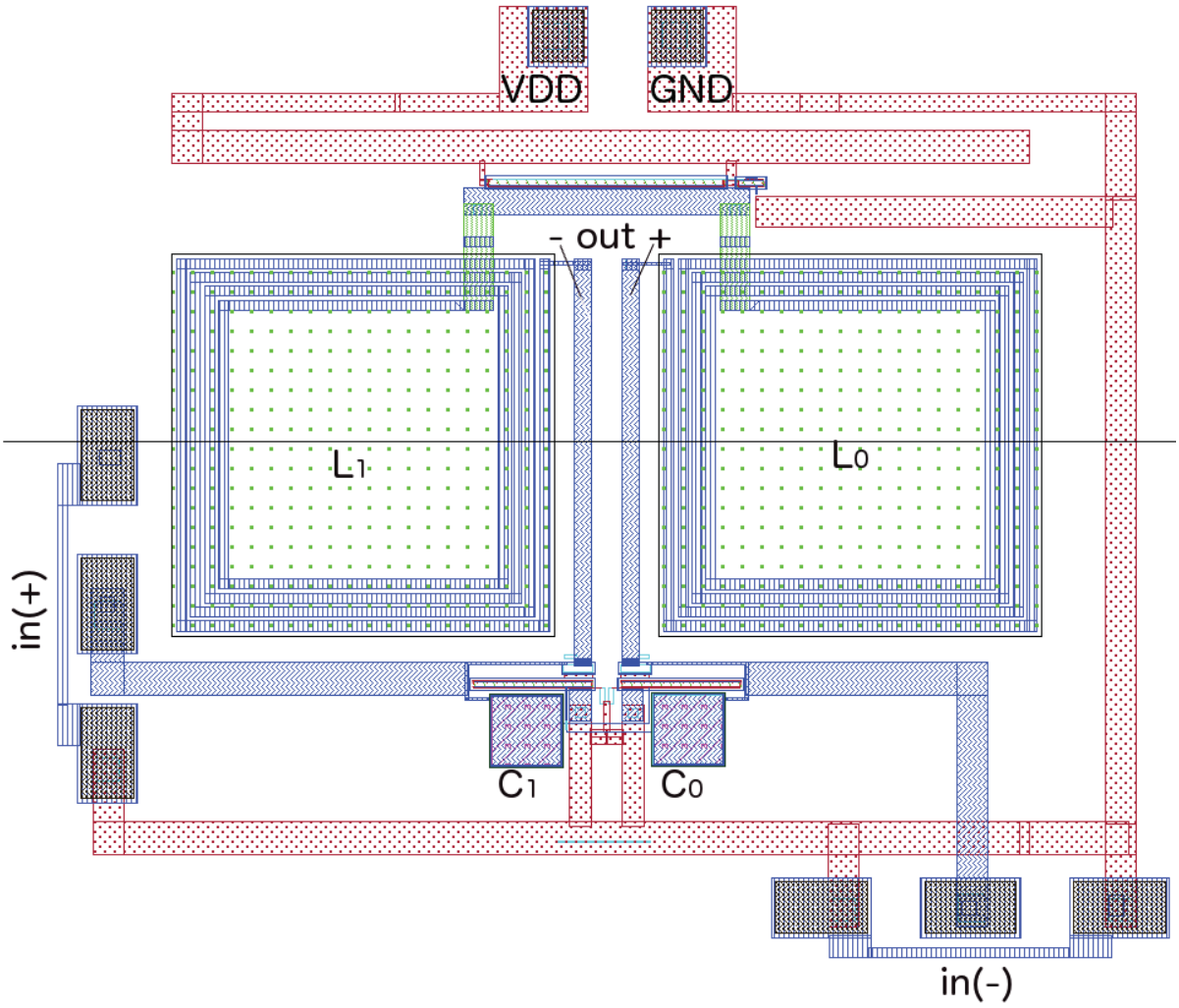

Figure 4.18 Annotated Layout of Implemented PNC LNA using Cadence Virtuoso ICFB

4.3 Performance of Low Noise Amplifiers

Cadence Virtuoso was used to simulate the dc node voltages and currents, ac voltage gain, ac input impedance, and output noise voltage of both the S-L and PNC LNAs. Simulation results in the form of plots and annotated schematics are reported for both LNA types. In addition to this, "testbench" schematics are included, used to replicate a "true" RF receiver frontend environment.

The testbench environment is intended to provide the following signal environment:

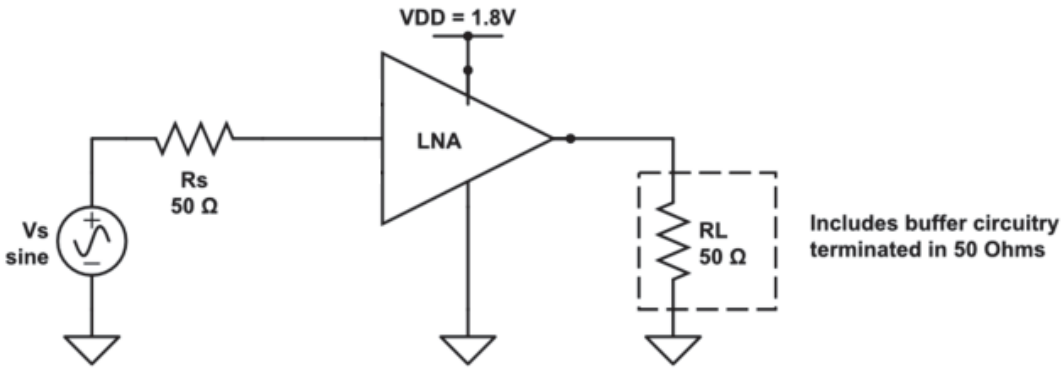

Figure 4.19 Simulated LNA "Testbench" Environment

For an LNA in the environment described by Figure 4.19, the following expression may be used to deduce the noise figure in dB:

$$NF_{dB} = F_{dB} = 20log\left[\frac{v_{n,out}}{A_v v_{n,s}}\right] \quad (4.112)$$

Where $v_{n,out}$ is the noise voltage at the output of the LNA, $v_{n,s}$ is the noise voltage at the input of the LNA due to the source resistance R_s, $(1/2)\sqrt{(4kTBR_s)}$, and $A_{v,l}$ is the "loaded" voltage gain of the LNA. The expression of (4.112) is useful when taking direct measurements of $v_{n,out}$ and $A_{v,l}$ from an LNA in a laboratory setting.

4.3.1 Source-Inductor Low Noise Amplifier

Figure 4.20 below shows the ICFB schematic of the S-L LNA, along with annotated dc voltages and currents. Note that the symbol named "K0" represents magnetic coupling between the two inductors, with a coupling coefficient of $k = -0.2$.

Figure 4.20 reports the drain current of M_1, which provides the dc biasing current in addition to acting as the input FET, as 8.2 mA. With a voltage supply of 1.8 V, this implies a power consumption of 14.8 mW.

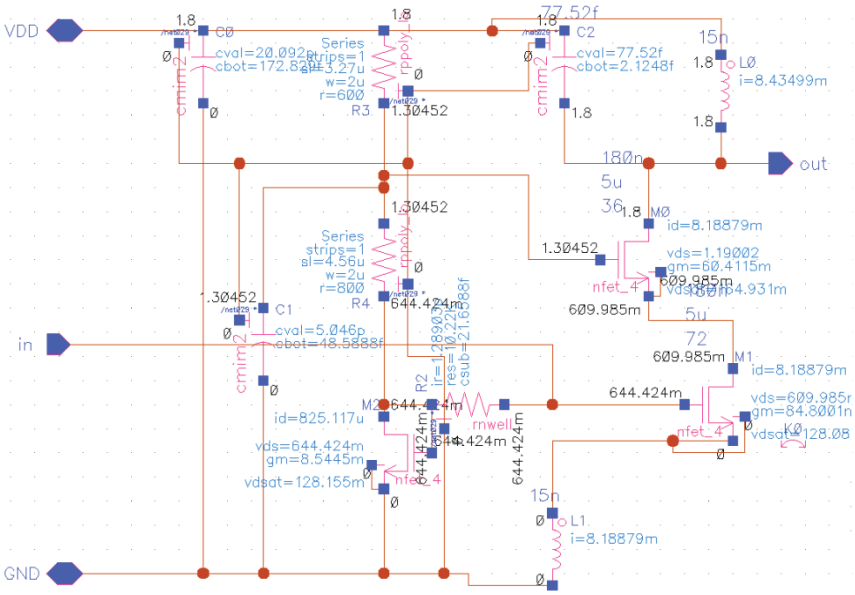

Figure 4.20 Annotated Layout of Implemented S-L LNA using Cadence Virtuoso ICFB

To simulate the voltage gain, the following testbench environment was used:

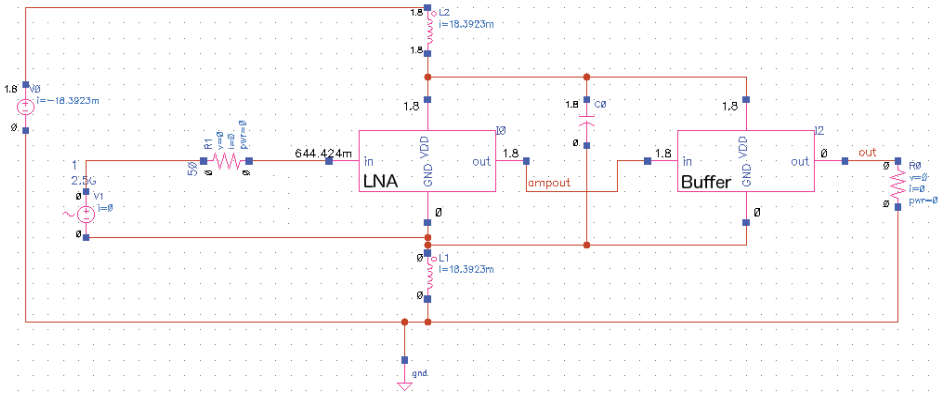

Figure 4.21 Testbench Schematic of S-L LNA using Cadence Virtuoso

From Figure 4.21 it can be seen that the total dc current consumption is roughly 18 mA. This is because the buffer circuitry, symbolized by the rectangle whose output is terminated in 50Ω, consumes 10 mA of current while the LNA preceding consumes 8.2 mA.

The voltage gain, in $^{V}/_{V}$ and *dB*, is shown in the plot below of Figure 4.22. This plot shows that the resonant frequency of the tuned load is closer to 2.81 GHz, including the parasitic capacitance introduced by the input FET of the buffer. The voltage gain of this S-L LNA at 2.81 GHz is 19.3 $^{V}/_{V}$, or 25.7 dB.

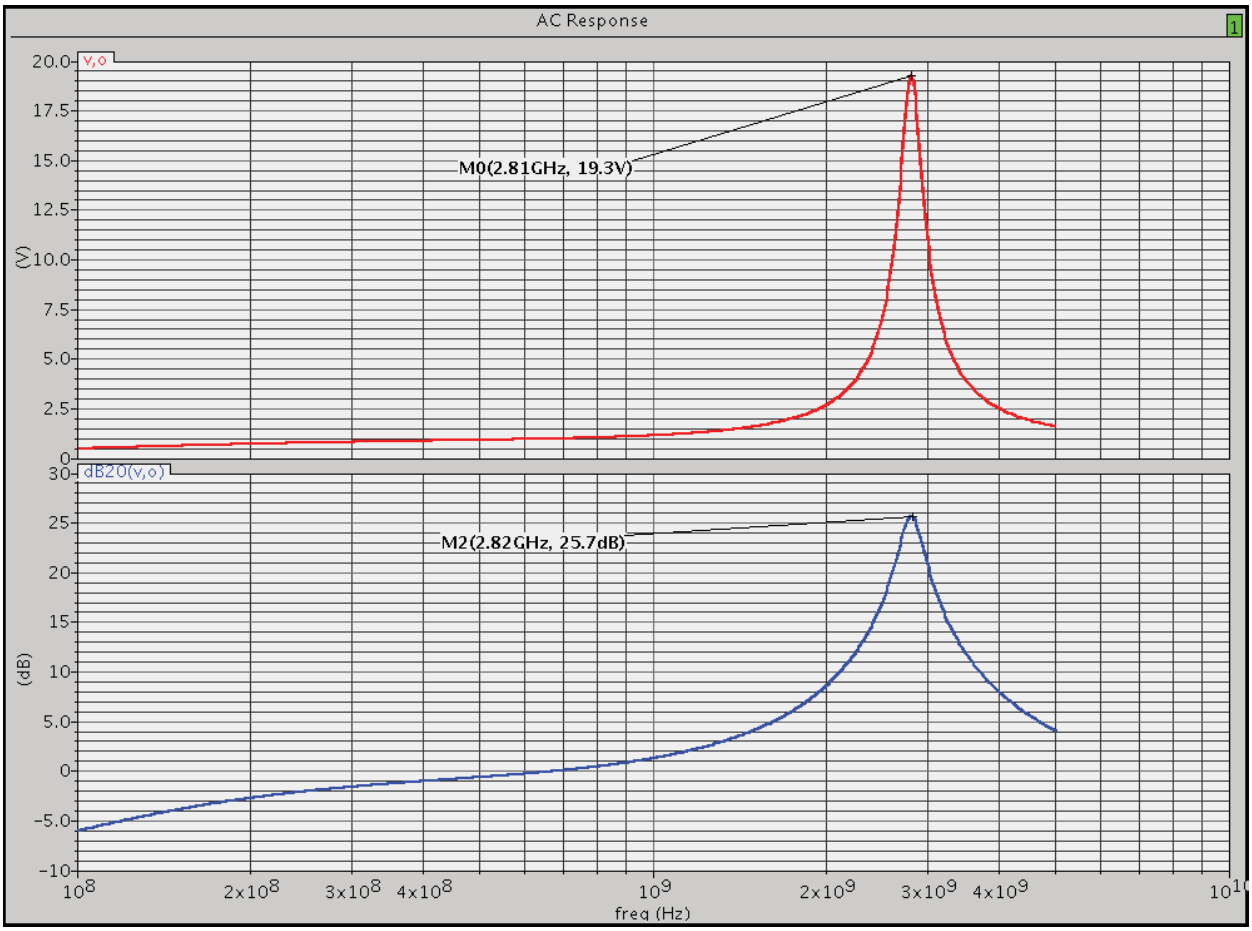

Figure 4.22 Simulated Voltage gain of S-L LNA

The input impedance of this S-L LNA was designed to be a purely real value 50Ω. In order to simulate this parameter using Cadence Virtuoso, the voltage across and current entering the positive input node (labeled "in" on the LNA symbol in Figure 4.15), was plotted. The real and imaginary parts of these values are shown in Figure 4.23. From the figure, it can be seen that the input impedance to this LNA can be written as:

$$Z_{in} = \frac{(835.2 - j66)mV}{(3.3 + j1.3)mA} \tag{4.113}$$

Solving (4.113) results in:

$$Z_{in} = 236.2\,\Omega \angle -26° \tag{4.114}$$

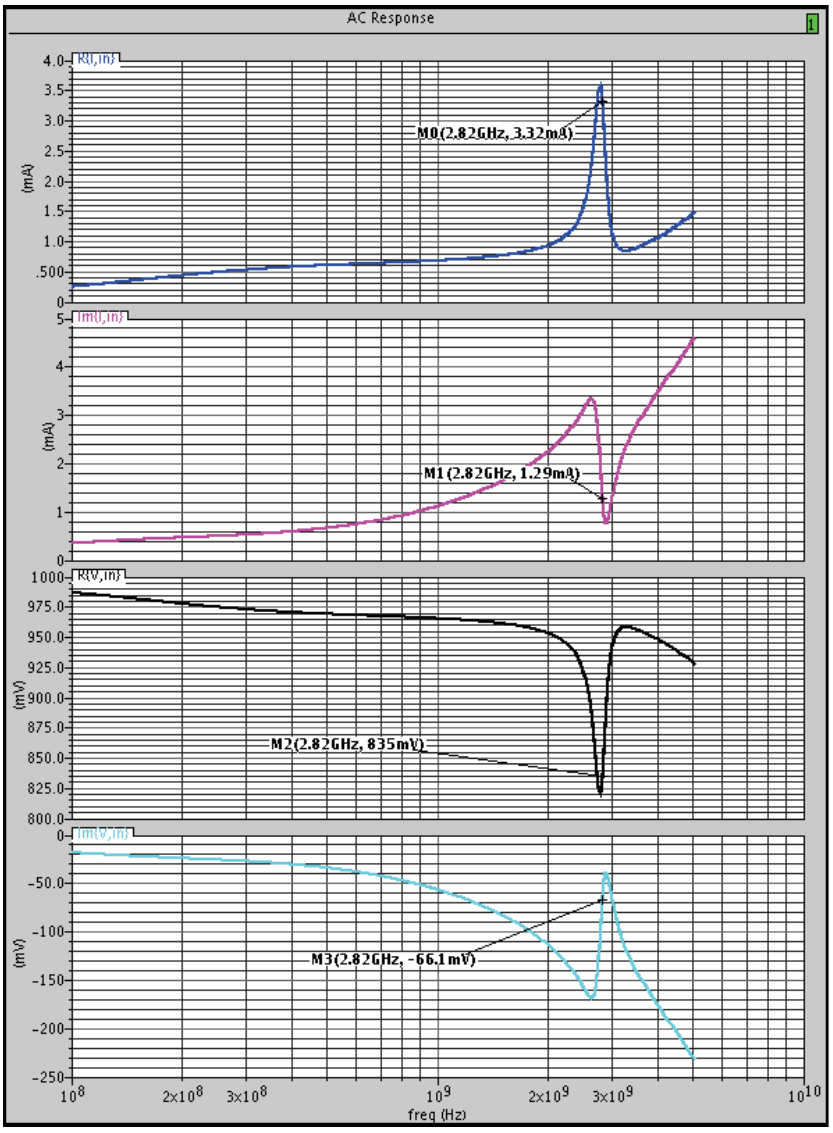

Figure 4.23 Simulated Input Impedance of S-L LNA

The Return Loss (RL), is defined as *-20log[Γ]*, where *Γ* is the reflection coefficient defined by:

$$\Gamma = \frac{Z_{in} - R_s}{Z_{in} + R_s} \tag{4.115}$$

The reflection coefficient and RL for this S-L LNA are:

$$\Gamma = \frac{236.2\,\Omega \angle -26° - 50}{236.2\,\Omega \angle -26° + 50} = .68\angle -11º \tag{4.116}$$

$$RL = -20\log[.68] = 3.35\ dB \tag{4.117}$$

The poor RL of (4.117) indicates an issue with the impedance matching mechanism of this LNA. The final simulation of interest is for the noise figure (NF). Figure 4.24 below shows a plot of the NF (in dB) versus frequency for this S-L LNA.

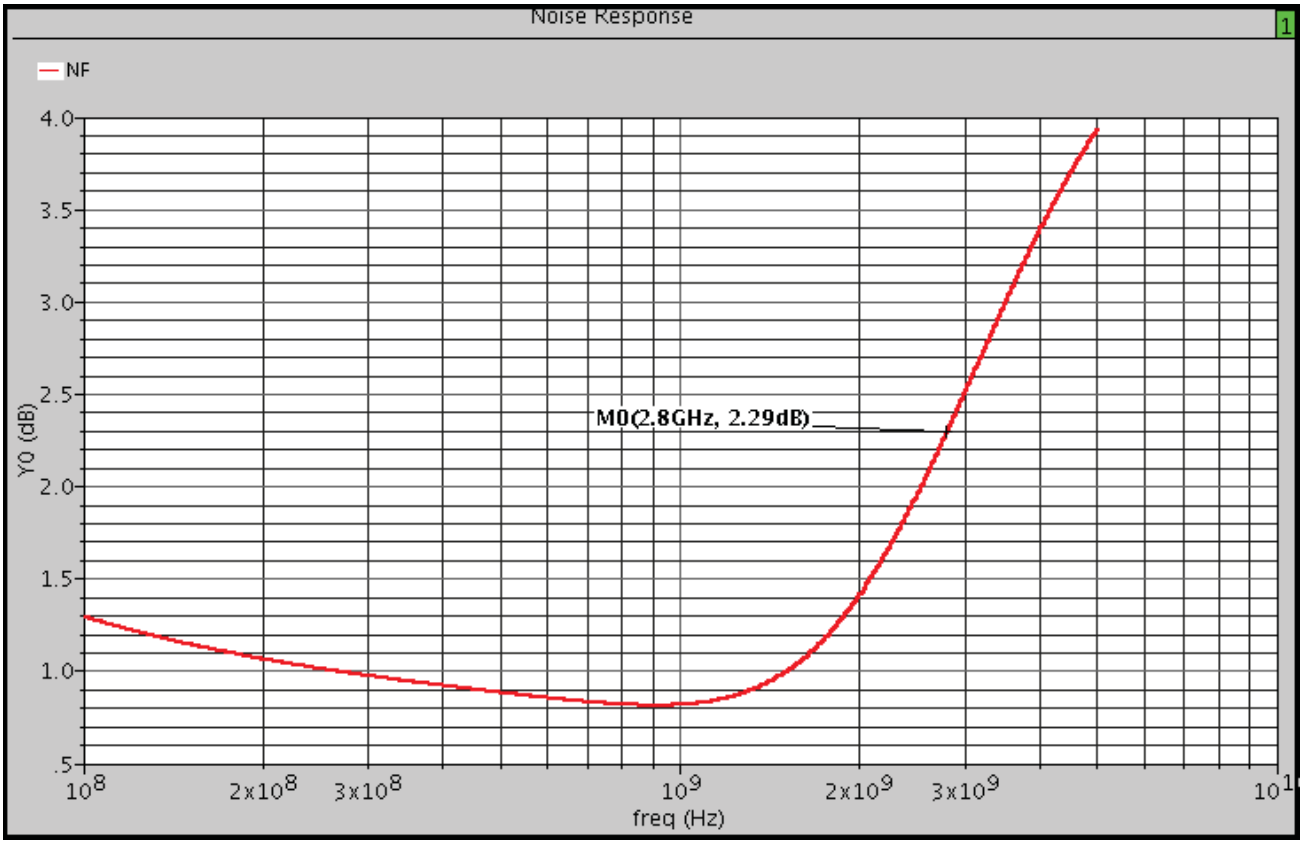

Figure 4.24 Simulation of Noise Figure of S-L LNA

From the above plot, the NF at ~2.82 GHz for the LNA of Figure 4.15 is:

$$F = 2.3\ dB \tag{4.118}$$

From the definition expressed in (2.49), the minimum theoretical *Sensitivity* of this S-L LNA is:

$$Sensitivity_{min} = [-171.7 + 10log(B) + \left(\frac{C}{N}\right)_{min}]\ dBm \tag{4.119}$$

From the parameters simulated above, the maximum input power before compression can be obtained for a generic LNA using the two following expressions:

$$P_{max,IR} = \frac{(V_{OV})^2}{2R_s} \tag{4.120}$$

$$P_{max,OR} = \frac{(4VDD)^2}{R_s(A_v)^2} \tag{4.121}$$

Where V_{OV} is the overdrive voltage of the input FET, R_s is source impedance value, *VDD* is the voltage of the power supply, and A_v is the voltage gain of the LNA. Solving (4.120) and (4.121) results in the input-referred and output-referred maximum input powers before compression (not to be confused with IIP3 and OIP3), respectively:

$$P_{max,IR} = 2.36\ mW \tag{4.122}$$

$$P_{max,OR} = 2.78\ mW \tag{4.123}$$

The minimum between (4.122) and (4.123) is *2.36 mW*, yielding the maximum input power to the S-L LNA before compression, and thus distortion of the output signal, occurs:

$$P_{in,max} = 10\log[2.36\ mW] = 3.7\ dB_m \tag{4.124}$$

4.3.2 Partial Noise Cancelling Low Noise Amplifier

Figure 4.25 is the schematic of the PNC LNA with dc biasing conditions imposed upon it. Within, the FET labeled "M0" represents the current-supply FET of Figure 4.14 M_b and is seen to have a dc current of 8.4 mA. This is the dc operating current of the PNC LNA.

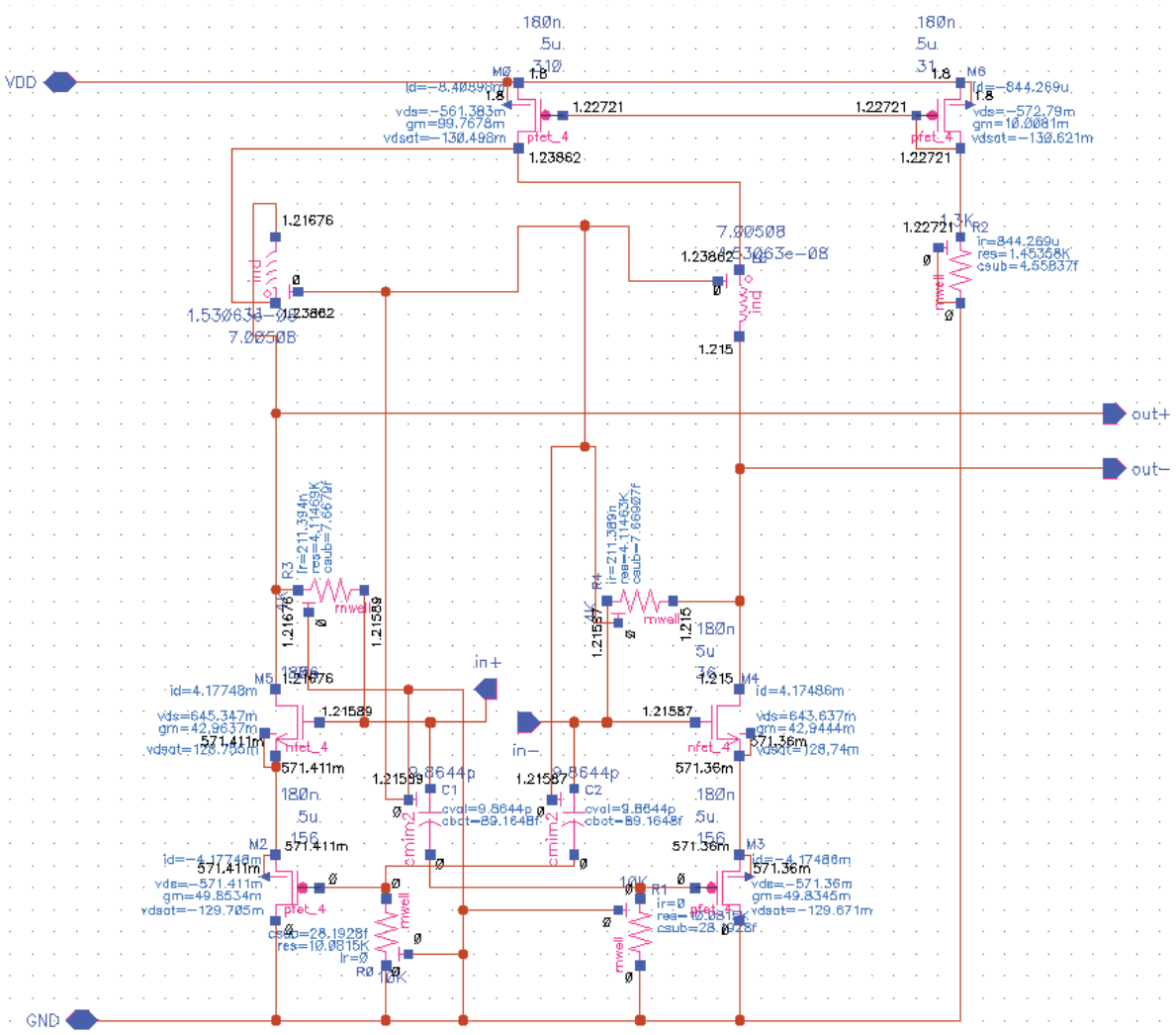

Figure 4.25 Annotated Layout of Implemented PNC LNA using Cadence Virtuoso

To simulate the voltage gain and other performance metrics, as well as the dc current of Figure 4.25, the testbench environment of Figure 4.26 was used. It is annotated with the dc voltages and currents that appear on the block-diagram level of the simulation environment. The source current of 26.8 mA consists of the 8.4 mA activating the PNC LNA, the bias current for each buffer, the biasing resistors, and current mirror.

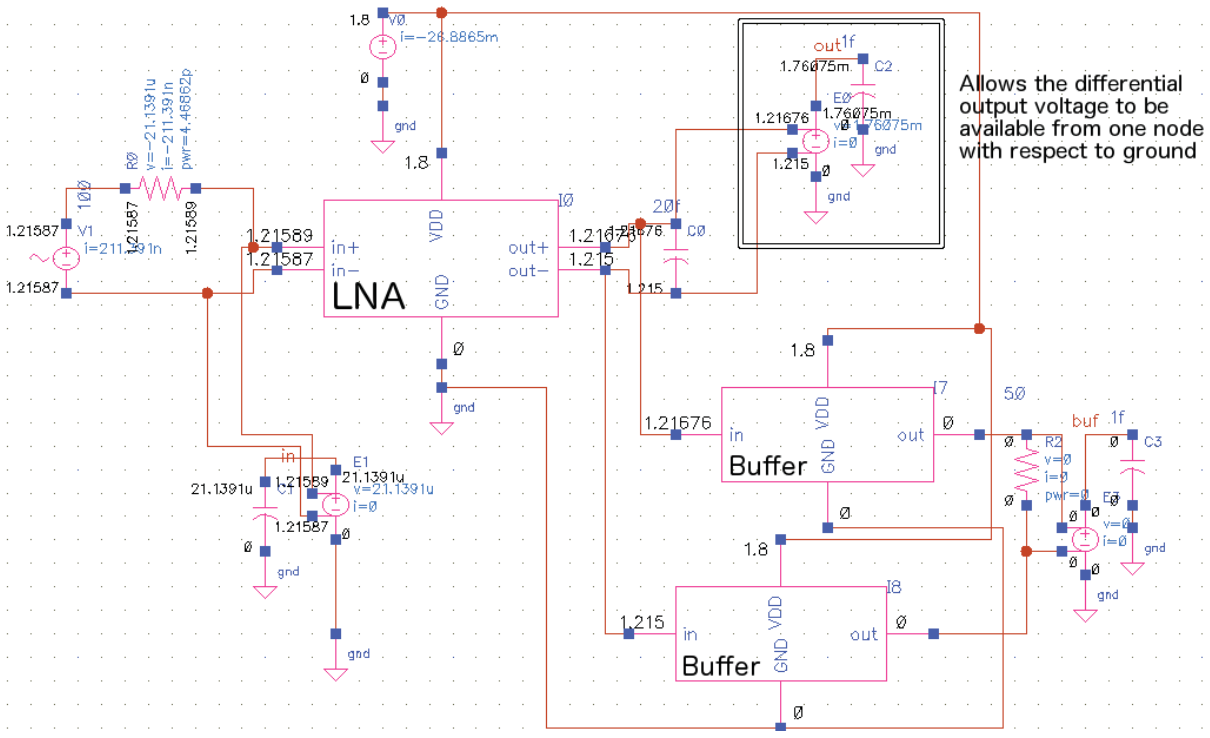

Figure 4.26 Testbench Schematic of PNC LNA using Cadence Virtuoso

In Figure 2.26, the differential output is applied to a voltage-controlled voltage source (VCVS) in order to obtain it at one node with respect to ground. This is also done for the output of the buffers. In the simulations that follow, the signal at the node labeled "out", which is the output of the annotated VCVS, is measured. The simulated frequency response of this LNA follows, in terms of voltage gain versus frequency. It has no effect on the noise simulation or any other simulation of interest in this thesis.

It can be seen from Figure 4.27 that the frequency of operation for this PNC LNA is 2.31 GHz. At this frequency, the voltage gain is 8.67 $^{v}/_{v}$ (18.8 dB).

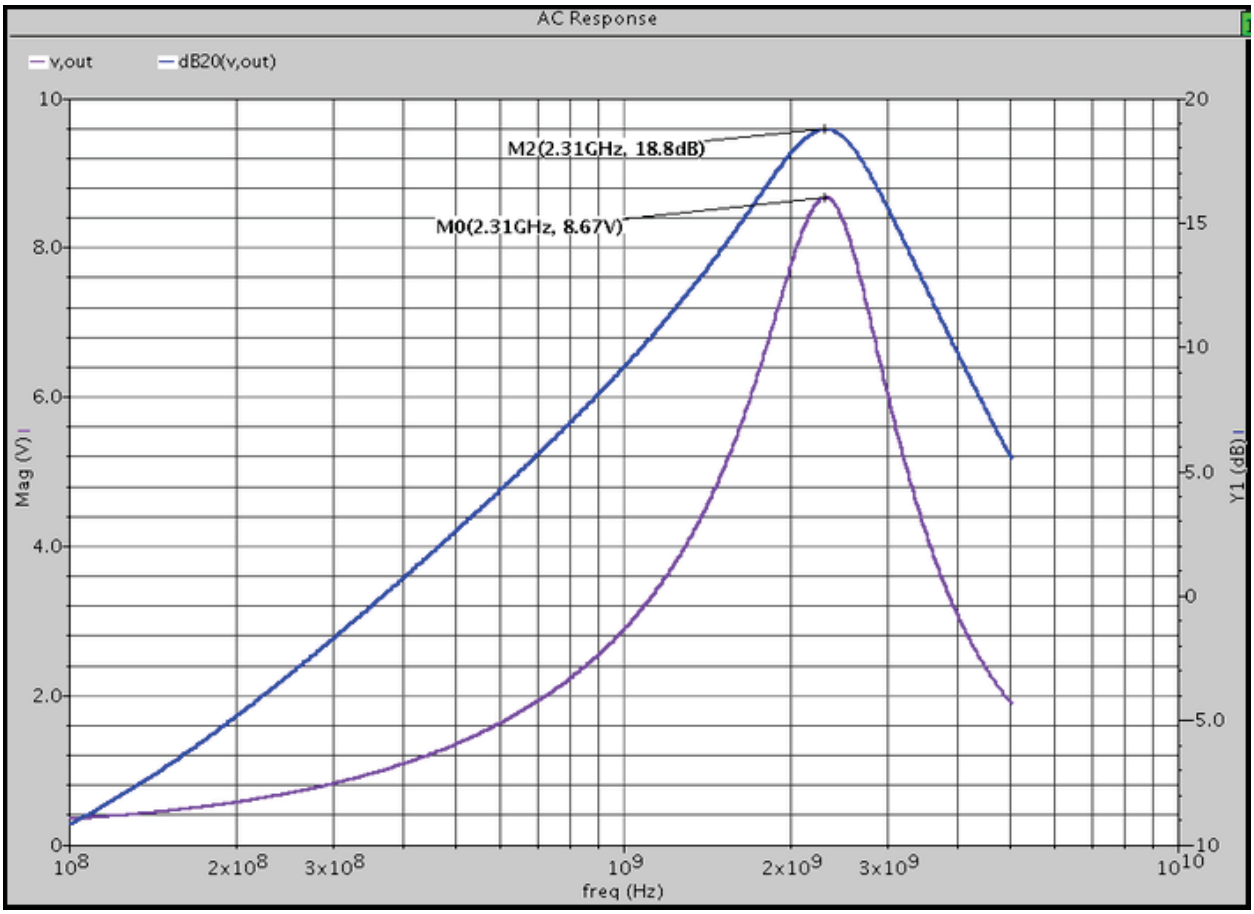

Figure 4.27 Simulated Voltage gain of PNC LNA

The input impedance at the operating frequency (2.31 GHz) is calculated using the plots of Figure 4.28. Within, the voltage of the wire labeled "in" on the input VCVS is measured as well as the current entering the terminal labeled "in+" on the LNA. From these values, Z_{in} is approximated as:

$$Z_{in} = \frac{(260 - j451)\,mV}{(7.4 + j4.51)\,mA} \tag{4.125}$$

which is solved for:

$$Z_{in} = 60\ \Omega \angle -91.4° \tag{4.126}$$

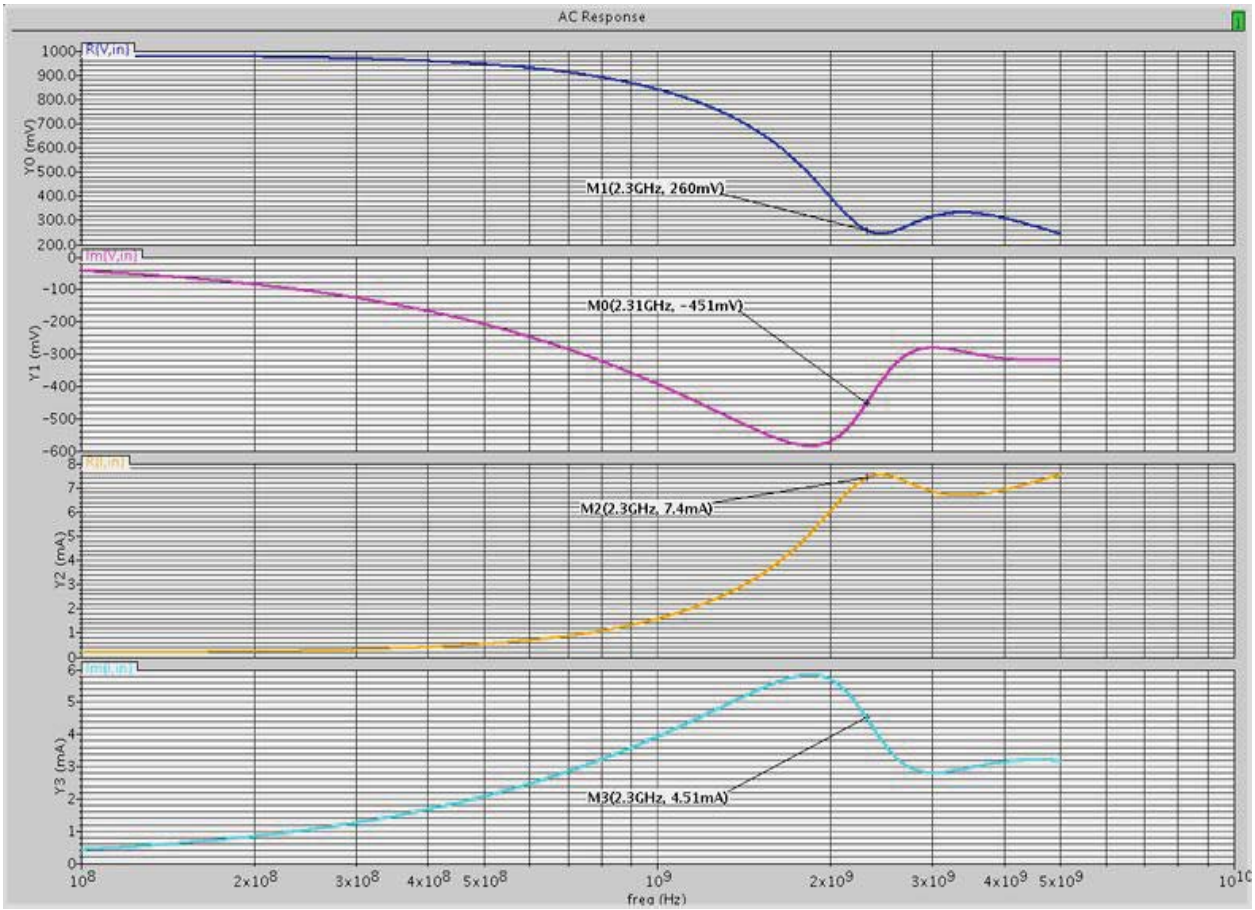

Figure 4.28 Simulated Input Impedance of PNC LNA

The corresponding Γ and RL for this LNA are:

$$\Gamma = 1.0 \angle -80° \tag{4.127}$$

$$RL = -20\log[1.0] = 0\,dB \tag{4.128}$$

The simulated RL for this PNC LNA is 0 dB. This, along with the fact that the input impedance has an angle of roughly -90º, implies that the input appears as an "open-circuit." Therefore, the feedback mechanism, which works by providing a current through R_F, is non-operational. Otherwise the input impedance would appear as $1/g_m$ at 2.4 GHz, implying a much better RL. Instead, the input terminals of this LNA terminate in the capacitance provided by the input FETs, $C_{gs,n}$. The reason the current feedback is no longer supplied is because the condition

of $R_F << R_L$ has been breached, due to the low quality factors of the tank inductors, causing all of the output current to flow through the tuned LC load. A good rule-of-thumb in RF design is a minimum RL of 12 dB, which neither simulated LNA achieves.

The NF for this LNA can be seen in the following plot of Figure 4.29, which shows the simulated NF in dB versus frequency for the PNC LNA of Figure 4.25.

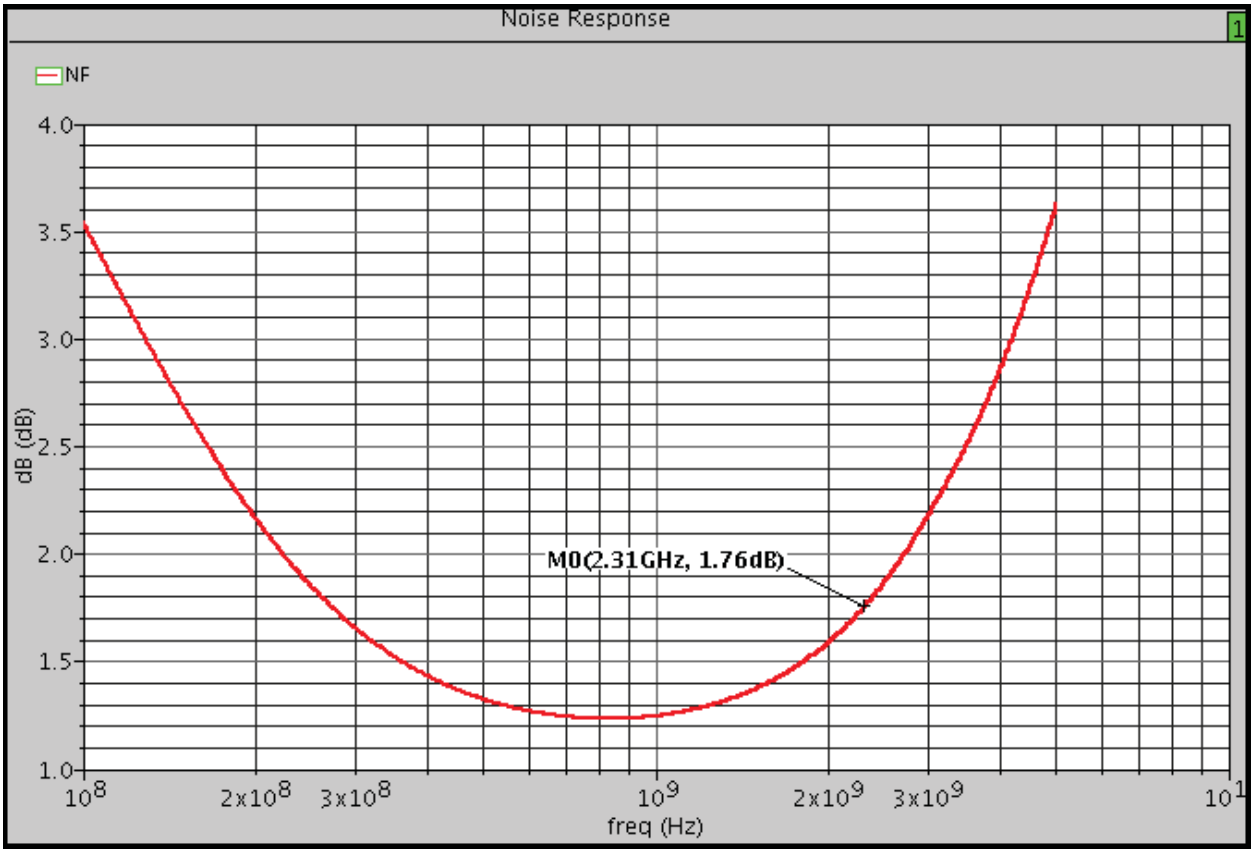

Figure 4.29 Simulated Output Noise Voltage of PNC LNA

From the figure above, it can be seen that the NF at 2.31 GHz is:

$$F = 1.76\ dB \tag{4.129}$$

which corresponds to a minimum Sensitivity of *.54 dB* less than that of the S-L LNA documented in the previous section, whose Sensitivity is expressed in (4.119).

Expressions (4.110) and (4.111) give the input-referred and output-referred maximum input powers before compression of the output signal occurs. Again, these power levels are not to be confused with the IIP3 and OIP3. Using the gain from Figure 4.27, the maximum input power before compression occurs is the minimum between the following two values:

$$P_{max,IR} = \frac{4(v_{ov})^2}{R_s} = 32.7\ mW \tag{4.130}$$

$$P_{max,OR} = \frac{\left(\frac{1}{4}\right)(VDD)^2}{R_F} = 16.2\ mW \tag{4.131}$$

The value of (4.131) sets the maximum input power before compression, and in dB_m is equal to:

$$P_{in,max} = 10\log[16.2] = 12\ dB_m \tag{4.132}$$

It should be noted that the value for $P_{in,max}$ for the S-L LNA given in (4.124) was $3.7\ dB_m$. This suggests that the PNC LNA should have higher values for IIP3 and OIP3, as well as a wider dynamic range (DR). However, the dynamic range will also be mitigated due to the poor NF of the PNC LNA given in (4.129).

4.4 Design and Suspected Device Layout Faults

This section briefly describes all of the known suspected design and device fabrication faults, at the time of writing this document. The following subsections discuss the design issues of the specific LNA implementation (S-L or PNC), while the layout faults common to both circuits are described here. The dc voltages and currents for both LNAs were found to be nominal with respect to dc currents reported in the testbench simulations of the preceding section. Figures 4.30 and 4.31 show the frequency responses for the measured S-L and PNC LNAs, recorded with a HP Network Analyzer and an Agilent Spectrum Analyzer, respectively.

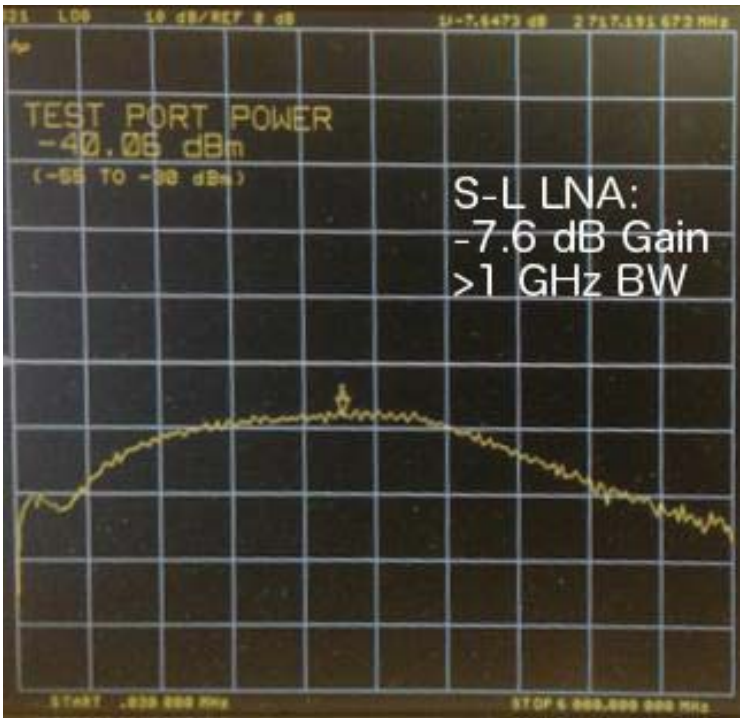

Figure 4.30 Measured s_{21} of Implemented S-L LNA in CMOS

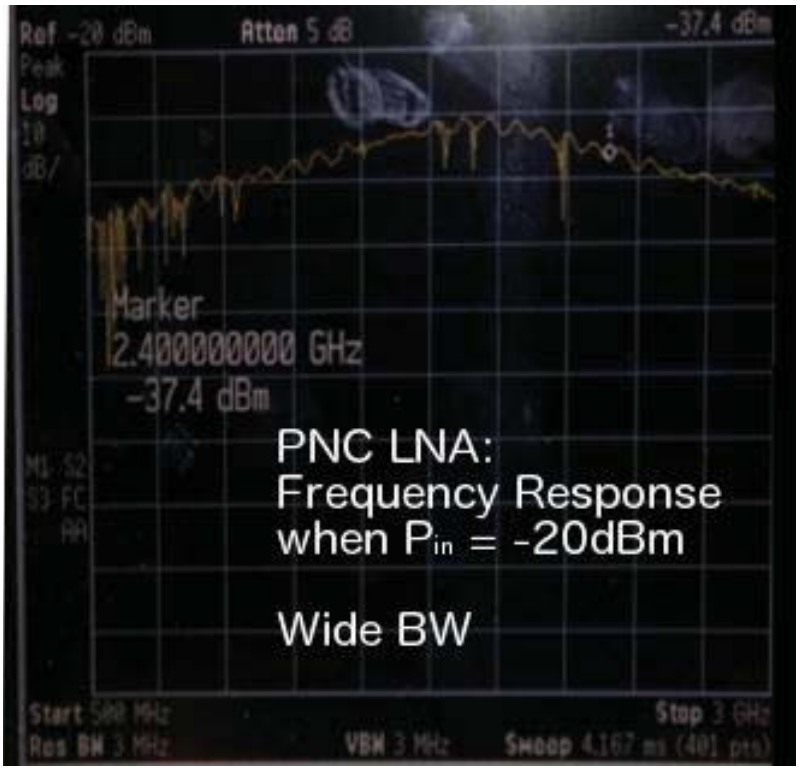

Figure 4.31 Measured s_{21} of Implemented PNC LNA in .180µ CMOS

Note that only one of two differential output nodes was measured in Figure 4.31. The wide bandwidths evident in Figures 4.30 and 4.31 indicate that the tank circuits used as loads in these two LNAs have very low effective *Q* factors. This also explains the high attenuation across the center frequency of the "bandpass" since R_p is dependent on *Q* for both circuits. The high attenuation may also be due to (i) various Q-degradation mechanisms, (ii) excess loss through the buffer, and/or (iii) circuit-specific design flaws, explained in the following subsections.

Metal vias that connect different metal layers in a given IC process often have some non-zero series resistance. For example, the vias implemented in the circuits of this thesis are estimated to have a series resistance as high as 20 Ω each. To eliminate the effects of via series impedances, vias are often arrayed so that all of their resistances combine in parallel fashion. However, in situations where only one via is used or where vias fail, the series impedance can become significant. Another way *Q* can be degraded is when the quality factor of the tank circuit's capacitance is non-infinite. *Q* values, like resistances, combine in parallel, and low-*Q* reactive components lose too much signal energy to implement a high-impedance node. This could be the case when no explicit tank capacitor is used, and instead the load inductors resonate with the parasitic capacitances of the active devices, whose characteristics change instantaneously. In addition to this, the resistors that appear at the output node (that bias the buffer FETs into the active region) appear in parallel and affect the output impedance of the LNA. The following figure is an image of the layout of the tank circuit load of the S-L LNA, indicating how these issues may be at hand.

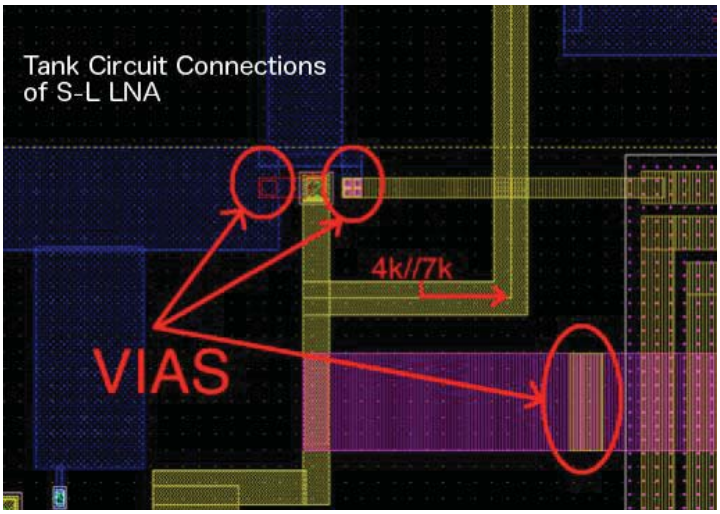

Figure 4.32 Layout Close-up of S-L LNA Tuned Load

Another source of the attenuation could have been through parasitics in the buffer chain. Figures 4.33 and 4.34 compare the simulated frequency responses of the buffered and non-buffered outputs of both LNAs.

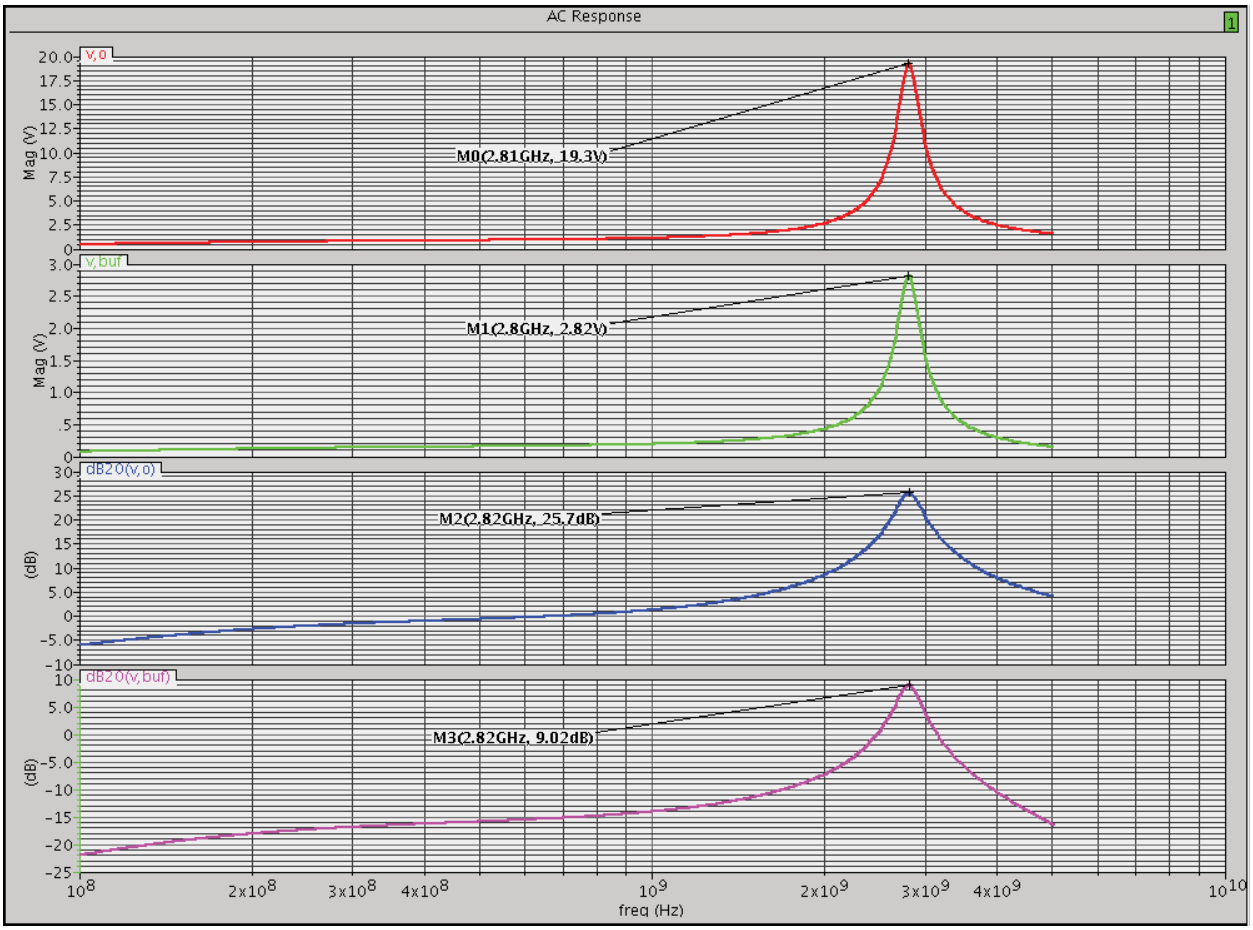

Figure 4.33 Buffered and Non-Buffered S-L LNA Voltage Gain

Figures 4.33 and 4.34 show the attenuation due to the buffers. This can have a significant effect on the NF, as per the Friis equation. Also, these simulations were not "extracted", i.e. did not include the parasitic capacitances and resistances of the metal traces or the devices at high frequency. The combined parasitics of the LNA circuitry and the buffers are likely causing this large deviation from simulation behavior.

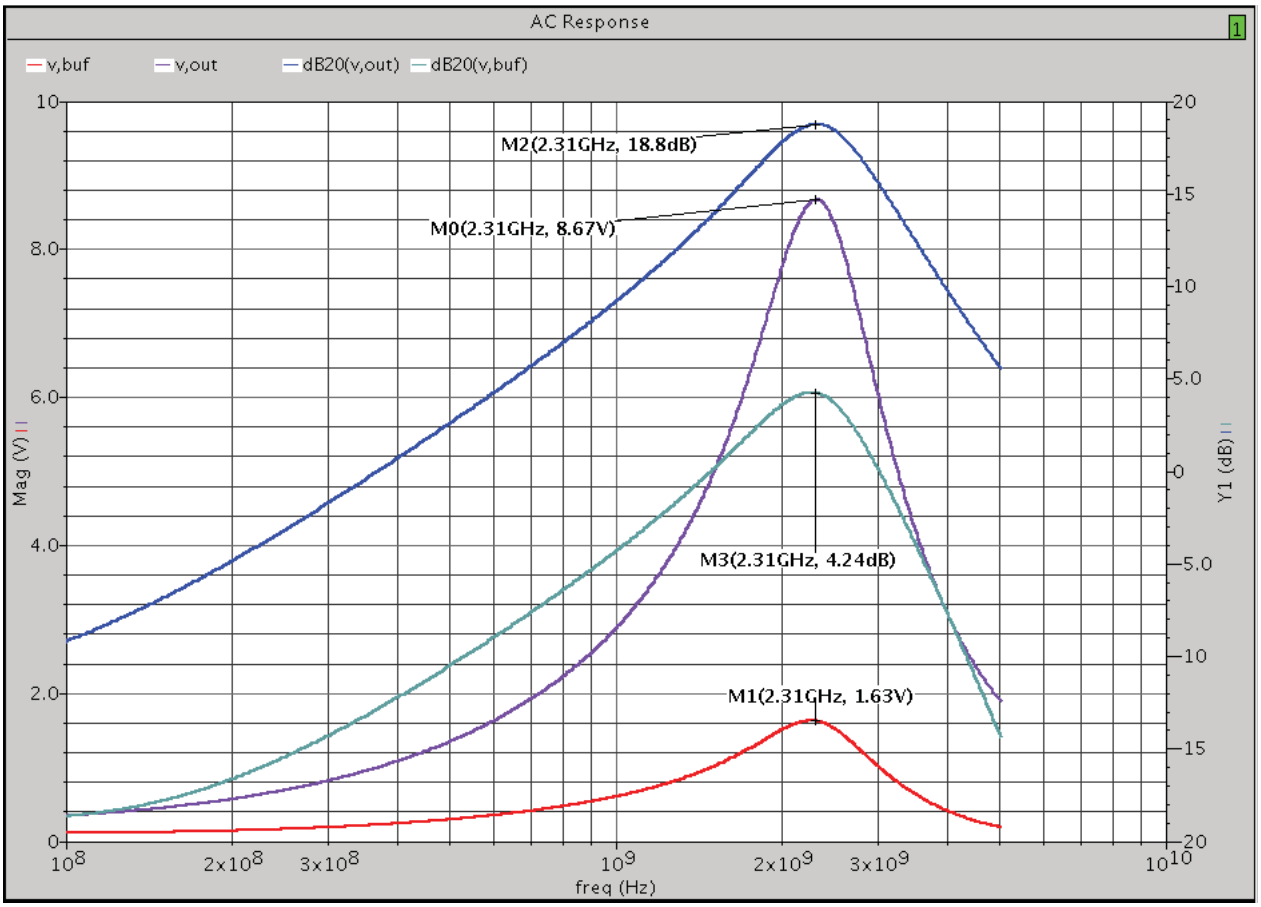

Figure 4.34 Buffered and Non-Buffered PNC LNA Voltage Gain

4.4.1 Source-Inductor Low Noise Amplifier

The design of the impedance matching circuitry for the S-L LNA resulted in an almost completely imaginary matched impedance of *~50Ω* at *70º*. The RL of (4.117) is based on the complex value of Γ, and perfect matching requires a real input impedance. Otherwise the magnitude of Γ may increase and diminish the RL.

In reality, the input impedance of the S-L LNA at 2.4 GHz was measured to be 44Ω - j72.7Ω, as seen in Figure 4.35. This corresponds to a reflection coefficient of .61 with an angle of -56º. The RL of this measured S-L LNA is 4.24 dB. This extra negative reactance is likely

due to the input capacitances that went unsimulated - such as non-C_{gs} FET capacitance, GSG capacitance, and trace capacitances.

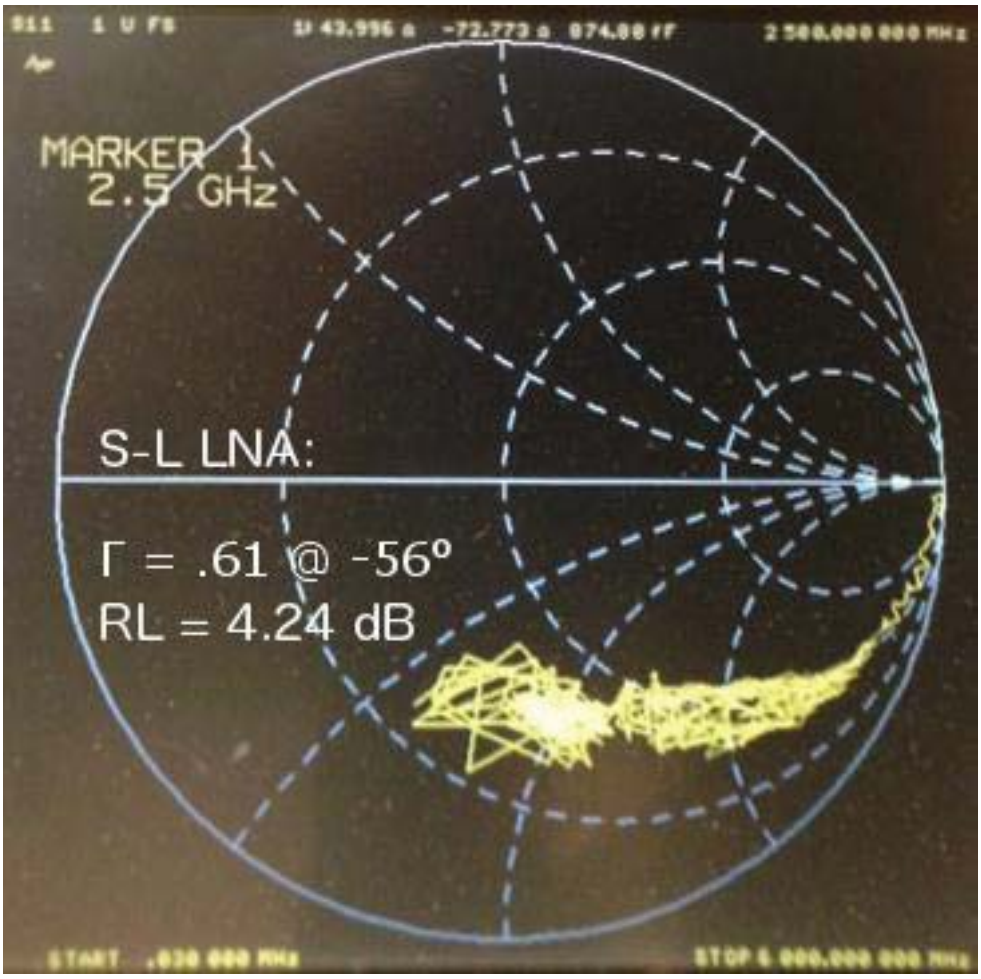

Figure 4.35 Measured Input Impedance of S-L LNA

In addition to impedance mis-match at the input, the FET M_1 in the S-L LNA has only haf the g_m of the input FET, M_0. This causes signal attenuation and noise generation at the output that serves to decrease the SNR at the output. This is likely a significant reason that the NF of the simulated LNA in the previous section was as high as *2.3 dB*, since perfect g_m-matching is assumed in the NF analysis of the cascoded S-L LNA.

4.4.2 Partial Noise Cancelling Low Noise Amplifier

At the time of writing this thesis, the most significant design flaw was the choice in feedback resistance $R_{F,0}$ and $R_{F,1}$. Throughout the analysis of the PNC LNA, found in section 4.1.1, the assumption that $R_F << R_p$ was made, since the gain and signal-feedback mechanism were contingent on this being the case. However, simulations suggest that the Q of the load inductors is only ~7 which, for an a frequency of 2.31 GHz and inductor of *15.3 nH*, would result in the following R_p:

$$R_p = Q2\pi fL = 1.55\ k\Omega \tag{4.133}$$

In the schematic of Figure 4.16, it can be seen that $R_{F,0} = R_{F,1} = 4k\Omega$. Therefore, the assumptions and analysis undertaken in section 4.1.2 are not valid for the PNC LNA documented here. Instead, a value of R_F should be chosen such that:

$$R_s << R_F << R_p \tag{4.134}$$

Also, the reason for the very poor RL of ~0dB for this LNA is because the current-feedback mechanism, wherein output current flows through R_F and back to the gate of the input FET, was non-operational. When properly designed, the input impedance of this LNA appears as $1/g_m$, due to this feedback. But, since the reactance of the output tank circuit is much lower than the value of R_F, the majority of output current flows through the tuned load, and not through R_F.

Chapter 5 - Conclusion and Future Works

5.1 Conclusions

5.1.1 Frequency Dividers

Injection Locked Frequency Dividers

For the ILFDs measured and documented in this thesis, it was shown that a Tail-ILFD has a wider locking range (LR) than a Quench-ILFD, all other circuit conditions held equal. Specifically, the LR of the Tail-ILFD was 12%, and the LR of the Quench-ILFD was 3.7%, of an operating frequency of 6.4 GHz. Both implementations consumed 2.28 mW of dc power in nominal operation. When locked, the phase noise of the oscillator reduces to at most -95 dB_c at a 10 kHz offset. This measurement of phase noise was limited by the Spectrum Analyzer used in the laboratory, so it could be below this figure.

Another observation was that the Quench-ILFD was capable of operating while consuming as low as 219.6 μW of dc power. In addition to this, the LR of the Quench-ILFD increased from 3.7% of the operating frequency to 4.8%. This suggests that Quench-ILFDs are a better option when low power consumption is required, and a low LR can be tolerated.

Lastly, it should be noted that for a VCO employing a tuned load, the LR is inversely proportion to the net Q, and is in general dependent on the relationship $\partial\phi/\partial\omega$ of the frequency selective network. Therefore, a frequency divider with a wide LR can be implemented by lowering the Q value of the output RLC network, but lowering Q is also associated with higher oscillator power consumption.

Regenerative Frequency Dividers

For the RFD that was reported in Chapter 3, simulations in Cadence Virtuoso reported a LR of 16.7% at an operating frequency of 7.8 GHz, while consuming 228 μA of dc current. This

implies only 410 μW of dc power, which is over 5 times less than the dc power consumption of the Tail-ILFD, whose LR was limited to 12% of its operating frequency while consuming 2.28 mW. These simulations imply potential as a low-power divider with a wide LR for this particular topology, but further research is needed.

5.1.2 Low Noise Amplifiers

Considering the LNAs documented in this thesis, simulations reported that the S-L LNA achieved higher gain than the PNC LNA, but had a higher NF at its frequency of operation. Simulations reported the NF of the S-L LNA as 2.3 dB at 2.8 GHz, while the NF of the PNC LNA was 1.76 dB at 2.31 GHz.

Because of the single-ended topology of the S-L LNA, compression of the output signal due to the input FET occurs at a lower power, when compared to the PNC LNA. And because of the high gain, the S-L LNA will also compress at the output at a lower power than the PNC LNA. Because of the differential nature of the PNC LNA, a higher input power before compression can be tolerated, since this input voltage is split evenly between two input FETS. Also, because the PNC LNA documented in this thesis has a lower voltage gain that the corresponding S-L LNA, its output-referred maximum input power before compression is also of higher magnitude. However, because empirical measurements were not possible, this was not proven in a laboratory setting.

A design flaw of not matching the transconductances of the S-L LNA's nFETs most likely resulted in the high NF of the simulated S-L LNA. This can be understood by considering the approximation for its NF, in Chapter 2. The assumption of matched transconductances revealed full cancellation of the thermal noise induced in the cascode FET. When this is not the case, this noise appears at the output of the LNA and contributes to an increased NF. The source inductor serves to match the impedance of the S-L LNA's input to any real arbitrary impedance, though this was not achieved in the S-L LNA implementation documented here.

Small-signal expressions derived for the input impedance, gain, output impedance, and noise figure of the PNC LNA reveal the following conditions for the optimization of its performance:

1. Impedance Matching: $(2/g_m) = R_s$
2. Minimize Noise Figure: $R_s << R_F << R_p$
3. Matched g_m among all FETs

Note that R_p is the equivalent parallel resistance calculated from the series resistance of the metal traces that make up the load inductance, and is proportional to the inductor's quality factor Q. The resistors represented by R_F provide the feedback to the input nFETs of the PNC LNA, and this mechanism must be enabled for impedance matching to be achieved. Lastly, the third condition states that all the transconductances of all FETs, both n and p, should be the same value for the PNC LNA to operate as described in section 4.1.2.

As reported in section 4.3.2, simulations show that the PNC LNA is capable of a NF as low as 1.76 dB. Along with a potentially high input compression point and high dynamic range (DR), this motivates further optimization of the schematic and layout of the PNC LNA documented in this thesis.

5.2 Future Works

5.2.1 Frequency Dividers

A different topology for an RFD should be designed and implemented in order to properly study its performance and compare it to an ILFD. The RFD documented in this thesis had built in negative-resistance mechanisms that implied free-running oscillations and injection-locked behavior. Essentially, the RFD designed and simulated in section 3.3.2 was a differential configuration of two Tail-ILFDs.

Despite the mis-design of the RFD of Chapter 3, simulations reported a LR for this RFD that was wider than that of the Tail-ILFD, while consuming over 5 times less dc current. This motivates the redesign of this topology on the basis of a low-power differential Tail-ILFD.

5.2.2 Low Noise Amplifiers

The impedance matching components of the S-L LNA need to be redesigned in order to achieve a match to 50Ω. More detailed approximations of input/parasitic capacitance should be used while calculating reactive values, and some portion of this should be implemented using a high quality explicit capacitor. Metal-Insulator-Metal (MIM) capacitors are typically the highest quality capacitor option in CMOS processes. When designing the impedance matching circuitry, one should consider the relationship between the FET parasitic capacitance C_G and g_m, since both are based on the device width, W. High overdrive of the FET achieves a higher transconductance for a fixed width, and also allows the input FET more input power before device compression. The danger of making g_m too large is compression of the LNA output signal at low input powers.

Due to the inherent power-handling capabilities of a differential amplifier technology, a S-L LNA with differential inputs and outputs should be capable of a low NF, as well as low sensitivity. And by using reactive feedback, the gain of the S-L LNA could be limited, thus improving the compression of its output due to the level of input power.

The PNC LNA performance optimization criterion derived in this thesis require that $R_s << R_F << R_p$ for the minimum NF. For the implementation of Chapter 4, R_F was 4kΩ, while R_p was only 1.55 kΩ. A new design of this LNA, assuming an R_s of 50Ω and the same R_p value, should improve the performance by changing R_F to 500Ω. However, an entire re-design based on the expressions derived in this thesis is suggested so that an optimized PNC LNA can be measured in the laboratory.

Changes to Layout

The layouts of the LNAs, as shown in this thesis, should be redone to minimize parasitic series resistances due to low-numbered via arrays. Also, more explicit capacitance should be used in the resonant circuits, such as in matching networks and tuned loads. It is currently believed that a major source of degradation originates from low-Q capacitive loading from the buffer transistors.

Instead of buffering the LNAs' output with an exponential chain of source-followers, a high-gain amplifier (followed by a low output-impedance buffer stage) should be used. By following the method described in [Friis, 1944], the NF of network composed of an LNA followed by a high gain stage can be easily determined using standard RF laboratory equipment. First, a method to measure the noise figure of the composite two-stage network, as well as the noise figure of the second stage, is described. Then, a method of determining the gain of the first stage is explained. Lastly, Friis gives the equation for the noise figure of the first stage (e.g. an LNA), shown in (1.12). Using this process, the NF of an LNA followed by any arbitrary high-gain stage can be empirically measured.

This however will not cure the issue of the low-Q capacitive loading due to the output buffer circuitry. In order to mitigate these effects, an explicit MIM capacitor should be implemented across the output inductors. This requires either less tank inductance, more power consumption, or both.

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Appendix A - 2.4-GHz Buffer Schematic and Layout

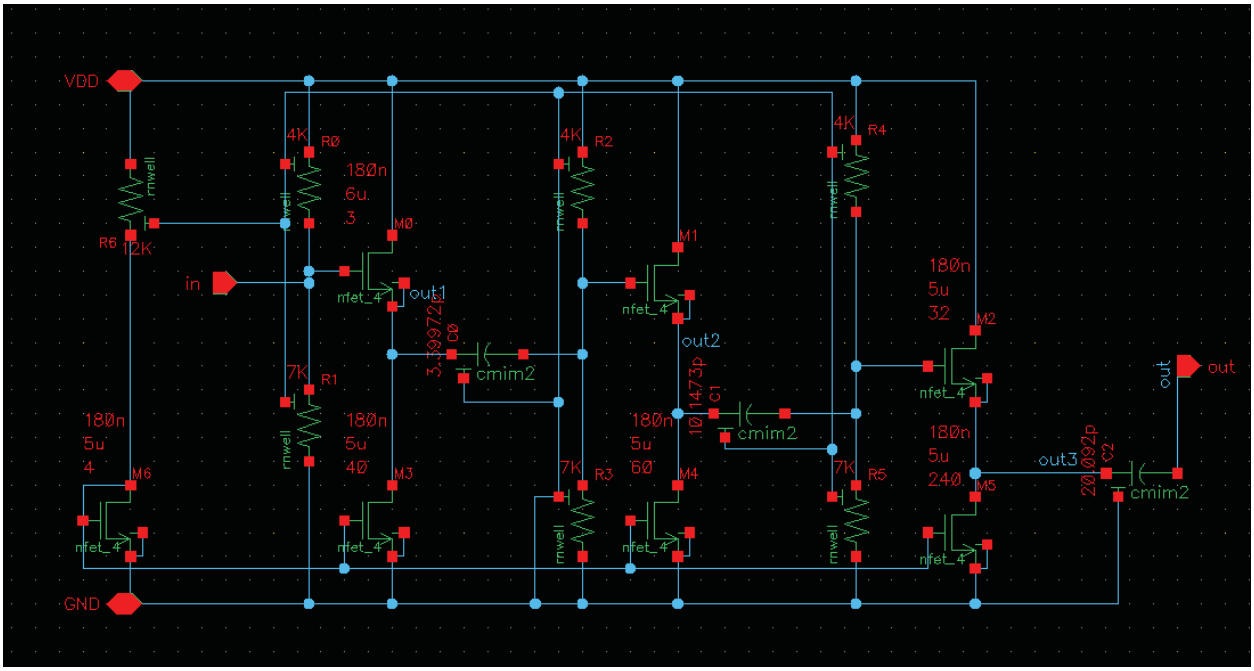

Figure A. 1 2.4-GHz Buffer Schematic

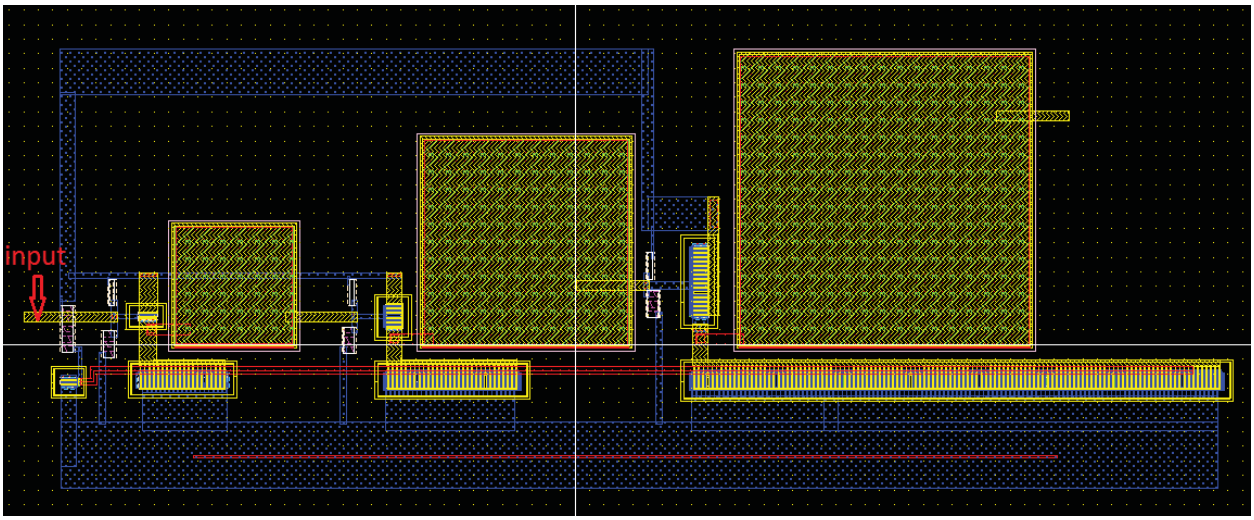

Figure A. 2 2.4-GHz Buffer Layout