SOME CONSIDERATIONS OF DIGITAL FILTER IMPLEMENTATION USING MICROPROCESSORS

by

JAY PURUSHOTHAMAN JAYAPALAN

B.Sc., University of Madras, 1971
B.E., Indian Institute of Science, 1974

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Approved by:

N. Ahmed

Major Professor

To the memory of

Dr. Dale E. Kaufman

who developed my interest in microprocessors

and initiated this line of research.

THIS BOOK CONTAINS NUMEROUS PAGES WITH DIAGRAMS THAT ARE CROOKED COMPARED TO THE REST OF THE INFORMATION ON THE PAGE.

THIS IS AS RECEIVED FROM CUSTOMER.

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CHAPTER 1

INTRODUCTION

Digital filters have been considered for various applications which include process control, guidance control, and data acquisition. Such filters are usually implemented via hardwired logic and involve the use of shift-registers, adders, multipliers and logic gates [1]. However, the hardware implementation of digital filters is yet a developing field. To this end, the main objective of the work explained in this report is to examine some aspects of implementing digital filters using microprocessors. There are several reasons for considering microprocessors for such implementations:

i) microprocessors are becoming increasingly powerful and yet their cost is reducing

ii) the number of components required is reduced

iii) there is a greater computational capability and flexibility.

A major disadvantage at present is that they are relatively slow. However, since the related technology is moving at a rapid pace, it is reasonable to expect that this disadvantage will be overcome in the relatively near future.

The effects of limited word length such as round off error and coefficient inaccuracy will still be present. However, implementation using microprocessors makes it possible to choose almost any desired word length rather than designing the filter to suit the commercially available hardware multipliers and adders with limited word lengths. For example, several 2 bit slices of Intel 3000 type microprocessors can be used to form a system

of almost any desired word length. Even among fixed word length processors there is a wide choice of word lengths to choose from.

The approach for implementing digital filters via microprocessors is introduced by considering a simple first order recursive filter represented by the transfer function,

$$H(Z) = \frac{Z}{Z + K} \qquad (1.1)$$

This filter has been implemented on a micro-computer system using the Intel 8008 microprocessor. Although Intel 8008 is one of the slowest microprocessors, it is considered for this study since hardware and software information pertaining to it are readily available. This is because it was one of the first microprocessors to have been available commercially. This system has been simulated on an IBM 370 system. Studies pertaining to the filter's frequency response characteristics using the simulator have been made. Interfacing units such as A/D converter have been included in the simulation. Some of the results obtained via the simulator have been verified on the actual microcomputer system.

Chapter 2 introduces some fundamentals pertaining to digital filtering. In Chapter 3 various factors related to digital design considerations are summarized. Conventional methods of digital filter implementation are discussed in Chapter 4, while implementation using microprocessors is considered in Chapter 5.