CHEMICAL MECHANICAL POLISHING AND GRINDING OF SILICON WAFERS

by

XIAOHONG ZHANG

B.S., Tsinghua University, 2001
M.S., Tsinghua University, 2004

AN ABSTRACT OF A DISSERTATION

submitted in partial fulfillment of the requirements for the degree

DOCTOR OF PHILOSOPHY

Department Of Industrial and Manufacturing Systems Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2007

Abstract

Silicon is the primary semiconductor material used to fabricate integrated circuits (ICs). The quality of integrated circuits depends directly on the quality of silicon wafers. A series of processes are required to manufacture the high-quality silicon wafers.

Chemical mechanical polishing is currently used to manufacture the silicon wafers as the final material removal process to meet the ever-increasing demand for flatter wafers and lower prices. A finite element analysis has been conducted to study the effects of influencing factors (including Young's modulus and Poisson's ratio of the polishing pad, thickness of the pad, and polishing pressure) on the wafer flatness. In addition, an experimental study was carried out on the effects of process variables (including wafer rotation speed, pad rotation speed, the temperature of the cooling wafer in polishing table, polishing pressure, and the slurry flow rate) on material removal rate (MRR) in polishing of silicon wafers. The results from this study show that the polishing pressure and the pad speed are the most significant factors affecting the MRR.

The polishing pad is one of the most critical factors in planarizing the wafer surface. It transports the slurry and interacts with the wafer surface. When the number of polished wafers increases, the pad is glazed and degraded and hence the polishing quality is decreased. The pad properties are changed during the process. The measuring methods for the pad properties including pad thickness monitoring, elastic properties and hardness are reviewed. Elasticity of two types of pads are measured and compared.

The poor flatness problems such as tapering, edge effect, concave or convex wafer shape were investigated. Finite element models were developed to illustrate the effects of polishing pad and carrier film properties on the stress and contact pressure distribution on the wafer surface. Moreover, the material removal unevenness is studied.

A grinding-based manufacturing method has been investigated experimentally to demonstrate its potential to manufacture flat silicon wafers at a lower cost. It has been demonstrated that the site flatness on the ground wafers (except for a few sites at the wafer center) could meet the stringent specifications for future silicon wafers. One of the problems is the poor flatness at the wafer center: central dimples on ground wafers. A finite element model is

developed to illustrate the generation mechanisms of central dimples. Then, effects of influencing factors (including Young's modulus and Poisson's ratio of the grinding wheel segment, dimensions of the wheel segment, grinding force, and chuck shape) on the central dimple sizes are studied. Pilot experimental results are presented to substantiate the predicted results from the finite element model. This provides practical guidance to eliminate or reduce central dimples on ground wafers.

The study in this thesis is to understand the mechanism of CMP and grinding of silicon wafers. Improving the processes and the quality of silicon wafers are the final goals.

CHEMICAL MECHANICAL POLISHING AND GRINDING OF SILICON WAFERS

by

XIAOHONG ZHANG

B.S., Tsinghua University, 2001
M.S., Tsinghua University, 2004

A DISSERTATION

submitted in partial fulfillment of the requirements for the degree

DOCTOR OF PHILOSOPHY

Department of Industrial and Manufacturing Systems Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2007

Approved by:
Major Professor

Dr. Zhijian Pei

Abstract

Silicon is the primary semiconductor material used to fabricate integrated circuits (ICs). The quality of integrated circuits depends directly on the quality of silicon wafers. A series of processes are required to manufacture the high-quality silicon wafers.

Chemical mechanical polishing is currently used to manufacture the silicon wafers as the final material removal process to meet the ever-increasing demand for flatter wafers and lower prices. A finite element analysis has been conducted to study the effects of influencing factors (including Young's modulus and Poisson's ratio of the polishing pad, thickness of the pad, and polishing pressure) on the wafer flatness. In addition, an experimental study was carried out on the effects of process variables (including wafer rotation speed, pad rotation speed, the temperature of the cooling wafer in polishing table, polishing pressure, and the slurry flow rate) on material removal rate (MRR) in polishing of silicon wafers. The results from this study show that the polishing pressure and the pad speed are the most significant factors affecting the MRR.

The polishing pad is one of the most critical factors in planarizing the wafer surface. It transports the slurry and interacts with the wafer surface. When the number of polished wafers increases, the pad is glazed and degraded and hence the polishing quality is decreased. The pad properties are changed during the process. The measuring methods for the pad properties including pad thickness monitoring, elastic properties and hardness are reviewed.

The poor flatness problems such as tapering, edge effect, concave or convex wafer shape were investigated. Finite element models were developed to illustrate the effects of polishing pad and carrier film properties on the stress and contact pressure distribution on the wafer surface. Moreover, the material removal unevenness is studied.

A grinding-based manufacturing method has been investigated experimentally to demonstrate its potential to manufacture flat silicon wafers at a lower cost. It has been demonstrated that the site flatness on the ground wafers (except for a few sites at the wafer center) could meet the stringent specifications for future silicon wafers. One of the problems is the poor flatness at the wafer center: central dimples on ground wafers. A finite element model is developed to illustrate the generation mechanisms of central dimples. Then, effects of

influencing factors (including Young's modulus and Poisson's ratio of the grinding wheel segment, dimensions of the wheel segment, grinding force, and chuck shape) on the central dimple sizes are studied. Pilot experimental results are presented to substantiate the predicted results from the finite element model. This provides practical guidance to eliminate or reduce central dimples on ground wafers.

The study in this thesis is to understand the mechanism of CMP and grinding of silicon wafers. Improving the processes and the quality of silicon wafers are the final goals.

Table of Contents

List of Figures

List of Tables

Acknowledgements

I would like to thank my advisor Professor Zhijian Pei for sharing with me his vast knowledge and great vision; for his continuous encouragement, and for helping me continually.

I would like to extend my sincere gratitude to Dr. Jennifer L. Anthony for being the chairperson of the examining committee. Meanwhile I would like to thank other committee members: Professor Stanley Lee, Professor Jack Xin and Dr. Graham Fisher for their constructive suggestions and valuable discussions along my studies. My interaction with them has benefited me both professionally and personally. I would like to express my thanks especially to Dr. Graham R. Fisher, from MEMC Electronic Materials, Inc., not only for being one of my supervisory committee members but also for his generous help and support to my research work.

My gratitude also goes to MEMC Electronic Materials, Inc. for giving me the opportunity to conduct my research in their fabs, and to visit MEMC Japan Plant. I learned a great deal from the contact with the real world, and I have tried to incorporate these learnings into my research. I would like to acknowledge Dr. Madhavan Esayanur and Mr. Roland Vandamme for their support to my research projects. I also want to acknowledge Dr. Peter Albrecht for helping in projects on CMP machine. I would like to thank Mr. Gary Bowers for working with me on the experimental part of CMP. Without their support all the tests that were carried out in those facilities would not have been possible.

I also would like to thank our department head, Professor Bradley A. Kramer for all his help and support to my research work and all the other department staff for their assistance and the research facilities provided.

I want to thank all of the current and past members in our research group: Dr. Wangping Sun and Ms. Lian Li, Dr. Jianmei Zhang and Mr. Ping Hu for their warmhearted help to my research work and life; I also want to thank Dr. Zhichao Li, Mr. Nickil Churi, Ms. Weike Lu, and Ms. Jinghua Liu, Mr. Pengfei Zhang and Mr. Yu Chen for their assistance to my research. To all the staff of the IMSE departments, and other friends; I want to thank them for making my life easy and happy.

I want to thank my parents and my sister, for their unconditional love, and incredible support. Last, but not least my greatest gratitude goes to my lovely fiancé Liang Zhou, for being with me in this adventure, for all the support, friendship and the happiness that he has brought to my life.

CHAPTER 1 - Introduction

1.1 Importance of Silicon wafers

Semiconductors have pervaded every fabric of our society. The basic semiconductor material from which electronic devices are made comes in the form of round thin crystalline wafers. Most integrated circuits (ICs) are built on silicon wafers [Van, 2000]. About 150 million silicon wafers of different sizes are manufactured each year worldwide [Tricard, 1998]. In year 2005, worldwide revenue generated by silicon wafers was $8.3 billion [Van et al., 2006], and worldwide sales of semiconductors reached a record $235 billion [Norwood et al., 2006].

The circuits will be printed on the silicon wafers by lithographic processes. Therefore, silicon wafers must be very flat. Wafer flatness directly impacts device line-width capability, process latitude, yield, and throughput [Kulkarni et al., 2001; Oh et al., 2001]. Flatter wafers are increasingly demanded because the feature sizes of semiconductor devices will continue to decrease [Ravi, 1999].

1.2 Silicon Wafer Manufacturing

The main processes in manufacturing of silicon wafers are shown in Fig. 1.1 [Bawa et al., 1995; Fukami et al., 1997; Pei et al., 1999; Tonshoff et al., 1994].

The cylindrical, single-crystal ingot undergoes a series of process steps to transform it into wafers that meet stringent specifications for semiconductor manufacturing [Bawa et al., 1995; Fukami et al., 1997; Pei et al., 1999; Tonshoff et al., 1994].

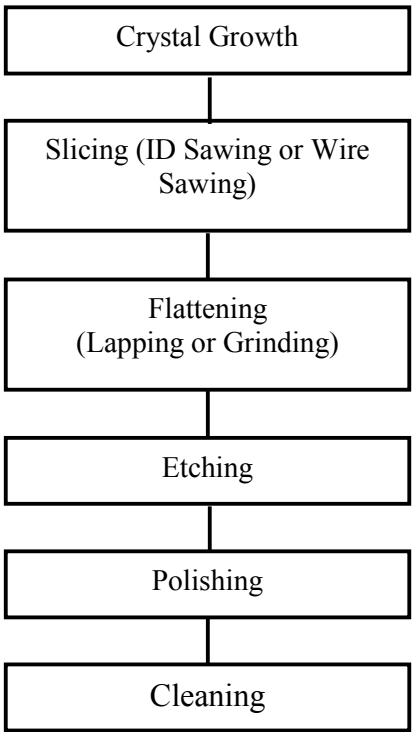
Wafer slicing is the first step after crystal growth. Slicing is to slice a silicon ingot into wafers of thin disk shape that have required thickness.

Lapping/grinding removes a certain amount of silicon from the wafer surfaces that have cracks or other damage induced in the slicing process, and assures a flat surface. Wafers are then etched in a chemically active reagent to remove any crystal damage induced by lapping/grinding.

Polishing is a chemical/mechanical process that smoothes the uneven surface left by the etching processes and makes the wafer flat and smooth enough to support photolithography.

Cleaning is to remove the polishing agent or dust particles from the wafer surfaces.

Figure 1.1 The Major Manufacturing Processes of Silicon Wafers



1.3 Objectives of the Thesis

The ever-increasing demand for high-performance microelectronic devices has motivated the semiconductor industry to design and manufacture integrated circuits with smaller feature size, denser packing, and multi-layer interconnects. The shrinking line width of the new integrated circuits requires a flatter surface on the silicon wafer. As the final material removal step in manufacturing of silicon wafers, chemical mechanical polishing (CMP) can produce excellent local and global planarization at low cost. Grinding is also an important material removal process for the wafers to obtain the desired thickness and good flatness. Improving the performance of CMP and grinding process is always needed to meet the ever-increasing stringent demand of wafer flatness. The goal of this thesis is to further understand CMP and grinding of silicon wafers in order to improve wafer flatness. The specific issues addressed in this thesis include:

How is the surface undulation on wafer surface removed over time in CMP?

How can the global and local flatness be improved in CMP?

How can the poor flatness at the wafer center be improved in grinding?

1.4 Outline of the Thesis

This thesis will be divided into nine chapters.

Following Chapter 1, Chapter 2 provides a review on CMP and grinding of silicon wafers. The state of the art of the CMP modeling and experimental study on silicon wafers are reviewed. The study on grinding of silicon wafers is also reviewed. Moreover, the unsolved problems are discussed.

A Finite Element Analysis (FEA) model of CMP is developed to study the wafer surface undulation in Chapter 3. The effects of influencing factors (including Young's modulus and Poisson's ratio of the polishing pad, thickness of the pad, and polishing pressure) on the wafer flatness are investigated.

Chapter 4 presents an analysis on the wafer local flatness problem - edge effect in CMP. The effects of the properties of polishing pad and carrier film on the distributions of the stress on the wafer surface are investigated.

Chapter 5 focuses on the global flatness problems – tapering in CMP. The effects of offsets between the pad and the carrier (block), and between the carrier (block) and the pad ring are analyzed by finite element analysis.

Chapter 6 presents the experimental study on the CMP of silicon wafers. The effects of the process variables (including wafer rotation speed, pad rotation speed, the temperature of the cooling wafer in polishing table, polishing pressure, and the slurry flow rate) on material removal rate (MRR) in polishing of silicon wafers are studied.

In Chapter 7, FEA models are conducted to study the effects of the carrier front surface and the back pressure on the wafer global shape.

An investigation on the central dimple generation mechanism is carried out in Chapter 8. This study provides a practical guidance in industry.

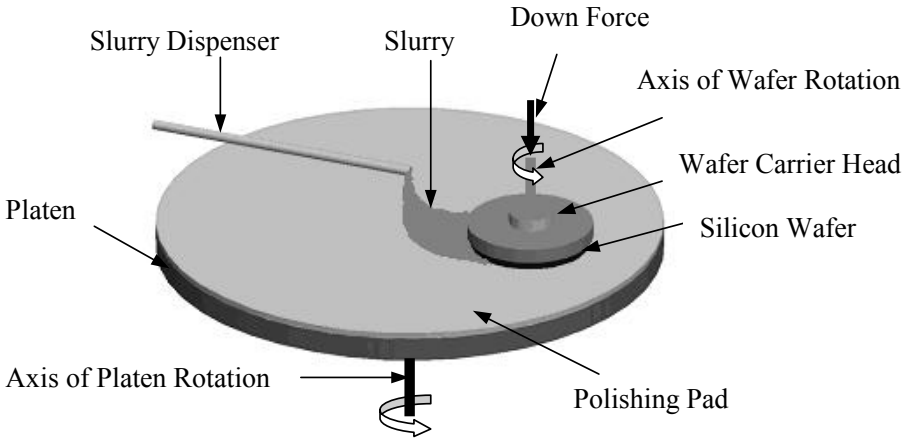
Chapter 9 gives the conclusions and the contributions of this thesis.

CHAPTER 2 - Literature Review

2.1 Chemical Mechanical Polishing

Chemical mechanical polishing is the final material removal step in manufacturing of silicon wafers. It is also used in IC manufacturing between operations to smooth and even the surface of the wafer. The CMP process consists of moving the wafer surfaces against a pad that provides support against the wafer surface. The pad experiences the pressure exerted on the wafer, and carries slurry between the wafer surface and pad [Steigerwald et al, 1997]. The polishing pad attached on the platen rotates either in the same direction or in the opposite direction to wafer rotation. The carrier film is on the backside of the wafer transferring the down force to the wafer. The retainer ring is used to hold the wafer into the right place and change the deformation of the pad. Fig. 2.1 is a schematic of a typical CMP process. The material removal in CMP occurs as a consequence of a combination of chemical reaction of the slurry chemicals with the silicon wafer surface and the repeated mechanical interaction between the pad and the silicon wafer.

Figure 2.1 A Schematic of a CMP Process.



Chemical–mechanical polishing (CMP), also known as chemical–mechanical planarization, has emerged as the fastest-growing operation in the semiconductor manufacturing

industry in the past decade, and it is expected to show equally explosive growth in the future [Braun, 2001]. However, CMP is a complicated process that has only a limited understanding from a fundamental scientific viewpoint and remains un-optimized. To get the benefits of CMP of silicon wafers, it is necessary to generate a more through research on the fundamental mechanism.

A mechanistic understanding of the CMP process can be developed by studying the wafer-pad-slurry interactions that occur at both the microscale and nanoscale [Lee et al., 2002; Mahajan et al, 1999]. At the microscale, the rough pad carrying the particle-based slurry interacts with the surface of the wafer. It is generally believed that the particles, which are between the wafer and the pad, participate in a mechanical abrasion process that results in material removal. At the nanoscale, the kinetics of the formation and removal of the thin surface layer controls CMP output parameters such as removal rate, surface planarity and surface directivity. Although the CMP process is intuitively quite simple, achieving a more detailed understanding has been limited primarily by the large number of input variables in the polishing process. They include slurry variables (such as particles and chemicals), pad variables, and tool variables (down pressure and linear velocity) [Steigerwald et al, 1997]. The total number of variables can exceed 20, making the process difficult to understand and control. Time-dependent contributions by some of these variables cause further complexities in the process.

2.2 Modeling Study of the CMP Material Removal Mechanism

2.2.1 Preston's Equation

The basic theory of the material removal in CMP is Preston's equation [Preston, 1927] where the material removal rate (MRR) is proportional to the applied load and the relative velocity between the wafer and the pad:

$$MRR = K \cdot P \cdot V \tag{2.1}$$

The surface chemistry, solution chemistry, and abrasion effects are combined into the Preston coefficient K. P is the polishing pressure applied on backside of wafer surface. V is the relative speed between the wafer and polishing pad. Observed removal rate profiles are usually proportional to the applied down pressure. However, even though a uniformly distributed

pressure is applied during polishing, the experimentally observed removal rate changes from the center to the edge. This NU (Non uniformity) is not described by Preston's equation [Srinivasa-Murthy et al., 1997].

2.2.2 Study on Stress Distribution on Wafer Surface and Edge Effect

Many different models are available in the literature to study the material removal mechanisms of the CMP process. Some models have taken the purely fluid mechanics approach in which the polishing pad and the wafer are separated by the slurry layer [Runnels, 1994]. Another approach to analyze the CMP process is based on the contact mechanics [Burke, 1991; Sivaram et al., 1994; Warnock, 1991]. Runnels and Renteln [1997] proposed an axisymmetric model with the assumption that the pad was elastic and the slurry flow could be neglected. The deformation of the pad and the stress distribution at the edge were analyzed. The results showed that the material removal rate was strongly affected by stresses. Srinivasa-Murthy et al. [1997] developed a 3D finite element model to study the stresses on wafer surface. The result showed that the von-Mises stress was uniform near the center of the wafer and increased towards the edge, which is very similar to the modeling work by Wang et al. [1997], with a 2D FEA model. Xin also used the static FEA model to study the contact pressure (surface normal stress) distribution between the pad and wafer [Xin, 1998]. He assumed that the process was static and the pad was elastic. The model revealed the pressure abrupt increment at the wafer peripheral portion. The amplitude of the pressure abruptness varied significantly with properties of the polishing pad. Moreover, the effects of the retainer ring geometry on the pressure distribution were also simulated. However, the simulation results would be different if different carrier films were used, which was not included in his research. Lin developed a 2D axisymmetric quasic-static finite element model to study the von-Mises stress distribution on wafer surface [Lin et al., 2004]. The theory was based on the principle minimum total potential energy and axisymmetric elastic stress-strain relations. He showed that the von-Mises stress distribution decreased in a large range and increased dramatically and peaked significantly at the edge. Tseng et al. [1998] used a thin plate as a wafer to calculate the stress distribution between the wafer and pad by means of the strain energy and Hertzian contact theory. Castillo-Mejia et al. [2000] also used Finite Element Method to calculate the von-Mises stress distribution on the SiO_2 wafer surface.

The results showed that the pressure on the retainer ring and the gap size had important impacts on the stress that was consistent with the experimental result. Sasaki et al. [1998] investigated the pressure distribution under a wafer, and the influences of the back film, wafer chamfer, and retainer ring on the pressure distribution using a FEA model. Fu et al. [2002; 2001] derived an analytical solution for the interface pressure distribution based on an elastic/viscoelastic half-space assumption for the pad. The result showed that the pad deformation affected the material removal rate. In 2005, they also conducted the research on the relationship between the wafer surface pressure distribution and wafer backside loading [Fu et al., 2005]. The results showed that under uniform pressure applied on wafer backside, irregularity of the dramatically increase of the pressure at the wafer edge. Xie et al. [2005] studied the effect of pad Young's modulus, the applied pressure, and the gap between the retainer ring and the wafer edge on the wafer edge geometry. Basically, bending of the wafer and the influence of the pad were the possible mechanisms as the potential causes of the edge effect [Baker, 1996]. Since the carrier film serves as cushion at of wafer backside, it also plays an important role in the wafer deformation. However, there are few reports in the literature regarding how the carrier film properties affect the edge effect.

2.2.3 Study on MRR

Some modifications of Preston's equation were presented to further understand polishing process [Tseng et al., 1997]. But all of those efforts only include the effects of polishing pressure and rotation speed on MRR. In 2005, Jeng et al. [2005] presented a model considering the effects of abrasive particles located between the polishing interfaces, which were not considered in Preston's equation. Based on the model, the effects of applied down force, slurry particle size, wafer surface hardness, and slurry concentration were studied. The effects of those parameters were also studied in Che's scratch intersection model [Che et al., 2005]. Fu et al. [2001; 2002] proposed models predicting the material removal rate based on the viscoelatstic pad deformation and plastic pad deformation respectively. The effects of abrasive particle size and concentration on removal rate were compared with the experimental results. The model Luo et al. [2001] proposed to predict the MRR of polishing process integrated not only the polishing pressure and the velocity but also other important parameters including the wafer hardness, pad hardness, pad

roughness, abrasive size, and the abrasive geometry. The modeling research gave good predictions of the effects of the input parameters including pressure, velocity, slurry properties and even the pad and wafer properties. However, they all are based on some assumptions which do not necessarily apply to every material of polishing pads and wafers.

2.3 Experimental Study on MRR in CMP

Experimental investigations give more straightforward understanding of the effects of the process parameters. Table 2.1 summarizes reported experimental work on the polishing rate of SiO_2, Cu, W, and Al. Although silicon wafers are the major substrates, the literature search shows that few reported the effects of process variables on material removal rate in polishing of silicon wafers. Forsberg [2005] reported an experimental study on the effects of polishing parameters on material removal rate of (1 0 0) silicon wafers. The removal rate increases with applied pressure, plate speed, and slurry silica content. The effect of slurry viscosity was also studied by Mullany et al., [2002]. Wafer shape and pad shape were also considered as factors influencing the material removal rate [Mcgrath et al., 2003].

Table 2.1 Polishing Removal Rate of Different Materials in Reported Work

Material	Experimental studies
SiO_2	Choi et al., 2004; Zhuang et al., 2005
Cu	Gotkis et al., 2001; VanKranenburg et al., 2000; Liang et al., 2000; Minamihaba et al., 2004
W	Kaufman et al.; 1991, Wang et al., 1999; Larsen et al., 1999
Al	Tsai et al., 1998
Si_3N_4	Jiang et al., 1998; Zhuang et al., 2005
Si	Sasaki et al., 2002; Tan, 2005; Forsberg, 2005

2.4 Measurement Methods for Polishing Pads

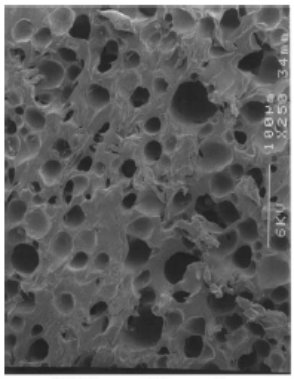
2.4.1 Materials and Structure of the Polishing Pad

The polishing pad is the key media enabling the transfer of mechanical forces to the surface being polished. It directly affects the material removal rate and its uniformity. The structure and material properties determine the polish rate and planarization ability. In general, polishing pad is composed of either a matrix of cast polyurethane foam with filler material to control hardness or polyurethane impregnated felts [Steigerwald et al., 1997]. The polishing pads are porous, having between 30% and 35% void content in volume [Wang, 1997]. Fig. 2.2 shows SEM microscope cross-section views of IC1000 polymer pad and a resilient soft SUBA IV sub pad (Rodel, Newark, DE). The rigid IC1000 pad made of mircoporous polyurethane (viscoelastic) material has a closed cell structure with hollow spherical micropores (Fig. 2.2a) [Machinski, 2001]. The pores on the pad can hold the slurry and transport the slurry to all part of the wafer. SUBA IV pads are made of polyurethane impregnated polyester felts and have a rougher surface. The most popular type of pads is a combination of the IC1000 and SUBA IV pads in a stacked form [Koizumi et al., 2000]. The pad fiber structure and height affect the transport of slurry and the local pressure gradients at the surface. Basically, the pores and the fibers could be accurately controlled when growing the polishing pad. The foam properties are a function of the polymer material and structure. Foam density, open or closed cells and cell shape, along with the polymer properties determine the pad properties [Bajaj et al., 1994]. Pore size may also affect the mechanical properties of the pad. With more and more wafers are polished, the slurry particles and polished silicon particles can be trapped in the surface pores, resulting in the pad surface glazing or degradation. Pad conditioning can refresh the pad surface by using a diamond-studded disk to grind over the pad surface. However, the pad thickness is thinner after conditioning which results in the poor repeatability from run to run and may even damage the wafer, and the pad life is shortened as well [Lawing, 2002].

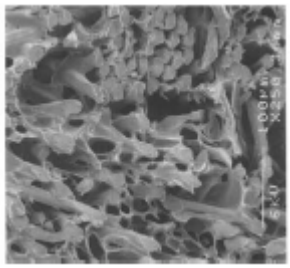
Observed removal rate profiles are usually proportional to the applied down pressure according to Preston's equation. It was also observed that contact pressure distribution on the wafer surface especially at the wafer edge was significantly affected by the thickness of polishing pad (Fig. 2.3) [Xin, 1998]. And also because pad conditioning has become essential to material removal uniformity of wafer surface and pad life, pad thickness becomes one of the

most important issues during polishing process. As the pad thickness reduces, the pad deformation changes and the polishing ability decreases. Beside the thickness, the Young's modulus, and the viscous properties also change. Young's modulus determines the mechanical stability and flexibility of pads during polishing under the load and rotational constraints. According to the modeling work by Xin [1998] and Wang et al. [1997], the nonuniformity of material removal decreases with the Young's modulus increasing. The Young's modulus of polishing pad not only affects the amplitude of the contact stress but also the nonuniform range on the wafer surface (Fig. 2.4) [Xin, 1998]. The evaluation of pad Young's modulus becomes very important to understand the relationship between the pad properties and polishing quality. The measurement of the pad properties is very important to understand the polishing non-uniformity and to keep the polishing process stable and maintain high uniformity from wafer to wafer or within wafer. Hardness and compressibility have been found empirically to affect planarity on the wafer surface. The harder and the more non-compressible the pad is, the less it will bend and conform to the wafer surface to remove material at the low regions. The material removal rate is adversely affected by the pad hardness [Liu et al., 1996].

Figure 2.2 SEM Cross-Section Views of Two Pads [Machinski, 2001]



(a) IC 1000 pad



(b) SUBA IV pad

Figure 2.3 The Effect of Pad Thickness on Contact Pressure on Wafer Surface

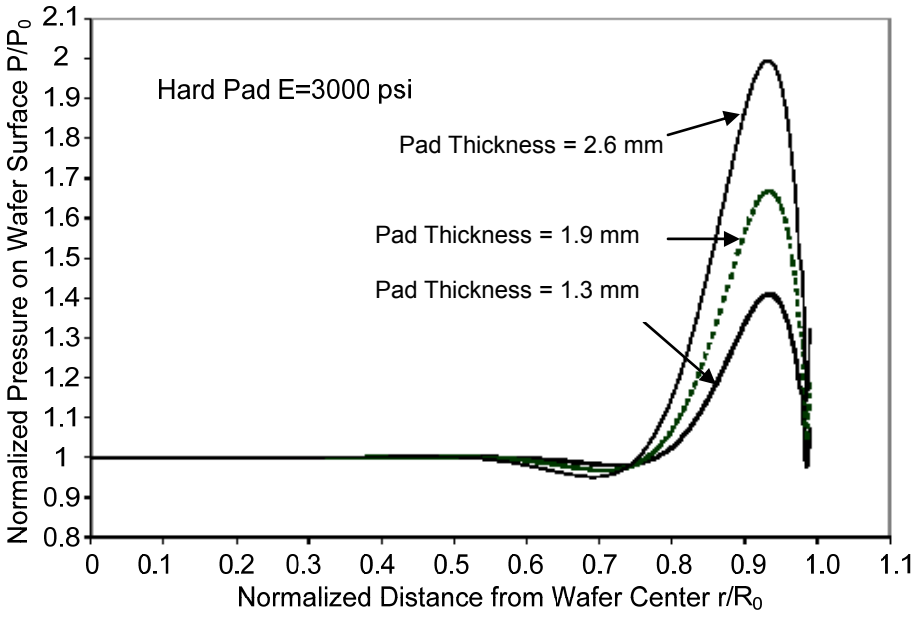
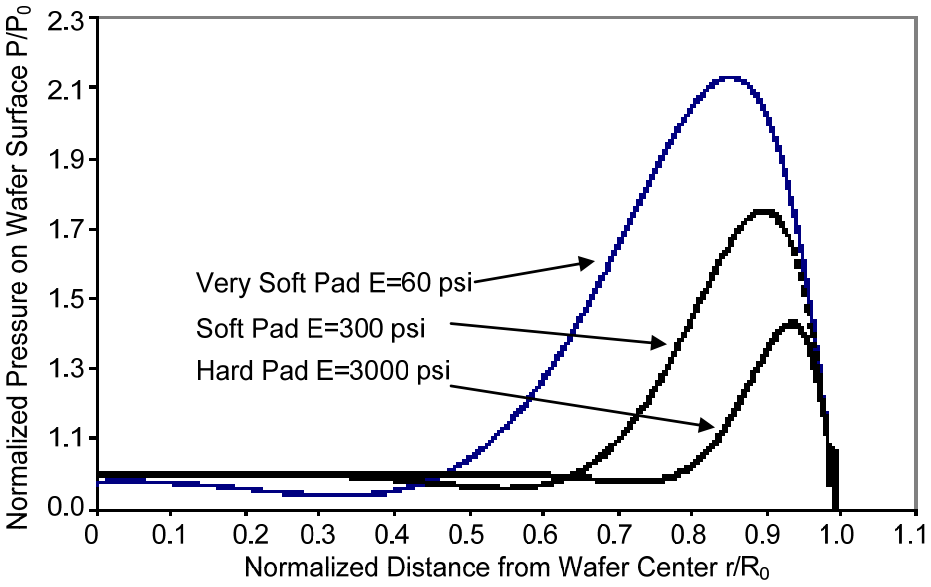


Figure 2.4 The Effect of Pad Young's Modulus on Contact Pressure Distribution on Wafer Surface

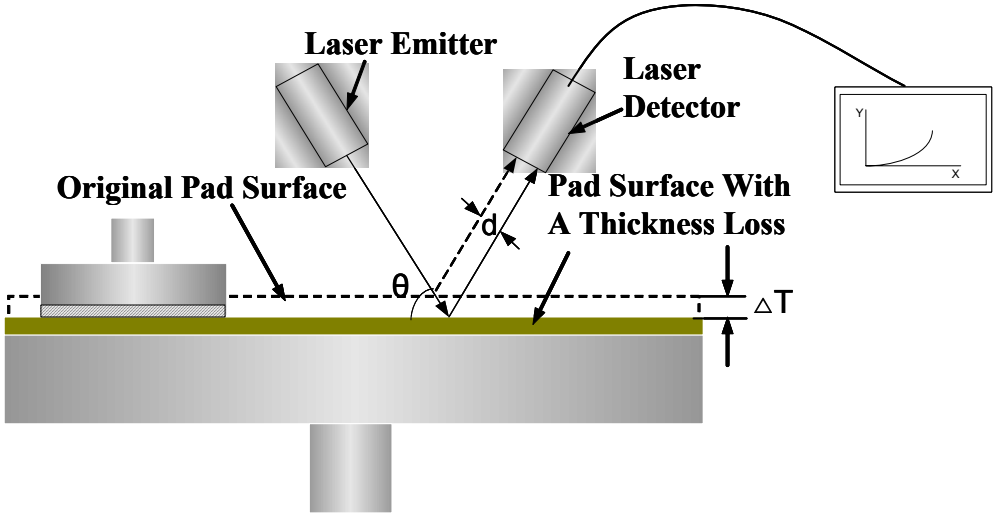


2.4.2 Methods of Monitoring Pad Thickness

The standard approach to determining the pad thickness consists of cutting out a radial piece of the pad, using a micrometer to measure the pad thickness directly. This is a destructive test.

Non-destructive tests were developed to monitor polishing pads since 1997. Meikle disclosed methods and apparatuses for measuring a change in the thickness of the polishing pad by using a laser beam detector [Meikle, 1997; Meikle et al., 1997; Meikle, 1998].

Figure 2.5 Laser Sensor Based Pad-Monitoring Method [Meikle, 1998]



The pad thickness is measured after a pad conditioning cycle. The measuring device (Fig. 2.5) is preferably a laser position sensor or a laser interferometer with an emitter and a detector. The laser beam shoots a laser beam onto the polishing pad. The laser beam reflects off the pad surface before and after thickness changing, and then is detected by the detector. The thickness change (ΔT) is calculated from the distance of the two reflected beams and the angle between the shooting beam and the pad surface:

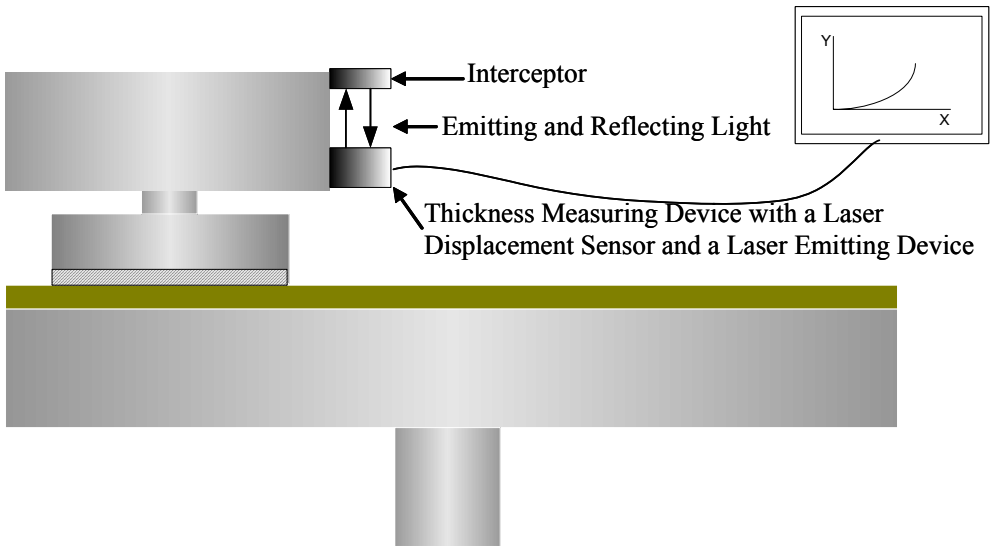
$$\Delta T = d \cdot \sin\theta \tag{2.2}$$

A disadvantage of this invention is that the thickness data were obtained from the discontinuous points on the pad. As the polishing slurry interfering with the pad surface, it is

difficult to determine which data point is valid. Furthermore, the thickness measurement is conducted before and after pad conditioning and cannot be realized during the CMP cycle.

Another invention using a laser sensor to monitor the pad thickness is reported in 2006 [Chuang, 2006]. The difference from the previous invention is that the measuring device is mounted on the polishing head (carrier) of the chemical mechanical polishing (CMP) machine monitoring the pad during a CMP cycle. The measuring device comprises a displacement sensor, a laser-emitting device, an interceptor, and a display device. The laser is emitted to the interceptor and reflected to the measuring device (Fig. 2.6). The measuring device computes the thickness of the polishing pad based on the reflection. The height of pad surface is detected to decide if the pad is thinner than the predetermined thickness so that the pad needs to be replaced. This invention achieves the in-situ measurement during the CMP cycle. But still only some specified points are measured.

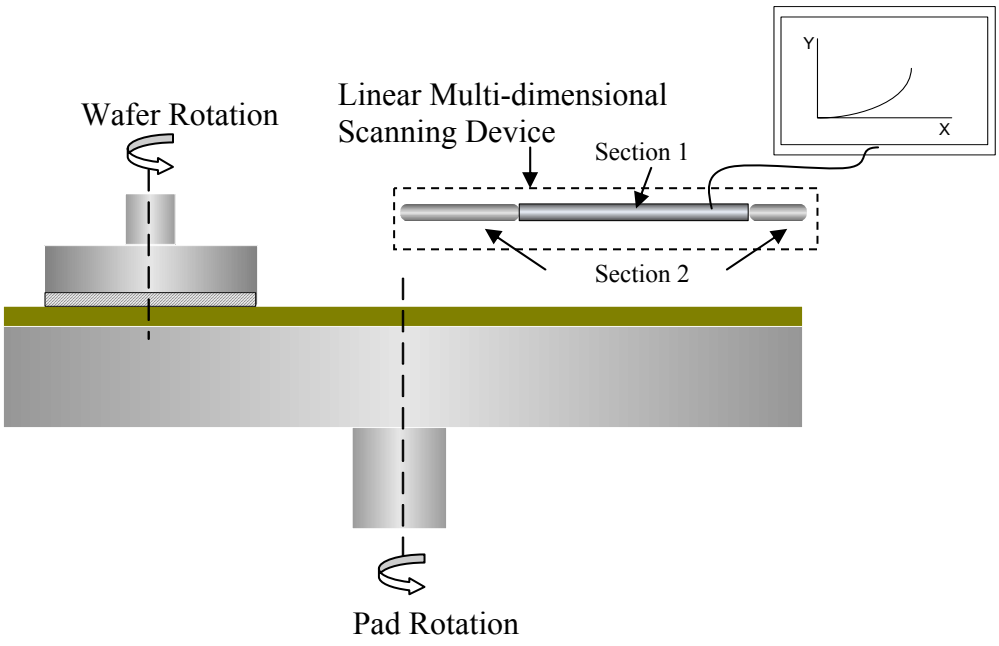
Figure 2.6 Laser Sensor Based Pad-Monitoring Device Installed in the Polisher [Chung, 2006]



Ho-Cheng et al. [2001] presented a linear multi-dimensional scanning device to monitor the polishing pad in a radial direction without overlapping the wafer. The scanning device includes two sections. In the first section, it scans a first portion of the polishing pad that is in intermittent contact with the wafer. In the second section, it scans a second portion of the

polishing pad that is never in contact with the semiconductor wafer during the CMP cycle (Fig. 2.7). The scanning device could be a 3D laser scanning system. After scanning the polishing pad surface, the profile is provided to the computer to determine if it needs to be changed. Although some thickness data are unreliable due to the polishing slurry interfering, they are easily excluded out of the profile information. The shortcoming is that they can be only used after the CMP cycle.

Figure 2.7 Linear Multi-dimensional Scanning Device for Monitoring Pad Surface [Ho-Cheng, 2001]



Nagai et al. [2003] also used Laser Focus Displacement Meter (LFDM, LT-8110 laser sensor head, Keyence Corp.) to monitor pad surface. The LFDM can be built in the equipment and the pad condition is observed without contacting the pad surface. The displacement and surface roughness are monitored by LFDM in-situ, which makes the dressing time adjusted and pad life prolonged.

In addition, ultrasound or electromagnetic radiation transmitters and receivers were used to measure the pad thickness change. Fisher et al. [2001] presented a patent utilizing ultrasound or electromagnetic radiation transmitters and receivers aligned to cover any portion of the radial

length of a polishing pad surface. Radiation wave signals from a single sensor or multiple sensors have a phase change or time delay compared to the reference signal that is obtained when the pad is new (Fig. 2.8). A change of pad thickness is measured by correlating the phase change (signal traveling distance difference) to the pad thickness change. Every sensor combines a radiation transducer and a radiation receiver. An analyzer capable of distinguishing the signal change sends the information to a controller that adjusts the CMP operation parameters accordingly.

Adebanjo et al. [2002] reported another non-destructive but contact method to in-situ measure the thickness loss of a polishing pad. Two rigid planar members are placed on the surfaces of the conditioned and non-conditioned sections of polishing pad respectively. Measurements are made using thickness gauge that is overhanging the depressed conditioned section and measures the step height between the planar members (Fig. 2.9). The measurement instruments may be repositioned and measurements repeated to obtain an average thickness loss. Although non-destructive measurements are performed, the apparatus contacts the pad unlike the laser displacement sensor.

Figure 2.8 Ultrasound or Electromagnetic Sensors for Monitoring Pad Surface [Fisher, 2001]

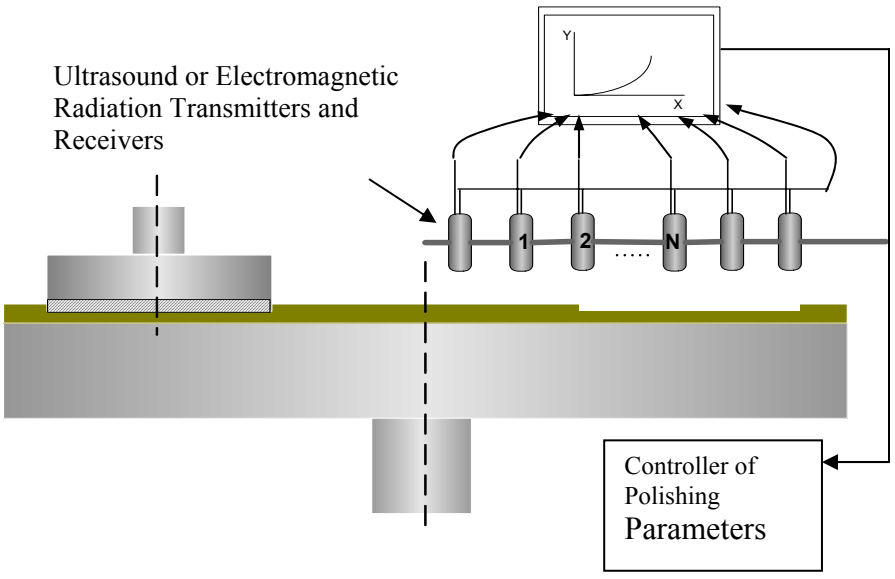
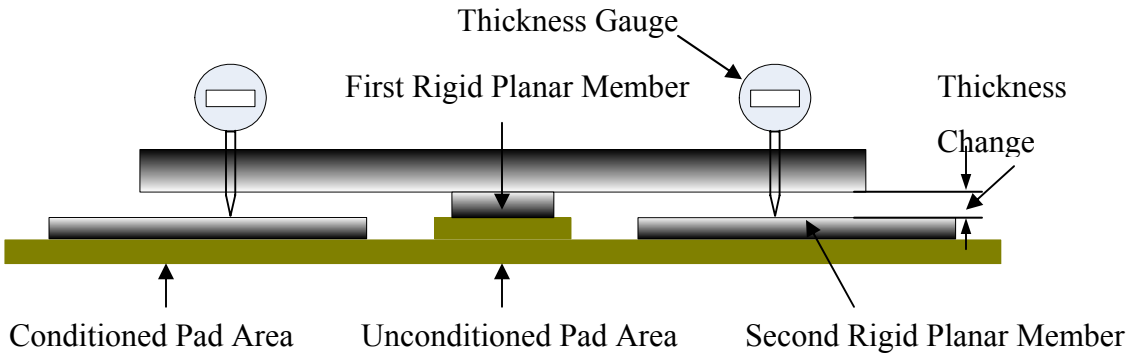


Figure 2.9 Contacting Method Monitoring Pad Thickness Change [Adebanjo et al. 2002]



PadProbe™ (Center for Tribology, Inc.) is another contact method. It shows high sensitivity in-situ or ex-situ monitoring pad wear. It is used effectively to know when to start and finish the pad conditioning or when to replace the pad instead of estimating the pad life by the number of polished wafers. Furthermore wafer-to-wafer uniformity of polishing is improved by maintaining the same pad condition. The PadProbe is small (Fig. 2.10) and very easy to install on the polisher [Center for Tribology Inc., 2006].

The different methods for monitoring pad thickness are summarized in Table 2.2.

Figure 2.10 PadProbe™ Installed in a Polisher [Center for Tribology Inc., 2006]

Table 2.2 Comparisons of the Apparatus for Monitoring Pad Thickness

Reference	Sensor	Contacting	During the CMP cycle	After a CMP cycle	Installed in a polisher	Thickness information
Meikle, 1997 Meikle et al., 1997 Meikle, 1998	Laser interferometer with emitter and detector	No	No	Yes	No	At specified locations
Chung, 2006	Laser emitting device, displacement sensor, and interceptor	No	Yes	Yes	Yes	At specified locations
Ho-Cheng, 2001	3D Engineering laser sensors along the radial directions	No	No	Yes	No	Pad Profile along the radial direction
Nagai et al., 2003	Laser Focus Displacement Meter (LFDM (LT-8100 Keyence Corp.))	No	No	Yes	Yes	Pad Profile along the radial direction
Fisher, 2001	Ultrasound or electromagnetic radiation transmitters and receivers	No	Yes	Yes	No	Pad Profile along the radial direction
Adebanjo, 2002	Thickness gauge plus two rigid planar members	Yes	No	Yes	No	Average thickness loss
Center for Tribology, Inc., 2006	PadProbe™	Yes	Yes	Yes	Yes	At specified locations

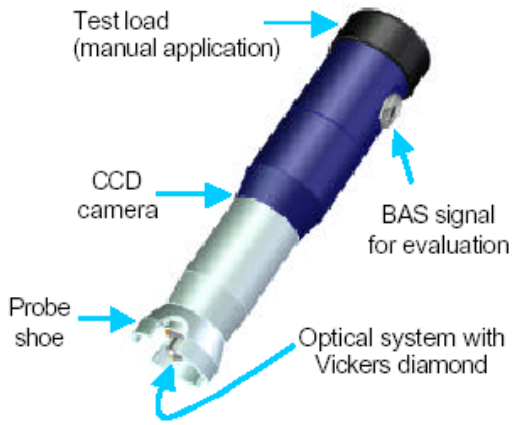
2.4.3 Methods for Hardness and Compressibility Measurements

Typically, polymer materials – unplasticized polyvinylchloride – have both Shore hardness and Rockwell hardness [Bolton, 1989]. The Shore hardness value is measured by the penetration of the Durometer indenter foot into the sample. The polymer material is usually soft and has resilience, so the indentation reading may change over time. Several standards (such as the ASTM test method designation ASTM D224000 and the related methods include ISO 7619

and ISO 868) are referenced to measure the Shore hardness. Other standards (such as ISO 2039-1 and DIN 53456) are generally used for the Rockwell hardness test [Online staff, 2007]. These conventional methods need a cut piece of the pad.

Portable testing devices have been developed that permit in-situ hardness measurements. TIV (Through Indenter Viewing Technique, also called Through Diamond Technique, Agfa NDT GmbH, Robert-Bosch-Str. 3, D-50354 Huerth, Germany) is one of the methods testing the hardness of the polishing pad in-situ [Frank, 2002]. The Vickers diamond indentation is evaluated by applying a certain load to the diamond penetrating into the material and the indentation size can be viewed through the diamond with an optical system having a CCD camera (Fig. 2.11).

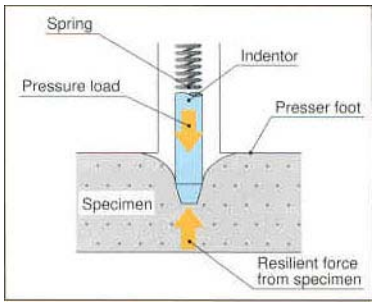
Figure 2.11 Schematic Description of the TIV Probe-Portable Hardness Tester [Frank, 2002]



Micro Photonics Inc. and Instron Corporation produce portable durometers that can be used to measure the hardness of polishing pad quickly (usually within 1 second) and without any damage on the part [Online staff, 2007]. The durometers is small enough to fit the palm of the hand (Fig. 2.12a). The indenter gives a distortion onto the surface of the sample with the presser foot and pressure produced by the spring load. The spring pushes the indenter into the sample and the indicator indicates the depth of penetration (Fig. 2.12b). The deeper the indentation is, the softer the material and the lower the indicator reading. The reading is shown either digital or analog. The portability of the hardness test makes it very convenient to evaluate the pad hardness.

Figure 2.12 Portable Durometer [Online Staff, 2007]

(a) Durometer



(b) Indenter

The compressibility of pad material, which is used as carrier film (Carrier films are mounted on the back of the wafers to hold the wafers in the wafer carriers during CMP) by Wang et al. [1999], was measured on SATEC (model 60HVL) tensile test machine [Online staff, 2007]. The pressure from 0 to 10 psi was applied on the top surface of the measured pad material at a speed of 0.005 in/s and then was maintained for 3 min. The pad material could be either dry or sprayed with water during testing. The machine records the vertical displacement of the top surface of a pad. The compressibility is calculated as the ratio of the displacement to the original pad thickness. The diagram of the machine is show in Fig. 2.13.

Figure 2.13 SATEC (Model 60HVL) Tensile Test Machine [Online staff, 2007]

2.4.4 Measurement of Elastic and Viscous-Elastic Properties

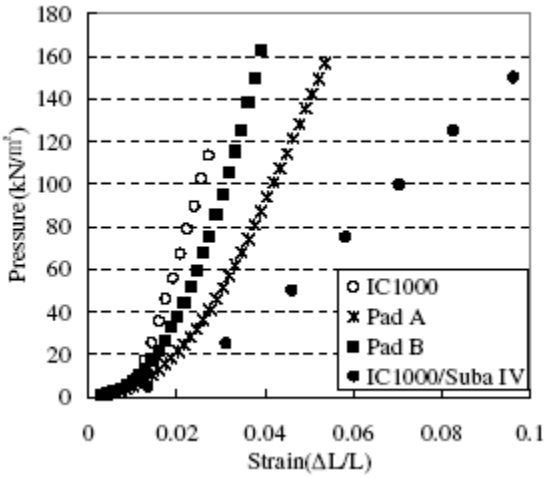
Static compression test is used to obtain stress-strain curve that determines the Young's modulus of polishing pad. Generally, the Young's modulus can be expressed as Hook's Law [Arthur et al., 1999]:

$$\sigma = E\varepsilon \tag{2.3}$$

Where σ is the stress, ε is strain (displacement/original thickness). During the test, the pad deformation was recorded as the load applied on the pad surface. The stress-strain curve is observed so that the Young's modulus is estimated for pad material. Several procedures and machines have been utilized to perform the compressive test.

Kim et al. [2003] used Universal material testing machine (UTM, Instron Co.) to study the Young's modulus. The result of the static compression test exhibits the nonlinear behavior from the stress-strain curve (Fig. 2.14).

Figure 2.14 Bilinear Stress-Strain Curve from Compression Test on CMP Pad [Kim et al. 2003]

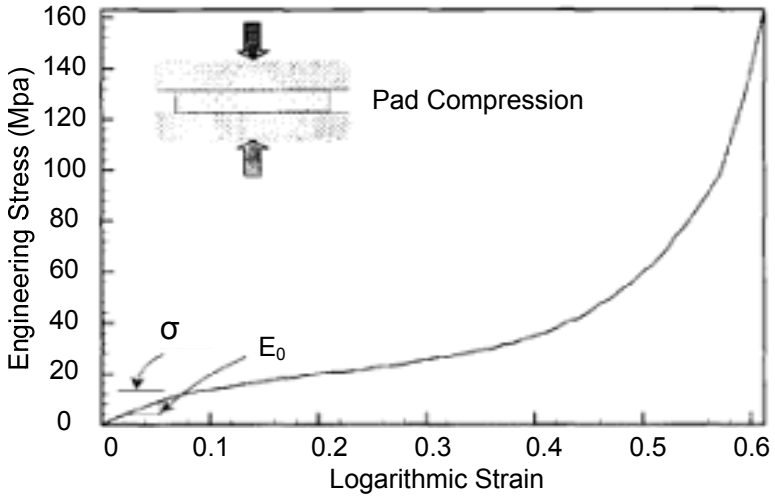


Instron 8162 (MTS systems Corp., Eden Prairie, MN) was also used by Bastawros et al. [2002] to get the compressive stress-strain curve. In their research, the dry pad sample size is 5.64×5.55×1.02 mm without the back packing. The result shows highly nonlinear relationship between the pressure and pad deformation (Fig. 2.15a).

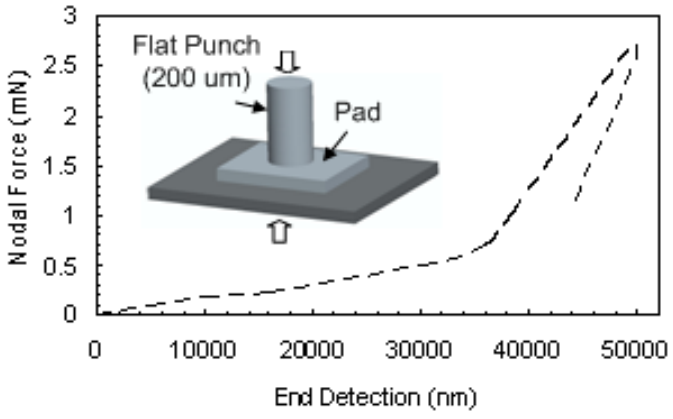
Nanoindentation technique is another widely used method to estimate the mechanical properties of the thin films [Fisher-Cripps, 2002]. Bastawros et al. [2002] performed the

Nanoindentation test in which a 200 um flat circular punch is pressed against the pad [Bastawros et al., 2002]. The result is shown in Fig. 2.15b. Zantye et al. [2005] used NANOTEST 600® [Online stuff, 2006] to characterize the mechanical properties of pad. The indention depth and load were recorded.

Figure 2.15 Stress-Strain Curve of Pad Using Instron 8162 and Nano-indentation Test [Bastawros et al., 2002]



(a) The macroscopic compressive stress-strain curve from Instron 8162



(b) The microscopic stress-strain curve from nano-indentation test

Pad deformation and load are also obtained by the test performed in a CMP tester model CP-4 (CETR, Mountain View, CA) equipped with CMP testing attachments. A 6" diameter pad sample is required as a stationary lower specimen. A 1" diameter stainless steel block was attached to the upper carriage. A compressive normal load was applied by lowering the steel block down to the pad with a speed of 5 μm/sec. A machine check with the similar procedure was conducted without a pad. Data of this pre-test was subtracted from the pad results [Online staff, 2006]. The pad sample could be either dry or with water soaked at an elevated temperature. Different punches such as a 2'' disc or a 10 mm steel ball could be used to compress the pads with the load [Online staff, 2006].

Table 2.3 gives a comparison and a summary about the methods to perform the compressive test. Almost all of the compressive tests need a pad sample that is a cut piece. None of the methods could perform measurement in-situ.

Table 2.3 Comparison of the Compression Test Machine

Machine		Load	Punch size	Sample condition
Universal material testing machine (UTM, instron Co.)	Single Column Models	0.5 kN (112 lbf) ~ 5 kN (1,100 lbs)	N/A	Wet, dry, with different temperature
	Dual Column Models	5kN (1,100 lbf) ~ 50 kN (11,250 lbf)		
Instron 8162 (MTS systems Corp., Eden Prairie, MN)		N/A	N/A	Dry, 5.64×5.55×1.02 mm
CMP tester mod. CP-4 (CETR, Mountain View, CA,)		At least 50 N	1" diameter stainless steel block, 2'' disc or a 10 mm steel ball	6" diameter pad sample
Nano-indentation (NANOTEST 600®)		0-500 mN	Microindenter (200 μm)	Hot stage for testing 0-500 °C
		0-20 N	Nanoindenter	

If the properties of the polishing pad are time independent, the polishing rate is uniform from wafer to wafer in the pad life. However, for real situations, changes in pad properties occur as polishing continues. Pad materials show both elastic and viscoelastic (time-dependent) deformation. Dynamic properties measurement accounting for both elastic and viscoelastic pad behavior should be done at the appropriate frequency. Dynamic Mechanical Analyzer (DMA) is used to evaluate viscoelastic materials, which exhibit frequency and temperature dependent mechanical properties [Steigerwald et al., 1997]. Basically, the theory of the DMA is:

$$E = E' + iE'' \tag{2.4}$$

$$\tan\delta = E''/E' \tag{2.5}$$

E is the combination of the storage modulus *E'* that indicates the Young's modulus and the loss modulus *E''* that indicates the viscous properties of the material. Tanδ is related to the material's ability to dissipate energy in the form of heat [Murayama, 1978].

TA Instruments DMA 2980 (New Castle, DE) was used to get the static and dynamic mechanical properties of polishing pads [Kumar et al., 2001; Charns et al., 2005; Li et al., 2000; Lu et al., 2003]. The pad samples could be measured under different conditions: fresh pad, soaked in the slurry, and after polishing cycles and different frequency and temperature to understand the intrinsic polishing mechanism [Charns et al., 2005]. Fig. 2.16 is the DMA apparatus in a tension mode (it could be in a compression mode too). An oscillating force at a certain frequency is applied to a sample and the resulting displacement of the sample is measured, from which the modulus and the damping factor can be calculated. The material response is monitored at a constant frequency and constant amplitude of deformation, and data are recorded at defined time intervals [TA Instruments, 2001]. Fig. 2.17 illustrates the stress and strain evolution when DMA is performed [Schlesing et al., 2004].

The Universal Nano+Micro materials Test UNMT-1 (Fig. 2.18) (CETR, Mountain View, CA) was used to determine the storage and loss moduli across the pad material at different locations and different sample shape [Online staff, 2006]. Force and displacement signals were recorded at frequencies at several locations across the sample. Both mirco and nano heads are used as the indentation head.

Figure 2.16 A Schematic Representation of DMA with the Specific Clamp Used for Tension Mode Experiments [TA Instruments, 2001]

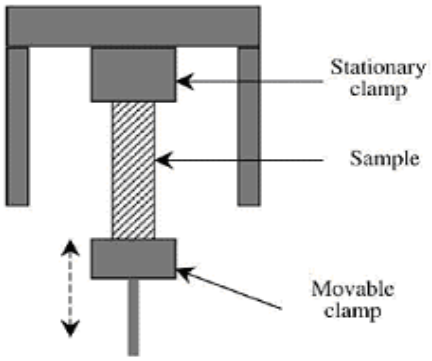


Figure 2.17 Dynamic Mechanical Analyzer in Tensile and Parallel Plate Mode [TA Instruments, 2001]

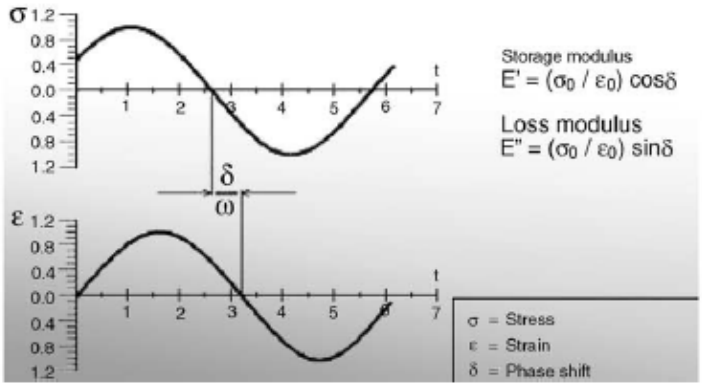
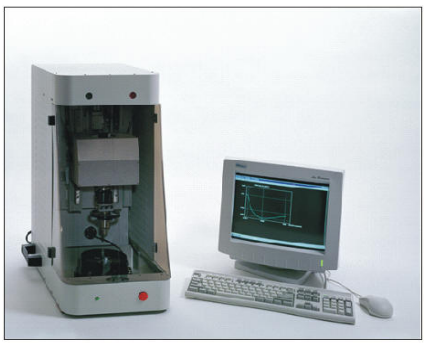


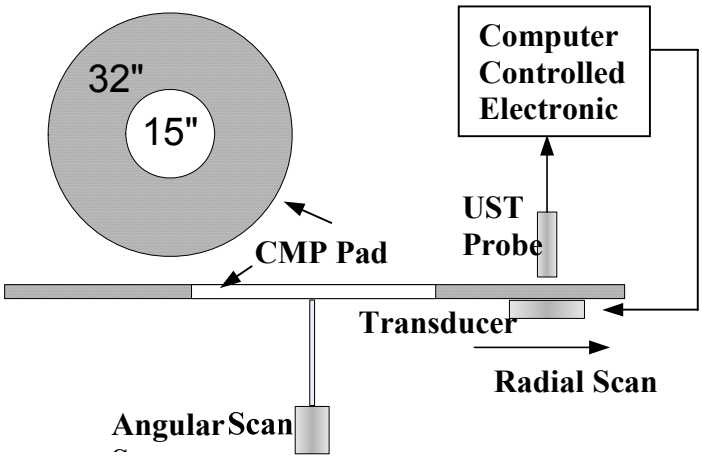
Figure 2.18 Nano+Micro Tester UNMT-1 [Online staff, 2007]



2.4.5 Measurement of Pad Density

A non-destructive Ultrasound Testing (UST) technique was developed at the Center for Microelectronics Research (University of South Florida). It is used to map variation of specific gravity and to determine the nonuniformity within a single pad [Totzke, 2000]. The principle is that the areas with different density and visco-elasticity have different adsorption to ultrasound. A resonance circular piezoelectric transducer (as an emitter of the acoustic vibration of the desired frequency and amplitude) and an acoustic probe (as a receiver of the ultrasonic vibrations) are the two key components of the UST system [Zantye et al., 2004]. The transducer operates at a certain frequency and moves along the radial direction in which the probe moves simultaneously (Fig. 2.19). The UST amplitude value across the pad surface or with the time shows the pad thickness and density non-uniformity [Totzke et al., 2001].

Figure 2.19 A Schematic Diagram for the UST System [Zantye et al., 2004]



As one of the most important factors in chemical mechanical polishing (CMP) of silicon wafers, the polishing pad plays a critical role in planarity. This section has reviewed the measurement methods of the polishing pad properties including pad thickness, hardness, and Young's modulus. The disadvantages and advantages of the measurement methods are summarized in Table 2.1 and Table 2.2. Most of the methods could be used to measure the thickness change of the polishing pad after a CMP cycle. However, measuring the polishing pad properties during CMP cycle is more efficient to silicon wafer manufacturing. The methods

presented in two patents [Chung, 2006; Fisher, 2001] are more preferable for in-situ measurements. PadProbe™ (Center for Tribology, Inc.) is the best procedure to measure the pad thickness change. It is small, easy to be installed on CMP machines, and measures the pad in-situ, which might be the future direction to develop new methods for measuring thickness change of the polishing pad. Among the methods for measuring the pad hardness, both TIV and portable durometers are very convenient for in-situ measurement. However, the polishing pad has to be cut into pieces if measuring the Young's modulus. Developing in-situ and non-destructive measurement methods for pad Young's modulus will be very beneficial to wafer polishing.

2.5 Flatness of Silicon Wafer in Grinding

Grinding is a process that flattens wafers and removes the damage caused by previous processes. Fig. 2.20 illustrates wafer grinding process. Grinding wheels are diamond cup-wheels. The wafer is held on a porous ceramic chuck by means of vacuum. The rotation axis for the grinding wheel is offset by a distance of the wheel radius relative to the rotation axis for the wafer. During grinding, the grinding wheel and the wafer rotate about their own rotation axes simultaneously, and the wheel is fed towards the wafer along its axis [Pei et al., 1999; Liu et al., 2002; Vandamme et al., 2001]. After the wafer front side is ground, the grinder flips the wafer over and continues to grind the backside. The advantages of single side grinding over lapping for include [Liu, et al., 2002; Vandamme, et al. 2001; Kato et al., 1998]:

(1) It uses fixed-abrasive grinding wheels instead of abrasive slurry so the cost of consumables per wafer is lower;

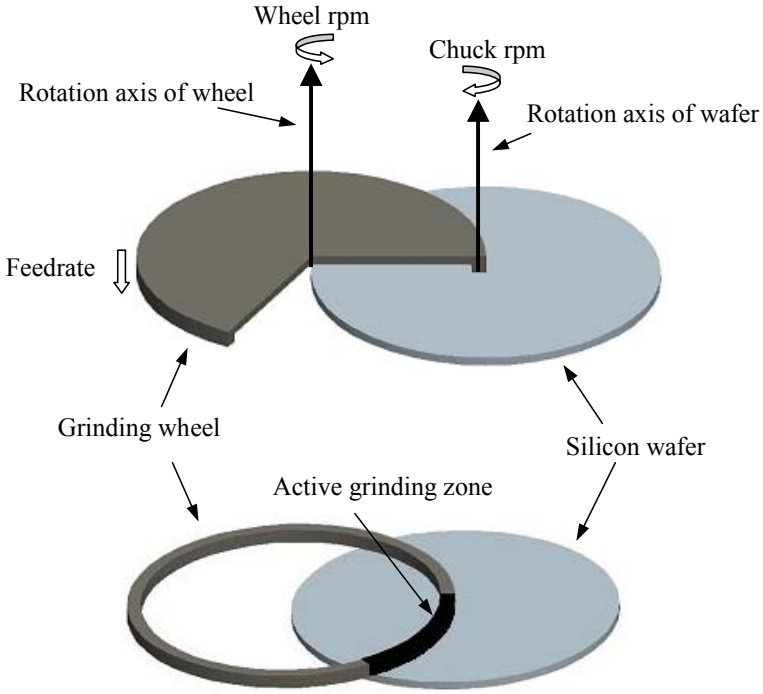
(2) Fixed-abrasive grinding wheels are more benign to the environment than lapping slurry;

(3) It has higher throughput (the number of wafers processed within the unit of time);

(4) It is fully automatic; and

(5) It grinds one wafer at a time.

Figure 2.20 Illustration of Wafer Grinding



As the starting materials for fabrication of most ICs, silicon wafers must be very flat so that the circuits could be printed on them by lithographic processes accurately. Flatness is one of the major topics in silicon wafer grinding [Pei et al., 2001] since the flatness of the ground wafers directly impacts the final flatness of the finished wafers [Jeong et al., 1996].

The flatness is affected by various process parameters and wheel properties in grinding. Efforts have made to understand the relationship between the process parameters and the wafer shape and thickness non uniformity that are directly related to the surface flatness.

Hinzen and Ripper [1993] reported that the material removal non uniformity that causes the inaccuracy of the ground wafer's thickness distribution is determined by positional stability of the cup-wheel axis relative to the wafer axis directly. However, the improper inclinations of the rotational axes [Tonshoff et al., 1990; Hinzen and Ripper, 1993] are related to grinding force, thermal influence, and machine tolerance and insufficient. Tso and Teng [2003] stated that flatness of the wafer deteriorates due to thermal distortion and the deflection of the cup wheel. The cup-wheel axis must be slightly justified to ensure good flatness on the ground wafer. Zhou et al. [2003] also reported that the cutting path density also affects the wafer's global flatness,

resulting in concave wafer shape. They suggested that tilting the axis of the wafer slightly inclining against the axis of the wheel will help to achieve the flat wafer shape.

Matsui and Horiuchi [1991] found that wafer periphery became thicker than the center by using infeed grinding. They claimed that this phenomenon is caused by elastic deformation of the wheel. The grinding force on the wheel is smaller at the center and larger at the wafer periphery. Thus, the elastic deformation of wheel segment is smaller at the wafer center, and larger at the wafer periphery. Therefore, the wafer's thickness increases with wafer radial position. In order to improve the flatness of the wafer, decreasing the difference of the speed of every point along the wafer radius or the grinding force within a wafer (such as by using spark-out grinding in the end) and using grinding wheel with high contact stiffness (such as vitrified bond) are two recommended actions from them.

CHAPTER 3 - Finite Element Analysis on CMP of Silicon Wafers: Surface Undulation

3.1 Introduction

The material removal in CMP occurs as a consequence of a combination of chemical reaction of the slurry chemicals with the silicon wafer surface and the repeated mechanical interaction between the pad and the silicon wafer with the abrasive particles in between. As the first attempt of a series, only the mechanical interaction between the pad and the silicon wafer is considered in the modeling here. Based on Preston's equation, a finite element model is built to study the effects of several variables on the polishing time to achieve certain flatness, say less than 30 nm in peak to valley value.

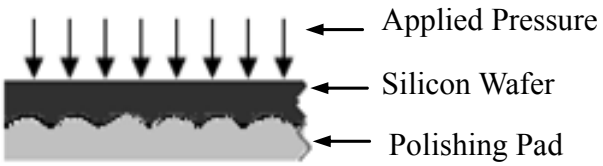
This chapter is organized into 4 sections. Following this introduction section, section 3.2 will provide some background information about the material removal mechanisms of CMP of silicon wafers. In section 3.3, procedures to build the finite element model will be presented. The developed model will be used in section 3.4 to predict the relationships between the influencing factors and the polishing time. Section 3.5 is the chapter summary.

3.2 Material Removal Mechanisms

Different models are available in the literature to study the material removal mechanisms of the CMP process [Runnels, et al., 1994, Burke, 1991, Warnock, 11991]. The basic material removal theory is still Preston's equation [Preston, 1927] where the material removal rate (MRR) is proportional to the applied unit load and the relative velocity between the wafer and the pad:

Achieving planarization on a wafer surface is to reduce the surface undulation of the silicon wafer. The contact pressure distribution at the wafer-pad interface plays a very important role in removing the surface undulation of the wafer. If a two-dimensional model is considered, the pad is deformed along the profile of the wafer surface under the applied pressure. Fig. 3.1 shows the pad deformation along the wafer surface undulation.

Figure 3.1 Pad Contact with Silicon Wafer



The material removal is defined as equation (3.1)

$$\Delta H = Y_{t+\Delta t} - Y_t \tag{3.1}$$

Where *Yt* is the wafer profile at time *t* and $Yt + \Delta t$ is the wafer profile after time period Δt. ΔH is the material removal. According to Preston's equation, the relationship between material removal rate (*MRR*) and contact pressure can be expressed as equations (3.2) and (3.3),

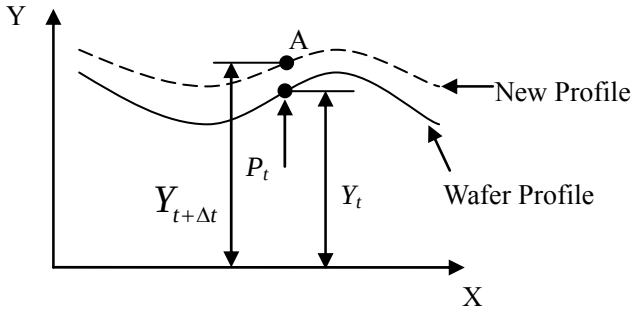
$$MRR = \frac{\Delta H}{\Delta t} = K \cdot P \cdot V \tag{3.2}$$

From (3.1) and (3.2),

$$Y_{t+\Delta t} = Y_t + KVP_t \cdot \Delta t \tag{3.3}$$

Referring to the illustrations in Fig. 3.2, it can be seen that *Pt* (the contact pressure between the wafer and the pad) is the key parameter to get the planarized surface.

Figure 3.2 Illustration of the Material Removal



3.3 The Finite Element Model

Commercial software, ANSYS (ANSYS Inc., Canonsburg, PA), was used for the contact pressure analysis. The analysis flow chart is shown in Fig. 3.3.

Fig. 3.4 schematically displays the two-dimensional (2D) model. Note that the amplitude and the wavelength of the surface undulation on the wafer are greatly exaggerated for illustration purposes. To simplify the problem, the surface undulation of the wafer is assumed to have a sinusoidal profile when viewing the cross section of the wafer. Building the 2D finite element model of wafer chemical mechanical polishing involves four main steps: building the 2D model; meshing; creating contact elements for the wafer-pad contacts; and imposing boundary conditions. The 8-node 2D elements (PLANE82) that provide more accurate results than the 4-node 2D elements (PLANE42) in ANSYS were used. 2D contact elements were used to model the wafer-pad contacts.

The finite element model was based on the following assumptions and simplifications:

1. The CMP process was modeled as a quasi-static problem (i.e., any dynamic effects were ignored), since the focus of this study was the contact pressure caused by the elastic deformation of the pad.

2. Since silicon wafers' Young's modulus is 135 GPa, much higher than the polishing pad's Young's modulus (3 to 30 MPa), the silicon wafer was modeled as a rigid body. Contact elements were used to model the wafer-pad interface. The contact elements for the wafer-pad pair were of rigid-flexible type.

3. The number of the surface undulation waves is infinite. So the deformation and the contact pressure distribution along every single wave are same. So only one wave is used in the model.

4. The 2D model is assumed as a plane strain problem because the diameter of the wafer is much larger than the amplitude of the surface undulation.

5. The CMP process is a very complicated process, which combines the chemical and mechanical actions among the silicon wafer, the polishing pad, the slurry fluid, and even the particles in the fluid. But this study focuses on the contact pressure, thus only mechanical factors such as the mechanical properties of the pad are considered and the chemical factors are ignored. Furthermore, the factors related to the slurry fluid are also ignored.

6. There was no friction force considered between the pad and the wafer surface.

7. The asperities and the roughness on the pad surface were ignored. Usually the polishing pad is porous and has many asperities on the surface.

Figure 3.3 Flow Chart of the FEM

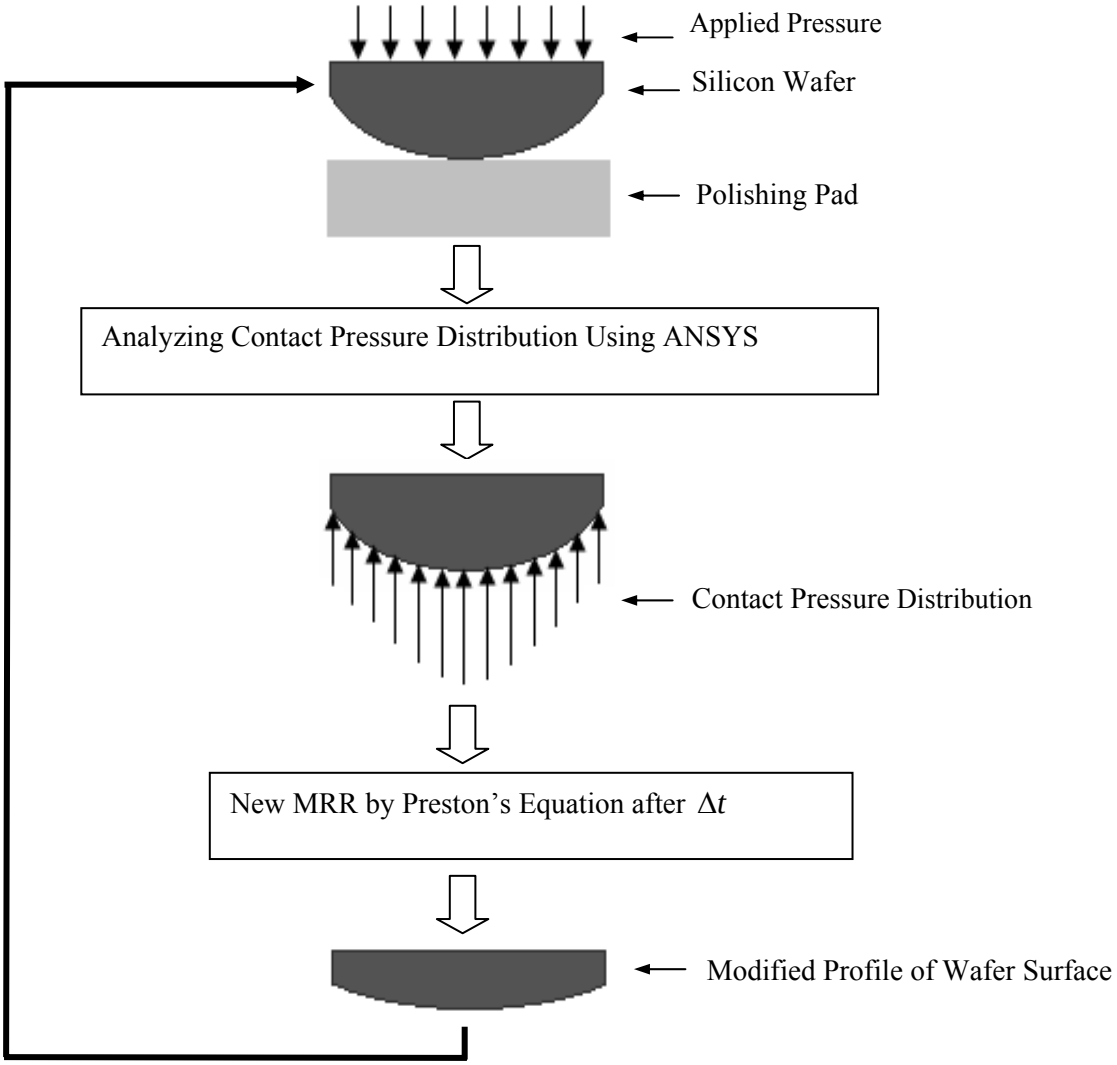
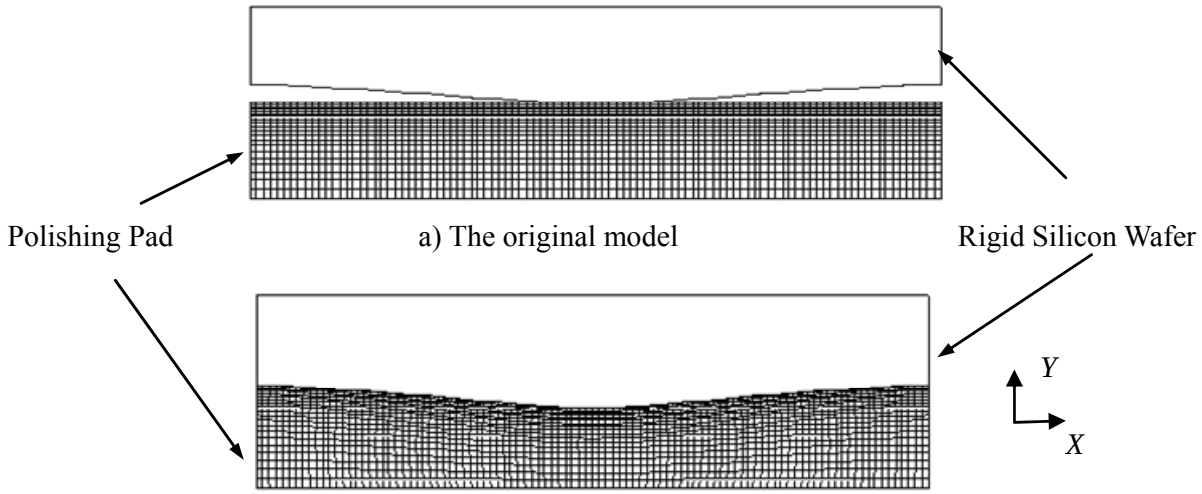


Figure 3.4 The 2D FEM Model



Boundary conditions of the FEA model include the followings:

1. DOF (degree-of-freedom) constraints: The bottom surface of the polishing pad was constrained from moving in the X and Y directions, representing the fixed support of the platen. The silicon wafer was constrained from moving in the X direction. Both left and right side of the pad were constrained in the X direction.

2. Forces: The down force was loaded on the pilot node (whose motion governs the motion of the entire wafer) of the silicon wafer in the Y direction. The down force applied is equivalent as the uniformly distributed pressure applied on the back surface of the wafer.

3. Contacts: A contact element pair was created between the wafer and the polishing pad. The pair consists of TARGE169 and CONTAL72 elements (both are standard elements in the ANSYS package).

Seven influencing factors were considered in the finite element simulation. Typical ranges for these influencing factors and their default values used in the simulation are listed in Table. 3.1. When studying the effects of one factor, only that factor was changed within a suitable range while the other factors were fixed at their default values unless specified otherwise.

3.4 Results and Discussion

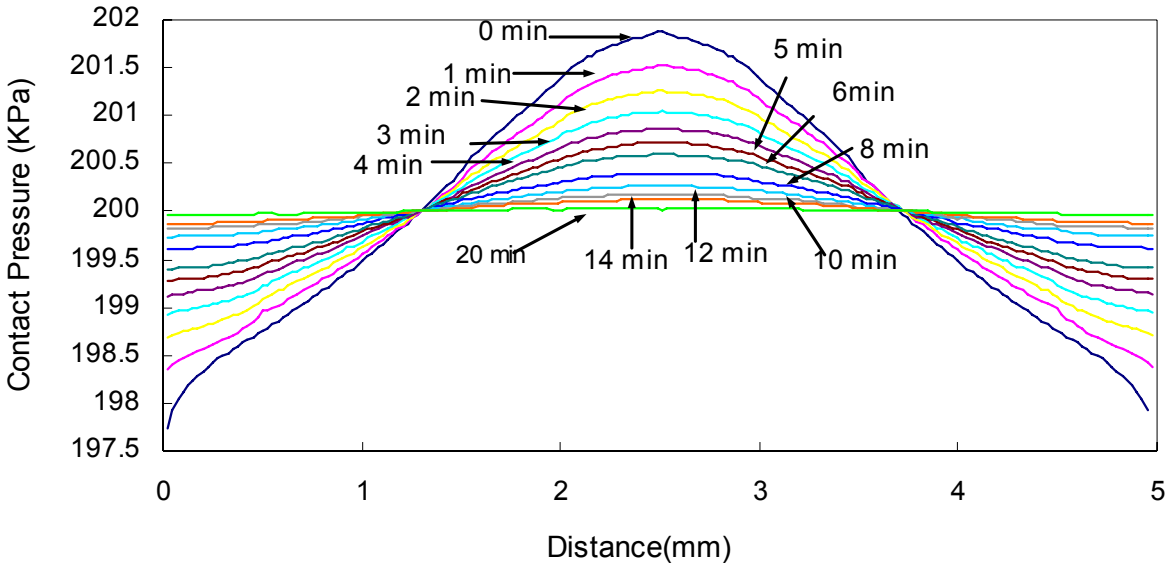
Based on Preston's equation and the FEA model, a series of the surface profiles are generated as a function of time. The pressure distribution and the corresponding pad deformation were solved iteratively by ANSYS. Then the updated pressure distribution and pad deflection were calculated. The procedure was repeated until the surface undulation was reduced to the preset value (30 nm in peak to valley value). Fig. 3.5a and 3.5b depict the evolution of the wafer surface profile and the contact pressure for a wave as a function of polishing time.

Table 3.1 Ranges and Default Values for the Seven Influencing Factors

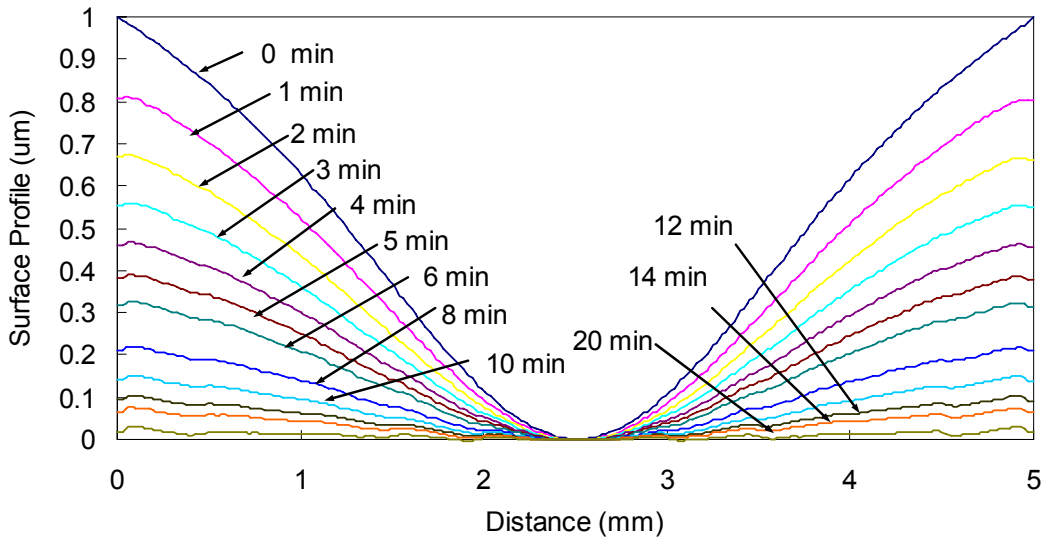
Factor	Symbol	Unit	Typical range	Default value
Young's modulus of the pad	E	MPa	1 ~ 30	12
Poisson's ratio of the pad	υ		0.1 ~ 0.4	0.2
The thickness of the pad	h	mm	0.5 ~ 1.5	1.0
The wavelength of the wafer	λ	mm	3 ~ 30	5
The wave height of the wafer	h	μm	0.2 ~ 2	1
Pressure on the wafer	P	KPa	50 ~ 300	200
The relative velocity between the pad and the wafer	V_r	m/s	0.05 ~ 3.91	0.2

For Fig. 3.5, the Young's modulus of the pad is 3 MPa. The profiles in Fig. 3.5b correspond to the contact distributions in Fig. 3.5a. Fig. 3.5a shows that the contact pressure between the pad and the wafer surface is not uniform as the pressure applied on the back surface of the wafer. It is more like a sinusoidal wave as the wafer surface profile. The peak pressure causes a faster MRR at the highest point on the wafer surface.

Figure 3.5 Pressure Distributions and Wafer Surface Profiles as Functions of Time



(a) The contact pressure distribution along the wafer surface

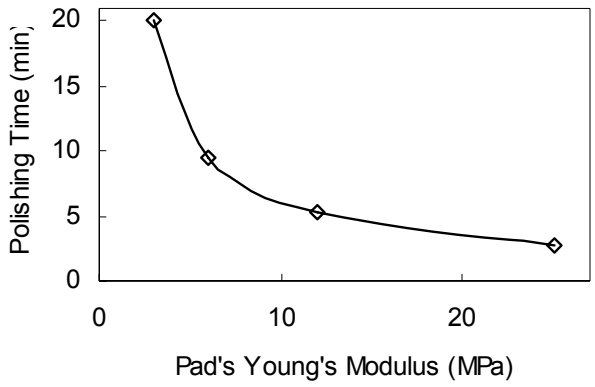


(b) Profiles of one wave on the wafer surface

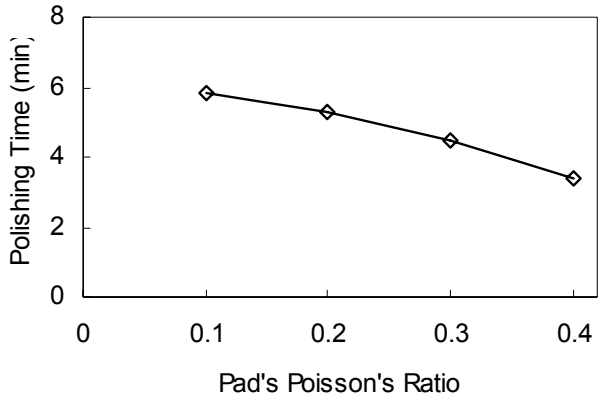
3.4.1 Effects of the Mechanical Properties of the Polishing Pad

Fig. 3.6a shows the relationship between the mechanical properties of the polishing pad and the polishing time to planarize the wafer. As Young's modulus increases, the polishing time decreases. So a pad with a larger Young's modulus is better for removing the surface undulation. However, the deformation of the pad is also dependent on Poisson's ratio. The effect of Poisson's ratio on the polishing time needed to remove the surface undulation is shown in Fig. 3.6b. The polishing time decreases as Poisson's ratio increases from 0.1 to 0.4. Fig. 3.6c shows the effects of the pad thickness on the polishing time. As the pad becomes thicker, the pressure difference on different locations is smaller. As a result, the polishing time to remove the waviness will be longer.

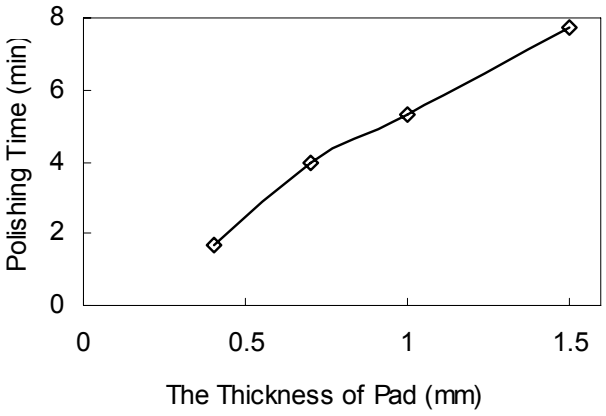
Figure 3.6 The Relationship between the Pad Properties and Polishing Time



(a)



(b)

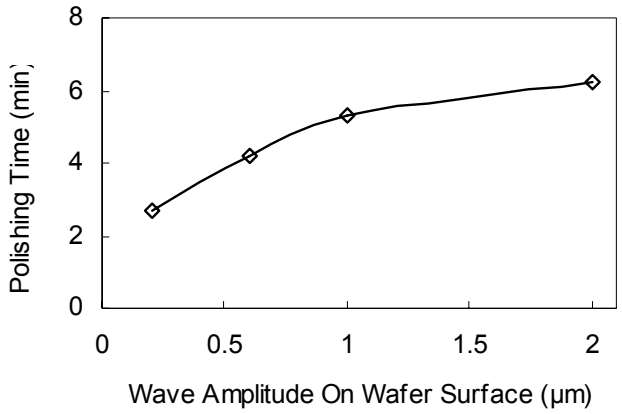


(c)

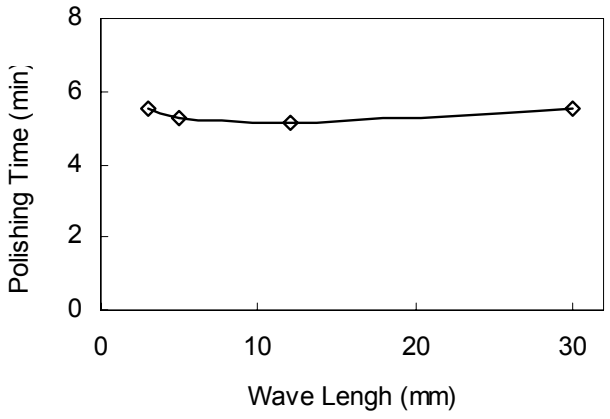
3.4.2 Effects of the Original Surface Undulation of the Wafer

As the amplitude of the wafer surface undulation increases, it takes longer time to remove the topography, as shown in Fig. 3.7a. However, in Fig. 3.7b, the polishing time does not change much when the wavelength of the wafer shape changes. The wavelength used in this model is relatively longer. The range of the wavelength is from 3 mm to 30 mm.

Figure 3.7 The Relationship between the Wafer Surface Undulation and Polishing Time



(a)



(b)

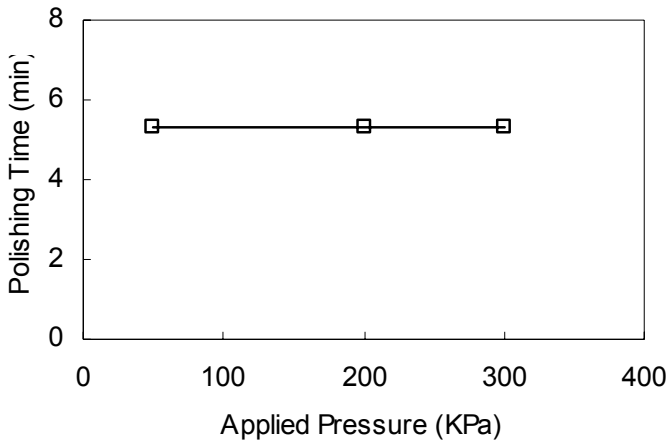
3.4.3 Effects of Applied Pressure

For the surface undulation with a wavelength of 5 mm and amplitude of 1 μm, the effects of the applied pressure on the polishing time to remove the surface undulation are shown in Fig. 3.8.

Since the pad fully contacts with the wafer surface, the contact pressure increases with the applied pressure. But the difference between the highest pressure and the lowest pressure on

the wafer surface doesn't change when the applied pressure changes. So changing pressure does not make any contribution to reduce the polishing time to remove the surface undulation.

Figure 3.8 The Relationship between the Applied Pressure and Polishing Time

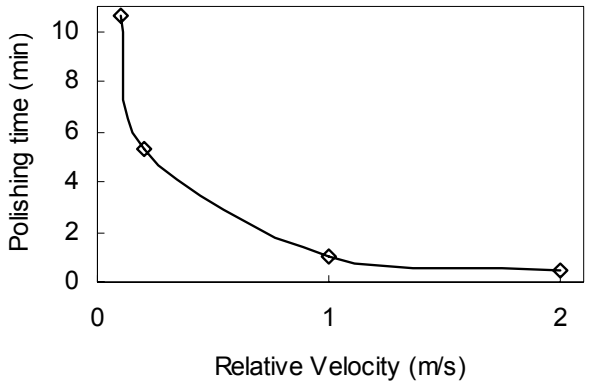


Not only the material removal is important for silicon wafer CMP, but also the final wafer surface flatness is crucial for wafer surface quality. To achieve good flatness requires removing the peak point and reducing the height difference between the highest point and the lowest point on wafer surface. According to Preston's equation, $MRR = KPV$, (V is assumed as a constant in this study), increasing the pressure results in larger material removal rate. However, the pressure distribution on wafer surface is unchanged by increasing polishing pressure. Thus, wafer flatness or the polishing time to achieve the flatness is not necessarily changed.

3.4.4 Effects of Relative Velocity

According to Preston's equation, the material removal rate is proportional to the relative velocity between the pad and the wafer rotation. Since the contact pressure is higher at the peak point and lower at the valley point, increasing the relative velocity helps to remove the peak faster, hence, to achieve a flat surface in a shorter cycle time. This is shown in Fig. 3.9

Figure 3.9 The Relationship between Relative Velocity and Polishing Time



3.5. Summary

Based on Preston's equation, a finite element model has been developed to simulate the effects of seven influencing factors on the polishing time to planarize a wafer surface. Major conclusions are:

1. The higher the pad's Young's modulus is, the faster the surface undulation of silicon wafers can be removed. Increasing the pad's Poisson's ratio can shorten the polishing time too. Increasing the thickness of the pad results in longer polishing time.

2. The polishing time needed to remove the surface undulation on the wafer surface depends on the original shape of the surface. The surface undulation with large amplitude needs longer polishing time to remove. The wavelength within the studied range doesn't affect the polishing time needed as much as the amplitude does.

3. Although the material removal rate is proportional to the pressure, for a certain shape of the wafer surface, changing applied pressure doesn't make much difference on the polishing time for removing the surface undulation.

4. As the relative velocity between the pad and the wafer becomes larger, the polishing time needed to remove the surface undulation becomes shorter.

CHAPTER 4 - Finite Element Analysis of Silicon CMP: Stress Distributions and Edge Effects

4.1 Introduction

To maximize the number of devices per wafer, semiconductor manufacturers use as much area of each wafer as possible. The trend for silicon wafers is that its size is increasing and more and more devices are built on one wafer. Good wafer planarity, both local and global, is essential for the dimensional accuracy required at subsequent lithography stages of the device manufacturing. Improving the non-uniformity within wafer, especially on the wafer edge, is important to reduce the yield loss. The edge effect in CMP, where sharp variation in removal rate is observed near the edge of the wafer, is a main concern when considering global planarity of wafers [Fu et al., 2001].

It has been widely observed in CMP that the material removal rate (MRR) near the edge of the wafer differs significantly from that in the central region of the wafer. According to Preston's equation, the normal stress or the pressure at the wafer-pad interface significantly influences the MRR. Thus, within wafer non-uniformity (WIWNU) in MRR may be the manifestation of pressure/stress variation across the wafer surface. However, even though a uniformly distributed pressure is applied during polishing, the experimentally observed removal rate changes from the center to the edge. This NU (Non uniformity) is not described by Preston's equation [Preston, 1927]. There are many articles on the edge effect considering the normal pressure and stress distribution, as reviewed in chapter 2. However, few of them have considered effects of the properties of both polishing pad and carrier film.

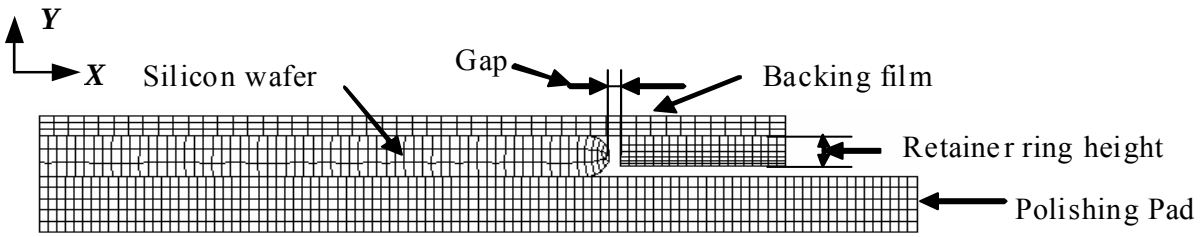
This chapter studies the effects of both carrier film and pad properties on the stress distribution on wafer surface. The influence of the retainer ring geometry is also studied. There are four sections in this chapter. Following this introduction section, section 4.2 provides procedures to develop the finite element model. The developed model is used in section 4.3 to predict the relations between the influencing factors (including Young's modulus and Poisson's ratio of polishing pad and carrier film, dimensions of the retainer ring, and the applied pressure). Section 4.4 gives the conclusions.

4.2 Development of the Finite Element Model

4.2.1 The 2D FEA Model

Commercial software, ANSYS (ANSYS Inc., Canonsburg, PA), was used for this study. Fig. 4.1 schematically displays the two-dimensional (2D) model developed. Some dimensions in the figure are exaggerated for illustration purposes.

Figure 4.1 The 2D FEA Model of CMP



The finite element model was based on the same assumptions and simplifications as stated in section 3.3. In addition, the carrier film was elastically deformed. Friction between the carrier film and wafer back surface was not considered. The retainer ring was isotropic and had stable mechanical properties.

4.2.2 The Boundary Conditions for the 2D FEA Model

The boundary conditions used for the FEA model include the followings:

1. DOF (degree-of-freedom) constraints: The bottom surface of the polishing pad was constrained from moving in both X and Y directions, representing the fixed support of the table. The carrier film, silicon wafer and the pad were constrained from moving in the X direction. Both left side and right side of the carrier film were constrained in the X direction. The entire back side of the carrier film had the same displacement in Y direction. The retainer ring was glued to the carrier film.

2. Pressure: The pressure was uniformly applied on the backside of the carrier film.

3. Contacts: Contact element pairs were created between the wafer and the polishing pad and between the carrier film and the back surface of the wafer. If the retainer ring contacted the polishing pad, another contact pair between the retainer ring and the polishing pad was created. The pair consisted of TARGE169 and CONTAL72 elements (both are standard elements in the ANSYS package).

The retainer ring was used to touch the pad and change the deformation of the pad near the wafer edge. Consequently, the stress on the wafer surface was redistributed. The properties of the pad and the carrier film were expected to affect the stress or the pressure distribution on the wafer surface and wafer edge.

4.3 Simulation Results and Discussion

4.3.1 The Stress Distributions on the Wafer Surface

Figure 4.2 Stress Distributions on the Wafer Surface

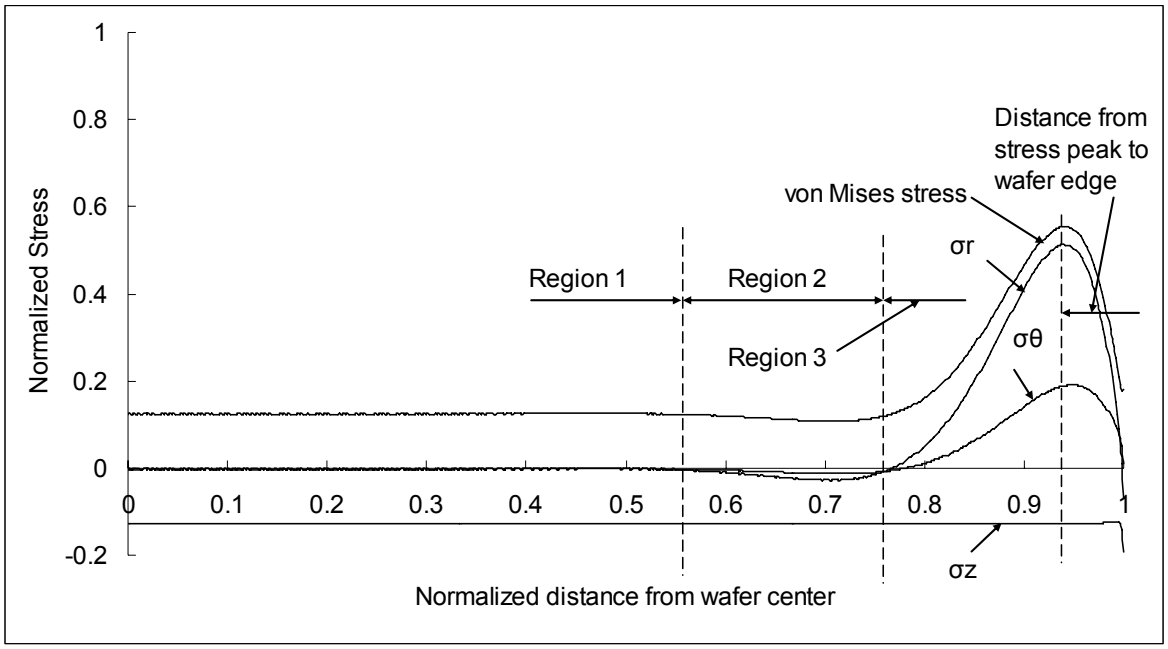
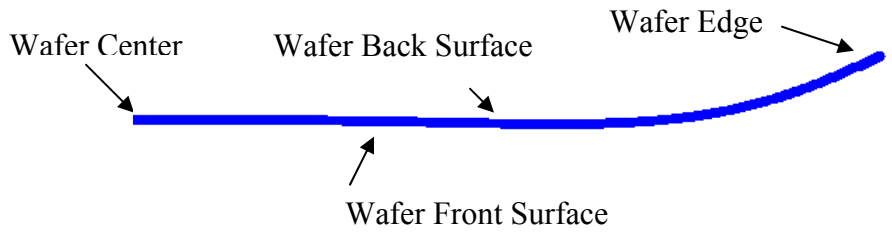


Fig. 4.2 shows calculated stress distributions on the wafer surface including von-Mises stress, radial stress (σr), angular stress (σθ), and the stress in the vertical direction (σz). The stress distributions are uniform in the first region. Consequently, uniform material removal rate and good flatness are achieved in this region. In the second region, the stress is lower than the applied pressure, and also is lower than the stress in the first region, and material removal rate is lower. The edge effect occurs in the third region where the stress is much higher than the other regions. The variation of the peak stress can be used to predict the edge effect. The properties of pad and carrier film are the main influencing factors on the stress distributions of the wafer surface. The corresponding wafer deformation is shown in Fig. 4.3. The wafer is bended up at the edge causing the stress abruption at the wafer edge. The more the wafer is bended, the higher stress the wafer has at the wafer edge, the resulting in the edge effect. Different pad and carrier film properties cause different wafer deformation and the stress distributions at the edge. The closer the stress peak to the wafer edge, the smaller the non-uniform region on the wafer. Reducing the stress peak amplitude and the distance to the wafer edge will improve wafer surface quality.

Figure 4.3 The Wafer Deformation under Pressure between the Carrier Film and Pad



4.3.2 Effects of Influencing Factors on Stress Distribution

Fig. 4.4 shows von-Mises stress distribution on the wafer surface as Young's modulus of the pad changes. Fig. 4.5a shows the relationship between Young's modulus and the stress peak amplitude. When Young's modulus of the pad is larger, the amplitude of the stress peak is smaller and also the curve levels down. The stress peak is closer to the edge with the increasing

of pad Young's modulus (Fig. 4.5b). So a more rigid polishing pad results in less edge effect on the wafer surface. (All the stress values and distances are normalized to the maximum values in this thesis)

Figure 4.4 Pad Young's Modulus vs. Von-Mises Stress

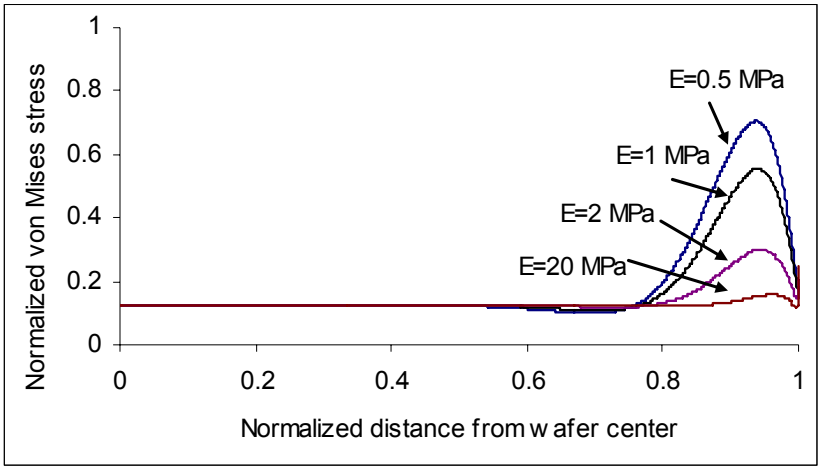
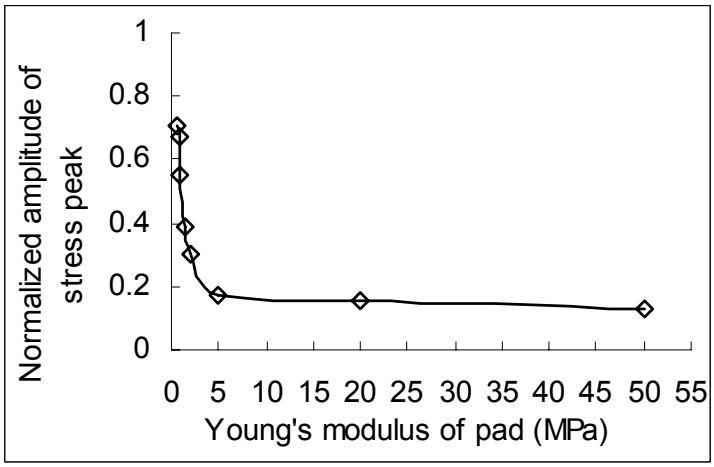
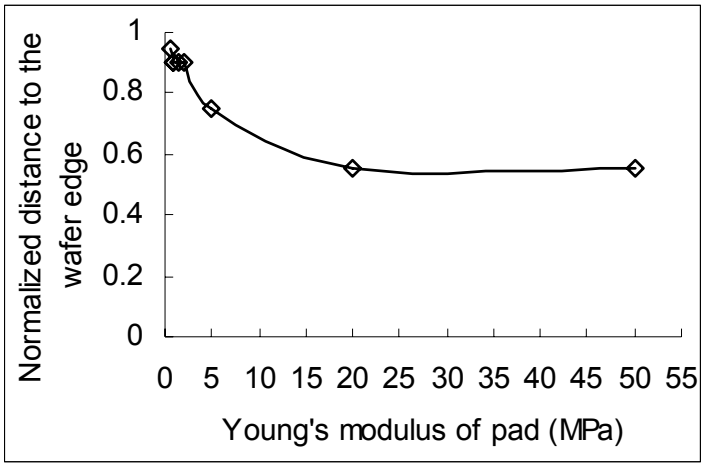


Figure 4.5 Effects of Pad Young's Modulus on (a) the Peak Stress, and (b) the Distance to the Wafer Edge



(a)



(b)

Poisson's ratio affects the pad and carrier film elastic deformation of which directly influence the stress distribution on the wafer surface. Generally, lower Poisson's ratio corresponds to the high porosity of the pad [Xin, 1998]. Fig. 4.6 shows the stress distributions on the wafer surface with different pad Poisson's ratio. When Poisson's ratio of pad increases, the amplitude of the peak stress decreases (Fig. 4.7a), and the distance from the stress peak to the wafer edge is decreased too (Fig. 4.7b). A pad with bigger Poisson's ratio results in smaller stress. This means that a pad with lower porosity is better for improving the edge effect. But lower porosity is not good for the slurry transportation.

Figure 4.6 Pad Poisson's Ratio vs. Von-Mises Stress

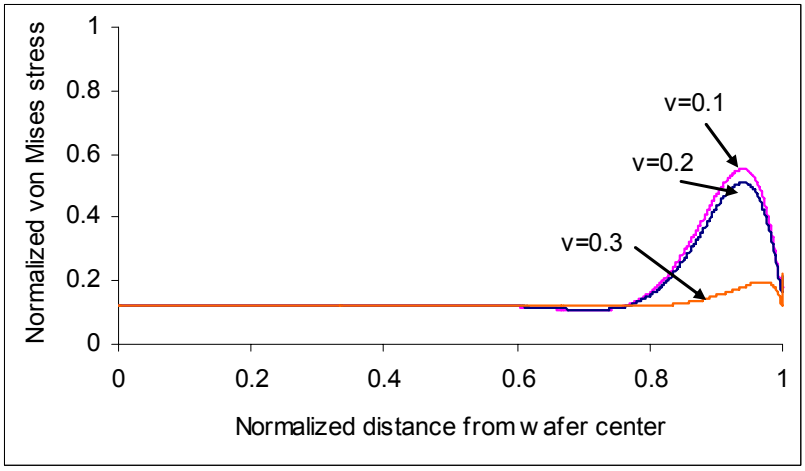
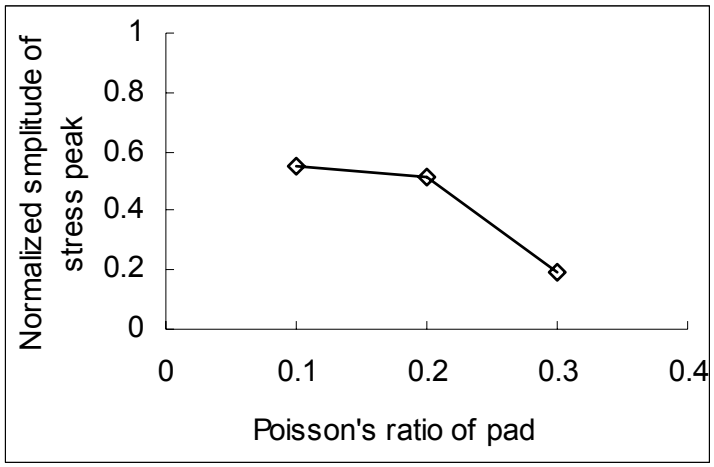
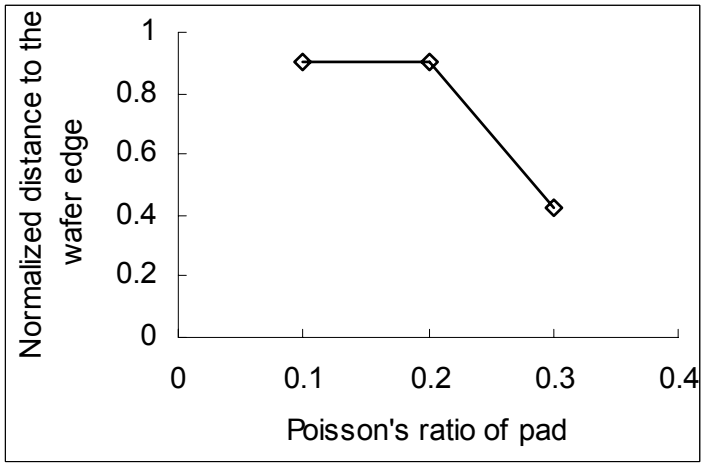


Figure 4.7 The Relationship between Pad Poisson's Ratio and the Stress Peak, and the Distance to the Wafer Edge



(a)



(b)

Fig. 4.8 shows the stress distributions with different pad thickness. The amplitude of the peak stress on the wafer edge increases with the increasing of the pad thickness (Fig. 4.9a). However, the distance from the stress peak to the wafer edge does not change much when the pad thickness changes (Fig. 4.9b). A thinner pad is better to reduce the irregularity at the wafer edge.

Note that whichever parameter of the pad properties is changed, the width of region 3 doesn't change much (Fig. 4.4, Fig. 4.6, and Fig. 4.8). The length over which the wafer has varied stress distributed doesn't change.

Figure 4.8 Pad Thickness vs. Von-Mises Stress

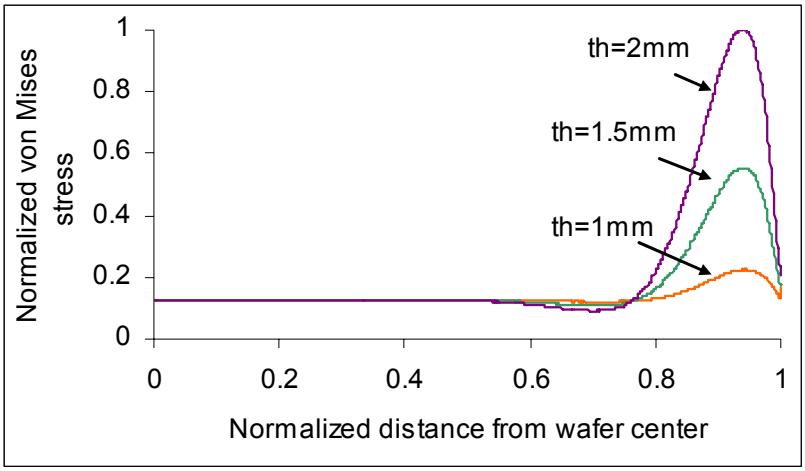
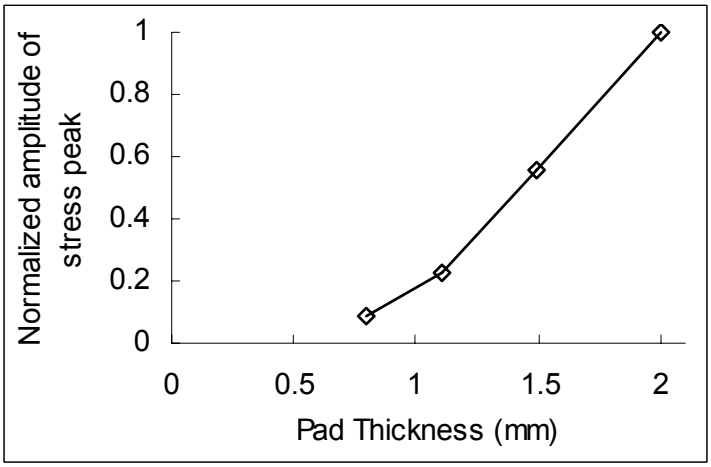
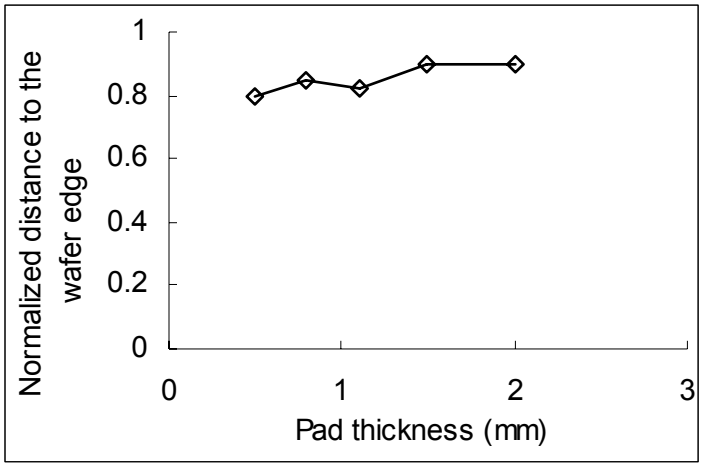


Figure 4.9 The Relationship between Pad Thickness and the Peak Stress, and the Distance to the Wafer Edge



(a)



(b)

Carrier films with different Young's modulus result in different stress distribution on the wafer surface (Fig. 4.10). When Young's modulus of the carrier film is increased, the stress decreases (Fig. 4.11a), the distance from the stress peak to the wafer edge is decreased, and the width of region 3 is decreased. This means that the range of the non-uniform area is narrowed by increasing Young's modulus of the carrier film. Therefore, a more rigid carrier film is better to improve the edge effect.

Figure 4.10 Carrier Film Young's Modulus vs. Von-Mises Stress

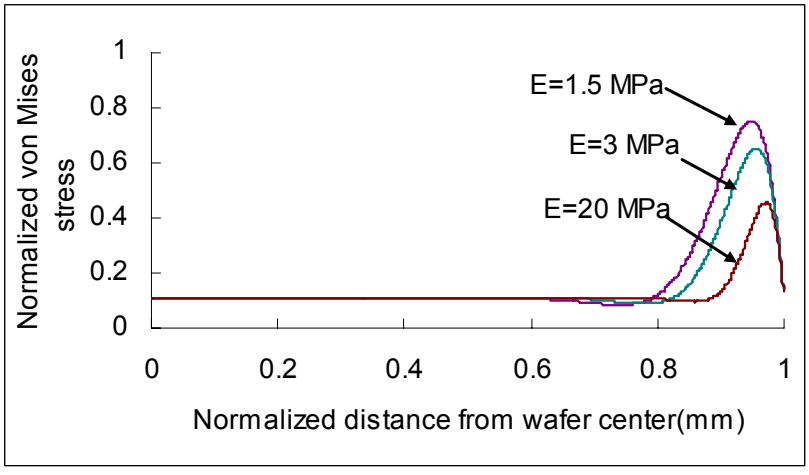
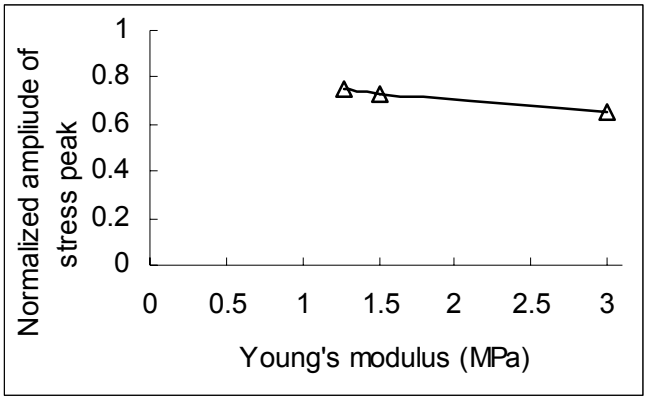
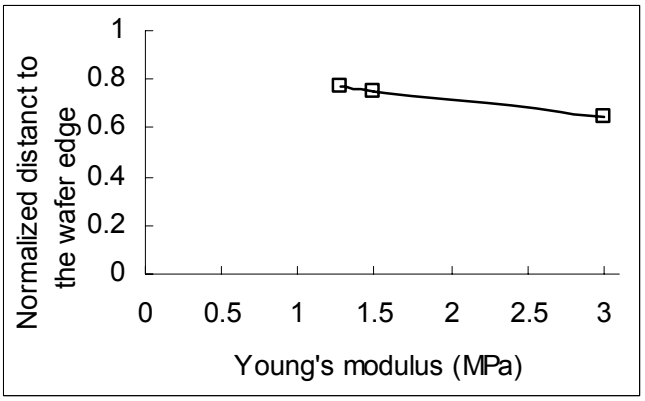


Figure 4.11 The Relationship between Carrier Film Young's Modulus and the Peak Stress, and the Distance to the Wafer Edge



(a)



(b)

Fig. 4.12 shows the stress distribution on the wafer surface with different Poisson's ratio of carrier film. As Poisson's ratio of the carrier film increases, the amplitude of the peak stress increases too (Fig. 4.13a). But the distance from the stress peak to the wafer edge remains unchanged (Fig. 4.13b). A carrier film with smaller Poisson's ratio (higher porosity) is better to reduce the edge effect.

Fig. 4.14 shows the stress distributions with different thickness of carrier film. The thicker the carrier film is, the smaller the amplitude of the peak stress on the wafer surface is (Fig. 4.15a). So the edge effect decreases when the thickness of the carrier film increases. However, changes in the thickness of the carrier film do not affect the distance from the stress peak

position to the wafer edge (Fig. 4.15b). To improve the uniformity at wafer edge, a thicker carrier film is better.

Figure 4.12 Carrier Film Poisson's Ratio vs. Von-Mises Stress

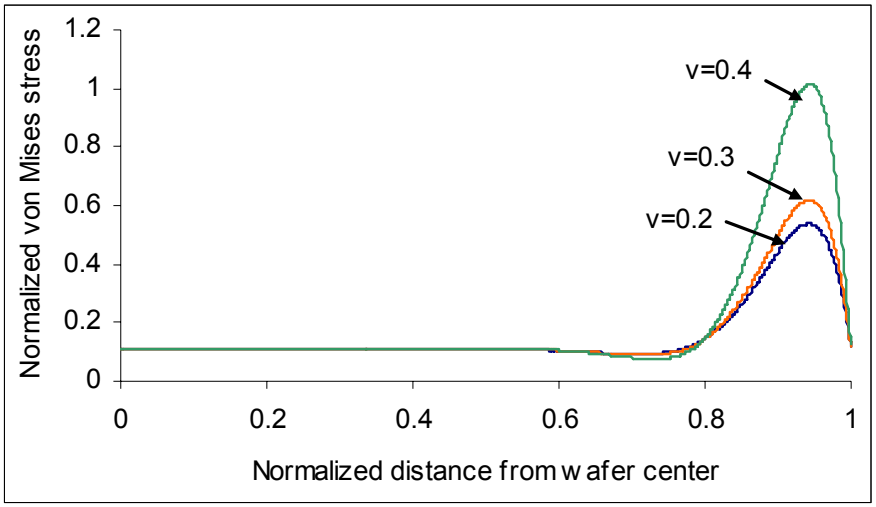
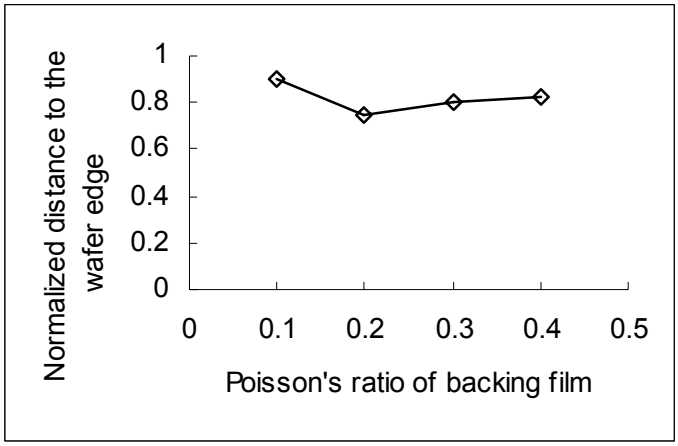


Figure 4.13 Effects of Carrier Film Poisson's Ratio on (a) Distance to the Wafer Edge and (b) Peak Stress on the Wafer Surface

(a)



(b)

Figure 4.14 Carrier Film Thickness vs. Von-Mises Stress

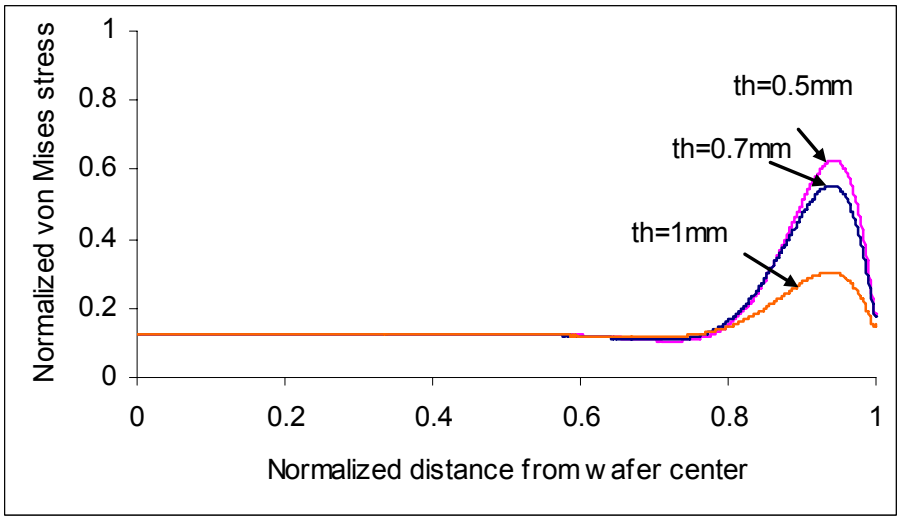
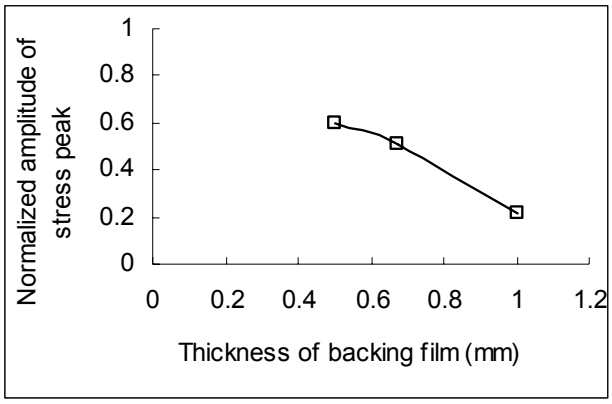
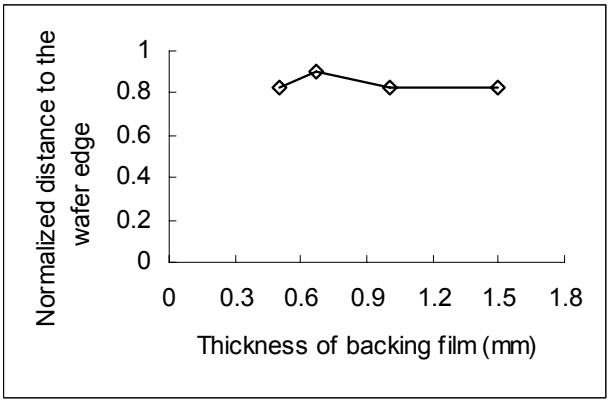


Figure 4.15 Effect of Carrier Film Thickness on (a) Stress Peak, and (b) the Distance to the Wafer Edge



(a)



(b)

4.3.3 Geometry of Retainer Ring

Besides controlling the wafer in place during polishing, another function of the retainer ring is to compress the rebound area in the pad. The gap is the distance from the wafer edge to the inner periphery of the retainer ring (Fig. 4.2). When the wafer gets closer to the retainer ring, the rebounding of the pad is pressed down more. Fig. 4.16 shows the stress distributions on the wafer surface with different gap size. When there is no gap between the wafer and the retainer ring, the stress peak is moved away from the wafer surface. The length of the region 1 (uniform removal area) become longer. As the gap size increases, the amplitude of the stress peak is increased (Fig. 4.16a). But the distance from the stress peak to the wafer edge does not change

(Fig. 4.16b). The gap size has significant effects on the stress distribution on the wafer surface. A smaller gap size is better to get better uniformity on the wafer surface.

Figure 4.16 Gap Size vs. Von-Mises Stress

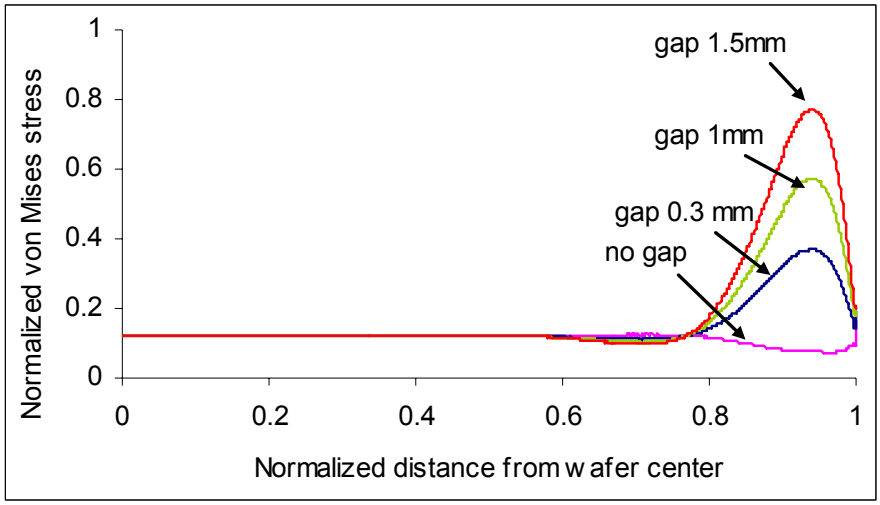
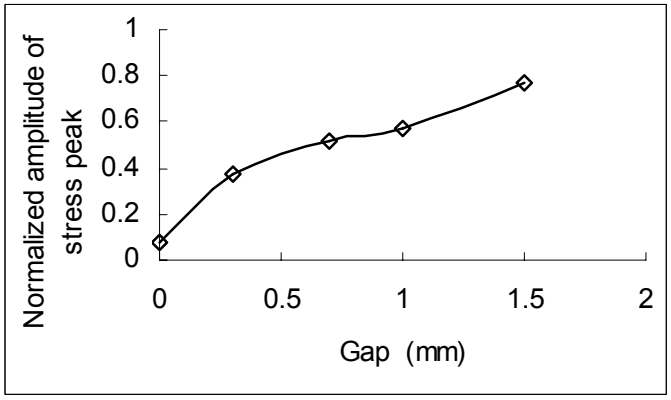
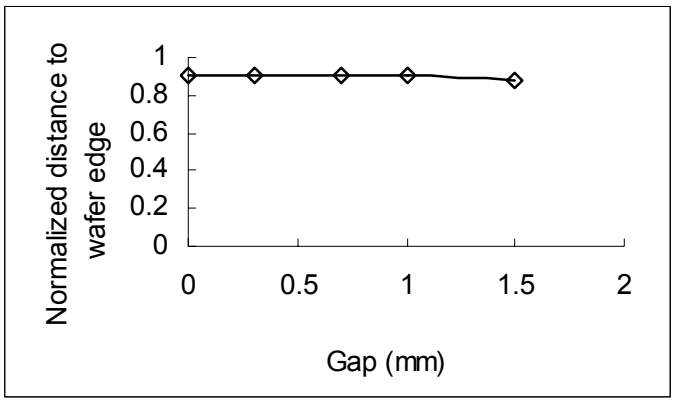


Figure 4.17 Effects of Gap Size on (a) the Stress Peak, and (b) the Distance to the Wafer Edge

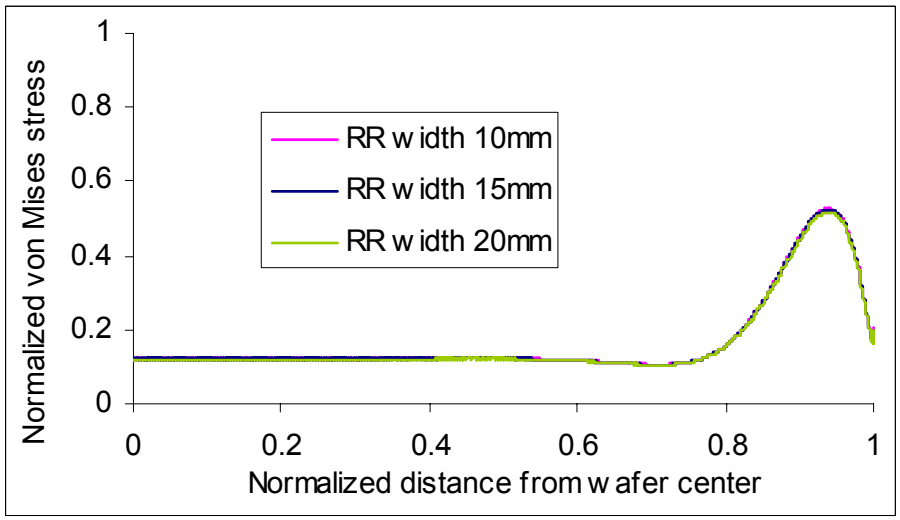


(a)



(b)

Figure 4.18 Retainer Ring Width vs. Von-Mises Stress



The width of retainer ring does not have much effect on the stress distribution on the wafer surface (Fig. 4.18) and on the distance from the stress peak to the wafer edge.

4.4 Summary

A finite element model has been developed for chemical mechanical polishing of silicon wafers. It has been used to simulate the effects of the influencing factors on the stress distributions at wafer surface which directly affect the material removal uniformity and the edge

effect. Besides the pad properties, the carrier film properties and the retainer ring geometry are studied. Major conclusions from the study are:

1. For the polishing pad, increasing Young's modulus or Poisson's ratio can reduce the stress peak at the wafer edge so hence improve the uniformity of material removal. Moreover, the thinner the pad is, the smaller the amplitude of the peak stress at the wafer edge, reducing the edge effect.

2. The more rigid carrier film results in better uniformity at the wafer edge. A carrier film with a low Poisson's ratio is better for reducing the edge effect. Meanwhile, thicker carrier films are better for edge uniformity.

3. As the width of the retainer ring changes, the distance from the stress peak to the wafer edge does not change much. So changing the width of the retainer ring does not affect edge geometry appreciably.

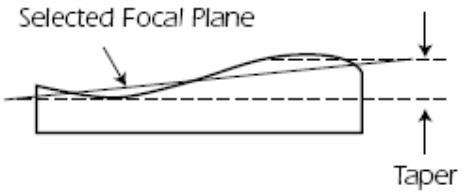
4. As the gap between the wafer and inner periphery of the retainer ring becomes smaller, the amplitude of the peak stress is decreased. Hence, the smaller gap is better to improve the uniformity at the wafer edge.

CHAPTER 5 - Finite Element Analysis of Silicon CMP: Tapering

5. 1 Introductions

Taper is the lack of parallelism between the back surface of the wafer and the selected focal plane (best fit plane) of the front surface [Online staff, 2001] (Fig 5.1). It is the non-uniformity of wafer global planarization where the surface material is removed more at one end than at the other end.

Figure 5.1 Definition of Taper [Online staff, 2001]



There are two major reasons causing the taper:

1. Off-center

On a CMP machine, the wafer is mounted on the block by liquid green wax, or by vacuum. The block with wafer is held on the hub. Sometimes, the wafer center is not aligned with the block center (Fig. 5.2). Or, the block center is not aligned with the hub rotation axis. When such misalignment occurs, the contact pressure is not distributed evenly on the wafer surface, causing the uneven material removal (taper).

2. Wafer flat

Even though the wafer, block and the hub are aligned very well, wafers with a flat (Fig. 5.3) will have an uneven pressure distribution and hence an uneven material removal between the two ends.

Figure 5.2 The Offset of Wafer Center from Block Center

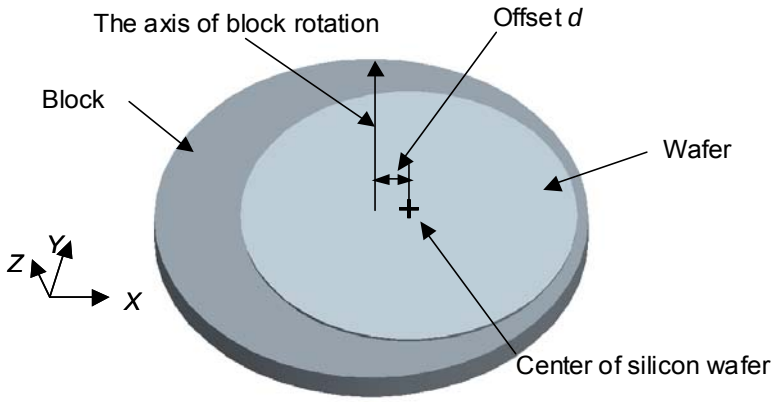
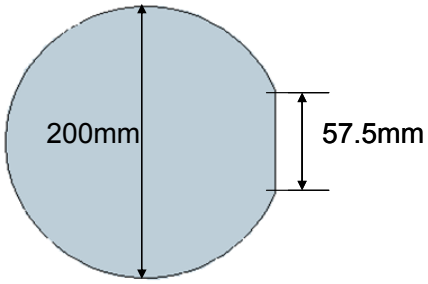


Figure 5.3 Illustration of a Wafer with a Flat



In practice, in order to reduce wafer taper, the wafer has to be positioned on the block center or with a predetermined eccentricity accurately, which is difficult and time consuming. This chapter uses the finite element analysis to find the effects of the misalignment and the wafer flat on the wafer taper. Three FEA models are created:

1. The pad-wafer-block model to study the effects of wafer-block misalignment.
2. The pad-wafer-block- hub ring (It is to transfer the down pressure to the block and to wafer) model to study the effects of both wafer-block misalignment and block-hub ring misalignment.
3. The pad-wafer-block model to study the effects of wafer-block misalignment while the wafer in this model has a flat.

5.2 Flow Chart of FEA Analysis

As Preston's equation predicts, the removal rate depends linearly on the downward pressure P and the relative velocity V between the pad and the wafer. If the product of K, V and polishing time t is maintained the same, then the material removal depends only on the polishing pressure. Suppose there is an offset between the wafer center and the block center, then the contact pressure distribution will not be uniform (Fig. 5.4). Then the taper is calculated as in equations (5.1)-(5.4), where P_1 is the contact pressure at one end, P_2 is the contact pressure at the other end.

$$MRR_0 = KVP_0 \tag{5.1}$$

$$MR\,(material\ removel) = MRR_0 \times t = KVP_0 t = (KVt)P_0 \tag{5.2}$$

$$KV = \frac{MRR_0}{P_0} \tag{5.3}$$

$$Taper = KVt(P_1 - P_2) \tag{5.4}$$

The purpose by using FEA is to get the contact pressure distribution that determined the material removal on wafer surface and to calculator the taper from it. The flow chart shown in Fig. 5.5 is used for all of the three modeling analyses.

Figure 5.4 Illustration of Pressure Distribution with an Offset

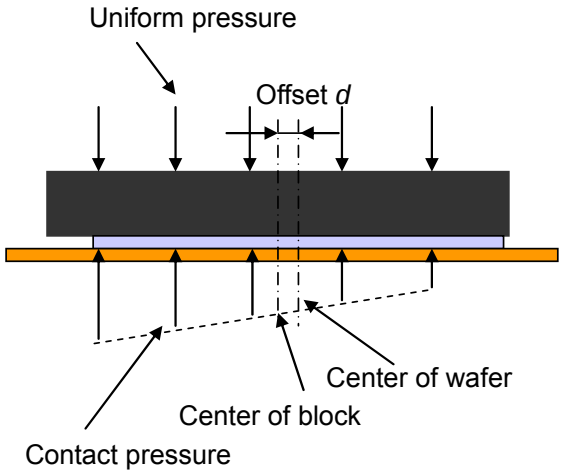
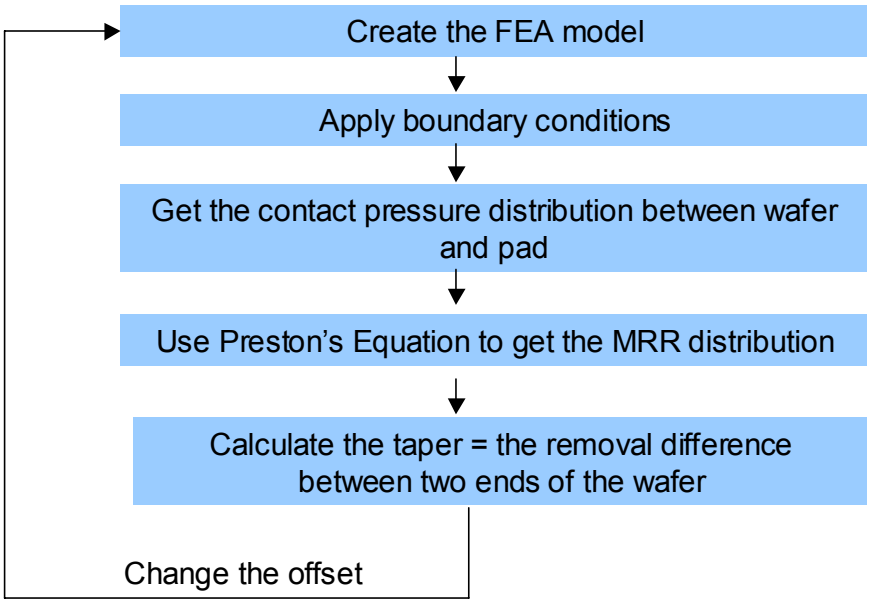


Figure 5.5 The Flow Chart for the FEA Modeling Analyses



5.3 The 3D FEA Model with Pad-Wafer-Block

5.3.1 Assumptions and Boundary Conditions

As shown in Fig. 5.6, the silicon wafer is mounted on the block and pressed against the polishing pad. Because of symmetry, only half of the structure is modeled and analyzed for all the three models. The size and the material properties are shown in Table 5.1.

Table 5.1 The Properties of the Three Parts

	Young's Modulus	Poisson's Ratio	Diameter	Thickness
Silicon wafer	147 GPa	0.3	200 mm	736 um
Polishing pad	3 MPa	0.1	260 mm*	0.75 mm
Carrier block	410.5 GPa	0.19	229 mm	20 mm

*Note: See assumption (b) below.

Several assumptions are made in addition to those for the FEA modeling in chapter 4:

a) The pressure applied on the backside of the block is uniformly distributed.

b) To save the number of elements, the polishing pad is simulated as a small round plate with the diameter of 260 mm.

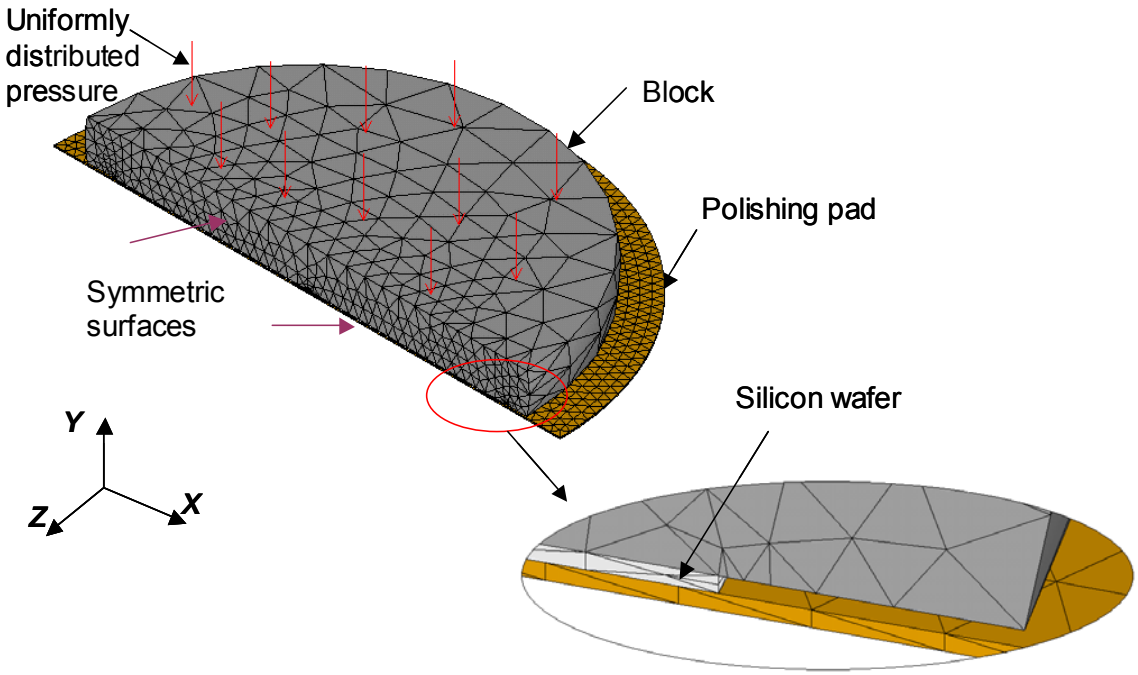
c) The block and the wafer are glued together to simulate the function of the wax layer.

d) For the polishing process, the carrier that holds the block and the wafer is rotating around its own axis.

The boundary conditions used for the FEA model include the followings:

1. DOF (degree-of-freedom) constraints: The bottom surface of the polishing pad was constrained from moving in both X and Y directions, representing the fixed support of the table.
2. Friction: there is no friction between wafer surface and polishing pad contributed to the material removal (except the model that studies the effects of friction).
3. Pressure: The pressure was uniformly applied on the backside of the block.
4. Contacts: A contact element pair was created between the wafer and the polishing pad.
5. The symmetric surfaces (of the wafer, pad, and block) were used as the symmetric boundaries.

Figure 5.6 The 3D Block-wafer-pad Model



5.3.2 Simulation Results

The contact pressure between wafer and polishing pad is shown in Fig. 5.7. If the wafer is not centered on the block, the contact pressure between pad and wafer is not uniformly distributed. As the offset of the wafer center away from the block center increases, the contact pressure distribution becomes more "tilted". The wafer end closer to the block edge experiences smaller contact pressure than the other end does. According to the contact pressure, the taper value is calculated for each offset value. The results are shown in Fig. 5.8. As the offset d increases, the taper is increased. The relationship between the offset and the taper value is approximately linear, as shown in Fig. 5.8. (Contact pressure is normalized to a certain value in this chapter.)

Figure 5.7 The Contact Pressure Distribution between Wafer and Polishing Pad

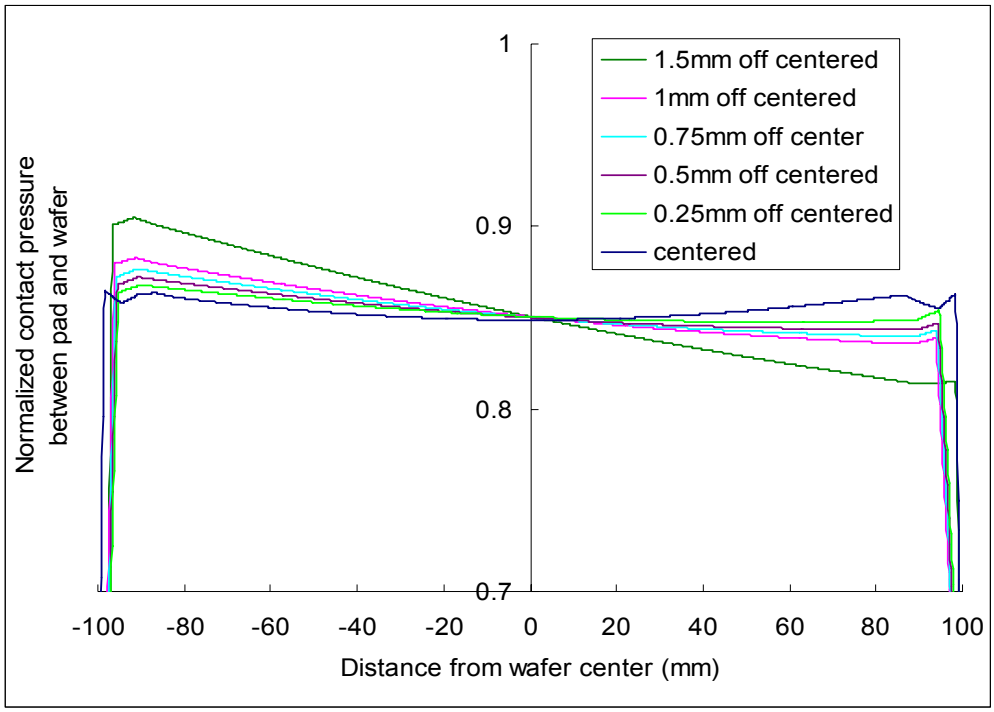
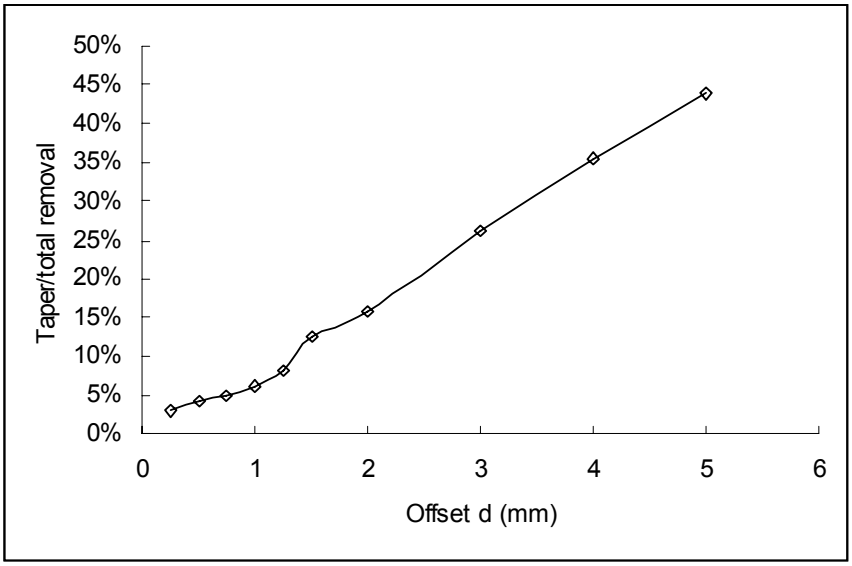


Figure 5.8 Taper vs. Wafer Offset



5.4 The 3D FEA Model with Pad-Wafer-Block and Hub Ring

5.4.1 The 3D FEA Model

Another misalignment causing the taper on wafer surface is the offset of hub ring from the block center when the block with wafer is held by vacuum onto the carrier. The pressure is applied by the hub and transferred to the ring. Then the block and the wafer experience the polishing pressure through the ring. However, if the ring is not aligned with the block center, the contact pressure between the ring and the block will not be uniformly distributed. This will affect the contact pressure between the wafer and polishing pad and, therefore, the taper. Fig. 5.9 shows the misalignment of the wafer, block, and the hub ring. *d1* is the offset of the wafer center from the block center, and *d2* is the offset of the hub ring center from the block center. In general, there will be an angle between *d1* and *d2* (Fig. 5.10). In this study, for simplification, the angles are assumed to be 0° and 180°. The purpose is to understand the effects of both offsets on the wafer taper. Fig. 5.11 is the 3D FEA model. The hub that applies the down force is modeled as a rigid body. Contact pairs are created for the hub/hub ring contact, hub ring/block contact and silicon wafer/polishing pad contact.

Figure 5.9 Illustration of the Front Side and Back Side of the Block

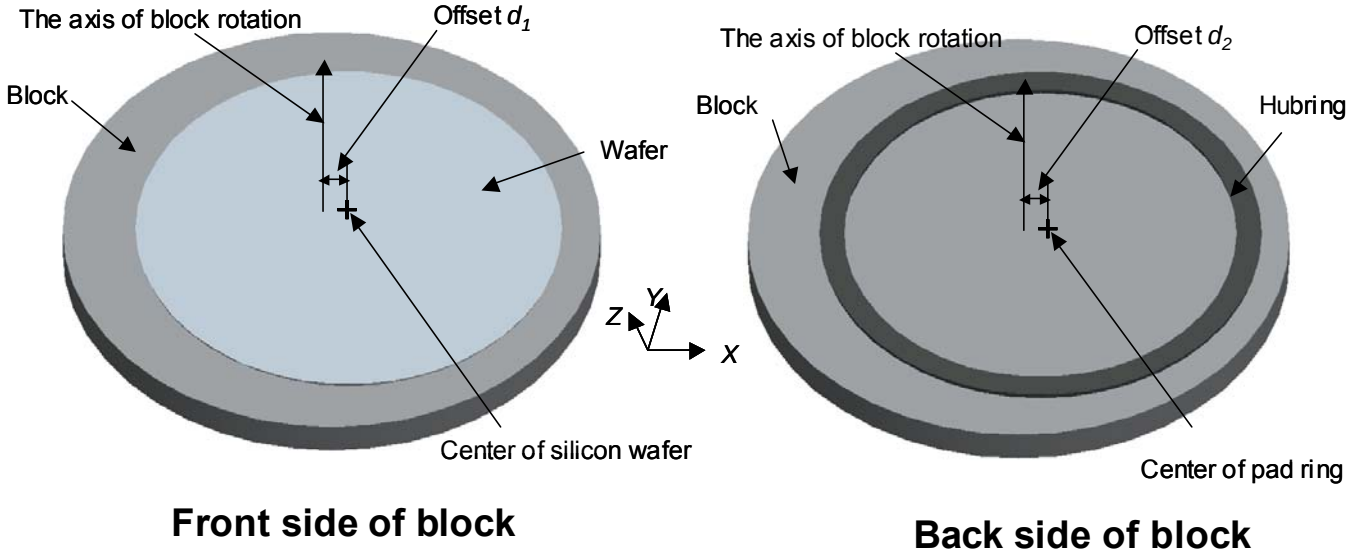
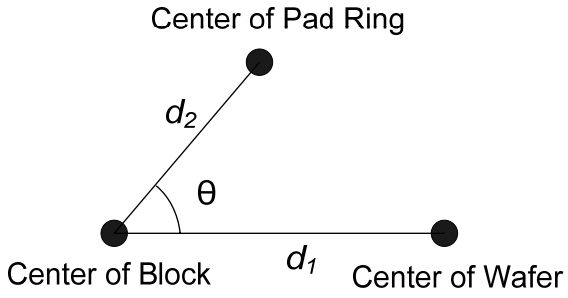


Figure 5.10 Relative Position of the Wafer Offset and the Hub Ring Offset



Four cases will be studied (Fig. 5.12):

Case I: the offset of hub ring center from block center is 0.

Case II: the offset of wafer center from block center is 0.

Case III: the angle between the two offsets is 0°.

Case IV: the angle between the two offsets is 180°.

Figure 5.11 The 3D FEA Model with the Hub Ring and Hub

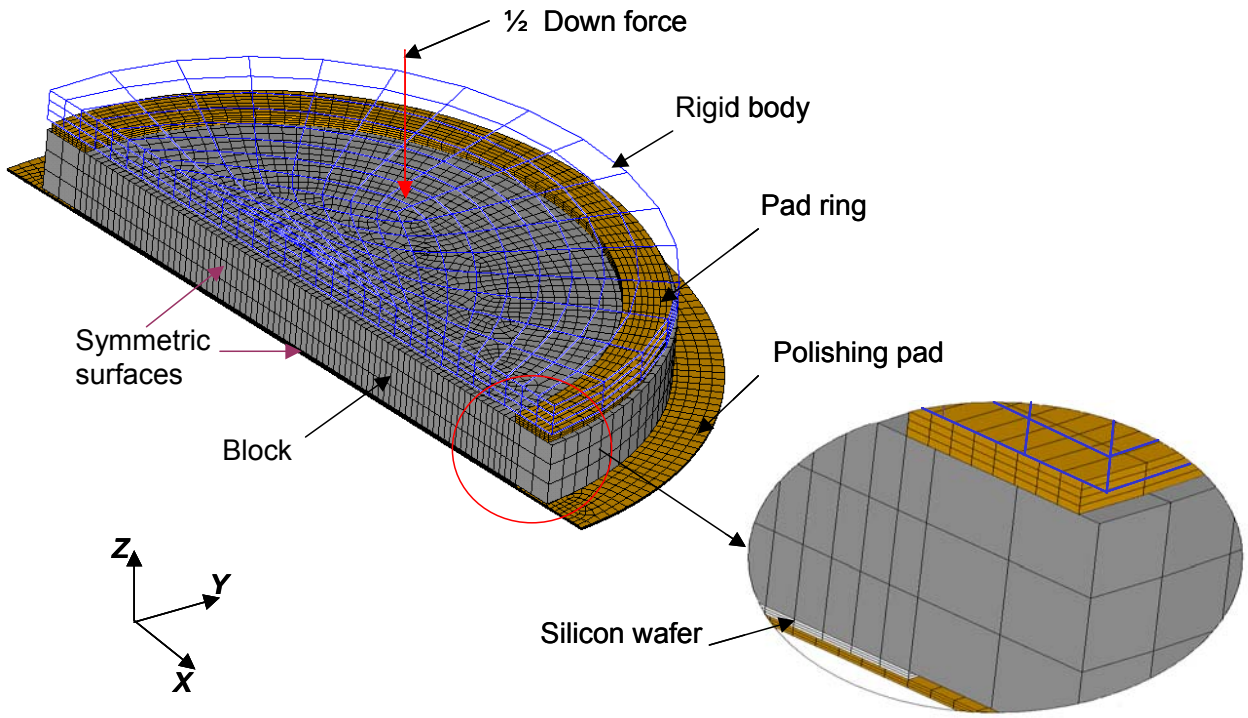
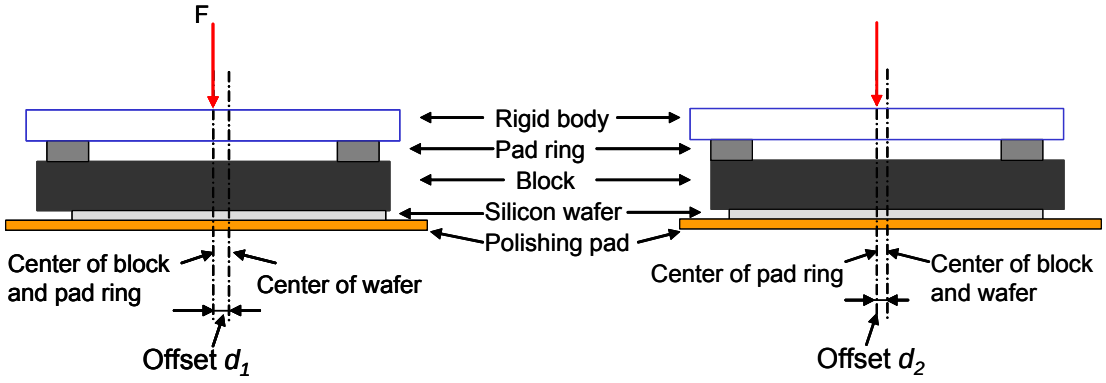
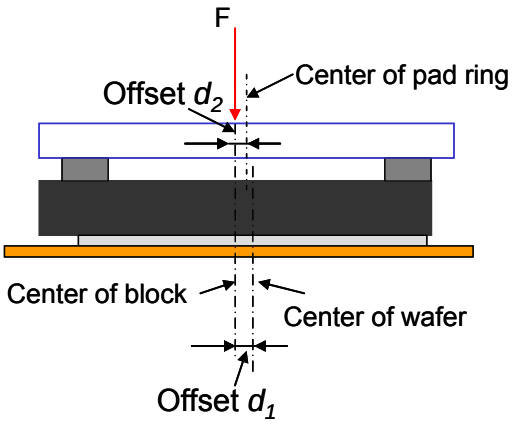


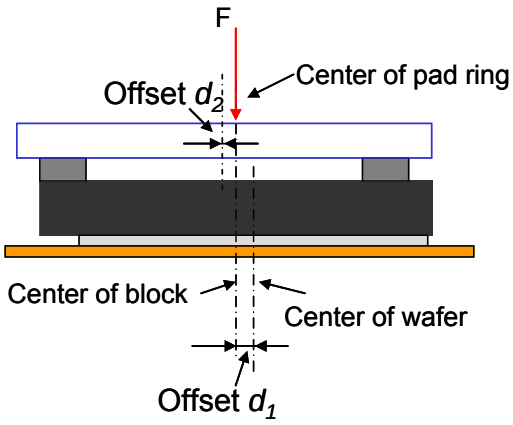
Figure 5.12 The Illustration of the Four Cases



Case I Case II



Case III



Case IV

5.4.2 Simulation Results

Case I:

When the wafer center is offset from the block center, the contact pressure distribution is "tilted" (Fig. 5.13). As the offset increases, the contact pressure distribution becomes more tilted. Therefore, the taper is increased when the offset is increased (Fig. 5.14).

Figure 5.13 Contact Pressure Distribution between Wafer and Polishing Pad with Wafer Offset

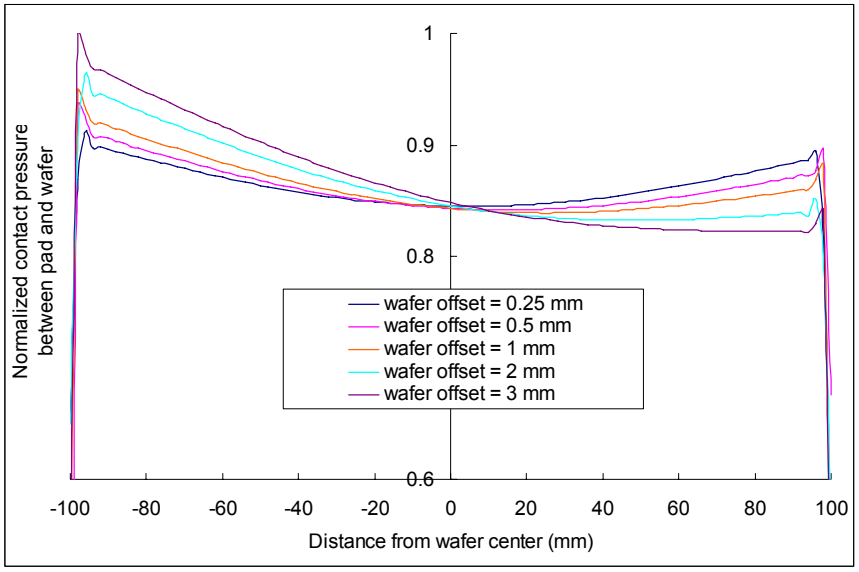
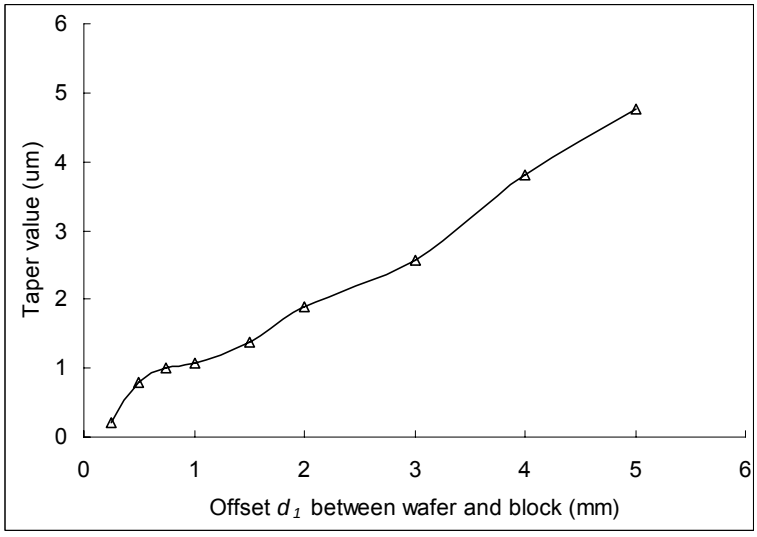


Figure 5.14 Taper vs. Offset of Wafer



Case II:

If there is only an offset of the hub ring from the block center, the wafer center will be at the block center. Similarly, the contact pressure distribution is tilted (Fig. 5.15).

Figure 5.15 Contact Pressure Distribution between Wafer and Polishing Pad with Hub Ring Offset

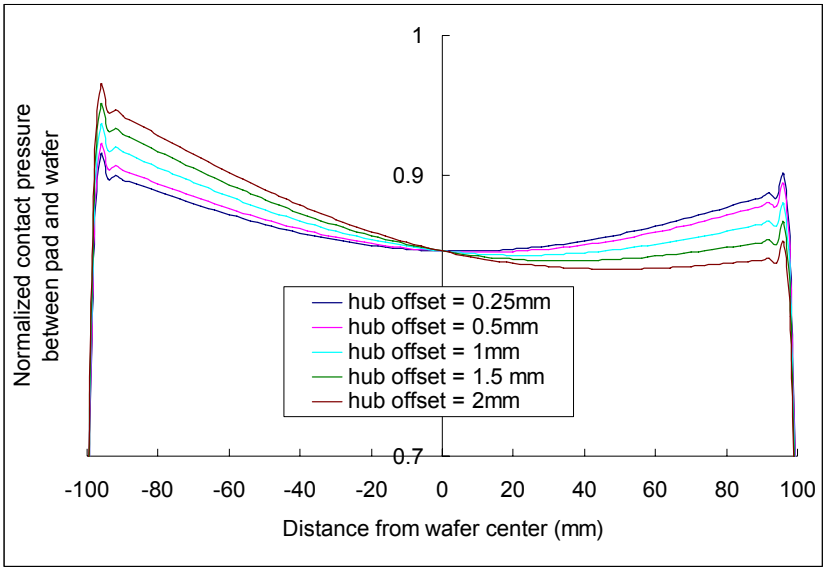


Figure 5.16 Taper vs. Offset of Pad Ring

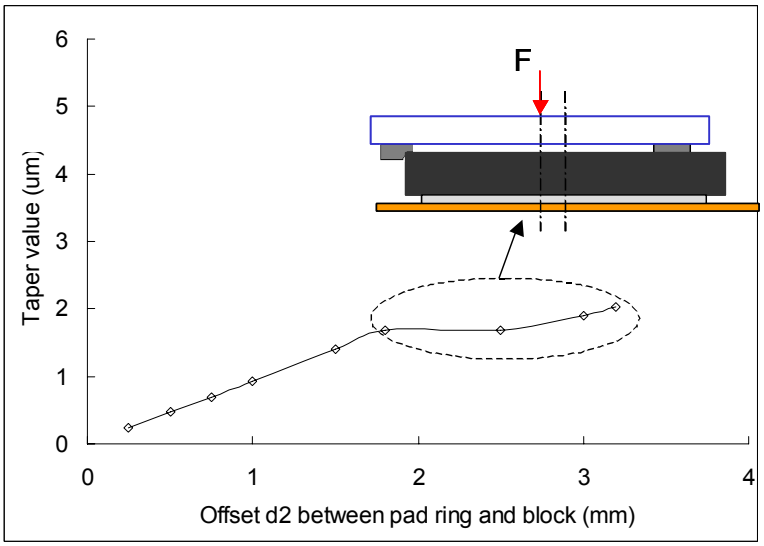


Fig. 5.16 shows the relationship between the taper value and the offset of pad ring. There are two stages:

Stage 1: when the offset *d2* is small, the hub ring is still on the block, the taper is increased linearly as the offset *d2* increases.

Stage 2: as the offset *d2* increases, part of the hub ring does not contact the block. The taper value is slightly increased when the offset *d2* increases. The slope is much lower than that in the first stage.

Case III:

Both wafer and hub ring are offset from the block center and the angle between the two offsets is 0. In this case, the taper is affected not only by the wafer offset but also by the hub ring offset away from the block center. The contact pressure (between wafer and polishing pad) distribution curve on the wafer surface does not change much and does not have any obvious inclination (Fig. 5.17) when the wafer and hub ring are offset the same distance and in the same direction. Therefore, there is almost no taper on the wafer surface (Fig. 5.18).

Figure 5.17 Contact Pressure Distribution between Wafer and Polishing Pad When Two Offsets are the same

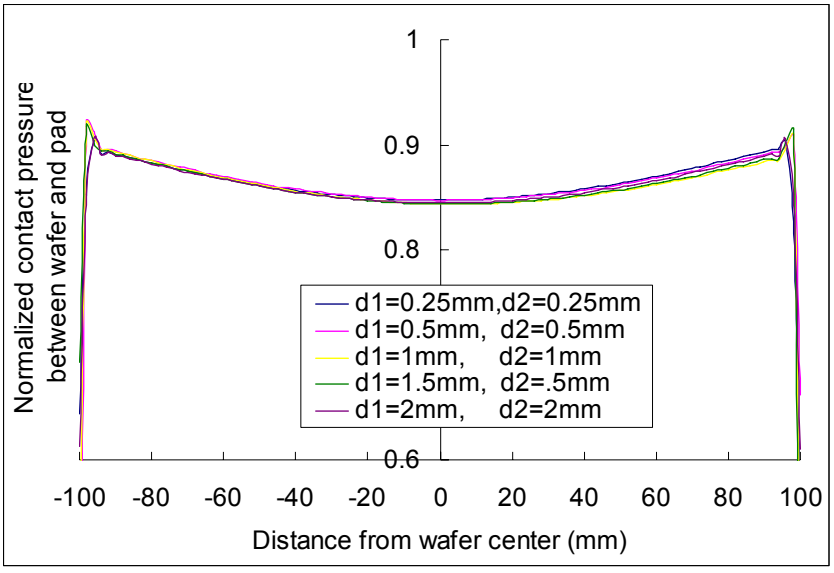
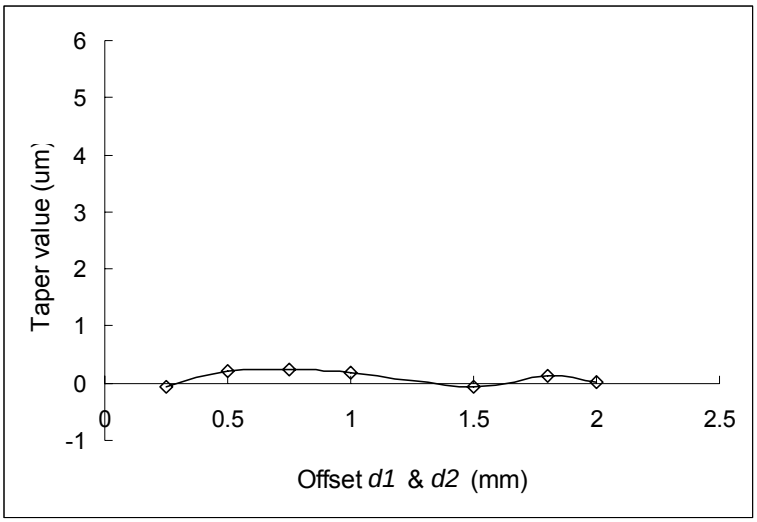


Figure 5.18 Taper vs. Same Offsets



Case IV:

Both wafer and hub ring are offset from the block center and the angle between the two offsets is 180°. As shown in Fig. 5.19, the contact pressure distribution on the wafer surface is more tilted than those when any single one offset exists. Therefore, the taper increases much faster than the other three cases (Fig. 5.20).

Figure 5.19 Contact Pressure Distribution between Wafer and Polishing Pad when Two Offsets are Different

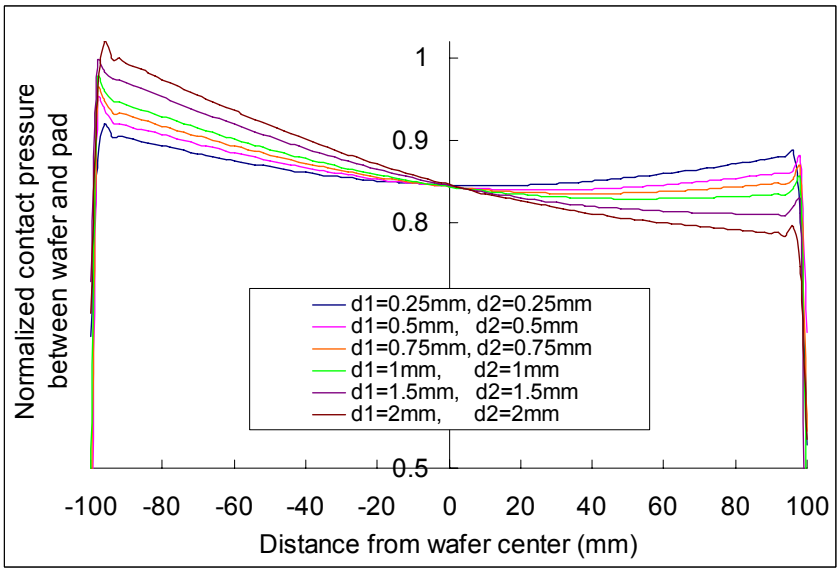
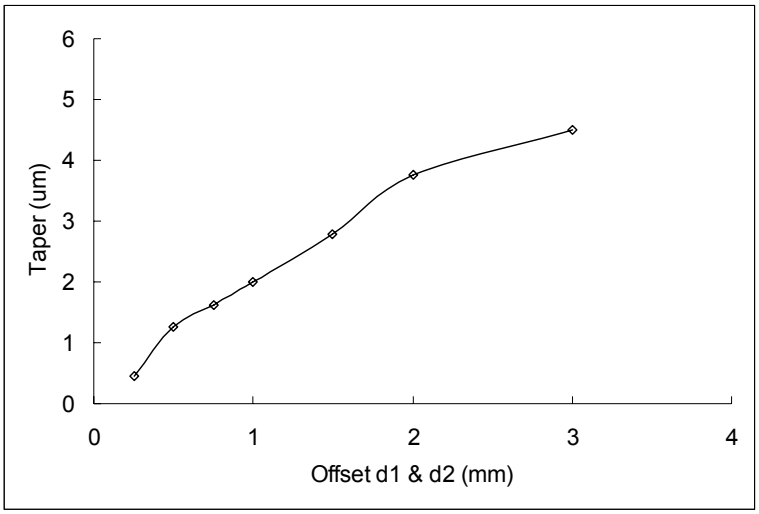


Figure 5.20 Taper vs. Different Offsets



5.4.3 Discussion

To compare the simulation results for the four cases, several notations are made here:

Case I – *d1*: with only wafer offset, resulting in taper1

Case II – *d2*: with only hub ring offset, resulting in taper2

Case III – *d1* & *d2* in the same directions, resulting in taper3

Case IV – *d1* & *d2* in the opposite directions resulting in taper4

Except case III, any offset increases the taper value. The more the wafer or the hub ring is offset, the more taper on the wafer surface. The worst case is when the hub ring offset and wafer offset are in the opposite directions. However, if both offsets happen to be in the same direction, the taper value is the smallest (Fig. 5.21). taper3 is the simulation result when the offset *d1* and *d2* are in the same direction. Fig. 5.22 shows that taper3 is approximately equal to the difference of taper1 and taper2. As shown in Fig. 5. 23, the taper is larger when either hub ring or wafer is offset from the block center. When both offsets exist and are in the same direction, one of the tapers caused by corresponding offset is cancelled by the other.

Figure 5.21 Comparison of Tapers of the Four Cases

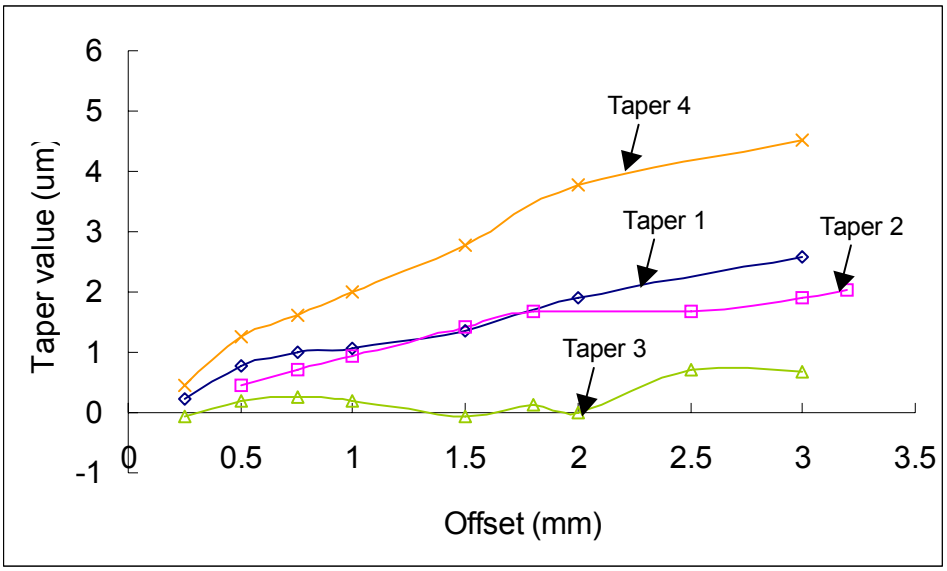


Figure 5.22 Comparison of taper 3 and taper1-taper2

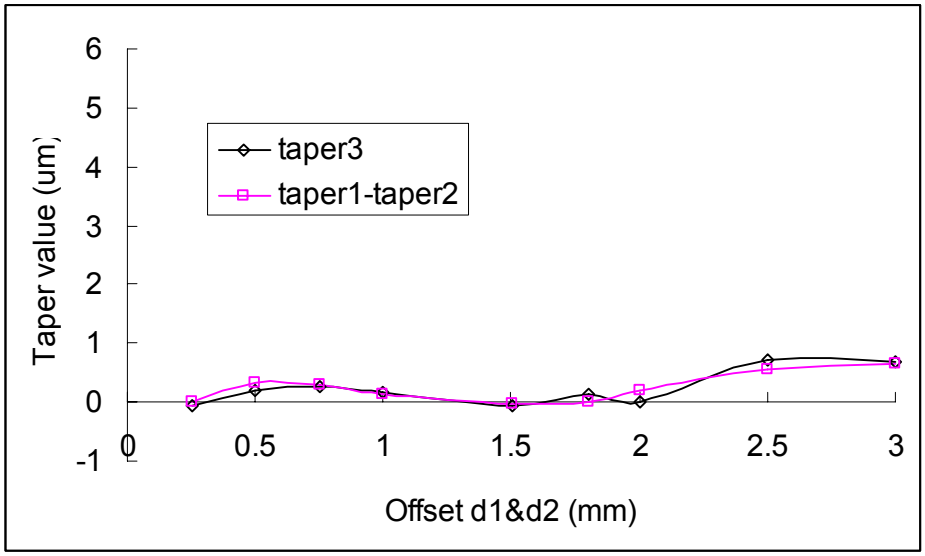
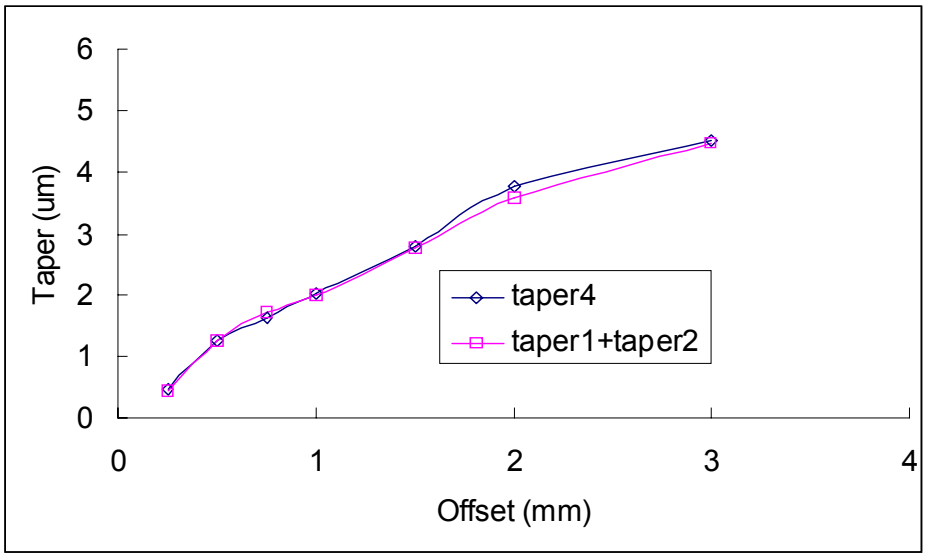


Figure 5.23 Comparison of taper 3 and taper1+taper2



taper4 is the simulation result when the offsets *d1* and *d2* are in the opposite directions. Fig. 5.23 shows that taper4 is the sum of taper1 and taper2. As shown in Fig. 5.23, the taper is smaller when either only hub ring or only wafer is offset from the wafer center. While both offsets exist and are in the opposite directions, one of the tapers caused by corresponding offset is enhanced by the other.

5.5 The 3D FEA Model When the Wafer Has a Flat

If the wafer has a flat, even though the wafer is centered on the block center, the contact pressure distribution on the wafer surface will not be uniform. This will cause the taper. A predetermined offset of wafer from block center is necessary to reduce the taper. The contact pressure distributions on wafer surface with different offsets are shown in Fig. 5.24. Fig. 5.25 shows the taper value increases approximately linear. Initially, if the wafer is centered on the block, the taper exists in the other direction. As the offset increases (less than 0.5 mm), the taper is decreased to 0 first, and then the taper value is increased.

Figure 5.24 Contact Pressure Distribution between Wafer (with a Flat) and Polishing Pad

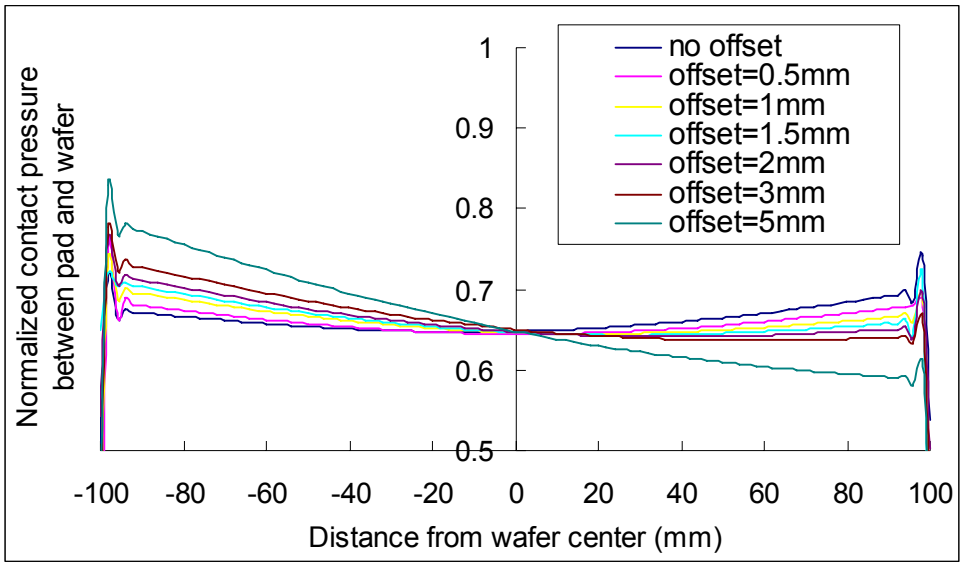
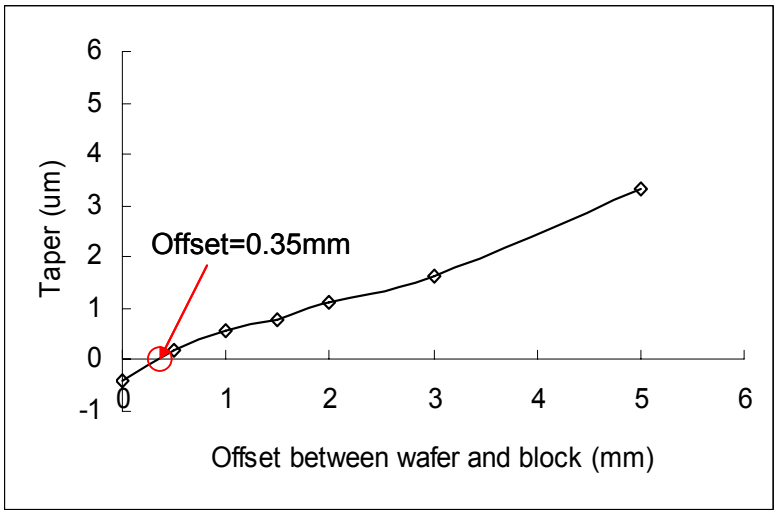


Figure 5.25 Taper vs. Offset (for Wafer with a Flat)



5.6 Summary

During the process of CMP, there almost always is a misalignment between the wafer and the carrier (block) when the wafer is loaded in the polishing head. The offset of the wafer from the block directly affects the taper value (flatness). The larger the offset is, the larger the taper value is.

The misalignment between the carrier (block) and the pad ring (hub ring) that is to transfer the polishing pressure is also a significant factor affecting taper on wafer surface. The larger the offset between the block and the pad ring is, the larger the taper value is.

Most of the time, both wafer and hub ring are offset from the block. The results show that:

1. If both offsets are in the same direction, the taper value is lower than that with any one offset and close to the difference of the two taper values.
2. If both offsets are in the opposite directions, the taper value is larger than that with any one offset and close to the sum of the two taper values.

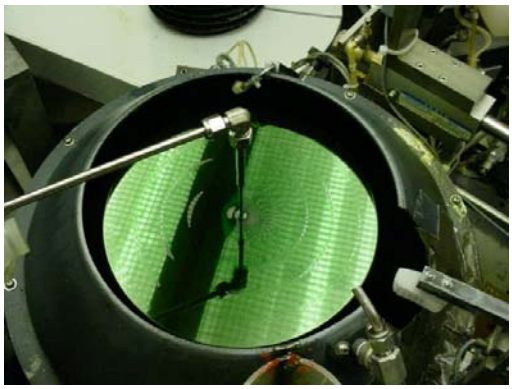
If the wafer has a flat, a predetermined offset of the wafer center from the block center can reduce the taper caused by the un-symmetry of the wafer.

CHAPTER 6 - An Experimental Investigation on Material Removal Rate in CMP of Silicon Wafers

6.1 Introduction

In wax mounting polishing, the wafer is wax mounted against a flat reference block. The wax used is called "green wax" (Fig 6.1). It does not require chlorinated hydrocarbon solvents and therefore is benign to the environment. When the wafer is mounted on the block surface the air is filtered to ensure that no particles can come between the ceramic block surface and the wafer backside. Fig 6.2 is a schematic diagram of the wax mounting polishing process. The carrier head (hub) and the pad rotate in the same direction. Meanwhile the arm of the carrier head oscillates around its own axis. The pad experiences the pressure exerted on the wafer, and carries the slurry between the wafer surface and pad (Steigerwald et al., 1997). The material removal in wax mounting polishing occurs as a consequence of a combination of chemical reaction of the slurry chemicals with the silicon wafer surface and the repeated mechanical interaction between the pad and the silicon wafer with the abrasive particles in between.

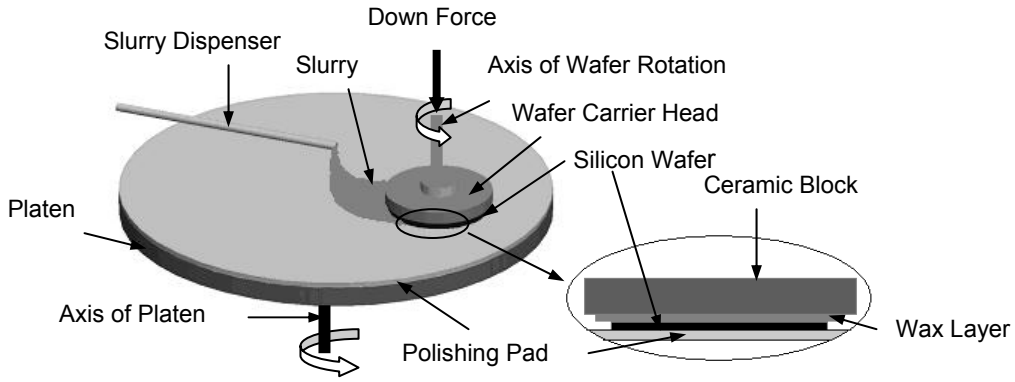
Figure 6.1 Wax Spinning on the Block [MEMC Electronics Materials, 2001]



In this chapter, the effects of process variables on the material removal rate in polishing of silicon wafers are studied experimentally. A series of experiments of 200 mm silicon wafers were conducted on a wax-mounting polisher. The variables considered include the applied pressure, the wafer rotation speed, the pad rotation speed, the table temperature, and the slurry

flow rate (including the ratio between potassium hydroxide, KOH, and the abrasive polishing slurry, Syton®) [Szafraniak, 2003]. The purpose was to understand the relationship between these variables and the MRR in polishing of silicon wafers.

Figure 6.2 Schematic Diagram of Wax Mounting Polishing Process



There are five sections in this chapter. Following this introduction section, the experimental conditions are explained. In section 6.3, the results of the experiments and the relationships between the variables (including applied pressure, the wafer speed, the pad speed, the table temperature, and the slurry flow rate) and the MRR are presented. Section 6.4 presents the designed experiment about the significant factors. Section 6.5 comprises the conclusions.

6.2 Experimental Conditions

The polishing machine was the wax-mounting polisher (Model MK9K, Strasbaugh, San Luis Obispo, CA). The polishing pad used was a highly porous polymeric material. The dimensions of the silicon wafer and the pad are listed in Table 6.1. The range and typical values of the input variables were fixed. When studying the effects of one factor, only that factor was changed within a suitable range while the other factors were fixed at their default values unless specified otherwise. The MRR is calculated as the difference of the wafer average thickness before and after polishing divided by the polishing time.

Table 6.1 The Dimensions of the Pad and the Wafer

	Pad	Wafer
Thickness	0.7 mm	0.7 mm
Diameter	546 mm	200 mm

The average wafer thickness was measured on a flatness gage, Model Ultragage 9700 (ADE Corporation, Westwood, MA). More information on the Ultragage 9700 flatness gage can be found at www.ade.com.

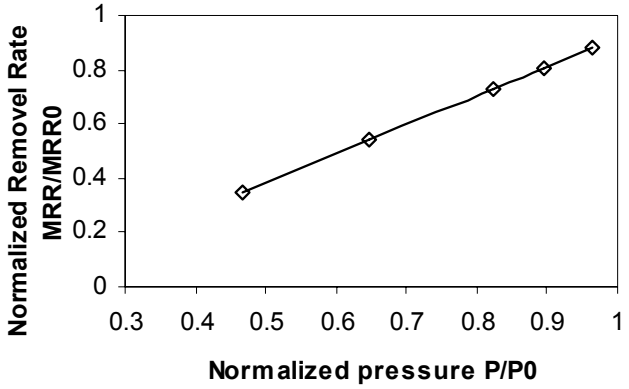
6.3 Results and Discussion

6.3.1 Pressure

The pressure was applied on the backside of the ceramic block via the hub (wafer carrier head). If the applied pressure is changed, the stress or the pressure distribution and even the chemical solution distribution on the wafer surface change accordingly, affecting the material removal rate. According to Preston's equation [Preston, 1927], if everything else is kept unchanged, as the applied pressure increases, the material removal rate will increase linearly. The experimental results show the linear trend which is consistent with Preston's equation (Fig. 6.3). The pressure and the material removal rate have been normalized. *P0* and *MRR0* are the maximum values for applied pressure and material removal rate respectively.

The material removal rates of other materials such as oxide and metal in polishing [Tseng et al., 1997; Steigerwald et al., 1997] also show the same trend. The increased pressure will increase the friction between the wafer and pad, so that more material can be removed off the wafer surface.

Figure 6.3 Effects of Applied Pressure on MRR



6.3.2 Wafer Speed and Pad Speed

The wafer with the carrier head rotates in the same direction as the platen (table) on which the pad is attached. If the wafer speed or the pad speed is changed, the relative velocity between the wafer and the pad is changed consequently. According to Preston's equation, the MRR is proportional to the relative velocity if all the other conditions are unchanged. If the oscillation of the polishing arm is ignored, the relationship between the wafer speed or the pad speed and the relative velocity is a second order function [Saka, 2001]:

$$V_r^{\,2} = \left[\left(\omega_w - \omega_p\right)y\right]^2 + \left[\left(\omega_w - \omega_p\right)x - \omega_p r_{cc}\right]^2 \tag{6.1}$$

Vr is the relative velocity between the pad and the wafer. The coordinates of the point on the wafer are x and y. The wafer and pad rotate at an angular speed of ω_w and ω_p respectively. According to equation (6.1), if wafer speed is equal to pad speed, the relative velocity is a minimum value, resulting in the lowest material removal rate. A change in either wafer speed or pad speed will result in a change in the relative velocity between them.

But in this experiment, when the wafer speed changes within the tested range, the MRR does not change significantly (Fig. 6.4). Since the radius of the wafer is much smaller than the pad's radius, the angular speed ($V = \omega \cdot r$) does not change much when the wafer speed changes.

However the change in the wafer speed may cause other problems, such as uneven pad wear, and poor global wafer shape.

The global wafer shape is defined by a parameter α. The measurement of α is done with respect to an imaginary plane formed by three points on the wafer. A negative value of α indicates a dished wafer (concave); a positive value of α indicates a domed (convex) wafer (Fig. 6.5). Fig. 6.6 shows the relationship between the wafer speed and α value. The results show that the wafer speed is not a significant factor to the global shape.

Figure 6.4 Effects of Wafer Speed on MRR

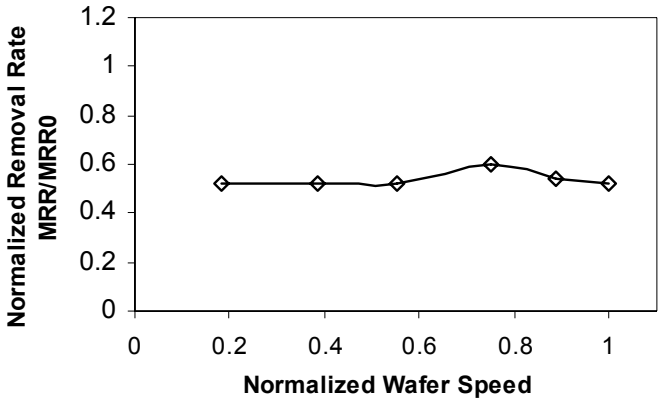


Figure 6.5 The Global Wafer Shape α Value

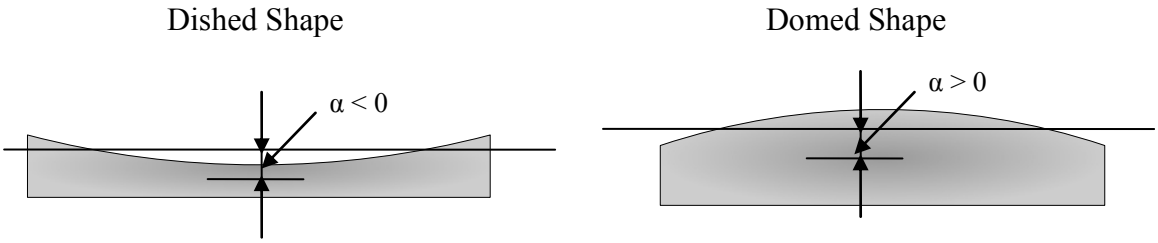
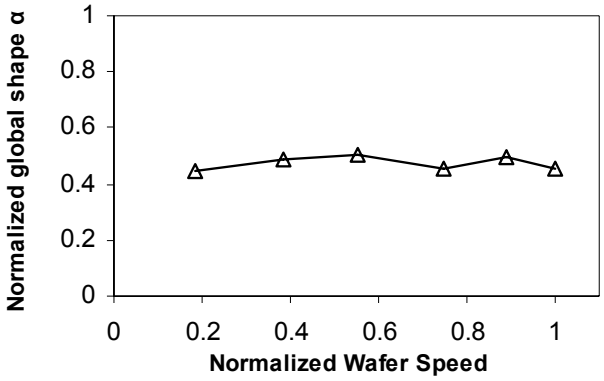


Figure 6.6 Effects of Wafer Speed on Global Shape α Value



But usually, for other materials in other polishing processes, the material removal rate is increased by using a higher carrier rotation speed [Tseng et al., 1997]. In this point, the wax mounting polishing of silicon wafer is different from others. So it is necessary to further study the polishing process of silicon wafers.

The pad speed is another factor that determines the relative velocity between the wafer and pad according to equation (6.1). Fig. 6.7 shows the effects of pad speed on MRR. The radius of pad is much larger than that of the silicon wafer, so the rotation speed of pad affects the relative velocity much more than the wafer speed does. As the pad speed increases, the MRR increases, and α value is decreased (Fig. 6.8). Therefore, the pad speed is a significant factor to both MRR and wafer global shape. Higher pad speed helps to increase MRR and get good wafer shape, consistent with the results of others' experiments and modeling [Fu et al., 2001]. But, when the pad speed is too high, non-desirable scratches may appear on the wafer surface.

Figure 6.7 Effects of Pad Speed on MRR

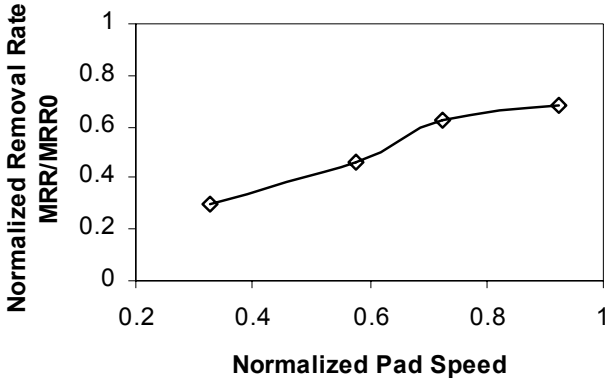
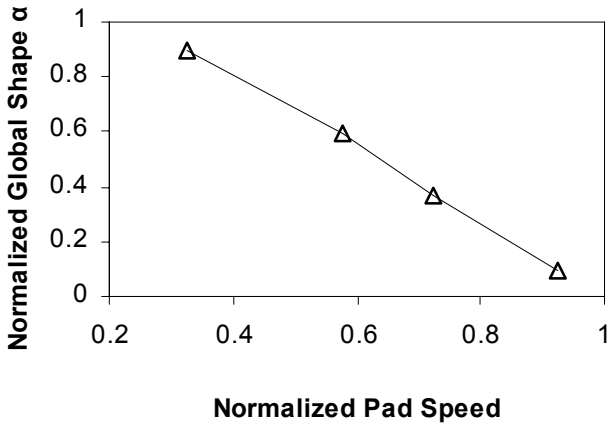


Figure 6.8 Effects of pad Speed on α Value

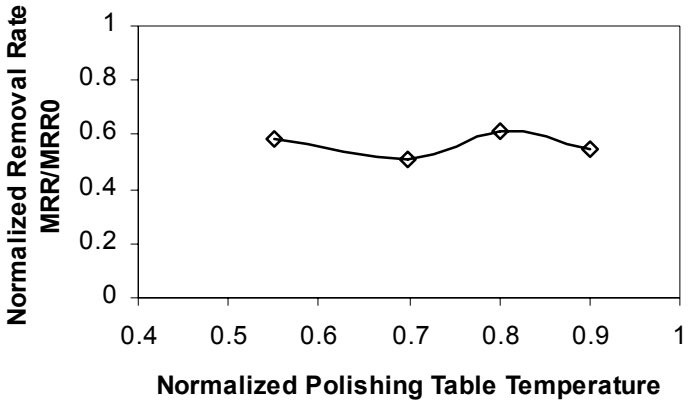


6.3.3 The Temperature of the Polishing Table

An increase in temperature is expected in polishing. The temperature can be controlled to some extent by maintaining the temperature of the polish table with recirculation water. Fig. 6.9 shows the relationship between the temperature of the polishing table and MRR. The temperature of the polishing table affects the temperature at the interface between the pad and wafer and the chemical reaction rate between the slurry and the wafer material, affecting the MRR on the wafer

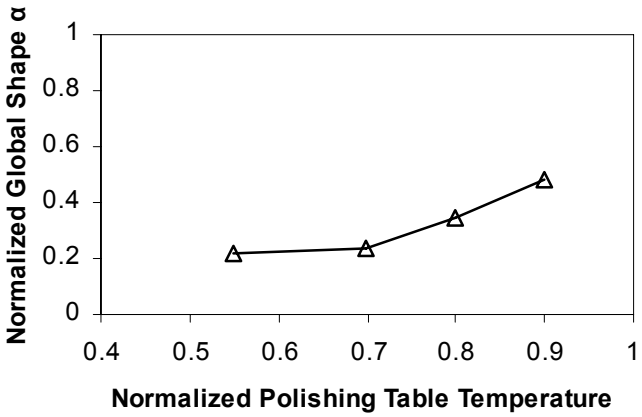
surface. However, within the temperature range tested, the temperature of the polishing table is not a significant factor on the MRR.

Figure 6.9 Effects of Polishing Table Temperature on MRR



Although the MRR doesn't change much with the polishing table temperature, the global shape α value increases when the polishing table temperature increases (Fig. 6.10). So maintaining a lower table temperature can help to reduce α to get a flat wafer surface.

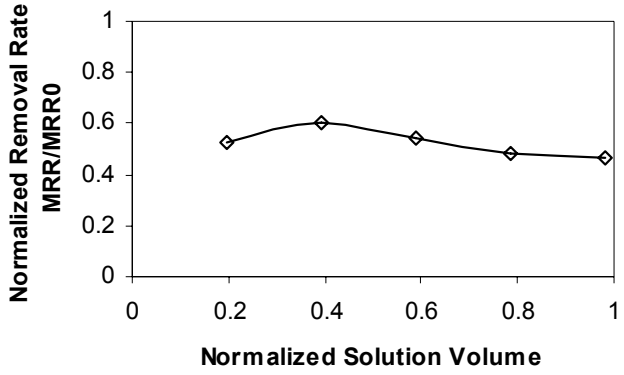
Figure 6.10 Effects of Table Temperature on α Value



6.3.4 Slurry Volume during Polishing

The polishing slurry serves the purpose of smoothing the contact surface but also acts as the carrier of the removed material. It affects how quickly new chemicals and abrasives are delivered to the pad. When the slurry volume is reduced significantly, the material removed from the wafer surface accumulates on the pad (due to insufficient liquid flow to flush it out) resulting in a brown ring on the pad, referred to as pad browning. However, from Fig. 6.11, it can be seen that within the tested range the slurry volume is not a significant factor in influencing the MRR.

Figure 6.11 Effects of Slurry Volume on MRR



In summary, from the results presented in the previous sections, pad speed and applied pressure are the factors that have significant effects on the MRR in polishing of silicon wafers. To further the understanding of the effects of these two factors, a two-factor three-level factorial design was used to conduct further experiments.

6.4 The Designed Experiment of Pad Speed versus Polishing Pressure

Three levels of the pad speed and polishing pressure were chosen for the experiment. Consistent with the previous experiments, the MRR increases with the applied pressure and pad speed. But pad speed and the pressure have an interaction effect on the MRR. When the pressure is low, changing the pad speed does not have a significant effect on the MRR. But when the

pressure is high, the difference in the MRR at the three levels of pad speeds becomes significant (Fig. 6.12).

Figure 6.12 The Relationship between the Polishing Pressure and MRR

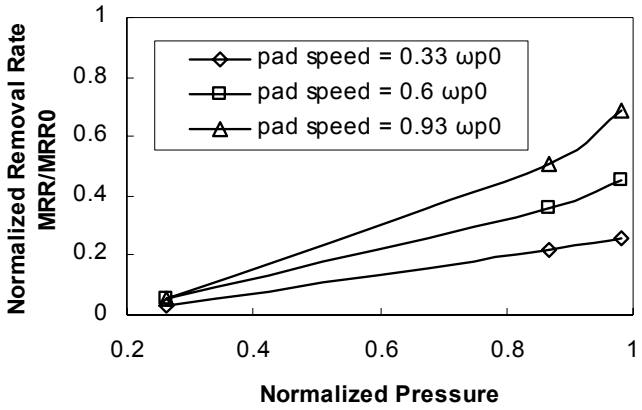


Fig. 6.13 shows the effects of the pad speed and the pressure on α value. For the response of α value, pad speed and the pressure have an interaction effect. As a conclusion of the two-factor three-level experiment, using a higher pressure and a higher pad speed is better for increasing the MRR and reducing the α value.

Figure 6.13 The Relationship between the Pressure and α Value

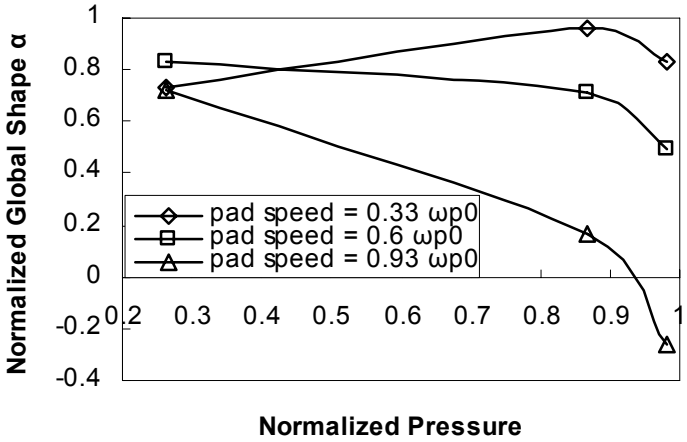


Table 6.2 ANOVA of the MRR in the Designed Experiment

Source	Sum of Squares	DF	Mean Square	F Value	Prob>F
Pad Speed(A)	0.22	2	0.11	0.52	0.6174
Pressure(B)	1.22	2	0.61	12.54	0.0072
AB	0.067	4	0.017	0.047	0.9942
Cor Total	1.51	8			

Table 6.3 ANOVA of α Value in the Designed Experiment

Source	Sum of Squares	DF	Mean Square	F Value	Prob>F
Pad Speed(A)	0.87	2	0.44	2.64	0.1505
Pressure(B)	0.43	2	0.21	0.90	0.4565
AB	0.56	4	0.14	0.43	0.7816
Cor Total	1.51	8			

The ANOVA of MRR is in Table 6.2. The polishing pressure has more significant effect on the MRR from the analysis of variance table. Table 6.3 shows the ANOVA for α values. When the polishing pressure is small, changing pad speed does not make much difference in α values. Only when the pressure is higher, increasing the pad speed can reduce α value.

6.5 Summary

1. Polishing pressure and pad speed are the most significant variables affecting the material removal rate (MRR) in polishing of silicon wafers. Increasing polishing pressure or pad speed can increase the MRR.

2. Although both wafer speed and pad speed contribute to the relative speed between wafer and pad which has a linear relationship with the MRR according to Preston's Equation, wafer speed within the test range does not affect the MRR and global shape. However, when the pad speed is increased, the MRR increases and α value also increases indicating that the global shape of the wafer becomes more convex.

3. Changing the temperature of the polishing table within the test range does not affect the MRR much. But maintaining lower table temperature is better for reducing α value.

4. The slurry volume within the test range is not significant factors affecting the MRR.

5. For the MRR, the polishing pressure has more significant effect than the pad speed. Both the pad speed and the interaction between pad speed and the polishing pressure are not significant in the three-level two-factor experiment.

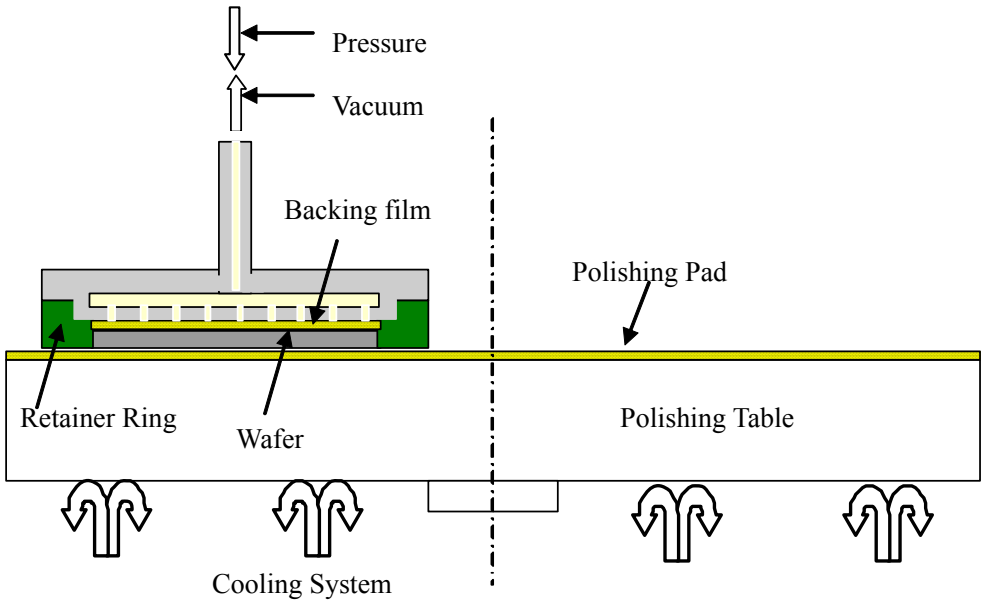
6. For the global shape α value, none of the polishing pressure, pad speed and the interaction between pad speed and the polishing pressure is not significant in the three-level two-factor experiment. But using a higher pressure and a higher pad speed is better for reducing α value to get a good wafer shape.

CHAPTER 7 - Finite Element Analysis on CMP of Silicon Wafers: Wafer Shape

7. 1 Introduction

The global wafer shape is also a concern for manufacturing high quality wafers. As described in chapter 5, either a domed or a dished wafer shape exists under different conditions. The non-uniformity of temperature distribution, pad wear on wafer surface, etc., cause wafer to "dish" or "dome". The material removal uniformity is affected not only by the wafer deformation itself during the polishing process, but also by the shape or deformation of the carrier. Fig. 7.1 shows how wafer is mounted in a carrier.

Figure 7.1 Illustration of the Structure of Polishing Head



The wafer is mounted in a carrier on a backing film. The retaining ring keeps the wafer in place horizontally. During loading and unloading, the wafer is kept in the carrier by the vacuum. During chemical mechanical polishing, pressure is applied by the down force on the carrier, transferred to the carrier through the carrier axis. If the vacuum or the back pressure is applied on the back side of the carrier, the carrier is deformed and has a curved shape, affecting the wafer

deformation and the material removal uniformity. The geometry of the carrier (such as the shape of the carrier front side and the carrier thickness) also affects the material removal uniformity during polishing.

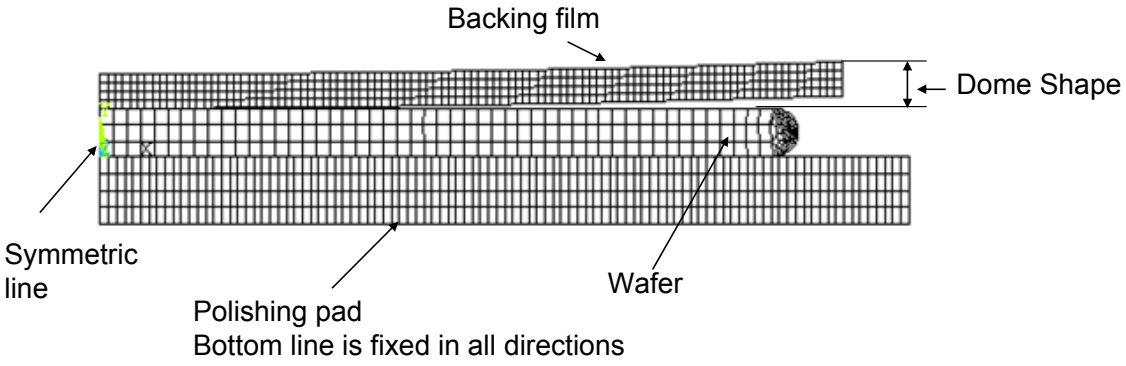
The shape of the carrier front side, the back pressure applied on the carrier, and the carrier thickness are three important factors on wafer global shape. In this chapter, the effects of those factors are investigated. The contact pressure between wafer and polishing pad is calculated by using FEA models. The wafer global shape is defined as the difference between the material removal amount on the wafer center and that on the wafer edge. The Preston's equation is used to calculate the material removal.

7.2 Effects of Carrier Front Surface Shape

7.2.1 The FEA Model

In the polishing head, the backing film is glued on the carrier (Fig. 7.1). The carrier front side is ground to be a dished or a domed shape before the backing film is attached. The backing film is so soft that it is conformed almost perfectly on the carrier surface. Therefore, to reduce the element number, the backside of the backing film is considered as a rigid line to simulate its interface with the carrier front side. Fig. 7.2 shows the FEA model in which the curved backing film implies the carrier has a dome shape.

Figure 7.2 FEA Model of Curved Backing Film



All of the assumptions and boundary conditions of this model are the same as the model in chapter 4 except that the backing film is glued on the domed carrier front side. The difference between the Z-position of backing film at the wafer center and that at the wafer edge indicates the amplitude of the dome.

7.2.2 Results

As the carrier front side (and the backside of the backing film) gets more domed (increasing from 1 μm to 5 μm), the contact pressure on the wafer surface will get larger at the center and smaller at the wafer edge, resulting in a larger difference in material removal from the wafer center to the edge (Fig. 7.3). As the carrier gets more domed, the wafer is more dished. The relationship shown in Fig. 7.4 is approximately linear. If the wafer shape is dished/domed before polishing, then by changing the shape of the carrier by doming/dishing in the opposite way, the wafer shape could be corrected and improved.

Figure 7.3 Pressure Distribution on Wafer Surface

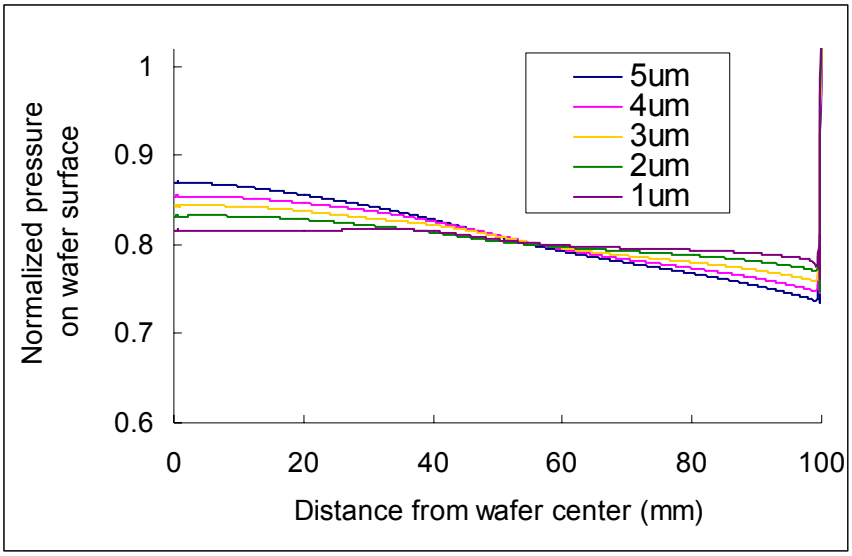
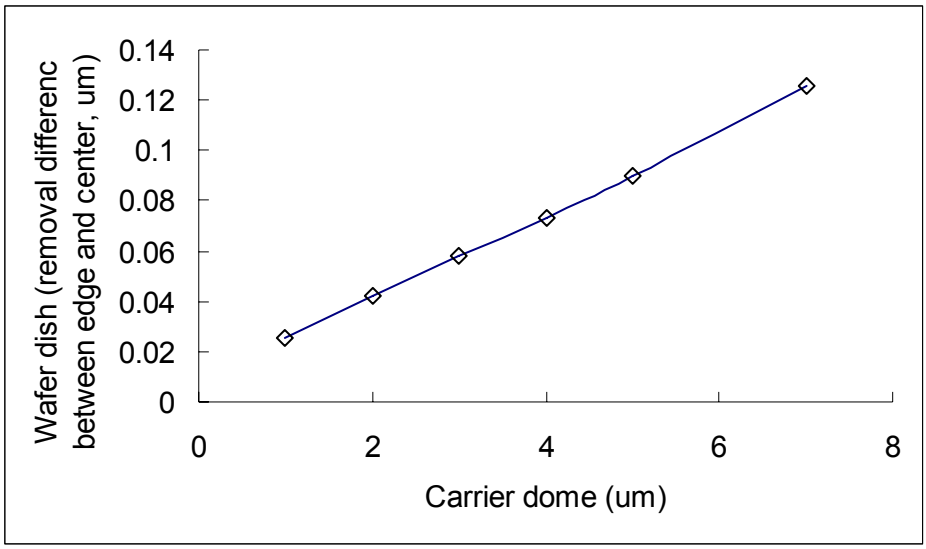


Figure 7.4 Wafer Shape vs. Carrier Shape

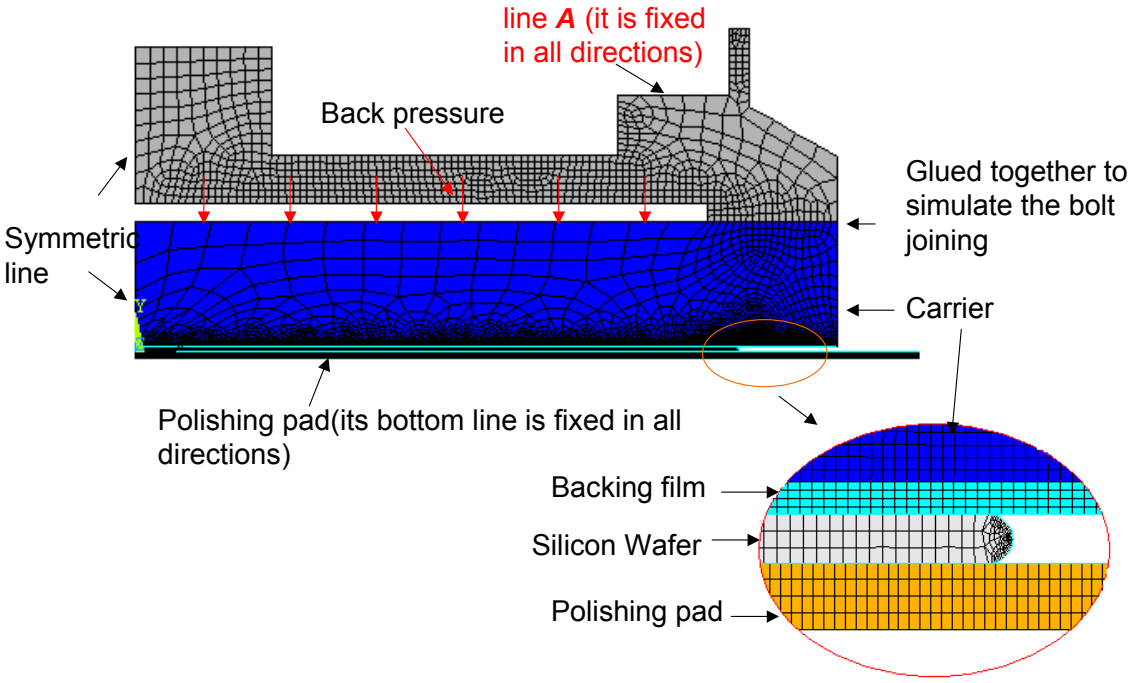


7.3 Effects of Back Pressure on Wafer Shape

7.3.1 The FEA model

The pressure or vacuum applied on the backside of the carrier also plays an important role in changing the shape of the carrier and, hence, to change the wafer shape. The carrier with the backing film is joined by a bolt with the hub adapter (the hub adapter is used the connected wafer carrier and the hub in the polishing head). Fig. 7.5 is the FEA model when the carrier is attached on the hub adapter.

Figure 7.5 The FEA Model of the Carrier Head



The boundary conditions of this FEA model are:

- The backing film is glued on the carrier.
- The hub adapter and the carrier are glued together to simulate the fact that they are joined by bolts.
- The top line of the hub adapter (line A) is fixed in all direction to simulate its connection with the upper part of CMP machine.
- Since the purpose of this study is to understand how the back pressure affects the wafer shape, the pressure is only applied on the back side of carrier, no additional polishing pressure is applied. Consequently, pressure distribution and material removal difference between wafer center and edge are caused only by the back pressure for simplification.

The carrier is attached on the hub in the polishing head. The pressure and the vacuum could be applied backside of the carrier. The back pressure or the vacuum will bend the carrier downward or upward. Hence, the final wafer shape will be changed. Contact pairs are created between wafer and pad and between wafer and backing film.

7.3.2 Results

Fig. 7.6 shows the pressure distribution, as back pressure applied on the backside of the carrier is increased. The pressure at the wafer center is larger than that at the wafer edge, implying more material removal at the wafer center. Therefore, the wafer is dished. The relationship between the back pressure and the wafer dish is approximately linear (Fig. 7.7).

Figure 7.6 Pressure Distribution on Wafer Surface when Back Pressure Changes

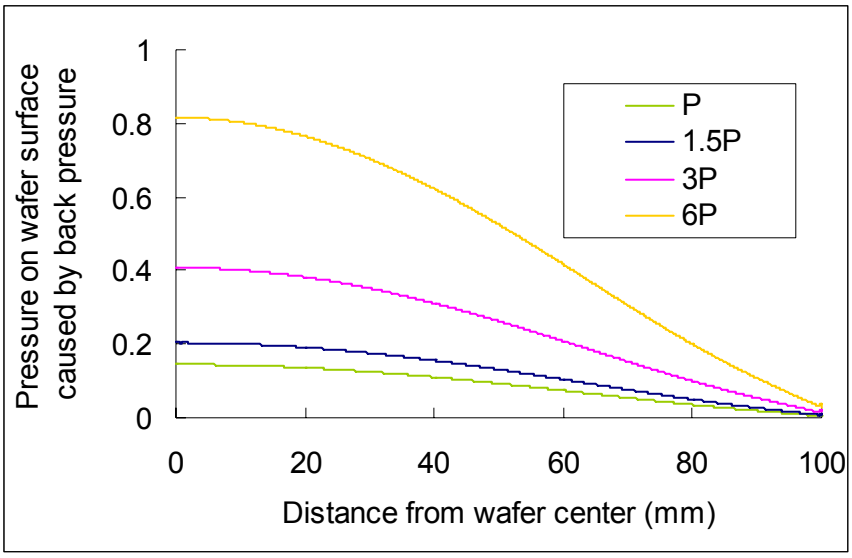
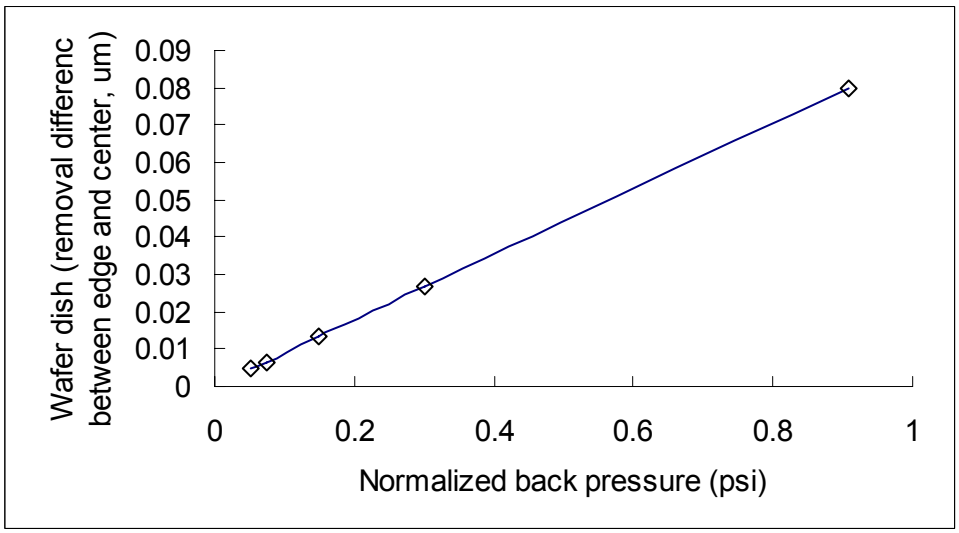


Figure 7.7 Wafer Dish vs. Back Pressure



7.4 Effects of Carrier Thickness

A carrier with different thickness under the same back pressure will have different deflection, causing the pressure distribution on the wafer surface different (Fig. 7.8). As the carrier thickness decreases, the pressure on the wafer surface will increase (Fig. 7.9). But the relationship between the wafer shape and the back pressure of the carrier remains linear. As the carrier gets thinner, wafer shape becomes more sensitive to the change in back pressure.

Figure 7.8 Pressure Distribution on Wafer with Different Carrier Thickness

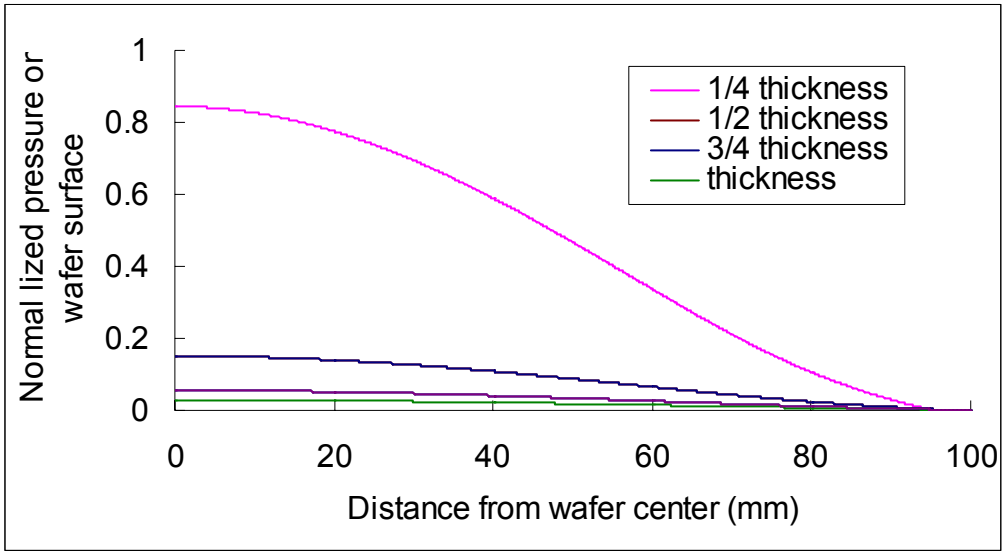


Figure 7.9 Wafer Shape vs. Back Pressure

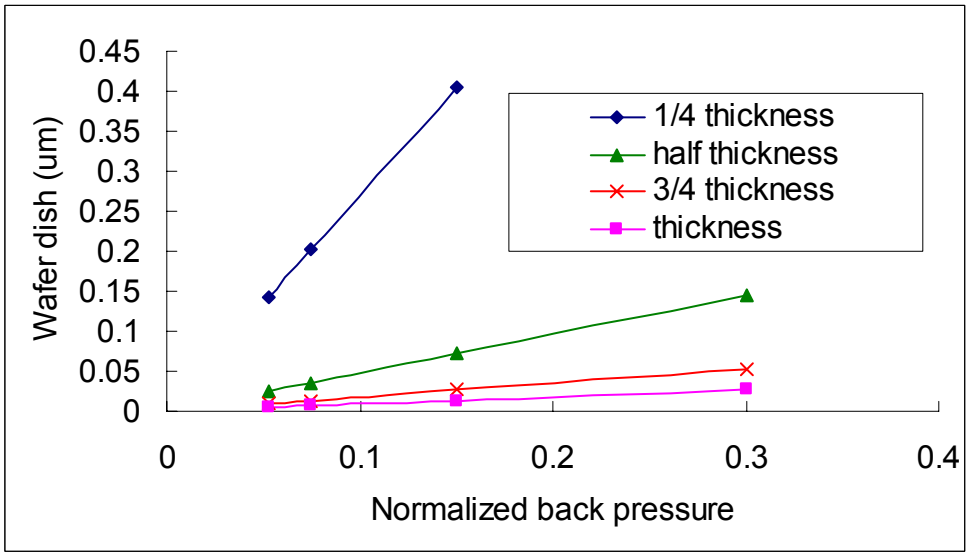


Figure 7.10 Back Pressure vs. Carrier Thickness

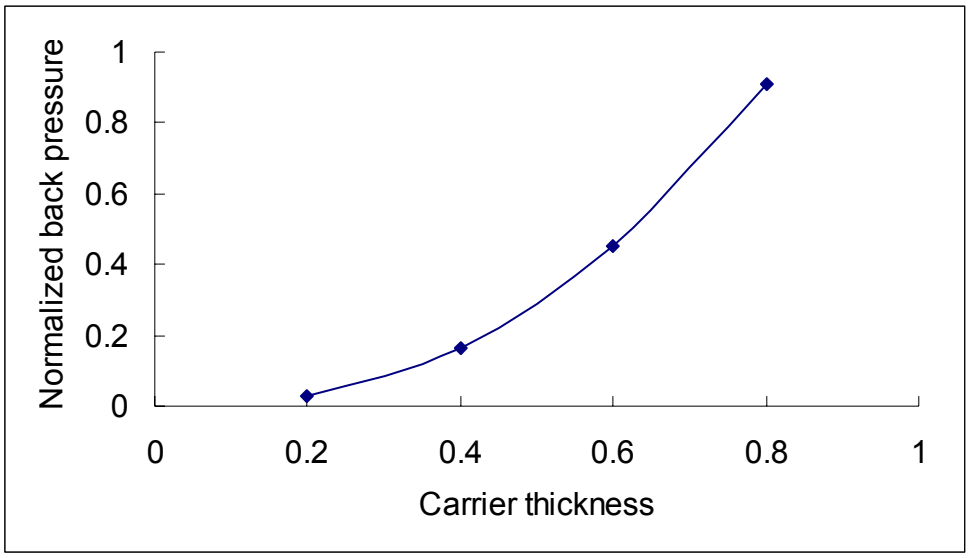


Fig. 7.10 shows that, to keep the same wafer shape, the back pressure needed is increased with the increasing of carrier thickness. However, the relationship is not linear any more.

7.5 Summary

The effects of the carrier front side shape, the back pressure, and the carrier thickness on the wafer shape are studied in this chapter:

The more domed the original carrier surface is, the more dished the wafer shape will become.

The larger the back pressure is, the more dished the wafer will become.

The thinner the carrier is, the less the pressure needed to get the same wafer shape will be.

CHAPTER 8 - Generation Mechanisms of Central Dimples on Ground Wafers

8.1 Introduction

As the dimension shrinkage of ICs, the wafer flatness plays more and more roles on device line-width capability, process latitude, yield, and throughput [Kulkarni, 2001, Oh, 2001]. Pei et al. [2005] demonstrated that grinding has the potential to manufacture flat silicon wafers at a lower cost. They investigated experimentally that the site flatness on the ground wafers (except for a few sites at the wafer center) could meet the stringent specifications for future silicon wafers. At the wafer center, one of the irregularities is central dimples causing the poor flatness on ground wafers. The objectives of this chapter are to understand the generation mechanisms of the central dimples and to provide practical guidance to eliminate or reduce central dimples on ground wafers.

There are six sections in this chapter. Following this introduction section, section 8.2 provides some background information about wafer grinding. In section 8.3, procedures to develop the finite element model are presented. The developed model is used in section 8.4 to predict the relations between the influencing factors (including Young's modulus and Poisson's ratio of the grinding wheel segment, dimensions of the wheel segment, grinding force, and chuck shape) and the size of the central dimple. Section 8.5 provides the pilot experimental results to substantiate the predicted results from the finite element model. Section 8.6 comprises the conclusions.

8.2 Central Dimples on Ground Wafers

Central dimples have been observed on some ground wafers. Fig. 8.1 illustrates the central dimple. This picture is a printout of UltraGage 9500 [www.ade.com]. Typically, for a silicon wafer with a diameter of 200 mm, its thickness is about 0.75 mm. The size of central dimples ranges from 10 mm to 30 mm in diameter, with a depth of less than 0.2 μm (0.0002 mm).

Figure 8.1 A Ground Wafer with a Central Dimple

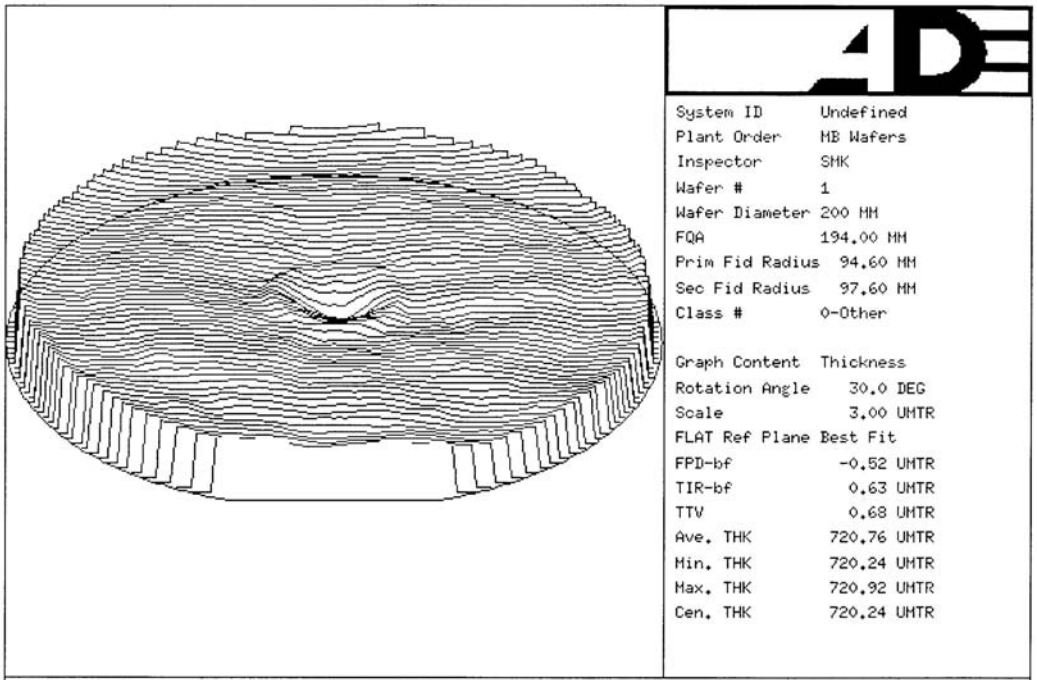
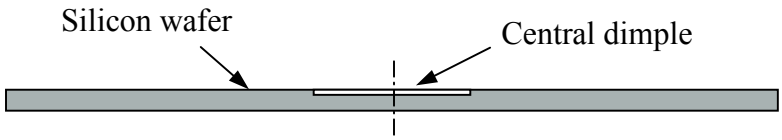


Figure 8.2 Illustration of a Central Dimple Cross Section View

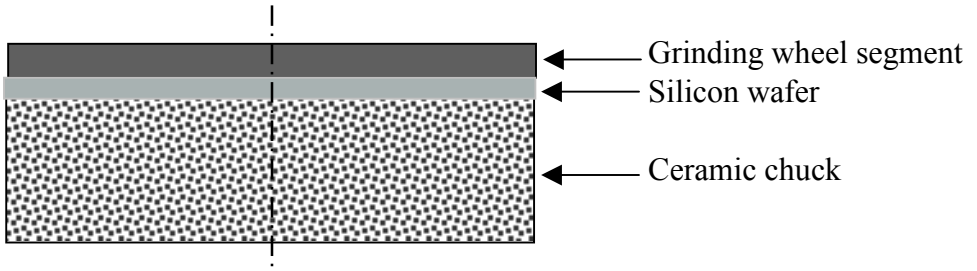


The central dimples affect the site flatness at the wafer center, which make the wafer center area unusable. Their elimination is critical to the improvement of silicon wafer grinding performance. However, it will be very difficult, if not impossible, to eliminate them if their generation mechanisms are unknown. This study is the first attempt (in the public domain) to understand the generation mechanisms of the central dimples on ground wafers and, based on this understanding, to provide solutions to eliminate or reduce the central dimples.

In grinding process, the wafer is held on a porous ceramic chuck by means of vacuum. The ceramic chuck is typically ground to a conic shape with a very small slope, as shown in Fig. 8.3(b). The graphs in Fig. 8.3 are cross-sectional views along the centerline of the wheel segment. When the wafer is held onto the chuck, it elastically deforms to the chuck's conic shape, thus

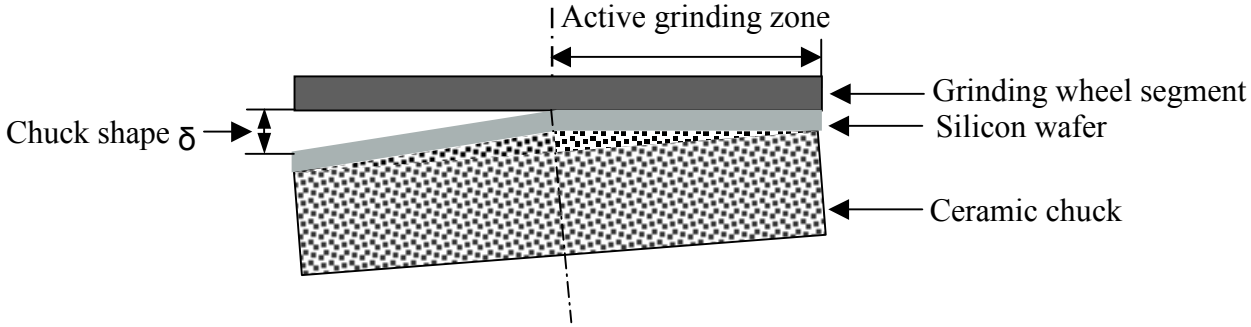
ensuring that the grinding wheel only contacts half of the wafer. This contact area is marked as "Active Grinding Zone" in Fig. 2.20.

Figure 8.3 Cross-Sectional Views of the Wheel Segment, Wafer, and Chuck



(a) Flat chuck ($\delta = 0$)

(b)



(c) Conic chuck ($\delta > 0$)

The hypothesis for the generation mechanisms for central dimples is as follows. During grinding, due to the grinding force, the portion of the grinding wheel segment that is in contact with the silicon wafer (or, the portion of the wheel segment that is within the active grinding zone) will elastically deform. This deformation will cause the portion of the wheel segment that is next to the active grinding zone to contact with (cut into) the silicon wafer near the wafer center. The cutting action of this portion of the wheel segment (outside the active grinding zone) will remove material from the silicon wafer near the wafer center, in addition to the material removed by the portion of the wheel segment within the active grinding zone. The additional

removal of material near the wafer center (on the opposite side of the active grinding zone) generates the central dimples.

In the following two sections, a finite element model is developed based on this hypothesis. Then, the developed model is used to predict the relationships between the influencing factors (including mechanical properties and geometry of the grinding wheel segment, chuck shape, and grinding force) and the dimple size.

8.3 Development of the Finite Element Model

Fig. 8.4 schematically displays the two-dimensional (2D) model developed. Please note that the height of the cone, δ, the measure of the chuck shape, is greatly exaggerated for illustration purpose.

A two-dimensional (2D) element model was built on the cross-section shown in Fig. 8.3. Please note that the cross-section is along the centerline of the wheel segment. The reasons that a 2D (instead of 3D) finite element model was used include the followings. Firstly, the focus of this study is the elastic deformation of the grinding wheel segment. Since the wheel segment is about 2 to 5 mm wide, 3D models will not add significantly more insights than the 2D model. Secondly, the 2D model requires a much smaller number of total nodes and much less computing time.

The finite element model was based on the following assumptions and simplifications.

1. The grinding process was modeled as a static problem (i.e., any dynamic effects were ignored), since the focus of this study was the elastic deformation of the wheel segment under the grinding force (i.e. the reaction force between the wheel segment and the wafer).
2. Since silicon wafers have much higher (two to three magnitude higher) Young's modulus than the wheel segment, the silicon wafer in the finite element model was modeled as a rigid body.
3. The grinding wheel was assumed to have a single segment.
4. Material removal would occur wherever the wheel segment was in contact with the wafer.

5. The radius of the central dimple on a ground wafer was computed as the contact length (measured from the wafer center) between the wheel segment and the wafer on the other side of the active grinding zone.

Since the areas around the wafer center were of major interest, finer meshes were employed for the portion of the wheel segment near the wafer center. Contact elements were used to model the wafer-wheel interface. Since the wafer was treated as a rigid body, the contact elements for the wafer-wheel pair were of rigid-flexible type.

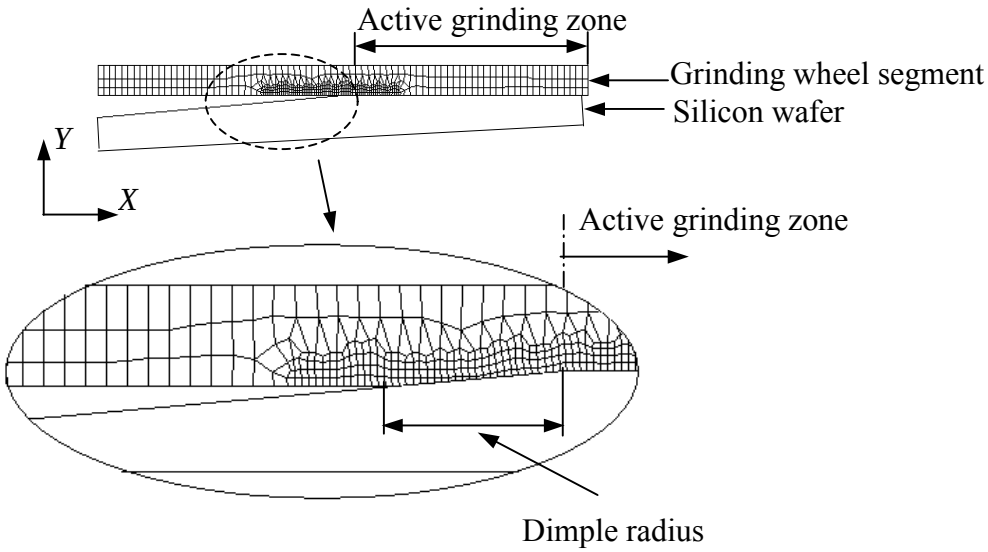
As shown in Fig. 8.4, the boundary conditions include the followings.

1. DOF (degree-of-freedom) constraints: The top line of the wheel segment was constrained from moving in the X direction. For the silicon wafer, its pilot node (whose motion governs the motion of the entire wafer) was constrained from moving in the X or Y directions to simulate the support from the ceramic chuck.

2. Forces: The grinding force was loaded on the top line of the wheel segment in the Y direction. The grinding force would cause a portion of the wheel segment to contact the wafer and even deform elastically.

3. Contacts: A contact element pair was created between the wafer and the wheel segment. The pair consists of TARGE169 and CONTAL72 elements (both are standard elements in the ANSYS package).

Figure 8.4 Illustration of the Finite Element Model



Six influencing factors were considered in the finite element model. Typical ranges for these influencing factors and their default values used in the finite element model are listed in Table 8.1. When studying the effects of one factor on the dimple size, only that factor was changed within a suitable range while the other factors were fixed at their default values unless specified otherwise.

Table 8.1 Typical Ranges for the Factors Considered and Their Default Values

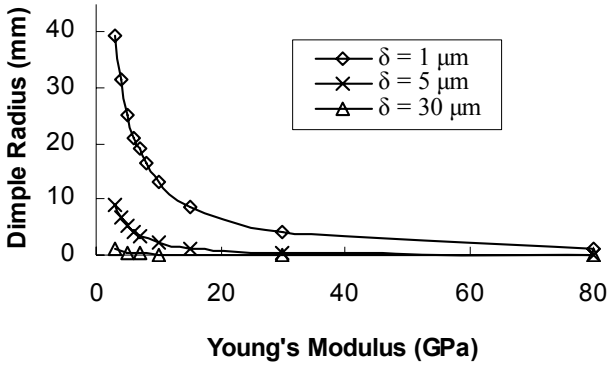
Factor	Unit	Typical range	Default value
Young's modulus of the grinding wheel segment	GPa	1 ~ 80	7
Poisson's ratio of the grinding wheel segment		0.2 ~ 0.4	0.3
Chuck shape (δ)	μm	1 ~ 30	1
Wheel segment width	mm	2 ~ 5	3
Wheel segment height	mm	3 ~ 7	5
Grinding force	N	67 ~ 200	100

8.4 Effects of Influencing Factors on Dimple Size

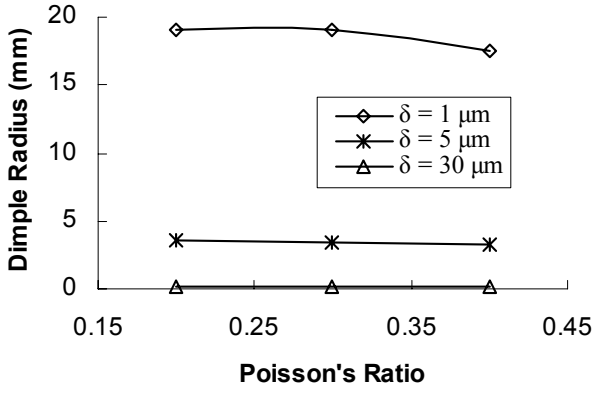
8.4.1 Mechanical Properties of the Grinding Wheel Segment

Fig. 8.5 shows how the mechanical properties of the grinding wheel segment affect the dimple radius. It can be seen from Fig. 8.5a that, as Young's modulus increases, the dimple radius will decrease. If Young's modulus of the wheel segment is sufficiently high, the dimple radius can be reduced to practically zero, and therefore there will be no central dimples on the ground wafer.

Figure 8.5 Effects of Mechanical Properties of the Grinding Wheel Segment



(a) Young's modulus



(b) Poisson's ratio

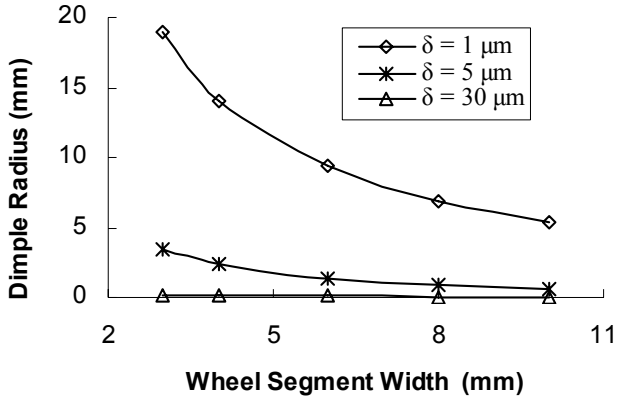
The interaction effects of Young's modulus of the wheel segment and the chuck shape can also be clearly seen in Fig. 8.5a. The effects of Young's modulus are enhanced for the chuck shape with a larger conic height. However, the effects of Poisson's ratio on the dimple radius are relatively trivial, as shown in Fig. 8.5b. The dimple radius changes very little as Poisson's ratio changes from 0.2 to 0.4.

The practical implication of the results is as follows. In order to eliminate or reduce the central dimples on ground wafers, grinding wheels whose segments have sufficiently high Young's modulus should be used.

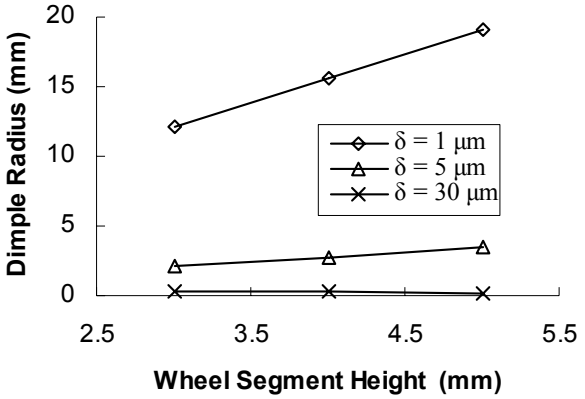
8.4.2 Geometry of the Grinding Wheel Segment

Fig. 8.6 shows the effects of the geometry (width and height) of the grinding wheel segment on the dimple radius. It can be seen from Fig. 8.6a that, as the wheel segment becomes wider, the dimple radius becomes smaller. Please note that this conclusion is obtained based on a constant grinding force. When the grinding force is constant, a wider wheel segment will have a larger contact area with the silicon wafer and hence a smaller stress. Consequently, the elastic deformation will be smaller, resulting in a smaller dimple radius. However, if the grinding force also changes as the wheel segment gets wider, it is possible that this conclusion will no longer be true.

Figure 8.6 Effects of Geometry of the Grinding Wheel Segment



(a) Width of wheel segment



(b) Height of wheel segment

Fig. 8.6b shows the relationship between the wheel segment height and the dimple radius. It can be seen that when the wheel segment is higher, the dimple radius will be larger.

The interaction effects between the chuck shape and the wheel segment width (as well as height) are obvious in Fig. 8.6. When the chuck is flatter (δ is smaller), the change in the wheel segment width (or height) causes a larger change in the dimple radius.

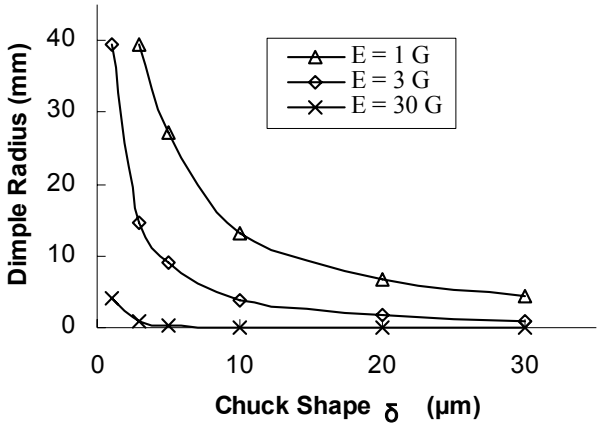
In summary, central dimples can be lessened if the wheel segment is made shorter and/or wider. (Please note that a wider wheel segment can reduce the dimple radius only if the grinding force is kept the same).

8.4.3 Chuck Shape

The effects of the chuck shape on the dimple radius are shown in Fig. 8.7. As the chuck gets flatter, the dimple radius increases exponentially. A chuck with a conic shape whose conic height is sufficiently large can effectively prevent the occurrence of central dimples on ground wafers.

The above results have provided an effective, yet relatively inexpensive, solution to the central dimple problem in grinding of silicon wafers. It involves using a conic chuck with a sufficiently large cone height. It does not involve any modifications on grinding wheels.

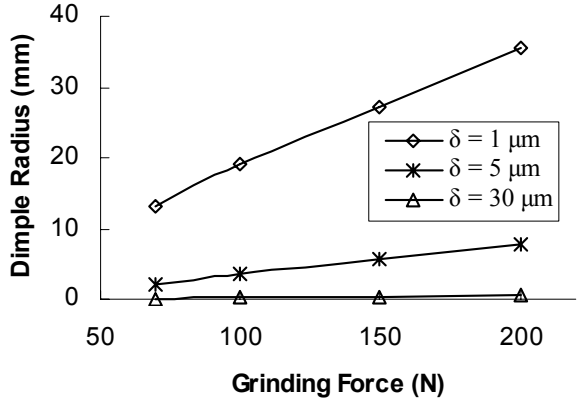
Figure 8.7 Effects of Chuck Shape



8.4.4 Grinding Force

Fig. 8.8 shows the relationship between the grinding force and the dimple radius. As the grinding force increases, the wheel segment will deform more. This will increase the dimple size. Therefore, from the perspective of reducing the central dimples on ground wafers, smaller grinding forces are desirable.

Figure 8.8 Effects of Grinding Force



The interaction effects between the chuck shape and the grinding force can be observed from Fig. 8.8. When the chuck is flatter (δ is smaller), the change in the grinding force causes a larger change in the dimple radius.

8.5 Pilot Experimental Verification

8.5.1 Experimental Conditions

Grinding experiments were conducted on a Strasbaugh Model 7AF wafer grinder (Strasbaugh, Inc., San Luis Obispo, California). The grinding wheels used were diamond cup-wheels. The grit size for the coarse grinding wheel was mesh #320. The grit size for the fine grinding wheels was mesh #2000. One of the fine wheels had a larger Young's modulus than the other fine wheel. The radius of the wheels was 140 mm.

Single crystal silicon wafers of 200 mm in diameter with the (1 0 0) plane as the major surface (the front or back surface of the wafer) were used for this investigation. To ensure the consistency of test wafers, all wafers were lapped using the same lapping conditions prior to grinding.

Grinding parameters and their values are listed in Table 8.2. Note that there were three feedrate values, used for three sequent steps, respectively. During grinding, deionized (purified) water was used to cool the grinding wheel and the wafer surface. The coolant was supplied to the inner side of the cup wheel, at a flow rate of 11.4 liter per minute (or, 3 gallon per minute).

The chuck shape used for the experiments was fairly flat, close to the chuck shape with $\delta = 1$ μm. Due to limitations of currently available measurement tools [Chidambaram et al., 2003], the exact chuck shapes were not known. However, based on the mathematical model for the chuck shape [Chidambaram et al., 2003; Sun et al., 2004; Sun et al., 2005], it is possible to know approximately the chuck shape once the setup parameters are determined.

Central dimples were measured on flatness gages, Model Ultragage 9500 (ADE Corporation, Westwood, MA). More information on the Ultragage 9500 flatness gage can be found at <www.ade.com>.

Table 8.2 Grinding Parameters and Their Values

Parameter	Unit	Coarse grinding	Fine grinding
Removal	μm	23	22
Wheel speed	rev s^{-1} (rpm)	32.05 (1923)	72.50 (4350)
Chuck speed	rev s^{-1} (rpm)	1.67 (100)	9.83 (590)
Feedrate for step 1	μm s^{-1}	1	1
Feedrate for step 2	μm s^{-1}	0.5	0.5
Feedrate for step 3	μm s^{-1}	0.3	0.3

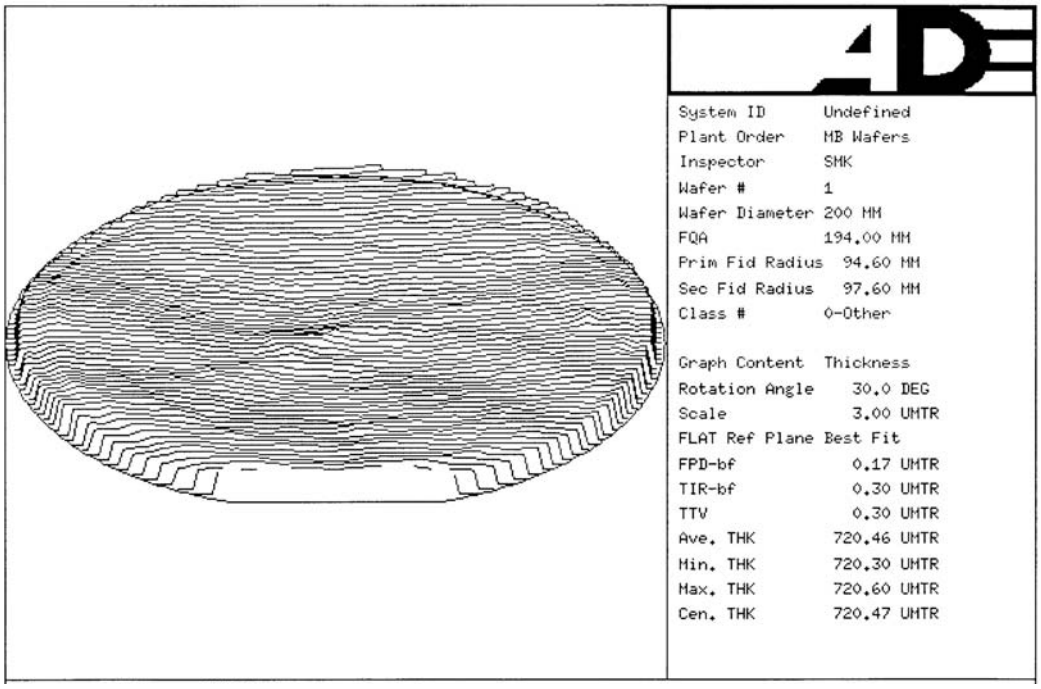
8.5.2 Experimental Results

Fig. 8.9 shows two wafers ground by two grinding wheels (A and B). For wheel A, the Young's modulus of the wheel segment was larger. The wafer ground by this wheel does not have a central dimple, as shown in Fig. 8.9a. The wafer ground by wheel B (its wheel segment has a smaller Young's modulus) shows a central dimple, as shown in Fig. 8.9b.

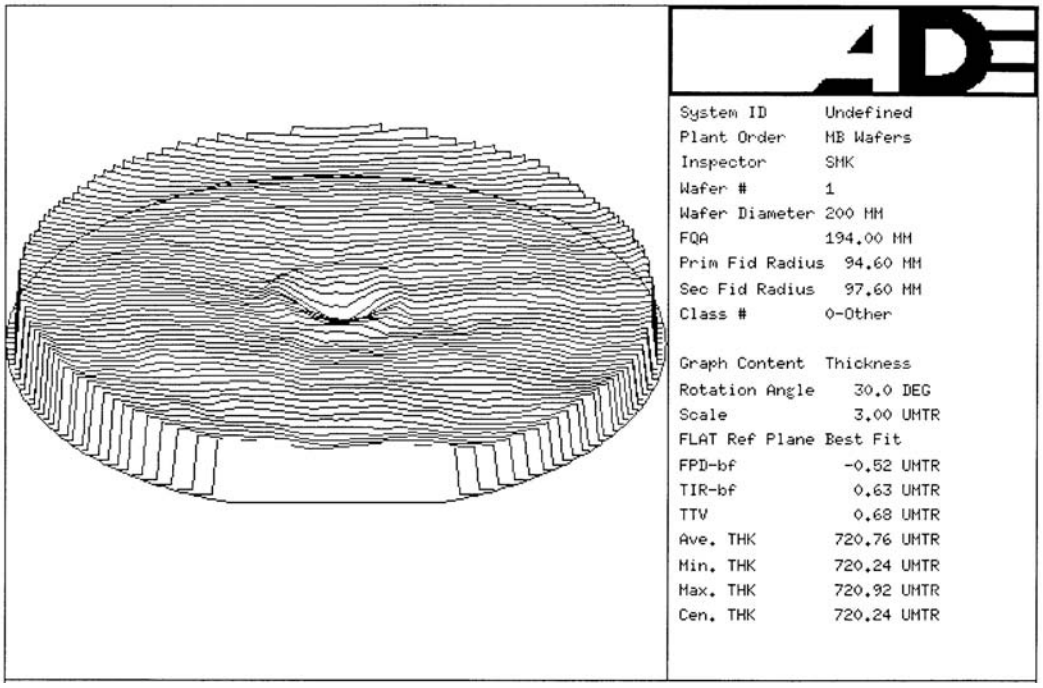
This experimental result is consistent with observations of many grinding tests conducted by other industrial practitioners. They reported that central dimples always appeared on the wafers ground by grinding wheels whose segments had very small Young's modulus.

The pilot experimental results and the reports from industrial practitioners have substantiated the predicted effects of the wheel segment' Young's modulus.

Figure 8.9 Results of Pilot Experiments



(a) Wafer ground by wheel A (with a large Young's modulus)



(b) Wafer ground by wheel B (with a small Young's modulus)

8.6 Summary

This chapter has addressed one of the critical issues in silicon wafer grinding: central dimples on ground wafers. A finite element model has been developed to illustrate the generation mechanisms of central dimples and to predict the effects of influencing factors on the dimple size. Pilot experimental results are consistent with model predictions. Major conclusions from the study are:

1. Central dimples on the ground wafers are due to the elastic deformation of the wheel segment, causing additional material removal at the wafer center outside the active grinding zone.

2. The size of central dimples will increase as the wheel segment's Young's modulus decreases, as the segment height increases or the segment width decreases. The effects of those factors will be much stronger for a flat chuck shape.

3. The size of central dimples will increase as the chuck shape gets flatter.

4. The size of central dimples will increase as the grinding force increases.

The results of this study have provided the practical guidance for eliminating or reducing the problem of central dimples on ground wafers. The most effective measure is to use a conic-shaped chuck with a sufficiently large slope. The second measure involves design and manufacturing of grinding wheels: more rigid segments (larger Young's modulus, larger width, and smaller height for the wheel segments). Finally, it is beneficial to choose grinding conditions that minimize the grinding force (for example, to select a lower feedrate).

CHAPTER 9 - Summaries

9.1 Conclusions of this research

In this dissertation, issues about wafer flatness (waviness, edge effect, taper, global shape) in polishing of silicon wafers are studied with Finite Element Analysis models. The influences of the factors such as the properties of polishing pad and carrier film are addressed. The misalignment of the wafer in the carrier and the carrier geometry are also studied to investigate their effects on wafer flatness. The material removal rate is studied experimentally with different conditions. The central dimple generation mechanism on ground wafers is investigated, and the effects on the dimple size of the geometry and the properties of the grinding wheel segment, grinding force, and chuck shape are studied.

The following conclusions can be drawn from this dissertation:

1. For the wafers with surface undulation, polishing pad with higher Young's modulus and Poisson's ratio, and lower thickness helps to reduce the polishing time. Changing applied pressure does not change the polishing time for removing the surface undulation. However, as the relative velocity between the pad and the wafer becomes larger, the polishing time needed to remove the surface undulation becomes shorter. The surface undulation with large amplitude needs longer polishing time to remove. The wavelength within the studied range doesn't affect the polishing time.
2. Increasing Young's modulus or Poisson's ratio of polishing pad can reduce the stress peak at the wafer edge. The carrier film with higher Young's modulus or lower Poisson's ratio results in better uniformity at the wafer edge. Moreover, the thinner pad or the thicker carrier is better for edge uniformity. And also the smaller gap is better to improve the uniformity at the wafer edge.
3. For chemical mechanical polishing, by changing the shape of carrier front surface, the thickness of the carrier, and the back pressure, the wafer shape (convex or concave) could be corrected.
4. The taper on a polished wafer will be reduced or eliminated if the wafer, block or the back ring are aligned very well. The taper will be worse if the offset of block/back

ring and the offset of wafer/block are in 180º, and will be improved if the offset of block/back ring and the offset of wafer/block are in 0º.

5. Polishing pressure and the polishing table rotation speed are proved to be the most significant factors affecting the material removal rate in silicon polishing by experimental investigation.
6. The central dimple on a ground wafer can be reduced by using a steep chuck, a lower grinding force, and a more rigid wheel (with larger Young's modulus, larger width and smaller height for the wheel segment).

9.2 Contributions of this research

The contributions of this thesis are:

1. For the first time in the public domain, the study of wafer flatness for chemical mechanical polishing reveals the following relationship:
   a) between the process variables (including the mechanical properties of carrier film and geometry on retainer ring) and stress distribution / edge effect.
   b) between the process variables and the polishing time needed to achieve certain flatness.
   c) between the misalignments of wafer center, carrier center and pad ring center and taper value on wafer surface.
   d) between the carrier front surface shape, back pressure, and wafer global shape.
2. For the first time in the public domain, it reveals the generation mechanism of the central dimples on ground wafers.

The research on wafer flatness in this thesis provides practical solutions to reduce the central dimple. Some of results are verified in industry and provide practical solutions and guidance to industry.

Appendix A - References

Adebanjo, R.O., Easter, W.G., Maury, A., Miceli, F., Rodriguez, J.O., 2002, Apparatus and method for in-situ measurement of polishing pad thickness loss, US Patent 6,354,910 B1

Arthur, P.B., Chong, K.P., 2000, Elasticity in Engineering Mechanics, John –Wiley & Sons Inc, New York

Bajaj, R., Desai, M., Jairath, R., Stell, M., Tolles, R., 1994, Effect of polishing pad material properties on chemical mechanical polishing (CMP) processes, Advanced Metallization for Devices and Circuits – Science, Technology and Manufacturability Symposium, 337, pp.637-644

Baker, A.R., 1996, The origin of the edge effect in CMP, Proceedings of Electrochemical Society Meeting, San Antonio, Texas, USA, October, pp.228

Bastawros, A., Chandra, A., Guo, Y., Yan, B., 2002, Pad effects on material-removal rate in chemical mechanical planarization, Journal of Electronic Materials, v.31, n.10, pp.1022-1031

Bawa, M.S., Petro, E.F., Grimes, H.M., 1995, Fracture strength of large diameter silicon wafers, Semiconductor International, v.18, n.11, pp.115-118

Bolton, W., 1989, Engineering Materials Pocket Book, CRC Press, Boca Raton, Florida, USA

Braun, A.E., 2001, CMP becomes gentler, more efficient, Semiconductor International, v.24, pp.54-66

Burke, P.A., 1991, Semi-empirical modeling of SiO2 chemical–mechanical polishing planarization, Proceedings of VMIC Conference., 1112, pp.379-384.

Castillo-Mejia, D., Perlov, A., Beaudion, S., 2000, Qualitative Pridiction of SiO_2 removal rates during Chemical Mechanical Polishing, Journal of the Electrochemical Society, v.147, n.12, pp.4671-4675

Charns, L., Sugiyama, M., Philipossian, A., 2005, Mechanical properties of chemical mechanical polishing pads containing water-soluble particles, Thin Solid Films, v.485, n.1-2, pp.188-193

Che, W., Guo, Y., Chandra, A., Bastawros, A., 2005, A Scratch intersection model of Material removal during chemical mechanical Planarization (CMP), Journal of Manufacturing Science and Engineering, v.127, pp.545-554

Chidambaram, S., Pei, Z.J., Kassir, S., 2003, Fine grinding of silicon wafers: a mathematical model for the chuck shape, International Journal of Machine Tools and Manufacture, v.43, n.7, pp.739-746

Choi, W., Lee, S.M., Singh, R.K., 2004, PH and Down load effects on silicon dioxide dielectric CMP, Electrochemical and Solid-State Letters, v.7, n.7, pp.G141-144

Chung, S.Y., 2006, Monitoring apparatus for polishing pad and method thereof, US Patent 6,995,850 B2

Fischer-Cripps, A.C., 2002, Nanoindentation, Springer, New York

Fisher, Jr., 2001, Method and apparatus for monitoring polishing pad wear during processing, US Patent 6,186,864 B1

Forsberg, M. 2005, Effect of process parameters on material removal rate in chemical mechanical polishing of Si (100), Microelectronic Engineering, v.77, pp.319-326

Frank, S., 2002, Portable hardness testing-principles and applications, 6° COTEQ – Salvador / BA – 19 a 21 de Agosto de 2002

Fu, G., Chandra, A., Guhua, S., Subhash, G., 2001, A plasticity-based model of material removal in chemical-mechanical polishing (CMP), IEEE Transaction: Semiconductor Manufacturing, v.14, n.4, pp.406-417

Fu, G.H., Chandra, A., 2002, A model for wafer scale variation of material removal rate in chemical mechanical polishing based on viscoelastic pad deformation, Journal of Electronic Materials, n.31, pp.1066–1073

Fu, G.H., Chandra, A., 2001, A model of Wafer Scale Variation of Removal Rate in Chemical Mechanical Polishing Based on Elastic Pad Deformation, Journal of Electronic Materials, v.30, n.4, pp.400-408(9)

Fu, G.H., Chandra, A., 2005, The relationship between wafer surface pressure and wafer backside loading in Chemical Mechanical Polishing, Thin Solid Films, v.474, pp.217-221

Fukami, T., Masumura, H., Suzuki, K., Kudo, H., 1997, Method of manufacturing semiconductor mirror wafers, European Patent Application EP96111698.5.

Gotkis, Y., Guha, S., 2001, Cu-CMP for dual damascene technology: Prestonian vs. non-Prestonian regimes of Cu removal, Journal of Electronic Materials, v.30, n.4, pp.396-399

Hinzen, H., Ripper, B., 1993, Precision grinding of semiconductor wafers, Solid State Technology, v.26, n.8, pp.53-56

Ho-Cheng, H., Liu, K.H., 2001, Method for monitoring polishing pad used in chemical-mechanical planarization process, US Patent 6,194,231 B1.

Jeng, Y.R., Huang, P.Y., 2005, A material removal rate model considering interfacial micro-contact wear behavior for chemical mechanical polishing, Journal of Tribology, v.127, pp.190-197

Jeong, H., Ohmori, Doy, T.K., Nakagawa, T., 1996, Integrated planarization technique with consistency in abrasive machining for advanced semiconductor, Proceedings of CIRP annals, v.45, n.1, pp.311-314

Jiang, M., Wood, N., Komanduri, R., 1998, On chemo-mechanical polishing (CMP) of silicon nitride (Si3N4) workmaterial with various abrasives, Wear, v.220, n.1, pp.59-71

Kato, T., Masumura, H., Okuni, S., Kudo, H., 1997, Method of manufacturing semiconductor wafers, European Patent Application EP0798405A2

Kaufman, F.B., Thompson, D.B., Broadie, R.E., Jaco, M.A., Guthrie, W.L., Pearsons, D.J., Small, M.B., 1991, Chemical mechanical polishing for fabricating patterned W metal features as chip interconnects, Journal of the Electrochemical Society, v.138, n.11, pp.3460-3464

Kim, H., Park, D.W., Hong, C.K., Han, W.S., Moon, J.T., 2003, The effect of pad properties on planarity in a CMP Process, Material Research Society Symposium Proceedings, 767, pp.F2.4.

Koizumi, S., Kato, K., 2000, New Method to Evaluate Stacked Polishing Pad for CMP, KTECH Research Corp.

Kulkarni, M., Desai, A., 2001, Silicon wafering process flow, US Patent 6,294,469.

Kumar, A., Sikder, A.K., Irfan, I.M., Belyaev, A., Ostapenko, S., Calves, M., Harmon, J.P., Anthony, J.M., 2001, Evaluation of mechanical and tribological behavior, and surface characteristics of CMP pads, Materials Research Society Symposium Proceedings, 671, pp.M1.8.1-M1.8.7.

Larsen, B., Liang, H., 1999, Probable role of abrasion in chemical-mechanical polishing of tungsten, Wear, v.233-235, pp.647-654

Lawing, A.S. 2002, Pad conditioning and pad surface characterization in oxide chemical mechanical polishing, Materials Research Society Symposium Proceedings. 732E, pp.I5.3.1-I5.3.6

Lee, S.M., Choi, W., Craciun, V., Jung, S.H. Singh, R.K., 2002, Electrochemical Measurements to Understand the Dynamics of the Chemically Modified Surface Layer Formation During Copper CMP, presented at Symposium I, Materials Research Society Meeting, San Francisco, April, Paper No. I4.11.

Li, I., Forsthoefel, K.M., Richardson, K.A., Obeng, Y.S., Easter, W.G., Maury, A., 2000, Dynamic Mechanical Analysis (DMA) of CMP pad materials, Material Research Society Symposium, 613, pp. E7.3.1-E7.3.10

Liang, H., Martin, J.M., Vacher, B., 2000, Chemical wear of Cu CMP, Materials Research Society Symposium Proceedings, 613, pp.E2.5.1-E2.5.5

Lin, Y.Y., Lo, S.P., 2004, A study of a finite element model fro the chemical mechanical polishing process, International Journal of Manufacturing Technology, v.23, pp.644-650

Liu, C.W., Dai, B.T., Tseng, W.T., Yeh, C.F., 1996, Modeling of the wear mechanism during chemical-mechanical polishing, Journal of the Electrochemical Society, v.143, n.2, pp.716-721

Liu, W.J., Pei Z.J., Xin X.J., 2002, Finite element analysis for grinding and lapping of wire-sawn silicon wafers, Journal Materials Processing Technology, v.129, n.1-3, pp.2-9

Lu, H., Obeng, Y., Richardson, K.A., 2003, Applicability of dynamic mechanical analysis for CMP polyurethane pad studies, Materials Characterization, v.49, pp.177-186

Luo, J., Dornfeld, D.A., 2001, Material removal mechanism in chemical mechanical polishing: Theory and modeling, IEEE Transactions on Semiconductor Manufacturing, v.14, n.2, pp.112-133

Machinski, S., 2001, Wear characterization of polyurethane chemical mechanical polishing pads, MS Thesis, University of Central Florida, FL, Summer

Mahajan, U., Bielmann, M., Singh, R.K., 1999, Dynamic Lateral Force Measurements during Chemical Mechanical Polishing of Silica, Electrochemical and Solid-State Letters, v.2, pp.80-82

Matsui, S., Horiuchi, T., 1991, Parallelism improvement of ground silicon wafers, Journal of Engineering for Industry, v.113, pp.25-28

Mcgrath, J., Davis., C., 2003 Combining a finite element model and a removal model to evaluate the effect of wafer and pad shape on removal in CMP, Electrochemical Society Proceedings, 21, pp.305-312

Meikle, S.G., 1997 Method and apparatus for measuring a change in the thickness of polishing pads used in chemical-mechanical planarization of semiconductor wafers, US Patent 5,609,718.

Meikle, S.G., 1998, Method and apparatus for measuring a change in the thickness of polishing pads used in chemical-mechanical planarization of semiconductor wafers, US Patent 5,801,066.

Meikle, S.G., Marty, L.F., 1997, Method for selectively reconditioning a polishing pad used in chemical-mechanical planarization of semiconductor wafers, US Patent 5,655,951.

Minamihaba, G., Yano, H., N. Kurashima, T., 2004, Improvement of Cu CMP by optimization of abrasive in slurry, Advanced Metallization Conference 2004, San Diego, CA, USA, October, pp. 589-593

Mullany, B., Byrne, G., 2003, The effect of slurry viscosity on chemical-mechanical polishing of silicon wafers, Jounal of Materials Processing Technology, v.132, pp.28-34

Murayama, T., 1978, Dynamic mechanical analysis of polymer material. New York: Elsevier Scientific Publication Corp.

Nagai, S., Fujishima, T., Sameshima, K., 2003, Nondestructive monitoring of CMP pad surface, Semiconductor Manufacturing, Proceedings of 2003 IEEE International Symposium, pp.343-346

Norwood, A., Van Hoy, G., 2006, Market share: semiconductor revenue, worldwide, 2005, Gartner Dataquest, available: http://www.gartner.com/DisplayDocument?doc_cd=139260

Oh, H.S., Lee, H.L., 2001, A comparative study between total thickness variance and site flatness of polished silicon wafer, Japanese Journal of Applied Physics, v.40, n.1, pp.5300-5301

Online Staff, Lithium Niobate: application note – single crystal substrates, 03/2001, available: http://crystaltechnology.com/docs/AppNotes_SingleCrystalSubstrates.pdf

Online Staff, High Precision Durometers, 8/23/2007, available: http://www.microphotonics.com/durometer.html

Online Staff, ABW1010 Tensile-Tester, 10/7/2007, available: http://www.ufdy.com/lab/images/ABW1010-tensile-tester-JPG.jpg

Online Staff, Nano-Indentation, 2006, available: http://www. cetr.com/nano-indentation.html

Online Staff, Pad deformation Tests on Cetr Tester, 12/28/2006, available: http://www.cetr.com/Brochures/Pad_Deformation_on_CETR%20_Tester.pdf

Online Staff, PadProbe for CMP Process Monitoring in the Fab, 2006, available: http://www.cetr.com/cetr_semiconductor.html

Online Staff, Portable hardness testing-principles and applications, 2002, available: http://www.aaende.org.ar/sitio/biblioteca/material/PDF/COTE246.PDF

Online Staff, Rockwell Hardness Testing of Plastics, 2007, available: http://www.matweb.com/reference/rockwell-hardness.asp

Online Staff, Shore (Durometer) Hardness Testing of Plastics, 2007, available: http://www.matweb.com/reference/shore-hardness.asp

Online Staff, Shore Test Method, 2007, available: http://www. instron.us/wa/applications/test_types/hardness/shore.aspx

Online Staff, Micromaterials Nanotest600, 4/20/2007, available: http://www. msm.cam.ac.uk/mechtest/machine%20pages/nanotest600.html

Online Staff, A history of industry innovation - ultraflat polished silicon wafers, 8/8/2001, available: http://www.memc.com/PDF_Files/Key_Topics_Articles/Ultraflat_wafers.pdf

Pei, Z.J., Strasbaugh, A., 2001, Fine grinding of silicon wafers, International Journal of Machine Tools and Manufacture, v.41, n.5, pp.659-672

Pei, Z.J., Billingsley, S.R., Miura, S., 1999, Grinding-induced subsurface cracks in silicon wafers, International Journal of Machine Tools and Manufacture, v.39, n.7, pp.1103-1116

Pei, Z.J., Fisher, G.R., Bhagavat, M., Kassir, S., 2005, A grinding-based manufacturing method for silicon wafers: an experimental investigation, International Journal of Machine Tools and Manufacture, v.45, n.10, pp.1140-1151

Preston, F., 1927, The theory and design of plate glass polishing machines, Society of Glass Technology, v.11, pp.214–256

Quick, M., Serda, J., 2001, Semiconductor Manufacturing technology, Prentice Hall

Ravi, K.V., 1999, Materials quality and materials cost – are they on a collision course?, Solid State Phenomena, v.69-70, pp.103-110

Runnels, S.R., Renteln, P., 1997, Modeling the effect of polish pad deformation on wafer surface stress distributions during chemical-mechanical polishing, Dielectric Science and Technology, VI, pp.110

Runnels, S.R., 1994, Featured-scale fluid-based erosion modeling for chemical-mechanical polishing, Journal of the Electrochemical Society, v.141, n.7, pp.1900-1905

Saka, N., Lai, J.Y., Chun, J.H., Suh, P.N., 2001, Mechanisms of the Chemical Mechanical Polishing (CMP) Process in Integrated Circuit Fabrication, Annals of the CIRP – Manufacturing Technology, v.50, n.1, pp.233-238

Sasaki, Y, Aoyama, H., Inasaki, I., Shibaya, H., Nippon Kikai Gakkai Ronbunshu, C Hen, 2002, Study on planarization of silicon-wafer by CMP, Transactions of the Japan Society of Mechanical Engineers, Part C, v.68, n.10, pp.3108-3114

Sasaki, Y., Aoyama, H., Inasaki, I., Miyairi, H., Shibaya, H., 1998, Proceedings of Silicon Machining, 1998 Spring Topieal Meeting, Carmel-by-the-sea, CA, USA, April 13-16, pp.92

Schlesing, W., Buhk, M., Osterhold, M., 2004, Dynamic mechanical analysis in coatings industry, Progress in Organic Coatings, v.49, pp.197-208

Singh, R.K., Bajaj, R., 2002, Advances in Chemical-mechanical planarization, MRS Bulletin (USA), v.27, n.10, pp.743-747

Sivaram, S., Tolles, R., Bath, H., Lee, E., Leggett, R., 1994, Chemical-mechanical polishing of interlevel dielectrics: Models for removal rate and planarity, SEMATECH, Austin, TX, Tech, Rep.

Srinivasa-Murthy, C., Wang, D., Beautoin, S.P., Bibby, T., Holland, K., Cale, T.S., 1997, Stress distribution in chemical–mechanical polishing, Thin Solid Films, v.308-309, pp.533

Steigerwald, J.M., Murarka, S.P., Gutmann, R.J., 1997, Chemical Mechanical Planarization of Microelectronic Materials, John Wiley & Sons, Inc., pp.66-67

Sun, W.P., Pei, Z.J., Fisher, G.R., 2004, Fine grinding of silicon wafers: a mathematical model for the wafer shape, International Journal of Machine Tools and Manufacture, v.44, n.7-8, pp.707-716

Sun, W.P., Pei, Z.J., Fisher, G.R., 2005, Fine grinding of silicon wafers: effects of chuck shape on grinding marks, International Journal of Machine Tools and Manufacture, v.45, n.6, pp.673-686

Szafraniak, I., Alexe, M., Gosele, U., 2003, Fabrication of metal-ferroelectric-silicon structure by layer transfer via wafer bonding, Special Issue on Feroic Domains and Mesosocopic Structures, Ferroelectrics, v.292, pp.23-28.

TA Instruments, 2001, Manual of DMA 2980: the instrument, New Castle (DE).

Tan, G., 2005, Study on the CMP mechanism and property of silicon wafer by nano-sized CeO2 abrasives, Zhongguo Jixie Gongcheng/China Mechanical Engineering, v.16, pp.341-343

Tonshoff, H.K., Hartmann, M., Klein, M., 1994, Analysis of grinding marks as a key to ultra-precision surfaces, Proceedings of the 3rd International Conference on Ultraprecision in Manufacturing Engineering, May, Aachen, Germany, pp.168-171

Tonshoff, H.K., Schmieden, W.V., Inasaki, I., Konig, W., Spur, G., 1990, Abrasive machining of silicon, CIRP Annals - Manufacturing Technology, v.39, n.2, pp.621-630

Totzke, D.G., 2000, MS Thesis, University of South Florida, Tampa, FL, May

Totzke, D.G., Belyaev, A., Moreno, W., Ostapenko, S., Tarasov, I., Easter, W., Maury, A., Crevasse, A., 2001, Non-destructive characterization of CMP pads using scanning ultrasonic transmission, AIP Conference Proceedings, January, v.550, n.1, pp.259-262

Tricard, M., Kassir, S., Herron, P., Pei, Z.J., 1998, New Abrasive Trends in Manufacturing of Silicon Wafers Silicon Machining Symposium, American Society for Precision Engineering, April, St. Louis, MO

Tsai, M.S., Lin, J.S. B.T., 1998, A novel two-step Al CMP process for overcoming pattern geometry effects, Proceedings of the International Society for Optical Engineering, v.3508, pp. 216-223

Tseng, W.T., Kang, L.C., Pan, W.C., Chin, J.H., Chen, P.Y., 1998, Distribution of Pressure and Its Effects on the Removal Rate during Chemical-Mechanical Polishing Process, Proceedings of the Third International Chemical-Mechanical Planarization for ULSI Multilevel Interconnection Conference, Tampa, FL, pp.87-94

Tseng, W.T., Wang, Y.L., 1997, Re-examination of pressure and speed dependences of removal rate during chemical mechanical polishing processes, Journal of the Electrochemical Society, v.44, n.2, pp.L15-L17

Tso, P.L., Teng, C.C., 2001, A study of the total thickness variation in the grinding of ultra-precision substrates, Journal of Materials Processing Technology, v.116, pp.182-188

Van Zant, P., 2000, Microchip Fabrication, McGraw-Hill, New York.

Van, B., Ogawa, T., 2006, Market share: silicon wafers, worldwide, 2005, Gartner Dataquest, available: http://www.gartner.com/DisplayDocument?doc_cd=141221

Vandamme, R., Xin, Y., Pei, Z.J., 2001, Method of processing semiconductor wafers, US Patent 6,114,245.

VanKranenburg, H., Woerlee, P., Nguyen, V., 2000, Dependency of dishing on polish time and slurry chemistry in Cu CMP, Microelectronic Engineering, v.50, n.1-4, pp.403-410

Wang, D., 1997, M.S. Thesis, Arizona State University, Phoenix, AZ

Wang, D., Lee, J., Holland, K., Bibby, T., Beaudoin, S., Cale, T.S., 1997, Journal of the Electrochemical Society, v.144, pp.1121

Wang, D., Zutchi, A., Bibby, T., Beaudoin, S.P., Cale, T.S., 1999, Effects of carrier film physical properties on W CMP, Thin Solid Films, v.345, n.2, pp.278-283

Warnock, J., 1991, A two-dimensional process model for chemi-mechanical polish planarization, Journal of the Electrochemical Society, v.138, n.8, pp.2398-2402

Xie, X.L., Boning, D., 2005, CMP at the wafer edge-Modeling the interaction between wafer edge geometry and polish performance, Material Research Society Symposium Proceeding, 867, pp.W5.5.1-W.5.5.11

Xin, Y.B. 1998, Modeling of Pad-wafer contact pressure distribution in chemical mechanical polishing, International Journal for Manufacturing Science and Technology, v.1, n.2, pp.20-34

Yu, T.K., Yu, C.C., Orlowski, M., 1993, A statistical polishing pad model for chemical-mechanical polishing, International Electron Devices Meeting, Proceedings of the IEEE, v.35, n.4, pp.1-4

Zantye P., Mudhivarthi, S., Sikder, A. K., Kumar, A., Ostapenko, S., Harmon, J., 2004, Investigation of Mechanical Integrity and its effect on Polishing for Novel Polyurethane Polishing Pad, Materials Research Society Symposium Proceeding, v.816, pp.K4.7.1-K4.7.6

Zantye, P.B., Mudhivarthi, S., Kumara, A., 2005, Metrology and characterization of application specific chemical mechanical polishing pads, Journal of Vacuum Science and Technology, v.23, n.5, pp.1392-1399

Zhou, L., Shimizu, J., Shinohara, K., Eda, H., 2003, Three-dimensional kinematical analyses for surface grinding of large scale substrate, Precision Engineering, v.27, n.2, pp.175-184

Zhuang, Y., King, D., Kido, T., Philipossian, A., 2005, Frictional and removal rate studies of silicon dioxide and silicon nitride CMP using novel cerium dioxide abrasive slurries, Japanese Journal of Applied Physics, Part: Regular Papers and Short Notes and Review Papers, v.44, n.1A, pp.30-33

Appendix B - List of Publications during Ph.D. Study

Zhang, X.H., Pei, Z.J., Fisher, G.R., 2006, A grinding–based manufacturing method for silicon wafers: generation mechanisms of central dimples on ground wafers, International Journal of Machine Tools and Manufacture, Vol. 46, No. 3-4, pp 397–403

Zhang, X.H., Pei, Z.J., Fisher, G.R., 2007, Measurement methods of pad properties for chemical mechanical polishing, CD–ROM Proceedings of the International Mechanical Engineering Congress and Exposition 2007 (IMECE 2007), Seattle, WA, November 11–15

Zhang, X.H., Pei, Z.J., Fisher, G.R., 2007, Finite element analysis of silicon wafer polishing: stress distributions and edge effects, Proceedings of International Symposium on Advances in Abrasive Technology (ISAAT2007), Dearborn, MI, September 25–28, pp. 193–199

Zhang, X.H., Pei, Z.J., Esayanur, M., Bowers, G.L., Fisher, G.R., 2007, An experimental investigation of material removal rate in polishing of silicon wafers, Transactions of the North American Manufacturing Research Institution of SME, Vol. 35, pp. 17–24

Zhang, X.H., Pei, Z.J., Xin, X.J., 2006, Soft-pad grinding of wire-sawn wafers: 2005 progress report, CD–ROM Proceedings of the 2006 NSF Design, Service and Manufacturing Grantees and Research Conference, St. Louis, MO, July 24–27

Zhang, X.H., Pei, Z.J., Fisher, G.R., 2005, Chemical mechanical polishing of silicon wafers: finite element analysis of wafer flatness, CD–ROM Proceedings of the International Mechanical Engineering Congress and Exposition 2005 (IMECE 2005), Orlando, FL, November 6–11

Zhang, X.H., Pei, Z.J., Xin, X.J., and Sun, X.K., 2005, "Three–dimensional FEA of soft–pad grinding of wire–sawn silicon wafers: effects of pad parameters," CD–ROM Proceedings of the 2005 NSF Design, Service and Manufacturing Grantees and Research Conference, Scottsdale, AZ, January 3–6