

D

C

B

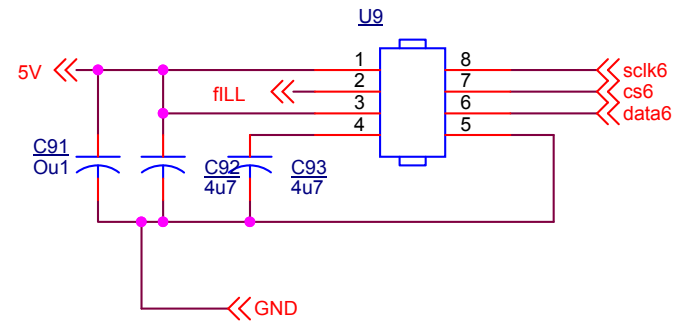
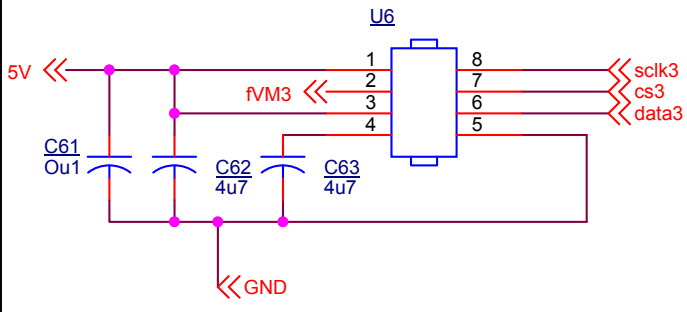
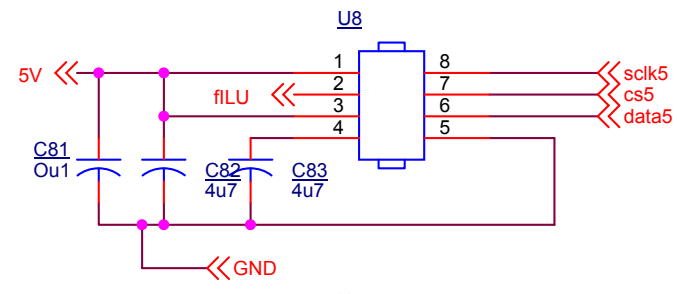
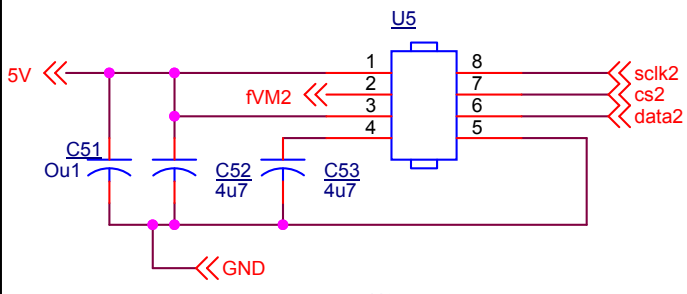
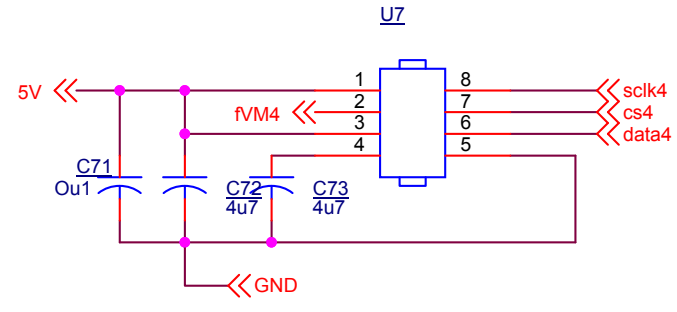
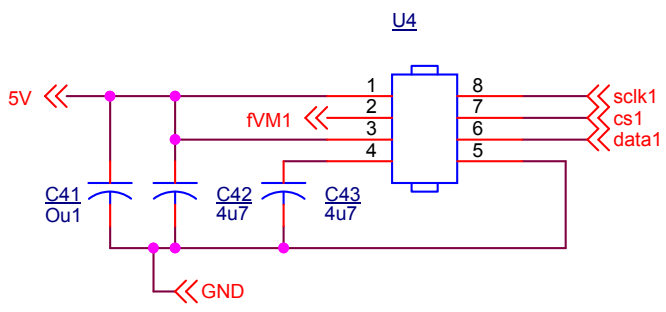
A

D

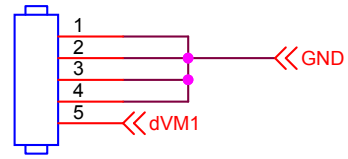
C

B

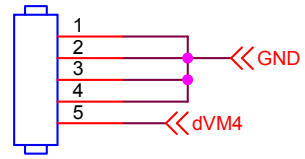
A



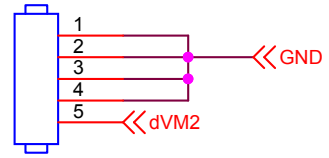
D4



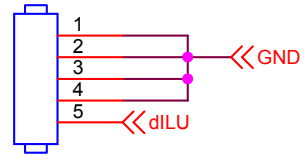
D7



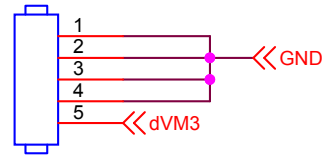
D5



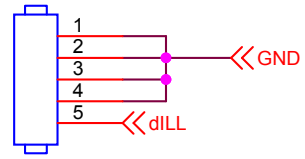
D8



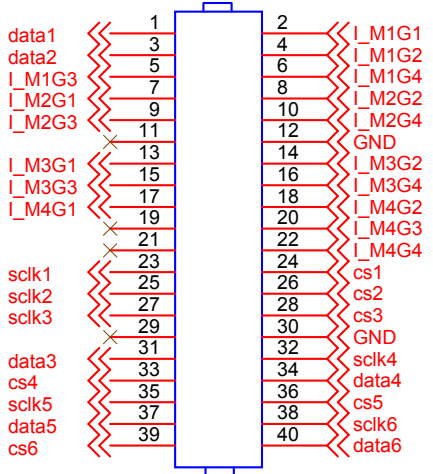
D6



D9

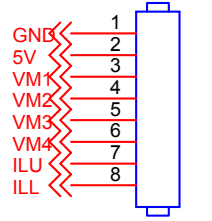


J1



HEADER 20X2

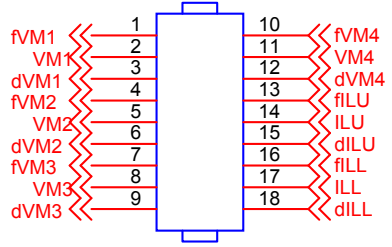
J2



8 pin Header

SW1

FPGA_OUTPUTS_1/4/7/10/13/16
 dSPACE_OUTPUTS_3/6/9/12/15/18



SW1