205

TECHNIQUES FOR TESTING A 15-BIT DATA ACQUISITION SYSTEM

by

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TECHNIQUES FOR TESTING A 15-BIT DATA ACQUISITION SYSTEM

Introduction

Recent advances in semiconductor technology have allowed higher performance and more complex integrated circuits to be manufactured; as a consequence, new methods of testing must be developed. This paper is primarily concerned with testing digital-to-analog and analog-to-digital converters.

Present converter technology makes it possible to obtain digital-to-analog converters (DACs) of up to 18-bits and analog-to-digital converters of up to 16-bits in both chip and modular form. Custom converters are being produced with 20-bit resolutions and above. In order to fully test a 12-bit converter, 4,096 possible output states must be examined; testing a 15-bit converter requires the examination of 32,768 states. By knowing the types of converter errors that are commonly encountered and where these errors occur, it is possible to significantly reduce the number of states tested. For high-resolution converters (12 bits and up), testing of at least 1,024 states is a minimum. Because of the large number of tests, automated techniques must be used to obtain accurate results and make efficient use of an engineer's time.

This thesis discusses techniques for testing a low-power data acquisition system (DAS). The system resolution is 15-bits, sampling frequency is 128 Hz, input range is ±5V, and the maximum input frequency is 45Hz. It is the purpose of this paper to

discuss some of the techniques which have been considered for testing the system, to present reasons why a particular technique may or may not be feasible, and to present the results of applying some of the techniques. Techniques which have been considered are those which lend themselves to an automated test, a test which is under computer control and which presents a numerical and/or a graphical result.

The 15-bit DAS uses a DAC generated reference voltage in a successive approximation analog-to-digital conversion technique. In Section 1, a method of testing a DAC's static linearity is presented together with the results of a static test. This static test is of considerable interest since the DAS cannot be expected to perform any better than its internal DAC. Should there be a need for dynamic testing the DAC, Section 2 presents a dynamic test method. Methods of static and dynamic testing ADCs are presented in Sections 3 and 4 respectively. Selected methods are applied to the 15-bit DAS and the results are presented.

In order not to constrict the flow of presenting the test methods, terminology relating to DACs and ADCs is presented in Appendices A and B respectively. The reader should refer to these for a definition and an explanation of terms used in the body of the report.

1. Static Testing Digital-to-Analog Converters

Static testing refers to performance evaluation under relatively slowly-varying conditions, conditions which may be considered dc. For a digital-to-analog converter (DAC), if the ~~the~~ amount of time allowed for the analog output voltage to settle is about an order of magnitude greater than its settling time (Appendix A), the operating conditions may be considered slowly-varying.

1.1 Direct Method

Static testing of a DAC is a relatively easy and straightforward task with the help of a digital voltmeter (DVM). The method to be described below will be referred to as the direct method. Figure 1 is a block diagram of a typical test setup. In this system, the DVM determines the accuracy of the test, therefore it should have an accuracy of at least 1/16 of the value of the least-significant bit of the DAC under test. There are DVMs available which are accurate to within 1 microvolt or less for input voltages up to 300 millivolts, 10 microvolts up to 3V, and 100 microvolts for input voltages up to 30 volts. The Hewlett-Packard 3478A digital multimeter is one example. Therefore, the span of the converter determines the accuracy of the test. For example, a DAC with a 10V span and 12-bits resolution would obtain 1/16 bit test accuracy using the 3478A. Converters of higher resolution but the same span would have to settle for less test accuracy. For high-resolution DACs, a DAC-

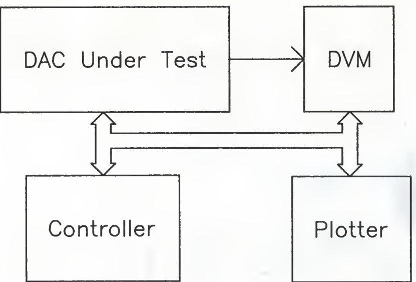


Figure 1. Block Diagram of Static Test Setup

to-DAC comparison technique using a higher resolution DAC would be necessary. This is discussed in Section 2. This is also the method used by the National Bureau of Standards (Section 3.4).

The following is an algorithm which can be used to obtain values for performance testing of the DAC under test.

1. Apply a digital input value.
2. Allow ample time for the output to settle.
3. Initiate the DVM to take a reading.
4. Record the result.
5. Goto 1 to acquire more data, Else goto 6.
6. Done.

The digital input can be applied manually using a toggle register, or automatically under computer control. Using the above algorithm, values can be obtained for integral linearity, differential linearity, offset error, and gain error:

linearity error,

$$IN(i) = \frac{V(i) - \left[\frac{i}{2^N-1}[V(2^N-1)-V(0)] + V(0)\right]}{LSB} \quad LSB,$$

differential linearity error,

$$DF(i) = \frac{[V(i)-V(i-1)]}{LSB} - 1 \quad LSB,$$

offset error,

$$V_{offset} = \frac{V_{zero}}{LSB} \quad LSB,$$

gain error,

$$G_{error} = \frac{FS - V(2^N-1)}{LSB} - 1 \quad LSB,$$

where:

$$LSB = \frac{V(2^N-1)-V(0)}{(2^N-1)},$$

i = The code number under test,

V(i) = Voltage of code i,

V_{zero} = Voltage for code zero,

= V(000...000) for straight binary coding,

= V(100...000) for offset binary coding,

N = Bits of resolution for DAC under test, and

FS = Ideal full scale range of the converter.

The above equations apply to a unipolar converter using straight binary coding. If a converter is operated in a bipolar mode, the coding is offset binary.

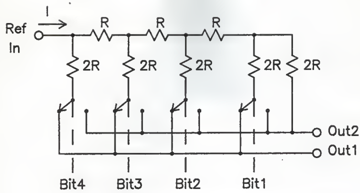
When testing digital-to-analog converters, it may not be feasible to test all possible codes. For example, a 14 bit DAC has 16,384 possible outputs and the time required to look at all outputs becomes quite long. A DVM of high accuracy usually employs an integrating technique to perform the analog-to-digital conversion. The reading rates are about 2 to 3 readings per second for 5 1/2 digit resolution. Therefore, the time required to make 16,384 readings is approximately 2 to 2 1/2 hours. This amount of time would be unreasonable in a production testing situation.

The testing time can be decreased by using a high-resolution analog-to-digital converter (ADC) using some other type of conversion technique in place of the DVM. However, the decrease of reliability and user friendliness of this approach is a major

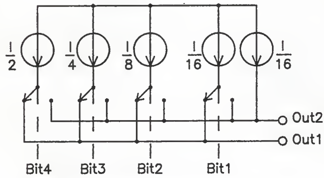
drawback. The accuracy of the readings will also decrease since the next most accurate technique which has an increase in speed is successive approximation. State-of-the-art in this technique is limited to about 16 bits, with many of these having only 14- or 15-bit linearity. Thus, with the requirement of having a resolution of 16 times the resolution of the converter under test, a 12-bit converter would be the highest resolution converter that could be evaluated.

Time of testing can be minimized by evaluating only a few of the codes. With this method, an educated guess is made as to which codes will have the largest errors. In most situations, these codes are the ones which make up major code transitions (Appendix A). Figure 2a shows an R-2R multiplying type DAC. This type of DAC has a characteristic such that the resistance seen by the reference is independent of the digital input code, it is always R. Also note the current entering each node is divided by two. This is because the resistance seen by any node looking to the right is R, or two resistors of value 2R in parallel. Thus the R-2R ladder can be modeled as current sources in parallel with magnitudes decreasing by a factor of two (Figure 2b). The switches of the R-2R ladder then serve to enable the current sources.

Nonlinearity in the DAC occurs when the resistance values are not perfectly matched. The most critical matching is required of the resistors which steer the most current. In this case the resistance matching of the most-significant bit output with the output of all the other current sources. Therefore, in going from code 0111 to 1000, the difference between the most-



a. 4-bit R-2R Ladder Network



b. Current Source Model

Figure 2. R-2R Multiplying Type DAC

significant current source and the sum of the rest of the sources must be matched accurately in order to insure an insignificant error contribution in the linearity. Hence, the largest linearity errors should be associated with the most major transitions.

Another philosophy of testing only major code transitions assumes that the errors associated with minor code changes repeat themselves as they reappear in stepping up the transfer characteristic. For example, the (differential) error associated with going from 0011 to 0100 would be the same as the error in going from 1011 to 1100.

1.2 Testing the Datel-Intersil DAC-HA14B

The data acquisition system to be tested uses a successive approximation technique for the analog-to-digital converter. The heart of this system is a 14-bit DAC, the Datel-Intersil DAC-HA14B. Using the method of Section 1.1, the static performance of this converter was evaluated. A block diagram of the test system is shown in Figure 3.

The control operations are performed by a Hewlett-Packard 9845B computer system. This consists of the 9845B computer, a 9885M Flexible Disc Drive, and a Hewlett-Packard 9872B Plotter. The system uses a Hewlett-Packard 3478A multimeter for dc measurements of the DACs analog output. The resolution of the 3478A is given in Table 1. The DVM was used in the 5 1/2 digit mode for maximum accuracy.

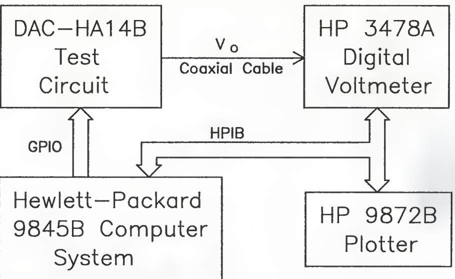


Figure 3. Setup for DAC–HA14B Tests

Table 1

HP 3478A DC Voltage Input Characteristics

Range	Resolution (digits) 5 1/2	4 1/2	3 1/2
30mV	100nV	1μV	10μV
300mV	1μV	10μV	100μV
3V	10μV	100μV	1mV
30V	100μV	1mV	10mV
300V	1mV	10mV	100mV

The full scale range of the DAC as it is being used in the data acquisition system is +5V. Therefore, the minimum resolution of the DVM is 100uV once the DAC output voltage passes 3V. In the static test circuit (Figure 4), the reference voltage of the DAC was lowered to 2.5V in order to lower the resolution of the test from 100μV to 10μV. This should have no effect on the results as long as the weight of the LSB is an order of magnitude greater than the noise present in the system. With a 2.5V reference, the LSB of the DAC is 153μV. Note that the resolution of the meter is 15.3 times greater than the resolution of the DAC under test. Thus, the results should be accurate to within 0.0654 LSBs.

A method which can be used to check the accuracy (consistency) of the test system is to take several readings of the same output voltage and find the standard deviation, SD, of the readings.

$$SD = \left[\frac{\sum V^2 - \frac{\left(\sum V\right)^2}{n}}{n-1} \right]^{1/2} \quad \text{Volts,}$$

where n is the number of readings taken.

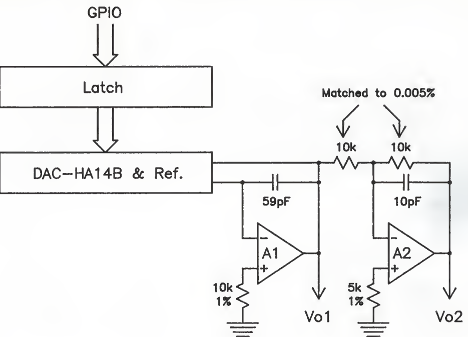


Figure 4. DAC-HA14B Static Test Circuit

For the DAC-HA14B system, 64 readings where taken and the standard deviation was calculated. This was performed for each of the major codes. The procedure was carried out under different laboratory conditions in order to evaluate the effect of the environment on the test results, Table 2. The tests were taken under three conditions: busy morning, busy afternoon, and quiet night. During the busy morning and busy afternoon conditions, other students were allowed to roam about the lab doing their work. This consisted of doing lab work at the bench and running other computer equipment. For example, one student was running a second 9845B directly adjacent to the system under test. The quiet night condition consisted of taking data in the evening (after 12:00 midnight) when no one was around and all lights were turned off. The closest possible noise source was a VAX 11/750 down the hall (the VAX 11/750 was also running during the daytime tests).

Table 2

Standard Deviation of Test Readings
Under Varying Laboratory Conditions

DAC Input (decimal)	Standard Deviation (μV) busy morning	busy afternoon	quiet night	3478A Resolution (μV)
1	0.377	0.456	0.419	0.1
2	0.669	0.563	0.382	0.1
4	0.615	0.449	0.576	0.1
8	0.468	0.469	0.325	0.1
16	0.535	0.794	0.514	0.1
32	0.443	0.669	0.507	0.1
64	0.566	0.526	0.396	0.1
128	0.449	0.577	0.509	0.1
256	0.626	0.794	0.695	1.0
512	1.11	1.09	1.22	1.0
1024	2.11	2.64	1.87	1.0
2048	5.12	4.78	5.02	10.0
4096	7.45	11.2	10.4	10.0
8192	15.9	28.5	22.9	10.0

The results of Table 2 show that the test system has an accuracy of about 30μVrms (the standard deviation is the same as an rms value) maximum, or about 0.197 LSB. The results also show that the period of the day in which data is taken is not of major concern. As a matter of fact, the night time results show greater error than some of the morning results. This may not be the case in general, since the tests were only run once, but it still is an interesting result. Running the above tests several more times and finding the average would give a better indication.

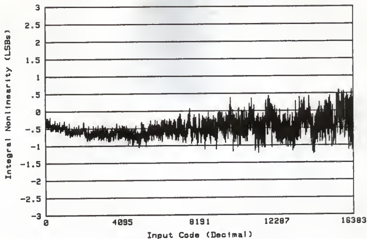
Using the static test procedure presented earlier, the DAC-HA14B was evaluated for integral linearity and differential linearity errors. The results of these tests are presented in Figures 5, 6, 7. In order to get a better indication of the performance of the DAC-HA14B, three different converters were evaluated, each having a different lot number. These will be referred to as DAC#1, DAC#2, and DAC#3 (Table 3).

Table 3

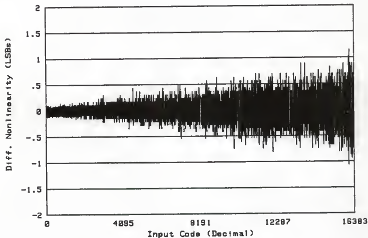
Lot Numbers of DACs Tested

DAC Designation	Lot Number
DAC#1	8025
DAC#2	8441
DAC#3	8240

Figures 5a, 6a, and 7a illustrate the integral nonlinearity of the three DACs. DAC#1 has an integral nonlinearity of +0.65 LSB and -1.25 LSB maximum. DAC#2 has an integral nonlinearity of +0.75 and -2.0 LSB maximum. The integral nonlinearity of DAC#3 is +1.0 and greater than -2.0 LSB maximum. Note the difference

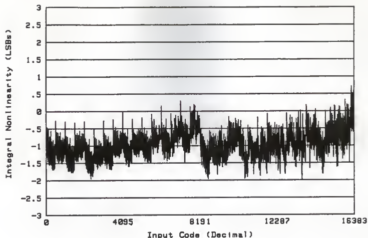


a. Integral Nonlinearity as a Function of Input Code

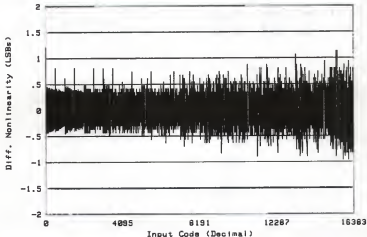


b. Diff. Nonlinearity as a Function of Input Code

Figure 5. Nonlinearity Results for DAC#1

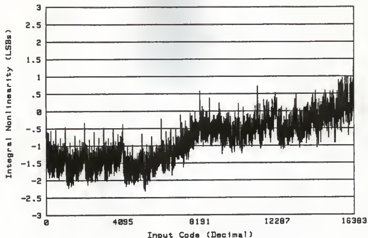


a. Integral Nonlinearity as a Function of Input Code

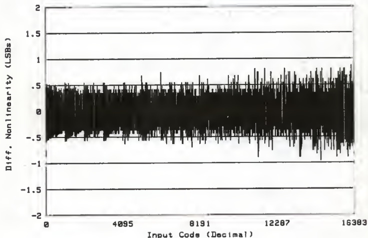


b. Diff. Nonlinearity as a Function of Input Code

Figure 6. Nonlinearity Results for DAC#2



a. Integral Nonlinearity as a Function of Input Code



b. Diff. Nonlinearity as a Function of Input Code

Figure 7. Nonlinearity Results for DAC#3

between the transfer characteristics in comparing the three DACs. This shows that it is a good idea to check more than one converter, especially ones with different lot numbers. Also note the abrupt changes in the characteristic as it goes through major code changes, Figure 6a is the best example. This supports the philosophy of checking major code changes for a quick check of the converter's performance, as stated in Section 1.1.

Datel-Intersil specifies the DAC-HA14B to have a maximum (@ 25°C) integral nonlinearity of ±1 LSB. All three of the DACs tested failed to meet this specification.

Figures 5b, 6b, and 7b illustrate the differential nonlinearity of the three DACs. DAC#1 has a differential linearity error of ±1.25 LSB maximum. However, these maximums occur at the very end of the transfer characteristic. The error is ±1.0 LSB over most of the transfer characteristic. DAC#2 has a differential nonlinearity error of +1.25 and -1.0 LSB maximum. Note the large error associated with the major transition from 255 to 256 and that it is repeated at integer multiples. Also note the difference in the transfer characteristic as compared with DAC#1. This is in agreement with the integral nonlinearity results. DAC#3's differential nonlinearity is within ±1 LSB over the entire operating range. DAC#3's transfer characteristic is similar to DAC#2's.

Datel-Intersil specifies the DAC-HA14B to have a typical differential linearity error of ±1/2 LSB and a maximum error of ±1 LSB. All three of the DACs fall quite close to the maximum specification. One should keep in mind that some of the specifications published are not actually verified by testing,

but are merely best guesses.[1] Therefore, if a certain specification is critical in a design, testing the device on your own is highly advisable.

The 15-bit data acquisition system uses two DAC followers to generate a positive and negative voltage output for use in bipolar conversion. Figure 8 is a plot of the difference between these two outputs as the converter is stepped through its operating range. This error is an indication of how well the gain resistors of the second follower are matched (Figure 4). The data shown were taken using DAC#1. Since the difference error is a function of the gain resistors, it is not necessary to evaluate it using different DACs. Theory dictates that as the magnitude of the output voltage increases, the voltage difference between the outputs of the two amplifiers should increase. Figure 8 shows that the resistors are matched well enough as to create an error of less than 1 LSB over the entire operating range.

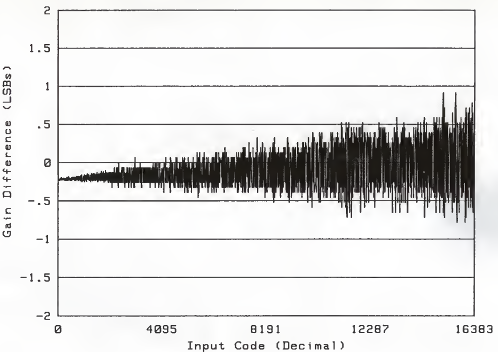


Figure 8. Gain Difference of Followers

2. Dynamic Testing Digital-to-Analog Converters

Dynamic testing refers to performance evaluation by subjecting the converter to rapidly changing conditions. For a digital-to-analog converter (DAC), rapidly changing conditions would correspond to changing input values at a rate which is not considered static, i.e. rates which are greater than dc (see Section 1.1). Dynamic testing subjects a converter to conditions which are more demanding than static testing, and hence gives a better indication of how well it will perform in its intended application. Note that since there are many different rates at which the converter can be tested, a parameter specifying performance must be associated with the operating conditions (e.g. the rate) to which it is to be subjected in order for the parameter to have any meaning. When performing dynamic testing, digital voltmeters like the one used in Section 1.2 can no longer be used because their reading rates are much slower than the conversion rates to which the DAC is being subjected. Therefore a different method needs to be used.

The method to be described uses a DAC of superior performance to the converter under test as a comparison reference (Figure 9). The reference DAC will serve the purpose of approximating the straight line transfer function of an ideal digital-to-analog converter. Therefore by comparing the DAC under test to the reference DAC, values for integral nonlinearity and differential nonlinearity can be calculated. Both DACs must have the same

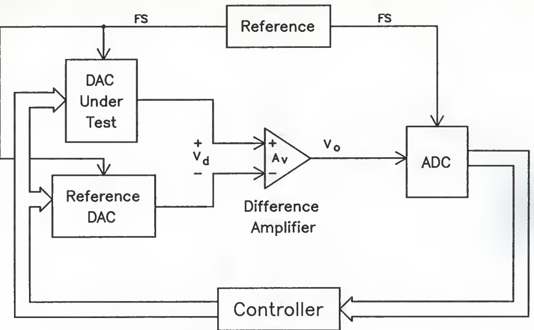


Figure 9. Block Diagram of DAC Dynamic Test Setup

output voltage range, e.g. ±5V. A DAC of superior performance refers to one which has a known dynamic performance of at least two bits greater resolution than the DAC under test for the rate being tested. As will be seen, this is the major limitation of this method as it contributes the most error to the test system. Note that this method may also be used for static testing. In a static test the input would not change rapidly compared to the DAC's settling time (see introductory paragraph of Section 1.1).

Using a controller, a specific digital value is input to the DAC under test and the reference DAC simultaneously. The difference amplifier subtracts the magnitude of the two DACs and amplifies the difference voltage (the linearity error). The amplified difference voltage is then applied to a fast analog-to-digital converter, probably a flash type for maximum conversion rates. The digital output of the ADC represents the deviation of the DAC-under-test transfer characteristic from that of the theoretical straight line. It is then used to calculate the integral and differential nonlinearity of the converter.

The major source of error with this technique lies in the use of a reference DAC to approximate the theoretical straight line transfer characteristic of an ideal DAC. For example, if the reference DAC has an accuracy of M bits and the DAC under test has a resolution of N bits, then the uncertainty in the test contributed by the reference DAC alone is

$$U_{ref} = \frac{1}{2^{M-N}} \text{ LSB}.$$

For example, a reference DAC having an accuracy of 2-bits more than the converter being tested contributes an uncertainty in the test result of 0.25 least-significant bit (LSB).

The gain of the difference amplifier depends on the maximum difference voltage (or nonlinearity) in LSBs the test system is to detect. For example, if the DAC under test has a resolution of N-bits, its LSB is

$$LSB = \frac{FS}{2^N},$$

where FS is the full-scale output voltage. If the system is to detect a nonlinearity of K LSBs, then the gain, A_V, of the amplifier must be set to amplify this to FS:

$$FS = K \frac{FS}{2^N} A_V.$$

Therefore

$$A_V = \frac{2^N}{K}.$$

For example, if a 14-bit converter is being tested and the assumed maximum error is 4-bits, then the gain of the amplifier is

$$A_V = \frac{2^{14}}{4},$$

or

$$A_V = 2,048.$$

The difference amplifier also contributes uncertainty to the test accuracy by way of its gain and offset errors (it will be assumed that the bandwidth of the amplifier is greater than that of the test system and it is allowed sufficient time to settle). If the difference voltage between the DAC under test and the

reference DAC is V_d, the equivalent input offset voltage (includes all error sources which are referred back to the amplifiers input) of the amplifier is V_{os}, and the gain error of the amplifier is G, then the amplifier output voltage is given by

$$V_o = A_v[(1+G)(V_d+V_{os})] \quad \text{Volts.}$$

The error which is introduced by the amplifier is

$$V_{error} = A_v(G)(V_d) + A_v(1+G)(V_{os}).$$

Normally, provisions are made to adjust V_{os} to zero, therefore the error voltage is

$$V_{error} = A_v(G)(V_d).$$

Since the output of the difference amplifier is being applied to the input of an ADC, the error voltage of the amplifier must be significantly less than the resolution of the ADC (somewhere on the order of two bits better) so that the accuracy of the test is not affected. For example, if an ADC with J-bits of accuracy is being used, a gain error of at least J+2-bits (or $(J+2)^{-1}$x100 percent, Appendix C) would be acceptable.

$$U_{amp} = \frac{K}{2^{J+2}} \text{ LSB.}$$

If a 7-bit ADC is being used, a gain error of 0.195% would suffice. This is not hard to accomplish, since resistor networks are available with ratio matching to 0.005%. The DAC system of Section 1.2 used such a resistor network. If the system is to detect a maximum of 4 LSBs, the amplifier contributes a test

uncertainty of

$$U_{amp} = \frac{4}{2^9} \text{ LSB}$$
$$= 0.00781 \text{ LSB}.$$

The resolution of the ADC determines the resolution of the nonlinearity estimate, i.e. the accuracy of the reading in fractions of an LSB. If the maximum difference voltage of the difference amplifier represents K-bits of the DAC under test, and the ADC has a resolution of J-bits then the resolution of the nonlinearity estimate is

$$R_{test} = \frac{K}{2^J} \text{ LSB}.$$

For example, if the ADC has a accuracy of 7-bits, and the maximum assumed difference voltage of the DAC under test is 4-bits, then the resolution of the test is

$$R_{test} = \frac{4}{2^7} = 0.03125 \text{ LSB}.$$

Using the above error analysis, a system composed of a reference DAC with an accuracy of 16-bits, a difference amplifier with a gain error of 0.195%, and a flash ADC with an accuracy of 7-bits is designed to detect the accuracy of a a DAC with 14-bits of resolution to 4 LSBs. The total uncertainty in the system estimate would be

$$\begin{aligned} U_{tot} &= U_{ref} + U_{amp} + R_{test} \\ &= 0.25 + 0.00781 + 0.03125 \quad \text{LSB} \\ &= 0.28906 \quad \text{LSB}. \end{aligned}$$

As stated previously, the reference DAC is the major component of uncertainty in the system.

3. Static Testing Analog-to-Digital Converters

Static testing refers to performance evaluation under dc input conditions. Testing ADCs (Analog-to-Digital Converters) is more difficult than testing DACs (Digital-to-Analog Converters). This is due to the fact that an ADC has as its input a continuous range of analog values. The purpose of the ADC is to estimate a sample of this continuous range to within a specified error; a process known as quantization (Appendix B). An N-bit ADC divides this into 2^N divisions. Thus the ADC has an inherent error, its output can only specify the input to an accuracy set by the quantization step. When testing an ADC it is necessary to determine the analog values which correspond to the transition points of a quantization step. Ideally this would require testing with an infinite number of analog input values, an impossible task. One method used to overcome this problem is to partition the continuous analog range into levels much smaller than the the quantization step of the ADC, providing an indication of the transition levels but only to a degree specified by the analog partition. This process is further complicated by the presence of noise, which introduces another source of error in the determination of the transition voltage. The following sections describe some methods used in the evaluation of ADCs.

3.1 DAC-to-ADC Loop Method

Perhaps the simplest method is the DAC-to-ADC loop method. A diagram of the test setup is shown in Figure 10. The DAC is used as a precision voltage reference, the extent of the precision specifying the degree of accuracy to which the ADC can be evaluated. Thus, this is the major limitation of the method when testing high resolution ADCs. For example, commercially available DACs have accuracies up to about 18-bits. Therefore, if a test accuracy of 1/16 bit is desired, 14-bits is the maximum resolution ADC which can be tested. If a higher resolution device is to be tested, either the test resolution can be decreased or a custom DAC of higher resolution can be developed.

A problem with this method is that the accuracy of the DAC must be evaluated before the ADC can be tested. Taking a manufacturer's specifications from the data sheet is unadvisable since these values are most likely based on tests performed during development of the device, and possibly a random sampling of devices during production. However, a static test of a DAC is relatively simple (Section 1.1), hence evaluating the DAC should not be much of a problem.

There are three procedures which can be performed using the DAC-to-ADC loop method.

3.1.1 Procedure 1 The simplest, but not very informative procedure, consists of a direct comparison of the DAC input with the ADC output. If the DAC is of higher resolution than the ADC, only the top N bits (N being the resolution of the ADC) of the DAC are used with the lower bits being set to zero. Below is the test algorithm.

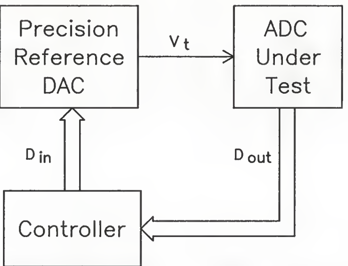


Figure 10. Block Diagram of DAC–to–ADC Loop Method

1. Adjust the zero offset of the ADC so that a code of 00...00 occurs for the DAC output voltage corresponding to 00...00 input.
2. Adjust the gain of the ADC so that a code of 11...11 occurs for the DAC output voltage corresponding to 11...11 input.

(note: The above digital values are straight binary for a unipolar converter, offset binary for a bipolar converter.)

3. Set the DAC input code of interest.
4. Record the ADC output code.
5. Calculate the difference between the DAC input code and the ADC output code. This is the nonlinearity.
6. Goto 3 to acquire more data, Else goto 7.
7. End.

The amount of information extracted from this procedure is at a minimum since it does not give the precise location of each analog transition voltage. This algorithm estimates the nonlinearity to a degree of only $\pm 1/2$ least-significant bit (LSB) assuming a perfect DAC. Normally it is desirable to determine nonlinearity to a greater degree of accuracy than this. However, in a noncritical application requiring a quick check of linearity this method would suffice. The speed of the test can be increased by checking only major codes or by setting the major codes in succession, hence requiring the test of only N points.

3.1.2 Procedure 2 An alternative to the above procedure is to step the DAC through all of its possible values and record the corresponding ADC output. This procedure can be used to determine the transition points of the ADC transfer

characteristic (to within the resolution of the DAC). From this data, differential and integral linearity errors can be calculated. The following is the algorithm used.

1. Adjust the zero offset of the ADC so that a code of 00...00 occurs for the DAC output voltage corresponding to 00...00 input.
2. Adjust the gain of the ADC so that a code of 11...11 occurs for the DAC output voltage corresponding to 11...11 input.

(note: The above digital values are straight binary for a unipolar converter, offset binary for a bipolar converter.)

3. Set the DAC input code, D_{in}, to 00...00; Initialize an array V_t to zero.
4. Record the ADC output code, D_{out};

   $D_{out1} = D_{out}$.
5. Increment D_{in}.
6. Read D_{out}.

   If $D_{out} = D_{out1}$ then goto 7.

   If $D_{out} = D_{out1}+1$ then transition voltage has been detected:

   $V_t(D_{out}) = (D_{in})(Lsb_dac)$,

   Record V_t and D_{out},

   $D_{out1} = D_{out}$.

   If $D_{out} > D_{out1}+1$ then missing codes have been found, $D_{out1}+1$ to $D_{out}-1$:

   $D_{out1} = D_{out}$.

7. Done?

No, goto 5;

Yes, goto 8.

8. Calculate the differential nonlinearity:

$$DF(i) = \frac{V_t(i+1)-V_t(i)}{LSB} - 1 \quad LSB \quad i=1,\ldots,2^N-1.$$

9. Calculate the integral nonlinearity:

$$IN(i) = \frac{V_t(i)-[V_t(1)+(i-1)(LSB)]}{LSB} \quad LSB \quad i=1,\ldots,2^N.$$

where:

$$LSB = \frac{V_t(2^N-1)-V_t(1)}{2^N-2},$$

D_{in} is the input code of the DAC,

D_{out1} is the previous ADC output code,

D_{out} is the present ADC output code,

V_t is an array containing the transition voltages for the ADC output codes (Note that this is the transition voltage to a code 1 greater than the code being tested),

Lsb_dac is the value of the DAC's LSB, and

N is the resolution of the converter.

A problem with this procedure is that for high resolution systems, noise inhibits the exact determination of the transition points. For example, if the noise of the system consisted of 1/16 LSB, and the resolution of the DAC is 1/8 LSB, the uncertainty in the measurement would be 3/16 bit. A method which can be used to improve the estimate is to take several readings of the ADC corresponding to a single DAC input and find the standard deviation, if it meets a certain limit specification

(e.g. less than 0.1) then the transition can be assumed to have taken place. However, this will significantly increase the test time for high-resolution converters and may complicate the determination of missing codes.

3.1.3 Procedure 3 A third procedure which can be performed using the test setup of Figure 9 will be referred to as the histogram procedure. This is similar to the one described above except that the purpose is not to search for the transition voltages, but to estimate them using statistics. The differential nonlinearity is found by counting the number of times a code occurs, normalizing with the number of times the code is expected to occur, and then subtracting 1. For example, if a 15-bit ADC is under test, and 10 readings are taken for each possible input code of an 18-bit DAC, the number of expected occurrences, ENO, for each ADC code is

$$\text{ENO} = \frac{(10)(2^{18})}{2^{15}} = 80.$$

If 30 occurrences actually occur, the differential nonlinearity is

$$\text{DF} = \frac{30}{80} - 1 = -0.625 \text{ LSB}.$$

Note that missing codes contain a count of zero in their bins, hence their differential nonlinearity is -1.

Again the resolution of this test is limited by the accuracy of the DAC. Below is an algorithm used for this procedure.

1. Adjust the zero offset of the ADC so that a code of 00...00 occurs for the DAC output voltage corresponding to 00...00 input.

2. Adjust the gain of the ADC so that a code of 11...11 occurs for the DAC output voltage corresponding to 11...11 input.

(note: The above digital values are straight binary for a unipolar converter, offset binary for a bipolar converter.)

3. Initialize a counting array, A, to zero.

4. Set the DAC input code to 00...00.

5. Read the ADC output, D_{out}:

   $A(D_{out}) = A(D_{out})+1.$

6. Need more readings?

   Yes, goto 5;

   No, goto 7.

7. Done?

   Yes, goto 8;

   No, Increment the DAC input, goto 5.

8. Divide each element of A by the expected number of occurrences and subtract one. The result is an estimate of differential nonlinearity:

$$DF(i) = \frac{A(i)}{ENO} - 1 \quad \text{LSB} \quad i=1,\ldots,2^N.$$

9. To find integral nonlinearity:

$$IN(i) = \frac{\left[\sum_{j=1}^{i} A(j)\right] - A(1)}{ENO} - (i-1) \quad \text{LSB} \quad i=1,\ldots,2^N,$$

where:

D_{out} is the ADC output code,

A is a counting array of length 2^N,

N is the resolution of the ADC,

ENO is the expected number of occurrences for each code.

The above equation for calculating integral nonlinearity assumes that the gain has been adjusted to zero. If there is not a gain adjustment available for the ADC, the gain adjustment of the DAC can be used to null it out. If neither is available, the slope of the ideal transfer characteristic can be be altered from its ideal value of one by calculating the slope of the line between the first and last codes (not that this is the end point definition described in Appendix B). Usually the first and last codes do not contain an accurate count in their bins. They either have too many or not enough since they accumulate counts for inputs outside the converters span. Therefore, the actual slope of the transfer characteristic is calculated using the second and the second from the last codes.

The expected number of occurrences should also be altered. It should be the number of counts in all codes, except the first and last, divided by two less than the number of possible output codes.

$$ENO' = \frac{\sum_{i=2}^{2^N-1} A(i)}{2^N-2}$$

$$\text{slope} = \frac{\sum_{i=2}^{2^N-2} A(i)}{(ENO')(2^N-2)} .$$

The differential and integral nonlinearity equations become

$$DF(i) = \frac{A(i)}{ENO'} - 1 \quad \text{LSB} \quad i=1,\ldots,2^N,$$

$$IN(i) = \frac{\left[\sum_{j=1}^{i} A(j)\right] - A(1)}{ENO'} - (i-1)(\text{slope}) \quad \text{LSB} \quad i=1,\ldots,2^N.$$

The histogram procedure has an advantage over the second procedure in that the noise in the system, which makes it difficult to find transition voltages, is averaged out if enough data points are taken. Therefore more accurate results are obtained.

3.2 Servo-Loop Integrating Method

The servo-loop integrating method can be used to evaluate the performance of an ADC without the use of a reference DAC. This method uses an operational amplifier based integrating amplifier in conjunction with a digital comparator and an averaging voltmeter to search for the transition voltages of the ADC under test. Though this method does not require a reference DAC, it does require another ADC (the voltmeter) of higher accuracy than itself. This is not a problem however since digital voltmeters (DVMs) with 19- and 20-bit accuracy are available. A block diagram of the test setup is shown in Figure 11. The ADC under test, the digital comparator, and the integrator form a servo-loop.

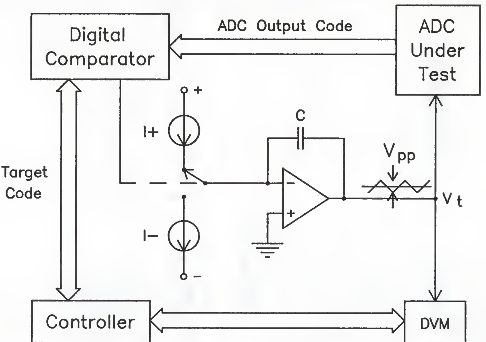


Figure 11. Block Diagram of Servo–Loop Integrating Method

A computer serves as the controller. It outputs a digital word, the target code, which is compared to the output of the ADC after each conversion. The output of the digital comparator controls the slope direction of the integrator. If the target code is greater than the ADC output code, the integrator slopes in the positive direction. If the target code is less than the ADC output code, the integrator slopes in the negative direction. After a few conversion periods, the integrator output approaches the transition voltage of the target code (the transition voltage being the voltage which causes a transition from the code 1 less than the target code to the target code), and then locks on to it. The locked state is reached when the output of the ADC toggles between the target code and the code one less than the target code.

When in the locked state, the integrator output will ideally be a triangle wave centered about the transition voltage. The peak-to-peak voltage of the integrator output is given by:

$$V_{pp} = -(I/C)(\text{delta_t})$$

where

I = integrator input current,

C = integrator capacitance, and

delta_t = conversion interval.

The voltmeter then acquires the transition voltage by averaging the integrator output. The voltage V_{pp} specifies the accuracy of the test, a typical value being 1/16 LSB.

The locked loop condition is sensed by taking successive readings with the voltmeter. When the voltage difference between successive DVM readings is smaller than a predetermined threshold

given by Vpp/delta_t and the time period separating the voltmeter readings, the system is considered locked.

After finding all transition voltages, the integral and differential nonlinearity can be calculated.

$$DF(i) = \frac{V_t(i+1)-V_t(i)}{LSB} - 1 \quad LSB \quad i=1,\ldots,2^N-1,$$

$$IN(i) = \frac{V_t(i)-[V_t(1)+(i-1)(LSB)]}{LSB} \quad LSB \quad i=1,\ldots,2^N,$$

where

$$LSB = \frac{V_t(2^N-1)-V_t(1)}{2^N-2},$$

V_t is an array containing the ADC transition voltage for the code specified by i,

N is the resolution of the converter.

The digital comparator is also used to sense missing codes. Once in the locked state, the ADC output code should never exceed the the target code, since the system toggles between the target code and the target code minus one. If after sufficient tracking time has been allowed the ADC output is sensed as being greater than the target code, the system is toggling between the target code plus one and the target code minus one and hence the target code is missing.

This system has limitations with converters of high-resolution and relatively slow sample rate. For example, suppose that a 15-bit ADC having a span of ±5V is to be tested to an accuracy of 1/16 LSB. The system parameters are as follows:

$$Vpp = \frac{10}{(2^{15})(16)} = 19(10^{-6}) \text{ Volts},$$

$$delta_t = \frac{1}{128} = 7.8125mS$$

and if C=5µF

$$I = \frac{(V_{pp})(C)}{delta_t} = 12nA.$$

The integrator current would be difficult to realize, and even more difficult to maintain. The current could be increased with a larger capacitor, but 5µF is about the maximum capacitance of a high quality capacitor. Although the above system is rather unique with its high resolution and slow sample rate, it is the problem faced in testing the 15-bit data acquisition system. In general though, a high-resolution system should have a conversion interval of less than 100µS to make this technique feasible.

3.3 Testing the 15-bit Data Acquisition System

The histogram procedure of the DAC-to-ADC loop method described in Section 3.1.3 was used to evaluate the static performance of the 15-bit data acquisition system. This procedure was chosen because of its ease of use, its accuracy, and its inherent property of averaging out noise in the determination of transition voltages. A block diagram of the test setup is shown in Figure 12.

The controller is a Hewlett-Packard 9845B desktop computer. The digital-to-analog converter is a system developed using the Analog Devices DAC1146 18-bit digital-to-analog converter. This is a modular converter with 16-bit (±1/2 bit with respect to 16-

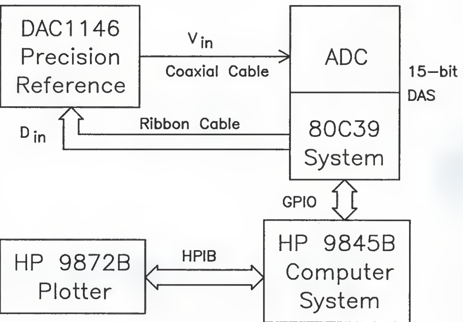


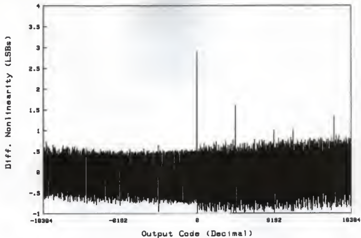
Figure 12. Setup for 15–bit DAS Static Tests

bits) accuracy specifications. The system was tested and the accuracy was verified to be within 16-bits.[2] It should be noted that the maximum differential nonlinearities were found to occur for only a fraction of the possible number of codes available and that 18-bit differential linearity is realized for approximately 99% of the output voltage levels. However, the test accuracy will be specified as ±1/4 LSB (±1/2 LSB with respect to 16 bits).

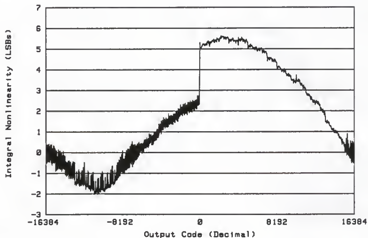
A total of 2,621,440 readings were taken to construct the histogram. This is 10 times the possible number of DAC input codes, or 80 times the possible number of ADC output codes. The test was initiated with the DAC at minus full-scale and the voltage was increased one DAC quantization level at a time until full-scale was reached.

The ADC system is a successive approximation type and uses the Datel-Intersil DAC-HA14B DAC. A test was run using each of the three DACs tested in Section 1.2. The differential nonlinearity results are shown in Figures 13a, 14a, and 15a. It should be noted that these plots do not show the differential nonlinearity for each possible code. Since there are 32,767 (-16,383 to +16,383) possible output codes, it is difficult and time consuming to plot every data point. Instead the data files were thinned to 2,048 of the maximum and minimum points. A search was performed which took 64 point blocks, keeping the minimum and maximum points in that block and throwing the rest away. Thus all of the interesting information is retained but yet there is 1/64 less data to plot.

For all three cases, the majority of the codes lie within the ±1 LSB test limit. Note that there is a large differential

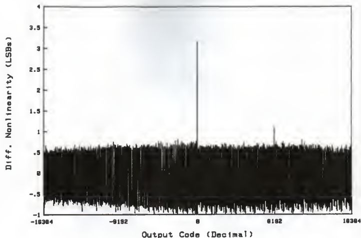


a. Diff. Nonlinearity as a Function of Output Code

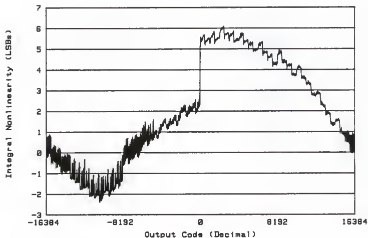


b. Integral Nonlinearity as a Function of Output Code

Figure 13. Static Nonlinearity Results using DAC#1

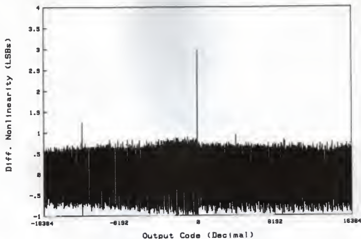


a. Diff. Nonlinearity as a Function of Output Code

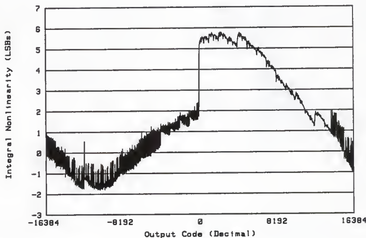


b. Integral Nonlinearity as a Function of Output Code

Figure 14. Static Nonlinearity Results using DAC#2



a. Diff. Nonlinearity as a Function of Output Code



b. Integral Nonlinearity as a Function of Output Code

Figure 15. Static Nonlinearity Results using DAC#3

nonlinearity found at the zero-crossing point. The plots also indicate missing codes, or differential nonlinearities of less than -1 LSB. A search of the data files found the following missing codes.

Table 4

Missing Codes for Static Histogram Tests

Figure	Number of Missing Codes
13a	5
14a	8
15a	9

Remember that the accuracy of the input reference is ±1/4 LSB, thus a missing code as indicated above may exist but its quantization step is less than 1/4 LSB. Overall though, the results show that the system obtains 14.5-bit differential linearity (±1 bit with respect to 15-bits), except at zero-crossing.

Integral nonlinearity for the same three cases mentioned above is shown in Figures 13b, 14b, and 15b. Again the data reduction process was performed for plotting purposes. All three plots carry similar information. The integral nonlinearity seems to fall in the range of -2 LSB to +6 LSB. The major contributor to the nonlinearity is the large differential nonlinearity associated with zero-crossing. If this can be corrected, the nonlinearity would probably be restricted to ±2 LSBs.

In conclusion, the 15-bit data acquisition system was found to have 14.5-bit differential linearity and about 12.5-bit integral linearity. The integral linearity can be increased to 14-bits by correcting the large differential nonlinearity at

zero-crossing.

3.4 The National Bureau of Standards Calibration Service

A calibration service based on an automated test facility has been developed at the National Bureau of Standards (NBS) for measuring the static transfer characteristics of high-performance ADCs and DACs. This service specifically addresses the measurement of static converter errors. A capability for making dynamic measurements is currently under development.[3]

The calibration service is particularly intended for the following customer applications:

1. Testing of high resolution converters for use in unique, highly demanding applications.
2. Satisfying traceability requirements imposed by State, Federal or military contracts.
3. Independently verifying the test methods of converter manufacturers through the use of transfer standards.
4. Verifying incoming inspection tests of converter user by the same use of transfer standards.
5. Periodically testing high-resolution converters used in precision automatic test equipment.
6. Providing performance data during development stages of new converter products.

The parameters measured include integral linearity, differential linearity, offset error, gain error, and equivalent rms input noise. Typically the 10 most-significant bits are tested, it is assumed that the errors due to the least-significant bits are insignificant. However it is possible to

test all 2^N codes, N being the resolution of the converter.

Figure 16 is a block diagram of the test setup used. DAC testing is accomplished by comparing the DAC under test to a DAC standard, a 20-bit plus sign, relay-switched converter developed at the National Bureau of Standards. This DAC incorporates less than 1 ppm linearity error and incorporates a self-calibration feature. ADCs are tested using the servo-loop integrating technique described in Section 3.3. However, instead of using an averaging voltmeter, the integrator output voltage is compared to the DAC standard. Table 5 gives the test set accuracy specifications.

It should be noted that converters must meet certain specifications in order to be compatible with the NBS test set. Table 6 lists these specifications. It is also the customers responsibility to mount the test converter on a suitable test board, provide all trimmer circuits, voltage references, input or output amplifiers, recommended power supply decoupling capacitors, and connectors for interfacing to the input/output lines.

Due to the slow sample rate of the 15-bit system tested in Section 3.4, it is not possible to make use of this service.

For more specific details of the service, see reference 3.

Figure 16. National Bureau of Standards Static Test Setup

Table 5

NBS Test Set Accuracy

Parameter		Estimated Systematic Uncertainty DAC's	ADC's
Linearity Error: ±10 V range		2.7 ppm + 0.04 LSB	4.7 ppm + 0.16 LSB
0-10 V, ±5 V		3.5 ppm + 0.04 LSB	5.5 ppm + 0.16 LSB
0-5 V		4.2 ppm + 0.04 LSB	6.2 ppm + 0.16 LSB
Bit Coefficients	0th	same as linearity error	same as for linearity error, less 0.06 LSB
	1st to 10th	same as linearity	same as for 0th coef., less 1 ppm
Differential Linearity Error:	±10 V	3.2 ppm + 0.04 LSB	5.2 ppm + 0.16 LSB
	0-10 V, ± 5 V	4.2 ppm + 0.04 LSB	6.2 ppm + 0.16 LSB
	0-5 V	5.2 ppm + 0.04 LSB	7.2 ppm + 0.16 LSB
Offset Error[a]		3 ppm	3 ppm + 0.07 LSB
Gain Error[a]		6 ppm	6 ppm + 0.13 LSB
RMS Input Noise		-------	-100%; +(20% + 10μV) Noise introduced by Test Set is $30nV/\sqrt{Hz}$ in a 1 MHz BW.

[a] Measured upon special request only, and only if no adjustable trimmers are provided for these parameters.

Table 6

NBS Test Converter Specifications

Parameter	Specifications of Test Converters DAC's	ADC's
Resolution (Bits)	12-18	12-16
Voltage Ranges (V)	0-10; ±10; 0-5; ±5	
Output Load Capability	10kΩ ‖ 100pF	------
Input Impedance	-------	≥ 200Ω/V
Coding	Full Parallel Input or Output: Binary Unipolar Offset Binary Two's Complement One's Complement Sign-Magnitude Binary Complemented Versions of Above	
Acceptable Convert Command	20 µs positive pulse for DAC's with input latches	2 µs positive pulse
Status Output Command	-------	Required
Logic Compatibility	TTL	
Settling Time	<2ms	-------
Conversion Time	-------	≤100µs
External Power Requirements	±15V, +5V	
Maximum error including gain & offset	500 ppm	

4. Dynamic Testing Analog-to-Digital Converters

Dynamic testing an analog-to-digital converter (ADC) refers to the performance evaluation of the converter when it is subjected to a time varying input voltage. A dynamic test will give a true indication of the converter's performance in its intended application. A dynamic test takes into account the slew rate limitations of active devices in the circuit, settling times, and the ADC aperture jitter. Normally the analog input voltage is a sinusoidal waveform. This is because readily available waveform generators can be used to supply the input waveform, a sinusoid is precisely known mathematically, and the sine wave allows the performance to be specified at discrete frequencies. Also, since the input waveform has to be of lower distortion than the degree to which the test accuracy has been specified, it is also much easier to obtain a low distortion sine wave than say a highly linear triangle wave. In addition it is easier to verify the distortion level of a sinusoid using a spectrum analyzer.

Three dynamic test methods will be discussed. The first method discussed is the histogram method. This method is used to find missing codes and give an estimate of the differential nonlinearity. The second method is the Fourier transform method. The error being measured with this method is integral nonlinearity, however, an indication of the differential nonlinearity, aperture uncertainty, and noise is also given. The

last method discussed is the sine wave curve fit method. This method gives an overall indication of a converters performance by calculating a parameter referred to as the effective number of bits. A block diagram of the setup used to acquire data for the three tests is shown in Figure 17.

4.1 Histogram Method

The dynamic differential nonlinearity performance of an ADC is best evaluated using the histogram method. This method consists of obtaining several samples of a spectrally pure sine wave and then forming a histogram of the number of occurrences as a function of the output code. From this missing codes can be found and an estimate of the differential nonlinearity can be obtained. Gain error is also observable since it tends to compress or expand the histogram. Offset error shows up as a shift of the histogram symmetry point from the ideal case of zero. The precision of the measurement is specified by the number of samples taken. This method can also be used to measure the overall noise in the system. A block diagram of the test setup is shown in Figure 17.

The histogram method also has the inherent property of eliminating noise from being a deterrent in the calculation of the transition voltages. Since noise has a random characteristic, it tends to be averaged out as the number of samples increases.

It may seem that a triangle wave is a more appropriate input waveform. However, it is much easier to obtain a low distortion sine wave than it is to obtain a low distortion triangle wave. It is also much easier to test the distortion level of a sine wave

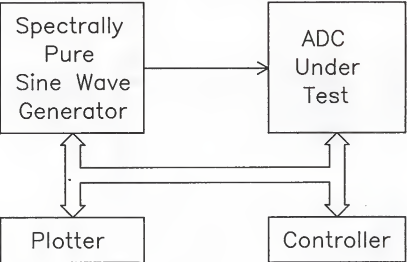


Figure 17. Block Diagram of ADC Dynamic Test Setup

than a triangle wave. Hence a sine wave will be used as the input waveform (see Appendix D).

The probability density function for a sine wave of the form Asin(wt) is[4]

$$p(V) = \frac{1}{\pi\sqrt{A^2-V^2}}.$$

This function is plotted in Figure 18. Integrating with respect to voltage gives the distribution function $P(V_a, V_b)$, the probability that the input voltage is between V_a and V_b:

$$P(V_a,V_b) = \frac{1}{\pi}\left[\sin^{-1}\left(\frac{V_b}{A}\right)-\sin^{-1}\left(\frac{V_a}{A}\right)\right] .$$

Converting this to a discrete distribution gives

$$P(i) = \frac{1}{\pi}\left[\sin^{-1}\left(\frac{V_r[i-2^{N-1}-1]}{A2^N}\right)-\sin^{-1}\left(\frac{V_r[i-2^{N-1}-2]}{A2^N}\right)\right]$$

$$i=1,\ldots,2^N$$

where

V_r is the reference voltage of the ADC,

N is the resolution of the ADC,

i is the code under test, and

A is the peak voltage of the input waveform.

The histogram is then normalized using P(i) and the differential nonlinearity is calculated:

$$DF(i) = \frac{\text{actual probability (i)}}{\text{ideal probability (i)}} - 1 \quad \text{LSB}$$

$$= \frac{H(i)/Npts}{P(i)} - 1 \quad \text{LSB}$$

$$i=1,\ldots,2^N$$

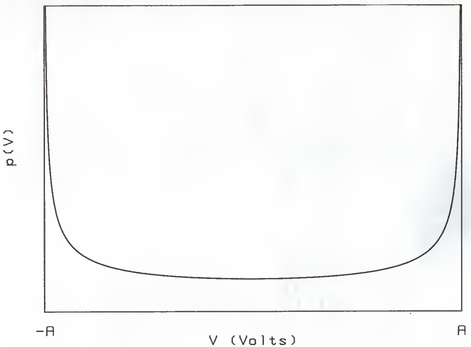


Figure 18. Probability Density Function of a Sine Wave

where

i is the code under test,

H(i) is the number of counts for code i, and

Npts is the total number of samples taken.

After the histogram has been generated, missing codes may be found; a missing code will have a bin with zero counts, or the differential nonlinearity will be minus one.

Note that when using this method, the amplitude A and the reference voltage V_r must be known, and to a high degree of accuracy for a high resolution converter. The reference voltage V_r may not be much of a problem to measure, since it is a dc voltage and dc voltmeters are available which are very accurate. However, it is much more difficult to measure the peak amplitude of the input waveform since ac voltmeters take rms measurements and very accurate ones have limited bandwidths. An alternate method of calculating differential nonlinearity is to estimate the transition voltages from the histogram data. This is accomplished with the use of the cumulative histogram CH(i), where CH(i) is

$$CH(i) = \sum_{j=1}^{i} H(j) \quad i=1,\ldots,2^N.$$

The voltage V(i) for a given CH(i) is given by[4]

$$V(i) = -A\cos\left[\frac{\pi\, CH(i)}{Npts}\right] \quad i=1,\ldots,2^N-1.$$

Here A can be normalized, since it is constant, so that the span of the converter is ±1. Now differential nonlinearity can be calculated from

$$DF(i) = \frac{V(i+1)-V(i)}{1\ LSB} - 1 \quad LSB$$

$$i=1,..,2^{N}-1.$$

It was noted earlier that the degree of test accuracy depends on the number of samples taken. To find the minimum number of samples needed for an estimate of differential nonlinearity, a 100(1-a) percent confidence interval of the form $(\mu - Z_{a/2}s, \mu + Z_{a/2}s)$ is set up. This says that the measured differential nonlinearity lies in the range $(\mu - Z_{a/2}s, \mu + Z_{a/2}s)$ with a 100(1-a) percent probability. The minimum number of samples, Npts, needed for B bit precision and 100(1-a) percent confidence is given by[4]

$$Npts > \frac{Z_{a/2}{}^{2}\ \pi\ 2^{N-1}}{B^{2}}$$

where $Z_{a/2}$ is found in a standard normal distribution table, and N is the resolution of the converter. Thus to know the differential nonlinearity for a 15-bit converter to within 0.1 bit with 95% confidence requires 19,770,000 samples.

This last calculation shows the major limitation of this method. For high-resolution converters, a large number of samples are required for a high test accuracy. This means that a large amount of time may be spent in acquiring the data, during which the amplitude of the input waveform drifts and hence degrades the desired accuracy of the test. For example, if the above converter has a maximum sample rate of 1,000 Hz, it will take 5 1/2 hours to acquire the data. Thus it may be desirable to test the converter with a lower degree of confidence and less precision in order to cut down on testing time. If the precision is changed to

0.25 bit and the confidence interval lowered to 85%, the number of samples is reduced to 1,708,000 and the test time becomes about 45 minutes.

The overall noise in the system is found (but only to a resolution of 1 LSB) by grounding the input and seeing how many of the bins fill up. Ideally only the bin corresponding to zero will be filled, but if noise is present in the system codes around zero will also contain some counts. It also possible to find the dc offset using this method. If the bin which accumulates the counts is anything other than zero, then the voltage which corresponds to that bin is the dc offset.

The offset can also be found using the histogram data. The offset voltage is found from the shift of the histogram about the midpoint of 0V. Let

$$N_n = \sum_{i=1}^{2^{N-1}} H(i) \quad \text{and} \quad N_p = \sum_{i=2^{N-1}+1}^{2^N} H(i)$$

then an estimate of the offset can found from[4]

$$V_o = A\frac{\pi}{2}\sin\frac{N_p-N_n}{N_p+N_n}.$$

4.2 Fourier Transform Method

The dynamic integral nonlinearity performance of an ADC is best evaluated using the Fourier transform method. A block diagram of the test setup is shown in Figure 17. The application of this method is simple. A spectrally pure sine wave is applied to the ADC under test and a sequence of samples is obtained. Then using a fast Fourier transform (FFT) algorithm, the discrete

Fourier transform (DFT) is computed and plotted. The output spectrum will contain the input sine wave plus errors introduced by the ADC. The errors of the ADC introduce harmonics and noise. When obtaining the samples, the sampling frequency should be noncoherent with the input sine wave in order to avoid sampling the same points over and over again.

Integral nonlinearity shows up as harmonics of the input sine wave. For example, given the nonlinear function of

$$f(t) = A\sin(wt) + B[\sin(wt)]^2$$

and expanding this function using the trigonometric identity

$$[\sin(wt)]^2 = \frac{1-\cos(2wt)}{2}$$

results in the equation

$$f(t) = \sin(wt) + \frac{B}{2} + \frac{B}{2}\cos(2wt).$$

Thus f(t) contains the fundamental plus the second harmonic and a dc offset. Further analysis shows that higher harmonics show up when additional terms of higher power are added to f(t).

The dynamic range (ratio of full-scale to the quantization error) of an N-bit converter is known to be

$$\text{dynamic range} = 20\log_{10}(2^N) = 6.02N \text{ dB}.$$

Therefore the number of bits of integral nonlinearity can be calculated by dividing the amplitude of the highest harmonic in the output spectrum by 6.02. If the integral nonlinearity is less than 6.02N dB below the fundamental, then it is less than one LSB. Dynamic range for various resolution converters is tabulated

in Appendix C.

Information about noise, differential nonlinearity, and aperture uncertainty can also be obtained from the output spectrum, although they can not be measured directly. All of these errors show up as an elevation of the noise floor.

The overall noise in the system can be modeled as being white noise since it is mostly due to resistors and active components in the system and hence the amplitude of all frequency components will be raised in the output spectrum. If a large amount of noise is due to digital circuitry, it will show up at frequencies corresponding to the digital clock frequency and its harmonics.

Ideal quantization of the input waveform introduces an rms noise voltage of

$$V_Q = \frac{Q}{\sqrt{12}} = \frac{2A}{\sqrt{12}\ 2^N}\ \text{V}.$$

Differential nonlinearity changes the quantization step size from its ideal size of one and hence tends to increase the rms quantization noise.

Aperture uncertainty (the uncertainty in the time at which a sample is taken, a characteristic of the sample-and-hold for most converters but an inherent characteristic for flash type converters) also tends to raise the noise floor. Aperture uncertainty introduces an amplitude uncertainty in the sample. This amplitude variation is different with every sample. Hence aperture uncertainty effectively adds a random noise voltage to the input waveform, hence the noise floor of the output spectrum increases. The amount is dependent upon the frequency of the

input waveform and the uncertainty time. Higher frequency waveforms require smaller aperture uncertainty times to achieve the same accuracy as a slower frequency waveform with a given aperture uncertainty.

Figures 19(a) and 19(b) illustrate the effect of an aperture uncertainty of 100nS and 500nS respectively. The input waveform in this case was generated in software with no quantization, thus the noise is due entirely to aperture uncertainty.

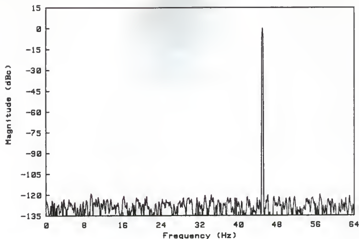
Ideally it is also possible to obtain the signal-to-noise ratio (SNR) from the output spectrum. This can be found by taking the ratio of the fundamental's power to that of the power in the rest of the components. The theoretical SNR is the ratio of the power in the input waveform to the quantization error, since quantization is the only noise source for an ideal system. The average power of a sinusoid is known to be $A^2/2$ and the power in the quantization noise is $Q^2/12$ where $Q=2A/2^N$. Thus

$$\mathrm{SNR} = 10 \ \mathrm{Log} \frac{\frac{A^2}{2}}{\frac{Q^2}{12}} \ \mathrm{dB}$$

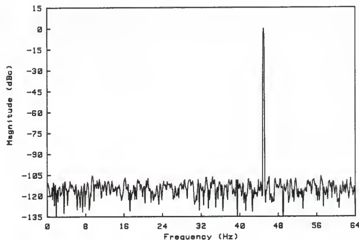
$$= 6.02N + 1.76 \ \mathrm{dB}.$$

The ideal signal to noise ratio for different resolution converters is tabulated in Appendix C.

When obtaining data, it is not always possible to sample an integral number of periods of the input waveform. If a DFT is performed on a sequence in which there is not an integral number of periods, a phenomenon known as spectral leakage occurs. This is because the DFT is a Fourier series expansion which assumes that all components are periodic over NT, where N is the number



a. Uncertainty=100nS, f=45 Hz, fs=128 Hz, 1024 points



b. Uncertainty=500nS, f=45 Hz, fs=128 Hz, 1024 points

Figure 19. Effects of Aperture Uncertainty

of samples taken and T is the sampling interval. If they are not, then the periodic extension of the sequence assumed by the DFT contains discontinuities. In addition there are only a finite number of frequencies which can be used to describe the input waveform. The frequency resolution of the transform is given by FS/N, where FS is the sampling frequency. If the input has a component which is not an integral number of the frequency resolution, its amplitude leaks over into the frequency components adjacent to it, thus the term spectral leakage. For example, if FS is 128 Hz and N is 1024, the frequency resolution of the DFT is 0.125 Hz. A frequency of 24.3 Hz is 194.4 times the frequency resolution, hence leakage occurs.

Spectral leakage also makes it impossible to calculate SNR from the output spectrum data due to the power in the fundamental spreading out into adjacent components.

In order to combat leakage, the input sequence is multiplied by a window function, a process known as windowing. The exact properties of windowing are beyond the scope of this discussion. For a full explanation of its properties, see references 5 and 6. In short though, the window function tapers off the ends of the input sequence to zero, hence eliminating the discontinuities that occur for a periodic extension of the sequence. The information of the input signal in the frequency domain is not lost however. A good window has a very narrow bandwidth in the frequency domain (it is approximately a delta function) and using the fact that multiplication in the time domain is convolution in the frequency domain, windowing is nothing more than convolving an approximate delta function with the input signal's output

spectrum. Thus the input signal's components still remain, but their amplitudes may change. It should be noted that the above discussion is very loose, and that not all window functions will give good results. Some may even make the situation worse. Reference 6 presents a good discussion of this.

The choice of which window to use is usually dependent on the application. Reference 6 gives some optimal windows for certain conditions. The Hanning (or Von Hann) window is a good general purpose window and is usually used in practice (at least it is the one which is used in most of the literature) for spectral estimation. Thus this will be the one used for the tests performed in Section 4.4.

4.3 Sine Wave Curve Fit Method

The sine wave curve fit test gives an overall indication of a converter's performance by finding its effective number of bits. The effective number of bits may be considered the number of bits in a perfect ADC whose rms quantization error is equal to the total rms error of the unit under test.[7] This total rms error would include the errors from all sources in the ADC under test: quantization error, differential nonlinearity error, missing codes, integral nonlinearity, aperture uncertainty and noise. A block diagram of the test setup used to obtain data is shown in Figure 17.

The first step in determining the effective bits is to apply a spectrally pure sine wave to the converter under test, digitizing it and then fitting the data to a sine wave of the form

$$A\sin[2\pi ft+theta]+dc$$

where A, f, theta, and dc are parameters selected using a least-squares error minimization algorithm. After the best fit sine wave has been calculated, the rms error between the actual data and the best fit sine wave, rms error (actual), is calculated. Then knowing the rms error of an ideal ADC of the same resolution, rms error (ideal), the effective number of bits is calculated from

$$\text{effective bits} = N - \log_2 \frac{\text{rms error (actual)}}{\text{rms error (ideal)}} .$$

Knowing that the quantization error as a function of input voltage for a perfect ADC is a ramp function with an amplitude of Q, Q being the quantization error of an ideal N-bit ADC, the rms error (ideal) is found to be

$$\text{rms error (ideal)} = \frac{Q}{\sqrt{12}} = \frac{2A}{\sqrt{12}\ 2^N} .$$

By obtaining the effective number of bits for several frequencies, the frequency response of the converter can be specified by a plot of the effective bits as a function of frequency.

When obtaining data for the sine fit, a large number of data points should be taken, on the order of 1,024 to 2,048. If an insufficient number of data points are obtained, errors in the ADC can change the apparent frequency of the sine wave and thus reduce the actual rms error.[8] The test frequency should also be nonharmonically related to the sample frequency. If it is not, then the same codes would occur over and over again, thus not exercising the entire system. Also, if the test frequency is

harmonically related to the sample frequency, harmonics introduced by the ADC will be aliased back into the fundamental, thus giving a higher number of effective bits. Finally, the test amplitude should be close to the full-scale input range of the converter. The amplitude should be kept just low enough not to introduce distortion due to clipping of the input waveform and hence decreasing the effective number of bits.

4.4 Testing a 15-bit Data Acquisition System

Using the methods described in Sections 4.1 and 4.2, a 15-bit data acquisition system (DAS) has been evaluated. A block diagram of the test setup used in acquiring data for both methods is shown in Figure 20. The control operations are performed by a Hewlett-Packard 9845B desktop computer system. Data from the DAS is passed to the 9845B via a Hewlett-Packard 98032A Bit-Parallel Interface. The purpose of the band-pass filter is to obtain a spectrally pure sine wave (Appendix D).

The DAS tested is a prototype, constructed to verify the operation of the design. The DAS consists of two sections, an analog section and a digital section. The analog section performs the analog-to-digital conversion while a microprocessor based (Intel 80C39) digital section performs the control functions, timing, and interface operations. Photographs of the system are shown in Figure 21.

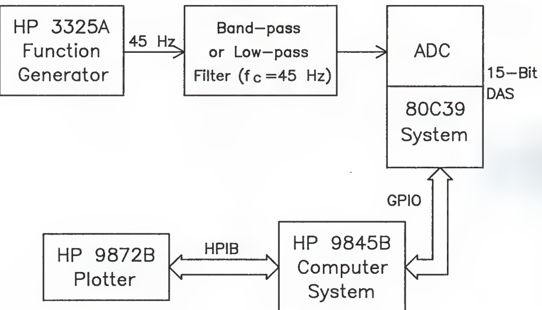
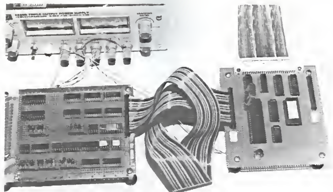


Figure 20. Setup for 15-bit DAS Dynamic Tests



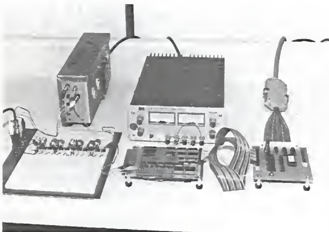


Figure 21. Photographs of 15-bit DAS

4.4.1 <u>Histogram Test</u> Using the histogram test of Section 4.1, an estimate of differential nonlinearity has been obtained. Three tests were performed, one for each of the three DACs tested in Section 1.2. The reason for this is to check the ADCs performance as a function of the DAC used, the most critical component in the design.

The key to obtaining accurate results using the histogram method is to acquire several samples. A method for calculating a minimum number of points given a desired confidence interval was presented in Section 4.1. It was shown that for a 15-bit converter 19,700,000 samples were required to estimate differential nonlinearity to within 0.1 bit with 95% confidence. The nominal sample rate for the DAS is 128 Hz. At this sample rate, it would require almost 43 hours just to acquire the data not to mention processing by the controller. In this time the input waveform would probably drift several millivolts and hence ruin the desired test accuracy. Thus, for the given application there will have to be a trade-off of test accuracy and confidence for testing time.

For the tests performed, 1,638,400 samples were taken. This corresponds to a 84% confidence interval with 0.25 bit precision. This still requires about 4 hours to acquire the data, during which processing and storage operations must be accomplished, adding an additional few hours. Therefore the input waveform will drift and hence degrade the given precision and confidence interval. However, this is all that can be done with such a slow sample rate. As will be seen though, the results pretty well agree with those of the static tests performed in Section 3.4.

The amplitude of the input waveform was set to be slightly greater than full-scale (±5V), ±5.091V (3.6Vrms). This is to ensure that all codes are exercised.

Figures 22 through 24 illustrate the results obtained. Figures 22a, 23a, and 24a are histograms of the data. Figures 22b, 23b, and 24b are the differential nonlinearity estimates obtained from the histogram data. As was noticed in the static tests, the system has a large differential nonlinearity at zero-crossing. At all other points however, the differential nonlinearity is less than two LSBs. Thus the system basically has 14-bit differential nonlinearity (with respect to ±1 LSB).

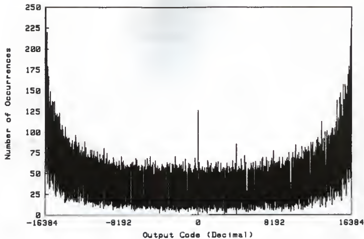
Missing codes show up as points with a differential nonlinearity of minus one. A search of the data files was performed to find the number of missing codes for each test. The results are given in Table 7.

Table 7

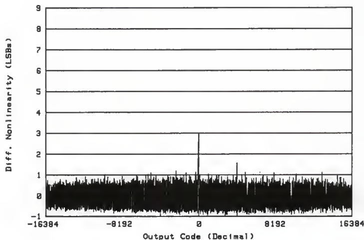
Missing Codes for Dynamic Histogram Test

Figure	Number of missing codes
22	5
23	44
24	32

Note that the tests performed using DAC#1 obtained much better results than the tests using DAC#2 and DAC#3. This indicates that the performance of the DAS is dependent on the DAC to some degree. Of the above missing codes, only one was common with all three tests, the code of -4. Thus it could be possible that some of the codes which are indicated as being missing are actually not. It could be due to the fact that an insufficient

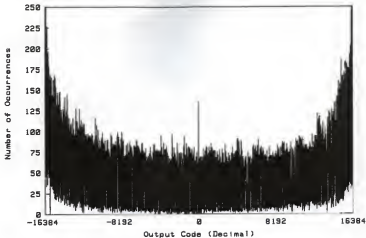


a. Number of Occurrences as a Function of Output Code

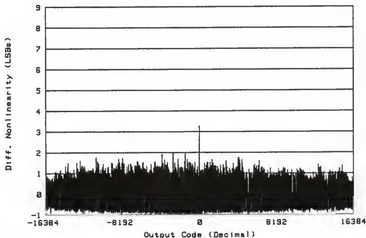


b. Diff. Nonlinearity as a Function of Output Code

Figure 22. Histogram Test Results using DAC#1

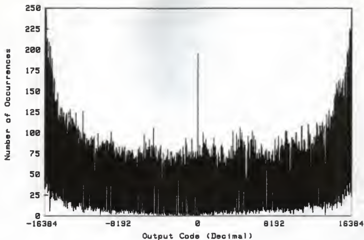


a. Number of Occurrences as a Function of Output Code

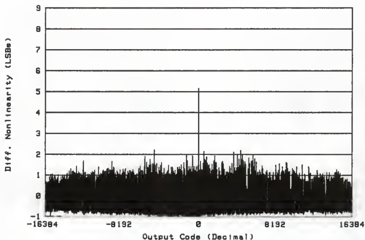


b. Diff. Nonlinearity as a Function of Output Code

Figure 23. Histogram Test Results using DAC#2



a. Number of Occurrences as a Function of Output Code



b. Diff. Nonlinearity as a Function of Output Code

Figure 24. Histogram Test Results using DAC#3

number of samples were taken to ensure that all the codes were exercised. Remember that the confidence interval was 84% and the bit precision was 0.25 bit. Thus 16% of the codes indicated as being missing could actually exist, or their code widths may be less than 0.25 LSB.

Comparing these results to the static tests of Section 3.3, the differential nonlinearity seems to be slightly greater for the dynamic tests, approximately 1 LSB. A larger differential nonlinearity indicates more missing codes, as was found to be true.

4.4.2 Fourier Transform Test Using the method of Section 4.2, the dynamic integral linearity performance of the 15-bit DAS has been evaluated. For the tests performed, 2,048 samples were taken. Even though this exercises only a fraction of the possible output codes, experience has shown that successive tests gives similar results. It should be noted that DAC#1 of Section 4.4.1 is used for all tests performed.

The maximum frequency of interest for the DAS is 45Hz and its span is ±5V. The nominal sampling frequency is 128Hz. When a DFT is performed on the samples, the frequency window is from dc to 64Hz. Therefore with an input frequency of 45Hz, the harmonics will be outside of the frequency window. However, due to aliasing they are all folded back into the window, showing up at their respective aliased frequencies. In order to determine exactly where they show up, a software simulation was performed. A 45Hz sinusoid and its first 8 harmonics were sampled at 128Hz. The amplitude of each harmonic was decreased by 20dB, thus making it possible to detect the respective harmonic in the frequency

window. The result is shown in Figure 25, and the exact frequencies are tabulated in Table 8.

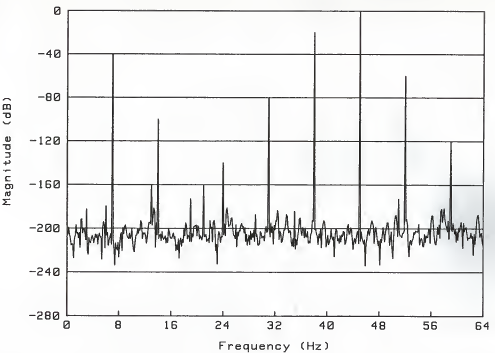
Table 8

Location of Harmonics in the DFT Frequency Window

Harmonic	Frequency (Hz)
1st	45
2nd	38
3rd	7
4th	52
5th	31
6th	14
7th	59
8th	24
9th	21

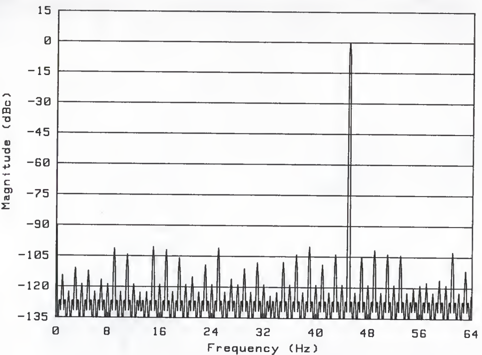
Using software, a perfect 15-bit ADC sampling a 45Hz sine wave at 128Hz was simulated. The resultant output spectrum is shown in Figure 26. This is used for comparison with the test results to follow.

The first test performed uses a 45Hz 9.9Vpp sine wave input. The input is slightly less than full-scale in order to avoid clipping, and hence erroneous results. The results are shown in Figure 27a. Dynamic range sets the test limit for 1 LSB accuracy of a 15-bit converter at -90dBc (all components must be 90dB below the fundamental of full-scale amplitude for 1 LSB accuracy). This test shows that there are several components well above -90dBc, indicating a large integral nonlinearity. The highest component is contained in the 2nd harmonic, at a magnitude of approximately -55dBc. The dynamic range for an N-bit converter was given in Section 4.2 as being 6.02N. Thus the DAS has an effective dynamic range of 9.1 bits. Further investigation



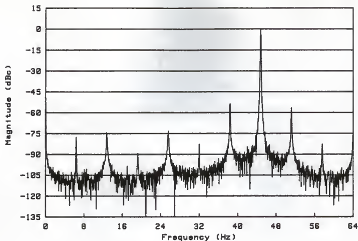
f = 45 Hz, Sampling Frequency = 128 Hz, 1024 points

Figure 25. Location of Harmonics in the DFT Frequency Window

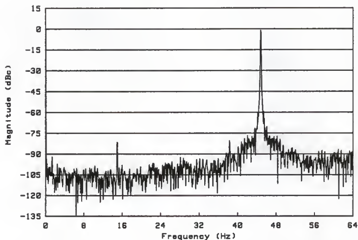


f=45 Hz, fs=128 Hz, 1024 points

Figure 26. Spectrum of an Ideal 15-bit ADC

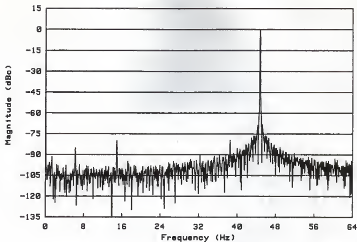


a. f=45 Hz, fs=128 Hz, Vin=9.9Vpp, 2048 points

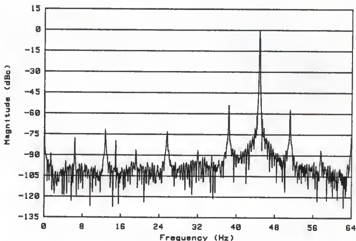


b. f=45 Hz, fs=128 Hz, Vin=4.9Vpp+2.5Vdc, 2048 points

Figure 27. Fourier Transform Test Results

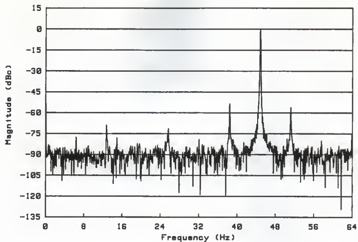


c. f=45 Hz, fs=128 Hz, Vin=4.9Vpp-2.5Vdc, 2048 points

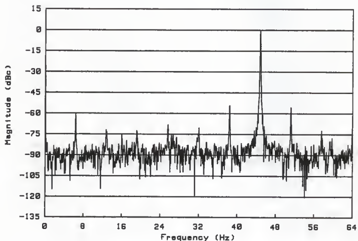


d. f=45 Hz, fs=128 Hz, Vin=4.9Vpp, 2048 points

Figure 27 (cont'd). Fourier Transform Test Results

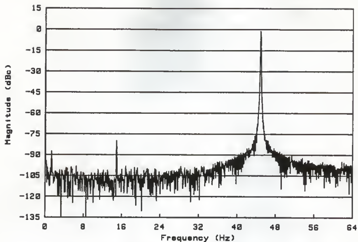


e. f=45 Hz, fs=128 Hz, Vin=4.9Vpp, 2048 points

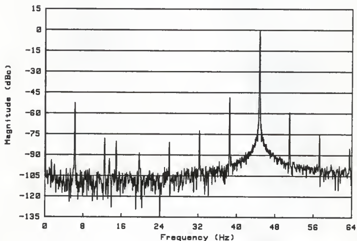


f. f=45 Hz, fs=128 Hz, Vin=500mVpp, 2048 points

Figure 27 (cont'd). Fourier Transform Test Results



g. f=45 Hz, fs=128 Hz, Vin=4.9Vpp+2.5Vdc, 2048 points



h. f=45 Hz, fs=128 Hz, Vin=4.9Vpp-2.5Vdc, 2048 points

Figure 27 (cont'd). Fourier Transform Test Results

has found that this is unique to a signal which changes sign. Part of this is due to the large differential nonlinearity at zero, but it does not explain distortion to the degree indicated. The noise floor of the spectrum is well below the 90dB threshold however. This indicates that the overall system noise, the differential nonlinearity, and the aperture uncertainty of the sample-and-holds are acceptable.

For the second test, the band-pass filter was replaced with a low-pass filter (see Appendix D) and a 4.9Vpp sine wave with a 2.5Vdc offset was applied, thus only exercising the positive range of the converter. The result is shown in Figure 27b. Since only one-half of the converter's span is being exercised, the results with the dc offset can be assumed to be those of a 14-bit converter. Therefore the test limit is now -84dBc. The component at 15Hz is from the function generator, a component the low-pass filter is unable to filter out, as predicted in Appendix D. Therefore the only unacceptable component due to the converter shows up at the 2nd harmonic. Its amplitude is about -80dBc, an effective dynamic range of 13.3 bits, only 0.7 bits away from the test limit. The noise floor is again well below -90dBc, indicating acceptable overall noise, differential nonlinearity, and aperture uncertainty.

Exercising the negative range with a -2.5Vdc offset and a 4.9Vpp input obtains similar results. This result is shown in Figure 27c. Note that a component at the 3rd harmonic is also present, but of a little less magnitude. This component therefore does not degrade the dynamic range, but does increase the signal-to-noise ratio. As an experimental control factor, a test was

performed with 4.9Vpp input but without the offset, still using the low-pass filter, Figure 27d, and without the filter, Figure 27e. Figure 27d supports the evidence that the converter's integral linearity is degraded when a bipolar signal is used. Figure 27e shows that the the distortion is not due to the filter, since the harmonics are of the same amplitude. The noise floor is raised however. This is because the noise of the function generator is filtered out when the low-pass filter is used.

Note that the second harmonic in the tests performed with the 4.9Vpp input is at -55dBc, the same as with a 9.9Vpp input. This suggests that the distortion is not dependent on the amplitude. To help support this last statement, a test with a 500mVpp input was performed, Figure 27f. Again the second harmonic is 55dB below the fundamental. This verifies that the distortion is amplitude independent.

It was found that the harmonics obtained in Figures 27b and 27c were due to the sample-and-hold opamps (Precision Monolithic OP-22s). The sample-and-hold opamps were replaced with some National Semiconductor LF356s, an industry standard high-performance opamp with excellent open-loop gain characteristics and an excellent sample-and-hold opamp. Figure 27g illustrates the results of digitizing a 4.9Vpp signal with a 2.5Vdc offset. In this test no significant harmonics are present, the one at 15Hz is introduced by the function generator as stated previously. The converter is working almost ideally, with the exception of unavoidable noise. A comparison of Figures 27g and 27b indicate that the 2nd harmonic of Figure 27b is due to the

nonlinearity of the sample-and-hold opamps. A rather interesting result was obtained when a -2.5Vdc offset was used, Figure 27h. In this example, several harmonics are present. An indication that one, if not both, of the LF356s used is very nonlinear for negative input voltages.

4.4.3 Conclusions Using the methods of Sections 4.1 and 4.2, the dynamic performance of a 15-bit data acquisition system has been evaluated.

The histogram method was used to estimate the differential linearity. Results show the differential nonlinearity to be about 14-bits. This test also showed that missing codes are present in the system, the number dependent on the DAC used in the system.

The Fourier transform method was used to estimate integral nonlinearity. It was found that the system has a large amount of distortion when a bipolar signal is sampled. When a dc offset is applied to the signal, hence exercising only positive or negative voltages, the system distortion was reduced dramatically. Effectively 13.3-bit linearity was achieved (since the span is cut in half the system resolution becomes 14 bits). Further tests indicated that the nonlinearity is independent of the input amplitude. Though the harmonics found in the tests which used a dc offset were at acceptable levels, it was found that they were due to the sample-and-hold opamps. Using a higher performance opamp obtained excellent results, essentially no distortion.

APPENDIX A

Digital-to-Analog Converter Terminology

APPENDIX A

Digital-to-Analog Converter Terminology

Introduction

As with many other areas of electronics, there is a lack of an industry-wide standardization of terminology used to describe the characteristics of digital-to-analog converters (DACs). It seems that every manufacturer has its own unique definition of a specific term. The following definitions are taken from the Analog Devices 1984 Databook, Volume 1, Section 9, and an applications note published by Teledyne Philbrick, bulletin AN-25, July 1976. Discussions in the body of this thesis are based on these definitions.

Parameter Definitions

Accuracy, Absolute - The error of a DAC is the difference between the actual analog output and the theoretical output when a given digital code is applied to the converter (Figure A-1b). Sources of error include gain (calibration) error, zero error, linearity errors, and noise. Absolute accuracy is normally expressed as a percentage of full-scale and when given with a maximum value, it indicates the worst case deviation from the ideal point.

Accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of

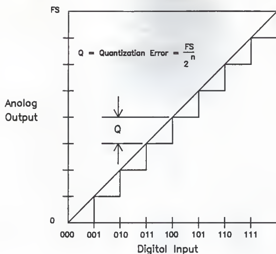


Figure A—1a. Transfer Function of Ideal 3—bit DAC

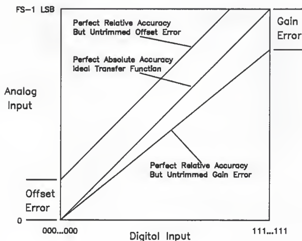


Figure A—1b. Accuracy, Gain Error, and Offset Error

1/16 (6.25%), but it might have an accuracy to within 0.01% of each ideal value.

Accuracy, Relative - Relative accuracy error is the deviation of the analog output at any code from its theoretical value after the full-scale range (FSR) has been calibrated (Figure A-1b). Since the discrete analog output values corresponding to the digital input values ideally lie on a straight line, the relative-accuracy error of a linear DAC can be interpreted as a measure of nonlinearity error.

After the gain and offset errors are adjusted to zero, a converter with perfect relative accuracy will display perfect absolute accuracy. Relative accuracy error is expressed in percent of full-scale, ppm, or fractions of 1 LSB.

Differential Nonlinearity - Differential nonlinearity for a DAC is defined as the maximum deviation of any bit size from its theoretical value of 1 LSB over the full conversion range (Figure A-2). For example, differential nonlinearity of ±1/2 LSB demands that each step be 1 ±1/2 LSB.

A differential nonlinearity of less than or equal to -1 LSB is the maximum allowed for monotonic operation. In addition, differential nonlinearity directly affects the nonlinearity of the input-output transfer function.

Full-Scale (FS) - Full-scale is defined as the absolute value of the maximum analog output voltage of the DAC. For example, a DAC with an output range of 0V to 10V has a full scale of 10V. A DAC with an output range of -5V to +5V has a full scale of 5V.

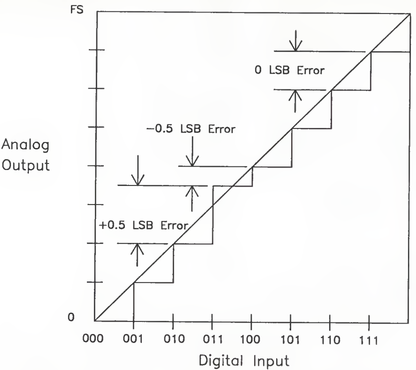


Figure A–2. Differential Nonlinearity

Gain Error - Gain error is the difference in slope between the actual input-output relationship and the ideal relationship, ignoring offset error (Figure A-1b). This is usually quoted as a percentage of full-scale, or fraction of 1 LSB.

Integral Nonlinearity - Integral nonlinearity (or just nonlinearity) of a converter is a deviation of the analog values, in a plot of the measured conversion relationship, from a straight line (Figure A-3).

The straight line can be either a "best straight line", determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or it can be a straight line passing through the end points of the transfer characteristic. Sometimes referred to as "end-point" linearity, the latter is both a more conservative measure and is much easier to verify in actual practice. "End-point" linearity error is similar to relative-accuracy error (see Accuracy Relative).

Least-Significant Bit (LSB) - In a system in which a numerical magnitude is represented by a series of binary (i.e. two-valued) digits, the "least-significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost "1" is the LSB. Its analog weight, relative to full-scale, is 2^{-N}, where N is the number of binary digits. It represents the smallest analog change that can be resolved by an N-bit converter.

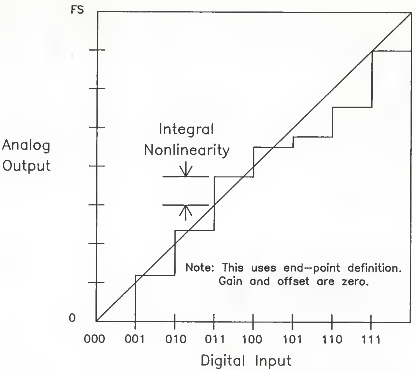


Figure A-3. Integral Nonlinearity

Major and Minor Transitions - The number of bits involved in a code change establish "major" and "minor" transitions. The most major transition occurs at 1/2 scale, when the DAC switches from 011...111 to 100...000. The most minor transition would occur when only the LSB changes, such as when the DAC switches from 000...000 to 000...001.

Monotonicity - A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases, with the result that the output will always be a single-valued function of the input. Monotonicity requires that the differential nonlinearity be > -1 LSB (Figure A-4).

Most-Significant Bit (MSB) - In a system in which a numerical magnitude is represented by a series of binary (i.e. two-valued) digits, the "most-significant bit" is that digit (or "bit") that carries the largest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the leftmost "1" is the MSB. Its analog weight, relative to full-scale, is 2^{-1}.

Noise - The noise of a DAC is defined as the amount of jitter in the analog output. It is usually expressed as a peak-to-peak or rms value over a defined bandwidth. Noise is of primary importance in high-resolution DACs ($\geq$ 12 bits resolution) where the noise can exceed the LSB value over a reasonable bandwidth and thereby reduce the useful resolution.

Offset Error - Offset error is the degree to which the transfer function fails to pass through the origin (Figure A-1b). If this error is not adjusted to zero, a constant absolute accuracy error is added to every point on the transfer function.

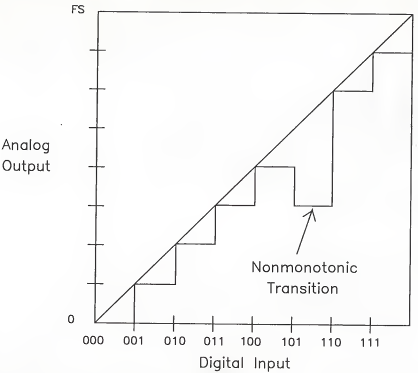


Figure A-4. Monotonicity

Offset error does not degrade the relative accuracy. Offset error is normally expressed as a percentage of full-scale or a fraction of an LSB. Provisions are normally made to adjust this error to zero.

Quantizing Error - The analog continuum is partitioned into 2^N discrete ranges for n-bit processing (Figure A-1a). All analog values within a given range of output are represented by the same digital code, usually assigned to the nominal midrange value. For applications in which an analog continuum is to be restored, there is an inherent quantization uncertainty of $\pm 1/2$ LSB, due to limited resolution, in addition to the actual converter errors.

Resolution - Resolution is defined as the relative value of the least-significant bit (LSB) - the smallest value of change that can be generated by a DAC. Resolution is determined by 2^{-N} of the span for a converter with N binary bits. Resolution is normally expressed in terms of the number of bits, as a percentage of full-scale, or in ppm. Note that useful resolution may be limited by relative accuracy but that resolution need not limit accuracy.

Settling Time - The time required, following a prescribed data change, for the output of a DAC to reach and remain within a given fraction (usually $\pm 1/2$ LSB) of the final value. Typical prescribed changes are full-scale, 1 MSB, and 1 LSB at a major code transition. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output opamp circuit.

Skew - Skew defines the degree to which events that are to occur (ideally) simultaneously do not. Internal DAC skewing is caused by the bit switches not switching simultaneously (in response to simultaneous input commands). Externally, bit switching skew can be aggravated due to skew of the individual bits of the input command. Output glitches are the direct result of skew.

Slew Rate - The maximum rate at which a DAC output voltage can change in response to a full-scale output command. Slew rate is only a guide to speed, In most applications, the important specification is the settling time, which is elapsed time to rated accuracy.

Span - For a DAC with a bipolar output, the span is defined as the sum of the minus full-scale and plus full-scale values, regardless of sign. For example, a converter with an output which has a range of -5V and +5V has a voltage span of 10V. A converter with an output range of 0V to 10V also has a voltage span of 10V.

Stability - Stability of a converter usually applies to the insensitivity of its characteristics to time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion of temperature coefficients in tables of specifications (see "Temperature Coefficients).

Temperature Coefficients - In general, temperature instabilities are expressed in %/^{o}C, ppm/^{o}C, as fractions of 1 LSB/^{o}C, or as a change in a parameter over a specified

temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include gain, linearity, offset (bipolar), and zero. The last three are expressed in % or ppm of full-scale range per degree Celsius.

Zero and Gain Adjustment Principles - Most manufacturers specify zero and gain adjustment instructions on the data sheet. The data sheet instructions should be followed. If instructions are not supplied, the following steps can be followed.

The output of a unipolar DAC is set to zero volts in the all-bits-off condition. The gain is set for $FS(1-2^{-N})$ with all bits on. The "zero" of an offset-binary bipolar DAC is set to -FS with all bits off, and the gain is set for $+FS(1-2^{-(N-1)})$ with all bits on.

APPENDIX B

Analog-to-Digital Converter Terminology

APPENDIX B

Analog-to-Digital Converter Terminology

Introduction

As with many other areas of electronics, there is a lack of an industry-wide standardization of terminology used to describe the characteristics of analog-to-digital converters (ADCs). It seems that every manufacturer has its own unique definition of a specific term. The following definitions are taken from the Analog Devices 1984 Databook, Volume 1, Section 10, and an applications note published by Teledyne Philbrick, bulletin AN-24, July 1976. Discussions in the body of this thesis are based on these definitions.

Parameter Definitions

Accuracy, Absolute - The error of an ADC at a given output is the difference between the theoretical and the actual analog input voltages required to produce that code (Figure B-1b). Since the code can be produced by any analog voltage in a finite band (see Quantizing Error), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce the code.

Absolute error comprises gain error, offset error, and nonlinearity, together with noise.

Accuracy, Relative - Relative accuracy error, expressed in %, ppm, or fractions of an LSB, is the deviation of the analog value at any code (relative to the full analog range of the device

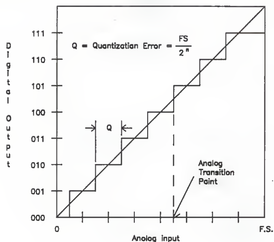


Figure B–1a. Transfer Function of Ideal 3–bit ADC

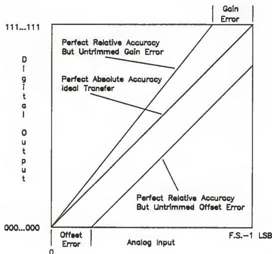


Figure B–1b. Accuracy, Gain Error, and Offset Error

transfer characteristic) from its theoretical value (relative to the same range), after offset and gain errors have been calibrated (Figure B-1b).

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Integral Linearity).

The "discrete points" of an ADC transfer characteristic are the midpoints of the quantization bands at each code (see Accuracy, Absolute).

Conversion Time and Conversion Rate - The time required for a complete measurement by an ADC is called conversion time. For most converters (assuming no significant additional systemic delays), this is identical to the inverse of conversion rate. However, in some high-speed converters, because of pipelining, new conversions are initiated before the results of prior conversions have been determined. Therefore the conversion rate can be greater than the inverse of the conversion time.

In successive-approximation converters, the conversion time is independent of input amplitude. In integrating converters, the conversion time may be somewhat proportional to the input amplitude, varying about 50% from zero to full scale.

Differential Nonlinearity - Differential nonlinearity is defined as the maximum deviation of any bit size from its theoretical value of 1 LSB over the full conversion range. For

example, a differential nonlinearity of ±1/2 LSB demands each step be 1 LSB ±1/2 LSB (Figure B-2).

It is an important specification, because a differential nonlinearity ≤ -1 LSB can lead to nonmonotonic behavior (see monotonicity) of a DAC, and missed codes in an ADC employing such a DAC. In addition, differential nonlinearity directly affects the input-output function's nonlinearity.

Often, instead of a maximum differential nonlinearity specification, there will be a simple specification of "no missing codes", which implies a differential nonlinearity less than 1 LSB.

Full-Scale (FS) - Full-scale is defined as the absolute value of the maximum analog input voltage of the ADC. For example, an ADC with an input range of 0V to 10V has a full scale of 10V. An ADC with an input range of -5V to +5V has a full scale of 5V.

Gain Error - Gain error is the difference in slope between the actual input-output relationship and the ideal relationship, ignoring offset error (Figure B-1b). Gain error does not degrade the relative accuracy. This is usually quoted as a percent error of full-scale. Provisions are normally made to adjust this error to zero. A proper gain adjustment results in the transition from 111...110 to 111...111 occurring at -1 1/2 LSB from the theoretical full-scale output.

Integral Nonlinearity - Integral nonlinearity (or just nonlinearity) of a converter, expressed in percent or parts-per-million of full-scale range, or fractions of a least-significant bit, is the deviation of the analog values from a straight line, in a plot of the measured conversion relationship (Figure B-3).

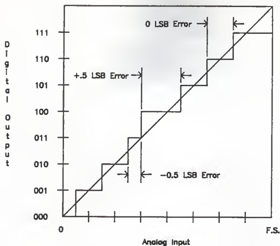


Figure B–2. Differential Nonlinearity

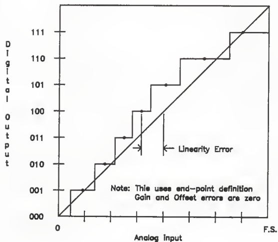


Figure B–3. Integral Nonlinearity

The straight line can be either a "best straight line", determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or , it can be a straight line passing through the end points of the transfer characteristic. Sometimes referred to as "end-point" nonlinearity, the latter is both a more conservative measure and is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Accuracy, Relative).

Figures B4a and B4b demonstrate how the linearity error depends on the definition used. Using the "best straight line" definition, the peak linearity error is minimized, giving a nonlinearity of $\pm 1/2$ LSB. The "end-point" definition gives a nonlinearity of 1 LSB.

Note that integral linearity error is independent of offset or gain errors. Thus, accurate linearity measurements can be made on uncalibrated converters.

Least-Significant Bit (LSB) - In a system in which a numerical magnitude is represented by a series of binary (i.e. two-valued) digits, the "least-significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost "1" is the LSB. Its analog weight, relative to full-scale, is 2^{-N}, where n is the number of binary digits. It represents the smallest change that can be resolved by an N-bit converter.

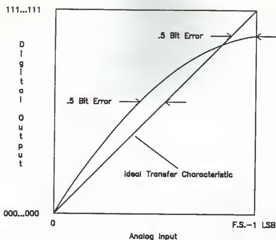


Figure B–4a. Best Fit Definition of Linearity Error

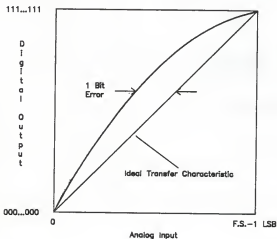


Figure B–4b. End Point Definition of Linearity Error

Major and Minor Transitions - The number of bits involved in a code change establish "major" and "minor" transitions. The most major transition occurs at 1/2 scale, when the ADC switches from 011...111 to 100...000. The most minor transition would occur when only the LSB bit changes, such as when the ADC switches from 000...000 to 000...001.

Missing Code - No missing (skipped) codes requires that the differential nonlinearity be less than +1 LSB. This means that for a continuously increasing input the converter's output, while increasing, will not skip or miss one or more codes (Figure B-5).

Monotonicity - Monotonicity requires that the differential nonlinearity be less than -1 LSB. This means that for a continuously increasing input, the converter's output must not decrease (Figure B-5).

Most-Significant Bit (MSB) - In a Binary (two-valued) numerical system, the most significant bit is that digit or bit that carries the greatest value or weight. For example, in the natural binary number 1011 (decimal 11, or $2^3 + 0 + 2^1 + 2^0$), the leftmost digit is the MSB, with weight, or value, of 1/2 nominal peak-to-peak full scale input.

Noise - The noise of an ADC is defined as the amount of jitter or uncertainty in the transition point for output code changes (Figure B-6). It is usually expressed as a fraction of an LSB. Noise is of primary importance in high-resolution ADC's (greater than or equal to 12 bits resolution) where the noise can exceed the LSB value and thereby reduce the useful resolution.

Offset Error - Offset error is the degree to which the transfer function fails to pass through the origin (Figure B-1b).

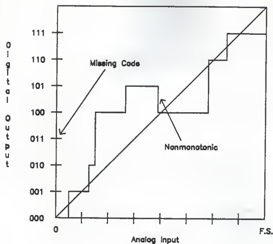


Figure B—5. Missing Code and Monatanicity

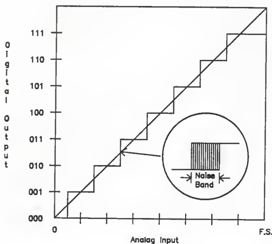


Figure B—6. Effect of Noise on the Transfer Characteristic

If this error is not adjusted to zero, a constant absolute accuracy error is obtained at every point on the transfer function. Offset error is normally expressed in microvolts or LSB's. Provisions are normally made to adjust this error to zero. A proper zero adjustment results in the transition from 000...000 to 000...001 occurring at +1/2 LSB for a unipolar ADC, or from 100.000 to 100...001 at FS/2 + 1/2 LSB for a bipolar ADC.

Quantizing Error - The analog continuum is partitioned into 2^N discrete ranges for N-bit conversion. All analog values within a given range are represented by the same digital code, usually assigned to the nominal midrange value (Figure B-1a). There is, therefore, an inherent quantization uncertainty of $\pm 1/2$ LSB, in addition to the actual conversion errors. In integration converters, this "error" is often expressed as "± 1 count."

Resolution - Resolution is defined as the relative value of the least significant bit (LSB) - the smallest value of change that can be distinguished by an ADC. Resolution is determined by 2^{-N} of the span for a converter with N binary bits. Resolution is normally expressed in terms of the number of bits, as a percentage or in parts-per-million (ppm).

Span - For an ADC with a bipolar input, the span is defined as the sum of the minus full-scale and plus full-scale values, regardless of sign. For example, a converter with an input which may vary between -5V and +5V has a voltage span of 10V.

Stability - Stability of a converter, usually applies to the insensitivity of its characteristics with time, temperature, etc. (See Temperature Coefficients).

Temperature Coefficients - In general, temperature instabilities are expressed in %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include gain, linearity, offset (bipolar), and zero. The last three are expressed in % or ppm of full-scale range per degree Celsius.

Zero and Gain Adjustment Principles - Most manufacturers specify zero and gain adjustment instructions on the data sheet. The data sheet instructions should be followed. If instructions are not supplied, the following steps can be followed.

The zero adjustment of a unipolar ADC is set so that the transition from all-bits-off to LSB-on occurs at $1/2 \times 2^{-n}$ of nominal full-scale. The gain is set for the final transition to all-bits-on to occur at $FS(1-3/2 \times 2^{-n})$. The "zero" of an offset-binary bipolar ADC is set so that the first transition occurs at $-FS(1-2^{-n})$ and the last transition at $+FS(1-3 \times 2^{-n})$.

APPENDIX C

Data Converter Characteristics

APPENDIX C

Data Converter Characteristics

Bits Resolution (N)	2^N	Percent Resolution	Dynamic Range (dB)	Signal-to-Noise Ratio (dB)
3	8	12.5	18.06	19.82
4	16	6.25	24.08	25.84
5	32	3.125	30.10	31.86
6	64	1.563	36.12	37.88
7	128	0.7813	42.14	43.91
8	256	0.3906	48.16	49.93
9	512	0.1953	54.19	55.95
10	1 024	0.09766	60.21	61.97
11	2 048	0.04883	66.23	67.99
12	4 096	0.02441	72.25	74.01
13	8 192	0.01221	78.27	80.03
14	16 384	0.006104	84.29	86.05
15	32 768	0.003052	90.31	92.07
16	65 536	0.001523	96.33	98.09
17	131 072	0.0007629	102.4	104.1
18	262 144	0.0003815	108.4	110.1
19	524 288	0.0001907	114.4	116.2
20	1 048 576	0.00009537	120.4	122.2

Percent Resolution = $1/2^N$

Dynamic Range = $20\text{Log}_{10}(2^N) = 6.02N$ dB

Signal-to-Noise Ratio = $10\text{Log}_{10}(3 \times 2^{2N-1}) = 6.02N + 1.76$ dB

where: signal power = $A^2/2$

A = Peak amplitude of sinusoid

noise power = $Q/(12)^{1/2}$

$Q = 2A/2^N$

APPENDIX D

Spectrally Pure Sine Wave Generation

APPENDIX D

Spectrally Pure Sine Wave Generation

When dynamic testing analog-to-digital converters, the input waveform must be of lower distortion than the converter-under-test in order to ensure that distortion detected in the results is due solely to the converter. When testing a 15-bit ADC, the input must have a distortion level of less than 0.00305% (-90dB), the percent resolution of the converter. Most commercially available function generators have sine wave outputs with distortion levels of -40dBc to -70dBc. The function generator available for work presented in this thesis was the Hewlett-Packard 3325A. The operator's manual states that the harmonic distortion is less than -65dBc and spurious signals are less than -70dBc.

The method used to lower the distortion and noise levels was to band-pass filter the output of the 3325A. The maximum frequency of interest for the data acquisition system was 45Hz. Thus, a band-pass filter with a center frequency of 45Hz was developed. Since some tests required the use of a dc offset, a low-pass filter with a cut-off frequency of 45Hz was also developed.

In order to verify the distortion specifications of the 3325A, the sine wave output was characterized at 45Hz using a Hewlett-Packard 3561A Signal Analyzer. The result is shown in Figure D-1. The amplitude of the fundamental was 6.47dBV (5.96V

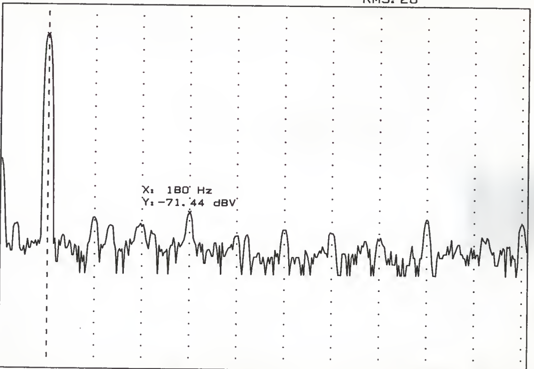


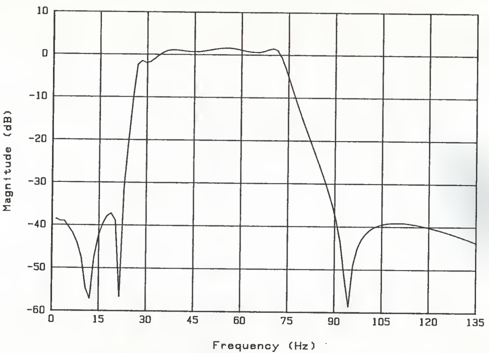
Figure D-1. Output Spectrum of HP-3325A Function Generator

peak-to-peak). The highest harmonic occurs at -71.44dBV, 77.91dB below the fundamental.

It was desired that all harmonics be -110dBc. Thus the filter must have an attenuation greater than 30dB at the second harmonic, 90Hz. An elliptic response was chosen because of its rapid fall-off in the transition band. This advantage comes at the expense of ripples in the passband and stopband. Since only one frequency passes through the filter, the ripple in the passband is of no significance. The ripple in the stopband is limited to be less than -30dB.

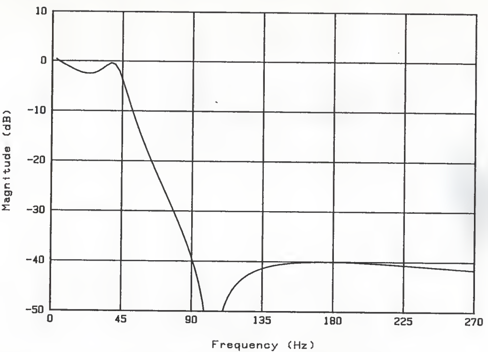
Using Reference 9 as a guide, an 8-pole band-pass elliptic filter was designed with a center frequency of 45Hz, a Q of 1, a passband ripple width of 1.0 dB, and a minimum stopband loss of 40dB. The frequency response is shown in Figure D-2. At 90dB, the second harmonic, the gain is -37dB. All other harmonics will be attenuated by at least 40dB.

Also using Reference 9 as a guide, a 3-pole low-pass elliptic filter was designed with a cut-off frequency of 45Hz, a passband ripple width of 3dB, and a minimum stopband loss of 40dB. The response is shown in Figure D-3. The gain at 90dB is -40dB. Note that the gain at 45Hz is -3dB, thus the attenuation is 37dB. The filter was designed with the attenuation of 3dB at 45Hz because this allows for maximum attenuation of the second harmonic from the fundamental; it makes maximum use of the rapid drop-off in the transition band. Note that in Figure D-1 there is a 15Hz signal with a significant amplitude which will not be filtered by the low-pass filter.



Band-pass Elliptic Filter Response

Figure D-2. Band-pass Filter



Low-pass Elliptic Filter Response

Figure D-3. Low-pass Filter

In implementing the above filters, the biquad band-pass filter circuit of Reference 9 was used. It was chosen because of its excellent stability and its relative ease in cascading several circuits to obtain higher-order filters. The Precision Monolithics OP-01 operational amplifier was chosen for its speed and its high open-loop gain (which makes for low distortion). Polystyrene capacitors and 1% metal film resistors were chosen for their excellent analog qualities.

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TECHNIQUES FOR TESTING A 15-BIT DATA ACQUISITION SYSTEM

by

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Abstract

This thesis discusses techniques for testing a low-power data acquisition system (DAS). The system resolution is 15-bits, sampling frequency is 128Hz, input range is ±5V, and the maximum input frequency is 45Hz. Techniques considered are those which lend themselves to an automated test, a test which is under computer control and which presents a numerical and/or graphical result. Static and dynamic test procedures are considered in testing a digital-to-analog converter (DAC) and an analog-to-digital converter (ADC).

The direct method of static testing DACs was found to be satisfactory for testing the 14-bit DAC used in the system. The DAC-to-ADC loop method using the histogram procedure is the best static test for the DAS; this procedure provides a good estimate of the transition voltages in the presence of noise and is easy to implement. Dynamic testing of the DAS involved two techniques; the histogram method was found to be best for estimating the differential linearity, and the Fourier transform method was found to be best for estimating the integral linearity. A third technique, the sine fit method, was used to give an overall indication of the system's performance.