

SOME CONSIDERATIONS IN THE DESIGN OF A
LOW-POWER, 15-BIT, ANALOG-TO-DIGITAL CONVERTER

by

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CHAPTER I
INTRODUCTION

The development of new devices which must be powered by batteries has given rise to demands for low-power A-D converters. Such demands may be met in a variety of ways, but when continuous conversion is not a requirement, one technique lends itself particularly well to the design of low-power A-D converters, and that technique is power switching. In this instance, where only two conversions are required every $1/128$ of a second, it seems evident that the design of a relatively high-speed system that could be operated at a low duty-cycle stands a good chance of making real savings in power, as long as the components used in the construction of the device, which would have to be significantly faster in terms of settling-time or slewing-rate than most of the ordinary low-power chips, do not use proportionately more power. This concept resulted in a long-term search for just such components, fast, with rapid settling times and which did not use so much power that when used in a low-duty cycle application, no advantage was gained. A myriad of calculations and design and re-design were required in order to reduce the power that the A-D converter used to a minimum.

The following chapters describe the final results of the above design process, and the means whereby the specifications were met in the development of a low-power 15-bit successive approximation A-D converter. In addition, the method of testing for power consumption and the static tests used to determine linearity are described.

CHAPTER II

CIRCUIT DESCRIPTION AND REQUIREMENTS

2.1 Initial Design Requirements

The initial design requirements for the low-power, 15-bit ADC were:

- i.) conversion by successive approximation
- ii.) bipolar 15-bit conversion
- iii.) differential linearity error of $\pm 1/2$ LSB max.
- iv.) integral linearity error of ± 1 LSB max.
- v.) no missing codes (either through logic or integral linearity error)
- vi.) input voltage range from + 5 V to - 5 V.
- vii.) maximum input frequency of 45 Hz
- viii.) conversion from two channels of data
- ix.) two conversions (one per channel) every 1/128 sec.
- x.) two's-complement form output from logic section
- xi.) microprocessor control
- xii.) supply voltages of ± 7.5 VDC
- xiii.) power consumption of less than 80 mW (analog section)

2.1.1 Applicability of Design Requirements to Analog Section

Of the above requirements, only (i.) through (vi.), (xii.) and (xiii.) apply to further discussion, since this thesis only treats the analog section of the ADC, excluding the sample-and-hold section. Since the requirements (vii.) through (ix.) are fundamentally dynamic performance requirements, they apply only to the sample-and-hold section, while requirements (x.) and (xi.)

apply only to the logic and microprocessor section.

2.1.2 Additional Design Requirements

In addition, it was desired that there be as few adjustments to the device as possible.

2.2 Design Philosophy

2.2.1 Power Reduction

Briefly, power reduction is accomplished by performing all conversions as quickly as possible.

A low-duty cycle of operation is essential to power reduction in this design.

By careful calculation, devices may be found whose speed and power consumption will result in an optimal design.

2.2.2 Microprocessor and Control Logic

A low-power microprocessor and control logic section that operates continuously controls all timing and all operations, including the successive-approximation A-D conversion.

2.2.3 Approach to A-D Conversion

A two-channel sample-and-hold section supplies held data from either one of the two channels to the ADC section.

Since any voltage may be represented by a sign and a magnitude, analog-to-digital conversion is carried out by a sign determination followed by a magnitude conversion. The magnitude conversion is accomplished by successive-approximation in either the positive or negative voltage range.

Whether the conversion is carried out in the positive or negative range is determined by the sign.

This is an optimal algorithm for use with the low-power

14-bit DAC, DAC-HA-14B.

2.3 The Circuit and a Description of Operation

2.3.1 The Circuit

The design is shown in the block and circuit diagram.

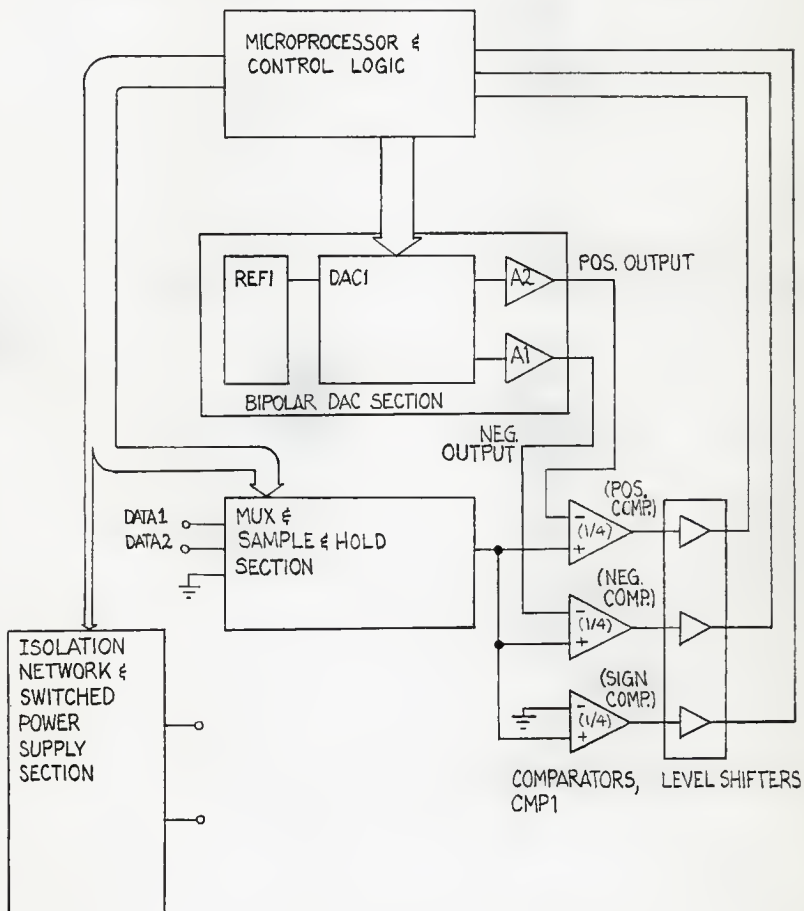
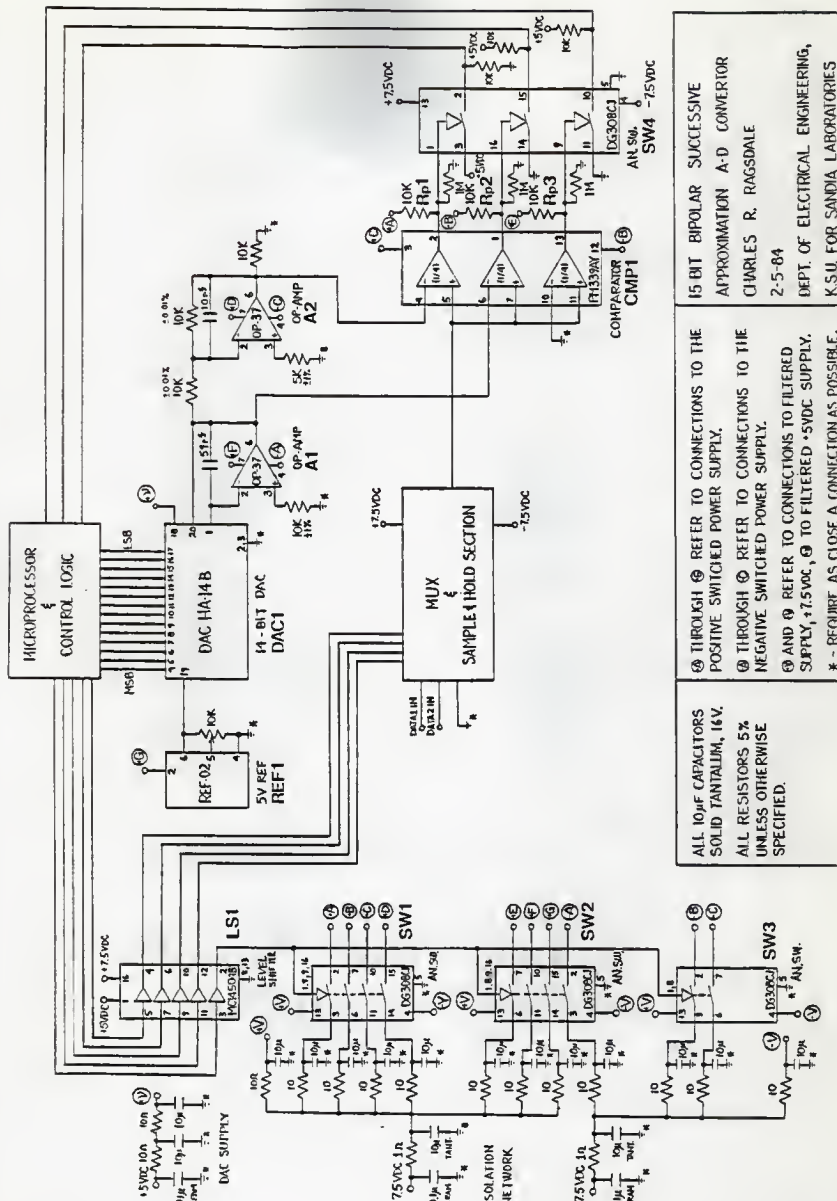


Fig. 2.1. Block diagram



ALL 10µF CAPACITORS SOLID TANTALUM, 16V. ALL RESISTORS 5% UNLESS OTHERWISE SPECIFIED.

⊕ THROUGH ⊕ REFER TO CONNECTIONS TO POSITIVE SWITCHED POWER SUPPLY.
 ⊙ THROUGH ⊙ REFER TO CONNECTIONS TO NEGATIVE SWITCHED POWER SUPPLY.
 ⊕ AND ⊙ REFER TO CONNECTIONS TO FILTERED SUPPLY, +7.5VDC, ⊕ TO FILTERED +5VDC SUPPLY.
 * - REQUIRE AS CLOSE A CONNECTION AS POSSIBLE.

15 BIT BIPOLAR SUCCESSIVE APPROXIMATION A-D CONVERTER
 CHARLES R. RAGSDALE
 2-5-84
 DEPT. OF ELECTRICAL ENGINEERING,
 K.S.U. FOR SANDIA LABORATORIES

Fig. 2.2. Circuit diagram

2.3.2 Description of Operation

The basic sequence of operations required to perform 15-bit conversions on both channels may be described as follows:

When conversion is desired, the microprocessor and control logic section turns on the analog switches S1 through S3 to supply power to the components in the analog section (the REF1, A1, A2 and CMP1). The sample-and-hold section remains on continuously. Then:

a) The sample-and-hold section provides a held data voltage from Channel 1.

b) The analog section performs a 15-bit conversion in sign-magnitude form on the held data voltage. The most significant bit represents sign, while the remaining 14-bits represent the magnitude of the voltage.

c) The microprocessor and control logic convert the results into two's-complement binary representation, which is stored into registers for final access.

d) The above process is repeated for Channel 2.

After these processes are completed, the microprocessor turns off the analog switches SW1 through SW3, shutting power off to the analog components.

The sections below describe the analog section's performance of one complete conversion and the timing scheme used to perform both conversions.

2.3.2.1 The Analog Section and the Performance of One Conversion

Since any DC voltage may be represented by a sign and a magnitude, the analog section of the converter is designed to

make a bipolar 15-bit conversion by first determining the sign, then the magnitude, of the held data voltage.

2.3.2.1.1. Sign

The sign, the most significant bit, is determined by means of one of the comparators in the quad comparator package CMP1 (either a PM339AY or CMP-04 quad comparator), by a comparison of the held data voltage to ground. (See block diagram on p. 4.)

Determination of sign is allowed 10 microseconds for completion.

The value of the sign bit determines whether the logic section takes its data for the magnitude from the positive or negative voltage region, as described below.

2.3.2.1.2 Magnitude

The remaining 14 bits of the 15-bit conversion represent the magnitude of the held data voltage.

These 14 remaining bits are determined by 14-bit successive-approximation conversion in either the positive half (from + 5 V to 0 V) or in the negative half (0 V to - 5 V) of the full scale voltage range.

2.3.2.1.2a Conversion in the Negative Voltage Range

The 14-bit successive-approximation conversions in the negative voltage range are accomplished by comparison of the output of A1 to the held data voltage.

The operational amplifier A1 (OP-37EZ) is the inverting output of DAC1 (DAC-HA-14B), which has a positive 5 V reference voltage input from REF1 (REF-02). Consequently, the voltage output of A1 lies in the negative voltage range.

The comparisons required for successive approximation in the

negative voltage range are accomplished by a separate comparator in CMP1 (the PM339AY or CMP-04 quad comparator), which is followed by an inverting level shifter in SW4 to convert the output to positive-true logic. (See block diagram, p. 4.)

Successive approximation in the negative voltage range follows standard procedure for the successive-approximation process in general, with the 14-bit DAC used for DAC1 providing voltage increments from 2.5 V, initially, down to 305.2 microvolts, corresponding to 1 LSB.

Conversion occurs at the rate of 1 bit per 10 microseconds.

2.3.2.1.2b Conversion in the Positive Voltage Range

The 14-bit successive-approximation conversions in the positive voltage range are accomplished by comparison of the output of A2 to the held data voltage.

The operational amplifier A2 (OP-37EZ) is the inverted output of A1, placing this output in the positive voltage range.

The required comparisons for successive-approximation in the positive voltage range are accomplished by another separate comparator in CMP1, followed by a non-inverting level shifter in SW4 to provide output in positive-true logic form.

Successive approximation proceeds as described above, with a rate of 1 bit per 10 microseconds.

2.3.2.2 Power Switching and Timing

With regard to power switching and timing, the circuit was designed to require only 10 microseconds of warm-up time before the initial conversion cycle can begin. During this time, the held data from Channel 1 is allowed to settle.

The optimum timing scheme is shown in Fig. 2.3.

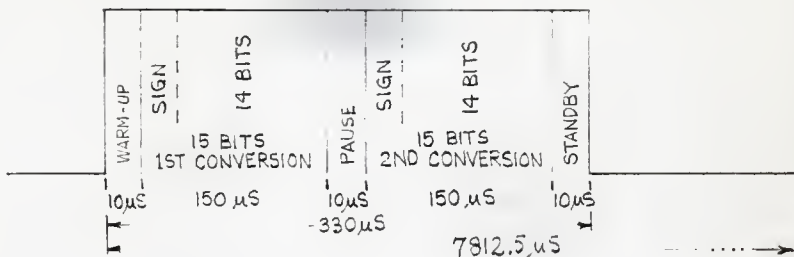


Fig. 2.3. Optimum timing scheme

The 10 microsecond pause after the first conversion allows time for the analog switches from the 2-channel sample-and-hold section to change from Channel 1 to Channel 2 and allow the data voltage output of the analog switches to settle.

The 10 microsecond delay following the second conversion is merely standby time allowed before turning off power, and is not absolutely necessary in this design.

The total "on" time is 330 microseconds out of 7812.5 microseconds (1/128-th seconds), which represents a duty cycle of only 4.224 %. From this, it is clear that the device will only use 4.224 % of the power it would consume if it were on continuously. This would be the most ideal timing scheme for the device, but in practice, this is limited by the microprocessor and control logic.

The timing schemes used for the linearity measurement and power measurement had "on" times of 365 microseconds and 360 microseconds, respectively.

The warm-up time allowed for the differential linearity

error measurement was limited to 10 microseconds, since it is necessary to demonstrate that 10 microseconds is sufficient warm-up time for conversion, while 20 microseconds is allowed for warm-up for the power measurement.

The only other differences are that more time was allowed after conversion for processor and control logic operations.

2.4 Demonstration of Circuit Performance

The figures below demonstrate the basic operation of the circuit, showing the successive approximation process performed in the positive voltage range, the negative voltage range, and the operation of the circuit with the power supply switched as previously described.

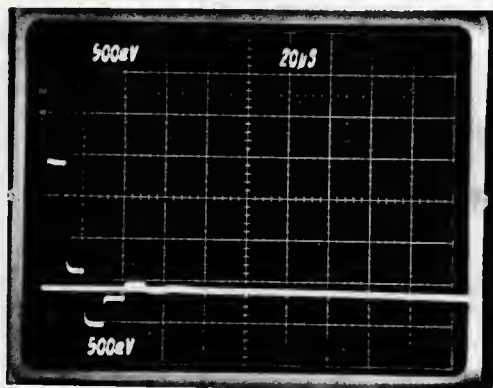


Fig. 2.4. Successive approximation occurring in the positive voltage range.

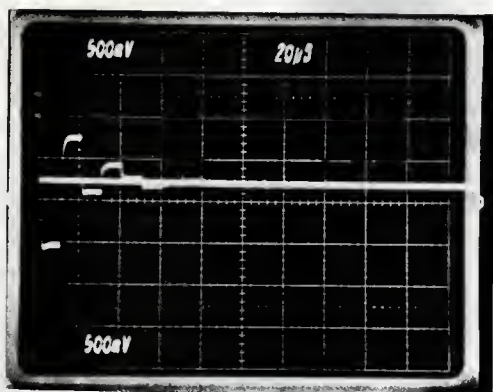


Fig. 2.5. Successive approximation occurring in the negative voltage range.

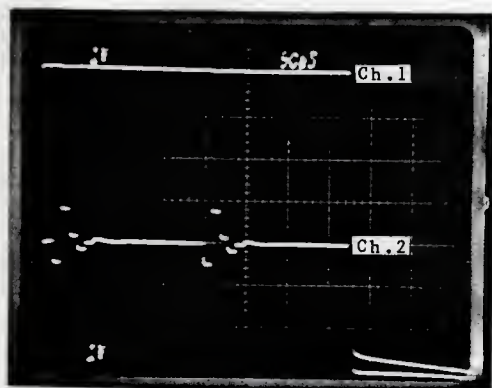


Fig. 2.6. Conversion of both channels under switched power supply conditions. Ch. 1.: Switched positive power supply to A1. Ch. 2.: Output of A1 during conversion of 3 V input data voltage (applied to both channels).

CHAPTER III
SOME CONSIDERATIONS IN THE DESIGN OF THE
LOW-POWER ADC AND VERIFICATION

3.1 General Considerations

Some of the major considerations in the design of the low-power, 15-bit, successive approximation ADC were power consumption, linearity and resolution. In order to design a system meeting the requirements, many additional effects, such as settling time, had to be taken into consideration as well.

As a result of these considerations, the following components were chosen based on the criteria given:

a) The REF-02, which supplies a 5 V reference voltage to the 14-bit DAC, was chosen for low power consumption and rapid turn-on settling time.

b) The DAC-HA-14B, the 14-bit DAC, was chosen for very low power consumption, rapid settling time to within $\pm 1/2$ bit, and tolerance of wide supply voltage ranges.

c) The OP-37EZ precision operational amplifiers, used as DAC-followers A1 and A2, supply the voltages for successive-approximation conversion in the negative and positive voltage ranges respectively. These amplifiers were chosen for relatively low power consumption, high gain, high gain-bandwidth product, high slew rate, rapid settling time, (and, theoretically, rapid settling time after turn-on), as well as very low offset voltages and currents, a characteristic that is of great importance.

d) The PM339AY or CMP-04 quad comparator, used to make all voltage comparisons for successive approximation and sign

determination, was chosen for low power consumption, high gain (hence high resolution), high CMRR, rapid small-signal response time (and, again, theoretically, rapid settling after turn-on).

e) The DG308CJ analog switches, which were used either as low-power level shifters (SW4), or as power supply switches (SW1 through SW3), were picked for their extremely low quiescent power consumption and low "on" resistance and high isolation when "off".

For specifications for these devices, see Appendix A.

Some of the many design considerations essential to the proper operation of the circuit as a low-power, 15-bit, ADC are given below:

3.2. Power Consumption

For those devices being power switched, upper bounds for average power consumption were computed by estimating an upper bound on power consumption as if all the devices were on continuously, then multiplying this result by the fractional duty cycle.

The fractional duty cycle is simply the fraction of time the device is on to the total period of the cycle.

Values for upper bounds on the average power consumption were computed from the specifications for both typical power consumption and maximum power consumption for the loading conditions used in the circuit.

Details of the exact method by which power was estimated for each device are given in Appendix B.

The total average power computed for typical and maximum

cases are given below. These values were computed for "on" times of 330 microseconds and 360 microseconds.

Table 3.1. Expected Power Consumption

For 330 μ S. "on" time, (4.224% duty cycle),

$$P_{d,total,avg,typ} = 8.345 \text{ mW.}$$

$$P_{d,total,avg,max} = 15.550 \text{ mW.}$$

For 360 μ S. "on" time, (4.608% duty cycle),

$$P_{d,total,avg,typ} = 9.105 \text{ mW.}$$

$$P_{d,total,avg,max} = 16.418 \text{ mw.}$$

Verification of these values is given in Chapter V, since power consumption falls within the purview of the specifications for the device.

3.3 Warm-up or Turn-on Time

Another important parameter requiring consideration in the design, the warm-up or turn-on time, was estimated for each device by the techniques described in more complete detail in Appendix B, Section B.3.

The estimated and measured values for the turn-on time for each device are given below.

All were estimated to have warm-up times of less than 10 microseconds, which is the allotted time, and were chosen as components partly on this basis.

Given below is a table of the estimated and measured turn-on times for the various components.

Table 3.2. Turn-on Times for Components, Estimated and Measured.

Component	Estimated t_{on}	Measured t_{on}
REF1 (REF-02)	~ 7.52 μ S.	~ 3 μ S.
A1 (OP-37EZ)	~ 0.5 μ S.	~ 8 μ S.
A2 (OP-37EZ)	~ 0.5 μ S.	~ 8 μ S.
CMP1 (PM339AY)	~ 2.1 μ S.	~ 3.9 μ S.

The values given as measured values for the turn-on times for each component really only represent the minimum possible values for the turn-on time.

These values were obtained by observing the output of the device after turn-on on an oscilloscope, and measuring the time required for the device to settle to within measurable limits (in this case, within approximately 1% to 2%, the limitations on the resolution of the oscilloscope). Hence, the measured turn-on times as specified in the above table only represent gross approximations.

Without a very high resolution sampling oscilloscope, it would be very difficult to correctly measure this parameter. The best indicator for whether or not 10 microseconds is sufficient turn-on time is the performance of the device itself.

In the figures shown below are the oscilloscope traces of the actual turn-on transient response for each of the devices listed in Table 3.2.

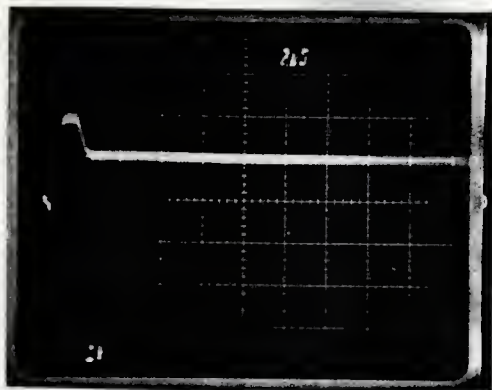


Fig. 3.1. Turn-on transient response, REF1 (REF-02).

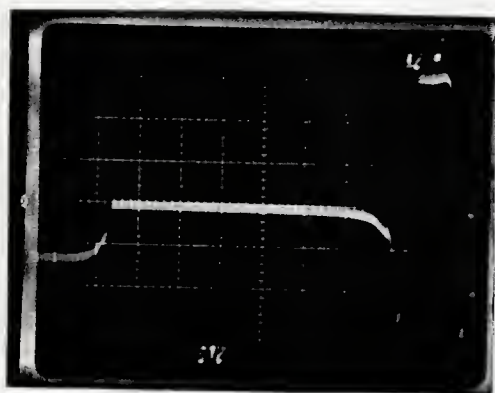


Fig. 3.2. Turn-on transient response, A1, A2 (OP-37EZ). Note the relatively long transient oscillatory response ($\sim 4 \mu\text{S.}$) followed by settling time.

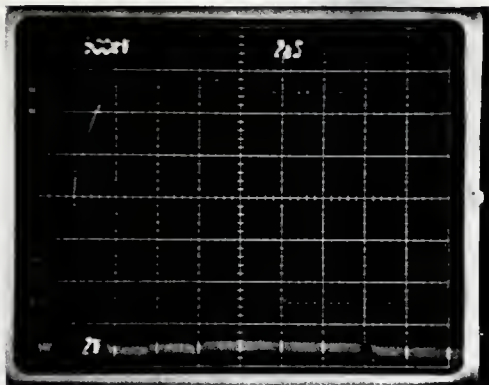


Fig. 3.3. Turn-on transient response, CMP1 (PM339AY).

The device that deviated the most from expected values was the OP-37EZ, which had been expected to settle within half a microsecond. While the device was expected to have an oscillatory period following turn-on, there was nothing within the specifications to indicate that this transient oscillatory response would be so long in duration. Most of the other devices were reasonably close to their expected values.

The probable cause of this discrepancy is the input capacitance to the first DAC-follower, A1, which is expected to be ~ 260 pf. This lengthens the measurement settling time, as described in Appendix B, Section B.4, and probably the turn-on settling time as well. A better estimate would be a settling time of ~ 5.94 microseconds, (see Table B.2).

3.4 Measurement Settling Time

Another of the most important parameters to be considered

was the measurement settling time, that is, the time required by the entire device to measure to within $\pm 1/2$ LSB., or 1 part in 2^{15} .

An approximate analysis (see Appendix B) yields an expected measurement settling time of roughly 9.1 microseconds per bit.

In the estimate, the DAC-HA-14B requires 7 microseconds for the current to settle to within 1 part in 2^{15} , while the comparator requires ~ 2.1 microseconds to respond to a transition of approximately $1/2$ LSB.

We wish to adhere to this settling time schedule as closely as possible, which requires a very detailed analysis of the circuit to insure proper settling of the DAC and DAC-followers.

Due to the output capacitance of the DAC-HA-14B, the output of the first DAC-follower, A1, has a significant 2-pole response to any input.

The settling time and damping factor for the DAC-followers are controlled by the value of the feedback capacitor, C_f , for each of the op-amps.

The detailed calculations required to estimate the best possible value and allowed values for these capacitors are given in Appendix B.

Given in the table below are the estimated and measured values for the damping factor and settling time to within 1 part in 2^{15} for given values of feedback capacitor, C_f , for the first DAC-follower, A1.

Table 3.3. Expected and Measured Values of Damping Factor, n , as a Function of Feedback Capacitor, C_f .

C_f	n , Expected	n , Measured
0.0 pf	0.0	0.0
5.0 pf	0.249	0.06
11.0 pf	0.543	0.11
21.0 pf	1.018	0.56
46.0 pf	2.136	> 1.0
59.0 pf	2.683	> 1.0

In the figures shown below, we see the actual response (approximately 2-pole) to two consecutive step inputs, the first being a step input of 2.5 V, the second being an input of an additional 1.25 V, output from the DAC-HA-14B, for differing values of C_f .

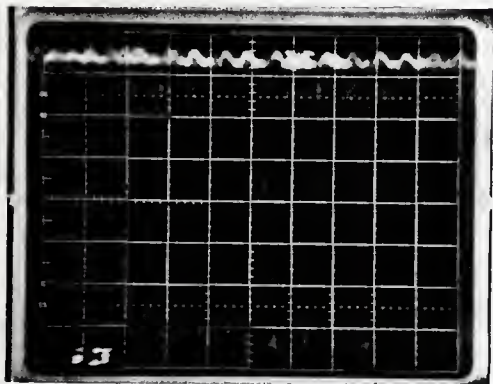


Fig. 3.4. The 2-pole response of A1 to two consecutive step inputs. $C_f=0$. $n=0$.

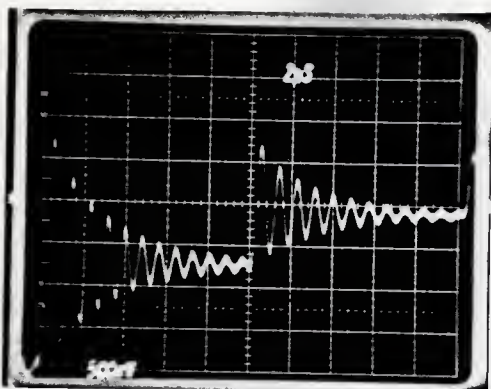


Fig 3.5. $C_f=5.0$ pf.
 $n \approx 0.06$.

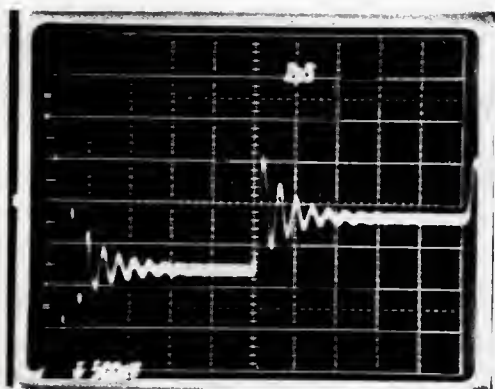


Fig. 3.6. $C_f=11$ pf.
 $n \approx 0.11$.

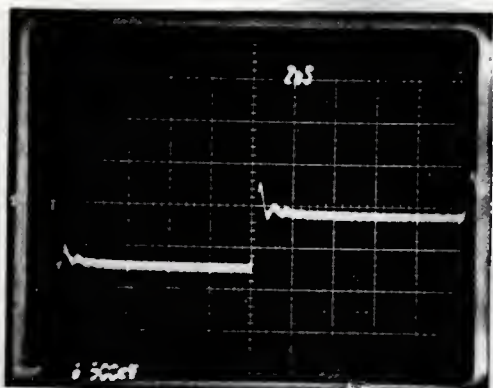


Fig. 3.7. $C_f=21$ pf.
 $n \approx 0.56$.

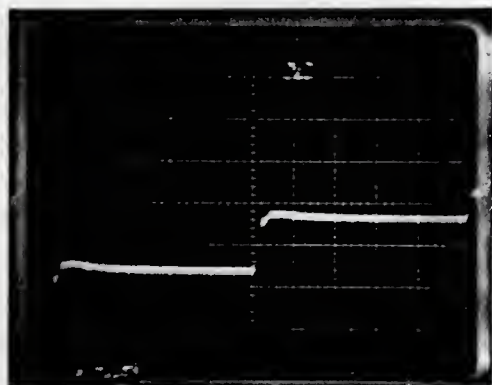


Fig. 3.8. $C_f=46$ pf.
 $n \approx 1.0$.

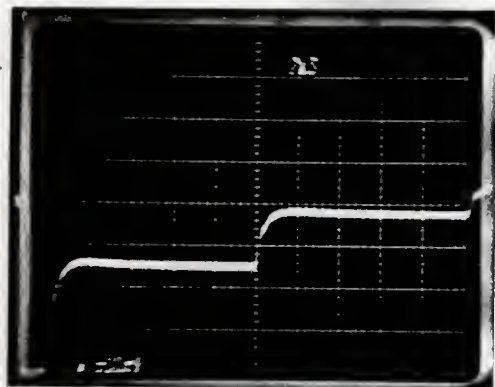


Fig. 3.9. $C_f=59$ pf.
 $n>1.0$.

The calculations explained in Appendix B accurately predict the fact that an input capacitance to the operational amplifier (in this case, the output capacitance of the DAC-HA-14B) will result in a 2-pole response to a step voltage.

Furthermore, they accurately predict the trend for the damping factor to increase when the value of the feedback capacitor C_f increases, but numerically, the results tend to differ, due possibly to any of several factors, the most important of which are the difference of the output capacitance of the DAC-HA-14B from specified values, the difference in the gain-bandwidth-product of the op-amp from specified values and the existence of higher order poles at high frequencies in the open-loop response of the op-amp (not taken into account in the equations), and stray, or parasitic, capacitance.

The value chosen for C_f for the first op-amp, A1, of 59 pf,

reflects a choice based on both the estimated and measured values for damping factor and settling time. This value of C_f falls within the acceptable range to get less than 7 microseconds settling time in both cases, while being greater than that required for the fastest settling time, which occurs when the damping factor is much closer to unity.

The choice of C_f to give a damping factor greater than unity adds considerably to noise reduction, since the circuit configuration is basically that for a low-pass active filter (see the circuit diagram on p. 5). A large value for C_f reduces the bandwidth of the filter.

3.5 Comparator Resolution and CMRR

Another important consideration to the design is the comparator resolution.

It is desirable for the gain of the comparator to be as high as possible, so that it can discriminate very small changes in voltage, and it is desirable for the CMRR of the comparator to be as high as possible.

For the comparator to perform properly, it must, as a minimum, be able to adequately resolve a voltage increment of $1/2$ LSB, or 152.6 microvolts out of 5 V, amounting to 1 part in 2^{15} .

Therefore, assuming that we desire an output voltage swing of approximately 10 V for the level shifter to register a logic change from "0" to "1", the gain of the comparator must be greater than 65,536 and the CMRR must be greater than 90.3 dB.

The comparator CMP-04 has, typically, a gain of 200,000, a

CMRR of 100 dB, and a minimum gain of 80,000 and a minimum CMRR of 80 dB. This implies that, generally, the comparator CMP-04 will meet specifications. However, some particular comparators may not.

No values for CMRR were found for the PM339AY, but it is assumed that they are approximately the same as for the CMP-04, since almost all other specifications were the same. The typical value for gain for the PM339AY was the same as for the CMP-04, but the minimum gain was given as 50,000, thereby making the CMP-04 preferred, since in all other important areas the specifications were the same.

Since some comparators may not meet specifications, some screening may be required for comparators used in the circuit.

No other comparator was found that could meet power and settling time specifications and which possessed a minimum CMRR greater than 90 dB.

It should be noted that a CMRR as low as 84.3 dB could actually be considered to be the minimum acceptable criterion with regard to comparator CMRR, since it would only result in 1 bit of error out of 5 V in either the positive or negative voltage range. Note that this value is very close to the minimum specification for the CMP-04.

Since the typical differential linearity error for the 14-bit DAC (the DAC-HA-14B) is $\pm 1/2$ LSB, or, in our case, ± 152.6 microvolts, it is clear that the inclusion of the error incurred by the comparator in our overall linearity error estimations will never result in a net worst case differential linearity error of less than $\pm 1/2$ LSB.

This implies that it would be desirable to find a 14-bit DAC with greater resolution, or find a 15 or 16-bit DAC with characteristics similar to the DAC-HA-14B. However, no DAC was found that had anywhere near the low power consumption characteristics possessed by the DAC-HA-14B which could be operated from a 7.5 VDC supply, or which could be power switched.

Assuming the use of the comparator CMP-04 in the circuit, the typical value for the differential linearity error was estimated to be 160 microvolts, or .524 LSB, while in the absolute worst case, the differential linearity error was estimated to be 197 microvolts, or .645 LSB. No missing bits should occur for a differential linearity error of less than 1 bit.

3.6 Noise

With regard to noise, the largest effect to be taken into account, from a theoretical standpoint, would be the noise from the sample-and-hold input to the comparators, which was given to be approximately 50 microvolts p-p. [1].

The next-to-largest effect would result from power supply ripple due to the discharge of the capacitors of the isolation network through the analog switches when turned on, and would amount to an estimated value of 41.2 microvolts. The noise supplied by the DAC-followers themselves would amount to no more than 1.5 microvolts p-p.

The largest supply of noise could realistically be expected to come from the digital section containing the microprocessor and control logic, and from cross-talk between the analog components, all of which the isolation network, to be described

later, was designed to prevent.

However, nothing can prevent some noise from leaking through to the analog section by means of stray capacitance and line inductance. There is no way precisely to predetermine this amount.

Most of this can be eliminated by proper board layout, spacing the digital section as far from the analog section as possible and making sure that the analog ground points are as close together as possible.

Since the quantity of noise leaking through from the digital to analog section may not be predetermined, we will omit this from our calculations. The net resulting noise was calculated to be 51 microvolts p-p.

3.7 Isolation Network

It can be considered that noise coming from the digital control logic (external noise), and noise coming from the operation of the analog components (which we will consider "internal noise") both have a fundamental harmonic at 100 kHz, due to the fact that all major transitions occur in 10 microsecond intervals. An isolation network was designed to eliminate as much noise from both sources as possible, by placing two poles of a low pass filter from the external power supply to each device, and placing three poles of a low pass filter between each analog device, as shown in the circuit diagram (p. 5).

The resulting isolation, at 100 kHz, was determined, and is listed in the table below.

Table 3.4 Isolation at 100 kHz Due to Isolation Network.

Isolation, external: -52.2 dB

Isolation, internal: -128.2 dB

The Bodé plots for the isolation network are given on the following pages.

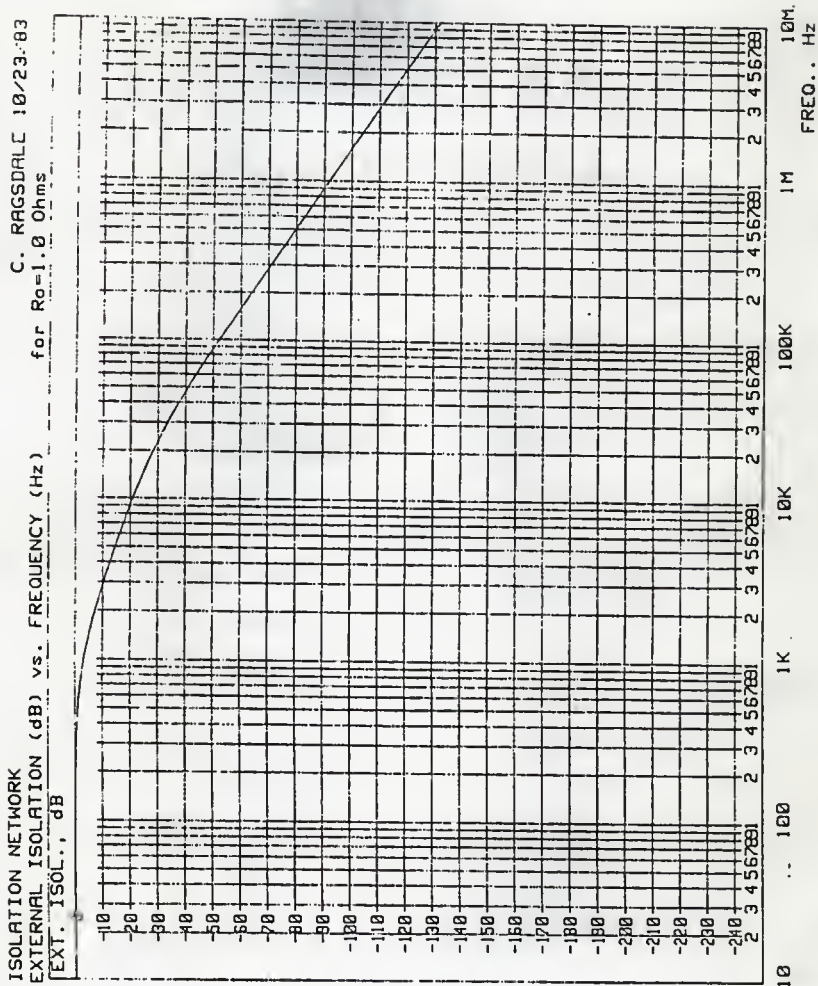


Fig. 3.10 External Isolation, Bode Plot

C. RAGSDALE 10/23/83

ISOLATION NETWORK
ISOLATION (dB) vs. FREQUENCY (Hz) for $R_0=1.0$ Ohms

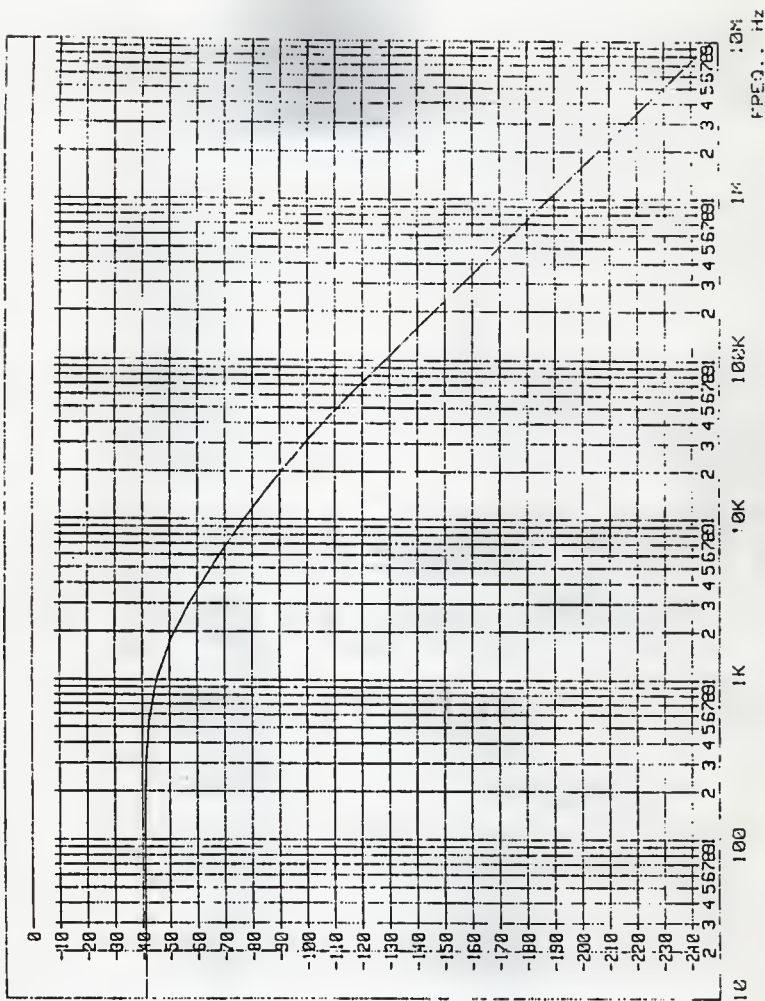


Fig. 3.11 Internal Isolation, Bode Plot

3.8 Miscellaneous Sources of Error

It is necessary to take several miscellaneous sources of error into account in this design.

While most of the effects turn out to be negligible, it is first necessary to show that they are negligible in order to insure that the design is workable.

Some of the sources of error taken into consideration are the effect of the supply voltage ripple produced by fluctuations in supply current due to the operation of an active device through an analog switch, the supply voltage ripple caused by the discharge of the isolation network capacitors through the circuit components when the analog switches supplying current are turned on, the effect of the offset voltage of the DAC-followers, the effect of the bias current of the DAC-followers, and the effect of the offset voltage for the comparators.

3.8.1 Supply Voltage Ripple Due to Operation of Active Device through Analog Switch "On" Resistance

With regard to the effect of supply voltage ripple produced by the fluctuation of supply current due to the operation of an active device through the analog switch, the most critical case of this occurs for the DAC-followers.

The active operation of the OP-37EZ, in the process of putting out voltages ranging from 0 V to 5 V, given the loading conditions shown in the circuit diagram on p. 5, will pull an additional 0 mA to 1 mA of current through the "on" resistance of the analog switch, where R_{on} is estimated to be $\sim 100 \text{ Ohms}$ for the DG308CJ Analog Switch. This will result in a voltage drop across the analog switch of $\sim 0 \text{ V}$ to $\sim 0.1 \text{ V}$. This supply voltage

ripple will, in turn, result in a small change in the output voltage of the OP-37.

It was calculated, however (see Appendix B) that by the time the output of the DAC-follower had settled to within 1 part in 2^{15} , that the resulting change in the output voltage would only be affected by approximately 0.2 microvolts, an insignificant amount. This is due to the high PSRR of the OP-37, which is on the order of 120 dB.

The existence of this ripple voltage is graphically demonstrated in the figure below.

This oscilloscope photograph was taken by allowing the power supply switches to remain constantly "on", and observing the trace of the supply voltage to the OP-37 on A-C coupling on channel 1, while showing the trace of the output of the OP-37 as the successive approximation is made to an input (data) voltage of 5 V on channel 2.

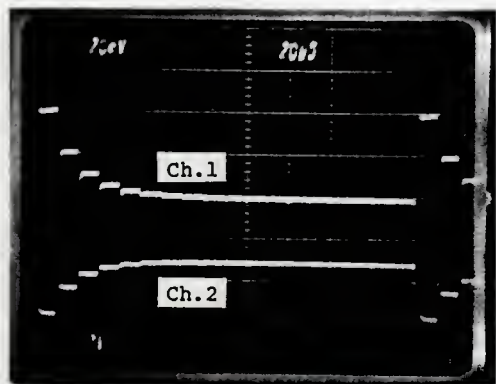


Fig. 3.12 Ch. 1:
Voltage drop across R_{ON} of analog switch due to "active" component of supply current. Channel #1 ground actually at +7.5 VDC due to A-C coupling. (20 mV/div)
Ch. 2: Output OP-37, for input of +5 V. (2 V/div).

Note that when the output of the DAC-follower has settled to 5 V, that the drop across R_{On} has settled to ~ 80 mV, reasonably close to the predicted value of 100 mV. The actual error produced by this ripple once the DAC-follower has settled should still be ~ 200 nV, as predicted.

3.8.2 Supply Voltage Ripple Due to Capacitor Discharge from Isolation Network

Due to the discharge of the capacitors in the isolation network through the switches to the circuit components when the switches are turned on, an exponential decrease with time should be experienced in the supply voltages to the circuit components, which will have an effect on their performance.

This effect will be the most critical with regard to the operation of the DAC-followers.

An analysis similar to that used to obtain results for the case given previously (where the supply voltage ripple was caused by the action of the active components) shows that, in this case, the worst case change in the output voltage with time would be ~ 41.7 microvolts. This will be considered to be part of the noise of the system.

3.8.3 Effect of Offset Voltage and Offset Current

One very important effect to take into account is the combined effect of the offset voltage and offset current of the operational amplifiers used as DAC-followers.

The final difference in output voltages between the two amplifiers due to internal offset voltage and offset current could result in either an overlap or a gap between the positive and negative voltage range.

In any case, the difference in the final offset voltage in outputs between the two amplifier stages should not exceed 1 bit, or an error would result.

If the offset resulted in an overlap between the two, an error would result for a voltage measured in either the positive or negative voltage range. This would be an error that could be corrected for by the microprocessor.

However, if the offset resulted in a gap of more than one bit, there would be a range between the positive and negative voltage ranges where no comparisons could be made. Any voltage to lying within this gap could not be measured and would be reported as either a positive or negative zero. This would not be a correctable error.

A complete calculation of the effect of offset voltage and offset current derived in Appendix B in Section B.7.3 and resulting in (Eq. B.54c) indicates that the best solution to this problem consists of matching the operational amplifiers A1 and A2 so that the offset voltages and currents are very nearly equal and that the offset currents for A1 and A2 do not exceed 15.2 nA. This should not be difficult, as the typical value for offset current in an OP-37EZ is approximately 7 nA.

Bias currents were corrected for in the usual manner by placing resistors between the positive terminal for the operational amplifiers and ground. For A1, the resistor value is 10 K, while for A2, the resistor value is 5 K.

3.8.4 Effect of the Offset of the Comparators and the Sample-and-Hold Section

The effect of the offset of the comparators, when connected as shown in the circuit diagram (p. 5), is simply that the held data voltage will appear to be offset by a fixed amount, typically on the order of 1 bit, assuming that each of the comparators in the comparator package has approximately the same offset. This is a reasonable assumption.

If the sample-and-hold section inputting the held data voltage has an offset (which may be different for each channel) the final result may be a different net offset for each of the two channels.

3.9. Summary

The most important considerations were power consumption, turn-on or warm-up time, measurement settling time, comparator resolution and CMRR, isolation from external noise and cross-talk provided by the isolation network, and, with regard to the performance of the circuit around 0 V, the relative offset of the DAC-followers A1 and A2, which is controlled by the offset voltage and offset current of each of the DAC-followers.

Many effects were predicted to be negligible, including the noise produced by the amplifiers, the effect on the output of the DAC-followers due to the ripple produced on the power supply produced by the operation of the op-amps through the "on" resistance of the switches and the ripple due to the discharge of the isolation network capacitors through the switches and circuit components when the switches are closed during "on" time. The offsets of the comparators and the offsets of the sample-and-hold will result in a net offset that may be different for each channel.

CHAPTER IV
TEST PROCEDURES FOR POWER AND
DIFFERENTIAL LINEARITY ERROR MEASUREMENT

The following is a brief summary of the test procedures that were applied to the low-power 15-bit successive approximation ADC.

4.1 Power Measurement

The power was measured using the true average power meter test circuit shown in Fig. 4.1. This test circuit was used in the automated system shown in Fig. 4.2, both of which are described in greater detail in Appendix C.

The true average power meter test circuit was designed to compute the average power to within $\sim \pm 1\%$ at DC and within a bandwidth of 4 decades from 10 Hz to 100 kHz from a measurement of the instantaneous voltage $v(t)$ and the instantaneous current $i(t)$ supplied to the device-under-test. The instantaneous current was measured by measuring the voltage drop across a 3 Ohm resistor placed in series with the current.

The true average power meter test circuit puts out a DC voltage proportional to the true average power to within $\pm 1\%$ (actually measured to be within $\sim .25\%$ typically), plus an additional error voltage produced by the relatively low (~ 80 dB) CMRR, and an additional error voltage produced by the offset of the operational amplifiers used. Both error voltages may be eliminated.

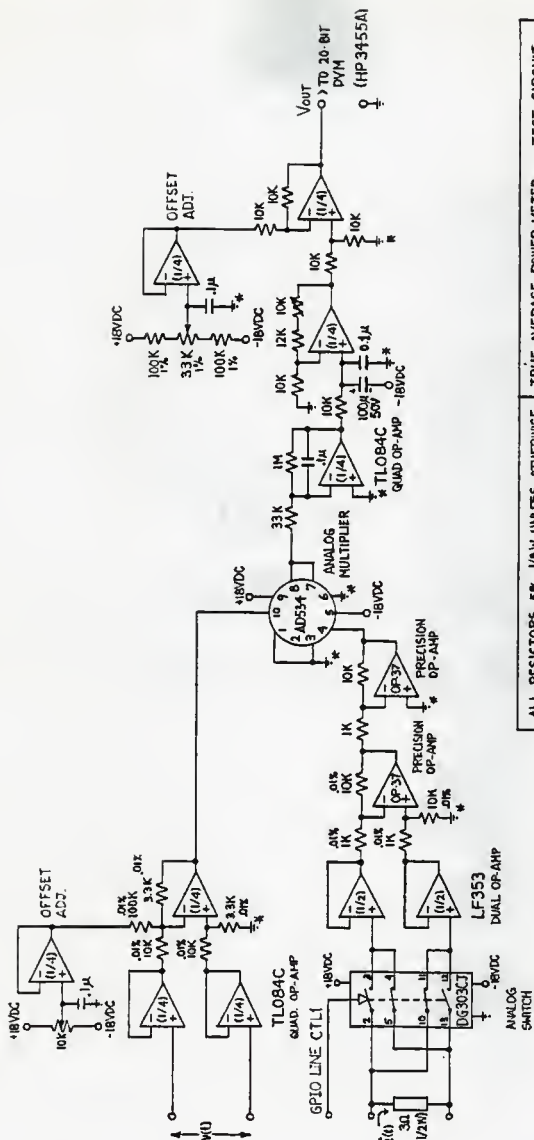
It is the function of the automated system to eliminate the errors produced by CMRR and offset by means of the analog switch

at the input to the current measuring section (see Fig. 4.1.), which it uses to reverse the leads to the input. The automated system reads the output voltage of the true average power meter using the HP3455A Digital Voltmeter, reverses the leads, takes a second reading, and the HP9845B Computer calculates the voltage difference and divides by two, thereby eliminating the effects of offset and CMRR (at low frequency, at least). The resulting voltage is proportional to the true average power.

To determine this constant of proportionality in this measurement, it is necessary to calibrate the device before taking measurements. This is done by using the A-C voltage measuring capability of the HP3455A Digital Voltmeter to accurately measure the RMS voltage of a sine wave supplied by the programmable HP3325A Synthesizer/ Function Generator to a known resistance. The HP9845B then computes the actual power used by this known resistance (in this case, a 10 K resistor) and then measures this power consumption with the true average power meter, using the method described previously, and computes the calibration factor.

In a full calibration, the device computes this calibration factor several times and takes the average calibration factor, which it uses in all subsequent measurements.

Each measurement then consists of an initial measurement using the true average power meter, followed by a reversal of leads to the current measuring section via the analog switch at the input, which is controlled by the HP9845B, and a second measurement to eliminate the effects of CMRR and amplifier offset, and a computation by the computer of the average power.



TRUE AVERAGE POWER METER — TEST CIRCUIT
 CHARLES R. RAGSDALE
 5-31-84
 DEPT. OF ELECTRICAL ENGINEERING
 K.S.U. FOR SANDIA LABORATORIES

ALL RESISTORS 5%, 1/8W UNLESS OTHERWISE SPECIFIED.
 1.0 μ F CAPACITORS ARE CERAMIC
 100 μ F CAPACITOR IS ELECTROLYTIC
 ALL POWER SUPPLIES $\pm 18VDC$

Fig. 4.1.

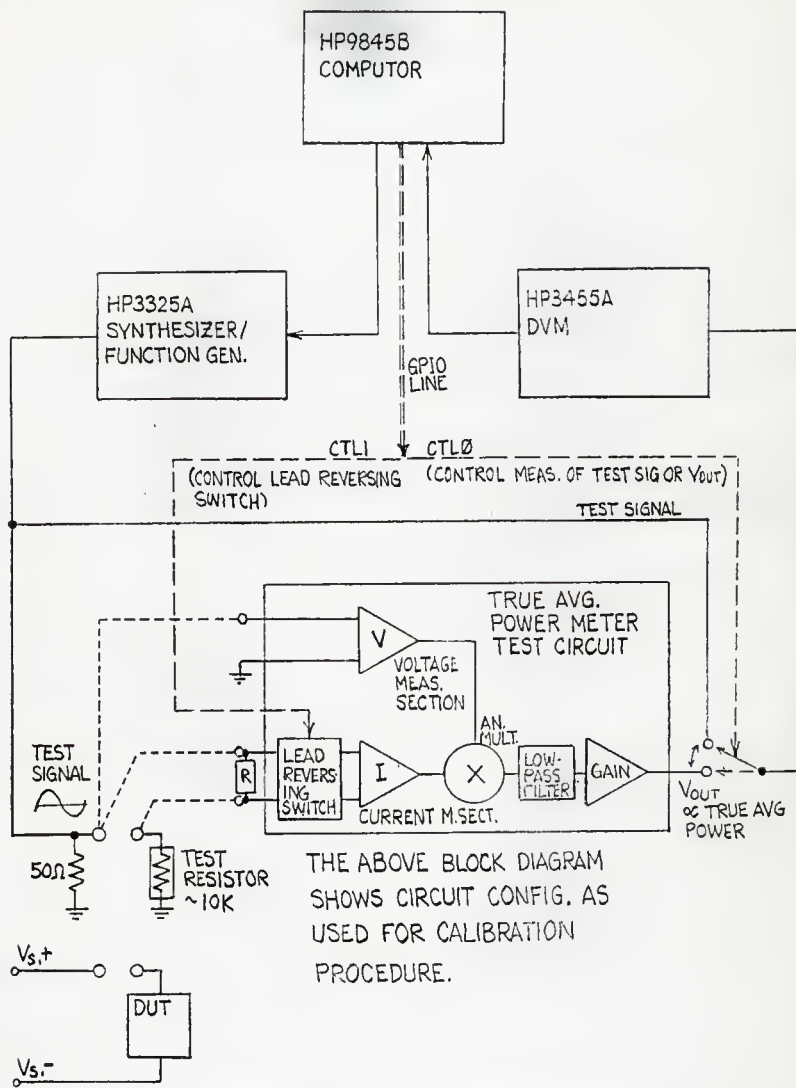


Fig. 4.2. Block diagram, automated test system

4.2 Differential Linearity Error Measurement

In order to make static measurements of the differential linearity error, it was first necessary to develop a device capable of putting out a voltage that could be regulated to within $\pm 1/2$ LSB.

The device used is the programmable reference voltage test circuit shown in Fig. 4.3, which is capable of being programmed by the HP9845B to supply any voltage within the range from + 5 VDC to - 5 VDC and regulating it to within ± 6 microvolts. This circuit is described in more detail in Appendix C.

The most essential part of the algorithm used to determine differential linearity error was, basically, to look for the voltage that would, when supplied to the 15-bit low power ADC under test, result in the output of a particular 15 bit binary code on the average, to within $\pm 1/8$ LSB.

It is necessary to consider the output binary code representations for a voltage as having average values, due to the existence of at least some finite amount of noise in the system.

The differential linearity error may then be determined from the input voltages required to give a particular output code.

The basic procedure used to measure differential linearity error is to look for the values of input voltages required to output a specific value of code on the average to within $\pm 1/8$ LSB, then decrement the desired output code and find the voltage required to output this code on the average to within $\pm 1/8$ LSB, and convert the input voltages to their corresponding number of bits by dividing by the voltage increment for 1 LSB, or 305.2 microvolts. The differential linearity error (see reference [2])

is then given by (Eq. 4.1) as:

$$\text{Diff. Lin. Err.} = |(V_i - V_{i-1}) - 1| \quad (\text{Eq. 4.1})$$

where V_i and V_{i-1} represent a voltage in bits for the i -th output code and $(i-1)$ -th output code respectively. Since the error associated with each V_i is $\pm 1/8$ LSB, the error associated with each differential linearity error measurement is inherently given by :

$$\begin{aligned} \text{Error, D.L.E.} &\sim (1/8) * 2^{1/2} \text{ LSB} && (\text{Eq. 4.2}) \\ &\sim 0.177 \text{ LSB} \end{aligned}$$

The algorithm used to compute the differential linearity error is given more exactly in Appendix C.

The number of data points for which the differential linearity error was measured and subsequently averaged was 497, with approximately 100 data points taken each for input voltage ranges close to + 5V (output codes 16383 to 16285), close to 2.5V (output codes 8242 to 8143), close to 0V (50 to -49), close to - 2.5V (-8142 to -8241), and close to - 5V (-16264 to -16383).

CHAPTER V
RESULTS AND MEASURED VALUES FOR POWER
AND DIFFERENTIAL LINEARITY ERROR

5.1 Power Measurement

For the power measurements, the table below itemizes for each component the average power measured, and provides a value for total average power consumed for the circuit. The test conditions under which the power consumption for the device was measured were an input (data) voltage of +5.00000 VDC to both channels, and power supply voltages of ± 7.5 VDC.

Table 5.1. Comparison of the Expected Values of Average Power to Measured Values. (% Error: measured value assumed accurate).

Component	P_d , Expected Value	P_d , Measured Value	% Error
Iso. Net. & SW1, SW2, SW3	.254 mW, typ	.344 \pm .016 mW	26.2 %
LS1	~0.000 mW, typ	.025 \pm .002 mW	100.0 %
REF1	.691 mW, typ	.791 \pm .002 mW	12.6 %
DAC1	.005 mW, typ	.000 \pm .000 mW	-----
A1	2.074 mW, typ	2.214 \pm .004 mW	6.3 %
A2	2.074 mW, typ	2.160 \pm .004 mW	4.0 %
CMP1	.553 mW, typ	.664 \pm .004 mW	16.3 %
Rp1	1.037 mW, typ	.065 \pm .000 mW	1495.3 %
Rp2	1.037 mW, typ	.013 \pm .000 mW	7876.9 %
Rp3	1.037 mW, typ	.010 \pm .000 mW	10270.0 %
SW4	.342 mW, typ	.267 \pm .005 mW	28.1 %

Total $P_{d,avg}$	9.105 mW, typ	6.554 \pm .016 mW	38.9 %

5.1.1 Explanation of Results

Note that the large error in the power consumed by the resistors is only a circumstantial error, since, when the input (data) voltage is 5 VDC, the output voltage from the comparators is always high, and little or no current flows through the resistors. The typical upper bound on the total power consumed was computed assuming that these resistors would always consume the maximum power possible, a deliberate over-estimation.

For most devices, however, the estimations were reasonably accurate, predicting the actual power consumed to within two-tenths of a milliwatt or less. If we ignore the power consumption of the pull-up resistors, we find that, overall, the total power consumption was within 8.5 % of the predicted value.

5.2 Differential Linearity Error and Noise

The following represents the findings with regard to noise and differential linearity error for a sample of 497 data points:

Table 5.2 Noise and Differential Linearity

Positive Voltage Range, +5V to 0V

Avg. Diff. Linearity Error	= .252 LSB
Std. Dev., Diff. Linearity Error	= .352 LSB
Avg. Noise Error	= .537 LSB
Avg. Err, Total	= .593 LSB

Negative Voltage Range, 0V to -5V

Avg. Diff. Linearity Error	= .240 LSB
Std. Dev., Diff. Linearity Error	= .439 LSB
Avg. Noise Error	= .462 LSB
Avg. Err, Total	= .530 LSB

Total, Full Voltage Range, +5V to -5V.

Avg. Diff. Linearity Error	=	.247 LSB
Std. Dev., Diff. Linearity Error	=	.400 LSB
Avg. Noise Error	=	.501 LSB
Avg. Err, Total	=	.559 LSB

5.2.1 Explanation of Statistical Results

The above statistics show that, on the average, over the entire voltage range, the average differential linearity error may typically be expected to be .247 LSB.

The typical "spread" of values for the differential linearity error, represented by the standard of deviation, was found to be .400 LSB.

The above statistics also show that the average error due to noise was .501 LSB.

The contribution of both noise and differential linearity error to the performance error of the 15-bit ADC under test may be summarized by the average total error, which represents the error of the device on a per-measurement basis, and was found to have the value of .559 LSB.

Taking into account that there is an expected error of ~ .177 LSB in the calculation of any single differential linearity error, the error associated with the average value (over 497 measurements) may assumed to be ~ 0.008 LSB.

CHAPTER VI
SUMMARY OF EXPECTED AND MEASURED
PERFORMANCE AND CONCLUSIONS

6.1 Measured Performance Compared to Design Requirements

Given in the table below are some of the expected and measured parameters for the performance of the device, as well as a summary of the actual performance of the device as compared to the desired performance as given in the original specifications. Table 6.1 Initial Design Requirements Compared to Rated Performance.

Desired Performance	Measured Performance
i) conversion by successive approximation:	insured by design
ii) bipolar 15-bit conversion:	insured by design
iii) differential linearity error of $\pm .500$ LSB:	$\pm .247$ LSB avg.
iv) integral linearity error of ± 1 LSB:	not measured
v) no missing codes:	no missing codes detected in 497 sample data points
vi) input voltage range of $\pm 5V$	insured by design
vii) maximum input frequency of 45 Hz:	not relevant (property of sample-and-hold section)
viii) conversion from two channels of data	insured by design (property of sample-and-hold)

ix) two conversions (one per channel) every 1/128 sec.:	insured by design (property of control logic)
x) two's-complement form output from logic section:	insured by design (property of control logic)
xi) microprocessor control:	insured by design (property of control logic)
xii) supply voltages of ± 7.5 VDC:	insured by design
xiii) power consumption of less than 80 mW (analog section):	6.55 ± 0.02 mW (not including sample-and-hold section)

6.2 Expected and Measured Performance

Given below in Table 6.2 is a more detailed summary of measured device performance as compared to expected performance.

Table 6.2 Summary of Expected Device Performance Compared to Measured Performance.

Expected Performance	Measured Performance
i) Power consumption: 9.105 mW (typ. upper bound)	$6.554 \pm .016$ mW
ii) Differential linearity error: ± 0.5 LSB	± 0.247 LSB avg.

iii) Error due to noise:		
excluding external noise		
65 uV = .213 LSB		.501 LSB
iv) Total avg. error		
expected per measurement:		
excluding external noise		
.543 LSB		.559 LSB

6.3 Conclusions

As can be seen, the above calculated values agree reasonably well with the measured values.

Generally, this was true, with the most notable exceptions being that the turn-on settling time for the OP-37EZ amplifiers was much larger than predicted (having a measured settling time of 8 microseconds as opposed to the 0.5 microseconds predicted), and the numerical value of the damping factor as a function of feedback capacitance was not predicted with great accuracy for small values of C_f for the DAC-follower A1. The equations did describe overall, the proper behavior of the op-amp circuit for reasonable values of input capacitance and feedback capacitance.

6.3.1 Effects Adverse to the Performance of the Circuit

With regard to most of the expected adverse effects, calculation usually showed them to be negligible.

In most cases, the presence of the effects could only be observed indirectly, as with the case of the supply voltage ripple caused by fluctuations in supply current due to the active operation of the amplifiers used as DAC-followers through the "on" resistance of the analog switches. Here, the supply voltage

ripple could be directly observed, but the final effect on the output of the op-amp was too small to be directly observed.

6.3.2 Comparator Noise

One small effect, however, that did have considerable importance was the voltage and current offset of the op-amps. The calculations showed that the operational amplifiers would have to be screened to eliminate the most extreme cases of offset current.

One effect that was not predicted that did have considerable influence on the performance of the circuit was the fact that the comparators were observed to pull sharp pulses of current through their inputs during transitions, resulting in voltage spikes at the inputs.

These sudden pulses in current are (most probably) the result of the 1-pole roll-off of the current gain in the input transistors to the comparators. Any sudden transition in the collector current of the input transistors due to feedback from the rest of the circuit during a transition in the output voltage will result in a sudden impulse in base current as a result of the lowered current gain with regard to frequency. This can be clearly seen from s-plane analysis, where it can be easily shown that, assuming a 1-pole roll-off model for current gain, in describing base current in terms of collector current, there will be a term in the description of base current that is proportional to a time derivative of the collector current. If the collector current makes a step transition, there will be an impulse term in the base current.

While, normally, this appears to have little effect on the

performance of the circuit (as long as the pulse is of too short a duration for the comparator to retrigger on it, which one would expect to be true under normal circumstances), it may result in problems for the circuit at voltages close to the offset of the comparators.

When one is measuring a voltage close to the offset voltage of the comparators, each comparator will oscillate, as one would normally expect, thereby putting voltage pulses onto the common line leading from the sample-and-hold section, and causing the other comparators to trigger on the pulses.

This has the effect of producing very noisy measurements at close to the offset voltage.

This effect must be corrected for in any modification of the basic design, as described in the ensuing chapter.

CHAPTER VII

CIRCUIT MODIFICATIONS

The circuit shown in Fig. 7.1 represents the modifications made to the original circuit shown in Fig. 2.2 on page 5.

7.1 Similarity of Revised Circuit to Original Circuit

The modified circuit in Fig. 7.1 is nearly identical to the original in that both are designed to meet the same specifications, which are given in Chapter II.

Both use power supply switching to reduce power consumption, and have an identical timing scheme and conversion rate. In addition, they utilize the same operating principles, insofar as both circuits are designed to measure the sign and magnitude of a voltage by comparing the voltage first to ground to measure sign and then performing successive approximation in either the positive or negative voltage ranges.

7.2 Differences between the Revised and Original Circuit

The differences between the revised and original circuit are that only one comparator is used, rather than three, with a switch (SW3) to select whether the comparator is reading the output of either A1 or A2, and hence, making the comparisons required for successive approximation in either the negative or positive voltage ranges respectively.

7.3 Advantages of Revisions

The advantages of this are that there is only one comparator present to put out the type of noise on the input lines during output voltage transitions that was described in Chapter 6, and

since there is no other comparator present to influence the performance of this comparator, the device should be much quieter, especially when measuring voltages near the comparator offset. In addition, there is only one offset to the one comparator that has to be taken into account, as opposed to three separate offsets for three different comparators.

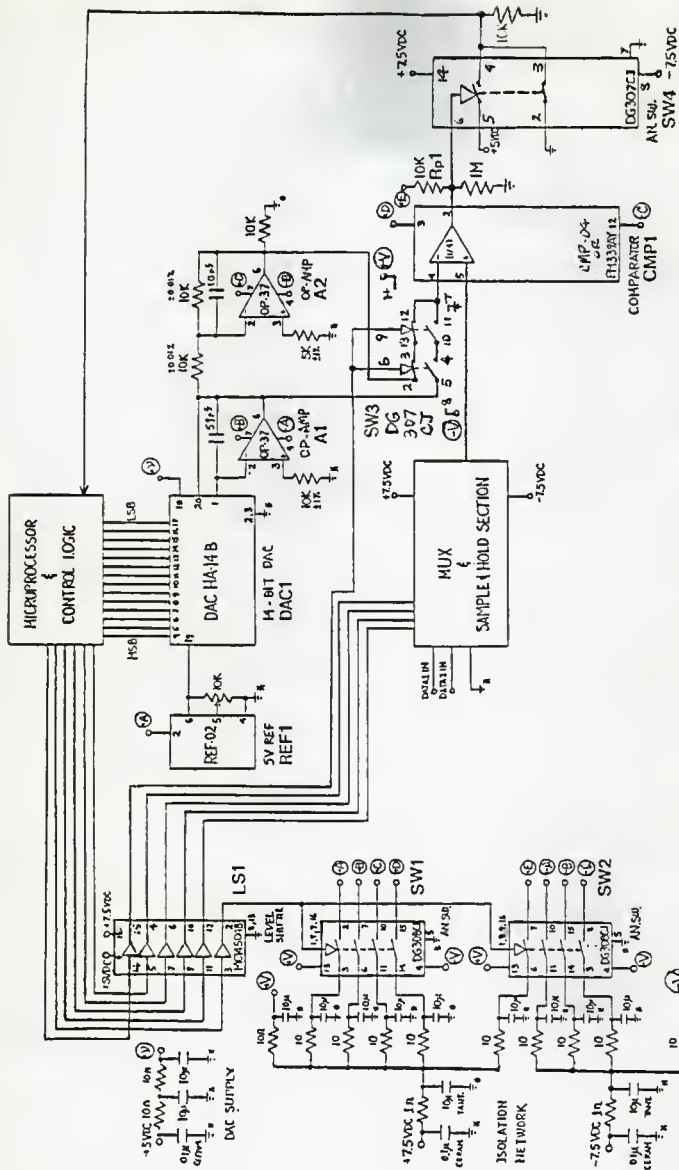
7.4 Principle of Operation for the Revised Circuit

A single conversion is performed by first measuring sign, then performing successive approximation in either the positive or negative voltage range.

The sign measurement is performed by first setting the analog switch SW3 so that the negative input of the comparator reads the output of the positive voltage range at the output of the DAC-follower A2, which is set to a nominal 0V by setting all 14 bits of the DAC (DAC-HA-14B) to "0". The positive input terminal of the comparator reads the held data voltage. The resulting comparison represents a measurement of the sign of the voltage and determines whether the comparisons required for successive approximation are to be made in the positive or negative voltage range.

If the voltage to be measured is positive, the status of SW3 remains as it is and successive approximation occurs in the positive voltage range, with the held data voltage being compared to the output of A2.

If the voltage proves to be negative, the control logic switches S3 so that all comparisons are made to the output of A1.



ALL 10 μ F CAPACITORS
SOLID TANTALUM, 10V.
ALL RESISTORS 5%
UNLESS OTHERWISE
SPECIFIED.

Ⓢ THROUGH Ⓠ REFER TO CONNECTIONS TO THE
POSITIVE SWITCHED POWER SUPPLY.
Ⓡ THROUGH Ⓢ REFER TO CONNECTIONS TO THE
NEGATIVE SWITCHED POWER SUPPLY.
Ⓣ AND Ⓤ REFER TO CONNECTIONS TO FILTERED
SUPPLY, +7.5VDC, Ⓡ TO FILTERED -5VDC SUPPLY.
Ⓢ - REFER TO AS CLOSE A CONNECTION AS POSSIBLE.

15-BIT BIPOLAR SUCCESSIVE
APPROXIMATION A-D CONVERTOR
CHARLES R. RAGSDALE
DEPT. OF ELECTRICAL ENGINEERING,
K.S. FOR. SANDIA LABORATORIES
2-5-81

Fig. 7.1. Modified design.

APPENDIX A

COMPONENT SPECIFICATIONS

The specifications listed below were obtained from the specifications for each component under the conditions used in the actual design (or as close as the given information would permit). These conditions are supply voltages of $\pm 7.5V$, and the loads shown in the circuit diagram (p. 5).

Table A.1. Circuit Components and Specifications ($\pm 7.5V$ Supply)

i) SW1-SW4 (DG308CJ Analog Switches) [3]

$$R_{ds,(on)} \approx 100 \text{ Ohms (Siliconix, p.3-91)}$$

$$P_{d,typ,quies.} \approx 15 \text{ nW}$$

$$P_{d,max,quies.} \approx 1.5 \text{ mW}$$

$$t_{on,typ} = 130 \text{ nS}$$

$$t_{off,typ} = 90 \text{ ns}$$

ii) LSl (MC14504B Level Shifter) [4]

$$I_{dd,cc} \approx .00075 \text{ } \mu\text{A,typ}$$

$$V_{ss} < V_{in} < V_{cc}$$

$$V_{ss} < V_{out} < V_{dd}$$

iii) REF1 (REF-02 5V-Voltage Reference) [5]

$$V_{sup,min} = 7.0 \text{ V}$$

$$t_{on} (.1\% \text{ final value}) = 5.0 \text{ } \mu\text{S}$$

$$I_{sup,quies.} = 1.0 \text{ mA,typ}$$

$$= 1.4 \text{ mA,max}$$

$$I_{load,max.} = 21.0 \text{ mA}$$

$$V_{out} = 5.000 \text{ V,typ}$$

$$= 4.985 \text{ V,min}$$

$$= 5.015 \text{ V,max}$$

iv) DAC1 (DAC-HA-14B, 14-Bit DAC, Std. Version Supply Voltage)[6]

Resolution = 14 Bits

Diff. Linearity Error = $\pm 1/2$ LSB,typ

= ± 1 LSB,max

Integ. Linearity Error = ± 1 LSB,max

Reference Input Resistance = 10K

Output Capacitance = 260 pf,max at Output 1

I_{out} Settling Time = 7 μ S,max to 1/2 LSB for full-scale digital input change.

Standard Version Supply Voltage Range = +15VDC, -10VDC

Standard Version I_{sup} = 1 μ A,max

$P_{d,typ,quies.}$ = 5 μ W

v) A1,A2 (OP-37EZ Precision Op-amps used as DAC-followers) [5]

GBW = 42 MHz,typ (63 MHz,typ for ± 15 VDC supply)

$A_{vo} \approx 1.2 * 10^6$ V/V

SR ≈ 14 V/ μ S,rise and 13 V/ μ S,fall

CMRR = 126 dB, falling off at 20 dB/decade at ~ 5 kHz

R_{cm} = 3 GOhms,typ

R_{dm} = 6 MOhms,typ

$e_n \approx 3.0$ nV/(Hz)^{1/2}

PSRR ≈ 120 dB, falling off at 20 dB/dec. at ~ 7 Hz,
pos. sup., 125 dB, falling of at 20 dB/dec. at
10 Hz, neg. sup.

E_{os} = 10 μ V,typ

= 25 μ V,max

$E_{os, long-term stability}$ = 0.2 μ V/Month

$$I_{os} = 7 \text{ nA, typ}$$
$$= 35 \text{ nA, max}$$

$$I_{bias} = \pm 10 \text{ nA}$$
$$= \pm 40 \text{ nA}$$

$$V_{sup} \text{ Range} = \pm 22 \text{ V}$$

$$I_{sup, quies.} \approx 2.5 \text{ mA, typ (PMI, p.5-144)}$$

$$P_{d, quies.} \approx 45 \text{ mW, typ (computed from } I_{sup, quies.} \text{.)}$$

vi) CMP1 (PM339AY or CMP-04 Quad Comparator) [5]

$$A_{vo} = 200 \text{ V/mV, typ}$$
$$= 50 \text{ V/mV, min for PM339AY}$$
$$= 80 \text{ V/mV, min for CMP-04}$$

$$\text{CMRR} = 100 \text{ dB, typ for CMP-04}$$
$$= 80 \text{ dB, min for CMP-04}$$

$$\text{Input Comm. Mode Vol. Range} = 0 \text{ V, min to } V_{sup, pos} - 1.5 \text{ V}$$
$$= 0 \text{ to } 6.0 \text{ V}$$

$$\text{Large Sig. Response Time} = 300 \text{ nS, typ for } R_{pu} = 5.1 \text{K}$$

$$\text{Small Sig. Response Time} = 1.3 \mu\text{S, typ for } R_{pu} = 5.1 \text{K}$$

$$E_{os} = \pm 1.0 \text{ mV, typ for PM339AY}$$
$$= \pm 2.0 \text{ mV, max for PM339AY}$$
$$= \pm 0.4 \text{ mV, typ for CMP-04}$$
$$= \pm 1.0 \text{ mV, max for CMP-04}$$

$$I_{os} = \pm 3.0 \text{ nA, typ for PM339AY}$$
$$= \pm 2.0 \text{ nA, typ for CMP-04}$$

$$I_{bias} = \pm 25 \text{ nA, typ}$$

$$I_{sup, pos} = 0.8 \text{ mA, typ}$$
$$= 2.0 \text{ mA, max}$$

$$I_{sup, neg} = -0.8 \text{ mA, typ}$$
$$= -2.0 \text{ mA, max}$$

APPENDIX B
CALCULATIONS REQUIRED TO DESIGN LOW POWER
15-BIT SUCCESSIVE APPROXIMATION A-D CONVERTER

The following calculations were required to design the low-power (switched power supply) successive approximation A-D converter described previously and shown in the circuit diagram on the following page.

B.1 Justification for Low Duty Cycle Method of Power Reduction

That power reduction can be achieved through operation at low duty cycle, while intuitively obvious, should be proved for the sake of completeness.

If we let V be the DC supply voltage for a load and I be the DC current drawn by the load, then the power consumed by the load, P_d , is given by the equation:

$$P_d = VI \quad (\text{Eq. B.1})$$

If, however, the device or load is power switched with a period T , out of which it is only on for a period of time t_1 , so that then instantaneous voltage and current are given by:

$$v(t) = V, \text{ for } 0 < t < t_1 \quad (\text{Eq. B.2a})$$
$$0, \text{ for } t_1 < t < T$$

$$i(t) = I, \text{ for } 0 < t < t_1 \quad (\text{Eq. B.2b})$$
$$0, \text{ for } t_1 < t < T$$

as shown below:

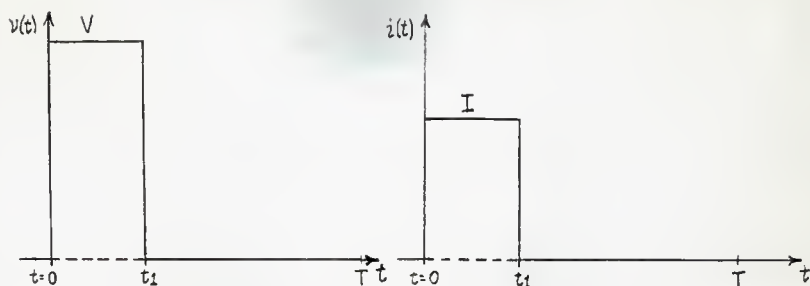


Fig. B.1. Plot of $v(t)$ and $i(t)$ vs. t

Then the average power consumed by the load is given by:

$$P_{d,avg} = (1/T) \int_0^T v(t) i(t) dt \quad (\text{Eq. B.3a})$$

$$= (1/T) \left(\int_0^{t_1} VI dt + \int_{t_1}^T 0 dt \right) \quad (\text{Eq. B.3b})$$

$$= (t_1/T) * VI \quad (\text{Eq. B.3c})$$

$$P_{d,avg} = (t_1/T) * P_d \quad (\text{Eq. B.4})$$

B.2 Power Consumption

From (Eq. B.4) we see that the average power consumed by a circuit component or load under switched power conditions is given by the fractional duty cycle, (t_1/T) , multiplied by the power consumption of the load under constant "on" conditions, P_d .

This gives us the basic method we will use to estimate the average power consumed by the circuit components or loads under switched power conditions. First, having designed a circuit that will meet required specifications, we will estimate the power consumed under constant "on" conditions for each component based both on the quiescent power consumption values given for that particular component in their specifications, which we will call P_{dq} , and the amount of additional power the device or load will

consume depending on the loading conditions. This variable we will consider to be the "active" component of the power, that is, the component of power consumed by the device under active conditions, and we will call this variable P_{da} . In short we are assuming that we may estimate the total amount of power a circuit component will use under constant "on" conditions by the formula:

$$P_d = P_{dq} + P_{da} \quad (\text{Eq. B.5})$$

and that, for the entire circuit, the total power consumed in the constant on condition is merely the sum of P_d for each chip, or:

$$P_{d,\text{total}} = (P_{dq} + P_{da}),\text{total} \quad (\text{Eq. B.6})$$

From (Eq. B.4), we may estimate the total average power consumed by the entire circuit by the formula:

$$P_{d,\text{total,avg}} = (t_1/T) * P_{d,\text{total}} \quad (\text{Eq. B.7})$$

Shown below are the calculations used to obtain P_d for each component in the circuit. It should be noted that the values obtained for each P_d represent "worst case" considerations for power. That is, each device individually is always assumed to be operating under conditions within the limits it will encounter in actual operation within the circuit that will cause it to consume the maximum amount of power possible, or, in short P_{da} is assumed to have the maximum value possible for each component and its dependent loads (ie. feedback resistors, load resistors, etc., whose current under operating conditions is supplied through the device's own power supply terminals). In addition, both typical and maximum values will be considered for the quiescent power,

P_{dq} , which will be called $P_{dq,typ}$ and $P_{dq,max}$. These values will be obtained from the specifications, and as a result, corresponding values will be computed for $P_{d,typ}$ and $P_{d,max}$ which will represent estimates for power consumption for the devices and their dependent loads under specified typical and specified maximum operating conditions. Furthermore, values will be obtained for $P_{d,total,typ}$ and $P_{d,total,max}$ which will represent the sum of the values obtained for $P_{d,typ}$ and $P_{d,max}$ for each individual component and, as such, may be considered to represent an upper bound for power consumption for the entire circuit for specified typical and specified maximum cases. Similarly, values will be calculated from (Eq. B.7) for $P_{d,total,avg,typ}$ and also for $P_{d,total,avg,max}$ which will represent expected upper bounds on the total average power consumption for the entire circuit under specified typical and specified maximum operating conditions.

It is the values for $P_{d,total,avg,typ}$ and $P_{d,total,avg,max}$ that will be the important quantities to be approximated by the calculations for power consumption contained in this section.

In the following subsections, the above described quantities will have the meanings given, and I_s will refer to supply current. In addition, any quantity to which a "+" or "-" is added in the subscript will refer to the appropriate supply terminal.

Note also that the power consumed by dependent loads (as describe above) is thrown in with the power consumed by the device, since the current supplied to a dependent load is pulled from the supply terminal for the device. By doing this, the results given for each device should represent what will actually be measured

by the application of a power meter to that device.

Also used in the P_d calculations are the equations:

$$I_s = I_{sq} + I_{sa} \quad (\text{Eq. B.8})$$

where I_{sq} is the quiescent supply current and I_{sa} is the "active" supply current due to the load under operating conditions shown, and:

$$P_d = (V_{s,+}) * (I_{s,+}) + (V_{s,-}) * (I_{s,-}) \quad (\text{Eq. B.9})$$

where $(V_{s,+})$ and $(V_{s,-})$ are taken to be +7.5V and -7.5V.

B.2.1 Pd Calculations, Individual Components and Dependent Loads

i) REF1 (Ref-02, 5-V Reference)

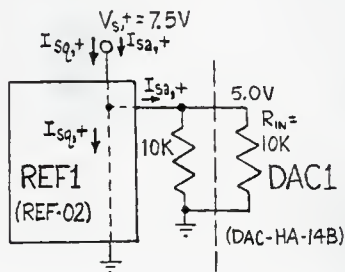


Fig. B.2. REF1 Block Diagram

By specification:

$$I_{sq,typ,+} = 1.0 \text{ mA}$$

$$I_{sq,max,+} = 1.4 \text{ mA}$$

$$I_{sq,-} = 0 \text{ mA}$$

By calculation:

$$I_{sa,+} = 5V/5K = 1.0 \text{ mA}$$

By calculation, from (Eq. B.8):

$$I_{s,typ,+} = 1.0 + 1.0 \text{ mA}$$

$$= 2.0 \text{ mA}$$

$$I_{s,max,+} = 1.4 + 1.0 \text{ mA}$$

$$= 2.4 \text{ mA}$$

$$I_{s,typ,-} = 0 \text{ mA}$$

$$I_{s,max,-} = 0.0 \text{ mA}$$

By calculation, from (Eq. B.9):

$$P_{d,typ} = 15 \text{ mW}$$

$$P_{d,max} = 18 \text{ mW}$$

ii) DAC1 (DAC-HA-14B, 14-Bit DAC, Low Power)

By Specification:

$$P_d = .005 \text{ mW}$$

iii) A1 and A2 (OP-37's used as DAC followers)

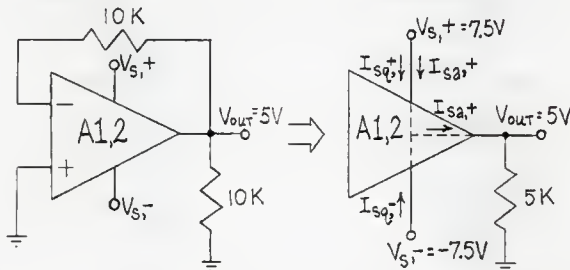


Fig. B.3. A1 and A2 Block Diagram

By specification:

$$I_{sq,typ,+} = 2.5 \text{ mA}$$

$$I_{sq,max,+} = 2.7 \text{ mA}$$

$$I_{sq,typ,-} = -2.5 \text{ mA}$$

$$I_{sq,max,-} = -2.7 \text{ mA}$$

By calculation:

$$I_{sa,+} = 5V/5K = 1.0 \text{ mA}$$

By calculation, from (Eq. B.8):

$$I_{s,typ,+} = 2.5 + 1.0 \text{ mA}$$

$$= 3.5 \text{ mA}$$

$$I_{s,max,+} = 2.7 + 1.0 \text{ mA}$$

$$= 3.7 \text{ mA}$$

$$I_{s,typ,-} = -2.5 \text{ mA}$$

$$I_{s,max,-} = -2.7 \text{ mA}$$

By calculation, from (Eq. B.9):

$$P_{d,typ} = 45.0 \text{ mW each}$$

$$P_{d,max} = 48.0 \text{ mW each}$$

iv) CMP1 (PM339AY or CMP-04, Quad Comparator)

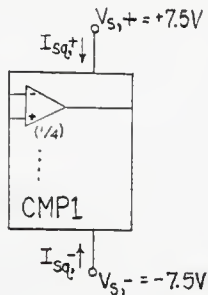


Fig. B.4. CMP1 Block Diagram

By specification:

$$I_{sq,typ,+} = 0.8 \text{ mA}$$

$$I_{sq,max,+} = 2.0 \text{ mA}$$

$$I_{sq,typ,-} = -0.8 \text{ mA}$$

$$I_{sq,max,-} = -2.0 \text{ mA}$$

By calculation:

$$I_{sa,+} = 0 \text{ mA}$$

$$I_{sa,-} = 0 \text{ mA}$$

By calculation, from (Eq. B.8):

$$I_{s,typ,+} = 0.8 \text{ mA}$$

$$I_{s,max,+} = 2.0 \text{ mA}$$

$$I_{s,typ,-} = -0.8 \text{ mA}$$

$$I_{s,max,-} = -2.0 \text{ mA}$$

By calculation, from (Eq. B.9):

$$P_{d,typ} = 12.0 \text{ mW}$$

$$P_{d,max} = 30.0 \text{ mW}$$

v) R_{p1}, R_{p2}, R_{p3} (10K, 5% Pull-up Resistors)

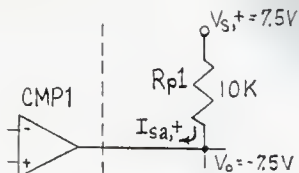


Fig. B.5. Pull-up Resistor Configuration

By calculation:

$$I_{sa,+} = 1.5 \text{ mA}$$

By calculation:

$$P_{d,typ} = 22.5 \text{ mW each}$$

$$P_{d,max} = 22.5 \text{ mW each}$$

vi) Pull-down Resistors (3 1Mohm Resistors)

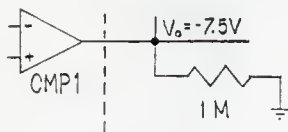


Fig. B.6. Pull-down Resistor Configuration

By calculation:

$$P_{d,typ} = .056 \text{ mW each}$$

$$P_{d,max} = .056 \text{ mW each}$$

vii) SW4 (DG308CJ Analog Switch used as a level shifter)

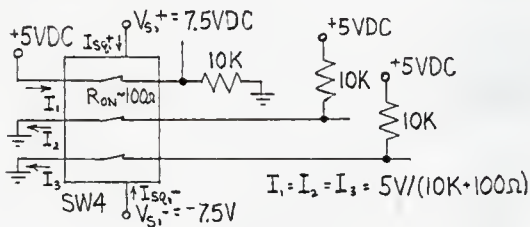


Fig. B.7. SW4 Block Diagram

By specification:

$$I_{sq,typ,+} = .001 \mu A$$

$$I_{sq,max,+} = 100 \mu A$$

$$I_{sq,typ,-} = -.001 \mu A$$

$$I_{sq,typ,-} = -100 \mu A$$

By calculation:

$$I_{sa,+} = 3 * (5V / (10K + 100))$$

$$= 1.485 \text{ mA}$$

By calculation:

$$P_{d,typ} = 7.426 \text{ mW}$$

$$P_{d,max} = 7.426 + 1.5 \text{ mW}$$

viii) LSI (MCI4504B Level Shifter)

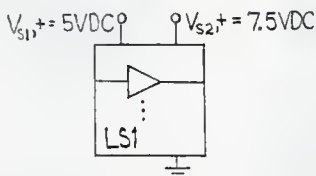


Fig. B.8. LSI Block Diagram

By specification (CMOS-CMOS mode, AL model):

$$I_{sq,typ,+} = .00075 \mu A$$

$$I_{sq,max,+} = .075 \mu A$$

$$I_{sq,typ,-} = -.00075 \mu A$$

$$I_{sq,max,-} = -.075 \mu A$$

By calculation:

$$I_{sa,+} = \sim 0 \text{ mA}$$

By calculation, using (Eq. B.8):

$$I_{s,typ,+} = .00075 \mu A$$

$$I_{s,max,+} = .075 \mu A$$

$$I_{s,typ,-} = -.00075 \mu A$$

$$I_{s,max,-} = -.075 \mu A$$

By calculation, using (Eq. B.9):

$$P_{d,typ} = .01125 \mu W$$

$$P_{d,max} = .001125 \text{ mW}$$

$$= \sim 0 \text{ mW}$$

$$= \sim 0 \text{ mW}$$

(Note: Assume this device uses ~ 0 mW in all future calculations or ignore.)

ix) Isolation Network

By calculation:

$$P_{d,typ} = 10 \text{ Ohms} * (\Sigma(I_{s,typ,+})^2 + \Sigma(I_{s,typ,-})^2) \\ + 1 \text{ Ohms} * ((\Sigma(I_{s,typ,+}))^2 + (\Sigma(I_{s,typ,-}))^2) \\ = 0.381 \text{ mW} + 0.244 \text{ mW}$$

$$P_{d,max} = 10 \text{ Ohms} * (\Sigma(I_{s,max,+})^2 + \Sigma(I_{s,max,-})^2) \\ + 1 \text{ Ohms} * ((\Sigma(I_{s,max,+}))^2 + (\Sigma(I_{s,typ,-}))^2) \\ = 0.465 \text{ mW} + 0.337 \text{ mW}$$

$$P_{d,typ} = 0.625 \text{ mW}$$

$$P_{d,max} = 0.802 \text{ mW}$$

x) SW1 (DG308CJ Analog Switch used for power switching)

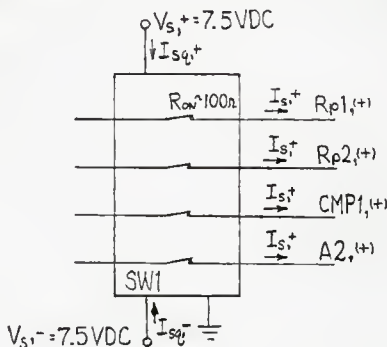


Fig. B.9. SW1 Block Diagram

By specification:

$$I_{sq,typ,+} = .001 \mu\text{A}$$

$$I_{sq,max,+} = 100 \mu\text{A}$$

$$I_{sq,typ,-} = -.001 \mu\text{A}$$

$$I_{sq,max,-} = -100 \mu\text{A}$$

By calculation, where $P_{da} = I_{sa} * R_{on}$, $R_{on} = 100 \text{ Ohms}$:

	$I_{sa,typ}$	$P_{da,typ}$	$I_{sa,max}$	$P_{da,max}$
a)	1.5 mA	0.225 mW	1.5 mA	0.225 mW
b)	1.5 mA	0.225 mW	1.5 mA	0.225 mW
c)	0.8 mA	0.064 mW	2.0 mA	0.400 mW
d)	3.5 mA	1.225 mW	3.7 mA	1.369 mW
Total:		1.739 mW	Total:	2.219 mW

By calculation, using (Eq. B.5):

$$P_{d,typ} = 1.739 \text{ mW}$$

$$P_{d,max} = 2.219 \text{ mW} + 1.5 \text{ mW}$$

xi) SW2 (DG308CJ Analog Switch used for power switching)

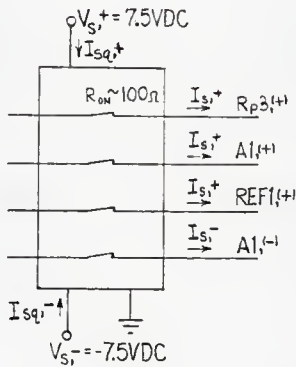


Fig. B.10. SW2 Block Diagram

By specification:

$$I_{sq,typ,+} = .001 \mu\text{A}$$

$$I_{sq,max,+} = 100 \mu\text{A}$$

$$I_{sq,typ,-} = .001 \mu\text{A}$$

$$I_{sq,max,-} = 100 \mu\text{A}$$

By calculation, where $P_{da} = I_{sa} * R_{on}$, $R_{on} = 100 \text{ Ohms}$:

	$I_{sa,typ}$	$P_{da,typ}$	$I_{sa,max}$	$P_{da,max}$
a)	-2.5 mA	0.625 mW	-2.7 mA	0.729 mW
b)	1.5 mA	0.225 mW	1.5 mA	0.225 mW
c)	3.5 mA	1.225 mW	3.7 mA	1.369 mW
d)	2.0 mA	0.400 mW	2.4 mA	0.576 mW
Total:		2.475 mW	Total:	2.899 mW

By calculation, using (Eq. B.5):

$$P_{d,typ} = 2.475 \text{ mW}$$

$$P_{d,max} = 2.899 \text{ mW} + 1.5 \text{ mW}$$

xii) SW3 (DG308CJ Analog Switch used for power switching)

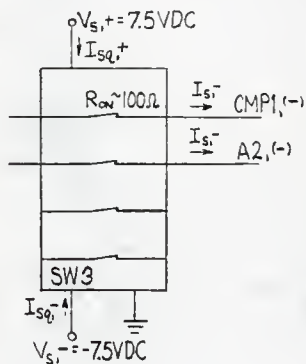


Fig. B.11. SW3 Block Diagram

By specification:

$$I_{sq,typ,+} = .001 \mu\text{A}$$

$$I_{sq,max,+} = 100 \mu\text{A}$$

$$I_{sq,typ,-} = -.001 \mu\text{A}$$

$$I_{sq,max,-} = -100 \mu\text{A}$$

By calculation, where $P_{da} = I_{sa} * R_{on}$, $R_{on} = 100$ Ohms :

	$I_{sa,typ}$	$P_{da,typ}$	$I_{sa,max}$	$P_{da,max}$
a)	-0.8 mA	0.064 mW	-2.0 mA	0.400 mW
b)	-2.5 mA	0.625 mW	-2.7 mA	0.729 mW
c)	0 mA	0 mW	0 mA	0 mW
d)	0 mA	0 mW	0 mA	0 mW
Total:		0.689 mW	Total:	1.129 mW

By calculation, using (Eq. B.5):

$$P_{d,typ} = 0.689 \text{ mW} \qquad P_{d,max} = 1.129 \text{ mW} + 1.5 \text{ mW}$$

From the above results, it is possible to calculate values for $P_{d,avg,typ}$ and $P_{d,avg,max}$ for each from (Eq. B.4). Note that in the cases of the DG308CJ Analog Switches, for the maximum case, since they are not power switched, the quiescent power of 1.5 mW must be taken into account separately, so that, for example, in the case of SW3 above:

$$P_{d,avg,max} = (t_1/T) * 1.129 \text{ mW} + 1.5 \text{ mW} \qquad (\text{Eq. B.10a})$$

whereas, in the typical case, since we can ignore the quiescent power, we would estimate:

$$P_{d,avg,typ} = (t_1/T) * 0.689 \text{ mW} \qquad (\text{Eq. B.10b})$$

This will be true for SW1, SW2, SW3, (and also for SW4, as will be shown).

Similarly, since the supply to the DAC-HA-14B is not power switched, and it's only contribution to power is (in our approximation) simply quiescent power, then we would have to assume:

$$P_{d,avg,typ} = P_{d,typ} = 0.005 \text{ mW}$$

and

$$P_{d,avg,max} = P_{d,max} = 0.005 \text{ mW}$$

In addition to the above exceptions, the power through the isolation network is treated as though power switched, since the current flowing through the resistors is indeed switched. The active component of power through SW4 may be treated as power switched, since the outputs of the comparator will go to ground when the power to the comparator is switched off, thereby opening the switches in SW4 and shutting off the flow of current through the pull-up or pull-down resistors. Therefore, the values for $P_{d,avg,max}$ and $P_{d,avg,typ}$ will be obtained in the manner described above for SW1, SW2, and SW3.

Of greater significance, the estimated total average power for the typical and maximum cases will be computed for the entire circuit, given by $P_{d,total,avg,typ}$ and $P_{d,total,avg,max}$.

B.2.2 Computed Values for $P_{d,avg,typ}$, $P_{d,avg,max}$, $P_{d,total,avg,typ}$ and $P_{d,total,avg,max}$.

The following tables were constructed to display the calculations obtained by the methods described above. The limits on t_1 are that t_1 lies between 330 and 375 microseconds. The limit of 375 microseconds occurs in the practical adaptation of the circuit, given limits on microprocessor performance in the control logic, while 330 microseconds represents the desired value for t_1 .

Table B.1. Computed Values for $P_{d,avg,typ}$, $P_{d,avg,max}$, $P_{d,total,avg,typ}$, and $P_{d,total,avg,max}$.

i) Case I; $t_1=330 \mu S$, $T=7812.5 \mu S$, $(t_1/T)=0.04224$ (4.2%)

Component	$P_{d,typ}$	$P_{d,avg,typ}$	$P_{d,max}$	$P_{d,avg,max}$
Iso. Net.	0.625 mW	0.026 mW	0.802 mW	0.034 mW
LS1	0	0	0	0
SW1	1.739	0.073	(2.219 +1.5)	1.594
SW2	2.475	0.105	(2.899 +1.5)	1.622
SW3	0.689	0.029	(1.129 +1.5)	1.548
REF1	15.000	0.634	18.000	0.760
DAC1	0.005	0.005	0.005	0.005
A1	45.000	1.901	48.000	2.028
A2	45.000	1.901	48.000	2.028
CMP1	12.000	0.507	30.000	1.267
Rp1	22.500	0.950	22.500	0.950
Rp2	22.500	0.950	22.500	0.950
Rp3	22.500	0.950	22.500	0.950
SW4	7.426	0.314	(7.426 +1.5)	1.814

Total: 8.345 mW

Total: 15.550 mW

$P_{d,total,avg,typ} = 8.345 \text{ mW}$

$P_{d,total,avg,max} = 15.550 \text{ mW}$

ii) Case II; $t_1=375 \mu\text{s}$, $T=7812.5 \mu\text{s}$, $(t_1/T)=0.048$ (4.8%)

Component	$P_{d,typ}$	$P_{d,avg,typ}$	$P_{d,max}$	$P_{d,avg,max}$
Iso. Net.	0.625 mW	0.030 mW	0.802 mW	0.039 mW
LS1	0	0	0	0
SW1	1.739	0.083	(2.219 +1.5)	1.607
SW2	2.475	0.119	(2.899 +1.5)	1.639
SW3	0.689	0.033	(1.129 +1.5)	1.554
REF1	15.000	0.720	18.000	0.864
DAC1	0.005	0.005	0.005	0.005
A1	45.000	2.160	48.000	2.304
A2	45.000	2.160	48.000	2.304
CMP1	12.000	0.576	30.000	1.440
Rp1	22.500	1.080	22.500	1.080
Rp2	22.500	1.080	22.500	1.080
Rp3	22.500	1.080	22.500	1.080
SW4	7.426	0.356	(7.426 +1.5)	1.856
-----		Total: 9.482 mW		Total: 16.852 mW

$$P_{d,total,avg,typ} = 9.482 \text{ mW} \quad P_{d,total,avg,max} = 16.852 \text{ mW}$$

The above tables summarize our expected upper bounds on power consumption for the different values of the duty cycle encountered in the experiment.

For a duty cycle of 4.224% (330 μs of "on" time) we may expect the maximum power consumption to lie between 8.345 mW and 15.550 mW, and for a duty cycle of 4.800%, between 9.482 mW and 16.852 mW.

B.3 Calculations Required for Turn-on Settling Time

In order to insure that all of the switched components of the device could be turned on and settle sufficiently within the allowed warm-up time of 10 microseconds to allow measurement with 15 bits of resolution, the turn-on settling time to within 15 bits (an error of 1 part in 2^{15} , or .0000305) was calculated from the specifications for each device being power switched.

B.3.1 Turn-on Settling Time Calculations to within 15 Bits, for Individual Components

i) REF1 (Ref-02, 5-V Reference)

From specifications:

ton, settling to 0.1% = 5 μ S

Calculations:

Where t_0 = time constant for 1-pole step response, we have:

$$\exp(-t/t_0) = 0.001, \text{ where } t = 5 \mu\text{S} \quad (\text{Eq. B.11})$$

then,

$$t_0 = t / (\ln 1000) \quad (\text{Eq. B.12a})$$

$$= 0.724 \mu\text{S} \quad (\text{Eq. B.12b})$$

To settle to within $1/2^{15}$, then

$$\exp(-t/t_0) = \frac{1}{2^{15}}, \text{ and we have:} \quad (\text{Eq. B.13a})$$

$$t = 7.52 \mu\text{S}. \quad (\text{Eq. B.13b})$$

ii) A1 and A2 (OP-37's used as DAC followers)

From specifications:

GBW \approx 42 MHz

SR \approx 14 V/ μ S (with power supply voltages of \pm 7.5V)

Calculations:

We will assume that the settling time for the operational amplifiers may be approximated by calculating, for a given value of $G = 1 + R_f/R_i$, GBW, and A_{VO} , the open loop gain, the response of the op-amp to the step input of the offset voltage. That is, we will assume that the op-amp will behave as though one of the device's own properties, namely the offset voltage, had suddenly been applied, and that the device responded accordingly for a given value of G . For the circuit configuration shown below, where $G = 1 + R_f/R_i$, and $V_o = A_{VO} * \Delta V$:

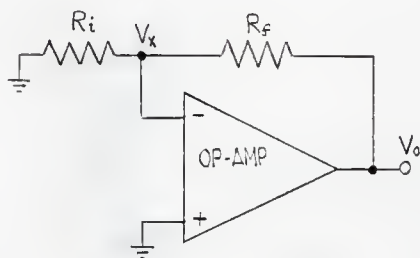


Fig. B.12. Op-amp Configuration, Offset Determination

a quick circuit analysis shows that:

$$(0 - V_x)/R_i = (V_x - V_o)/R_f, \quad V_x = V_{os} - \Delta V \quad (\text{Eq. B.14})$$

$$\text{and } V_o = A_{VO} * \Delta V.$$

Solving the above for ΔV yields:

$$\Delta V = G * V_{os} / (G + A_{VO}). \quad (\text{Eq. B.15})$$

and since $V_o = A_{VO} * \Delta V$, we have:

$$(\text{Eq. B.16a})$$

$$V_o = \frac{G}{1 + \frac{G}{A_{VO}}} * V_{os} \quad (\text{Eq. B.16b})$$

as one would expect. Assuming the 1-pole roll-off model for the s-plane analysis of the op-amp, where we find A_{vo} is of the form $A_{vo} = A_o * \omega_o / (s + \omega_o)$, we have, upon substitution:

$$V_{os}(s) = \frac{A_o * \omega_o}{s + (1 + \frac{A_o}{G}) \omega_o} * V_{os}(s). \quad (\text{Eq. B.17})$$

where, since we have assumed $V_{os}(t)$ is of the form:

$$V_{os}(t) = V_{off} * u(t), \quad (\text{Eq. B.18})$$

then,

$$V_{os}(s) = \frac{V_{off}}{s}, \quad (\text{Eq. B.19})$$

and we find:

$$V_o(s) = \frac{A_o * \omega_o}{s + (1 + \frac{A_o}{G}) \omega_o} * \frac{V_{off}}{s} \quad (\text{Eq. B.20a})$$

$$= \frac{A_o * V_{off}}{(1 + \frac{A_o}{G})} \left(\frac{1}{s} - \frac{1}{s + (1 + \frac{A_o}{G}) \omega_o} \right). \quad (\text{Eq. B.20b})$$

Solving for $V_o(t)$ by using the inverse Laplace transform, we have an exact solution of the form: (Eq. B.21a)

$$V_o(t) = \frac{A_o}{1 + \frac{A_o}{G}} (V_{off} * u(t)) \left(1 - e^{-\omega_o (1 + \frac{A_o}{G}) t} \right),$$

For the case $G \ll A_o$, we have, approximately: (Eq. B.21b)

$$V_o(t) \approx G * V_{os}(t) * (1 - e^{-t/t_o}), \quad t_o \approx \frac{G}{A_o * \omega_o} = \frac{G}{2 * \pi * GBW}.$$

Consequently, for 15 bits, the fractional error is given by:

$$\frac{-t/t_o}{e} = (1/2)^{15}, \quad \text{where: } t_o \approx G / (2 * \pi * GBW). \quad (\text{Eq. B.22a})$$

In this instance, $G = 2$, $GBW \approx 42$ MHz, and:

$$t_o = 7.57 \text{ nS}, \quad (\text{Eq. B.22b})$$

and solving for t , we have, for the settling time:

$$t = 78.7 \text{ nS.} \quad (\text{Eq. B.22c})$$

The above result is obviously too small to be realistic, as one would expect, since it omits several important items from consideration, the most obvious of them being the time required to charge up the internal frequency compensation capacitor (an unspecified value), as well as the Miller capacitances of the transistors themselves (also unknown quantities). Since all of this would require an extremely detailed analysis of the circuit and a knowledge of these unknown quantities, it would perhaps be better to add a term when estimating the settling time that would include slewing time, since the slewing rate of an op-amp is usually limited by the value of the frequency compensation capacitor [7]. This should be a better approximation to the actual settling time. Therefore, we will assume that the device must slew from one of the "rails" (assume $\sim 7.0\text{V}$ or $\sim -7.0\text{V}$) to the offset, which is approximately 0V , or ground, before settling can occur. Therefore, the total settling time is considered to consist of a slewing time and a settling time to within 15 bits, as shown below, and we have:

$$t \approx 7.0\text{V}/(14\text{V}/\mu\text{S}) + 50.9 \text{ nS} \quad (\text{Eq. B.23a})$$

$$\approx 550 \text{ ns} \quad (\text{Eq. B.23b})$$

$$\sim .5 \mu\text{S.} \quad (\text{Eq. B.23c})$$

We may therefore conclude approximately that settling will occur in much less time than our required limit of $10 \mu\text{S}$.

iii) CMP1 (PM339AY or CMP-04 Quad Comparator)

By specification:

$$E_{OS} = .3 \text{ mV}$$

$$\text{Small signal response time } (R_{pu} = 5.1K) = 1.3 \mu\text{S}$$

Calculations:

By a consideration similar to that used above in estimating the settling time of the DAC-followers, we will assume that the settling time for the comparators may be estimated by the response of the device to the sudden input of the device's own off-set voltage. Therefore, despite the difference in load resistors used at the output (a 10K pull-up resistor was used, rather than a 5.1K pull-up resistor, which will have the effect of slowing the small signal response slightly), we will assume that the device will respond to the sudden (step) input of its own off-set voltage as it would to any small signal, and use the device's small signal response time, so that we will estimate the settling time of the device to be:

$$t_{\text{settling}} \sim 1.3 \mu\text{S} \quad (\text{Eq. B.24})$$

From the above considerations, we may conclude, at least in approximation, that all devices to be power switched will settle to the desired accuracy within 10 μS .

It may be that the presence of the DAC-HA-14B, which has, for any bit transition in its digital input, a settling time of 7.0 μS for $\pm 1/2$ bit, will add to the settling time of the DAC-followers, bringing their settling time to $\sim 7.0 \mu\text{S}$. However, in no case was anything found within the calculations to indicate that the settling time of any of the devices would exceed 10 μS .

B.4 Calculations Required to Determine Measurement Settling Times

It was decided, primarily on the basis of the DAC-HA-14B settling time of $7.0 \mu\text{S}$ to within $\pm 1/2$ bit, and the small signal settling time of the comparator, which was estimated to be $\sim 1.3 \mu\text{S}$ (actually measured at $2.1 \mu\text{S}$ with a 10K pull-up resistor by inputting a $1/2$ LSB, or $152 \mu\text{V}$, peak-to-peak square wave oscillating around the input offset voltage to the comparator), to use $10 \mu\text{V}$ as a convenient unit of time within which all the important measuring devices (ie. the DAC, the DAC-followers, and the comparators) could settle to within $\pm 1/2$ LSB. Initially, the measurement settling time was estimated at:

$$t_{\text{meas. settling}} \sim 7.0 + 2.1 \mu\text{S} \quad (\text{Eq. B.25a})$$

$$\sim 9.1 \mu\text{S} \quad (\text{Eq. B.25b})$$

The above figure merely includes the settling time for the DAC and the subsequent settling of the comparator, which, being a non-linear device, must be considered to make a transition only after the DAC has settled to within $\pm 1/2$ LSB to allow for the worst possible case. Note that the measured value of the settling time for the comparator was used in this estimate, rather than that obtained from the specification, since it may reasonably be assumed to be much more accurate.

Choosing a unit of time of $10 \mu\text{S}$ for 1 bit of conversion in the successive approximation conversion process allows for an additional "safety margin" of $\sim .9 \mu\text{S}$ for settling, and is, in addition, a reasonably convenient unit of time.

More detailed calculations were made to determine whether or not the device could actually be made to settle within that span of time.

First, it may be shown (and will be shown below) that the DAC and the first output DAC-follower constitute (at least predominately) a 2-pole system. This makes it necessary to determine the value of the damping factor, which we will here call n , required to allow the output to settle as quickly as possible, given a step voltage input. This means that we must determine the value of n which will cause the maximum voltage error to be a minimum at a given time t . We can take the maximum error to be the magnitude of the difference between the envelope of the step-response and the ideal step output (as shown below). The value obtained for n so that the maximum error voltage is minimized can be shown, for all practical purposes, to be $n=1$. A demonstration of this, as well as the required background information and derivations, is given on the following pages.

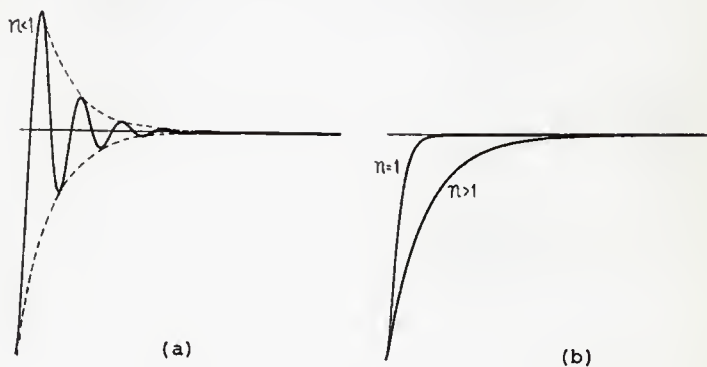


Fig. B.13. Step response and envelope, (a) $n < 1$, (b) $n \geq 1$.

B.4.1 General Information, 2-Pole Response to Voltage Step-function Input

We will assume that the DAC-followers constitute a 2-pole system, so that the transfer function in the s-plane is of the form:

$$F(s) = V_o(s)/V_i(s) \quad (\text{Eq. B.26a})$$

$$= \frac{H*\omega^2}{[s^2 + (2*n*\omega)s + \omega^2]} \quad (\text{Eq. B.26b})$$

which has poles at: (Eq. B.26c)

$$s = [-n + (n^2 - 1)^{1/2}] * \omega, \text{ and } [-n - (n^2 - 1)^{1/2}] * \omega.$$

If we assume that the DAC-follower receives a step-function input of the form:

$$V_i(t) = a_o * u(t), \quad (\text{Eq. B.27})$$

so that the Laplace Transform of $V_i(t)$ is given by:

$$V_i(s) = a_o/s, \quad (\text{Eq. B.28})$$

then:

$$V_o(s) = \frac{H*\omega^2}{[s^2 + (2*n*\omega)s + \omega^2]} * \frac{a_o}{s}, \quad (\text{Eq. B.29a})$$

which may be written in the form: (Eq. B.29b)

$$V_o(s) = \frac{a_1}{s - [-n + (n^2 - 1)^{1/2}] \omega} + \frac{a_2}{s - [-n - (n^2 - 1)^{1/2}] \omega} + \frac{a_3}{s}$$

where:

$$a_1 = -\frac{H*a_o}{2} [1 + n/(n^2 - 1)^{1/2}], \quad (\text{Eq. B.29c})$$

$$a_2 = \frac{H*a_o}{2} [-1 + n/(n^2 - 1)^{1/2}], \quad (\text{Eq. B.29d})$$

$$a_3 = H*a_o. \quad (\text{Eq. B.29e})$$

Taking the Inverse Laplace Transform, we have the usual solution for $n > 0$:

(Eq. B.30)

$$V_0(t) = H * a_0 * u(t) \left\{ 1 - \frac{1}{2} * [1 + n / (n^2 - 1)^{1/2}] * e^{[-n + (n^2 - 1)^{1/2}] \omega t} \right. \\ \left. + \frac{1}{2} * [-1 + n / (n^2 - 1)^{1/2}] * e^{[-n - (n^2 - 1)^{1/2}] \omega t} \right\}$$

which can be reduced to the usual three cases [8]:

a) Case I; $0 < n < 1$

(Eq. B.31a)

$$V_0(t) = H * a_0 * u(t) * \left\{ 1 - \frac{e^{-n\omega t}}{(1-n^2)^{1/2}} \cos[(1-n^2)^{1/2} \omega t] \right. \\ \left. - \frac{n}{(1-n^2)^{1/2}} e^{-n\omega t} \sin[(1-n^2)^{1/2} \omega t] \right\}$$

(Eq. B.31b)

$$= H * a_0 * u(t) * \left\{ 1 - \frac{e^{-n\omega t}}{(1-n^2)^{1/2}} \sin[(1-n^2)^{1/2} \omega t + \theta] \right\}$$

$$\text{where } \theta = \tan^{-1} \frac{(1-n^2)^{1/2}}{n}.$$

b) Case II; $n = 1$

$$V_0(t) = H * a_0 * u(t) * [1 - (1 + \omega t) e^{-\omega t}] \quad (\text{Eq. B.31c})$$

c) Case III; $n > 1$

(Eq. B.31d)

$$V_o(t) = H * a_o * u(t) * \left\{ 1 - e^{-n\omega t} \cosh[(n^2-1)^{1/2} \omega t] \right. \\ \left. - \frac{n}{(n^2-1)^{1/2}} * e^{-n\omega t} \sinh[(n^2-1)^{1/2} \omega t] \right\}$$

(Eq. B.31e)

$$V_o(t) = H * a_o * u(t) * \left\{ 1 - \frac{1}{2} \left[1 + \frac{n}{(n^2-1)^{1/2}} \right] e^{[-n+(n^2-1)^{1/2}] \omega t} \right. \\ \left. - \frac{1}{2} \left[1 - \frac{n}{(n^2-1)^{1/2}} \right] e^{[-n-(n^2-1)^{1/2}] \omega t} \right\}$$

Note that for Case I, from (Eq. B.31b), the envelope of the transient response is given by the pair of curves defined by the relationship $1 + [e^{-n\omega t} / (1-n^2)^{1/2}]$, while the envelope of the transient responses for Case II and Case III are simply the curves themselves, as given by (Eq. B.31c) through (Eq. B.31e).

B.4.2 Determination of Optimal Value of Damping Factor, n , for Most Rapid Settling Time, from Fractional Error

The fractional error, which we consider to be defined as shown:

(Eq. B.32a)

$$\text{Fract. Err.} = | [V(t) - V_{\text{ideal}}(t)] / V_{\text{ideal}}(t) |,$$

where $V_{\text{ideal}}(t)$ is the ideal step voltage output given by:

$$V_{\text{ideal}}(t) = H * a_o * u(t) \quad (\text{Eq. B.32b})$$

and is given for the three cases mentioned above in (Eq. B.33a) through (Eq. B.33c).

a) Case I; $0 < n < 1$ (Eq. B.33a)

$$\text{Fract. Err.} = \left| \frac{e^{-n\omega t} \sin[(1-n^2)^{1/2} \omega t + \tan^{-1} (1-n^2)^{1/2}]}{(1-n^2)^{1/2}} \right|$$

b) Case II; $n = 1$

$$\text{Fract. Err.} = (1+\omega t)e^{-n\omega t} \quad (\text{Eq. B.33b})$$

c) Case III; $n > 1$

(Eq. B.33c)

$$\begin{aligned} \text{Fract. Err.} = \frac{1}{2} \{ & [1 + n/(n^2-1)^{1/2}] e^{[-n+(n^2-1)^{1/2}]\omega t} \\ & + [1 - n/(n^2-1)^{1/2}] e^{[-n-(n^2-1)^{1/2}]\omega t} \} \end{aligned}$$

To determine the conditions for n for the most rapid settling time, we are not really concerned with the fractional error as a function of time, but with the maximum upper bounds for the fractional error. Hence, we are more interested in the magnitude of the envelope of the transient response, which is given below for each case.

a) Case I; $0 < n < 1$

$$E(t) = \frac{e^{-n\omega t}}{(1-n^2)^{1/2}} \quad (\text{Eq. B.34a})$$

b) Case II; $n = 1$

$$E(t) = (1+\omega t)e^{-\omega t} \quad (\text{Eq. B.34b})$$

c) Case III; $n > 1$

(Eq. B.34c)

$$E(t) = \frac{1}{2} \{ [1 + n/(n^2-1)]^{1/2} \}_* e^{[-n+(n^2-1)^{1/2}]\omega t} \\ + [1 - n/(n^2-1)]^{1/2} \}_* e^{[-n-(n^2-1)^{1/2}]\omega t}$$

In order to solve for the settling time, we must set the magnitude of error as a function of time, $E(t)$, to some specific value, say F , for allowed fractional tolerance, then solve for t . The value of t thus obtained is then the time required for the system to settle to within the tolerance F . The equations below represent the solutions for the settling time, t , to within the fractional tolerance, F , for the three cases.

a) Case I; $0 < n < 1$

$$t = \frac{1}{n*\omega} [-\ln (1-n^2)^{1/2} - \ln F]$$

b) Case II; $n = 1$

For this case (Eq. B.34b) must be set equal to F , and the resulting transcendental equation solved for t by rearranging the equation so that the dominant term in t is on the left side of the equation. The equation may then be solved by iterative substitutions for t . The iterative equation is given by:

$$t = \frac{1}{\omega} [-\ln F + \ln (1+\omega t)] \quad (\text{Eq. B.35b})$$

Note that the end result of an infinite number of iterations will simply result in a constant divided by w for any given value of F . In our case, where $F = 2^{-15}$, we have, $t = (13.03905...)/w$ as a solution.

Case III; $n > 1$

Again, in this case, we have a transcendental equation in t , obtained from setting (Eq. B.34c) equal to a fixed value for F , and which may be solved in a manner identical to that described for Case II. The iterative equation is:

$$t = \frac{1}{\omega} * \frac{1}{[-n+(n^2-1)^{1/2}]} * \{ \ln [2*p*(n^2-1)^{1/2} + (n-(n^2-1)^{1/2})e^{-n-(n^2-1)^{1/2}}] \omega t_1 - \ln [n+(n^2-1)^{1/2}] \} \quad (\text{Eq. B.35c})$$

Note that this is an exact equation, completely equivalent to (Eq. B.34c), which would converge to an exact solution in an infinite number of iterations, and which converges very rapidly, even for a finite number of iterations.

The equations (Eq. B.35a) through (Eq. B.35c) were used to compute the values for settling time, t , as a function of n for $F = 2^{-15}$, that were used in the graphs shown in Fig. B.14 and in Fig. B.15.

Also note that, in the above equations, the results are always obtained in terms of $1/\omega$. That is, the settling time for any given tolerance F , will, for any given value of n , be equal to a proportionality constant multiplied by $1/\omega$.

This implies that for any given value of ω it is possible to determine an optimal value of damping factor, n , so that the settling time will be minimized for a given tolerance F . This may be accomplished by merely setting the derivative $dt/dn = 0$ for

Case I and Case II above.

For Case I, using (Eq. B.35a) and taking the derivative with respect to n , we have:

a) Case I; $0 < n < 1$ (Eq. B.36a)

$$\begin{aligned} dt/dn &= \frac{1}{(n^2 * \omega)} * [-\ln (1-n^2)^{1/2} - \ln F] - \frac{1}{n^2 \omega} * [n / (1-n^2)] \\ &= 0 \end{aligned}$$

The terms of this equation may be rearranged and given in the exact form:

$$\ln F = -\ln (1-n^2)^{1/2} + 1 - 1/(1-n^2), \quad (\text{Eq. B.36b})$$

The terms of this equation may be rearranged so that the following exact iterative equation in terms of the damping factor, n , results, as shown below.

(Eq. B.36c)

$$n = \sqrt{\frac{[-\ln F - \ln (1-n)^{2 \ 1/2}]}{1 + [-\ln F - \ln (1-n)^{2 \ 1/2}]}}$$

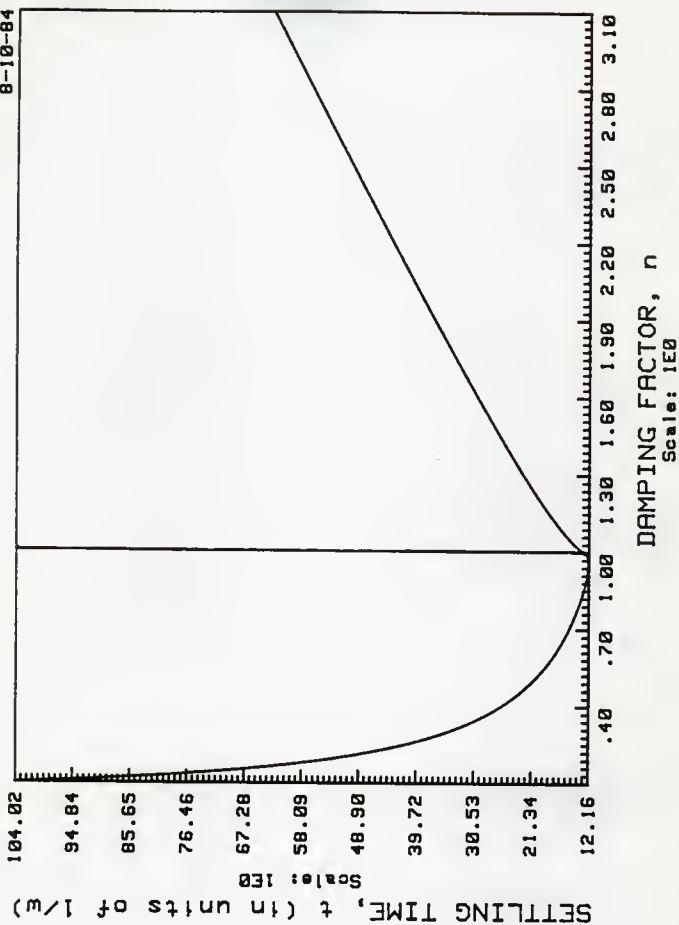
with the first order approximation being:

(Eq. B.36c)

$$n \approx \sqrt{\frac{\ln F}{-1 + \ln F}}$$

In our case, where $F = 2^{-15}$, the first order approximation is $n \approx 0.9551226...$, while the final approximation, correct to six decimal places, is $n \approx 0.959715$. This shows how close the first order approximation may be, using the iterative technique.

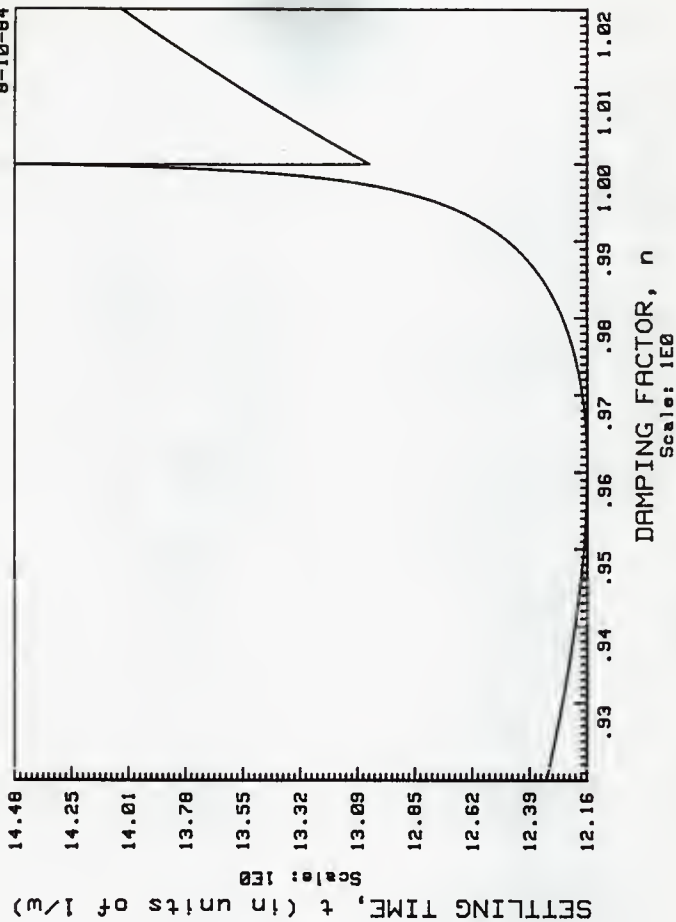
C. R. RAGSDALE
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SETTLING TIME VS. DAMPING FACTOR

Fig. B.14

C. R. RAGSDALE
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SETTLING TIME VS. DAMPING FACTOR

Fig. B.15.

B.4.3 The 2-Pole Analysis of an Operational Amplifier with Input Capacitance and Feedback Capacitance

Since the DAC-HA-14B has an output capacitance of 260 pf maximum, we may utilize a feedback capacitor to control the value of the damping factor and determine settling time. A model for the operational amplifier utilized in an inverting configuration with input capacitance and feedback capacitance is shown below.

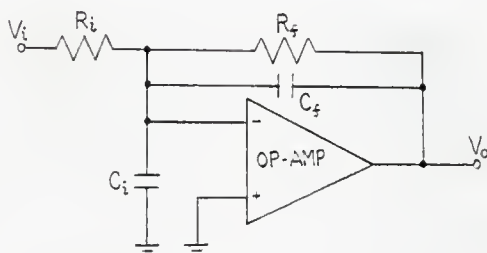


Fig. B.16 Inverting op-amp configuration with input capacitance (C_i) and feedback capacitance (C_f) shown.

An elementary circuit analysis of the above circuit by the usual methods yields:

$$V_o = \frac{-(Z_f/R_i) * V_i}{1 + (1 + \frac{Z_f}{R_i} + \frac{Z_f}{X_{C_i}}) * 1} \quad (\text{Eq. B.37a})$$

and, in the s-plane, where:

$$Z_f = R_f / [1 + (R_f * C_f) s], \quad (\text{Eq. B.37b})$$

and,

$$X_{C_i} = 1 / C_i * s \quad (\text{Eq. B.37c})$$

and,

$$A = A_o * \omega_o / (s + \omega_o), \quad (\text{Eq. B.37d})$$

we have a transfer function of the form:

$$V_o(s) = \frac{-(R_f/R_i)V_i(s)}{Ms^2 + Ns + P} \quad (\text{Eq. B.38a})$$

where:

$$M = [R_f(C_f + C_i)] / (A_o * \omega_o), \quad (\text{Eq. B.38b})$$

$$N = [(R_f * C_f) + \frac{R_f(C_f + C_i)}{A_o} + \frac{(1 + (R_f/R_i))}{A_o * \omega_o}], \quad (\text{Eq. B.38c})$$

$$\cong R_f * C_f, \quad (\text{Eq. B.38d})$$

$$P = [1 + \frac{(1 + (R_f/R_i))}{A_o}], \quad (\text{Eq. B.38e})$$

$$\cong 1.$$

Using the approximate values given above, we have:

$$V_o(s) \cong \frac{-(R_f/R_i)V_i(s)}{\frac{[R_f(C_f + C_i)]s^2}{A_o * \omega_o} + (R_f * C_f)s + 1} \quad (\text{Eq. B.39a})$$

which may easily be put in the form:

$$V_o(s) = \frac{H * \omega^2}{s^2 + (2 * \omega * n)s + \omega^2} * V_i(s) \quad (\text{Eq. B.39b})$$

by assuming that:

$$H = -R_f/R_i \quad (\text{Eq. B.39c})$$

$$\omega = \{(A_o * \omega_o) / [R_f(C_f + C_i)]\}^{1/2} \quad (\text{Eq. B.39d})$$

$$n = \frac{1}{2} * (R_f * C_f) * \omega \quad (\text{Eq. B.39e})$$

$$= \frac{1}{2} * (R_f * C_f) * \{(A_o * \omega_o) / [R_f(C_f + C_i)]\}^{1/2} \quad (\text{Eq. B.39f})$$

Note that since:

$$A_o * \omega_o = 2\pi * \text{GBW} \quad (\text{Eq. B.40})$$

we may write ω and the damping factor, n , directly as a function of the gain-bandwidth product, GBW, and we have:

$$\omega = \sqrt{\frac{2\pi * GBW}{R_f(C_f + C_i)}} \quad (\text{Eq. B.41a})$$

$$n = \frac{1}{2} * (R_f * C_f) \sqrt{\frac{2\pi * GBW}{R_f(C_f + C_i)}} \quad (\text{Eq. B.41b})$$

The above equations clearly show that for a given value of the gain-bandwidth product, GBW, feedback resistor, R_f , and input capacitance, C_i , that the value of the damping factor, and hence, the settling time of the system, can be controlled by the value of the feedback capacitance, C_f .

Since we wish to arrive at values of C_f for a desired value of damping factor, we may simply solve (Eq. B.41b) for C_f , and we get the useful relationship:

$$(\text{Eq. B.42})$$

$$C_f = \frac{2n}{R_f * (2\pi * GBW)} + \sqrt{\frac{4n}{[R_f * (2\pi * GBW)]^2} + \frac{4n^2 * C_i}{R_f * (2\pi * GBW)}}$$

For $n = 1$, we have $C_f = 20.7$ pf.

A graph of the settling time as a function of capacitance was plotted for the first DAC-follower, A1, assuming an input capacitance of 260 pf, using (Eq. B.41a), (Eq. B.41b) and (Eq. B.35a) through (Eq. B.35c), with the results shown in Fig. B.17 and Fig. B.18. Fig. B.18 shows the behavior of the settling time with more detail in the region $C_f = 19$ pf to $C_f = 21$ pf.

From these plots it is clear that we wish to avoid choosing the feedback capacitance, C_f , too close to 1, since there is a singularity present there (given the settling time criterion for

$n < 1$ to be the envelope, as given in (Eq. B.33a), which represents the worst case of values for the error signal). Considering the tolerance on actual physical capacitors, we may be in danger of selecting a value for which settling to within the specified tolerance is uncertain.

Therefore, it is evident, from Fig. 17, that we must choose a value of capacitance for C_f between 20.7 pf and 69.0 pf to stay within the limit of 7 μ S settling time to 1 part in 2^{15} as described earlier.

The value chosen for C_f was 59 pf, which was estimated to have a settling time of 5.94 μ S associated with it.

This choice leaves the DAC-HA-14B as the dominant pole, and the overall settling time of 7 μ S associated should be relatively undisturbed, since the output of the DAC-follower A1 will have settled to within 1 part in 2^{15} within 5.94 μ S.

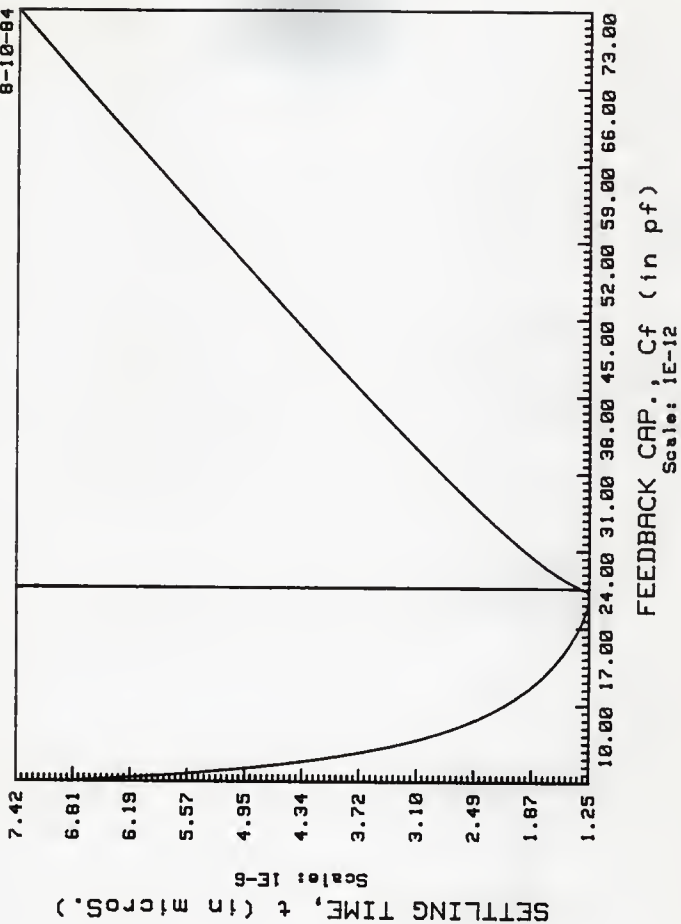
A similar analysis was performed for the second DAC-follower, A2, assuming an input capacitance ~ 2 pf, a value which may account for both stray capacitance and the capacitance of the op-amp itself. The value chosen for the feedback capacitance for A2 was 10 pf.

The expected results of this choice are summarized below in Table B.2.

Table B.2. C_f , n , and Settling Time, t , for A1 and A2

A1, ($C_{in} = 260$ pf)	$C_f = 59$ pf	$n = 2.68$	$t = 5.94$ μ S
A2, ($C_{in} \sim 2$ pf)	$C_f = 10$ pf	$n = 2.34$	$t = 0.99$ μ S

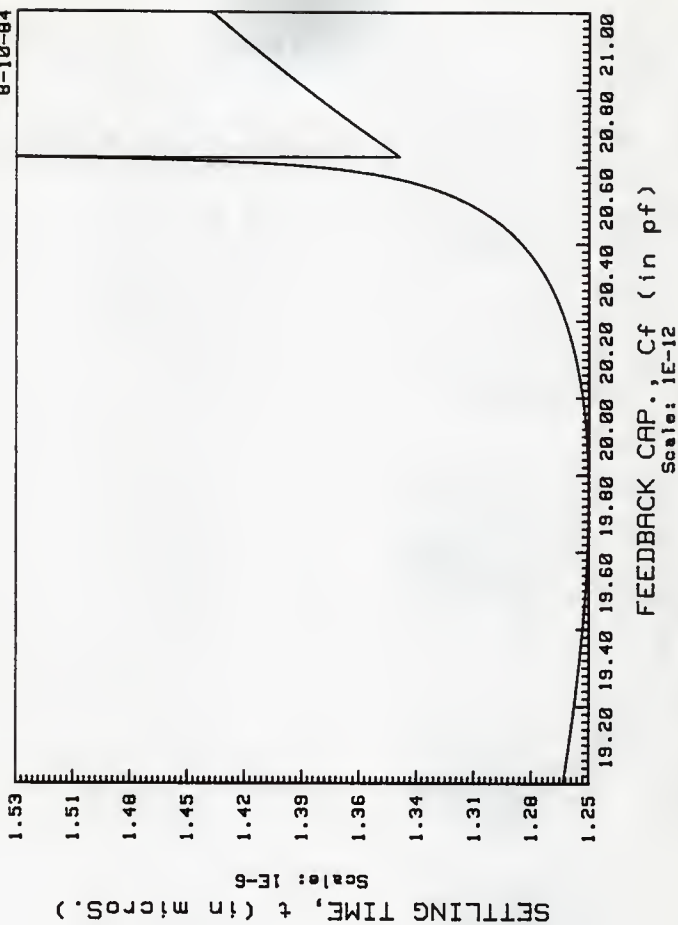
C. R. RAGSDALE
8-10-64



SETTLING TIME VS. FEEDBACK CAPACITANCE

Fig. B.17. Settling time as function of C_f

C. R. RAGSDALE
8-10-84



SETTLING TIME VS. FEEDBACK CAPACITANCE

Fig. B.18. Settling time as function of C_f

B.5 Comparator Resolution and CMRR

Since the comparator, must, at a minimum, be able to discriminate a voltage increment as small as 1/2 LSB, or 152.6 microvolts, we may use the equation:

$$V_o = A * \Delta V, \quad (\text{Eq. B.43})$$

with V_o expected to represent a maximum voltage swing ~ 10 V, and ΔV expected to be 152.6 microvolts, so that the value of A must then be 65,536 minimum.

Since the comparator must be able to resolve 1/2 LSB, or 152.6 microvolts out of 5 V, (which implies a resolution of 1 part in 2^{15}), this represents a CMRR of 90.3 dB. This would be required for no more than 1/2 LSB out of the entire range of 5 V. However, a CMRR of as low as only 84.3 dB would be required in order to obtain only 1 LSB error in this range.

The comparator CMP-04 chosen for use in the circuit has a minimum gain of 80,000, and a typical gain of 200,000 and a minimum CMRR of 80 dB, with a typical value of 100 dB. Evidently, all the specifications are met very closely and are exceeded in the typical case. It may be possible, however, to find an occasional CMP-04 which would have slightly more than 1 LSB of error associated with it, due to low CMRR.

The PM339AY has almost identical characteristics, but a lower minimum gain, making the CMP-04 the comparator of choice.

B.6 Noise

The largest source of noise would, from a theoretical standpoint, be the noise put out by the sample-and-hold circuits to the comparators, which was given to be 50 microvolts peak-to-peak [1].

B.6.1 Noise Resulting from Power Supply Ripple Due to Isolation Network Capacitor Discharge

The next largest source of noise would come from the power supply ripple associated with the discharge of the capacitors in the isolation network through the circuit components.

This ripple voltage would contribute $\sim 41.7 \mu\text{V}$ to the noise level. The calculations for this will be described in detail in the section on miscellaneous sources of error.

B.6.2 Operational Amplifier Noise

Since the operational amplifiers used as DAC-followers have at most (in the case of A2) a bandwidth of 1.59 MHz due to the resistor and capacitor values in the feedback loop, a calculation by the usual methods indicates a maximum noise contribution of only $3.78 \mu\text{V}$, which may be considered insignificant.

B.6.3 Combined Noise Voltage

Considering these components of noise as uncorrelated sources, we may figure the overall peak-to-peak noise voltage as being the square root of the sum-of-squared noise voltages, as usual, and we arrive at an estimated overall random noise voltage of $\sim 65 \mu\text{V}$.

B.6.4 External Noise Sources

It should be noted that the above value does not take into account the noise entering the circuit from external sources, such as the microprocessor and control logic section. Realistically, this could be expected to be the largest source of noise. However, since this noise cannot be predicted in advance and would depend on microprocessor and control logic design, it could not be taken into account from a strictly theoretical

standpoint. (It is worthwhile to note, however, that when the actual noise measured on the external +7.5 VDC power supply line, which was determined to be ~ 50 mV p-p, was taken into account, and assuming -52.2 dB of external isolation, as described in the succeeding section, the resulting noise at the supply terminals was estimated at ~ 123 μ V, close to the measured value of 152.6 μ V. This may imply a lower PSRR than expected at 100 kHz for one or more of the components.)

B.7 Isolation Network

It can be considered that noise coming from the digital control logic (which we shall consider to be the "external noise" source), and noise coming from the operation of the analog components (which we shall consider here as "internal noise") both have a fundamental harmonic at 100 kHz, due to the fact that all major transitions occur in 10 μ S intervals.

An isolation network was designed to eliminate as much noise from both sources as possible, by placing two poles of a low-pass filter from the external power supply to each device, and placing three poles of a low-pass filter between the supply pins of each device, as shown in the partial diagram, Fig. B.17, below. The "on" resistance of the DG308CJ analog switches, which has a value of approximately 100 Ohms constitutes of the R-C network, as shown in the diagram below.

Calculation of the frequency response was performed by the Hewlett-Packard program "A-C Circuit Analysis" with the results shown in Figs. B.20 through B.23.

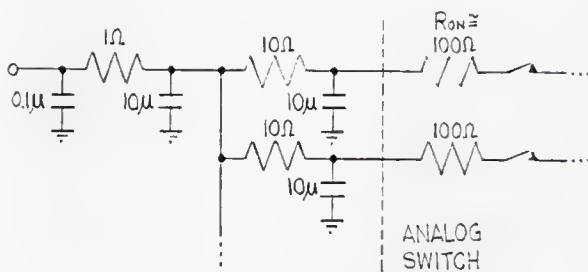


Fig. B.19 Partial diagram, isolation network

ISOLATION NETWORK
 C. RAGSDALE 10/23/63
 EXT. ISOL., dB
 for $R_o=1.0$ Ohms

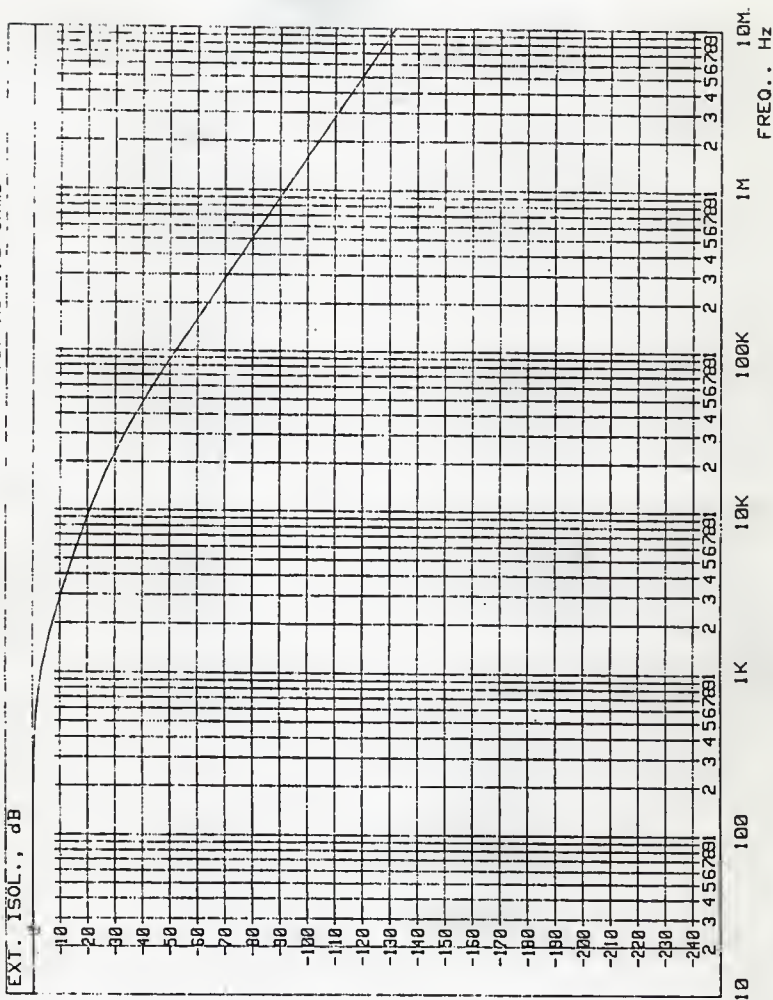


Fig. B.20. External isolation, Bodé plot

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-----
LOG SWEEP
START FREQUENCY = 10 Hz
END FREQUENCY = 10 MHz
OUTPUT ON PRINTER
24 INTERVALS
FREQUENCY          MAGNITUDE (dB)          PHASE (Deg)
10.00 Hz           - .00                   - .61
17.78 Hz           - .00                   -1.09
31.62 Hz           - .00                   -1.93
56.23 Hz           - .01                   -3.44
100.00 Hz          - .05                   -6.10
177.83 Hz          - .14                   -10.77
316.23 Hz          - .44                   -18.73
562.34 Hz          -1.26                   -31.31
1.00 kHz           -3.15                   -48.04
1.78 kHz           -6.41                   -65.26
3.16 kHz           -10.71                  -79.84
5.62 kHz           -15.58                  -92.37
10.00 kHz          -20.89                  -105.43
17.78 kHz          -26.93                  -121.16
31.62 kHz          -34.19                  -138.72
56.23 kHz          -42.77                  -154.13
100.00 kHz         -52.21                  -164.82
177.83 kHz         -62.02                  -171.34
316.23 kHz         -71.96                  -175.11
562.34 kHz         -81.94                  -177.25
1.00 MHz           -91.93                  -178.45
1.78 MHz           -101.93                 -179.13
3.16 MHz           -111.93                 -179.51
5.62 MHz           -121.93                 -179.72
10.00 MHz          -131.93                 -179.84
-----

```

Fig. B.21. External isolation, data

C. RAGSDALE 10/23/83

for $R_o = 1.0$ Ohms

ISOLATION NETWORK
ISOLATION (dB) vs. FREQUENCY (Hz)

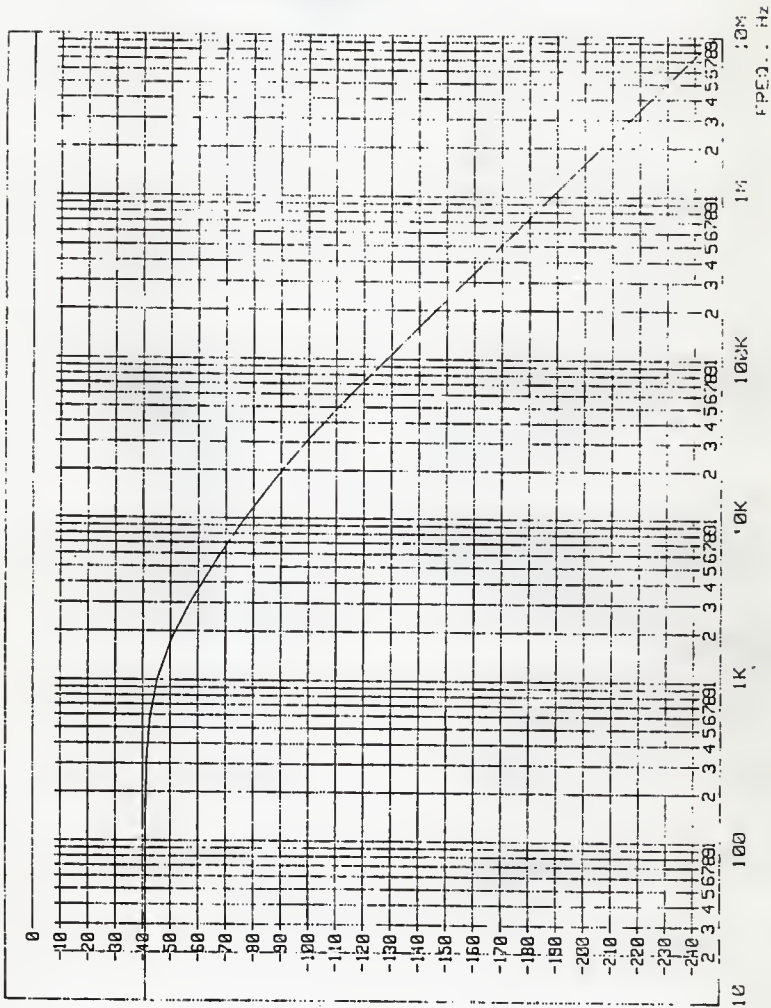


Fig. B.22 Internal isolation, Bode plot

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LOG SWEEP
START FREQUENCY = 10 Hz
END FREQUENCY = 10 MHz
OUTPUT ON PRINTER
24 INTERVALS

```

FREQUENCY	MAGNITUDE (dB)	PHASE (Deg)
10.00 Hz	-40.91	-.93
17.78 Hz	-40.91	-1.66
31.62 Hz	-40.91	-2.94
56.23 Hz	-40.92	-5.23
100.00 Hz	-40.96	-9.28
177.83 Hz	-41.09	-16.42
316.23 Hz	-41.47	-28.74
562.34 Hz	-42.55	-48.79
1.00 kHz	-45.21	-77.46
1.78 kHz	-50.31	-110.55
3.16 kHz	-57.83	-140.83
5.62 kHz	-66.94	-165.07
10.00 kHz	-76.98	174.50
17.78 kHz	-87.93	154.46
31.62 kHz	-100.16	134.45
56.23 kHz	-113.74	117.66
100.00 kHz	-128.18	106.18
177.83 kHz	-142.98	99.22
316.23 kHz	-157.92	95.21
562.34 kHz	-172.90	92.93
1.00 MHz	-187.89	91.65
1.78 MHz	-202.89	90.93
3.16 MHz	-217.89	90.52
5.62 MHz	-232.89	90.29
10.00 MHz	-247.89	90.17

Fig. B.23. Internal isolation, data

The performance of the circuit at 100 kHz, the fundamental harmonic of the noise expected from both internal and external sources is summarized in the table below.

Table B.3 Isolation at 100 kHz Due to Isolation Network

Isolation, external: -52.2 dB

Isolation, internal: -128.2 dB

B.8 Miscellaneous Sources of Error

It is necessary to take into account several miscellaneous sources of error in this design. While most of the effects turn out to be negligible, it is necessary, first, to show that these effects are negligible in order to have complete confidence in the design.

B.8.1 Supply Voltage Ripple Due to Current Produced by Operation of Active Device through "On" Resistance of Analog Switch.

With regard to the effect of supply voltage ripple produced by the fluctuation of supply current due to the operation of an active device through the analog switches, the most critical case of this occurs for the DAC-followers. The active operation of the OP-37EZ, in the process of putting out voltages ranging from 0 V to 5 V, given the loading conditions shown in the circuit diagram on p. 5, will pull an additional 0 mA to 1 mA of current through the "on" resistance of the analog switch, where R_{ON} is estimated to be ~ 100 Ohms for the DG308CJ Analog Switch, resulting in a voltage drop across the analog switch of ~ 0 V to ~ 0.1 V. This supply voltage ripple will, in turn, result in a small change in the output voltage of the OP-37. This may be calculated in the

following manner [7].

Since the specifications for the OP-37EZ show that the power supply rejection ratio is approximately given by [5]:

$$\text{PSRR} = -20 \log P_o + 10 \log [1 + (f/f_o)^2]. \quad (\text{Eq. B.44})$$

where $P_o \cong 10^6$, and $f_o \cong 10$ Hz.

In real numbers, the PSRR may be expressed, for the purposes of s-plane analysis, as:

$$\text{PSRR} = \frac{s + \omega_o}{P_o * \omega_o}. \quad (\text{Eq. B.44b})$$

and the output voltage from the DAC-follower may be expressed as:

$$V_o = (1 + R_f/R_i) * \frac{s + \omega_o}{P_o * \omega_o} * V_{\text{sup}} \quad (\text{Eq. B.45})$$

where V_{sup} represents the supply voltage ripple, which in this case will be assumed have the form of a step function due to the nature of the operation of the DAC, and in consequence, V_{sup} can be written, in s-plane form, as:

$$V_{\text{sup}}(s) = V_r/s \quad (\text{Eq. B.46})$$

where $V_r = R_{\text{on}} * I_{\text{sa},+} \cong .100$ V.

Therefore, equation (B.45) may be written as:

$$V_o(s) = (1 + R_f/R_i) * \frac{s + \omega_o}{P_o * \omega_o} * \frac{V_r}{s} \quad (\text{Eq. B.47a})$$

$$= (1 + R_f/R_i) * \left[\frac{V_r}{P_o * \omega_o} + \frac{V_r}{P_o * s} \right] \quad (\text{Eq. B.47b})$$

(Eq. B.48a)

$$V_o(t) = (1 + R_f/R_i) * [\frac{V_r * \delta(t)}{P_o * \omega_o} + \frac{1}{P_o} * (V_r * u(t))]$$

Since, in this case, $R_f/R_i = 1$, $P_o \cong 10^6$, $\omega_o \cong 62.8 \bar{S}^1$, and $V_r = 0.100$ V, we get from this an impulse response, and a step-function one one-millionth of the step in the supply voltage V_r , all times a factor of 2 to take into account the gain, and:

$$V_o(t) = 3.18 * 10^{-9} \text{ V} * \delta(t) + .2 * 10^{-6} \text{ V} * u(t) \quad (\text{Eq. B.48b})$$

As can be seen, once the impulse response has died out, the residual effect is an error of .2 μV (that is, after the device has settled, the effect would be the same as if the PSRR for DC of 120 dB, or $1/10^6$, were applied to the ripple voltage).

B.8.2 Effect of Ripple Voltage Due to the Discharge of the Capacitors in the Isolation Network when Switches Turned On.

Due to the discharge of the capacitors in the isolation network through the switches to the circuit components when the switches are turned on, an exponential decrease in the supply voltage should be seen by the circuit components.

The worst case of this should occur for the DAC-followers, since when the analog switches supplying current are turned on, a quiescent supply current of 2.5 mA would cause a voltage drop across the 10 Ohm resistors in the isolation network of 25 mV, if the current was allowed to reach a steady state.

However, with consideration to the small signal equivalent of this circuit, it is evident that the voltage drop would approach the steady state in an exponential fashion, with a time constant obtained approximately by multiplying the 10 Ohm

resistance in the isolation network by the 10 microfarad capacitance, yielding a value for the time constant of 10^{-4} .

From this, we have an equation for the ripple voltage expected of the form:

$$V_{rip}(t) = V_r * e^{-\omega_1 * t}, \quad (\text{Eq. B.49})$$

where $V_r \cong 25$ mV, and $\omega_1 \cong 10^4$.

Using a method of analysis similar to that given for the ripple voltage previously, and giving consideration to the fact that in this case, we must pay attention to the fact that the PSRR for the positive and negative supplies is different, and that from the specifications, for the positive supply, $P_{O1} \cong 10^6$, and $\omega_{O1} \cong 44.0$ S⁻¹, and for the negative supply, $P_{O2} \cong 1.78 * 10^6$, and $\omega_{O2} \cong 62.8$ S⁻¹, and, in the s-plane, V_o is given by:

$$V_o(s) \cong [1 + (R_f/R_i)] * \left[\frac{s + \omega_{O1}}{P_{O1} * \omega_{O1}} - \frac{s + \omega_{O2}}{P_{O2} * \omega_{O2}} \right] * \frac{V_r}{s + \omega_1} \quad (\text{Eq. B.50})$$

and, ignoring the impulse term and the smallest term we obtain by solving the above equation and taking the inverse Laplace transform, we have:

$$(\text{Eq. B.51a})$$

$$V_o(t) \cong \left(1 + \frac{R_f}{R_i}\right) * \frac{P_{O2} * \omega_{O2} - P_{O1} * \omega_{O1}}{P_{O2} * \omega_{O2} * P_{O1} * \omega_{O1}} * (-V_r * \omega_1 * e^{-\omega_1 * t})$$

$$\cong -43.3 \mu\text{V} * e^{-10^4 * t}, \quad (\text{Eq. B.51b})$$

from the values given above. Since we expect t , the duration of

the "on" time to be $\sim 330 \mu\text{S}$, it is clear that with time, we may expect a difference in the output offset voltage of each DAC-follower to change, over the $330 \mu\text{S}$ interval, by approximately $41.7 \mu\text{V}$. We shall consider this to be part of the noise of the system, as this error occurs as a function of time which cannot be correlated with the random noise of the DAC-followers, or any other source of noise in the system.

B.8.3 Effect of the Offset Voltages and Currents for the DAC-followers

One of the most important set of parameters to consider, with regard to the DAC-followers, is the final output offset voltages, and, most especially, the difference between the final offset voltages, caused by E_{OS} and I_{OS} for the OP-37EZ op-amps used.

This is important because if the difference between the final output offset voltages is such that the positive and negative ranges overlap by more than 1 LSB, then a correctable error will occur, while if there is a gap between the positive and negative voltage ranges by more than 1 LSB, then there exists a region where no voltage comparisons can be made, and a differential linearity error of more than 1 LSB will inevitably occur around the voltage whose output code is "0". This situation is shown in Fig. 24.(a) and Fig. 24.(b).

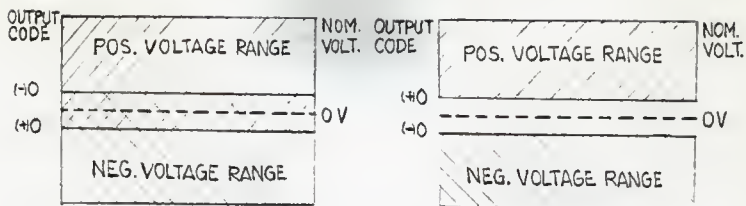


Fig. 24.(a) Overlap case, (b) Gap in voltage ranges.

For the generalized form of the circuit as shown in the circuit diagram in Fig. B.25, where R_{i1} will be considered to be the effective value of the input resistance represented by the $R-2R$ ladder of the DAC, we may compute V_{os1} and V_{os2} , the final output offset voltages from A1 and A2 respectively.

From this, we may compute the difference between them, a critical parameter with regard to the differential linearity of this circuit around 0 V input.

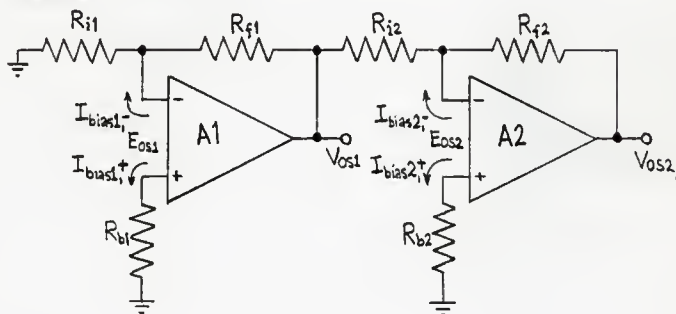


Fig. B.25. Generalized DAC-follower configuration.

For the generalized DAC-follower configuration shown in Fig. B.25, the values of V_{Os1} and V_{Os2} are obtained when R_{i1} is assumed to be infinite, and we have the equations:

$$V_{Os1} = \left(1 + \frac{R_{f1}}{R_{i1}}\right) * [E_{Os1} + (I_{bias1,pos} * \frac{R_{i1} * R_{f1}}{R_{i1} + R_{f1}}) - (I_{bias1,neg} * R_{b1})] \quad (\text{Eq. B.52a})$$

$$V_{Os2} = -\frac{R_{f2}}{R_{i2}} * V_{Os1} + \left(1 + \frac{R_{f2}}{R_{i2}}\right) * [E_{Os2} + (I_{bias2,pos} * \frac{R_{i2} * R_{f2}}{R_{i2} + R_{f2}}) - (I_{bias2,neg} * R_{b2})] \quad (\text{Eq. B.52b})$$

If we set R_{b1} and R_{b2} so that generally, $R_b = R_i * R_f / (R_i + R_f)$, for both A1 and A2, as is usually done to minimize the effect of I_{bias} , as is usually done, and assuming that the offset current is the difference between $I_{bias,pos}$ and $I_{bias,neg}$, then we have (Eq. B.52a) and (Eq. B.52b) becoming:

$$V_{Os1} = \left(1 + \frac{R_{f1}}{R_{i1}}\right) * [E_{Os1} + I_{Os1} * (\frac{R_{i1} * R_{f1}}{R_{i1} + R_{f1}})] \quad (\text{Eq. B.52c})$$

and:

$$V_{Os2} = -\frac{R_{f2}}{R_{i2}} * \left(1 + \frac{R_{f1}}{R_{i1}}\right) * [E_{Os1} + I_{Os1} * (\frac{R_{i1} * R_{f1}}{R_{i1} + R_{f1}})] + \left(1 + \frac{R_{f2}}{R_{i2}}\right) * [E_{Os2} + I_{Os2} * (\frac{R_{i2} * R_{f2}}{R_{i2} + R_{f2}})] \quad (\text{Eq. B.52d})$$

Since we only wish to determine the difference between V_{Os1}

and V_{Os2} around the point at which the ADC is outputting a binary code for "0", which is very close to an input voltage of 0 V, we will assume R_{i1} is infinite and that $R_{f1} = R_{i2} = R_{f2} = 10K$, which implies that:

$$R_{b1} = 10 K, \quad (\text{Eq. B.53a})$$

and

$$R_{b2} = 5 K, \quad (\text{Eq. B.53b})$$

since generally, $R_b = R_i * R_f / (R_i + R_f)$, which applies to both A1 and A2, then (Eq. B.52c) and (Eq. B.52d) reduce to:

$$V_{Os1} = E_{Os1} + I_{Os1} * (10 K) \quad (\text{Eq. B.54a})$$

$$V_{Os2} = - E_{Os1} - I_{Os1} * (10 K) + 2 * [E_{Os2} + I_{Os2} * (5 K)]$$

or (Eq. B.54c)

$$|V_{Os2} - V_{Os1}| = |2 * (E_{Os2} - E_{Os1}) + (I_{Os2} - 2 * I_{Os1}) * (10 K)|$$

It is clear, from (Eq. B.54c), that if A1 and A2 are matched with regard to E_{Os} , then the magnitude of the difference between V_{Os2} and V_{Os1} will be minimized, while no such simple case prevails with regard to I_{Os} .

Using typical values for E_{Os} and I_{Os} for A1 and A2, and assuming the op-amps are reasonably well matched, we obtain that the magnitude of the difference between V_{Os1} and V_{Os2} is typically 70 μ V.

To compute a reasonable upper bound for the magnitude of the difference between V_{Os1} and V_{Os2} , we will assume that A1 and A2

are poorly matched, with the parameters for A1 assuming maximum values, while the parameters for A2 assume minimal values. Therefore, we will assume that $E_{Os1} \approx 25 \mu V$, $I_{Os1} \approx 35 \text{ nA}$, and $E_{Os2} \approx 0 \mu V$, and $I_{Os2} \approx 0 \text{ nA}$. Then the magnitude of the difference in voltages for this maximum case is approximately $750 \mu V$, or approximately 2.5 LSB's.

It should be noted that if A1 and A2 are well matched, even for the maximum cases, then the magnitude of the difference between V_{Os1} and V_{Os2} should not exceed $350 \mu V$, or 1.1 LSB's.

To insure that there does not exist a differential linearity error of greater than $1/2$ LSB, which is to be desired, the op-amps for A1 and A2 should be as closely matched for E_{Os} and I_{Os} as possible and I_{Os} should not exceed 15.2 nA , a tolerance more than twice that typical for the OP-37EZ.

It is suggested that the difference in the offset voltages for A1 and A2 be controlled by screening and matching of the OP-37's, rather than by any adjustment, since adjustments should be avoided as much as possible, and since the E_{Os} and I_{Os} parameters are temperature dependent.

Furthermore, the screening and matching process is a fairly easy one.

All that is required is to build a circuit identical to that shown in Fig. B.23 for R_{i1} being infinite, and the values for R_{f1} , R_{b1} , R_{i2} , R_{f2} , and R_{b2} being the same as given previously, then measuring, first, V_{Os1} to make sure it is within approximately $162 \mu V$, (including $10 \mu V$ for E_{Os1}) and then measuring V_{Os2} , and making certain that the voltage difference between V_{Os1} and V_{Os2} does not exceed $152.6 \mu V$.

This is a simple procedure, and a process which could be automated.

Below is a summary of expected values for the magnitude of the difference between offset voltages V_{Os1} and V_{Os2} for the cases given above.

Table B.4 $|V_{Os2} - V_{Os1}|$, Expected Limiting Values.

i). Matched A1 and A2, typical values.

$$|V_{Os2} - V_{Os1}| \cong 70 \mu V. \quad (\sim 0.2 \text{ Bits})$$

ii). Matched A1 and A2, maximum values.

$$|V_{Os2} - V_{Os1}| \cong 350 \mu V. \quad (\sim 1.1 \text{ Bits})$$

iii). Mismatched A1 and A2, maximum values for A1

$$|V_{Os2} - V_{Os1}| \cong 750 \mu V. \quad (\sim 2.5 \text{ Bits})$$

B.8.4 Effect of Gain Error Associated with DAC-follower A2

There is a small gain error associated with the DAC-follower circuit due to the fact that the resistors are only specified to a tolerance of .01%.

Over the full range of 5V, this will result in an absolute error of ~ 3 LSB's maximum. However, since differential linearity is more important, and since this will only introduce an error of $\sim 1/10^4$ per bit, it may be considered insignificant.

B.9 Summary

The most important considerations in the design of the low power 15-bit ADC were power consumption, turn-on or warm-up time, measurement settling time, comparator resolution and CMRR, isolation from external noise and cross-talk provided by

the isolation network, and with regard to the performance of the circuit around 0 V, the relative offset of the DAC-followers A1 and A2.

This relative offset is controlled by the offset voltage and offset current of each of the DAC-followers. If the difference in offsets of A1 and A2 is not taken into account, a nonlinearity of 1/2 LSB or more can occur, but this can be avoided by proper screening and matching of the OP-37EZ's used as DAC-followers.

The process of screening and matching can be facilitated, even automated by the process outlined briefly above.

The above considerations are some of the most important with regard to the design.

Many of the effects considered, however, proved to be negligible, most notably those effects caused by the operation of the devices through the "on" resistance of the analog switches.

The importance of this lies in the fact that this validates the concept of using power switching techniques for power reduction on analog circuits requiring a high degree of accuracy and resolution.

APPENDIX C
TEST PROCEDURES, CIRCUITRY AND PROGRAMS
USED FOR POWER AND LINEARITY ERROR MEASUREMENTS

Given below are the basic test procedures, circuitry and programs used to measure power and differential linearity error. These methods were used to obtain the results that are listed in Appendix D.

C.1 Methods, Circuitry and Programs Used in Power Measurement

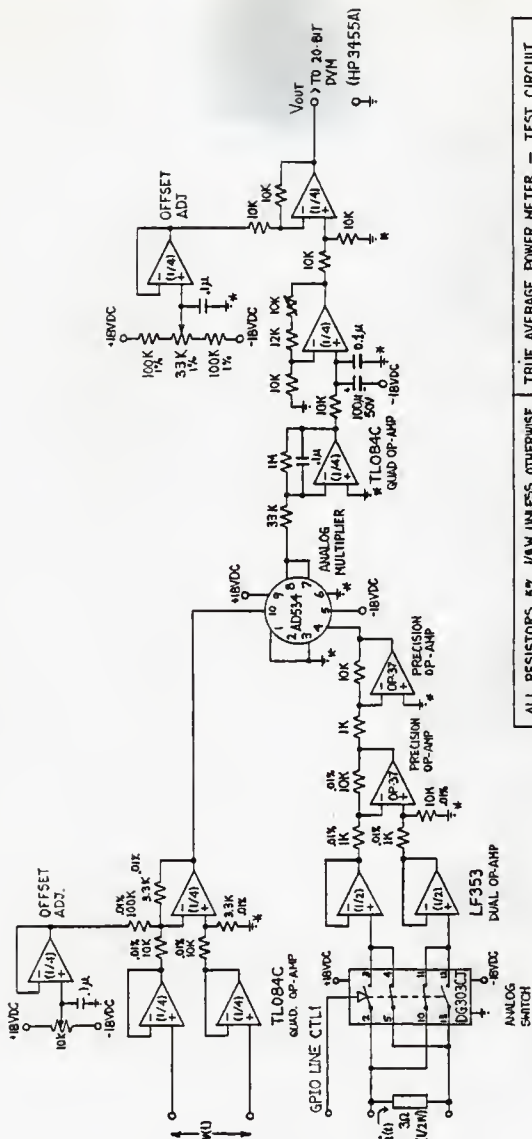
The power was measured using the true average power meter test circuit shown in Fig. C.1 and used in the automated test system shown in Fig. C.3.

C.1.1 Circuit Description for True Average Power Meter Test Circuit

C.1.1.1 General Description

The true average power meter test circuit was designed to compute the average power consumed by a device-under-test to within $\sim \pm 1\%$ in the range of 1 mW to 10 mW at DC and within a bandwidth of 4 decades from 10 Hz to 100 kHz from a measurement of the instantaneous voltage $v(t)$ and the instantaneous current $i(t)$ supplied to the device-under-test, the instantaneous current being measured by measuring the voltage drop across a 3 Ohm resistor placed in series with the current.

The true average power meter test circuit puts out a DC voltage proportional to the true average power to within $\pm 1\%$ (actually measured to be within $\sim .25\%$ typically) and an error voltage produced by the relatively low (~ 80 dB) CMRR, and an error voltage produced by the offset of the operational



TRUE AVERAGE POWER METER — TEST CIRCUIT
 CHARLES R. RASSDALE
 5-31-84
 DEPT. OF ELECTRICAL ENGINEERING
 K.S.U. FOR SANDIA LABORATORIES

ALL RESISTORS 5%, $1/8W$ UNLESS OTHERWISE SPECIFIED.
 $1\mu F$ CAPACITORS ARE CERAMIC
 $100\mu F$ CAPACITOR IS ELECTROLYTIC
 ALL POWER SUPPLIES $\pm 18VDC$

Fig. C.1. Circuit diagram for true average power meter

amplifiers used. (Both error voltages may be practically eliminated, as will be described later.)

C.1.1.2 Principle of Operation and Design

C.1.1.2.1 General Description

The true average power meter accomplishes the above tasks by simply multiplying a voltage proportional to the instantaneous voltage and a voltage proportional to the instantaneous current (with a suitable gain, in this case, a gain of ~ 100) together, by means of the AD534 Analog Multiplier, to get a voltage proportional to the instantaneous power.

Since true average power is simply the DC component of the instantaneous power (see reference [9]), we may simply filter the output of the analog multiplier. This is accomplished by two filters, the first being an active filter, which has, in addition, a gain of ~ 30 , the distinct advantage gained here is that the presence of the capacitor in the feedback loop helps to prevent voltage swings so large that the non-linear region around the voltage "rails" of the op-amp would be reached by the output voltage, a condition that could happen very easily, especially when measuring large pulses of current, and a second, passive, filter, which has a cut-off frequency of .159 Hz. The first filter was designed to cut out the higher frequencies, since the ceramic capacitor used has better properties at high frequency than the electrolytic capacitor used in the passive filter, a second advantage to this design.

The cut-off frequency of the first filter is 1.59 Hz. The

second filter insures that the output response at 10 Hz will be $\sim 1\%$ of any input signal, as a simple calculation will show, and therefore insuring that errors above 10 Hz will be no more than 1%. These filters are followed by a gain of ~ 3 , resulting in an overall gain such that the output of the test circuit for a measured power of 1 mW corresponds to $\sim .9$ V. The exact gain is not critical, since only proportionality of the output signal to true average power is needed. A calibration factor will be determined by the automated system, as will be described later.

C.1.1.2.2 Bandwidth

The range of frequency over which the circuit may operate to within 1% accuracy is determined, on the low-frequency end, by the cut-off frequency of the passive filter.

On the high frequency end, the limiting frequency for operation with $\sim 1\%$ accuracy is determined primarily by the difference in closed-loop phase shift between the voltage measuring section and the current measuring section, since after the DC-component of the product is taken, the resulting measurement will be proportional to the cosine of the phase difference between the two.

The circuit is, therefore, only accurate when the cosine of the phase difference is as close to unity as possible, which will occur only when the phase difference is very small. This implies that the gain stages for the voltage and current measuring sections must be designed for an equal phase shift, as closely as is possible, over the entire frequency range, despite the great difference in gains between the two stages.

For the current measuring section, with its much greater

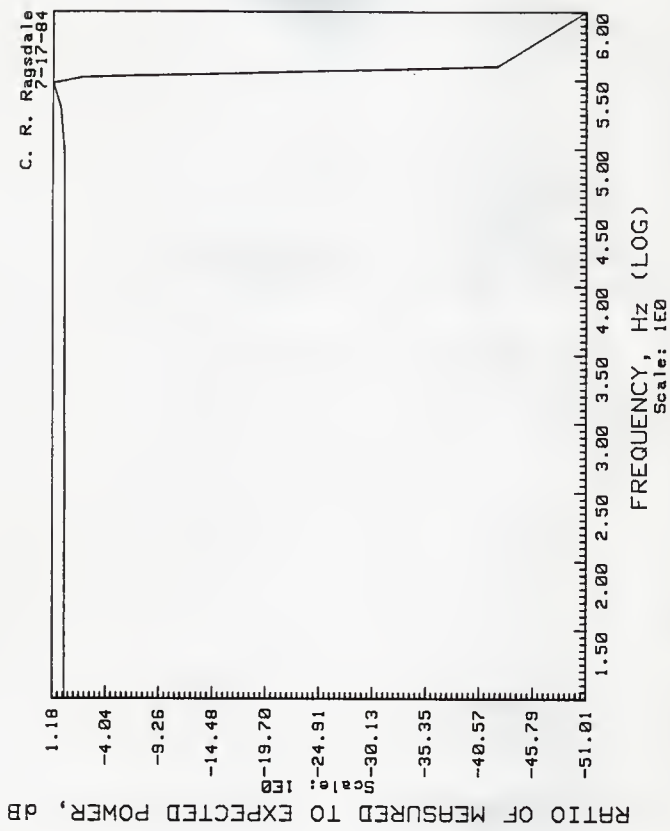
gain, this requires that the overall large gain be accomplished in stages, using much higher gain-bandwidth product operational amplifiers than are used in the voltage measuring section. The next most important factor in determining the upper limit on frequency is the magnitude of the outputs of the voltage and current measuring sections as a function of frequency, a condition requiring that the gain-bandwidth products of the operational amplifiers used be as high as possible, generally.

Other factors in determining the upper limit are the roll-off with frequency of the CMRR, the high frequency poles of the operational amplifiers, and the frequency response of the analog multiplier.

To get very much better performance than this at high frequencies would require the use of much faster (and more expensive) components.

This frequency response should be sufficient for our needs, as 100 kHz, the limit for ~ 1% accuracy, represents very nearly the 1000th harmonic for the voltage and current pulses they will be used to measure, since the fundamental harmonic is 128 Hz for the low duty-cycle voltage and current pulses associated with the switched power supply of the 15-bit ADC.

The actual measured frequency response of the true average power meter is given in Fig. C.2 on the following page. As can be clearly seen, the measured performance is very close to that expected for the circuit, with the 1% frequency range extending



FREQ. RESP., TRUE AVG. PWR. METER TEST CKT.

Fig. C.2. Measured frequency response, avg. power meter

very nearly from 10 Hz to 100 kHz. The actual data points were taken from the complete calibration section listed in Appendix D.

C.1.1.2.3 Problems Associated with the Power Meter Design

Some of the problems associated with this circuit design are the low CMRR (~ 80 dB), and the offset voltage of the gain stages, and $1/f$ noise.

The low CMRR comes from being able to specify or measure resistor tolerances of only .01% in the initial difference amplifier, which corresponds to an error of approximately $1/10^4$, or when estimating CMRR, ~ 80 dB, at low frequencies. This is a particularly important parameter when measuring current, since the common mode signal may be as high as ~ 7.5 V, while the difference mode signal, which is measured across the 3 Ohm resistor, may range from only a few millivolts down to a few microvolts.

The offset of the gain stages tends to be particularly severe, considering that the offset of the initial stages is multiplied by a factor of ~ 1000 . Typically, the output tends to be offset by ~ 1 V, but this can be reduced initially by the offset adjustments shown in the circuit diagram.

C.1.1.2.4 Solution to Problems

Both the effects of CMRR at low frequency and the offset may be nearly eliminated by simply reversing the leads in the current measuring section, taking the difference in the measured output voltages of the power meter, and dividing by 2. While this is a fairly standard technique for eliminating CMRR from measurements, it is only as effective as the $1/f$ noise will permit, since $1/f$ noise will produce a slow variation in offset that introduces

error in sequential measurement, but this error is typically ~ .25 %. It should be especially noted that this technique will not remove the effects of CMRR at higher frequencies. Direct observation showed, however, that this does not present much of a problem for frequencies much below 100 kHz.

C.1.1.2.5 Corrected Power Measurements

A complete power measurement, then, consists of a single power measurement, a reversal of the leads to the current measuring section, a second measurement, and the computation of the difference in the two voltages representing the power measurements divided by 2, which yields a value that is proportional to the true average power.

C.1.2 The Automated Test System for True Average Power Measurements

It is the function of the automated test system, in part, to eliminate the problem of offset and CMRR at low frequencies by performing automatically the lead reversals, the required measurements, and all calculations. In addition, since the output of the true average power meter is only proportional to the average power, it is first necessary for the automated test system to compute a calibration factor.

C.1.2.1 Calibration

C.1.2.1.1 General Description

The calibration factor is computed from a carefully measured voltage across a known resistance, which provides a standard.

More exactly, this calibration factor is computed by applying a sinusoidal voltage of measured RMS value (using the

HP3455A Digital Voltmeter in the high resolution RMS voltage measurement mode) across a known resistance (measured previously using a GenRad Digibridge impedance measuring device), and from this, computing the average power, then measuring the power consumed by the resistor using the true average power meter using the techniques described previously, and computing the calibration factor necessary to convert the computed reading to give the same results in mW as that computed from the RMS voltage and the known resistance.

The program "POWERM", listed in the following section, controls the entire calibration procedure and all subsequent measurements.

C.1.2.1.2 Procedure

From a procedural standpoint, the calibration consists of loading and running the program "POWERM" on the HP9845B computer and physically connecting the power meter to the test resistor as shown in Fig. C.3, where the automated test system is shown connected for calibration, responding the appropriate query from the program "POWERM" for the measured value of the resistor, and entering this value with a carriage return. The program performs all the necessary operations to compute the calibration factor by setting the switch at the input to the DVM, via the GPIO lines, so that the DVM makes voltage measurements from across the test resistor, which is supplied with a sine wave input from the HP3325A Synthesizer/Function Generator, as shown in Fig. C.3, with the DVM in the high resolution RMS voltage measurement mode (set by the program). The average power is computed from the measured RMS voltage and known resistance by the usual means.

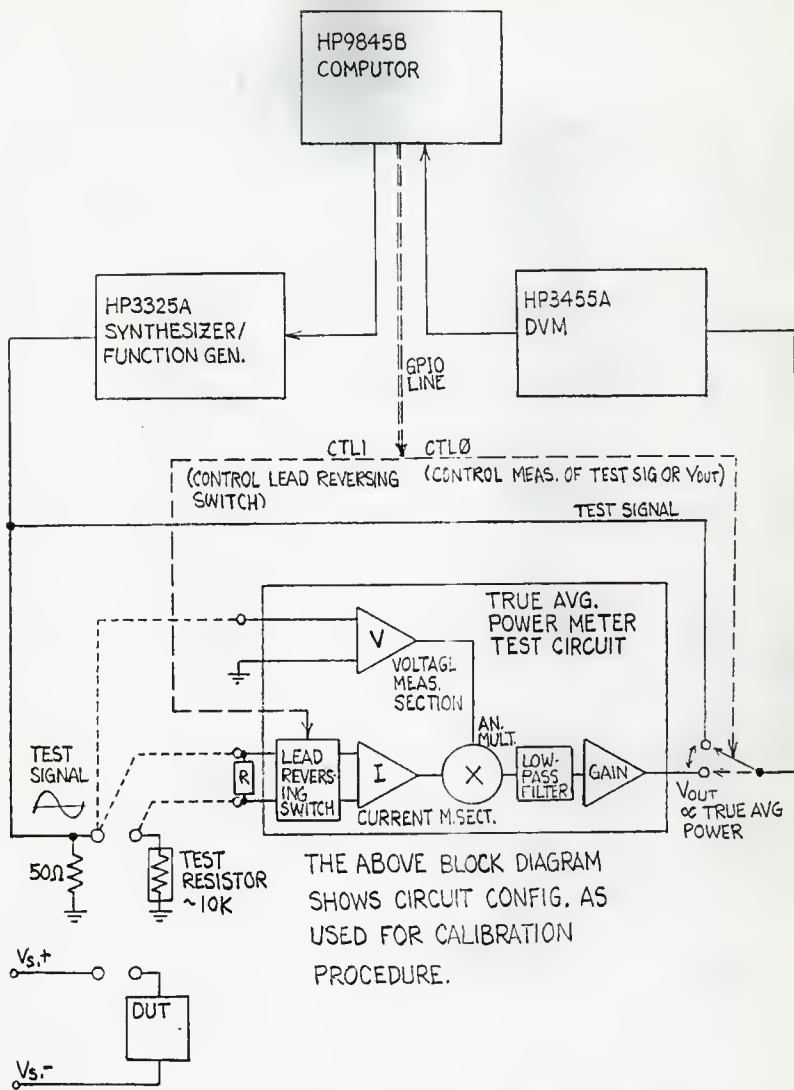


Fig. C.3. Block diagram, automated test system

Then the analog switch to the input to the DVM is set to read the voltage put out by the true average power meter test circuit, and a complete measurement is made as described previously, with the program "POWERM" causing the DVM (set by the program for high resolution DC measurements) to perform the necessary voltage measurements. The lead reversals to the current measuring section required for each measurement are controlled directly by the HP9845B via the GPIO lines connected to the analog switch at the input to the current measuring section of the true average power meter, as shown in Fig. C.3. The program calculates the calibration factor necessary to equate the value measured from the true average power meter test circuit to that measured by the DVM as described previously.

One of the options available with the "POWERM" program is a complete calibration, which includes a frequency response measurement, a measurement of drift in the true average power meter, and additional information.

C.1.2.2 Power Measurement

After the calibration procedures are complete, power measurements on the device-under-test may be performed, with the true average power meter connected physically to the device-under-test in a manner similar to that shown for the test resistor in Fig. C.3, with the leads to the 3 Ohm resistor of the current measuring section placed in series with the supply current to the device-under-test, and the voltage measured from the ground to the voltage supplied to the device-under-test. The program will set the switch at the input to the DVM to read only from the true average power meter and to perform the complete

power measurements as described earlier.

C.1.2.2.1 The Role of the Program in Power Computations

In actuality, the program performs a succession of measurements to arrive at an average value and an associated error.

The program can be used to compute total power measurements for each of the components, where two measurements are required, one on the positive supply line and one on the negative supply line, and also to compute a complete total for the power consumption of a large number of components in a system. (The program will handle up to 100 separate measurements.)

C.1.3 Program "POWERM"

C.1.3.1 General Description and Summary

The basic operating procedure for power measurement that the program "POWERM" follows has been largely described in the preceding section. In summary, the program performs all calculations for the calibration procedure, as well as for each separate and complete power measurement, including an estimation of error. The program handles all the lead reversal to the current measurement section to remove the effects of CMRR and offset. The program is interactive and allows entry of labelling statements for each power measurement recorded so that a complete record of the measurement process can be kept. Further power measurement is terminated when a comment entry of "STOP" or "NONE" is entered into the labelling statements. This section of the program is followed by the subtotal section where any subtotal (or difference) may be specified. The program requests a measurement number applying to a measurement contained in the

record previously kept, and uses this to add (or subtract if the number is preceded by a "-" sign) the measurement to the subtotal. An individual subtotal is terminated and the summed result, with proper propagation of measurement errors, is printed when an entry of "0" is made. The program can handle up to 100 subtotals from up to 100 separate measurements.

The actual program listing for "POWERM" begins on the following page.

```

10 | *****
20 |
30 | POWERM (POWER Measurement)
40 |
50 | PROGRAM DESIGNED TO AUTOMATE POWER MEASUREMENTS
60 |
70 | THIS PROGRAM MAKES EACH MEASUREMENT IN CONJUNCTION WITH
80 | THE TRUE AVERAGE POWER METER TEST CIRCUIT, WHICH MEASURES
90 | THE INSTANTANEOUS VOLTAGE AND CURRENT THROUGH THE DEVICE-
100 | UNDER-TEST, MULTIPLIES THE RESULT TO PRODUCE A VOLTAGE
110 | PROPORTIONAL TO THE INSTANTANEOUS POWER, AND THEN AVERAGES
120 | THIS VOLTAGE TO OUTPUT A VOLTAGE THAT, WHEN CMRR EFFECTS ARE
130 | TAKEN INTO ACCOUNT, IS PROPORTIONAL TO THE TRUE AVERAGE POWER.
140 |
150 | THIS PROGRAM TAKES THE EFFECT OF THE CMRR OF THE POWER METER
160 | INTO ACCOUNT BY ACTIVATING A SWITCH THAT REVERSES THE LEADS TO
170 | THE CURRENT MEASURING SECTION OF THE POWER METER, TAKING THE
180 | DIFFERENCES OF THE OUTPUT VOLTAGES OF THE METER AS MEASURED BY
190 | THE HP3455A DIGITAL VOLTMETER, AND DIVIDING THE RESULTS BY 2.
200 | ALL POWER MEASUREMENTS ARE MADE IN THIS FASHION, AND ARE AC-
210 | COMPLETED WITHIN THE PROGRAM BY SUBROUTINE Avg_power.
220 |
230 | THIS PROGRAM IS ALSO SELF-CALIBRATING, IN THAT IT ALSO USES
240 | THE HP3455A DVM TO MEASURE THE RMS VOLTAGE PROVIDED BY THE
250 | HP3325A SYNTHESIZER/FUNCTION GENERATOR ACROSS A RESISTOR OF KNOWN
260 | VALUE, COMPUTES THE POWER BY THE FACT THAT  $P_d = (V_{rms}^2)/R$ , THEN
270 | COMPUTES A CALIBRATION FACTOR THAT, WHEN MULTIPLIED BY THE
280 | CORRECTED OUTPUT OF THE POWER METER AS DESCRIBED ABOVE, WHICH
290 | IS ONLY PROPORTIONAL TO THE AVERAGE POWER, YIELDS A CORRECTED
300 | VALUE EQUAL TO THE POWER MEASURED BY THE DVM, WHICH IS USED AS
310 | THE STANDARD.
320 |
330 | THIS SELF CALIBRATION IS ACCOMPLISHED IN THE FIRST PART OF THE
340 | PROGRAM.
350 |
360 | THE FIRST PART OF THE PROGRAM ALSO INCLUDES THE OPTION OF A MORE
370 | COMPLETE CALIBRATION, WHICH INCLUDES A MEASURE OF THE DRIFT OF THE
380 | SYSTEM (MOST OF THE ERROR IN THE SYSTEM IS DUE TO 1/F NOISE IN THE
390 | AMPLIFIERS OF THE POWER METER TEST SYSTEM), AND ALSO A MEASUREMENT
400 | OF THE FREQUENCY RESPONSE OF THE SYSTEM. THE POWER METER IS DE-
410 | SIGNED TO BE ACCURATE TO ~1% OR BETTER FROM 1 Hz TO 100 KHz FOR
420 | MEASUREMENTS OF POWER IN THE RANGE OF 1 mW.
430 |
440 | THE PROGRAM PROMPTS THE USER THROUGHOUT, AND IS EASY TO USE.
450 |
460 | THE PROGRAM ALLOWS THE ENTRY OF NOTES TO LOG THE DIFFERENT POWER
470 | MEASUREMENTS MADE, DISPLAYS OR RECORDS THE RESULTING MEASUREMENTS ON
480 | HARDCOPY PRINTOUT, AND COMPUTES, IN ADDITION, THE APPROXIMATE ERROR
490 | ASSOCIATED WITH THE PARTICULAR MEASUREMENT. AN ADDITIONAL FEATURE IS
491 | THE OPTION TO ADD OR SUBTRACT THE RESULTS OF THE POWER MEASUREMENTS
492 | MADE. THE PROGRAM WILL ALSO HANDLE THE PROPAGATION OF THE ERRORS
493 | INCURRED WHEN COMPUTING THE SUM OR DIFFERENCES OF THE POWER MEASURE-
494 | MENTS. THIS ALLOWS THE USER TO EASILY COMPUTE A VALUE FOR THE TOTAL
495 | POWER USED BY A NUMBER OF DIFFERENT COMPONENTS IN A CIRCUIT, AND THE
496 | ERROR ASSOCIATED WITH THE TOTAL POWER MEASUREMENT.
497 |
500 | *****

```

```

510 !
511 ! *****
512 !
513 ! THIS SECTION ALLOWS USER TO SET PRINTER TO CRT OR HARDCOPY
514 !
520 INPUT "PRINTER IS 16 OR 0?",Pr
530 IF Pr=16 THEN PRINTER IS 16
540 IF Pr=0 THEN PRINTER IS 0
550 !
551 ! *****
552 !
553 ! THIS SECTION DIMENSIONS ARRAYS AND PRE-CONFIGURES
554 ! THE NP3455A DVM AND THE HP3325A FUNCTION GENERATOR
555 ! AND INITIALIZES VALUES
556 !
560 DIM Comm1$(300),P(100),E(100)
570 Voltmeter=722
580 Func_gen=717
590 RESET Voltmeter
600 OUTPUT Voltmeter;"F2R7T1M3A1N1D1"
610 OUTPUT Func_gen;"SMRD1FU1"
630 OUTPUT Func_gen;"FR10NZAM10V00F0V0"
631 !
632 ! *****
633 !
634 ! ALLOWS USEP TO ENTER VALUE OF TEST RESISTOR USED IN
635 ! SELF-CALIBRATION
636 !
650 INPUT "VALUE OF TEST RESISTOR (OHMS)=?",R
651 !
652 ! *****
653 !
654 ! CALLS SUBROUTINE Confirm TO GET CONFIRMING VALUES OF
655 ! POWER FOR SELF-CALIBRATION
656 !
660 GOSUB Confirm
661 !
662 ! *****
663 !
664 ! SECTION BELOW PROVIDES FOR SINGLE CALIBRATION AT FREQ.
665 ! OF 10 Nz.
666 !
670 FIXED 6
680 PRINT " "
690 PRINT "*****"
700 PRINT " "
710 PRINT "          10 NZ CALIBRATION (SINE WAVE)"
720 PRINT " "
730 PRINT "VALUE OF TEST RESISTOR (OHMS)=",R
740 PRINT " "
750 PRINT " "
760 PRINT "VOLTAGE RMS=",V_avg,"VOLTAGE PK=",V_avg*2^0.5
770 PRINT " "
780 PRINT "V RMS SIG=",V_sig,"V PK SIG=",V_sig*2^0.5
790 PRINT " "
800 PRINT "TRUE AVG POWER (MW)=",P_avg_mu,"+/-",P_err_mu
810 Flag=0
820 GOSUB Avg_power
830 Flag=1
840 PRINT " "
850 PRINT "V_POWER=",V_power,"+/-",V_power_err
860 Cal=P_avg_mu/V_power
870 Cal_err=Cal*((V_power_err/V_power)^2+(P_err_mu/P_avg_mu)^2)^0.5
880 PRINT " "
890 PRINT "CAL. FACTOR=",Cal,"+/-",Cal_err
900 P_meas_err1=P_meas*((V_power_err/V_power)^2+(Cal_err/Cal)^2)^0.5
910 PRINT " "
920 PRINT "POWER, (MW)=",P_meas*Cal,"+/-",P_meas_err1
930 PRINT " "
940 PRINT "*****"

```

```

951 |
952 | *****
953 |
954 | SECTION BELOW PROVIDES FULL CALIBRATION, INCLUDING DRIFT
955 | AND FREQUENCY RESPONSE MEASUREMENTS.
956 |
960 LIHPUT "DO YOU WANT FULL (FREQ.) CALIBRATION? (Y/N)",Resp$
970 IF Resp$(">")="Y" THEN GOTO 1720
980 PRINT " " FULL CALIBRATIONH"
990 PRINT " "
1000 PRINT " COMPUTE AVG. CAL. FACTOR"
1010 FOR G=1 TO 10
1020 OUTPUT Func_gen;"FR10HZ"
1030 GOSUB Confirm
1040 Flag=0
1050 GOSUB Avg_power
1060 Flag=1
1070 Cal=P_avg_mv/V_power
1080 Cal_avg=Cal_avg*(G-1)/G+Cal/G
1090 Cal_sig=(Cal_sig^2*(G-1)/G+(Cal-Cal_avg)^2/G)^.5
1100 PRINT Cal
1110 HEXT G
1120 PRINT " "
1130 PRINT "AVG CAL.=" ,Cal_avg,"CAL. ERR=" ,Cal_sig
1140 PRINT " "
1150 PRINT "PERCENT DRIFT=" ,100*Cal_sig/Cal_avg,"%"
1160 PRINT " "
1170 PRINT " FREQUENCY RESPONSE"
1180 PRINT " "
1190 PRINT " FREQ. (HZ) PWR. (MW) EXP. PWR. (MW) MEAS. RATIO
(dB)"
1200 PRINT " " ERROR
(%)"
1210 PRINT " "
1220 FOR H=1 TO 15
1230 IF H=1 THEN Freq=10
1240 IF H=2 THEN Freq=30
1250 IF H=3 THEN Freq=100
1260 IF H=4 THEN Freq=300
1270 IF H=5 THEN Freq=1000
1280 IF H=6 THEN Freq=3000
1290 IF H=7 THEN Freq=10000
1300 IF H=8 THEN Freq=30000
1310 IF H=9 THEN Freq=70000
1320 IF H=10 THEN Freq=100000
1330 IF H=11 THEN Freq=200000
1340 IF H=12 THEN Freq=300000
1350 IF H=13 THEN Freq=330000
1360 IF H=14 THEN Freq=400000
1370 IF H=15 THEN Freq=1000000
1380 OUTPUT Func_gen;"FR",Freq,"HZ"
1390 GOSUB Confirm
1400 GOSUB Avg_power
1410 GOSUB Print
1420 IF H<=9 THEN Avg_err=Avg_err*(H-1)/H+Perc_err/H
1430 HEXT H
1440 PRINT " "
1450 PRINT "AVG. % ERROR, 10HZ-100KHZ :",Avg_err
1460 PRINT " "

```

```

1470 PRINT " "
1480 OUTPUT Func_gen;"FU1FR1000HZAM10V00F0V0"
1490 GOSUB Confirm
1500 GOSUB Avg_power
1510 PRINT " "
1520 PRINT "          1 KHZ SINE WAVE RESPONSE"
1530 GOSUB Print1
1540 OUTPUT Func_gen;"FU2FR1000NZAM10V00F0V0"
1550 GOSUB Confirm
1560 GOSUB Avg_power
1570 PRINT " "
1580 PRINT "          1 KNZ SQUARE WAVE RESPONSE"
1590 GOSUB Print1
1600 OUTPUT Func_gen;"FU3FR1000NZAM10V00F0V0"
1610 GOSUB Confirm
1620 GOSUB Avg_power
1630 PRINT " "
1640 PRINT "          1 KHZ TRIANGULAR WAVE RESPONSE"
1650 GOSUB Print1
1660 OUTPUT Func_gen;"FU00F0V0"
1670 GOSUB Confirm
1680 GOSUB Avg_power
1690 PRINT " "
1700 PRINT "          GROUND (NO POWER) RESPONSE"
1710 GOSUB Print1
1711 |
1712 | *****
1713 |
1714 | SECTION BELOW PROVIDES FOR UP TO 100 SEPERATE POWER
1715 | MEASUREMENTS.
1716 |
1720 FOR K=1 TO 100
1721 |
1730 DISP "ENTER COMMENTS, MEASUREMENT #",K
1740 GOSUB Delay
1750 LINPUT Comm1$
1760 IF (Comm1$="NONE") OR (Comm1$="STOP") OR (Comm1$="END") THEN GOTO 1850
1770 DISP "HOOK UP V(t) AND I(t) CONNECTIONS FOR MEASUREMENT #",K
1780 PAUSE
1790 DISP "WORKING, POWER MEASUREMENT #",K
1800 GOSUB Avg_power
1810 GOSUB Print2
1820 P(K)=P_meas
1830 E(K)=P_meas_err
1831 |
1840 NEXT K
1841 |

```

```

1842 | *****
1843 |
1844 | SECTION BELOW ALLOWS USER TO SUBTOTAL ALL POWER
1845 | MEASUREMENTS.
1846 |
1850 DISP "DO YOU WISH SUBTOTALS? (Y/N)",Que$
1860 GOSUB Delay
1870 BEEP
1880 LINPUT Que$
1890 IF Que$(">Y") THEN GOTO 2100
1900 PRINT " "
1910 PRINT "BEGIN SUBTOTALS"
1920 PRINT " "
1930 FOR K2=1 TO 100
1940 P_sub=0
1950 P_sse_sub=0
1960 DISP "SUBTOTAL COMMENTS?"
1970 GOSUB Delay
1980 LINPUT Comm1$
1990 IF (Comm1$="NONE") OR (Comm1$="STOP") OR (Comm1$="END") THEN GOTO 2180
2000 PRINT "SUBTOTAL *****"
2010 PRINT " "
2020 PRINT Comm1$
2030 PRINT " "
2040 PRINT " "
2050 PRINT " "
2060 FOR K3=1 TO 100
2070 INPUT "MEASUREMENT #?",Mn
2080 IF Mn=0 THEN GOTO 2160
2090 IF Mn>0 THEN Sign=1
2100 IF Mn<0 THEN Sign=-1
2110 P_sub=P_sub+Sign*P(ABS(Mn))
2120 P_sse_sub=P_sse_sub+E(ABS(Mn))^2
2130 IF Mn>0 THEN PRINT "(+) MEASUREMENT",ABS(Mn),Sign*P(ABS(Mn)),E(ABS(Mn))
2140 IF Mn<0 THEN PRINT "(-) MEASUREMENT",ABS(Mn),Sign*P(ABS(Mn)),E(ABS(Mn))
2150 NEXT K3
2160 GOSUB Print3
2170 NEXT K2
2180 PRINT "DONE+*****"
2190 FIXED 12
2191 |
2192 |
2193 | *****
2194 |
2195 | END OF MAIN BODY OF PROGRAM
2196 |
2200 END
2201 |

```

```

2202 |
2210 | *****
2211 |
2212 | BEGINNING OF SUBROUTINES
2213 |
2219 | *****
2220 |
2230 | SUBROUTINE TO GENERATE SHORT DELAY
2240 Delay: |
2250 FOR K1=1 TO 2000
2260 |
2270 NEXT K1
2280 RETURN
2290 |
2300 | *****
2310 |
2320 | SUBROUTINE TO PRINT FREQ. RESPONSE OUTPUT
2330 |
2340 Print: |
2350 P_meas=P_meas+Cal_avg/Cal
2360 Ratio=P_meas/P_avg_mu
2370 Perc_err=ABS((P_meas-P_avg_mu)/P_avg_mu*100)
2380 PRINT Freq,P_avg_mu,P_meas,10*LGT(Ratio)
2390 PRINT " ", " ", " ", Perc_err
2400 PRINT " "
2410 RETURN
2420 | *****
2430 |
2440 | SUBROUTINE TO PRINT SQ. AND TRIANG. WV. MEASUREMENTS
2450 |
2460 Print1: |
2470 P_meas=P_meas+Cal_avg/Cal
2480 PRINT " "
2490 PRINT "PWR. (MW) EXP. PWR. (MW) MEAS. ERROR (%)"
2500 PRINT " "
2510 PRINT P_avg_mu,P_meas,ABS((P_meas-P_avg_mu)/P_avg_mu*100)
2520 PRINT " "
2530 RETURN
2540 | *****
2550 |
2560 | SUBROUTINE TO PRINT POWER MEASUREMENT DATA
2570 |
2580 Print2: |
2590 IF Resp$(">") THEN Cal_avg=Cal
2600 P_meas=P_meas+Cal_avg/Cal
2610 P_meas_err=P_meas_err+Cal_avg/Cal
2620 PRINT "MEASUREMENT #",K
2630 PRINT " "
2640 PRINT Comm1$
2650 PRINT " "
2660 PRINT "P_avg (MW) =",P_meas,"+/-",P_meas_err
2670 PRINT " "
2680 PRINT " ", "(+/-",P_meas_err/P_meas*100,"%)"
2690 PRINT " "
2700 PRINT "*****"
2710 RETURN
2720 | *****

```



```

2730 !
2740 Print3: !,
2750 PRINT ""
2760 PRINT "SUBTOTAL", " ", P_sub, P_sse_sub^.5
2770 PRINT ""
2780 PRINT "Pavg, (mW) =", P_sub, "+/-", P_sse_sub^.5
2790 PRINT ""
2800 PRINT " ", "(+/-", P_sse_sub^.5/P_sub*100, "%)"
2810 PRINT ""
2820 ! *****
2830 !
2840 ! SUBROUTINE TO MAKE CONFIRMATION VOLTAGE/POWER MEASUREMENTS
2850 ! UTILIZING THE DVM (HP 3455A)
2860 !
2870 Confirm: !
2880 OUTPUT Voltmeter;"F2R7T1M3A1H1D1"
2890 WRITE IO 3,5;3
2900 GOSUB Read_voltage
2910 FOR I=1 TO 25
2920 GOSUB Read_voltage
2930 V_avg=V_avg*(I-1)/I+Value/I
2940 V_sig=(V_sig^2*(I-1)/I+(Value-V_avg)^2/I)^.5
2950 NEXT I
2960 P_avg_mu=V_avg^2/R*1000
2970 P_err_mu=ABS(2-V_avg+V_sig/R)*1000
2980 RETURN
2990 !
3000 ! *****
3010 !
3020 ! *****
3030 !
3040 ! SUBROUTINE TO MAKE AVG. POWER MEASUREMENT, CORRECTED
3050 ! FOR CMRR
3060 !
3070 Avg_power: !
3080 OUTPUT Voltmeter;"F1R7T1M3A1H1D1"
3090 IF Flag=0 THEN Cal=1
3100 IF Flag=0 THEN Cal_err=0
3110 V_avg=0
3120 V_sig=0
3130 FOR J=1 TO 2
3140 IF J=1 THEN WRITE IO 3,5;0
3150 IF J=2 THEN WRITE IO 3,5;2
3160 FOR J1=1 TO 13000 !DELAY FOR POWER METER SETTLING
3170 NEXT J1
3180 FOR J1=1 TO 15
3190 GOSUB Read_voltage
3200 ! PRINT Value
3210 V_avg=V_avg*(J1-1)/J1+Value/J1
3220 V_sig=(V_sig^2*(J1-1)/J1+(Value-V_avg)^2/J1)^.5
3230 NEXT J1
3240 V_a(J)=V_avg
3250 V_s(J)=V_sig
3260 NEXT J
3270 V_power=ABS((V_a(1)-V_a(2))/2)
3280 V_power_err=.5*(V_s(1)^2+V_s(2)^2)^.5
3290 P_meas=V_power*Cal
3300 P_meas_err=P_meas*((V_power_err/V_power)^2+(Cal_err/Cal)^2)^.5
3310 RETURN
3320 ! *****

```

```

3330      !
3340      ! SUBROUTINE TO READ DVM VOLTAGE
3350      !
3360  Read_voltage:      !
3370      !
3380      TRIGGER Voltmeter
3390  Status:      !
3400      STATUS Voltmeter;Stat
3410      IF Stat=65 THEN Get_value
3420      IF Stat=0 THEN Status
3430      DISP "DVM ERROR"
3440      BEEP
3450      STOP
3460  Get_value:      !
3470      ENTER Voltmeter;Value
3480      RETURN
3490      !
3500      ! *****
3510      ! *****
3520      !

```

C.2 Methods, Circuitry and Programs Used in Differential Linearity Error Measurement

C.2.1 General Description

C.2.1.1 Programmable Voltage Reference Test Circuit

In order to measure the differential linearity error, it was first necessary to develop a device capable of putting out a voltage that could be regulated to within $\pm 1/2$ LSB. The device used is the programmable reference voltage test circuit shown in Fig. C.4, which is capable of being programmed by the HP9845B to supply any voltage within the range from +5 VDC to -5 VDC and regulating the voltage to within $\pm 6 \mu\text{V}$.

C.2.1.2 Basic Approach to Differential Linearity Error Measurement

The basic approach to linearity measurement is to locate specific bits of output code from the 15-bit ADC under test by finding the value of the input voltage needed to produce this value of output code.

The differential linearity error is measured by determining the voltage for any given bit for which the output code is the within $\pm 1/8$ LSB of the desired bit, then taking the difference in these input voltages (in bits, or units of $305.2 \mu\text{V}$) for decremented values of average output code, which ideally should represent a decrement of 1 bit of input code, and finding the absolute value of the difference between the measured value and the ideal value (see reference [2]). The differential linearity error is given by:

$$\text{Diff. Lin. Err.} = |(V_i - V_{i-1}) - 1| \quad (\text{Eq. C.1})$$

where V_i and V_{i-1} represent a voltage in bits for the i -th output code and $(i-1)$ -th output code respectively.

The error associated with this process is given by:

$$\text{Error, D.L.E.} \sim 0.177 \text{ LSB} \quad (\text{Eq. C.2})$$

The circuit and the algorithm used to compute the differential linearity error are described more exactly in the following sections.

C.2.2 Circuit Description for the Programmable Voltage Reference Test Circuit

C.2.2.1 General Description

The programmable voltage reference test circuit shown in Fig. C.4 is designed to regulate voltage by continuously re-measuring the output voltage and correcting for errors.

C.2.2.2 Principle of Operation

The test circuit performs this by first setting a voltage level calculated approximately by the computer to within 1 bit, which, for the 16-bit DAC, the MP9331, correspond to increments of 152.6 μV when using the REF-02 5V Reference as shown in the circuit diagram in Fig. C.4. Then the output of the test circuit is measured by the HP3455A DVM, and the difference between the output voltage and the desired voltage is computed, providing a calculated value for the voltage that must be added to get the output voltage to the desired value. The output DAC-follower has a resistor applied in the inverting adder configuration at a nominal ratio of 1:100, which can add a voltage 1/100th of a voltage supplied to it by the programmable HP3325A Synthesizer/Function Generator, shown in the block

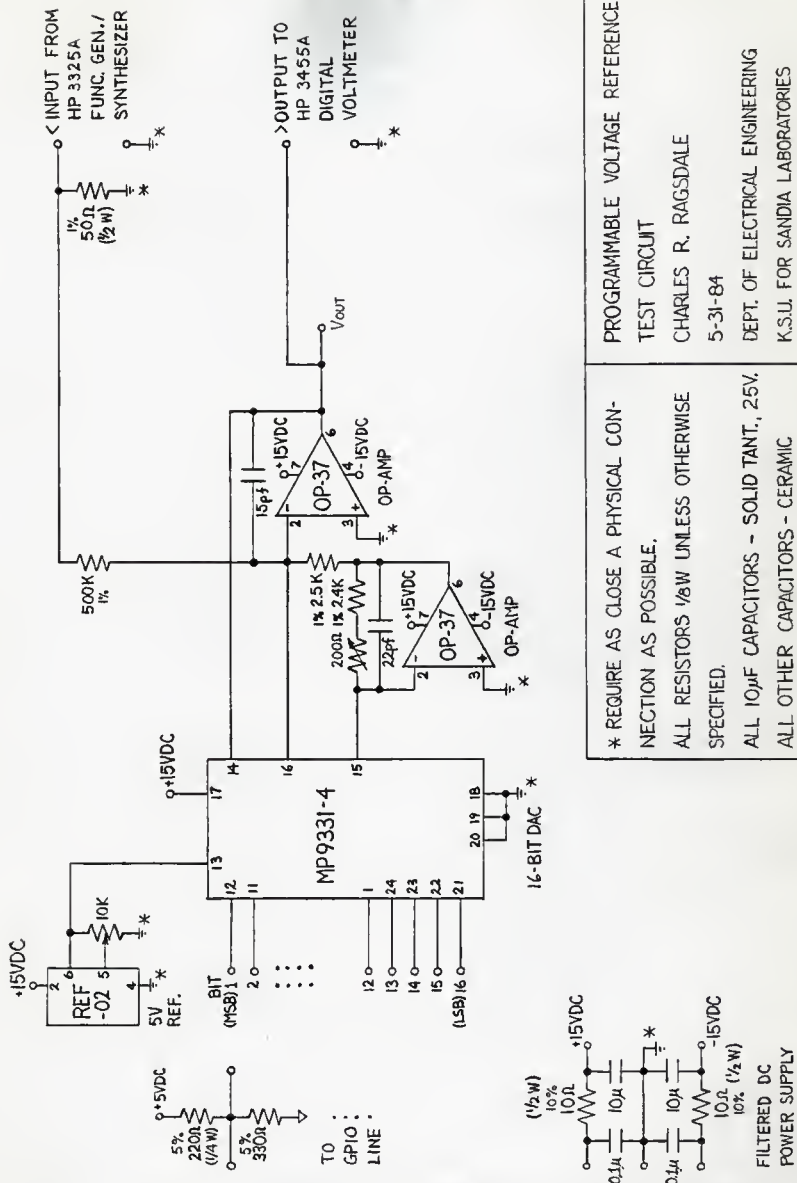


Fig. C.4. Circuit diagram, programmable voltage reference

PROGRAMMABLE VOLTAGE REFERENCE
TEST CIRCUIT
CHARLES R. RAGSDALE
5-31-84
DEPT. OF ELECTRICAL ENGINEERING
K.S.U. FOR SANDIA LABORATORIES

* REQUIRE AS CLOSE A PHYSICAL CON-
SECTION AS POSSIBLE.
ALL RESISTORS 1/4W UNLESS OTHERWISE
SPECIFIED.
ALL 10μF CAPACITORS - SOLID TANT., 25V,
ALL OTHER CAPACITORS - CERAMIC

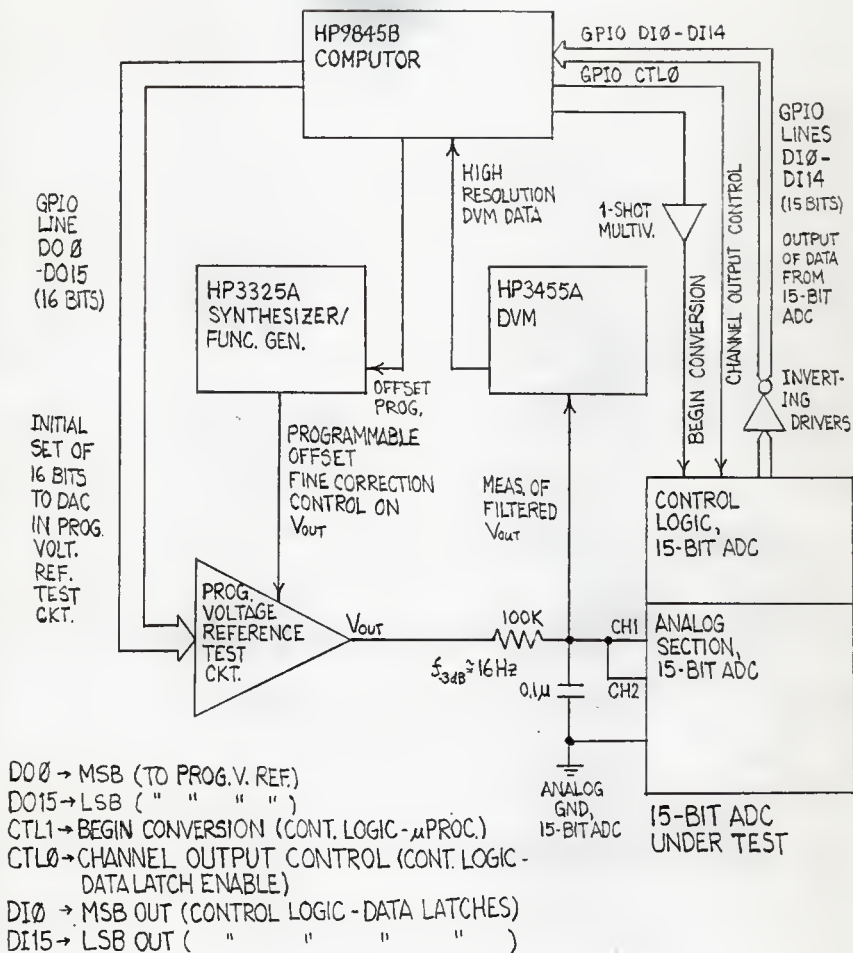


Fig. C.5. Block diagram, automated test system

diagram in Fig. C.5.

The program then computes a voltage 100 times the difference voltage computed above (the negative sign takes into account the inverting nature of the adder) and sets the programmable DC offset of the function generator to put out this additional voltage.

This process may be repeated indefinitely to regulate the voltage to typically within $\pm 6 \mu\text{V}$. Usually twenty such corrections are sufficient to set the voltage to within this tolerance, but continuous correction is necessary to maintain it.

Examples of the typical performance of the device may be found in Appendix E, which describes the operation of the program "VREF" and gives typical data from it illustrating the effectiveness of the circuit.

C.2.3 Algorithm and Program Used for Differential Linearity Error Measurement

C.2.3.1 General Description

The program used to measure the differential linearity error is "BTHNTR", a mnemonic for "Bit Hunter", which, in turn explains the basic function of the algorithm used to measure the differential linearity error, which is to hunt for specific "bits" of output code by finding the input voltage required to produce them.

C.2.3.2 Basic Algorithm

The basic process is similar in nature to the control system employed in the design of the programmable voltage reference test circuit, in that the difference between measured values and the

ideal value is used to supply correction.

The programmable voltage reference test circuit supplies the voltage calculated by the computer to yield a specific output code. The output code is then measured for approximately 16 trials (more may be used for greater resolution), and an average computed. The difference between this average output code and the desired number of bits is taken, and represents the correction needed (in bits or units of $305.2 \mu\text{V}$) to make the input voltage put out the desired output code.

This process is repeated as often as necessary to obtain an average output code that is within $1/8$ LSB of the desired code, with the exception that when oscillation around a particular output code is detected by comparison of the signs of the difference between output codes and desired codes in successive runs, then the computer tells the programmable voltage reference to increment by $1/2$ th of the difference, applying a heavy damping factor to the system, or $1/4$ th of the difference if oscillation is still detected. This helps overcome the effect of the noise output of the 15-bit ADC, the effect being that the noise causes the small increments of the ADC all but indistinguishable, and allows more averaging to be performed within the approximate area wherein the desired bit may be expected to be found. Up to 30 runs or trials for a particular output code are allowed by the program.

The program makes 497 separate differential linearity error measurements, with roughly 100 measurements being made in 5 input voltage ranges. The ranges are close to $+5 \text{ V}$ (desired output

codes are 16383 to 16285), + 2.5 V (desired output codes of 8242 through 8143), 0 V (+50 through -49), - 2.5 V (-8142 through -8241), and - 5 V (-16264 through -16383).

The program is given in the next section.

C.2.4 The Program "BTHNTR"

The basic explanation of the operation of program "BTHNTR" and the algorithm used was explained in the preceding section.

C.2.4.1 The Program Listing

The listing for the program is given on the following pages, and the data obtained is given in Appendix D.

```

10 | *****
20 |
30 | BTHNTR      ( B I T H U N T E R )
40 |
50 | PROGRAM USED TO DETERMINE LINEARITY OF 15-BIT
50 | A-D CONVERTER BY DETERMINING THE VOLTAGE
70 | REQUIRED TO PRODUCE A PARTICULAR OUTPUT CODE
90 | OF 15 BITS.
90 |
100 | THIS PROGRAM CHOOSES THE OUTPUT CODE DESIRED
110 | FROM A RANGE OF APPROXIMATELY 500 SAMPLE POINTS
120 | AS SHOWN BELOW.
130 |
140 | INPUT VOLTAGES      DESIRED OUTPUT CODES
150 |
160 | ~ +5.0 V           16383 TO 16285
170 | ~ +2.5 V           0242 TO 0143
180 | ~ 0.0 V            50 TO -49
190 | ~ -2.5 V          -8142 TO -0241
200 | ~ -5.0 V          -16264 TO -16303
210 |
220 | THE PROGRAM DECREMENTS THE DESIRED OUTPUT CODE
230 | WITHIN EACH RANGE AND ATTEMPTS TO FIND INPUT
240 | VOLTAGE CAPABLE OF PRODUCING DESIRED OUTPUT CODE.
250 |
260 | THE PROGRAM ACCOMPLISHES THIS BY MEASURING THE
270 | NUMBER OF BITS IT IS IN ERROR FROM THE DESIRED
280 | OUTPUT CODE, AND INCREMENTS THE INPUT VOLTAGE
290 | BY THAT NUMBER OF BITS.
300 |
310 | OSCILLATION IS DETECTED WHEN THE PRODUCT OF THE
320 | DIFFERENCES FROM THE DESIRED OUTPUT IS NEGATIVE,
330 | AND THE PROGRAM ATTEMPTS TO CORRECT FOR THIS BY
340 | ONLY INCREMENTING BY 1/2 THE NUMBER OF BITS IT IS
350 | IN ERROR BY, AND IF OSCILLATION IS STILL DETECTED,
360 | IT ONLY INCREMENTS BY 1/4 THE NUMBER OF BITS IN
370 | ERROR.
380 |
390 | IF AFTER 30 ATTEMPTS TO FIND THE DESIRED OUTPUT
400 | CODE IT IS UNABLE TO, IT PRINTS THAT THE DESIRED
410 | BIT "DOES NOT CONVERGE".
420 |
430 | THE MEASURED RESULTS OF THIS PROGRAM ARE STORED
440 | IN DATA FILE "SAMPLE"
450 |
460 |
470 | *****
480 |
490 | THIS PROGRAM HAS FOR DATA FILES: "SAMPLE"
500 |
510 | *****
520 |

```

```

530 |
540 | *****
550 |
560 PRINTER IS 0
570 PRINT " "
580 PRINT " "
590 PRINT " BIT NO.          PRESEHCE          STD. DEV.          VOLTAG
E"
600 PRINT " "
610 PRINT " "
620 INPUT "DO YOU WANT PRINTER TO BE 16 OR 0? (ANS.: 16 OR 0)",Pr
630 IF Pr=0 THEN PRINTER IS 0
640 IF Pr=16 THEN PRINTER IS 16
650 |
660 | *****
670 |
680 | THIS SECTION ASSIGNS "SAMPLE" AS THE DATA FILE
690 |
700 ASSIGN #1 TO "SAMPLE"
710 DIM Ch1(2)
720 |
730 | *****
740 |
750 | THIS SECTION PRECONFIGURES THE DVM FOR HIGH
760 | RESOLUTION DC VOLTAGE MEASUREMENTS AND THE
770 | FUNCTION GENERATOR FOR PROGRAMMABLE DC OFFSET,
780 |
790 Voltmeter=722
800 Func_gen=717
810 RESET Voltmeter
820 OUTPUT Voltmeter;"F1R7T1M3A1N1D1"
830 OUTPUT Func_gen;"SMRD1FU0"
840 |
850 | *****
860 |
870 | THIS SECTION DEFINES VOLTAGE ASSOCIATED WITH
880 | ONE BIT
890 |
900 Bit=5*2^(-14)
910 Bits=5*2^(-14)
920 Sum_miss=0
930 |
940 | *****
950 |
960 | THIS "FOR" LOOP COLLECTS THE DATA ON THE APPROX.
970 | 500 DATA POINTS.
980 |
990 FOR I=1 TO 500
1000 |
1010 Dif_bit=0
1020 B_p=0
1030 Dbflag=0
1040 |

```

```

1050 | *****
1060 |
1070 | THIS SECTION SELECTS THE DESIRED OUTPUT CODE
1080 | BY STARTING WITH APPROPRIATE INITIAL VALUES AND
1090 | DECREASING WITH EACH PASS THROUGH THE LOOP
1100 |
1110 IF I=1 THEN Num_bits=2^14-1
1120 IF I=1 THEN V_ideal=Num_bits*Bit
1130 IF (I>1) AND (I<100) THEN Num_bits=Num_bits-1
1140 IF (I>1) AND (I<100) THEN V_ideal=V_avg-Bit
1150 IF I=100 THEN Num_bits=2^13+50
1160 IF I=100 THEN V_ideal=Num_bits*Bit
1170 IF (I>100) AND (I<200) THEN Num_bits=Num_bits-1
1180 IF (I>100) AND (I<200) THEN V_ideal=V_avg-Bit
1190 IF I=200 THEN Num_bits=50
1200 IF I=200 THEN V_ideal=Num_bits*Bit
1210 IF (I>200) AND (I<300) THEN Num_bits=Num_bits-1
1220 IF (I>200) AND (I<300) THEN V_ideal=V_avg-Bit
1230 IF I=300 THEN Num_bits=-2^13+50
1240 IF I=300 THEN V_ideal=Num_bits*Bit
1250 IF (I>300) AND (I<400) THEN Num_bits=Num_bits-1
1260 IF (I>300) AND (I<400) THEN V_ideal=V_avg-Bit
1270 IF I=400 THEN Num_bits=-2^14+102
1280 IF I=400 THEN V_ideal=Num_bits*Bit
1290 IF (I>400) AND (I<500) THEN Num_bits=Num_bits-1
1300 IF (I>400) AND (I<500) THEN V_ideal=V_avg-Bit
1310 |
1320 | *****
1330 |
1340 Dbflag=0
1350 Dbflag1=0
1360 Dn=0
1370 Err=0
1380 |
1390 | *****
1400 |
1410 | THIS "FOR" LOOP ALLOWS UP TO 30 CORRECTIONS
1420 | OF INPUT VOLTAGE TO TRY TO DETERMINE THE
1430 | INPUT VOLTAGE REQUIRED TO OBTAIN A PARTICULAR
1440 | OUTPUT CODE OR THE AVERAGE TO WITHIN 1/8 LSB.
1450 |
1460 FOR I1=1 TO 30
1470 |
1480 | *****
1490 |
1500 | THIS CONDITION DECIDES WHETHER THE VOLTAGE
1510 | CAN BE DETERMINED OR NOT FOR A PARTICULAR
1520 | DESIRED OUTPUT CODE. IF IT CANNOT BE DETER-
1530 | MINED, THE BIT IS SAID TO NOT CONVERGE.
1540 |
1550 IF I1=30 THEN Err=1
1560 |

```

```

1570 | *****
1580 |
1590 | THIS SECTION DETERMINES THE VOLTAGE COR-
1600 | RECTION NECESSARY TO APPROACH THE INPUT
1610 | VOLTAGE FOR A PARTICULAR CODE AS CLOSELY AS
1620 | POSSIBLE.
1630 |
1640 V_ideal=V_ideal-Dif_bit*Bit
1650 Dec_rep=INT((5-V_ideal)/(5*2^(-15)))
1660 GOSUB Write_dac_voltg
1670 GOSUB Read_voltage
1680 |
1690 | *****
1700 |
1710 V_dif=0
1720 PRINT " "
1730 |
1740 | *****
1750 |
1760 | THIS "FOR" LOOP ACTUALLY CHANGES THE
1770 | VOLTAGE TO THE DESIRED VALUE AND ALLOWS
1780 | THE VOLTAGE TO STABILIZE FOR 20 COUNTS,
1790 | THEN MEASURES AND AVERAGES THE OUTPUT
1800 | CODE FOR 16 COUNTS.
1810 |
1820 FOR J=1 TO 44
1830 |
1840 | *****
1850 |
1860 IF J=1 THEN Avg=0
1870 IF J=1 THEN Sig=0
1880 |
1890 | *****
1900 |
1910 | THIS SECTION READS THE VOLTAGE OUTPUT
1920 | OF THE PROGRAMMABLE REFERENCE VOLTAGE
1930 | TEST CIRCUIT, AND CORRECTS THE VOLTAGE
1940 | BY OUT-PUTTING A VOLTAGE ON THE HP3325A
1950 | SYNTHESIZER/FUNCTION GENERATOR.
1960 |
1970 GOSUB Read_voltage
1980 |
1990 |
2000 V_dif=V_ideal-Value+V_dif
2010 V_out=-100*V_dif
2020 |
2030 |
2040 OUTPUT Func_gen;"0F",V_out,"V0"
2050 |
2060 | *****
2070 |
2080 GOSUB Read_voltage
2090 |
2100 FIXED 6
2110 IF J<=25 THEN GOTO 2750
2120 |

```

```

2130 | *****
2140 |
2150 | THIS SECTION SELECTS THE CHANNEL OF
2160 | THE 15-BIT A-D TO READ FROM, THEN
2170 | READS IN THE DATA
2180 |
2190 WRITE IO 3,5;3
2200 WRITE IO 3,5;1
2210 READ IO 3,6;Data1
2220 |
2230 | *****
2240 |
2250 Ch1(2)=Data1/2
2260 |
2270 | *****
2280 |
2290 Dif=Ch1(2)-Ch1(1)
2300 |
2310 | *****
2320 |
2330 | THIS SECTION PREVENTS THE PROGRAM FROM
2340 | PERFORMING ANY COMPUTATIONS UNTIL THE
2350 | INPUT VOLTAGE HAS HAD A CHANCE TO SETTLE,
2360 | ALLOWING 28 COUNTS BEFORE PERFORMING
2370 | COMPUTATIONS.
2380 |
2390 IF J<=20 THEN GOTO 2660
2400 |
2410 | *****
2420 |
2430 | THIS SECTION PERFORMS COMPUTATIONS, AVERAGING
2440 | THE INPUT VOLTAGES AND OUTPUT CODES.
2450 |
2460 |           V_avg = AVERAGE VOLTAGE OUTPUT BY TEST CKT, INPUT TO 15-BIT DAC
2470 |
2480 |           V_sig = STANDARD OF DEVIATION, VOLTAGE INPUT TO 15-BIT ADC
2490 |
2500 |           Avg = AVG. OUTPUT CODE FROM 15-BIT ADC
2510 |
2520 |           Sig = STD. DEV. OF OUTPUT CODE
2530 |
2540 K=J-20
2550 |
2560 V_avg=V_avg*(K-1)/K+Value/K
2570 V_sig=(V_sig^2*(K-1)/K+(Value-V_avg)^2/K)^.5
2580 Avg=Avg*(K-1)/K+Ch1(2)/K
2590 Sig=(Sig^2*(K-1)/K+(Ch1(2)-Avg)^2/K)^.5
2600 |

```

```

2610 | *****
2620 |
2630 | THIS SECTION STORES PREVIOUS OUTPUT CODES TO
2640 | DETERMINE DIFFERENCE AFTER NEXT INCREMENT OF J
2650 |
2660 Ch1<1>=Ch1<2>
2670 |
2680 | *****
2690 |
2700 IF J>26 THEN PRINT Data1/2,Avg,Sig,Value
2710 |
2720 IF Data1/2=Hum_bits THEN B_p=1
2730 |
2740 | *****
2750 |
2760 NEXT J
2770 |
2780 | *****-----*****
2790 |
2800 | THIS SECTION PRESENTS STATUS OF BIT BEING HUHTED FOR
2810 | ON THE CRT.
2820 |
2830 PRINT " "
2840 PRINT "BIN. COHV. AVG.      STD. DEV. (BITS)      V. AVG      V. STD. DEV
"
2850 PRINT "-----"      "-----"      "-----"      "-----"
"
2860 PRINT Avg,Sig,V_avg,V_sig
2870 |
2880 Dif_bit=Avg-Num_bits
2890 Db2=Dif_bit
2900 |
2910 IF ABS(Dif_bit)<=.125 THEN PRINT "*****"
2920 IF ABS(Dif_bit)<=.125 THEN PRINT " "
2930 IF ABS(Dif_bit)<=.125 THEN PRINT "IDEAL=",Num_bits,"AVG=",Avg,"STD. DEV.=",
,Sig
2940 IF (ABS(Dif_bit) = .125) AND (B_p=1) THEN PRINT "PRESENT NUMBER IS ",Num_b1
ts
2950 IF ABS(Dif_bit)<=.125 THEN PRINT " "
2960 IF ABS(Dif_bit)<=.125 THEN PRINT "*****"
2970 IF ABS(Dif_bit)<=.125 THEN GOTO 3330
2980 |
2990 | *****-----*****
3000 |
3010 IF I1=1 THEN GOTO 3200
3020 |
3030 | *****

```

```

3040 |
3050 | THIS SECTION DETECTS OSCILLATION BY SEQUENTIALLY
3060 | MEASURING DIFFERENCE OF OUTPUT CODES FROM DESIRED
3070 | OUTPUT CODE. IF OSCILLATION IS DETECTED, THE PROGRAM
3080 | ONLY INCREMENTS BY 1/2 OF DIFFERENCE. IF OSCILLATION
3090 | IS STILL DETECTED AFTER 4 MORE MEASUREMENTS, THE PROGRAM
3100 | INCREMENTS BY 1/4 OF THE DIFFERENCE.
3110 |
3120 | IF (ABS(Dif_bit/Db1)>.5) AND (Dif_bit*Db1<0) THEN Dbflag=1
3130 | IF Dbflag=1 THEN Dif_bit=Dif_bit/2
3140 | IF Dbflag=1 THEN Dn=Dn+1
3150 | IF (Dn>=4) AND (ABS(Dif_bit/Db1)>.25) AND (Dif_bit*Db1<0) THEN Dbflag=1
3160 | IF Dbflag=1 THEN Dif_bit=Dif_bit/2
3170 |
3180 | *****
3190 |
3200 | PRINT Db2,Db1,Dif_bit,"      ", "DBFLAG=",Dbflag,"DBFLAG1=",Dbflag1,"DN=",
Dn
3210 |
3220 | Db1=Db2
3230 |
3240 | *****
3250 |
3260 | NEXT I1
3270 |
3280 | *****
3290 |
3300 | THIS SECTION PRINTS WHEN UNABLE TO FIND INPUT
3310 | VOLTAGE FOR DESIRED OUTPUT CODE AFTER 30 TRIES.
3320 |
3330 | PRINTER IS 0
3340 |
3350 | IF Err=1 THEN PRINT "ERROR *** THE BIT BELOW DOES NOT CONVERGE"
3360 | PRINT Num_bits,B_p,Sig,V_avg
3370 |
3380 | PRINTER IS 16
3390 |
3400 | *****
3410 |
3420 | THIS SECTION RECORDS NUMBER OF MISSING BITS FOUND
3430 |
3440 | IF (Num_bits+2 MOD 2=0) AND (B_p=0) THEN Sum_miss=Sum_miss+1
3450 | DISP "THE TOTAL SUM OF MISSING BITS IS: ",Sum_miss
3460 |
3470 | *****
3480 |
3490 | THIS SECTION STORES THE DATA IN "SAMPLE" AFTER
3500 | EACH MEASUREMENT
3510 |
3520 | PRINT #1;Num_bits,B_p,Avg,Sig,V_avg,V_sig
3530 |

```



```

3540 | *****
3550 |
3560 B_p=0
3570 |
3580 | *****
3590 |
3600 NEXT I
3610 |
3620 | *****
3630 |
3640 PRINT " "
3650 PRINT " "
3660 PRINTER IS 0
3670 PRINT "THE TOTAL SUM OF MISSING BITS IS: ",Sum_miss
3680 PRINT " "
3690 PRINT "*****DONE"
3700 PRINTER IS 16
3710 PRINT " "
3720 PRINT " "
3730 PRINT " "
3740 PRINT " "
3750 PRINT "*****DONE"
3760 |
3770 | *****
3780 |
3790 END
3800 |
3810 | *****
3820 | *****
3830 |
3840 | SUBROUTINE TO OUTPUT CODE TO DAC TO CONTROL VOLTAGE
3850 |
3860 Write_dac_voltg:      !
3870 IF (Dec_rep)=0) AND (Dec_rep<=32767) THEN Numb=-Dec_rep-1
3880 IF (Dec_rep)=32768) AND (Dec_rep<=65535) THEN Numb=65535-Dec_rep
3890 WRITE IO 3,6;Numb
3900 RETURN
3910 |
3920 | *****
3930 | *****
3940 |
3950 | SUBROUTINE TO READ DVM VOLTAGE
3960 |
3970 Read_voltage:      !
3980 |
3990 TRIGGER Voltmeter
4000 Status:      !
4010 STATUS Voltmeter;Stat
4020 IF Stat=65 THEN Get_value
4030 IF Stat=0 THEN Status
4040 DISP "DVM ERROR"
4050 BEEP
4060 STOP
4070 Get_value:      !
4080 ENTER Voltmeter;Value
4090 RETURN
4100 |
4110 | *****
4120 | *****
4130 |

```

APPENDIX D
DATA OBTAINED FOR POWER AND DIFFERENTIAL
LINEARITY ERROR MEASUREMENTS

D.1 Power Measurement Data

The data presented is the original output of the program "POWERM", with the complete calibration section preceding the individual measurements, which are followed by the subtotals.

10 HZ CALIBRATION (SINE WAVE)

VALUE OF TEST RESISTOR (OHMS)=	10004.000000		
VOLTAGE RMS=	3.967376	VOLTAGE PK=	5.610717
V RMS SIG=	.011391	V PK SIG=	.016110
TRUE AVG POWER (MW)=	1.573378	+/-	.009035
V_POWER=	1.182387	+/-	.000381
CAL. FACTOR=	1.330679	+/-	.007654
POWER, (MW)=	1.573378	+/-	.006811

FULL CALIBRATION

COMPUTE AVG. CAL. FACTOR

1.338149
1.338352
1.341329
1.332301
1.337804
1.339990
1.346128
1.333344
1.339748
1.340346

AVG CAL.=	1.338749	CAL. ERR=	.003377
PERCENT DRIFT=	.252286	%	

FREQUENCY RESPONSE

FREQ. (HZ)	PWR. (MW) EXP.	PWR. (MW) MEAS.	RATIO (dB) ERROR (%)
10.000000	1.576104	1.574234	-.005157 .118669
30.000000	1.576603	1.577817	.003344 .077033
100.000000	1.578697	1.583529	.013273 .306095
300.000000	1.580060	1.586404	-.037699 .864295
1000.000000	1.582420	1.584907	.006821 .157175
3000.000000	1.583970	1.581326	-.007254 .166900
10000.000000	1.585260	1.583280	-.005427 .124873
30000.000000	1.584712	1.588410	.010123 .233352
70000.000000	1.584018	1.588504	.012281 .283189
100000.000000	1.584037	1.612005	.076012 1.765649
200000.000000	1.585607	1.753008	.435884 10.557540
300000.000000	1.583034	2.077555	1.180623 31.238817
330000.000000	1.582888	1.051022	-1.778384 33.600987
400000.000000	1.583018	.000092	-42.339377 99.994165
1000000.000000	1.576711	.000012	-51.010177 99.999208
AVG. % ERROR, 10HZ-100KHZ :		.259065	

1 KHZ SINE WAVE RESPONSE

PWR. (MW) EXP.	PWR. (MW) MEAS.	ERROR (%)
1.585517	1.569428	1.014757

1 KHZ SQUARE WAVE RESPONSE

PWR. (MW) EXP.	PWR. (MW) MEAS.	ERROR (%)
3.044286	3.194921	4.948123

1 KHZ TRIANGULAR WAVE RESPONSE

PWR. (MW) EXP.	PWR. (MW) MEAS.	ERROR (%)
1.102583	1.055916	4.232443

GROUND (NO POWER) RESPONSE

PWR. (MW) EXP.	PWR. (MW) MEAS.	ERROR (%)
.000392	.001521	288.626403

```

MEASUREMENT #      1.000000
POINT +A Rp1 (10K PULL-UP RESISTOR) CURRENT MEAS: +A VOLTAGE MEAS: +A
P, avg (mW) =      .065041          +/-          .000297
                  (+/-          .456096          %)

*****
MEASUREMENT #      2.000000
POINT +A Rp1 (10K PULL-UP RESISTOR) CURRENT MEAS: +A VOLTAGE MEAS: +7.5VDC
P, avg (mW) =      .080879          +/-          .003362
                  (+/-          4.156861          %)

*****
MEASUREMENT #      3.000000
POINT +B Rp2 (10K PULL-UP RESISTOR) CURRENT MEAS: +B VOLTAGE MEAS: +B
P, avg (mW) =      .013361          +/-          .000196
                  (+/-          1.469745          %)

*****
MEASUREMENT #      4.000000
P, avg (mW) =      .015938          +/-          .003251
                  (+/-          20.397254          %)

*****
MEASUREMENT #      5.000000
POINT +C CMP1 (PM339AY QUAD COMP) CURRENT MEAS: +C VOLTAGE MEAS: +C
P, avg (mW) =      .324735          +/-          .001005
                  (+/-          .309522          %)

*****
MEASUREMENT #      6.000000
POINT C CMP1 (PM339AY QUAD COMP) CURRENT MEAS: +C VOLTAGE MEAS: +7.5VDC
P, avg (mW) =      .332019          +/-          .003391
                  (+/-          1.021249          %)

*****

```

```

MEASUREMENT #          7.000000
POINT +D A2 (OP-37EZ DAC FOLLOWER) CURRENT MEAS: +D VOLTAGE MEAS: +D
P, avg (mW) =          1.239923          +/-          .003504
                    (+/-          .282633          %)
*****
MEASUREMENT #          8.000000
POINT +D A2 (OP-37EZ DAC FOLLOWER) CURRENT MEAS: +D VOLTAGE MEAS: +7.5VDC
P, avg (mW) =          1.381594          +/-          .004434
                    (+/-          .348656          %)
*****
MEASUREMENT #          9.000000
POINT +E Rp3 (10K PULL-UP RESISTOR) CURRENT MEAS: +E VOLTAGE MEAS: +E
P, avg (mW) =           .009760          +/-          .000203
                    (+/-          2.083430          %)
*****
MEASUREMENT #         10.000000
POINT +E Rp3 (10K PULL-UP RESISTOR) CURRENT MEAS: +E VOLTAGE MEAS:
P, avg (mW) =           .010845          +/-          .000162
                    (+/-          1.489796          %)
*****
MEASUREMENT #         11.000000
POINT +F A1 (OP-37EZ DAC FOLLOWER) CURRENT MEAS: +F VOLTAGE MEAS: +F
P, avg (mW) =           .914823          +/-          .002588
                    (+/-          .282846          %)
*****
MEASUREMENT #         12.000000
POINT +F A1 (OP-37EZ DAC FOLLOWER) CURRENT MEAS: +F VOLTAGE MEAS: +7.5VDC
P, avg (mW) =           .942948          +/-          .004963
                    (+/-          .526337          %)
*****
MEASUREMENT #

```

```

MEASUREMENT #          13.000000
POINT +G REF1 (REF-02 5V REFERENCE) CURRENT MEAS: +G VOLTAGE MEAS: +G
P,avg (mW) =           .791190           +/-           .002234
                    (<+/-           .202374           %)
*****
MEASUREMENT #          14.000000
POINT +G REF1 (REF-02 5V REFERENCE) CURRENT MEAS: +G VOLTAGE MEAS: +7.5VDC
P,avg (mW) =           .029752           +/-           .002596
                    (<+/-           .312870           %)
*****
MEASUREMENT #          15.000000
POINT -A A1 (OP-37EZ DAC FOLLOWER) CURRENT MEAS: -A VOLTAGE MEAS: -A
P,avg (mW) =           1.290953           +/-           .003650
                    (<+/-           .201003           %)
*****
MEASUREMENT #          16.000000
POINT -A A1 (OP-37EZ DAC FOLLOWER) CURRENT MEAS: -A VOLTAGE MEAS: -7.5VDC
P,avg (mW) =           1.349195           +/-           .004310
                    (<+/-           .320063           %)
*****
MEASUREMENT #          17.000000
POINT -B CMP1 (PM339AY QUAD COMP) CURRENT MEAS: -B VOLTAGE MEAS: -B
P,avg (mW) =           .339691           +/-           .003728
                    (<+/-           1.097331           %)
*****
MEASUREMENT #          18.000000
POINT -B CMP1 (PM339AY QUAD COMP) CURRENT MEAS: -B VOLTAGE MEAS: -7.5VDC
P,avg (mW) =           .333506           +/-           .002952
                    (<+/-           .805246           %)
*****

```



```

MEASUREMENT #      19.000000
MEAS #18 REPEAT
P,avg (mW) =      .334011      +/-      .004938
                  (+/-      1.478443      %)
*****
MEASUREMENT #      20.000000
MEAS #17 REPEAT
P,avg (mW) =      .366284      +/-      .004715
                  (+/-      1.287137      %)
-----
MEASUREMENT #      21.000000
MEAS #18 REPEAT
P,avg (mW) =      .339893      +/-      .004024
                  (+/-      1.184001      %)
*****
MEASUREMENT #      22.000000
MEAS #17 REPEAT
P,avg (mW) =      .339529      +/-      .003520
                  (+/-      1.036797      %)
-----
MEASUREMENT #      23.000000
POINT -C A2 (OP-37EZ DAC FOLLOWER) CURRENT MEAS: -C VOLTAGE MEAS: -C
P,avg (mW) =      .928088      +/-      .002573
                  (+/-      .279638      %)
*****
MEASUREMENT #      24.000000
POINT -C A2 (OP-37EZ DAC FOLLOWER) CURRENT MEAS: -C VOLTAGE MEAS: -7.5VDC
P,avg (mW) =      .944745      +/-      .004928
                  (+/-      .511018      %)
*****

```

```

MEASUREMENT #      25.000000
POINT +H SW1 (DG308CJ AN. SW.) CURRENT MEAS: +H VOLTAGE MEAS: +H
P, avg (mW) =      .017330      +/-      .005745
                  (<+/-      33.148690      %)

*****
MEASUREMENT #      26.000000
POINT +H SW1 (DG 308CJ AN. SW.) CURRENT MEAS: +H VOLTAGE MEAS: +7.5VDC
P, avg (mW) =      .057742      +/-      .003571
                  (<+/-      6.184940      %)

*****
MEASUREMENT #      27.000000
POINT +I SW2 (DG308CJ) AN. SW.) CURRENT MEAS: +I VOLTAGE MEAS: +I
P, avg (mW) =      .004174      +/-      .003032
                  (<+/-      72.648921      %)

*****
MEASUREMENT #      28.000000
POINT +I SW2 (DG308CJ AN. SW.) CURRENT MEAS: +I VOLTAGE MEAS: +7.5VDC
P, avg (mW) =      .004915      +/-      .002757
                  (<+/-      56.009359      %)

*****
MEASUREMENT #      29.000000
POINT +J SW3 (DG308CJ AN. SW.) CURRENT MEAS: +J VOLTAGE MEAS: +J
P, avg (mW) =      .011701      +/-      .006289
                  (<+/-      53.751400      %)

*****
MEASUREMENT #      30.000000
POINT +J SW3 (DG308CJ AN. SW.) CURRENT MEAS: +J VOLTAGE MEAS: +7.5VDC
P, avg (mW) =      .015911      +/-      .004754
                  (<+/-      29.081601      %)

*****

```

```

MEASUREMENT #      31.000000
MEASUREMENT #25 REPEAT (POINT +H, SW1)
P, avg (mW) =      .019121      +/-      .005463
                (<+/-      28.570620      %)
*****
MEASUREMENT #      32.000000
MEASUREMENT #25 REPEAT (POINT +H, SW1)
P, avg (mW) =      .000447      +/-      .004029
                (<+/-      901.406205      %)
*****
MEASUREMENT #      33.000000
MEASUREMENT #26 REPEAT
P, avg (mW) =      .004080      +/-      .006748
                (<+/-      138.281573      %)
*****
MEASUREMENT #      34.000000
MEASUREMENT #25 REPEAT
P, avg (mW) =      .045796      +/-      .002914
                (<+/-      6.361989      %)
*****
MEASUREMENT #      35.000000
MEASUREMENT #26 REPEAT
P, avg (mW) =      .050013      +/-      .003124
                (<+/-      6.247309      %)
*****
MEASUREMENT #      36.000000
POINT -D SW1 (DG308CJ AN. SW.) CURRENT MEAS: -D VOLTAGE MEAS: -D
P, avg (mW) =      .060851      +/-      .010542
                (<+/-      17.324209      %)
*****

```

```

MEASUREMENT #          37.000000
POINT -D SW1 (DG308CJ AN. SW.) CURRENT MEAS: -D VOLTAGE MEAS: -7.5VDC
P, avg (mW) =          .042555          +/-          .006859
                   (<+/-          16.117899          %)
*****
MEASUREMENT #          38.000000
MEASUREMENT # 36 REPEAT
P, avg (mW) =          .019195          +/-          .004705
                   (<+/-          24.508835          %)
*****
MEASUREMENT #          39.000000
POINT -E SW2 (DG308CJ AN. SW.) CURRENT MEAS: -E VOLTAGE MEAS: -E
P, avg (mW) =          .005423          +/-          .002980
                   (<+/-          54.954926          %)
*****
MEASUREMENT #          40.000000
POINT -E SW2 (DG308CJ AN. SW.) CURRENT MEAS: -E VOLTAGE MEAS: -7.5VDC
P, avg (mW) =          .000094          +/-          .000037
                   (<+/-          38.973823          %)
*****
MEASUREMENT #          41.000000
MEASUREMENT #40 REPEAT
P, avg (mW) =          .000287          +/-          .000030
                   (<+/-          10.267543          %)
*****
MEASUREMENT #          42.000000
REPEAT MEASUREMENT #39
P, avg (mW) =          .000119          +/-          .000027
                   (<+/-          22.622860          %)
*****

```

```

MEASUREMENT #          43.000000
POINT -F SW3 (DG300CJ AN. SW.) CURRENT MEAS: -F VOLTAGE MEAS: -F
P, avg (mW) =          .000206          +/-          .000020
                    (<+/-          9.647469          %)
*****
MEASUREMENT #          44.000000
POINT -F SW3 (DG300CJ AN. SW.) CURRENT MEAS: -F VOLTAGE MEAS: -7.5VDC
P, avg (mW) =          .000150          +/-          .000027
                    (<+/-          17.231894          %)
*****
MEASUREMENT #          45.000000
REPEAT MEASUREMENT #43
P, avg (mW) =          .000159          +/-          .000021
                    (<+/-          13.331752          %)
*****
MEASUREMENT #          46.000000
REPEAT MEASUREMENT #44
P, avg (mW) =          .000070          +/-          .000017
                    (<+/-          21.421436          %)
*****
MEASUREMENT #          47.000000
REPEAT MEASUREMENT #43
P, avg (mW) =          .000250          +/-          .000023
                    (<+/-          9.025354          %)
*****
MEASUREMENT #          48.000000
REPEAT MEASUREMENT #44
P, avg (mW) =          .000090          +/-          .000024
                    (<+/-          27.115933          %)
*****

```

```

MEASUREMENT #      49.000000
REPEAT MEASUREMENT #44
P,avg (mW) =      .000097      +/-      .000032
                (<+/-      33.031553      %)

*****
MEASUREMENT #      50.000000
REPEAT MEASUREMENT #43
P,avg (mW) =      .000287      +/-      .000021
                (<+/-      7.424135      %)

*****
MEASUREMENT #      51.000000
REPEAT MEASUREMENT #44
P,avg (mW) =      .000081      +/-      .000029
                (<+/-      36.335907      %)

*****
MEASUREMENT #      52.000000
REPEAT MEASUREMENT #43
P,avg (mW) =      .000091      +/-      .000019
                (<+/-      19.387352      %)

*****
MEASUREMENT #      53.000000
REPEAT MEASUREMENT #44
P,avg (mW) =      .000199      +/-      .000031
                (<+/-      15.828289      %)

*****
MEASUREMENT #      54.000000
POINT +K (PULL-DOWN RESISTOR, SW4) CURRENT MEAS: +K VOLTAGE MEAS: +K
P,avg (mW) =      .006433      +/-      .003649
                (<+/-      56.723637      %)

*****

```

```

MEASUREMENT #      55.000000
POINT +L (PULL-UP RESISTOR, SW4) CURRENT MEAS: +L VOLTAGE MEAS: +5.0VDC
P,avg (mW) =      .141895      +/-      .002850
                (<+/-      2.015527      %)

*****
MEASUREMENT #      56.000000
POINT +M (PULL-UP RESISTOR, SW4) CURRENT MEAS: +M VOLTAGE MEAS: +5.0VDC
P,avg (mW) =      .118476      +/-      .002663
                (<+/-      2.247681      %)

*****
MEASUREMENT #      57.000000
POINT +0 SW4 (POS. SUPPLY) CURRENT MEAS: +0 VOLTAGE MEAS: +0 (+7.5VDC)
P,avg (mW) =      .000102      +/-      .000019
                (<+/-      18.456304      %)

*****
MEASUREMENT #      58.000000
POINT -G SW4 (NEG. SUPPLY) CURRENT MEAS: -G VOLTAGE MEAS: -G (-7.5VDC)
P,avg (mW) =      .000349      +/-      .000023
                (<+/-      6.516882      %)

*****
MEASUREMENT #      59.000000
POINT +P LS1 (MC14504B LEVEL SHIFTER) CURRENT MEAS: +P VOLTAGE MEAS: +P (+5VDC)
P,avg (mW) =      .024439      +/-      .001521
                (<+/-      6.223067      %)

*****
MEASUREMENT #      60.000000
POINT +Q LS1 (MC14504B LEVEL SHIFTER) CURRENT MEAS: +Q VOLTAGE MEAS: +Q (7.5VDC)
P,avg (mW) =      .000068      +/-      .000021
                (<+/-      31.460310      %)

*****
MEASUREMENT #      61.000000

```

MEASUREMENT # 61.000000
POINT +R DAC1 (DAC HA-14B 14-BIT DAC) CURRENT MEAS: +P VOLTAGE MEAS: +P (7.5VDC)
P, avg (mW) = .000120 +/- .000023
<+/- 19.078594 %>

BEGIN SUBTOTALS

SUBTOTAL *****

REF1, TOTAL POWER CONSUMPTION (EXPECTED VALUE: 0.720 mW, typ; 0.864 mW, max)

		P, avg	+/-	Std. Dev.
(+) MEASUREMENT	13.000000		.791190	.002234
SUBTOTAL			.791190	.002234
Pavg, (mW) =	.791190	+/-		.002234
	(+/-	.282359		%

SUBTOTAL *****

DAC1, TOTAL POWER CONSUMPTION (EXPECTED VALUE: 0.005 mW, typ; 0.005 mW, max)

		P, avg	+/-	Std. Dev.
(+) MEASUREMENT	61.000000		.000120	.000023
SUBTOTAL			.000120	.000023
Pavg, (mW) =	.000120	+/-		.000023
	(+/-	19.078594		%

SUBTOTAL *****

A1, TOTAL POWER CONSUMPTION (EXPECTED VALUE: 2.160 mW, typ; 2.304 mW, max)

		P, avg	+/-	Std. Dev.
(+) MEASUREMENT	11.000000		.914823	.002538
(+) MEASUREMENT	15.000000		1.296953	.003658
SUBTOTAL			2.213776	.004474
Pavg, (mW) =	2.213776	+/-		.004474
	(+/-	.202116		%

SUBTOTAL *****

A2, TOTAL POWER CONSUMPTION (EXPECTED VALUE: 2.160 mW, typ; 2.304 mW, max)

		P, avg	+/-	Std. Dev.
(+) MEASUREMENT	7.000000		1.239923	.003504
(+) MEASUREMENT	23.000000		.920088	.002573
SUBTOTAL			2.160011	.004347
Pavg, (mW) =	2.160011	+/-		.004347
	(+/-	.201259		%

SUBTOTAL *****

CMp1, TOTAL POWER CONSUMPTION (EXPECTED VALUE: 0.575 mW,typ; 1.440 mW,max)

		P, avg	+/-	Std. Dev.
(+) MEASUREMENT	5.000000	.324735		.001005
(+) MEASUREMENT	22.000000	.339529		.003520
SUBTOTAL		.664264		.003661
Pavg, (mW) =	.664264		+/-	.003661
	(+/-	.551085		%

SUBTOTAL *****

Rp1, TOTAL POWER CONSUMPTION (EXPECTED VALUE: 1.080 mW,typ; 1.080 mW,max)

		P, avg	+/-	Std. Dev.
(+) MEASUREMENT	1.000000	.065041		.000297
SUBTOTAL		.065041		.000297
Pavg, (mW) =	.065041		+/-	.000297
	(+/-	.456635		%

SUBTOTAL *****

Rp2, TOTAL POWER CONSUMPTION (EXPECTED VALUE: 1.080 mW,typ; 1.080 mW,max)

		P, avg	+/-	Std. Dev.
(+) MEASUREMENT	3.000000	.013361		.000196
SUBTOTAL		.013361		.000196
Pavg, (mW) =	.013361		+/-	.000196
	(+/-	1.466956		%

SUBTOTAL *****

Rp3, TOTAL POWER CONSUMPTION (EXPECTED VALUE: 1.080 mW,typ; 1.080 mW,max)

		P, avg	+/-	Std. Dev.
(+) MEASUREMENT	9.000000	.009760		.000203
SUBTOTAL		.009760		.000203
Pavg, (mW) =	.009760		+/-	.000203
	(+/-	2.079918		%

SUBTOTAL *****

LS1, TOTAL POWER CONSUMPTION (EXPECTED VALUE: ~0 mW,typ; ~0 mW,max)

		P, avg	+/-	Std. Dev.
(+) MEASUREMENT	59.000000			
(+) MEASUREMENT	50.000000	.024433		.001521
		.000068		.000021
SUBTOTAL		.024507		.001521
Pavg, (mW) =	.024507		+/-	.001521
	(+/-	6.206488		%

SUBTOTAL *****

SN4, TOTAL POWER CONSUMPTION (EXPECTED VALUE: 0.356 mW,typ; 1.856 mW,max)

		P, avg	+/-	Std. Dev.
(+) MEASUREMENT	54.000000			
(+) MEASUREMENT	55.000000	.006433		.003649
(+) MEASUREMENT	55.000000	.141895		.002860
(+) MEASUREMENT	56.000000	.118476		.002663
(+) MEASUREMENT	57.000000	.000102		.000019
(+) MEASUREMENT	58.000000	.000349		.000023
SUBTOTAL		.267255		.005347
Pavg, (mW) =	.267255		+/-	.005347
	(+/-	2.000671		%

SUBTOTAL *****

COMBINED POWER CONSUMPTION, ISOLATION NETWORK & SW1, SW2, SW3
(EXPECTED VALUE: 0.265 mW, typ; 4.839 mW, max).

	P, avg	+/-	Std. Dev.
(+) MEASUREMENT	14.000000	.829752	.002596
(-) MEASUREMENT	13.000000	-.791190	.002234
(+) MEASUREMENT	12.000000	.942948	.004963
(-) MEASUREMENT	11.000000	-.914823	.002588
(+) MEASUREMENT	16.000000	1.349195	.004318
(-) MEASUREMENT	15.000000	-1.298953	.003650
(+) MEASUREMENT	8.000000	1.301594	.004434
(-) MEASUREMENT	7.000000	-1.239923	.003504
(+) MEASUREMENT	24.000000	.944745	.004828
(-) MEASUREMENT	23.000000	-.920088	.002573
(+) MEASUREMENT	6.000000	.332019	.003391
(-) MEASUREMENT	5.000000	-.324735	.001005
(+) MEASUREMENT	21.000000	.339893	.004024
(-) MEASUREMENT	22.000000	-.339529	.003520
(+) MEASUREMENT	2.000000	.080879	.003362
(-) MEASUREMENT	1.000000	-.065041	.000297
(+) MEASUREMENT	4.000000	.015938	.003251
(-) MEASUREMENT	3.000000	-.013361	.000196
(+) MEASUREMENT	10.000000	.010845	.000162
(-) MEASUREMENT	9.000000	-.009760	.000203
(+) MEASUREMENT	35.000000	.050013	.003124
(+) MEASUREMENT	28.000000	.004915	.002757
(+) MEASUREMENT	30.000000	.015911	.004754
(+) MEASUREMENT	37.000000	.042555	.006859
(+) MEASUREMENT	41.000000	.000287	.000030
(+) MEASUREMENT	53.000000	.000199	.000031
SUBTOTAL		.344285	.016943
Pavg, (mW) =	.344285	+/-	.016943
	(+/-	4.921183	%

SUBTOTAL *****+*****

ALL COMPONENTS, TOTAL POWER CONSUMPTION (EXP. VAL.: 9.482 mW, typ; 16.852 mW, max)

	P, avg	+/-	Std. Dev.
(>) MEASUREMENT	14.000000	.029752	.002596
(>) MEASUREMENT	12.000000	.942948	.004963
(>) MEASUREMENT	16.000000	1.349195	.004318
(>) MEASUREMENT	8.000000	1.301594	.004434
(>) MEASUREMENT	24.000000	.944745	.004823
(>) MEASUREMENT	6.000000	.332019	.003391
(>) MEASUREMENT	21.000000	.339093	.004024
(>) MEASUREMENT	2.000000	.080879	.003362
(>) MEASUREMENT	4.000000	.015938	.003251
(>) MEASUREMENT	10.000000	.010845	.000162
(>) MEASUREMENT	35.000000	.050013	.003124
(>) MEASUREMENT	28.000000	.064915	.002757
(>) MEASUREMENT	30.000000	.015911	.004754
(>) MEASUREMENT	37.000000	.042555	.006359
(>) MEASUREMENT	41.000000	.000207	.000030
(>) MEASUREMENT	53.000000	.000199	.000031
(>) MEASUREMENT	54.000000	.006433	.003649
(>) MEASUREMENT	55.000000	.141095	.002060
(>) MEASUREMENT	56.000000	.118476	.002663
(>) MEASUREMENT	57.000000	.000102	.000019
(>) MEASUREMENT	58.000000	.000349	.000023
(>) MEASUREMENT	59.000000	.024439	.001521
(>) MEASUREMENT	60.000000	.000068	.000021
(>) MEASUREMENT	61.000000	.000120	.000023
SUBTOTAL		6.553570	.016140
Pavg, (mW) =	6.553570	+/-	.016140
	(<+/-	.246272	%

D.2 Differential Linearity Error Data

The following is a listing made of all 497 data points used to estimate the differential linearity error.

CORRECTED VERSION FOR NEGATIVE NUMBERS

BIT NO.	PRESENCE	STD. DEV.	VOLTAGE
16383.000000	1.000000	0.000000	4.999912
16382.000000	1.000000	.385406	4.999408
16381.000000	1.000000	.575762	4.999095
16380.000000	1.000000	.513789	4.998789
16379.000000	1.000000	.484862	4.998375
16378.000000	1.000000	.661802	4.998073
16377.000000	1.000000	.465772	4.997821
16376.000000	1.000000	.445767	4.997465
16375.000000	1.000000	.296223	4.997166
16374.000000	1.000000	.377453	4.996835
16373.000000	1.000000	.640676	4.996532
16372.000000	1.000000	.697533	4.996405
16371.000000	1.000000	.726776	4.995884
16370.000000	1.000000	.867131	4.995640
16369.000000	1.000000	.625170	4.995398
16368.000000	1.000000	.558053	4.995087
16367.000000	1.000000	.366127	4.994783
16366.000000	1.000000	.302686	4.994389
16365.000000	1.000000	.682585	4.994099
16364.000000	1.000000	.493362	4.993795
16363.000000	1.000000	.501634	4.993562
16362.000000	1.000000	.831097	4.993331
16361.000000	1.000000	.808119	4.993025
16360.000000	1.000000	.914836	4.992717
16359.000000	1.000000	.365199	4.992298
16358.000000	1.000000	.302686	4.991995
16357.000000	1.000000	.526945	4.991694
16356.000000	1.000000	.641416	4.991501
16355.000000	1.000000	.847223	4.991023
16354.000000	1.000000	.847445	4.990808
16353.000000	1.000000	.547412	4.990502
16352.000000	1.000000	.635684	4.990196
16351.000000	1.000000	.541818	4.989908
16350.000000	1.000000	.434847	4.989492
16349.000000	1.000000	.775679	4.989186
16348.000000	1.000000	.289808	4.988884
16347.000000	1.000000	.574272	4.988516
16346.000000	1.000000	.788944	4.988339
16345.000000	1.000000	.616024	4.988028
16344.000000	1.000000	.594482	4.987656
16343.000000	1.000000	0.000000	4.987351
16342.000000	1.000000	.295346	4.987021
16341.000000	1.000000	.864620	4.986854
16340.000000	1.000000	.940789	4.986656
16339.000000	1.000000	.773021	4.986091
16338.000000	1.000000	.962566	4.985971

16337.000000	1.000000	.726613	4.985649
16336.000000	1.000000	.836177	4.985477
16335.000000	1.000000	.377749	4.985093
16334.000000	1.000000	.499601	4.984984
16333.000000	1.000000	.684738	4.984962
16332.000000	1.000000	.615609	4.983952
16331.000000	1.000000	.620027	4.983717
16330.000000	1.000000	.753573	4.983407
16329.000000	1.000000	.759086	4.983282
16328.000000	1.000000	.787842	4.982965
16327.000000	1.000000	.429626	4.982463
16326.000000	1.000000	.478286	4.982076
16325.000000	1.000000	.993963	4.981944
16324.000000	1.000000	.839952	4.981834
16323.000000	1.000000	.839096	4.981274
16322.000000	1.000000	.901985	4.981038
16321.000000	1.000000	.706782	4.980772
16320.000000	1.000000	.697200	4.980466
16319.000000	1.000000	.288238	4.980161
16318.000000	1.000000	.436451	4.979856
16317.000000	1.000000	.665270	4.979545
16316.000000	1.000000	.686544	4.979034
16315.000000	1.000000	.608574	4.978860
16314.000000	1.000000	.787638	4.978553
16313.000000	1.000000	.418461	4.978245
16312.000000	1.000000	.440144	4.977941
16311.000000	1.000000	.221837	4.977637
16310.000000	1.000000	.590012	4.977270
16309.000000	1.000000	.755200	4.977051
16308.000000	1.000000	.533215	4.976838
16307.000000	1.000000	.218100	4.976539
16306.000000	1.000000	.798479	4.976138
16305.000000	1.000000	.694928	4.975924
16304.000000	1.000000	.542276	4.975578
16303.000000	1.000000	.218100	4.975223
16302.000000	1.000000	.524566	4.974728
16301.000000	1.000000	.736421	4.974619
16300.000000	1.000000	.417553	4.974318
16299.000000	1.000000	.322750	4.974005
16298.000000	1.000000	.710974	4.973736
16297.000000	1.000000	.834329	4.973437
16296.000000	1.000000	.799507	4.973304
16295.000000	1.000000	.439440	4.972909
16294.000000	1.000000	.536698	4.972354
16293.000000	1.000000	1.118230	4.972138
16292.000000	1.000000	.859877	4.972041
16291.000000	1.000000	.555661	4.971562
16290.000000	1.000000	.798103	4.971201
16289.000000	1.000000	1.806935	4.971051
16288.000000	1.000000	.943065	4.970906
16287.000000	1.000000	.800000	4.970437
16286.000000	1.000000	.429784	4.969951
16285.000000	1.000000	.754812	4.969715

8242.000000	1.000000	.728454	2.518228
8241.000000	1.000000	.695015	2.517923
8240.000000	1.000000	.375100	2.517621
8239.000000	1.000000	.683712	2.517351
8238.000000	1.000000	.732577	2.517266
8237.000000	1.000000	.756968	2.516728
8236.000000	1.000000	.435710	2.516585
8235.000000	1.000000	.437501	2.516061
8234.000000	1.000000	.764519	2.515808
8233.000000	1.000000	.553766	2.515530
8232.000000	1.000000	.491898	2.515220
8231.000000	1.000000	.300752	2.514916
8230.000000	1.000000	.831269	2.514719
8229.000000	1.000000	.635168	2.514241
8228.000000	1.000000	0.000000	2.513987
8227.000000	1.000000	.513148	2.513684
8226.000000	1.000000	.709171	2.513308
8225.000000	1.000000	.664103	2.512932
8224.000000	1.000000	0.000000	2.512776
8223.000000	1.000000	.498778	2.512471
8222.000000	1.000000	.692880	2.512182
8221.000000	1.000000	.684883	2.511899
8220.000000	1.000000	.616379	2.511701
8219.000000	1.000000	.702240	2.511456
8218.000000	1.000000	.890021	2.511154
8217.000000	1.000000	.489285	2.510722
8216.000000	1.000000	.743416	2.510476
8215.000000	1.000000	.488174	2.509922
8214.000000	1.000000	.312791	2.509670
8213.000000	1.000000	.355889	2.509371
8212.000000	1.000000	.425543	2.509068
8211.000000	1.000000	.375955	2.508888
8210.000000	1.000000	.977410	2.508506
8209.000000	1.000000	.221405	2.508205
8208.000000	1.000000	.293158	2.507899
8207.000000	1.000000	.215788	2.507592
8206.000000	1.000000	.643951	2.507139
8205.000000	1.000000	.606430	2.506891
8204.000000	1.000000	.296487	2.506588
8203.000000	1.000000	.747473	2.506285
8202.000000	1.000000	.291473	2.505951
8201.000000	1.000000	.180710	2.505790
8200.000000	1.000000	.576646	2.505484
8199.000000	1.000000	.309060	2.505176
8198.000000	1.000000	.776088	2.504805
8197.000000	1.000000	.746725	2.504384
8196.000000	1.000000	.539373	2.504081
8195.000000	1.000000	.599369	2.503773
8194.000000	1.000000	1.416618	2.503556
8193.000000	1.000000	1.250326	2.503336
8192.000000	1.000000	1.013390	2.503052
8191.000000	1.000000	.213720	2.502819
8190.000000	1.000000	.615574	2.502514
8189.000000	1.000000	.869873	2.502386
8188.000000	1.000000	.347356	2.502105
8187.000000	1.000000	.596953	2.501828
8186.000000	1.000000	.908775	2.501404

8185.000000	1.000000	.218100	2.501100
8184.000000	1.000000	0.000000	2.500705
8183.000000	1.000000	.484162	2.500396
8182.000000	1.000000	.218976	2.499971
8181.000000	1.000000	.981089	2.499886
8180.000000	1.000000	.659362	2.499688
8179.000000	1.000000	0.000000	2.499331
8178.000000	1.000000	.996636	2.499027
8177.000000	1.000000	.283286	2.498735
8176.000000	1.000000	.180710	2.498429
8175.000000	1.000000	.220360	2.497966
8174.000000	1.000000	0.000000	2.497484
8173.000000	1.000000	.585577	2.497387
8172.000000	1.000000	.221837	2.497081
8171.000000	1.000000	0.000000	2.496724
8170.000000	1.000000	.973697	2.496575
8169.000000	1.000000	.295778	2.496267
8168.000000	1.000000	.520643	2.495952
8167.000000	1.000000	.000000	2.495646
8166.000000	1.000000	.298004	2.495039
8165.000000	1.000000	.981406	2.495015
8164.000000	1.000000	.417872	2.494778
8163.000000	1.000000	0.000000	2.494475
8162.000000	1.000000	.724987	2.494012
8161.000000	1.000000	.209611	2.493831
8160.000000	1.000000	.206047	2.493522
8159.000000	1.000000	.212224	2.493096
8158.000000	1.000000	.214218	2.492685
8157.000000	1.000000	.860037	2.492614
8156.000000	1.000000	.606884	2.492469
8155.000000	1.000000	0.000000	2.492372
8154.000000	1.000000	.871149	2.492191
8153.000000	1.000000	.697338	2.491908
8152.000000	1.000000	.000000	2.491601
8151.000000	1.000000	.277785	2.491134
8150.000000	1.000000	0.000000	2.490826
8149.000000	1.000000	.883431	2.490575
8148.000000	1.000000	.427451	2.490429
8147.000000	1.000000	.180710	2.490121
8146.000000	1.000000	.820377	2.489748
8145.000000	1.000000	.387052	2.489441
8144.000000	1.000000	.316863	2.489191
8143.000000	1.000000	.200928	2.488888

CORRECTED VERSION FOR NEGATIVE NUMBERS

BIT NO.	PRESENCE	STD. DEV.	VOLTAGE
50.000000	1.000000	.139534	.021954
49.000000	1.000000	.190545	.021644
48.000000	1.000000	.000000	.0213
47.000000	1.000000	.288515	.02102
46.000000	1.000000	.131255	.020652
45.000000	1.000000	.329237	.020340
44.000000	1.000000	.139674	.020024
43.000000	1.000000	.000000	.019709
42.000000	1.000000	.114007	.019490
41.000000	1.000000	.365193	.019114
40.000000	1.000000	.350725	.018797
39.000000	1.000000	.140903	.018488
38.000000	1.000000	.141198	.018178
37.000000	1.000000	.273718	.017906
36.000000	1.000000	.274177	.017590
35.000000	1.000000	.191283	.017274
34.000000	1.000000	.298761	.016962
33.000000	1.000000	.194930	.016646
32.000000	1.000000	.237432	.016335
31.000000	1.000000	.195017	.016022
30.000000	1.000000	.262602	.015711
29.000000	1.000000	.345455	.015448
28.000000	1.000000	.289785	.015137
27.000000	1.000000	.137699	.014821
26.000000	1.000000	.197038	.014570
25.000000	1.000000	.336677	.014200
24.000000	1.000000	.300253	.013888
23.000000	1.000000	.114007	.013573
22.000000	1.000000	.141162	.013262
21.000000	1.000000	.224919	.013056
20.000000	1.000000	.439980	.012642
19.000000	1.000000	.283592	.012330
18.000000	1.000000	.329338	.012073
17.000000	1.000000	.380716	.011756
16.000000	1.000000	.294728	.011374
15.000000	1.000000	.114007	.011059
14.000000	1.000000	0.000000	.010748
13.000000	1.000000	.269249	.010562
12.000000	1.000000	0.000000	.010104
11.000000	1.000000	.264256	.009890
10.000000	1.000000	.261964	.009716
9.000000	1.000000	.441181	.009317
8.000000	1.000000	.288541	.008911
7.000000	1.000000	.000000	.008601
6.000000	1.000000	.000000	.008290
5.000000	1.000000	.223246	.008119
4.000000	1.000000	.407923	.007730
3.000000	1.000000	.508333	.007343
2.000000	1.000000	.263509	.007143
1.000000	1.000000	0.000000	.006723
0.000000	1.000000	0.000000	.006411
ERROR ***	THE BIT BELOW DOES NOT CONVERGE		
-1.000000	1.000000	7.347357	.006366
ERROR ***	THE BIT BELOW DOES NOT CONVERGE		
-2.000000	1.000000	0.000000	.006495

-2.000000	1.000000	0.000000	.006495
-3.000000	1.000000	.000000	.004782
-4.000000	1.000000	.141084	.004401
-5.000000	1.000000	0.000000	.004084
-6.000000	1.000000	.268495	.003852
-7.000000	1.000000	.000000	.003541
-8.000000	1.000000	.196619	.003232
-9.000000	1.000000	0.000000	.002917
-10.000000	1.000000	.129121	.002774
-11.000000	1.000000	0.000000	.002458
-12.000000	1.000000	.298448	.002063
-13.000000	1.000000	0.000000	.001751
-14.000000	1.000000	.136343	.001562
-15.000000	1.000000	.000000	.001245
-16.000000	1.000000	.000000	.000883
-17.000000	1.000000	0.000000	.000461
-18.000000	1.000000	.140617	.000145
-19.000000	1.000000	0.000000	-.000105
-20.000000	1.000000	.000000	-.000267
-21.000000	1.000000	.000000	-.000582
-22.000000	1.000000	.510905	-.000893
-23.000000	1.000000	0.000000	-.001207
-24.000000	1.000000	.194488	-.001517
-25.000000	1.000000	.195016	-.001834
-26.000000	1.000000	.302562	-.002135
-27.000000	1.000000	.000000	-.002452
-28.000000	1.000000	.139674	-.002763
-29.000000	1.000000	0.000000	-.003078
-30.000000	1.000000	.744298	-.003296
-31.000000	1.000000	.000000	-.003608
-32.000000	1.000000	.193900	-.004060
-33.000000	1.000000	.297301	-.004377
-34.000000	1.000000	.194073	-.004623
-35.000000	1.000000	0.000000	-.004935
-36.000000	1.000000	.306148	-.005237
-37.000000	1.000000	0.000000	-.005554
-38.000000	1.000000	.238938	-.005832
-39.000000	1.000000	.000000	-.006142
-40.000000	1.000000	.000000	-.006510
-41.000000	1.000000	.000000	-.006826
-42.000000	1.000000	.294134	-.006956
-43.000000	1.000000	.000000	-.007272
-44.000000	1.000000	.389593	-.007713
-45.000000	1.000000	.000000	-.008028
-46.000000	1.000000	.356086	-.008176
-47.000000	1.000000	.000000	-.008488
-48.000000	1.000000	.000000	-.008966
-49.000000	1.000000	.000000	-.009283

-8142.000000	1.000000	.215788	-2.475889
-8143.000000	1.000000	.298004	-2.476191
-8144.000000	1.000000	0.000000	-2.476654
-8145.000000	1.000000	.404168	-2.476852
-8146.000000	1.000000	0.000000	-2.477157
-8147.000000	1.000000	.218976	-2.477536
-8148.000000	1.000000	.383929	-2.477770
-8149.000000	1.000000	.295023	-2.478001
-8150.000000	1.000000	.380678	-2.478306
-8151.000000	1.000000	0.000000	-2.478609
-8152.000000	1.000000	.000000	-2.479108
-8153.000000	1.000000	.597230	-2.479325
-8154.000000	1.000000	.220360	-2.479513
-8155.000000	1.000000	0.000000	-2.479814
-8156.000000	1.000000	.453922	-2.480181
-8157.000000	1.000000	.295346	-2.480352
-8158.000000	1.000000	0.000000	-2.480658
-8159.000000	1.000000	.200928	-2.480961
-8160.000000	1.000000	.221405	-2.481479
-8161.000000	1.000000	.384060	-2.481759
-8162.000000	1.000000	.273720	-2.482064
-8163.000000	1.000000	.180710	-2.482373
-8164.000000	1.000000	.429435	-2.482645
-8165.000000	1.000000	0.000000	-2.482825
-8166.000000	1.000000	0.000000	-2.483131
-8167.000000	1.000000	.217056	-2.483601
-8168.000000	1.000000	.295418	-2.483991
-8169.000000	1.000000	.527926	-2.484135
-8170.000000	1.000000	.282117	-2.484385
-8171.000000	1.000000	.214218	-2.484690
-8172.000000	1.000000	.577895	-2.485029
-8173.000000	1.000000	.315359	-2.485259
-8174.000000	1.000000	.302818	-2.485567
-8175.000000	1.000000	0.000000	-2.485871
-8176.000000	1.000000	.221405	-2.486374
-8177.000000	1.000000	.607862	-2.486541
-8178.000000	1.000000	.000000	-2.486847
-8179.000000	1.000000	0.000000	-2.487205
-8180.000000	1.000000	.434414	-2.487494
-8181.000000	1.000000	.419844	-2.487695
-8182.000000	1.000000	.209611	-2.488002
-8183.000000	1.000000	0.000000	-2.488309
-8184.000000	1.000000	.285152	-2.488815
-8185.000000	1.000000	.472755	-2.488974
-8186.000000	1.000000	.287004	-2.489281
-8187.000000	1.000000	0.000000	-2.489586
-8188.000000	1.000000	.516798	-2.489872
-8189.000000	1.000000	.269323	-2.490029
-8190.000000	1.000000	.318434	-2.490260
-8191.000000	1.000000	.421379	-2.490562

-8192.000000	1.000000	.205047	-2.490863
-8193.000000	1.000000	.311833	-2.491151
-8194.000000	1.000000	0.000000	-2.491453
-8195.000000	1.000000	.269323	-2.491756
-8196.000000	1.000000	.699959	-2.492105
-8197.000000	1.000000	.200928	-2.492411
-8198.000000	1.000000	.526879	-2.492714
-8199.000000	1.000000	0.000000	-2.493014
-8200.000000	1.000000	.366850	-2.493497
-8201.000000	1.000000	.384692	-2.493703
-8202.000000	1.000000	.533741	-2.493962
-8203.000000	1.000000	.000000	-2.494271
-8204.000000	1.000000	.485585	-2.494629
-8205.000000	1.000000	0.000000	-2.494935
-8206.000000	1.000000	.532464	-2.495118
-8207.000000	1.000000	0.000000	-2.495426
-8208.000000	1.000000	.218976	-2.495909
-8209.000000	1.000000	.300769	-2.496216
-8210.000000	1.000000	.214218	-2.496469
-8211.000000	1.000000	.000000	-2.496772
-8212.000000	1.000000	.473387	-2.497158
-8213.000000	1.000000	.215788	-2.497466
-8214.000000	1.000000	.710970	-2.497609
-8215.000000	1.000000	0.000000	-2.497919
-8216.000000	1.000000	0.000000	-2.498490
-8217.000000	1.000000	.291830	-2.498734
-8218.000000	1.000000	.484179	-2.498930
-8219.000000	1.000000	0.000000	-2.499231
-8220.000000	1.000000	.503507	-2.499663
-8221.000000	1.000000	.217056	-2.499894
-8222.000000	1.000000	.714745	-2.500048
-8223.000000	1.000000	0.000000	-2.500358
-8224.000000	1.000000	.180710	-2.500712
-8225.000000	1.000000	.296223	-2.501074
-8226.000000	1.000000	0.000000	-2.501382
-8227.000000	1.000000	.214218	-2.501687
-8228.000000	1.000000	.697745	-2.501992
-8229.000000	1.000000	0.000000	-2.502300
-8230.000000	1.000000	.415124	-2.502606
-8231.000000	1.000000	.180710	-2.502911
-8232.000000	1.000000	.301405	-2.503361
-8233.000000	1.000000	.484001	-2.503592
-8234.000000	1.000000	.570714	-2.503795
-8235.000000	1.000000	0.000000	-2.504101
-8236.000000	1.000000	.529673	-2.504503
-8237.000000	1.000000	.291830	-2.504811
-8238.000000	1.000000	.600471	-2.504918
-8239.000000	1.000000	.219720	-2.505213
-8240.000000	1.000000	.214218	-2.505732
-8241.000000	1.000000	.291302	-2.506038

-16284.000000	1.000000	.619619	-4.957530
-16285.000000	1.000000	.685345	-4.957719
-16286.000000	1.000000	.193095	-4.958031
-16287.000000	1.000000	.520677	-4.958662
-16288.000000	1.000000	.422672	-4.958968
-16289.000000	1.000000	.732822	-4.959254
-16290.000000	1.000000	.526476	-4.959559
-16291.000000	1.000000	.536155	-4.959868
-16292.000000	1.000000	.730979	-4.960021
-16293.000000	1.000000	.648726	-4.960324
-16294.000000	1.000000	0.000000	-4.960631
-16295.000000	1.000000	.615233	-4.961114
-16296.000000	1.000000	.080460	-4.961351
-16297.000000	1.000000	.762599	-4.961601
-16298.000000	1.000000	.542089	-4.961792
-16299.000000	1.000000	.424946	-4.962106
-16300.000000	1.000000	.786703	-4.962311
-16301.000000	1.000000	.654897	-4.962558
-16302.000000	1.000000	0.000000	-4.962858
-16303.000000	1.000000	.079275	-4.963378
-16304.000000	1.000000	.724881	-4.963852
-16305.000000	1.000000	.835826	-4.964033
-16306.000000	1.000000	.431577	-4.964334
-16307.000000	1.000000	.742230	-4.964717
-16308.000000	1.000000	.781003	-4.964842
-16309.000000	1.000000	.756245	-4.965124
-16310.000000	1.000000	.287877	-4.965434
-16311.000000	1.000000	.309411	-4.965801
-16312.000000	1.000000	.626695	-4.966096
-16313.000000	1.000000	.848784	-4.966408
-16314.000000	1.000000	.576787	-4.966640
-16315.000000	1.000000	.759061	-4.966946
-16316.000000	1.000000	.575076	-4.967098
-16317.000000	1.000000	.729030	-4.967246
-16318.000000	1.000000	.301946	-4.967662
-16319.000000	1.000000	.218100	-4.968293
-16320.000000	1.000000	.370154	-4.968595
-16321.000000	1.000000	.886150	-4.968895
-16322.000000	1.000000	.193095	-4.969198
-16323.000000	1.000000	.730454	-4.969568
-16324.000000	1.000000	.630276	-4.969749
-16325.000000	1.000000	.925886	-4.969972
-16326.000000	1.000000	.282050	-4.970281
-16327.000000	1.000000	.518167	-4.970791
-16328.000000	1.000000	.576580	-4.971084
-16329.000000	1.000000	.845264	-4.971336
-16330.000000	1.000000	.297555	-4.971501
-16331.000000	1.000000	.321128	-4.971804
-16332.000000	1.000000	.795965	-4.972108

-16333.000000	1.000000	.726462	-4.972279
-16334.000000	1.000000	.218976	-4.972584
-16335.000000	1.000000	.653152	-4.973328
-16336.000000	1.000000	.584777	-4.973511
-16337.000000	1.000000	.826736	-4.973916
-16338.000000	1.000000	.268093	-4.974115
-16339.000000	1.000000	.842196	-4.974424
-16340.000000	1.000000	.732112	-4.974615
-16341.000000	1.000000	.892716	-4.974779
-16342.000000	1.000000	.314287	-4.975079
-16343.000000	1.003000	.500097	-4.975567
-16344.000000	1.000000	.573889	-4.975868
-16345.000000	1.000000	.757472	-4.976165
-16346.000000	1.000000	.441014	-4.976302
-16347.000000	1.000000	.656278	-4.976556
-16348.000000	1.000000	.686457	-4.976848
-16349.000000	1.000000	.678342	-4.977087
-16350.000000	1.000000	0.000000	-4.977394
-16351.000000	1.000000	.361322	-4.978021
-16352.000000	1.000000	.389483	-4.978448
-16353.000000	1.000000	.766744	-4.978655
-16354.000000	1.000000	.180710	-4.978953
-16355.000000	1.000000	.842445	-4.979267
-16356.000000	1.000000	.972135	-4.979426
-16357.000000	1.000000	.600747	-4.979651
-16358.000000	1.000000	.220917	-4.980012
-16359.000000	1.000000	.777985	-4.980580
-16360.000000	1.000000	.717491	-4.980764
-16361.000000	1.000000	.731101	-4.981003
-16362.000000	1.000000	.293425	-4.981234
-16363.000000	1.000000	.442346	-4.981538
-16364.000000	1.000000	.770655	-4.981625
-16365.000000	1.000000	.546705	-4.981942
-16366.000000	1.000000	.300361	-4.982242
-16367.000000	1.000000	.485418	-4.982890
-16368.000000	1.000000	.766594	-4.983213
-16369.000000	1.000000	.841004	-4.983454
-16370.000000	1.000000	.429436	-4.983769
-16371.000000	1.000000	.725219	-4.984056
-16372.000000	1.000000	1.022971	-4.984244
-16373.000000	1.000000	.585007	-4.984409
-16374.000000	1.000000	.219720	-4.984711
-16375.000000	1.000000	.437506	-4.985224
-16376.000000	1.000000	0.000000	-4.985529
-16377.000000	1.000000	.944025	-4.985779
-16378.000000	1.000000	.547012	-4.985955
-16379.000000	1.000000	.591582	-4.986345
-16380.000000	1.000000	.634493	-4.986519
-16381.000000	1.000000	.763424	-4.986647
-16382.000000	1.000000	0.000000	-4.986947

APPENDIX E

PROGRAM "VREF" AND SAMPLE OUTPUT

The following is a listing of "VREF", a program designed for use with the programmable voltage reference test circuit, which adequately demonstrates the degree to which a desired voltage entered into the program may be regulated. The program works in a manner consistent with the description in Appendix C. The data output is listed in section II.

E.1 "VREF" Program Listing

```

10 | *****
20 |
30 | VREF      Voltage Reference.
40 |
50 | THIS PROGRAM IS DESIGNED TO BE USED IN CONJUNCTION WITH
60 | THE PROGRAMMABLE VOLTAGE REFERENCE TEST CIRCUIT, TO PUT OUT
70 | A VOLTAGE ENTERED INTO THE PROGRAM AND, WITH THE AID OF THE
80 | HP3455A DIGITAL VOLTMETER, TO MONITOR THE VOLTAGE PUT OUT
90 | AND TO CORRECT FOR ANY DISCREPANCIES FROM THE DESIRED VOLTAGE
100 | (THE VARIABLE Videal) IN THE PROGRAM) WITH THE PROGRAMMABLE
110 | OFFSET PROVIDED BY THE HP3325A SYNTHESIZER/FUNCTION GENERATOR.
120 |
130 | THE PROGRAMMABLE VOLTAGE REFERENCE TEST CIRCUIT IS PROGRAMMED
140 | THROUGH THE GPIO LINE.
150 |
160 | THE PROGRAMMABLE VOLTAGE REFERENCE TEST CIRCUIT, THE HP3455A
170 | DVM AND THE HP3325A SYNTHESIZER/FUNCTION GENERATOR FORM A CON-
180 | TROL LOOP. THE VOLTAGE IS CORRECTED APPROXIMATELY EVERY 1/3 SEC.,
190 | THE LIMITATION BEING THE SPEED OF THE DVM IN THE HIGH RESOLUTION
200 | MODE. THE CONTROL LOOP IS CAPABLE OF REGULATING THE OUTPUT VOL-
210 | TAGE TO WITHIN +/- 6 microV. TYPICALLY. THE PROGRAMMABLE VOLTAGE
220 | REFERENCE TEST CIRCUIT HAS A VERY LOW NOISE OUTPUT, (OBSERVED TO
230 | BE LESS THEN 10 microV.), AND IS CAPABLE OF SETTLING TO WITHIN
240 | 1 PART PER MILLION WITHIN 2 MICROSECONDS, SO THAT, WITH A FASTER
250 | CONTROL LOOP, IT COULD BE PROGRAMMED AS A HIGH PRECISION WAVE
260 | FUNCTION GENERATOR.
270 |
280 | THE PROGRAM IS EASY TO USE. IT PROMPTS THE USER FOR A VOLTAGE
290 | BETWEEN +5V AND -5V, AND PROCEEDS TO OUTPUT THE VOLTAGE, SETTLING
300 | TYPICALLY WITHIN 10 SECONDS TO THE SPECIFIED VALUE +/- 6 microV.
310 | AFTER THE SYSTEM HAS SETTLED, IT PRINTS THE FIRST 10 VOLTAGES
320 | READ BY THE DVM. IT WILL CONTINUE TO MONITOR AND CORRECT THE
330 | VOLTAGE FOR AN INDEFINITE PERIOD OF TIME, PRINTING EVERY 100TH
340 | VOLTAGE READING, ALONG WITH THE AVERAGE VOLTAGE AND AN ESTIMATE
350 | OF THE STANDARD OF DEVIATION.
360 |
370 | THIS PROGRAM AND THE OPERATION OF THE CONTROL LOOP FORMED BY
380 | THE PROGRAMMABLE VOLTAGE REFERENCE TEST CIRCUIT, THE HP3455A
390 | DIGITAL VOLTMETER, AND THE HP3325A SYNTHESIZER/FUNCTION GENERATOR
400 | FOR THE BASIS FOR HUMEROUS OTHER PROGRAMS, MOST NOTABLY THOSE
410 | DESIGNED TO TEST THE STATIC RESPONSE OF THE LOW-POWER 15-BIT A-D
420 | CONVERTOR.
430 |

```

```

448 | *****
450 |
460 | THIS SECTION SETS THE PRINTER AND INITIALIZES THE DVM AND
470 | THE FUNCTION GENERATOR.
480 |
490 | THE VOLTMETER IS SET TO DC HIGH RESOLUTION AND THE FUNCTION
500 | GENERATOR IS SET TO PROGRAMMABLE DC OFFSET MODE.
510 |
520 | PRINTER IS 16
530 | Voltmeter=722
540 | Func_gen=717
550 | RESET Voltmeter
560 | OUTPUT Voltmeter;"F1R7T1M3A1N1D1"
570 | OUTPUT Func_gen;"SMRD1FUB"
580 |
590 | *****
600 |
610 | THIS SECTION PRINTS A HEADING.
620 |
630 | PRINT " "
640 | PRINT " "
650 | PRINT "DESIRED VOLTAGE      MEASURED VOLTAGE      DIFFERENCE"
660 | PRINT " "
670 |
680 | *****
690 |
700 | THIS SECTION DEFINES THE VALUE OF A BIT, SO THAT VOLTAGE MAY
710 | BE ENTERED IN TERMS OF BITS APPLICABLE TO THE 15-BIT A-D
720 | CONVERTOR.
730 |
740 | Bit=5*2^(-14)
750 | Bits=5*2^(-14)
760 |
770 | *****
780 |
790 | THIS SECTION ALLOWS THE ENTRY OF THE DESIRED VALUE OF THE
800 | VOLTAGE TO BE OUTPUT BY THE PROGRAMMABLE REFERENCE VOLTAGE
810 | TEST CIRCUIT
820 |
830 | INPUT "ENTER VOLTAGE",V_ideal
840 |
850 | *****
860 |
870 | THIS SECTION INSURES VOLTAGE NOT OUT OF RANGE
880 |
890 | IF V_ideal>5 THEN DISP "VOLTAGE OUT OF RANGE"
900 | IF V_ideal>5 THEN V_ideal=5
910 | IF V_ideal<5 THEN BEEP
920 | IF V_ideal<-5*(1-2^(-15)) THEN DISP "VOLTAGE OUT OF RANGE"
930 | IF V_ideal<-5*(1-2^(-15)) THEN V_ideal=-5*(1-2^(-15))
940 | IF V_ideal<-5*(1-2^(-15)) THEN BEEP
950 |

```

```

960 | *****
970 |
980 | THIS SECTION CALLS SUBROUTINE TO WRITE INITIAL VOLTAGE TO
990 | 16-BIT DAC COMPONENT OF PROGRAMMABLE VOLTAGE REFERENCE TEST
1000 | CIRCUIT
1010 |
1020 Dec_rep=INT((5-V_ideal)/(5*2^(-15))) !SETS VAL. FOR SUB Write_dac_val
1030 |
1040 GOSUB Write_dac_voltg
1050 |
1060 | *****
1070 |
1080 GOSUB Read_voltage !CLEARS OUTPUT OF DVM OF PREVIOUS VALUES
1090 |
1100 | *****
1110 |
1120 | INITIALIZATION OF PARAMETERS USED IN FURTHER CALCULATIONS
1130 |
1140 V_dif=0
1150 Avg_v=0
1160 Sse=0
1170 |
1180 PRINT " "
1190 |
1200 | *****
1210 |
1220 | BEGINNING OF MEASUREMENT-CORRECTION LOOP
1230 |
1240 FOR J1=0 TO 1000000
1250 FOR J1=0 TO 1000000
1260 FOR J=1 TO 1000000
1270 |
1280 | *****
1290 |
1300 | THIS LOOP SECTION MEASURES OUTPUT VOLTAGE AND MAKES CORRECTIONS
1310 | FOR DIFFERENCES BETWEEN MEASURED VOLTAGE AND DESIRED (IDEAL)
1320 | VOLTAGE
1330 |
1340 GOSUB Read_voltage
1350 |
1360 V_dif=V_ideal-Value+V_dif
1370 V_out=-100*V_dif
1380 |
1390 OUTPUT Func_gen;"OF",V_out,"V0" ! OUTPUTS CORR. FOR VOLTAGE ON FUNC.
1400 |
1410 GOSUB Read_voltage
1420 |
1430 | *****
1440 |
1450 | THIS LOOP SECTION COMPUTES AVG. VOLTAGE AND STD. DEV.
1460 |
1470 J2=J+1+1000000+J1+1E12
1480 IF J2>=15 THEN Avg_v=Avg_v*(J2-15)/(J2-14)+Value/(J2-14)
1490 IF J2>=15 THEN Sse=((Sse^2*(J2-15)/(J2-14)+(Value-V_ideal)^2/(J2-14)
1500 |
1510 |
1520 |

```

```

1530 | *****
1540 |
1550 | THIS LOOP SECTION PRINTS DATA ON VOLTAGE, AVG. VOLTAGE, AND STD. DE
1560 | EVERY 100TH MEASUREMENT AND FIRST 10 MEASUREMENTS AFTER SETTLING.
1570 |
1580 | IF (J2)=15) AND (J2<25) OR (J2 MOD 100=0) THEN PRINT V_ideal,Value,v
_ideal
1590 | IF (J2=25) OR (J2 MOD 100=0) THEN PRINT " "
1600 | IF (J2=25) OR (J2 MOD 100=0) THEN PRINT "AVG. VOLTAGE=",Avg_u,"STD.
+/-",Sse
1610 | IF (J2=25) OR (J2 MOD 100=0) THEN PRINT " "
1620 | IF J2=25 THEN PRINT " FIRST 10 CONSECUTIVE VOLTAGE MEASUREMENTS PRIN
OVE"
1630 | IF J2=25 THEN PRINT " "
1640 |
1650 | NEXT J
1660 | NEXT J1
1670 | NEXT J11
1680 |
1690 | *****
1700 |
1710 | END OF MEASUREMENT-CORRECTION LOOP
1720 |
1730 | *****
1740 |
1750 | END OF MAIN BODY OF PROGRAM
1760 |
1770 | END
1780 |
1790 |
1800 | *****

```

```

1810 |
1820 | *****
1830 | *****
1840 |
1850 | SUBROUTINE TO OUTPUT CODE TO DAC TO CONTROL VOLTAGE
1860 |
1870 Write_dac_voltg: |
1880 |
1890 IF (Dec_rep)=0) AND (Dec_rep<=32767) THEN Numb=-Dec_rep-1
1900 IF (Dec_rep)=32768) AND (Dec_rep<=65535) THEN Numb=65535-Dec_rep
1910 |
1920 WRITE IO 3,6;Numb ! OUTPUTS CODE TO CONTROL DAC ON GPIO LINE
1930 |
1940 RETURN
1950 |
1960 | *****
1970 | *****
1980 |
1990 | SUBROUTINE TO READ DVM VOLTAGE
2000 |
2010 Read_voltage: |
2020 |
2030 TRIGGER Voltmeter
2040 Status: |
2050 STATUS Voltmeter;Stat
2060 IF Stat=65 THEN Get_value
2070 IF Stat=0 THEN Status
2080 DISP "DVM ERROR"
2090 BEEP
2100 STOP
2110 Get_value: |
2120 ENTER Voltmeter;Value
2130 RETURN
2140 |
2150 | *****
2160 | *****
2170 |

```

E.2 Data from "VREF" with Sample Voltages as Data Points

DESIRED VOLTAGE	MEASURED VOLTAGE	DIFFERENCE
5.000000	5.000000	0.000000
5.000000	5.000000	0.000000
5.000000	5.000000	0.000000
5.000000	5.000000	0.000000
5.000000	5.000000	0.000000
5.000000	5.000000	0.000000
5.000000	5.000010	.000010
5.000000	5.000010	.000010
5.000000	4.999990	-.000010
5.000000	4.999990	-.000010

FIRST 10 CONSECUTIVE VOLTAGE MEASUREMENTS PRINTED ABOVE

DESIRED VOLTAGE	MEASURED VOLTAGE	DIFFERENCE
4.000000	3.999990	-.000010
4.000000	3.999990	-.000010
4.000000	3.999990	-.000010
4.000000	4.000000	0.000000
4.000000	4.000000	0.000000
4.000000	4.000000	0.000000
4.000000	3.999990	-.000010
4.000000	4.000000	0.000000
4.000000	4.000000	0.000000
4.000000	4.000000	0.000000

FIRST 10 CONSECUTIVE VOLTAGE MEASUREMENTS PRINTED ABOVE

DESIRED VOLTAGE	MEASURED VOLTAGE	DIFFERENCE
2.000000	2.000000	0.000000
2.000000	2.000000	0.000000
2.000000	1.999990	-.000010
2.000000	1.999990	-.000010
2.000000	2.000000	0.000000
2.000000	1.999990	-.000010
2.000000	2.000010	.000010
2.000000	2.000010	.000010
2.000000	2.000010	.000010
2.000000	2.000000	0.000000

FIRST 10 CONSECUTIVE VOLTAGE MEASUREMENTS PRINTED ABOVE

DESIRED VOLTAGE	MEASURED VOLTAGE	DIFFERENCE
1.000000	1.000005	.000005
1.000000	1.000000	0.000000
1.000000	1.000000	0.000000
1.000000	1.000000	0.000000
1.000000	1.000001	.000001
1.000000	1.000002	.000002
1.000000	1.000001	.000001
1.000000	1.000001	.000001
1.000000	1.000002	.000002
1.000000	1.000001	.000001

FIRST 10 CONSECUTIVE VOLTAGE MEASUREMENTS PRINTED ABOVE

DESIRED VOLTAGE	MEASURED VOLTAGE	DIFFERENCE
0.000000	0.000000	0.000000
0.000000	0.000000	0.000000
0.000000	0.000000	0.000000
0.000000	0.000000	0.000000
0.000000	-0.000001	-.000001
0.000000	0.000000	0.000000
0.000000	0.000000	0.000000
0.000000	0.000000	0.000000
0.000000	0.000000	0.000000
0.000000	0.000000	0.000000

FIRST 10 CONSECUTIVE VOLTAGE MEASUREMENTS PRINTED ABOVE

DESIRED VOLTAGE	MEASURED VOLTAGE	DIFFERENCE
-1.000000	-1.000000	0.000000
-1.000000	-.999998	.000002
-1.000000	-.999999	.000001
-1.000000	-.999997	.000003
-1.000000	-.999999	.000001
-1.000000	-1.000000	0.000000
-1.000000	-.999999	.000001
-1.000000	-.999997	.000003
-1.000000	-1.000001	-.000001
-1.000000	-1.000001	-.000001

FIRST 10 CONSECUTIVE VOLTAGE MEASUREMENTS PRINTED ABOVE

DESIRED VOLTAGE	MEASURED VOLTAGE	DIFFERENCE
-4.000000	-4.000000	0.000000
-4.000000	-4.000000	0.000000
-4.000000	-4.000000	0.000000
-4.000000	-4.000000	0.000000
-4.000000	-4.000000	0.000000
-4.000000	-3.999990	.000010
-4.000000	-4.000000	0.000000
-4.000000	-4.000000	0.000000
-4.000000	-4.000000	0.000000
-4.000000	-4.000000	0.000000

FIRST 10 CONSECUTIVE VOLTAGE MEASUREMENTS PRINTED ABOVE

DESIRED VOLTAGE	MEASURED VOLTAGE	DIFFERENCE
-4.999847	-4.999830	.000017
-4.999847	-4.999860	-.000013
-4.999847	-4.999830	.000017
-4.999847	-4.999850	-.000003
-4.999847	-4.999860	-.000013
-4.999847	-4.999830	.000017
-4.999847	-4.999860	-.000013
-4.999847	-4.999830	.000017
-4.999847	-4.999860	-.000013
-4.999847	-4.999850	-.000003
-4.999847	-4.999850	-.000003

FIRST 10 CONSECUTIVE VOLTAGE MEASUREMENTS PRINTED ABOVE

DESIRED VOLTAGE	MEASURED VOLTAGE	DIFFERENCE
3.141590	3.141590	0.000000
3.141590	3.141590	0.000000
3.141590	3.141590	0.000000
3.141590	3.141580	-.000010
3.141590	3.141580	-.000010
3.141590	3.141590	0.000000
3.141590	3.141590	0.000000
3.141590	3.141590	0.000000
3.141590	3.141590	0.000000
3.141590	3.141590	0.000000

FIRST 10 CONSECUTIVE VOLTAGE MEASUREMENTS PRINTED ABOVE

APPENDIX F
EQUIPMENT USED

The following equipment was used in the measurements described in this thesis.

Table F.1 Equipment Used

Model	Description	Serial #
HP9845B	Computer	#1742A01011
HP3455A	Digital Voltmeter	#1622A03512
HP3325A	Synthesizer/Function Generator	#1748A01578
HP59500A	Multiprogrammer Interface	#1927A01751
HP6236B	Triple Output Power Supply	#1705A00495
HP6236B	Triple Output Power Supply	#1705A00441
Tkx 5440	Tektronix Oscilloscope (5A48 Dual Trace Amp.) (5A26 Dual Diff. Amp.) (5B40 Time Base)	#B097445
Tkx 2213	60 MHz Oscilloscope	#B014954

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SOME CONSIDERATIONS IN THE DESIGN OF A
LOW-POWER, 15-BIT, ANALOG-TO-DIGITAL CONVERTER

by

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AN ABSTRACT OF A MASTER'S THESIS

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MASTER OF SCIENCE

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ABSTRACT

The development of new devices which must be powered by batteries has given rise to demands for very low-power analog-to-digital converters. When continuous operation is not a requirement, power may be reduced by power switching, operating the device at very low duty-cycles.

This design for a low-power, 15-bit ADC performs analog-to-digital conversions on data from two separate channels, 128 times per second, and is capable of completing both conversions in 330 microseconds, operating at a duty cycle of 4.2 %. The power consumed was measured at 6.55 mW for the ADC section under these circumstances.

The magnitude of the differential linearity error was measured to be 0.247 LSB, with approximately 0.501 LSB of noise.

The calculations and considerations required to design the circuit were explored in detail.

Some new test circuits for measuring power and completing static differential linearity error measurements were described.