SOME APPLICATIONS OF MICROELECTRONIC DEVICES IN DATA ACQUISITION AND PROCESSING

by

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INTRODUCTION

During the Second World War, stringent military requirements imposed a constant pressure to produce smaller, lighter and reliable electronic equipment which had more capabilities and higher performance. These requirements resulted in only miniature tubes and miniature passive elements. True miniaturization was not a success until the invention of the transistor in 1948. The transistor was a revolution in electronic industry. Since this invention, industry has introduced one device after another and one process after another such that the transistor by now has broken frequency, power and cost barriers. In just a few years, the transistor has found its way into modern electronic equipment. The further advancement in semiconductor technology has brought about another development called the integrated circuit which promises an even greater impact on electronic systems.

The typical integrated circuit is a piece of tiny block silicon into or on which all circuit components are manufactured. Individual parts are not separable from the complete circuit. Connections between each component is done by a deposition of appropriate thin film metal strips on the silicon block.

The integrated circuit is particularly attractive in applications such as missile guidance and space exploration where high degree of performance and reliability, small size and light weight are the basic requirement, and in applications such as data processings where identical circuits are used in very large quantities.

In this report, some basic semiconductor properties and definitions which are related to the understanding of integrated circuits are presented first. Qualitative description of the fabrication of monolithic integrated circuits

and passive components and four families of digital logic circuits are presented next. In the last part of this report, the application of integrated circuits in data processing is presented.

SEMICONDUCTOR GROWTH AND IMPURITY DIFFUSIONS[1,3]

Complementary Error Function Distribution of Diffused Impurities

The transistor with inhomogeneous impurity distributions has better electrical performance and technological advantages. Inhomogeneous impurity distributions are mostly obtained by diffusion of impurities. At semiconductor crystal temperature below approximately 300°C, impurities are immobile; however, at higher temperature, 800-1200°C, impurities become mobile. Gaseous state impurities are usually introduced on the surface of high temperature silicon or germanium crystal. As time passes, more and more impurities diffuse deeper into the crystal.

The flow of current I due to the impurity gradient for one dimentional, positive particles is expressed as

$$I = - qAD \frac{\partial N}{\partial x} \qquad (1\text{-}1)$$

N: impurity concentration

D: diffusion constant

q: charge of a particle

A: Area

At any point in the crystal, if current changes, there must be a corresponding change in the build-up of impurities, or mathematically

$$qA\frac{\partial N}{\partial t} = -\frac{\partial I}{\partial x} \qquad (1\text{-}2)$$

combining equations (1-1) and (1-2) we have

$$\frac{\partial N}{\partial t} = D\frac{\partial^2 N}{\partial x^2} \qquad (1\text{-}3)$$

The impurity concentration at the heated crystal surface N_o is assumed to be constant and independent of diffusion time. Then the solution to equation (1-3) is given by

$$N = N_o \left(1 - \frac{x}{\sqrt{\pi}}\int_0^{\frac{x}{2\sqrt{Dt}}} e^{\varepsilon^2}\, d\varepsilon\right)$$

$$= N_o \left(1 - \operatorname{erf}\frac{x}{2\sqrt{Dt}}\right) = N_o \operatorname{erfc}\frac{x}{2\sqrt{Dt}} \qquad (1\text{-}4)$$

In diffusing a uniformly doped silicon wafer of n- or p-type, the first procedure is to raise temperature of the silicon wafer to about 1200°C. Then one of the wafer surfaces is exposed to a gas of uniform impurity concentration, N_o. The gaseous state impurity, called diffusant, will diffuse into the silicon wafer. Distribution of the impurity in the silicon wafer is as shown in Fig. 1-1, if diffusant and original doping of the silicon wafer are of the same type; or in Fig. 1-2, if diffusant and the original doping are of an opposite type.

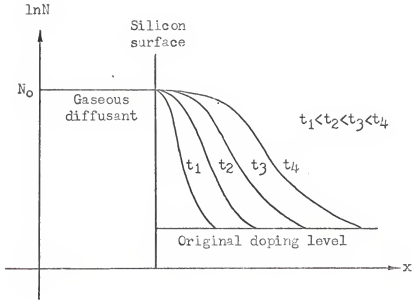

lnN
Silicon surface
N_o
Gaseous diffusant
$t_1<t_2<t_3<t_4$
t_1 t_2 t_3 t_4
Original doping level
x

Fig. 1-1

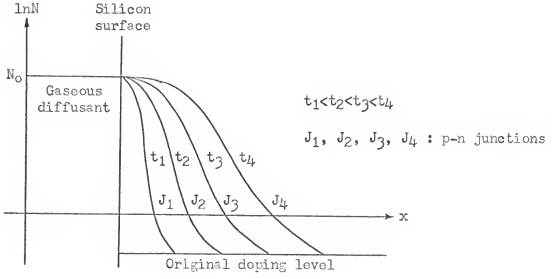

lnN
Silicon surface
N_o
Gaseous diffusant
$t_1<t_2<t_3<t_4$
J_1, J_2, J_3, J_4 : p-n junctions
t_1 t_2 t_3 t_4
J_1 J_2 J_3 J_4
x
Original doping level

Fig. 1-2

Note that a junction is formed, if the diffusant and the original doping are of the opposite type, at the place where the number of diffusant atoms and the number of atoms of the original doping are equal.

Multiply Diffused Transistor

Drift transistors formed by two diffusions from the same side of the crystal are known as planar transistors. By utilizing a very thin layer of silicon dioxide on the crystal surface, impurities diffusing into the crystal can be restricted only to desired places. The silicon-dioxide is easily grown directly on the silicon surface by oxidation. The thin oxide is sufficiently impervious to impurities so that diffusion can proceed only where openings through the oxide exist. The delineation of the openings is accomplished by using photographic emulsion techniques and chemical etching. The planar NPN transistor, for example, begins with a uniformly doped n-type silicon substrate. The substrate is then oxidized to grow a thin layer of silicon dioxide as shown in Fig. 1-3.

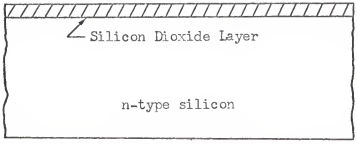


Fig. 1-3

A part of the silicon dioxide layer is etched away to make an opening for the diffusion of impurities. Gaseous state trivalent impurity such as boron is then introduced to the opening and the impurity diffuses through the opening to constitute p-type transistor base as shown in Fig. 1-4.

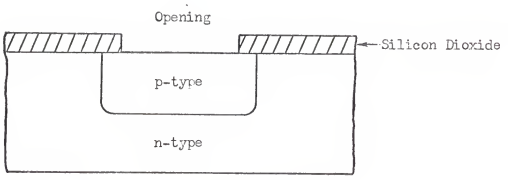


Fig. 1-4

Reoxidizing the opening, covering the opening by a new layer of silicon dioxide is the next step in the process. A smaller window on the new layer is then etched out for another diffusion. The diffusant is pentavalent material such as phosphorous. By the same processes, a large part of the p-type material is again changed into n-type which constitutes the emitter of the transistor. The final result is shown in Fig. 1-5.

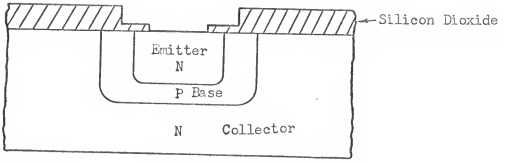


Fig. 1-5

Such planar transistors consist of three separate semiconductor layers. The wafer represents the collector of a transistor. If more than one transistor is to be fabricated on the same wafer, the transistors have a common collector. For the manufacture of discrete transistors, this is entirely permissible, since the wafer will eventually be separated into individual transistor dice.

For monolithic integrated circuits, where all components, active and passive, are on or in the same wafer, a common collector is not permitted. Various components must be isolated electrically from one another in order to have proper functions. Isolation is accomplished by means of reverse-biased p-n junctions.

Epitaxy

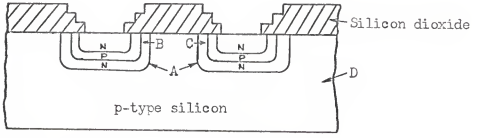
Epitaxy is a method by which a thin additional layer of a semiconductor material is grown from the vapor phase by deposition; i.e., the growth of a single crystal material upon a single-crystal substrate so that the crystal structure of the grown layer is an exact extention of the substrate crystal structure. The growth of intrinsic silicon layers by epitaxy is not a common requirement. The common practice is to grow epitaxially a thin layer of n-type or p-type silicon with a controlled doping level. This is accomplished by introducing a mixture of silicon tetrachloride, hydrogen and phosphine (PH_3) gases onto a heated subtrate for n-type epitaxial growth and a mixture of silicon tetrachloride, hydrogen and diborane (B_2H_4) for p-type.

FABRICATION OF MONOLITHIC INTEGRATED CIRCUITS

Diffused-collector Process[3,5]

The difference between discrete transistors and monolithic integrated circuit transistors is that the integrated circuit transistor has three p-n junctions and four semiconductor layers. The fourth layer is the common layer shared by various transistors. The p-n junction formed by the fourth layer and the collector of transistors isolates the transistor from the other components when the p-n junction is reverse-biased.

The diffused-collector process starts with a p-type (for n-p-n transistors) silicon wafer on which a layer of silicon dioxide is grown. The silicon dioxide is selectively etched to open specific areas through which an n-type impurity can diffuse to form the collector of the transistors. By the same method as is used to fabricate planar transistors, base and emitter are formed subsequently. Two transistors formed by this process are shown in Fig. 2-1.



A: p-n junction

B, C: collector of the transistor

D: p-type silicon substrate

Fig. 2-1

In the figure if B and C are held positive with respect to D, then p-n junction A is reverse-biased and the two transistors are isolated.

Since diffusion of impurities is performed from the same side of the wafer, impurity distribution as a function of distance x into the wafer is as shown in Fig. 2-2. It is seen that the most undesirable situation is a negative impurity gradient of the collector. The number of impurities in the collector decreases as x increases toward the substrate.

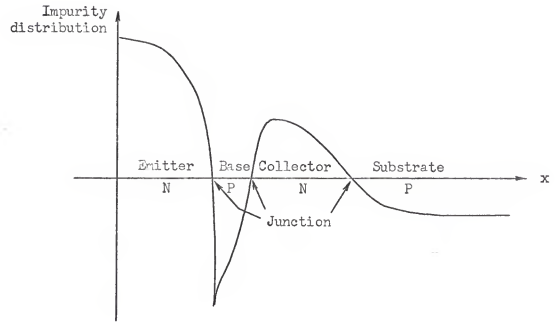


Fig. 2-2

Parasitic capacitance existing between base and collector is determined mostly by impurity concentration in the collector adjacent to base-collector junctions. Impurity concentration is almost a maximum at the base-collector junction, making parasitic collector-base capacitance value a maximum. Thus switching speed is largely impaired. Breakdown voltage is also reduced.

Triple-diffusion Process

This process starts with an n-type substrate which serves to form the collector of transistors and utilizes three successive diffusions of impurities. The n-type substrate is then covered by a thermally grown layer of silicon dioxide. All regions of silicon dioxide, except the places where transistors, diodes and other passive components are to be formed, are removed. The entire substrate is heavily diffused with p-type impurity, such as boron, until the diffusing impurities from both surfaces meet at the center of the substrate. A layer of silicon dioxide is grown over the surface of the substrate that has silicon dioxide left unremoved.

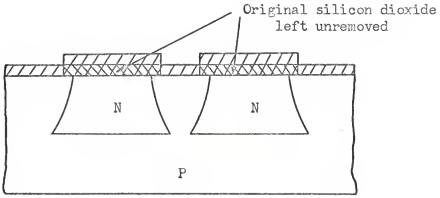


Fig. 2-3 (a)

By performing successive window cutting, p-type impurity diffusion, oxidization, window cutting, and n-type impurity diffusion, a triple-diffusion monolithic integrated circuit can be obtained. Fig. 2-3(b) is an example of two transistors fabricated on a p-type substrate. By properly reverse-biasing the p-n junction formed by p-type substrate and n-type collector of the transistor, the transistors can be isolated from each other.

The advantage of this process is that the collector of a transistor has a

uniform doping level. An optimum doping level for the collector may be chosen so that collector-to-base capacitance can be a minimum and the collector-to-base breakdown voltage can be a maximum. However, since a certain doping level of collector is required to ensure proper characteristics, some considerable value of capacitance always exists between collector and substrate, impairing switching speed or high frequency capabilities. Since p-type substrate is obtained from an n-type starting material by diffusion, it takes a very long time for p-type diffusant to reach the center of the subtrate; therefore, the thickness of the wafer must be limited in order to maintain a reasonable diffusion time, and at the same time a minimal thickness must be provided to assure mechanical strength.

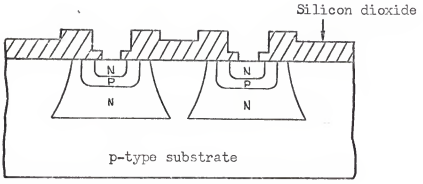


Fig. 2-3 (b)

Epitaxy-diffusion Process

Integrated circuits fabricated by this method begin with a p-type silicon substrate upon which a thin layer (approximately 25 microns) of n-type epitaxial film is grown. The n-type epitaxial film becomes the collector of transistors, or an element of diodes and capacitors. A thin film of silicon

dioxide is grown over the n-type epitaxial layer. Unnecessary parts of silicon dioxide are etched away using a photolithographic masking process. Remaining are places where transistors, diodes, diffused resistors, etc., are to be fabricated. The substrate with n-type epitaxial layer and etched silicon dioxide is now subjected to p-type impurity diffusion. The result after p-type diffusion of fabricating two transistors is shown in Fig. 2-4. Note that all regions except those covered by unetched silicon dioxide are now p-type silicon

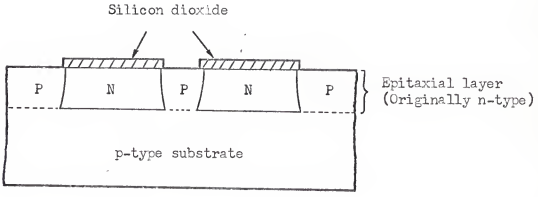


Fig. 2-4

which serves to isolate one element from another. A new layer of silicon dioxide is grown over the entire wafer. It is seen that the existing silicon dioxide grows thicker. By the same method as before, i.e., window cutting and p-type impurity diffusion to fabricate the base of transistors; silicon dioxide growth, window cutting and n-type impurity diffusion to fabricate the emitter region of transistors; the integrated circuit containing two transistors can be obtained as shown in Fig. 2-5.

Integrated circuits obtained by an epitaxy-diffusion process have all the advantages of those by a triple-diffused process, and there are no limitations on the thickness of the starting wafers. The doping level of the substrate may

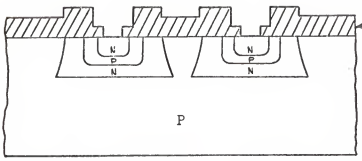


Fig. 2-5

be chosen so that the parasitic capacitance between collector and substrate can be minimized without affecting other electrical characteristics.

Capacitors for Monolithic Integrated Circuits

In a p-n junction, there exists a depletion region which represents a parallel-plate capacitor, since when an incremental reverse voltage is added to or substracted from the p-n junction, charge is stored on or recovered from both sides of the junction. This is called junction capacitance. The capacitance depends on the applied voltage, dielectric constant, impurity concentration and area. The junction capacitance per unit area for the unsymmetrical step junction is expressed as

$$C = \left[\frac{q\epsilon\epsilon_0(N_a + N_d)}{2Vt}\right]^{\frac{1}{2}} \left[\left(\frac{N_d}{N_a}\right)^{\frac{1}{2}} + \left(\frac{N_a}{N_d}\right)^{\frac{1}{2}}\right]^{-1} \qquad (2\text{-}1)$$

N_a: Acceptor impurity concentration

N_d: donor impurity concentration

V_t: total voltage between two junctions

ϵ: dielectric constant

ϵ_o: permittivity of free space

In many practical cases, one impurity concentration is much larger than the other. Let N represent the impurity concentration on the lightly doped side, then the junction capacitance per unit area is

$$C = \left(\frac{q\epsilon\epsilon_o N}{2V_t}\right)^{\frac{1}{2}} \qquad (2\text{-}2)$$

For a linearly graded junction, unit area capacitance is

$$C = (\epsilon\epsilon_o)^{\frac{2}{3}} \left(\frac{q\frac{dN}{dx}}{12V_t}\right)^{\frac{1}{3}} \qquad (2\text{-}3)$$

In monolithic integrated circuits, capacitors are reverse-biased diffused p-n junctions within the silicon material. They are fabricated simultaneously with other circuit elements. The fabrication of diffused capacitors, the same as is used to fabricate transistors, starts with a p-type silicon wafer on which an n-type epitaxial layer is grown. The epitaxial layer is covered with silicon dioxide, which, except the regions where circuit elements are to be fabricated, is etched away. The wafer is then subjected to deep p-type impurity diffusion until the diffusant reaches the p-type starting material to isolate each remaining n-type island from other by back-to-back diodes. The previously unetched silicon dioxide, after a layer of silicon dioxide is again grown over the entire wafer, is masked and etched according to the area required for bases of transistors, anodes of diodes and a plate of capacitors. A p-type diffusion is again conducted over the wafer and bases of transistors, diodes and junction capacitors are formed. Again the newly diffused areas, except for

the formation of ohmic contacts to the capacitor plates, are covered with silicon dioxide. The diffused capacitor[3] is shown in Fig. 2-6.

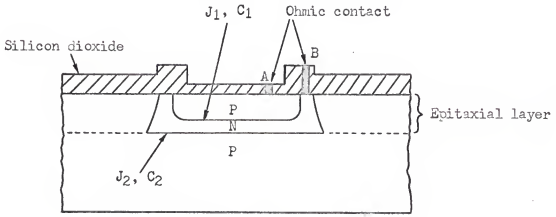


Fig. 2-6

The capacitor C_1 associated with junction J_1 is the desired capacitance. The capacitor C_2 is parasitic and is coupling between the substrate and any element in the wafer.

Every junction capacitor has always a series resistance resulting from the bulk resistance of the n-type region. The equivalent circuit for the diffused capacitor is shown in Fig. 2-7.

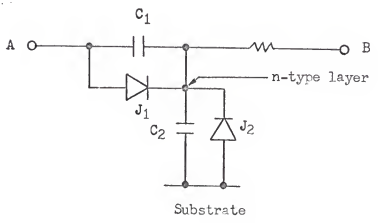


Fig. 2-7

It is seen that two junction diodes must be back-biased to prevent J_1 and J_2 from conducting. The potential at the substrate must be more negative than A in order to minimize the parasitic capacitance C_2.

Diffused capacitors are relatively simple and inexpensive to fabricate. However, parasitic capacitance is inherently larger and the maximum unit area capacitance is relatively small. Moreover, the capacitance is a function of voltage difference between two plates; its value changes when the voltage difference changes and the capacitor must be properly polarized. The difficulties can be greatly reduced by utilizing a combination of semi-conductor and thin-film processes. The advantages are offset by additional process steps and associated higher costs. One of the commonly used thin film capacitors for monolithic structures is the silicon dioxide capacitor.

Silicon dioxide capacitors consist of two plates separated by a thin layer of silicon dioxide. The two plates are the heavily doped n-type silicon layer and the aluminum metallization film. The procedure to fabricate the capacitor is essentially the same as that of diffused capacitors, except for the second p-type diffusion. Instead of the p-type impurity diffusion, the n-type epitaxial island is diffused with n-type impurities to form a heavily doped n-type region which is covered with a layer of silicon dioxide. A thin layer of aluminum is then deposited on the silicon dioxide layer. The silicon dioxide capacitor and its equivalent circuit are shown in Fig. 2-8.

The p-n junction J is used to provide isolation of the capacitor C from the substrate. The series resistor R_p and capacitor C_p are parasitic elements associated with the bulk resistance of heavily doped n-type region and the p-n junction J. The capacitor C is independent of the voltage difference between two plates and is bipolar. Since the parasitic resistance is smaller than that in the junction transistor, ω is higher.

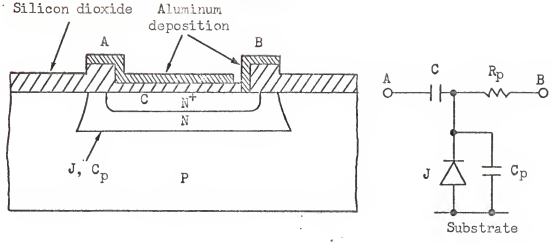


Fig. 2-8

Resistors for Monolithic Integrated Circuits

Resistors for monolithic integrated circuits are obtained by utilizing the bulk resistance of n- or p-type semiconductor or of the deposited thin film. A practical way to fabricate a defined value of resistance is to obtain a separate thin region for diffusions, where the extent of the diffusions is the same as is used to fabricate bases or emitters of transistors, to simplify the fabrication process, and use the separate region as the required resistor. Let ϱ be the resistivity of the diffused semiconductor region, where ϱ is determined by the extent of diffusion. Then the resistance of the volume of semiconductor with cross-sectional area $W \cdot D$ and length L is defined by

$$R = \varrho \frac{L}{WD}$$

Since ϱ and D, the depth of diffusion, are determined by the same requirements as are used to fabricate bases or emitters of transistors, the design of a resistor of a given value is simply to find a suitable proportion of the width of diffused area W and length L, or

$$\frac{L}{W} = \frac{RD}{\rho}$$

In transistors, emitter regions are more heavily diffused than base regions. Therefore emitter diffusions provide a low-resistivity region and base diffusions provide a medium resistivity region for resistor fabrication. Top and cross-sectional views of a diffused resistor are shown in Fig. 2-9.

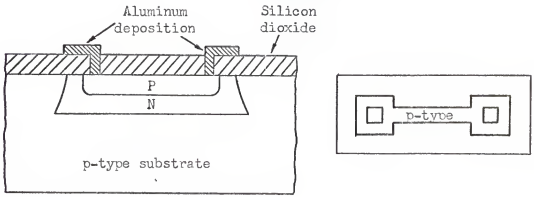


Fig. 2-9

The resistor made by diffusion produces a distributed capacitance and a distributed p-n-p transistor. In order to prevent conduction between each layer, it is proper to keep n-type epitaxial layer at the highest potential.

Multiphase Monolithic Integrated Circuits

In the monolithic integrated circuits previously discussed, isolation between each element is accomplished through the use of back-to-back diodes which are provided by an additional p-type semiconductor layer. The isolation so provided is very effective; however, the parasitic capacitance associated with p-n junctions between circuit elements and the substrate has conspicuous drawbacks on the switching speed or frequency response of the integrated

circuit. The parasitic p-n-p transistor formed by bases, collectors of transistors and the p-type substrate may shunt useful signal or power to the substrate. These drawbacks can be greatly reduced by physically isolating each element from the other; that is, each element, active or passive, is separated by a layer of thin electrically and chemically inert dielectric material within the wafer.

The fabrication of multiphase monolithic integrated circuits starts with an n-type uniformly doped silicon wafer on which a layer of silicon dioxide is grown. The silicon dioxide is selectively etched to open windows for further isolation channel etching. Then on the etched surface of the wafer, a layer of insulation, silicon dioxide, for example, is grown. The resulting wafer is shown in Fig. 2-10. The unetched n-type islands are later on used to fabricate transistors, diodes, resistors and capacitors by diffusions or deposition of thin film materials.

A layer of silicon is epitaxially grown again over the surface. The thickness of the grown polycrystalline material is determined by mechanical strength of the layer required to withstand subsequent fabrication operations. The starting n-type silicon, except unetched islands, is taken away mechanically. The resulting wafer is shown in Fig. 2-11.

The remaining n-type silicon islands are used to fabricate transistors, etc., by diffusion.

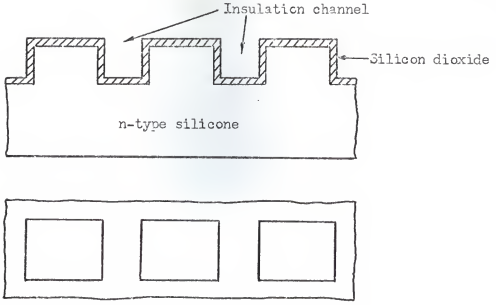


Fig. 2-10

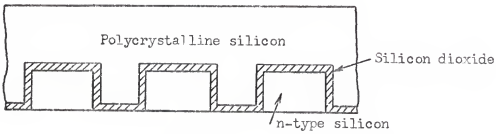


Fig. 2-11

DIGITAL LOGIC CIRCUITS

All the integrated logic circuits presently available are of the direct translation form or of the modified version of the discrete design. It is quite possible that, as the state-of-the-art improves and technology advances, more convenient and wider-ranged integrated circuits will add to the present ones. Among the logic circuits commercially available are the resistor-transistor logic circuit, the diode-transistor logic circuit, the emitter-coupled transistor logic circuit and the transistor-transistor logic circuit.

No one logic circuit is better than any other for all applications. Each has its own advantages such as speed, power consumption, noise immunity, etc., in a certain application. The circuit configuration differs more or less from one manufacturer to another; however, the basic theory upon which the logic circuits rest is the same. A discussion of these logic circuits follows.

Resistor-Transistor Logic (RTL)[4,6]

RTL is a modified form of the Direct-Coupled Transistor Logic. Its basic circuit is the Direct-Coupled Transistor Logic circuit with addition of a suitable resistor to each transistor base circuit. Figs. 3-1 and 3-2 are schematic diagrams for the RTL NOR gate and the RS flip-flop.

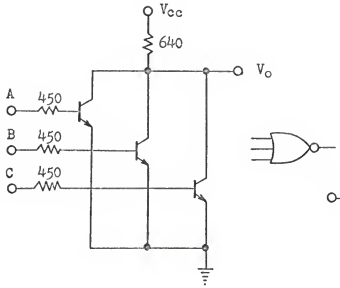


Fig. 3-1

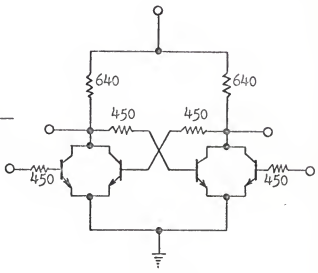
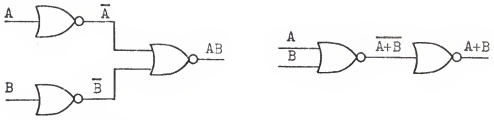


Fig. 3-2

It is observed from Fig. 3-1 that for positive logic, V_o is in the logic 0 state (low voltage) when either A or B or C is in the logic "1" state, and that

V_o is in 1 state when all inputs are in the 0 state. The number of inputs can be increased to such an extent that when all inputs are in the 0 state, the combined leakage current through all the transistors does not pull down V_o substantially to affect the required output voltage swing. All logic functions can be realized using RTL NOR circuits as shown in Fig. 3-3.



AND OR

Fig. 3-3

Since RTL integrated circuits have less stringent requirements on individual circuit components and are relatively easy to fabricate, they have many multiple-function and complex elements such as monolithic J-K flip-flops, decade counters, full adders and four-bit shift registers.

In certain applications where low power dissipation is required the milliwatt RTL is available. The value of base resistors and the collector load resistor is significantly increased to reduce power consumption as shown in Fig. 3-4.

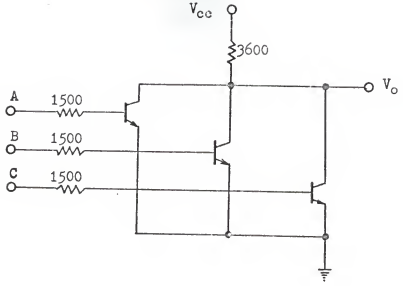


Fig. 3-4

Diode-Transistor Logic (DTL) [4,6]

The DTL integrated circuit family has many advantages such as large output voltage swings and higher noise immunities over the RTL. The basic circuit of the family is shown in Fig. 3-5.

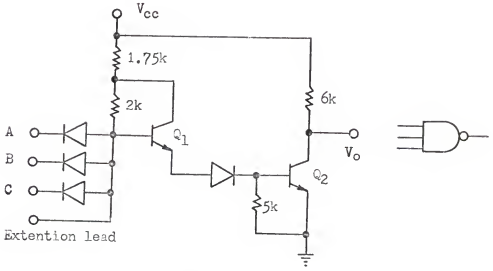


Fig. 3-5

The noticeable feature of this circuit is the replacement of one of the two offset diodes usually found in conventional DTL circuits by the transistor Q_1 whose collector is connected to a point in the input pull-up resistor. The transistor provides current to drive the inverter and at the same time reduces the value of the Q_2 base resistor and eliminates the need of using the negative power supply for rapid transistor turn-off. High speed diodes or input extenders can be connected to the input extention lead for greater fan-in requirements.

The outputs of two or more DTL gates may be connected together to perform an OR function. This connection is very useful and often results in a reduction in the total amount of circuitry to implement a function. For example, the outputs of two gates with inputs A,B,C, and C,D,E are connected together as shown in Fig. 3-6.

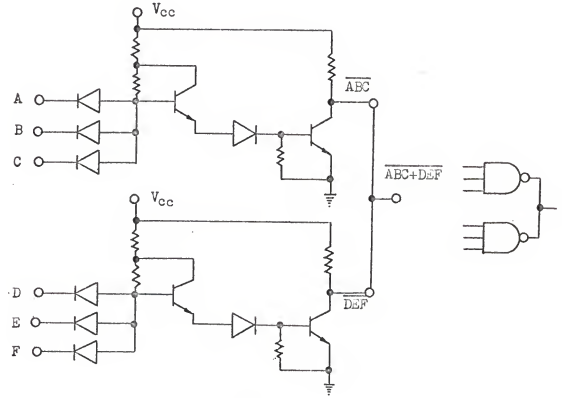


Fig. 3-6

From the circuit diagram of the gates, it is clear that either output may pull the connection point to ground. To make the connection point positive, both outputs must be positive, or all the inputs must be at the ground potential simultaneously. This is obviously an AND operation. The combined output is expressed as $\overline{ABC} \cdot \overline{DEF}$ which by DeMorgan's theorem is equal to $\overline{ABC + DEF}$.

In many instances, integrated circuits must operate physically close to relays or devices producing noise spikes higher than noise immunity levels. The DTL circuits can be modified to provide higher noise immunity levels to reject voltage disturbances on signal and ground lines. This logic circuitry is called Variable Threshold Logic (VTL). The basic VTL circuit is shown in Fig. 3-7. The noise immunity level can be changed from 2V to 5V by changing the values of V_1 and V_2.

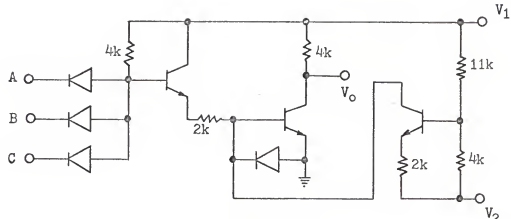


Fig. 3-7

Emitter-coupled Transistor Logic (ECTL)[4,6]

Because of inherent limitations, an integrated circuit family can be used only in some applications. For an application in the field of high switching speeds, short propagation delays, low power dissipations, high fan-in and fan-out and better noise immunity, the ECTL circuit is the choice. The basic ECTL

gate circuit is shown in Fig. 3-8.

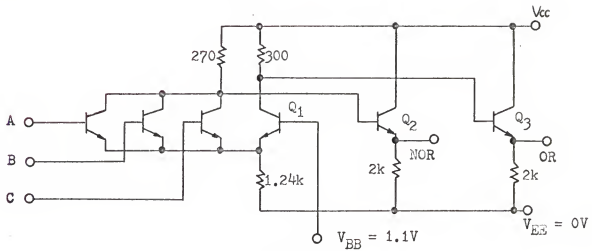


Fig. 3-8

The circuit consists of a current mode switch followed by two emitter followers serving as output stages. The current switch consists of three common collector transistors and a fixed bias transistor. The fixed bias transistor makes the operating point of the switch always stay at the center of the transition region. The emitter follower stages are to restore output DC levels. For example, if all inputs are at the logical 0, input transistors are OFF. The base voltage of Q_2 is at 5V which makes Q_2 conduct and logical 1 appears at the NOR output. Since Q_1 is conducting when all the inputs are logical 0, the base voltage of Q_3 is less positive than V_{cc} determined by collector and emitter resistors of Q_1, and the OR output is logical 0. If one or more inputs are at the logical 1 potential, NOR and OR outputs become logical 0 and 1 respectively. Thus a logical function and its complement are available simultaneously at outputs. This scheme not only is convenient in system designs but also considerably reduces propagation delays.

Transistor-Transistor Logic (TTL)[6]

TTL circuits are another modified version of the DTL. A fast responding multiple-emitter transistor is used instead of diodes. The multiple-emitter transistor performs the same functions as the diodes in the DTL. However, the transistor action of the multiple-emitter transistor causes the next transistor (Fig. 3-9) to turn-off more rapidly, thus providing an inherent switching time advantage over the DTL circuit. TTL circuits have active pull-up and pull-down elements which form a low output impedance in both logical 0 and 1 states. The low output impedance in either state rejects reactively coupled a-c pulses and keeps the time constant small to preserve wave shape integrity.

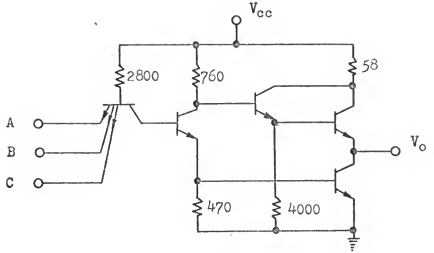


Fig. 3-9

The TTL circuit family consists of gates and flip-flops as well as complex function elements to perform all logic functions and to reduce system cost.

SOME APPLICATIONS OF INTEGRATED CIRCUITS

In arithmetic and control units of digital computers, counters, shift registers and half and full adders are intensively used. The activities of these sequential circuits may be performed by a variety of counting circuits. In applications where the speed is not as critical as in electronic computers, electro-mechanical relays can also be used to implement the counting operations. The following is a discussion of how these operations are implemented using integrated circuits.

Ripple-carry Counter (Frequency Divider)[8]

The simplest counting method is by a non-synchronous technique as shown in Fig. 4-1. Each stage in the counter has its outputs cross-connected to its imputs so that input pulses are routed alternately to each of the two inputs. Consider flip-flop A for example. Suppose the flip-flop state is as shown after an input pulse has appeared, then C is at a higher potential (logical 1) and S is at ground potential (logical 0). When the next pulse comes, the pulse is routed to C and the flip-flop complements itself and propagates a change to the flip-flop B and at the same time makes preparations for routing the next input pulse to S.

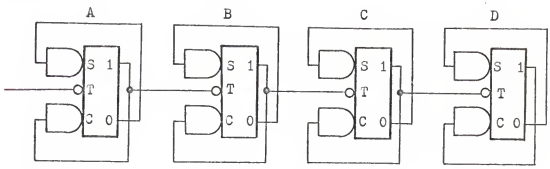


Fig. 4-1

Each output waveform is a square wave at one-half the frequency of its input. By using the output of one stage as the input, the frequency is successively halved as shown in Fig. 4-2.

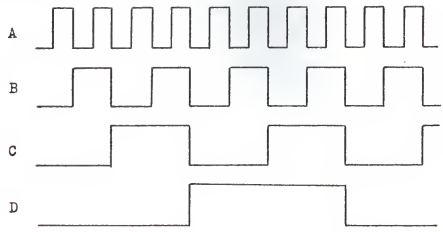


Fig. 4-2

When the circuit is used for a frequency divider, there are no serious problems whatsoever since the frequency of the output stage is of greatest importance. However, when the circuit is to be used in applications where two or more outputs of the flip-flops are used as inputs to a logic gate, the propagation delays between stages can cause errors.

Synchronous Counter

As individual delays are cumulative, the change of state in the last flip-flop may be long behind that of the first flip-flop. This may result in unwanted gating spikes or shortened pulses. Thus the ripple counter is not suitable in many applications. The delay can be effectively avoided through the use of synchronous techniques. The synchronous counter has its clock inputs connected in common and the ANDed logical 1 of the previous stages is connected to the S and C terminals of the following stage as shown in Fig. 4-3.

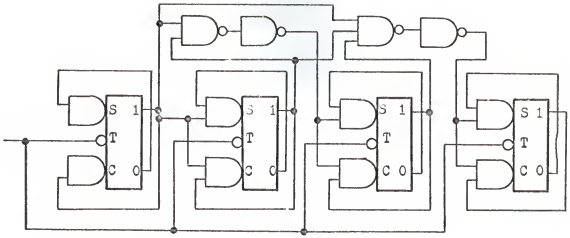


Fig. 4-3

The fan-in requirement of each successive gate increases by one and the outputs of the less significant stages are gradually consumed as the stage of flip-flops increases. In large parallel counters, fan-in extender elements may be provided to meet the fan-in requirement and buffer driver elements may be needed to provide sufficient drive to the entire carry system.

Decade Counter[8]

Synchronous counters and ripple-carry counters of four stages have repetitive sixteen discrete steps (from 0 to 15 inclusive). In a decade counter, only ten steps are required and the other six steps must be eliminated. Which six of the sixteen must be eliminated is a question worthy to consider. If the last six steps are chosen, then the remaining ten steps maintain the 1-2-4-8 normal binary code.

The binary coded clocked decade counter can be implemented by flip-flops A,B,C and D representing 1,2,4 and 8 respectively. The sequence and its binary representation are shown in Fig. 4-4. Karnaugh maps and Boolean representations of S and C inputs to the flip flops found by sequential circuit

analysis are shown in Fig. 4-5. These Boolean functions are mechanized with a few integrated circuit gates and flip-flops (Fig. 4-6).

Sequence		Binary Representation	
Present State	Next State	ABCD	ABCD
0	1	0000	1000
1	2	1000	0100
2	3	0100	1100
3	4	1100	0010
4	5	0010	1010
5	6	1010	0110
6	7	0110	1110
7	8	1110	0001
8	9	0001	1001
9	0	1001	0000

Fig. 4-4

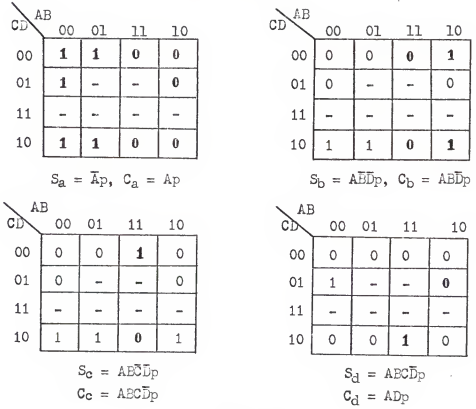


Fig. 4-5

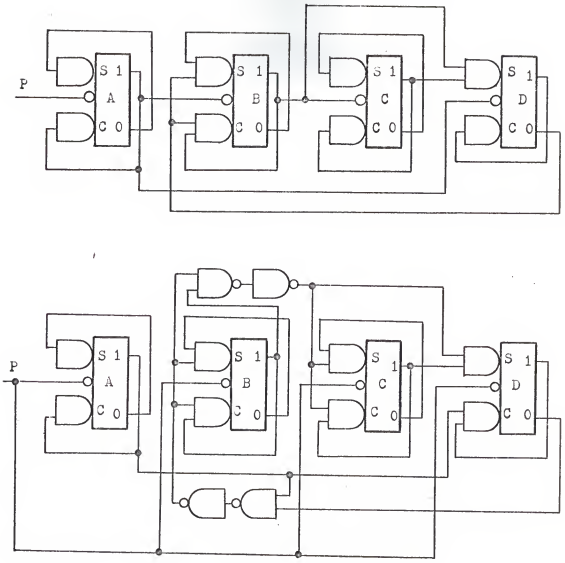


Fig. 4-6

The Karnaugh map in Fig. 4-7 shows the counting sequence of the decade counter. Decoding expressions of the ten discrete states can be found from the Karnaugh map. The decoding requires one 4-input double gate element, two 3-input triple gate elements, one 2-input quad gate element and two 1-input hex gate elements to implement the circuit as shown in Fig. 4-7.

In large counters, where many fan-in extender and buffer drivers must be used, a compromise between speed and cost can be reached by arranging stages

in groups. Intragroup carry may then be parallel without exceeding fan-out capabilities while intergroup is serial. For example a modulo 100 counter with display can be implemented by two decade counters with the tenth step of the Units counter used as the input pulse to the Tens counter as shown in Fig. 4-8.

CD \ AB	00	01	11	10
00	0	2	3	1
01	8	-	-	9
11	-	-	-	-
10	4	6	7	5

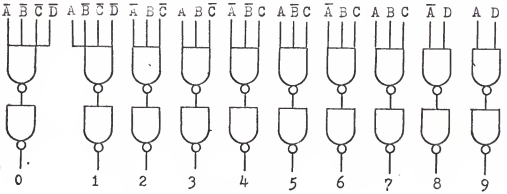


Fig. 4-7

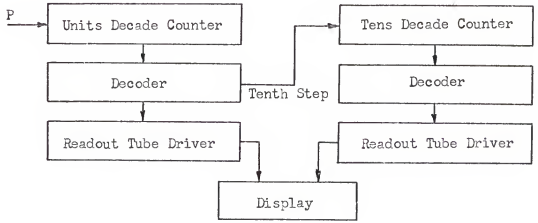


Fig. 4-8

Binary Full Adder[7]

The classical binary adder is formed with two half adders for economical reasons. Such a method, though inherently slower, reduces the number of circuit components by a considerable amount. By using integrated circuit elements and by utilization of the wired OR capabilities of the DTL's, the arrangement shown in Fig. 4-10 satisfies both economy and reasonable speed. A full adder has three inputs A, B and C which are the augend bit, addend bit and input carry bit respectively. The two outputs S and T are the sum bit and the output carry bit respectively. The operation of the full adder is shown in Fig. 4-9.

A	B	C	T	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Fig. 4-9

The Boolean expressions for S and T were found to be

$$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$T = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

By mathematical manipulation S and T can be expressed in the following form suitable for wired OR implementation.

$$S = \overline{\overline{\bar{A}B + A\bar{B} \cdot C} \cdot \overline{\bar{A}B + A\bar{B}} \cdot \overline{\bar{A}B + A\bar{B} \cdot C} \cdot C}$$

$$T = \overline{\bar{A}B \cdot \overline{\bar{A}B + A\bar{B}} \cdot C}$$

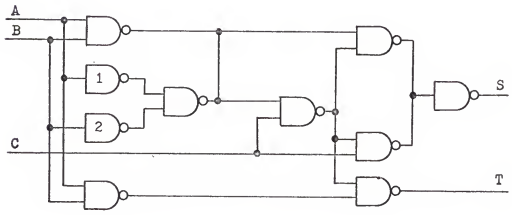


Fig. 4-10

The adder requires only $2\frac{1}{2}$ quad two-input integrated circuit elements. And if $\bar{A}$ and $\bar{B}$ are available through other sources without generating them in this circuit, as is always the case, gates 1 and 2 can be eliminated.

Shift Register[7]

A shift register is a group of flip-flops serially connected to perform the temporary storage of information. It is mostly used in binary multiplication and division. The shift register can be made to shift the information stored in the register one position to the right or to the left with each

clock pulse. In the shift right register, flip-flop outputs $\bar{Q}$ and Q are connected directly into the input gates of the next flip-flop as shown in Fig. 4-11. With each positive going clock pulse, the information available at

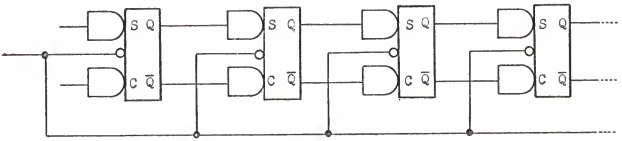


Fig. 4-11

its S, C inputs will be shifted into that flip-flop and stored there until the next clock pulse comes. For the shift left register, Q and $\bar{Q}$ are connected back to inputs gates of the previous flip-flops. In the practical case, a shift register can be made to shift right or left, as shown in Fig. 4-12. The

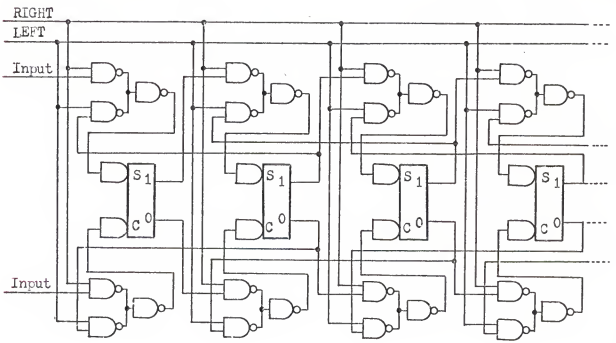


Fig. 4-12

control signals Shift Right and Shift Left must be mutually exclusive. If both are positive the register will malfunction; if both are grounded at the same time, the register will be disabled.

CONCLUSIONS

Although digital integrated circuits are versatile, space-saving and cost-reducing, they function only at very low voltages and small currents. For applications in higher power outputs and large voltage swings, discrete circuits or other means must be employed. Built-in inductors are not possible in monolithic integrated circuits. Discrete passive components are always used when the value of the passive components is critical.

ACKNOWLEDGEMENT

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SOME APPLICATIONS OF MICROELECTRONIC DEVICES IN DATA ACQUISITION AND PROCESSING

by

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AN ABSTRACT OF A MASTER'S REPORT

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requirements for the degree

MASTER OF SCIENCE

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KANSAS STATE UNIVERSITY
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1968

ABSTRACT

Miniaturization of active electronic devices has been the subject of intensive research and development efforts following the invention of the transistor. These efforts have been intensified during the past few years in an attempt to produce hardware that minimizes volume and weight requirements in deep space probes. Military requirements have also contributed to this activity.

Integrated logic circuit miniaturization has usually preceeded linear integrated circuit development. This report is concerned with certain aspects of digital integrated circuit construction and design. Features and limitations such as built-in gates and fan-out capabilities are considered briefly. Four groups of integrated circuits, i.e., RTL ECTL, DTL and TTL are discussed. Some applications of integrated circuits are presented in this report.