MITIGATING OSCILLATOR PULLING DUE TO MAGNETIC COUPLING IN MONOLITHIC MIXED-SIGNAL RADIO-FREQUENCY INTEGRATED CIRCUITS

by

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Abstract

An analysis of frequency pulling in a varactor-tuned LC VCO under coupling from an on-chip PA is presented. The large-signal behavior of the VCO's inversion-mode MOS varactors is outlined, and the susceptibility of the VCO to frequency pulling from PA aggressor signals with various modulation schemes is discussed. We show that if the aggressor signal is aperiodic, band-limited, or amplitude-modulated, the varactor-tuned LC VCO will experience frequency pulling due to time-modulation of the varactor capacitance. However, if the aggressor signal has constant-envelope phase modulation, VCO pulling can be eliminated, even in the presence of coupling, through careful choice of VCO frequency and divider ratio. Additional mitigation strategies, including new inductor topologies and system-level architectural choices, are also examined.

The analysis is then applied to improve a fully-integrated half-duplex UHF microtransceiver in which signal coupling between the LO and PA caused frequency pulling that prevented the use of QPSK signaling at certain data rates. We determine that a VCO operating at 4× transmit frequency will be naturally insensitive to pulling from QPSK signals. To validate the proposed solution, a prototype IC containing a pair of QPSK transmitters with integrated 100 mW Class-C PAs was designed and fabricated in 0.18um SOI. The transmitters—one utilizing a 2× VCO, one utilizing a 4× VCO—were designed to closely match the performance of the original microtransceiver when transmitting QPSK data. The transmitter with the 2× VCO experienced frequency pulling from the PA while transmitting QPSK data, but the transmitter with the 4× VCO did not, thereby confirming the analysis in this work.

A revision of the microtransceiver was designed in 0.5 μm SOS utilizing an off-chip PA inductor to reduce signal coupling with the VCO. A second revision of the microtransceiver with two prototype transmitters was designed in 0.25 μm SOS utilizing 4× VCOs and figure-8 VCO inductors for maximum insensitivity to pulling from QPSK and band-limited modulation, as well as other design improvements that leverage the higher f_t of the smaller process. Both revisions also include a hardware FSK modulator, a new charge pump, and a redesigned fractional-N synthesizer to attenuate a divided-reference spur in the IF output. These revisions of the radio will enable future researchers to focus on system-level applications where highly-integrated medium-power transceivers with fully-functioning IQ modulation are needed.

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Chapter 1

Introduction

This thesis investigates a problem where signal coupling in a fully-integrated ultra-high-frequency (UHF) microtransceiver caused pulling of its local oscillator (LO), preventing the use of quadrature phase-shift-keying (QPSK) signaling at certain data rates. To identify the source of this problem, all major on-chip coupling mechanisms—substrate, electric field, and magnetic coupling—were considered, as well as ground bounce and power supply ripple caused by bondwire inductance.

Substrate and electric field (capacitive) coupling can be easily mitigated using techniques and features available in most modern IC processes. These mechanisms, although present in the microtransceiver to some degree, were found to be well-addressed in the original design. Magnetic coupling, however, is difficult to mitigate because magnetic shielding techniques consume valuable layout area and significantly reduce the Q of integrated inductors. While magnetic coupling was also considered during the original design, it was ultimately found to be the cause of frequency pulling. A system-level architectural solution, rather than a shielding strategy, became the primary focus of this research.

1.1 Problem Overview

The microtransceiver IC which formed the focus of this research is part of a fully-integrated half-duplex radio prototyped in 2006 [1]. The K-State Microtransceiver radio-frequency integrated circuit (RFIC), shown in Figure 1.1, operates in the 390–450 MHz range and is intended to transmit data with binary phase-shift keying (BPSK), $\pi/2$ residual-carrier BPSK (RC-BPSK), QPSK, and frequency-shift keying (FSK) modulation, with a total power consumption of 50 mW on receive and 100 mW or 300 mW on transmit for 10 mW or 100 mW output power settings. The micro-

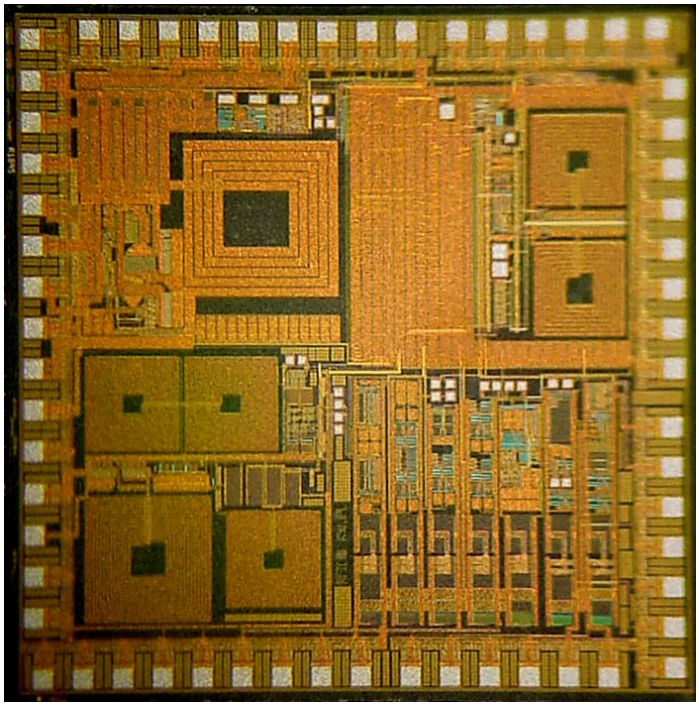


Figure 1.1: *Photograph of the K-State Microtransceiver.*

transceiver was designed to be used in a two-chip or three-chip system consisting of the transceiver RFIC, an FPGA operating as a digital modem, and an optional 1 W CMOS power amplifier [2] for higher-power applications. Both the Microtransceiver and the 1 W PA were fabricated in the 0.5 μm version of Peregrine Semiconductor's silicon-on-sapphire (SOS) UltraCMOS process. The high substrate resistivity and high f_t of SOS enables integration of the oscillator, transmitter, receiver, and embedded LC passives on a single 3.2×3.2 mm die. The only external components required are a temperature-compensated crystal oscillator (TCXO), a 10.7 MHz ceramic filter, and surface-mount passives for power supply decoupling.

The K-State Microtransceiver has been used as a radio link in many applications, including UHF propagation studies [3], energy-harvesting research [4], and a prototype body-area network for space suit biomedical sensing [5]. While this radio has been used with both BPSK and FSK modulation in these applications, it was found to experience frequency pulling and constellation smearing when transmitting QPSK with the 100 mW PA active. At data rates greater than 1 kbps, pulling is so severe that the transmitted data could not be demodulated. Previous attempts to identify the cause of the QPSK pulling problem were unsuccessful, and the transceiver was constrained to BPSK and FSK operation. This research began in response to renewed interest in restoring the Microtransceiver's QPSK and related RC-BPSK capabilities

as part of a NASA/EPSCoR-funded technology-development effort.

1.2 Literature Review

The phenomenon of local oscillator (LO) pulling by feedback from a PA in direct-conversion and superheterodyne transceiver architectures is widely recognized, as are the dominant coupling mechanisms in integrated circuits [6]. However, the literature contains little information on the precise mechanisms involved in the pulling problem. Bronckers et. al. [7] conducted an investigation of coupling mechanisms between a VCO and a PA in 0.13 μm CMOS, but LO pulling is only briefly mentioned, and modulated PA output signals are not considered. While [7] successfully identifies substrate and magnetic coupling as the dominant PA-VCO coupling mechanisms in bulk CMOS, they fail to draw conclusions beyond those already addressed in previous K-State research [1, 8] regarding effective isolation strategies. Physical separation of the LO and PA is consistently cited as the most effective coupling mitigation strategy. However, the maximum achievable separation of the LO and PA in fully-integrated transceivers is fundamentally limited by the available die area and the size of integrated passives.

The relationship between VCO operating frequency and PA output transmit frequency is also considered in the literature. Many published integrated transceiver designs use LO signals at half the desired frequency [9, 10], twice the desired frequency [11], or fractional thirds [12] to reduce LO pulling by the PA driver and other in-band interferers. Transceiver designs with LO frequencies higher than the transmit frequency are more prevalent because generating I and Q signals through frequency division also provides high I/Q phase accuracy [13]. This method is applied in the existing K-State Microtransceiver for both reasons. Other transceivers employ a direct-upconversion architecture, again for the stated reasons of preventing VCO pulling and reducing in-band spurs [14, 15, 16].

Operating the LO outside the band of interest prevents direct injection-locking of the LO by the PA. However, a frequency and phase relationship still exists between the LO and PA output frequencies in transceivers where I and Q are generated through frequency multiplication or division. The choice of LO frequency and divider ratio appears to be dictated by the preferred method of generating I and Q, not by efforts to mitigate pulling. Direct-upconversion transceiver architectures often provide high levels of integration with low power consumption [15], but require additional filtering to attenuate unwanted sidebands. There is no discussion in this prior art as to the

effectiveness of frequency multiplication, division, or up-conversion at mitigating LO pulling from the PA.

Another widely-published LO pulling mitigation strategy targeted at non-constant envelope modulation schemes (QAM, CDMA, etc.) advocates the use of digital pre-distortion (DPD) networks to reject LO pulling while simultaneously linearizing the PA [17, 18, 19]. These methods are effective at mitigating LO self-injection and spectral regrowth in the transmitted signal, but do not address LO pulling due to PA output modulation. Additionally, this strategy is targeted at transceivers that already employ a pre-distortion network to linearize the PA. Constant-envelope modulation schemes, such as unfiltered BPSK, QPSK, and FSK, do not require linear power amplifiers. Hence, due to its complexity, implementing a pre-distortion network in transceivers with constant-envelope modulation schemes solely to mitigate LO pulling is not a desirable solution.

Review of this prior art showed no publications making a clear connection between LO pulling, LO operating frequency, PA output frequency, and modulation in fully-integrated transceivers. This thesis demonstrates that it is possible to design a robust fully-integrated transceiver, even in the presence of unavoidable coupling, by identifying potential on-chip coupling mechanisms and tailoring the transceiver architecture to be naturally insensitive to them.

1.3 Thesis Outline

Chapter 2 presents a brief overview of coupling mechanisms and mitigation strategies in modern IC processes. The fundamental limits on the performance of integrated passives—substrate resistivity and metal resistance—are also discussed, as well as issues surrounding on-chip magnetic shielding. We show how magnetic shielding techniques, if attempted, are generally undesirable because they can significantly degrade the Q of integrated inductors. Finally, system-level issues such as power supply crosstalk and ground bounce are briefly addressed.

Chapter 3 identifies two magnetic coupling paths between the 100 mW PA and the VCO in the K-State Microtransceiver. When the 100 mW PA is operating, the PA output is magnetically coupled into the VCO inductors from both the 100 mW PA inductor and the inductor in an integrated resonant T/R switch. Simulations of the microtransceiver transmitting QPSK under coupling from both aggressors closely match the transceiver's measured performance. A potential capacitive coupling path between the PA and VCO through a top-metal ground shield is also investigated and

found not to be a strong contributor to the pulling problem.

Chapter 4 reviews the theory and operation of the varactor-tuned LC VCO in the K-State Microtransceiver, and presents a detailed analysis of the large-signal operation of inversion-mode MOS varactors used for analog frequency tuning. MOS varactors have steep C-V curves and high on/off capacitance ratios, suggesting a similar VCO frequency tuning characteristic. However, due to the large-signal output swing of the VCO, the effective capacitance seen by the LC tank is a time-averaged function of the varactor C-V curve. This averaging produces a smooth, linear VCO tuning characteristic. Chapter 4 shows that the relationship between varactor capacitance and LC tank voltage implies that signals coupled into the LC tank will time-modulate this varactor capacitance and pull the VCO.

Having established a foundation for the discussion of chip-level coupling in Chapters 2 and 4, Chapter 5 presents a time-domain analysis of frequency pulling in a varactor-tuned LC VCO from an on-chip PA, focusing on the susceptibility of the VCO to pulling from aggressor signals with different modulation schemes. If the aggressor signal is band-limited and/or amplitude-modulated, a varactor-tuned LC VCO will experience frequency pulling due to time-modulation of the varactor capacitance by the aggressor signal. However, if the aggressor signal has constant-envelope phase modulation, VCO pulling can be eliminated, even in the presence of coupling, through careful choice of the VCO frequency and VCO divider ratio.

Chapter 6 presents pulling mitigation strategies for integrated transceivers based on the results in Chapter 5. These strategies are targeted at transceiver designers in the first stages of system architecture planning. In particular, Chapter 6 showcases a new figure-8 inductor topology [20] that is immune to coupling from external B-fields. Simulations of the inductor in the K-State Microtransceiver demonstrate that the figure-8 topology can provide greater than 40 dB of additional isolation between the PA and VCO compared to traditional inductor topologies. Because it is not always possible to fabricate custom inductors, Chapter 6 discusses other mitigation strategies, such as choice of VCO frequency, VCO divider ratio, modulation scheme, and PA topology to design a fully-integrated transceiver that is naturally insensitive to pulling.

Chapter 7 describes the design and performance of a pair of QPSK transmitters fabricated in 0.18 μm SOI to test a potential pulling mitigation strategy for the K-State Microtransceiver. Based on the analysis in Chapter 2, it was concluded that a VCO operating at 4$\times$ the transmit frequency would be naturally insensitive to pulling from BPSK and QPSK-modulated carrier waves. The pair of transmitters de-

signed in this research—one utilizing a 2× VCO, one utilizing a 4× VCO—consisted of a differential LC VCO, an integer-N synthesizer, an IQ modulator, and 10 mW and 100 mW power amplifiers, and were designed to closely match the performance of the K-State Microtransceiver when transmitting QPSK data. Testing confirmed that the transmitter with the 2× VCO experienced frequency pulling when transmitting QPSK, but the transmitter with the 4× VCO did not, thereby confirming the assessment in Chapter 3.

Having confirmed the effectiveness of pulling mitigation strategies presented in Chapter 7 and having proposed a solution to enable even non-constant envelope modulation in Chapter 6, Chapter 8 describes two revisions of the K-State Microtransceiver that were designed as part of an independent study by the author. One revision of the microtransceiver was designed utilizing an off-chip PA inductor to reduce signal coupling with the VCO. In addition, a second revision containing two prototype microtransceiver transmitters with 4× VCOs and figure-8 inductors is being designed in 0.25 μm SOS to validate the effectiveness of the figure-8 inductor topology at eliminating frequency pulling from band-limited modulation. Other critical circuits, such as frequency dividers, are being redesigned to take advantage of the higher f_t of the smaller process. The prototype transmitters are targeted for fabrication in early 2015. Both revisions of the microtransceiver also include an improved charge pump, a hardware FSK modulator with a dedicated FSK data pin, and six years' worth of miscellaneous bug fixes and improvements. The microtransceiver's fractional-N synthesizer was also redesigned to mitigate a capacitive coupling path between the synthesizer ground shield and the receiver responsible for the appearance of a 4.8 MHz divided reference spur in the IF output. Finally, Chapter 9 concludes the thesis with a summary of results and future work.

Chapter 2

Coupling Mechanisms in Integrated Circuits

In this chapter, the three dominant coupling mechanisms in modern IC processes—substrate, electric field, and magnetic coupling—are examined, and mitigation strategies for each mechanism are discussed. Two process technologies in particular are singled out for examination. The K-State Microtransceiver is designed in a 0.5 μm silicon-on-sapphire (SOS) IC process, while another IC fabricated in the course of this research is fabricated in a 0.18 μm thick-film silicon-on-insulator (SOI) process. This chapter presents research that demonstrates that both processes can provide comparable substrate and electric field coupling isolation at high frequencies. However, both processes are equally susceptible to magnetic coupling, a direct result of the flux linkage between integrated inductors. This allows magnetic coupling mitigation strategies to be investigated in either process technology and applied to both with identical results. System-level coupling mechanisms, such as crosstalk, power supply ripple, and ground bounce, are also identified and discussed.

2.1 Substrate Coupling in Bulk CMOS

Before discussing substrate coupling in SOI, it is beneficial to briefly consider substrate coupling in bulk CMOS. A typical bulk CMOS process, shown in Figure 2.1, consists of a highly-doped silicon substrate between 600 um and 900 um thick, with a moderately to lightly-doped epitaxial layer (epi layer) between 0.5 um and 4 um thick to provide latch-up immunity [21]. Bulk CMOS processes have been extensively studied and modeled, and are favored for their high availability and low cost. However, bulk CMOS provides poor inductor performance and poor circuit isolation, both at

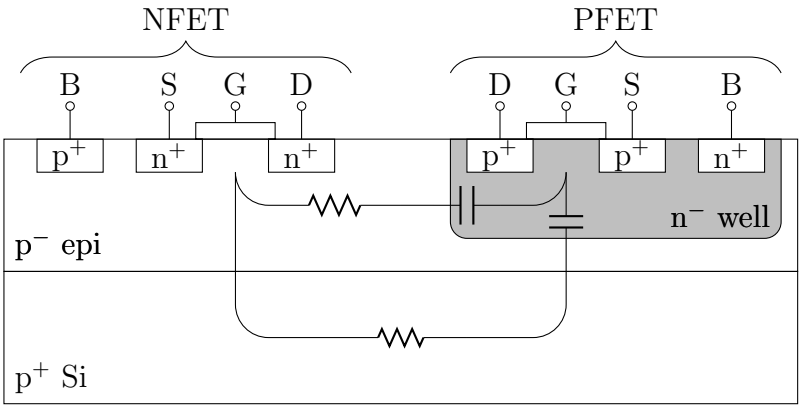


Figure 2.1: *Cross-section of a typical bulk CMOS process showing substrate coupling paths.*

DC and at high frequencies, because devices have direct DC coupling paths through both the substrate and the low-resistivity epi layer.

In bulk CMOS, selective oxide growth methods such as local oxidation of silicon (LOCOS) and shallow-trench isolation (STI) are utilized to block the DC epi layer coupling path between devices [21] and provide additional latch-up immunity [22]. Other techniques, such as surrounding sensitive circuits with grounded substrate contacts and deep-well guard rings [23] and following line-of-diffusion and standard-cell layout conventions [21], help capture and shunt stray epi-layer noise to ground, providing an additional measure of isolation. However, while these techniques are effective at mitigating coupling through the epi layer, they are ineffective at mitigating coupling through the heavily-doped Si substrate. Signals which reach the low-resistivity substrate can travel long distances, allowing them to couple into circuits far away from the source.

2.2 Substrate Coupling in SOI

Silicon-on-insulator IC technologies were developed to address the poor isolation, low speed, and high power consumption of bulk CMOS. These processes also allow high-performance inductors to be constructed, and are therefore generally preferred for RF work. In SOI, an epitaxial film of single-crystalline Si is separated from the substrate by an insulating layer of SiO_2. Compared to bulk CMOS, SOI technology allows for the fabrication of smaller devices with simpler, more effective isolation structures [24], lower parasitic substrate capacitance, higher f_t, and reduced short-channel effects [25], and provides a 30-40% reduction in power consumption [26]. Some forms of SOI technology are also inherently immune to latch-up, and high-resistivity substrates, if

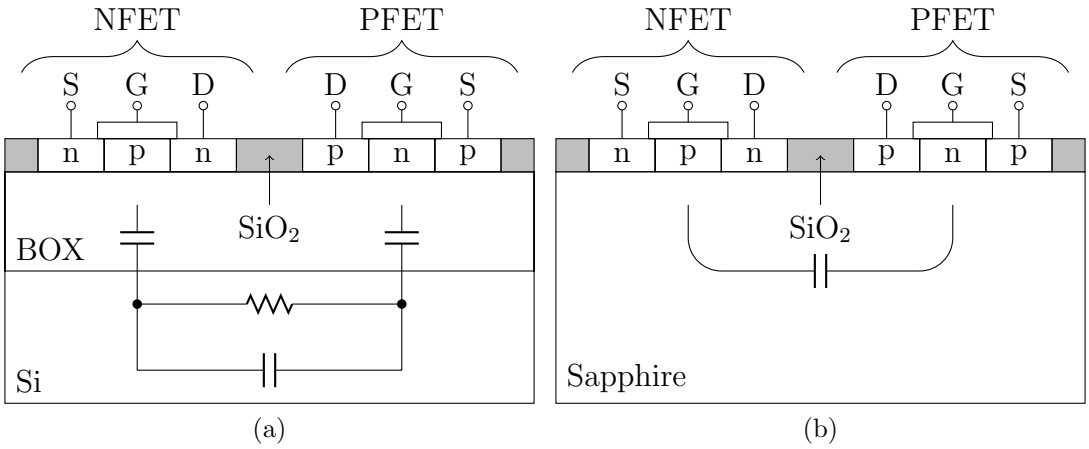


Figure 2.2: *Substrate coupling paths in thin-film SOI processes. (a) SOI on buried oxide. (b) Silicon-on-sapphire.*

used, eliminate the need for wells and buried doped layers. SOI technologies can be grouped into two categories—thin-film or thick-film—based on the thickness of the epi layer.

2.2.1 Thin-Film SOI

In thin-film SOI, a thin layer of epitaxial silicon—between 10 nm and 1000 nm thick—is grown on an insulating substrate, such as SiO_2 or sapphire. Both process technologies are illustrated in Figure 2.2. Thin-film SOI is also referred to as fully-depleted SOI (FD-SOI) to emphasize that the channel region of a thin-film MOSFET extends from the gate oxide to the insulating layer. As a result, devices fabricated in thin-film SOI suffer from floating-body and kink effects [27].

Because the epi layer is so thin, it can be oxidized or etched away. This restricts substrate coupling in thin-film SOI to capacitive mechanisms through the high-resistivity substrate. The high-resistivity substrate also allows IC designers to fabricate high-Q integrated passives. Q values greater than 30 have been reported for integrated inductors fabricated in SOS, compared to typical achievable Q values of 3-12 in bulk CMOS [28]. The K-State Microtransceiver was originally designed in 0.5 μm SOS for this reason.

2.2.2 Thick-Film SOI

In thick-film SOI, shown in Figure 2.3, a thicker layer of epitaxial silicon—approximately 1 μm thick—is separated from a Si substrate by a layer of buried oxide. Unlike thin-

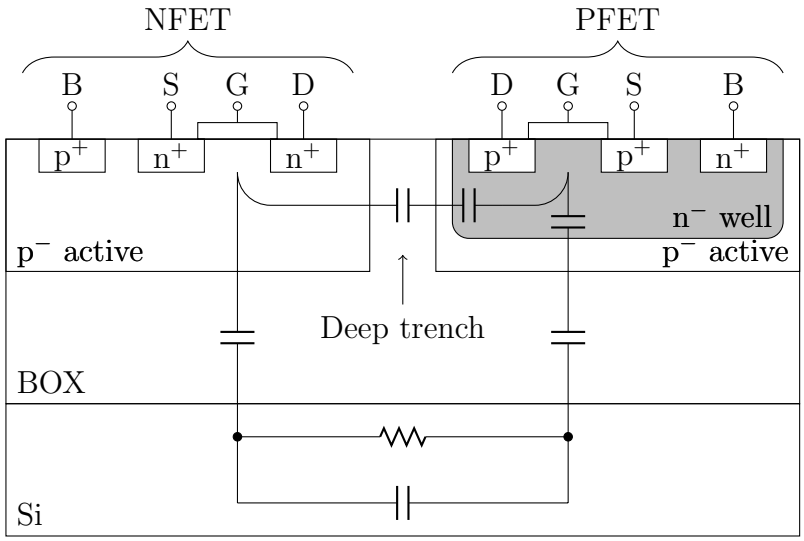


Figure 2.3: *Substrate coupling paths in a typical thick-film SOI process.*

film SOI, the height of the silicon film in which thick-film devices are fabricated is larger than the height of the devices' depletion regions. As a result, thick-film SOI technology is referred to as partially-depleted SOI (PD-SOI), and necessitates the use of body contacts to prevent the floating-body effect.

Previous K-State research [8] characterized substrate coupling in a commercial 0.18 μm thick-film SOI process used to fabricate an IC designed in the course of this research and measured the effectiveness of different substrate coupling mitigation techniques, including increasing the physical separation between active devices, isolating circuits with deep-trenches, blocking channel-stopper implant used to prevent surface inversion to increase the resistivity of the epi layer, and isolating circuits with grounded NTAP guard rings to absorb substrate currents. Of these strategies, a combination of deep-trench wells and substrate-contact guard rings was found to produce the best isolation, resulting in a 40 dB-per-decade increase in isolation at high frequencies [8].

2.3 Electric Field Coupling Between Interconnects

Another dominant on-chip coupling mechanism is capacitive coupling caused by fringing electric fields between metal interconnects. Capacitive coupling paths can form between metal device interconnects, adjacent traces on routing layers, and through floating fill metal, as illustrated in Figure 2.4, and between adjacent bondwire pads.

Metal-to-metal coupling was extensively studied and simulated in [8]. To a first

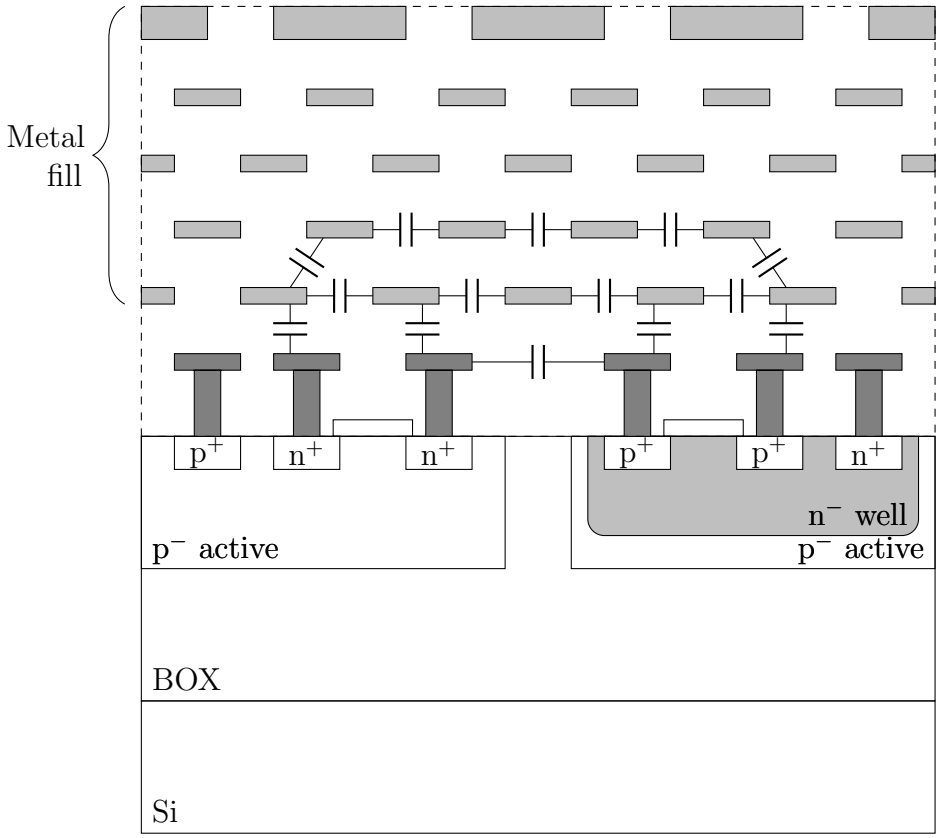


Figure 2.4: *Capacitive coupling paths in a six-metal-layer thick-film SOI process.*

order, the capacitance between two overlapping metals in a uniform dielectric can be approximated as a parallel-plate capacitor

$$C = \frac{A\epsilon_0\epsilon_r}{h} \tag{2.1}$$

where A is the overlapping area, ϵ_r is relative the dielectric constant of the oxide, and d is the inter-metal dielectric (IMD) thickness. The fringing-field capacitance between two adjacent metal interconnects, such as device contacts or parallel traces, may be approximated by modeling the adjacent metals as parallel coplanar strips in a multilayer dielectric and applying the closed-form formulas presented in [8] and [29]. It is left to an exercises to the reader to solve for the fringing-field capacitance between two parallel metals. However, both Equation 2.1 and [29] show that fringing-field capacitance decreases as the separation between metal objects increases. It is important to note that the capacitance between two parallel metal interconnects is largely dependent on the separation between the two traces, not the trace width, because the primary fringing field interaction occurs between the near edges of the traces [8].

2.3.1 Metal Fill

Another potential metal-to-metal coupling path in ICs is through metal fill. Dummy metal fill patterns, shown in Figure 2.5, are generated in empty areas of the die to reduce variations in interlayer dielectric thickness and prevent the accidental partial removal of metal layers during chemical-mechanical polishing (CMP), which is used to planarize inter-metal dielectric (IMD) oxide layers.

As illustrated in Figure 2.4, capacitive coupling between floating metal fill shapes could allow high-frequency signals to couple between metal interconnects and active devices. However, research has shown that there is no significant change in coupling between active devices when fill metal is blocked because the high-frequency capacitive coupling path through the insulating substrate has a much lower impedance than the series-connected fringing-field capacitances of a chain of metal fill shapes [8]. Blocking fill metal above metal interconnects was only found to provide a 1 dB increase in metal-to-metal isolation.

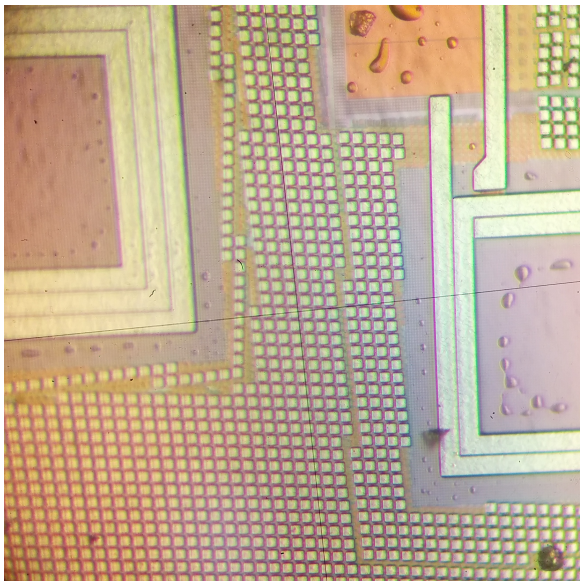


Figure 2.5: *Example of floating fill metal patterns in a six-metal 0.18 μm SOI process.*

2.3.2 Electric Field Coupling Mitigation Strategies

To a first order, capacitive coupling between metal interconnects in ICs can be modeled using well-known capacitance equations. Since interconnects to active devices are generated by the process toolkit, metal-to-metal coupling between the drain, gate and source interconnects of a MOSFET is unavoidable to some degree. Such parasitic capacitances become part of the model of the active device. In general, however, capacitive coupling can be mitigated in both thick-film and thin-film SOI by increasing the vertical and horizontal separation between adjacent metal interconnects leading to the device, and by avoiding closely-spaced parallel metal runs.

Coupling between bondwire pads on an IC should also be addressed. In thick-film SOI, a combination of substrate and capacitive coupling mitigation techniques can be used to increase pad-to-pad isolation, including increasing the pad pitch, surrounding the pads with grounded substrate-contact guard rings to trap stray epi-layer noise currents, and inserting deep-trench grids beneath the pads to reduce pad-to-pad coupling through the substrate [8].

2.4 Magnetic Field Coupling

Before discussing magnetic coupling, it is important to review mutual inductance. Figure 2.6 is a schematic diagram of two coupled inductors with reference dots denoting the polarity of the mutual inductance. The subscripts $L_{m,m}$ and $L_{n,n}$ are used

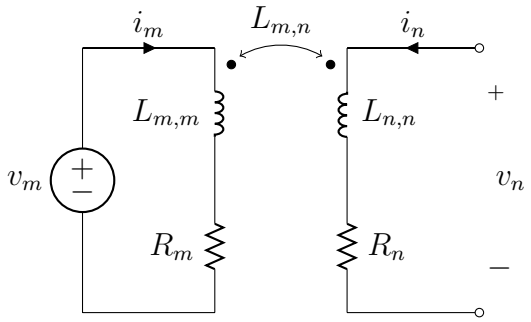


Figure 2.6: *Mutual inductance and the dot convention.*

to denote the self-inductance of each coil. To a first order, the planar spiral inductors fabricated in ICs can be treated as wire loops. The flux linkage between two coupled coils m and n is given by

$$L_{m,n} = \frac{N_n \Phi_{n,m}}{i_m} \tag{2.2}$$

where N is the number of turns in the inductor, Φ is the magnetic flux through inductor n generated by inductor m, and $L_{m,n}$ is the mutual inductance between the two inductors. It is important to note that the forward and reverse mutual inductances of two coupled coils are equal, and are given by

$$L_{m,n} = L_{n,m} = M = k\sqrt{L_{m,m}L_{n,n}} \tag{2.3}$$

where the coupling coefficient $0 \leq k \leq 1$ is the ratio of the total magnetic flux linking L_m and L_n to the total flux through both coils. A coupling coefficient of 1 therefore implies complete flux linkage between the two inductors. By Faraday's law of induction, the voltage induced in coil n due to flux from coil m is given by

$$v_{n,m}(t) = N_n \frac{d\Phi_n}{dt} = M\frac{di_m}{dt} \tag{2.4}$$

therefore, the total voltage across coil n, as shown in 2.6, can be expressed as

$$v_n(t) = L_{n,n}\frac{di_n}{dt} + i_n(t)R_n + M\frac{di_m}{dt} \tag{2.5}$$

where R_n is the equivalent series resistance of the lumped-element inductor model.

2.4.1 Magnetic Coupling Mitigation Strategies

Equations 2.2 and 2.4 suggest that magnetic coupling can be mitigated in two ways. First, the flux linkage between two inductors can be reduced by decreasing the number of turns in the inductor, or by physically shrinking the size of the inductor to decrease the amount of flux passing through it. Unfortunately, this is not always possible. Inductor dimensions and number of turns are usually set by the desired inductance, self-resonant frequency, and Q in a particular process. The flux linkage between two inductors can also be reduced by employing solid metal shields above or below sensitive inductors. The time-varying magnetic field creates eddy currents in the shield which flow in accordance with Lenz's law, creating magnetic fields that oppose the flux through the inductor. The net flux through the inductor is therefore decreased. Unfortunately, so too is the self-inductance, and hence the inductor Q. Simulations of a $300\times300\,\mu$m, 0.5 nH single-turn spiral inductor in $0.25\,\mu$m SOS [8] show that, in order to achieve a 20 dB reduction in magnetic coupling, a solid metal ground shield must be located 1-2 μm above the inductor and produces a 90% decrease in effective inductance. The parasitic capacitance between the ground shield and inductor windings also significantly reduces the inductor's self resonant frequency. Ground shields are therefore undesirable for use in circuits requiring high-Q inductors.

If the designer is unable to change the dimensions of the inductors, magnetic coupling may be mitigated by reducing the mutual inductance M and coupling coefficient k using physical separation. As the two coupled inductors are separated, the amount of flux linking the two inductors decreases, and k converges to zero. In the far field, the value of the coupling coefficient is largely dependent on the separation of the inductors and not on the size or number of turns [8]. Increasing the physical separation between inductors is the most straightforward magnetic coupling mitigation strategy [30]. However, the maximum achievable inductor separation is limited both by the size of the inductors and the size of the die.

2.5 System-Level Coupling

Designers of integrated circuits occasionally forget that the devices they build are part of a larger system. While an in-depth study of system-level coupling mechanisms is outside the scope of this thesis, common-mode noise sources such as power supply ripple and ground bounce caused by bondwire inductance will be considered in Chapter 3 as potential LO pulling mechanisms.

The use of differential circuits and signaling is critical for power-supply and common-mode noise immunity, especially in RF circuits. The K-State Microtransceiver is almost entirely differential to provide high common-mode rejection in addition to simplified circuit layout and higher voltage swings. Active supply filters are also implemented in sensitive circuits, such as high-gain IF amplifiers, to prevent unwanted feedback and oscillation [1]. In addition to employing differential circuit topologies, power supply ripple and ground bounce can be mitigated by designing low-power circuits with small switching currents, operating at lower supply voltages, and reducing bondwire and package lead inductance by choosing smaller packages. Additional techniques commonly used include the separation of analog and digital power and ground pins and employing ground down-bonds to shorten the length of the bondwire, and allocating multiple power and ground pins for a single domain.

Many of these techniques were utilized to mitigate power supply ripple and ground bounce in the in the K-State Microtransceiver's 100 mW Class-C PA, which draws a peak switching current of 90 mA during normal operation. To reduce bondwire and package-lead inductance, the microtransceiver was packaged in a QFN with an exposed ground paddle, and the PA was allocated three power pins and four ground pins. Ground down-bonds to the exposed paddle reduce the inductance of each ground bondwire by half. In addition to 600 pF of on-chip decoupling, each PA power pin is decoupled at the board level by multiple ceramic and low-ESR tantalum capacitors.

2.6 Summary

Substrate and electric field (capacitive) coupling are present to some degree in all modern IC technologies. While thin-film SOI and SOS are much less susceptible to substrate coupling than thick-film SOI, [8] demonstrated that thick-film SOI can provide as much high-frequency substrate isolation as SOS through proper use of deep-trench surrounds, PTAP and NTAP guard rings, and selective blocking of any channel-stopper implant. Additionally, all ICs, regardless of process technology, are susceptible to capacitive coupling between metal interconnects, and to system-level coupling mechanisms such as power supply ripple and ground bounce. These can be easily mitigated through board-level and on-chip supply decoupling, on-chip supply filtering, reducing bondwire and lead inductance through the use of down-bonds and multiple power and ground pins, and by employing separate power and ground connections for separate subsystems and differential signaling on chip to reject common-mode disturbances when crossing power and ground domains.

Unfortunately, while substrate, electric field, and system-level coupling can be mitigated without dramatically impacting circuit performance, magnetic shielding techniques such as ground shields reduce magnetic flux and increase inductor parasitic capacitance, thereby reducing inductor Q. This is extremely undesirable in RF circuits. Increasing the physical separation between inductors decreases magnetic coupling without impacting Q, however, the maximum separation—and therefore the upper bound on achievable magnetic isolation—is set by the inductor dimensions and the available die size. In the case of the K-State Microtransceiver, which has seven integrated inductors on a $3.2 \times 3.2\,\text{mm}$ die, magnetic interaction is inevitable and must be mitigated in other ways.

Chapter 3

Frequency Pulling in the K-State Microtransceiver

A top-level block diagram of the K-State Microtransceiver is shown in Figure 3.1. The upper half consists of a direct-modulation transmitter capable of transmitting BPSK, $\pi/2$ RC-BPSK, QPSK, and FSK with externally-generated IQ waveforms. The VCO operates at twice the modulated output frequency and is divided down to generate differential quadrature outputs for IQ modulation. A 10-bit fractional-N synthesizer with 3rd-order Σ-Δ modulator operating from a 19.2 MHz off-chip reference oscillator allows the transmitter to achieve a tuning step size of 4.7 kHz. The microtransceiver can transmit using either a 10 mW exponential-horn pad driver or an integrated 100 mW class-C PA. The lower half is a classic superheterodyne receiver with an off-chip 10.7 MHz IF filter and a 1-bit oversampling ADC. An integrated T/R switch designed into the LNA allows the LNA to be directly connected to the PA output as shown in Figure 3.1. The combination of 10.7 MHz IF and oversampled ADC was selected over a direct-conversion architecture due to the requirement for the radio to process extremely low data rate BPSK and QPSK at sensitivities $\leq$ -120 dBm in an IC process where $1/f$ noise can extend into the MHz range [1].

3.1 Identification of the LO Pulling Mechanism

The microtransceiver's LO pulling problem had been investigated by various graduate researchers in the past; however, the results of their investigations were largely unsuccessful, and the specific LO pulling mechanism remained unidentified. The first step in identifying the LO pulling mechanism in this thesis was to extensively test the microtransceiver and attempt to replicate the problem. The microtransceiver

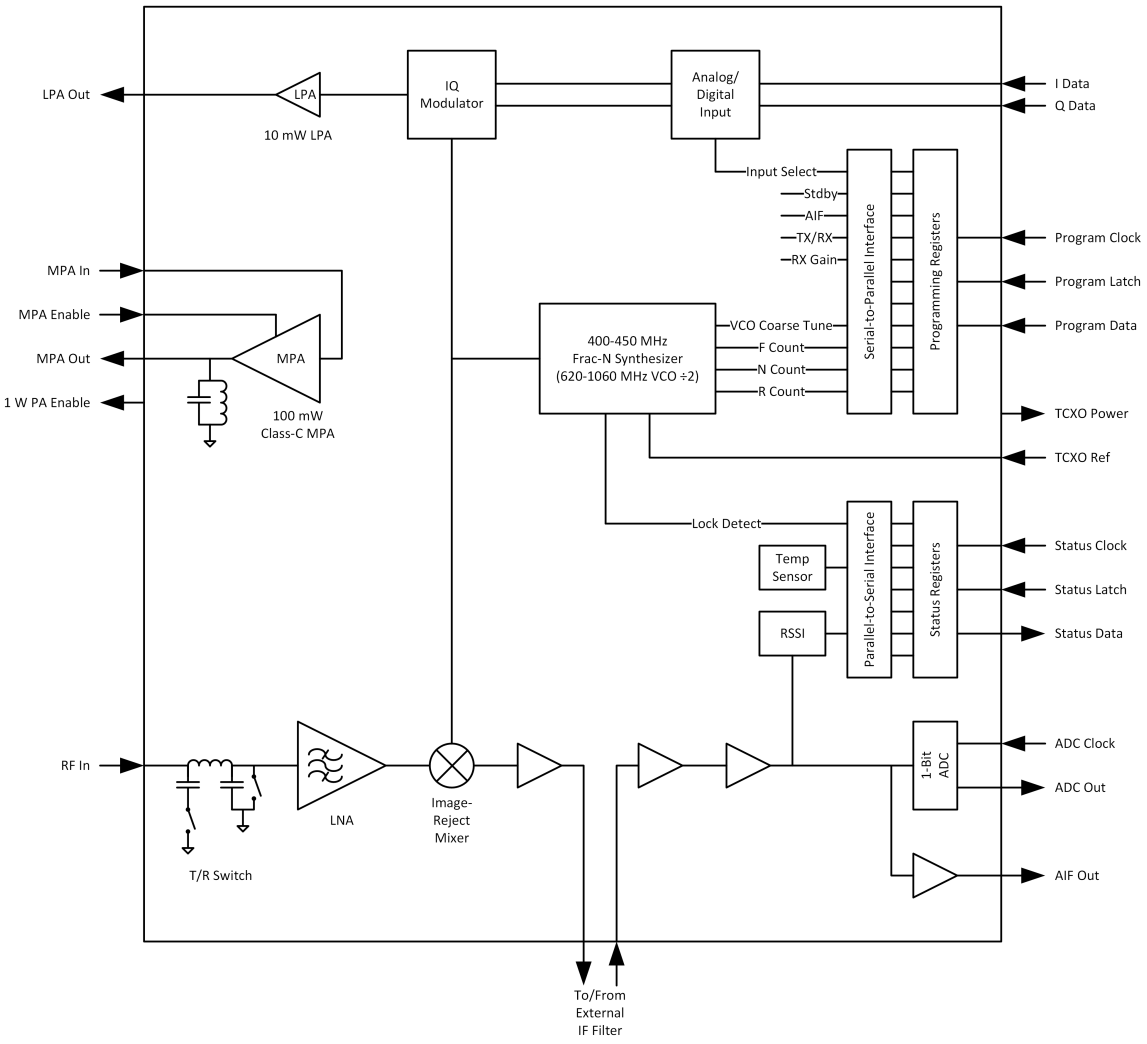


Figure 3.1: *Block diagram of the K-State Microtransceiver.*

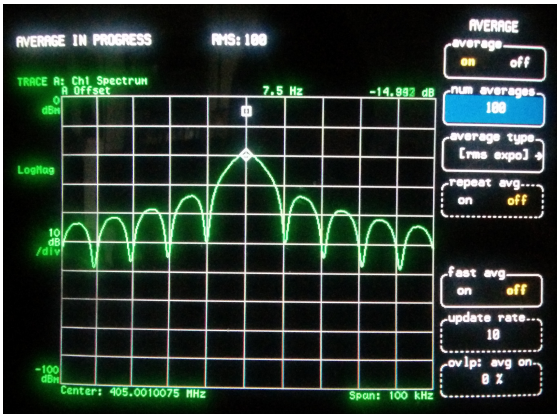
was operated in BPSK and QPSK mode at various data rates at 10 mW and 100 mW output power settings, and the radio's output spectrum and symbol constellation were examined on an HP89410A Vector Signal Analyzer in an attempt to determine which factors let to frequency pulling. An Agilent 33220A Function/Arbitrary Waveform Generator programmed with a 2^{64}-symbol PRBS sequence was used to generate pseudo-random I or Q data. Because an arbitrary waveform generator capable of synthesizing phase-coherent I and Q data waveforms was not accessible, $\pi/2$ residual-carrier BPSK (RC-BPSK) modulation was used to test the microtransceiver's QPSK performance. RC-BPSK is generated by fixing the value of either the in-phase or quadrature channel and transmitting data on the other, thereby using only two adjacent QPSK symbols, producing a QPSK spectrum with a large residual-carrier peak. Transmitting RC-BPSK is a simple way of exercising an IQ modulator in QPSK mode in the absence of a dual-data-stream PRBS generator.

Figure 3.2 compares the microtransceiver's BPSK and RC-BPSK (QPSK) performance transmitting 10 kbps data with the 10 mW low-power amplifier, an inductorless exponential-horn inverter pad driver. Similar tests revealed that the microtransceiver is able to transmit both BPSK and RC-BPSK (QPSK) successfully at data rates up to 1 Mbps. At data rates above 1 Mbps, both the BPSK and RC-BPSK output spectrums become lopsided, shown in Figure 3.3, due to asymmetrical prefiltering on the microtransceiver's data inputs.

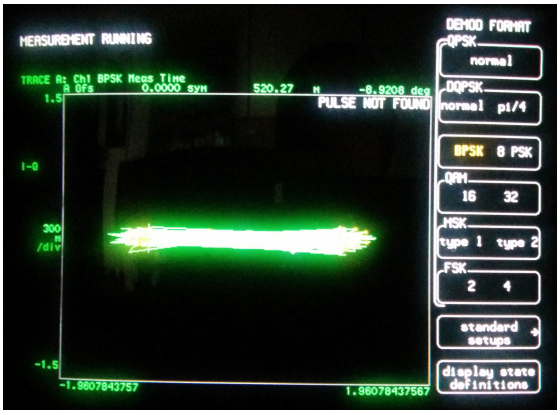
Figure 3.4 compares the BPSK and QPSK performance transmitting 10 kbps data with the 100 mW PA active. The radio's BPSK performance is not affected by the 100 mW PA. However, the QPSK spectrum (Figure 3.4c) was severely degraded, and symbols in the QPSK constellation (Figure 3.4d) are indicative of severe LO pulling. At 10 kbps, each QPSK symbol accumulated between $\pi/4$ and $\pi/2$ radians of phase error within one bit period, and at data rates greater than 10 kbps, pulling is so severe that the signal constellation cannot be demodulated. This strongly indicates that the 100 mW PA is the source of the LO pulling.

3.2 Magnetic Coupling

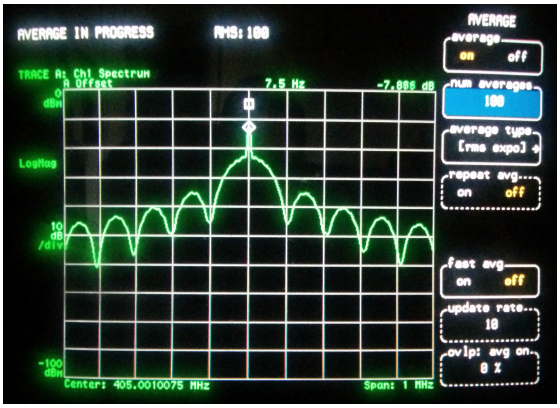
Having discovered that 100 mW PA was the apparent aggressor responsible for LO pulling, magnetic coupling between the PA and VCO inductors was suspected to be the dominant coupling mechanism. A design review identified two potential magnetic coupling paths between the PA and VCO. The 100 mW PA output can potentially couple directly into the VCO inductors from the inductor in the 100 mW PA, or from



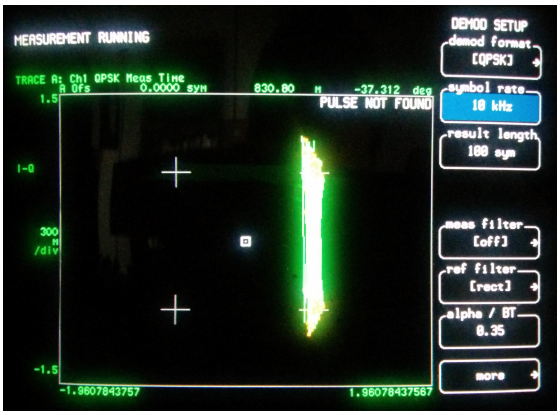
(a) *10 kbps BPSK spectrum.*



(b) *10 kbps BPSK constellation.*

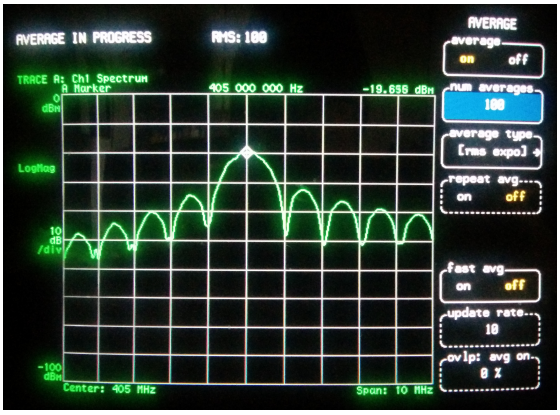


(c) *10 kbps RC-BPSK spectrum.*

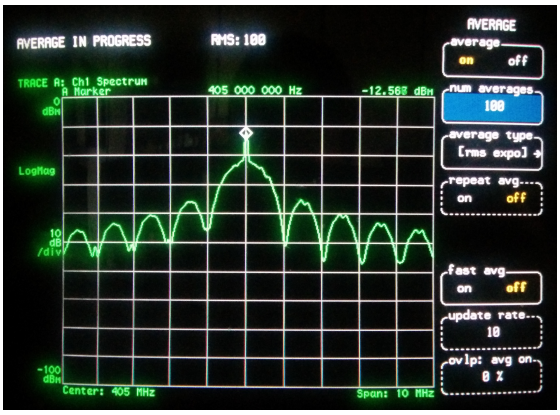


(d) *10 kbps RC-BPSK constellation.*

Figure 3.2: *Fab 5 BPSK and RC-BPSK performance at 10 kbps using the microtransceiver's inductorless 10 mW exponential-horn pad driver.*

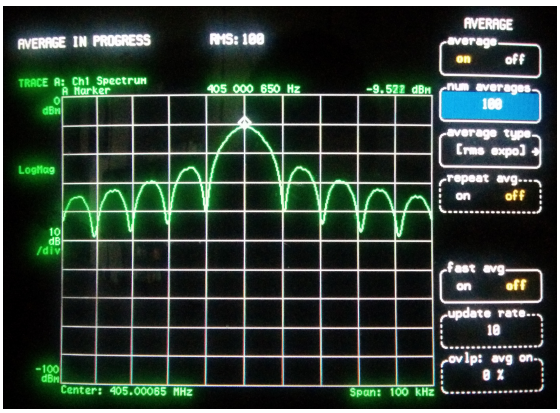


(a) *1 Mbps BPSK spectrum.*

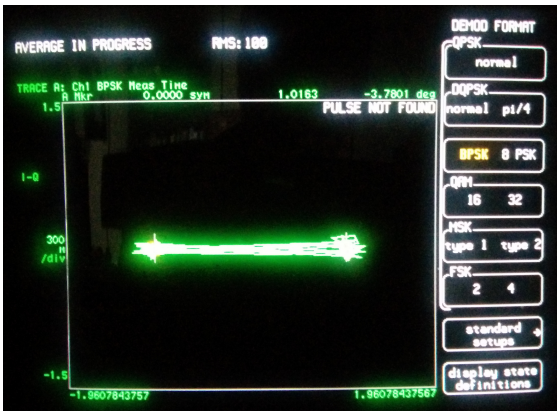


(b) *1 Mbps RC-BPSK spectrum.*

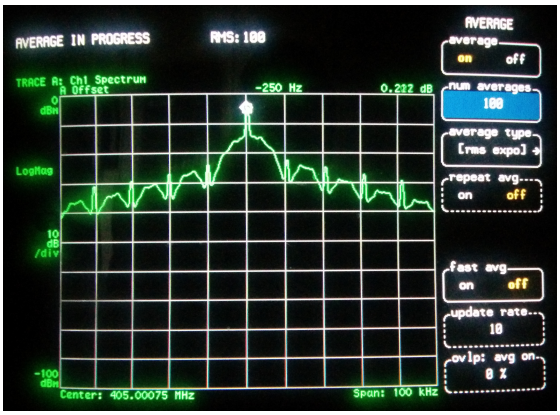
Figure 3.3: *Fab 5 BPSK and RC-BPSK spectrums at 1 Mbps. The lopsided spectrums are caused by asymmetrical prefiltering on the I and Q data inputs.*



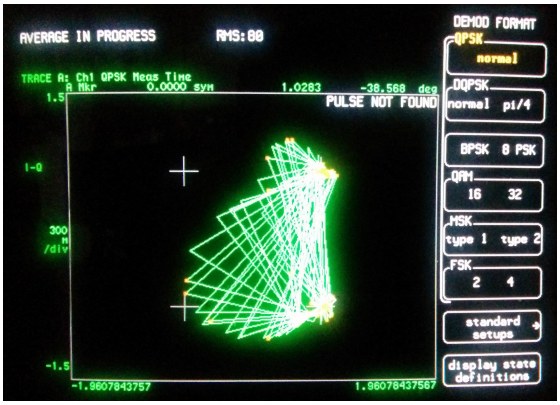
(a) 10 kbps BPSK spectrum.



(b) 10 kbps BPSK constellation.



(c) 10 kbps QPSK spectrum.



(d) 10 kbps QPSK constellation.

Figure 3.4: *Comparison of Fab 5 BPSK and QPSK performance transmitting 10 kbps data with the 100 mW PA active.*

Inductor	Designation	Design Value	Extracted Value
100 mW PA	a	16 nH	14.8 nH
T/R switch	b	80 nH	77.6 nH
VCO (top)	c	17.5 nH	17.2 nH
VCO (bottom)	d	17.5 nH	18.1 nH

Table 3.1: *Table of Fab 5 inductor design values and extracted values.*

an inductor in the resonant T/R switch used to protect the LNA input. Figure 3.5 indicates the position of both inductors. Note that the VCO employs two inductors in a counterwound arrangement in an attempt to reduce coupling. This attempt is shown to be less than totally effective in Chapter 6, where we investigate the detailed origin of the pulling problem. To quantify the coupling between each set of inductors, the VCO, 100 mW PA, and T/R switch inductors were drawn and simulated together in ADS Momentum, as shown in Figure 3.6. An 8-port S-parameter network was extracted to model the interactions between inductors. The mutual inductance M and coupling coefficient k for each pair of inductors can be calculated from the extracted S-parameters using

$$M = \sqrt{\mathrm{Im}(Z_{12})\,\mathrm{Im}(Z_{21})} \tag{3.1a}$$

$$k = \sqrt{\frac{\mathrm{Im}(Z_{12})\,\mathrm{Im}(Z_{21})}{\mathrm{Im}(Z_{11})\,\mathrm{Im}(Z_{22})}} \tag{3.1b}$$

Table 3.1 compares the design values of the inductors in Figure 3.5 with their extracted inductances. Following the inductor labeling in Figure 3.5, $k_{a,c}$ and $k_{a,d}$ will be used to denote the coupling coefficients between the 100 mW PA inductor and the top and bottom VCO inductors, respectively. Likewise, $k_{b,c}$ and $k_{b,d}$ denote the coupling coefficients between the VCO inductors and the resonant T/R switch.

3.2.1 Coupling Between the 100 mW PA and the VCO

Figure 3.7 plots the simulated mutual inductance and coupling coefficient between the VCO inductors and the 100 mW PA inductor. Although the differential VCO was laid out symmetrically, it was positioned slightly off the centerline of the 100 mW PA inductor. This resulting in slightly different flux linkage between the upper and lower VCO inductors. In the extracted model, $k_{ac} = 0.00073$ and $k_{ad} = 0.00071$.

The 100 mW PA delivers a measured +18 dBm into 50 Ω, corresponding to a peak voltage of 2.51 V. To determine the voltage induced across the VCO inductors by

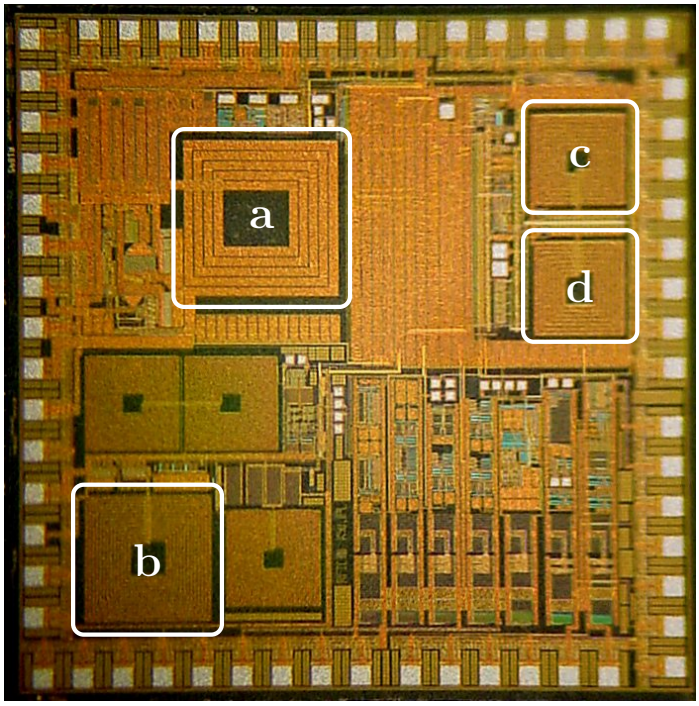


Figure 3.5: *Inductor locations in the K-State Microtransceiver. (a) 100 mW PA inductor. (b) Resonant T/R switch. VCO inductors (c) and (d).*

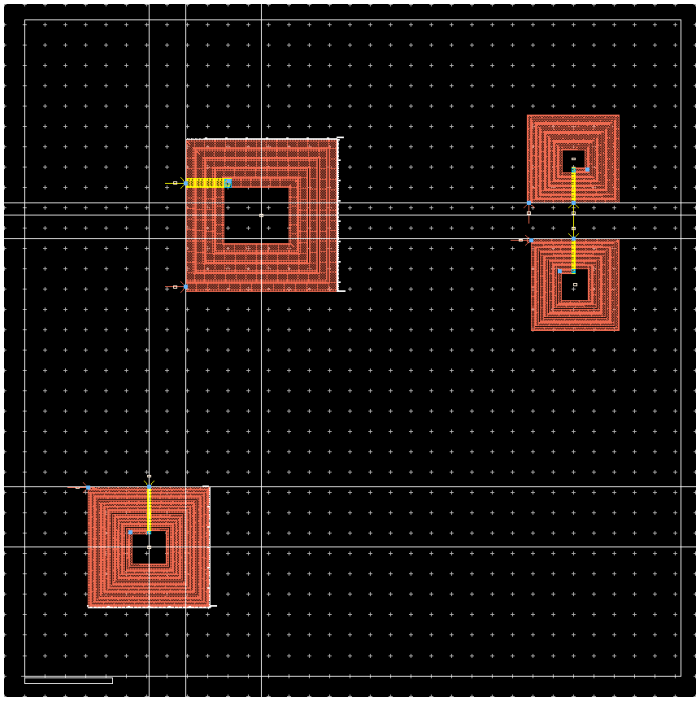
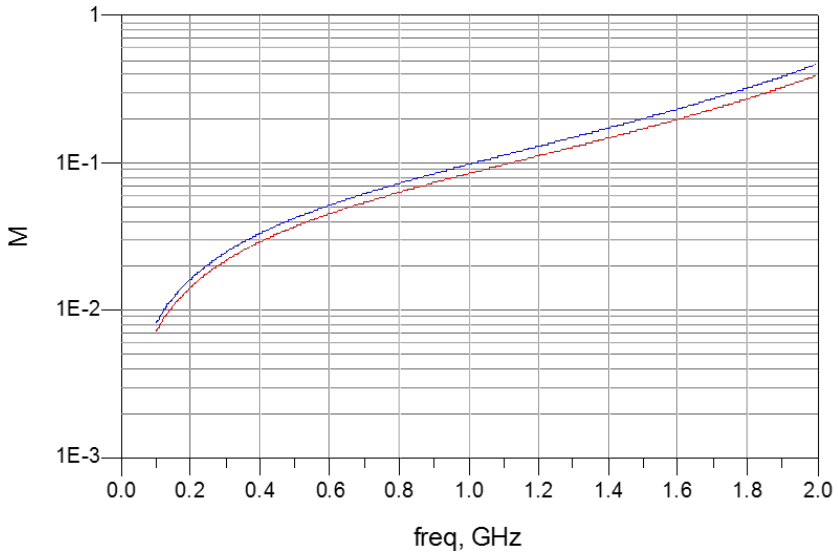
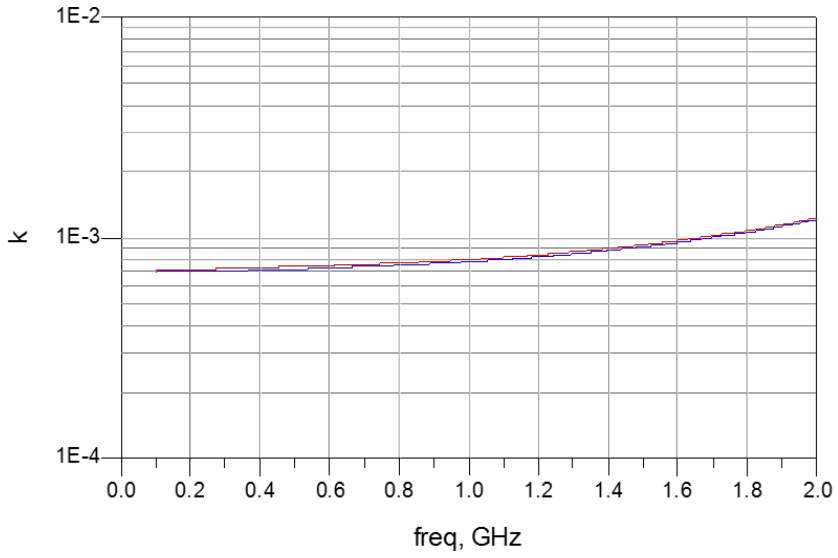


Figure 3.6: *ADS Momentum simulation of Fab 5 inductor S-parameters.*



(a)



(b)

Figure 3.7: *Extracted M and k between the 100 mW PA and the top (red) and bottom (blue) VCO inductors. At midband (420 MHz), $k_{a,c} = 0.00073$ and $k_{a,d} = 0.00071$.*

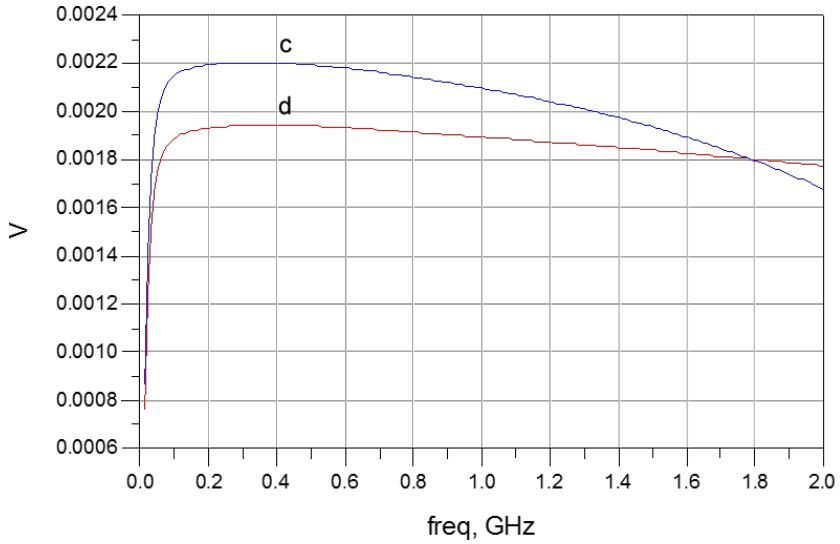


Figure 3.8: *Voltage induced in the VCO inductors (c and d) by the 100 mW PA.*

the 100 mW PA, a frequency-domain simulation was performed on the extracted S-parameter network. The PA inductor was driven with a 2.51 V source, and the induced voltage across the other extracted inductors was simulated over the microtransceiver's operating band. Figure 3.8 is a plot of the voltage induced in the VCO inductors by the 100 mW PA. At 420 MHz, the PA induced a 1.9 mV voltage across the terminals of the VCO inductor.

3.2.2 Coupling Between the T/R Switch and the VCO

The second potential magnetic coupling path is through the microtransceiver's resonant T/R switch. The radio operates in half-duplex mode and uses one antenna, so the output of the 100 mW PA can be connected directly to the LNA input, as shown in Figure 3.1. A resonant T/R switch developed at K-State, shown in Figure 3.9a, is used to protect the sensitive LNA input during transmit and provide input matching for the LNA in receive mode [2]. When the microtransceiver is receive mode, the TX line in Figure 3.9a is pulled low, and L_1 and C_2 form a highpass matching network between the antenna and the LNA. When the microtransceiver is transmitting, TX is pulled high, and L_1 resonates with C_1 to present a high impedance to the PA output while simultaneously shorting the LNA input to ground. As shown in Figure 3.9b, the entire PA output voltage is developed across the resonating inductor when the radio is transmitting, potentially creating another magnetic coupling path between the PA and VCO.

Figure 3.10 plots the extracted M and k between the inductor in the resonant

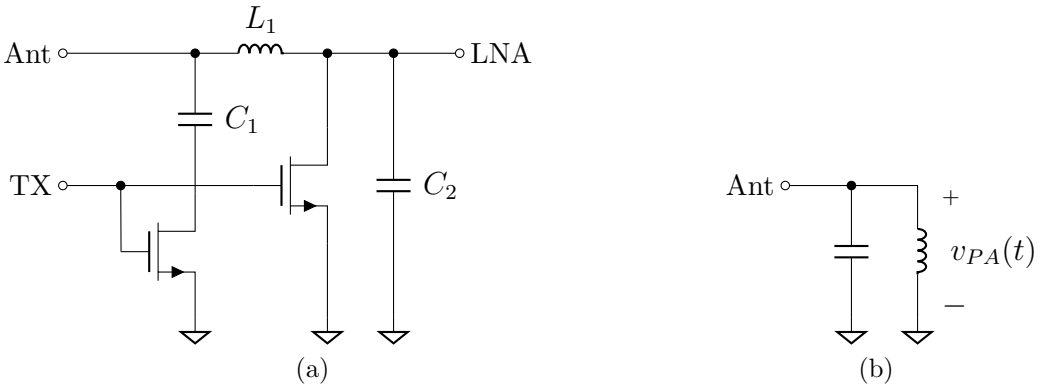


Figure 3.9: *(a) Schematic of the resonant T/R switch in the K-State Microtransceiver and (b) Equivalent circuit in transmit mode.*

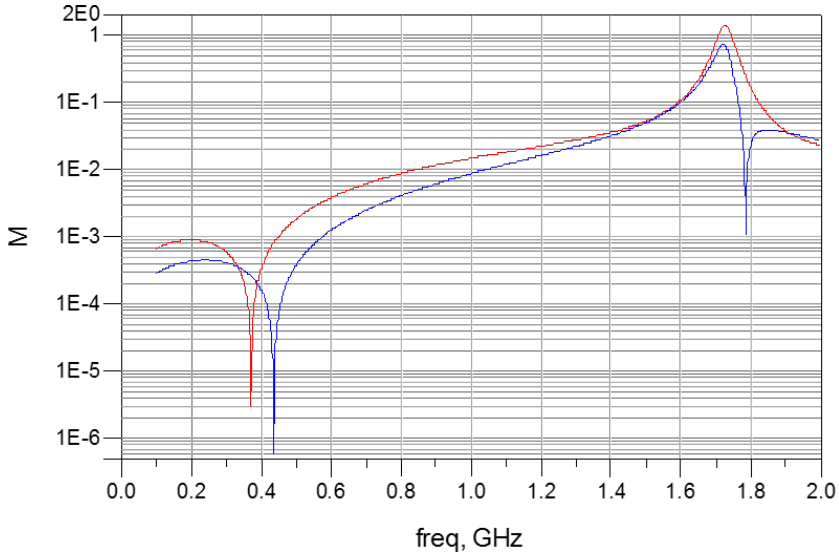
T/R switch and both VCO inductors. The extracted coupling coefficients between the T/R switch inductor and the upper and lower VCO inductors were calculated to be 6.3×10^{-6} and 6.1×10^{-6}, respectively, at 420 MHz, over two orders of magnitude less than the coupling coefficients between the PA and VCO inductors.

Figure 3.11 compares the simulated voltages induced in the VCO inductors by the PA and by the T/R switch. At 420 MHz, the T/R switch induces a 53 μV voltage across the VCO inductors, compared to a 1.9 mV induced voltage from the PA. This implies that, although a small degree of magnetic coupling exists between the resonant T/R switch and the VCO, it is not as significant a contributor to the QPSK pulling problem as the main PA inductor aggressor.

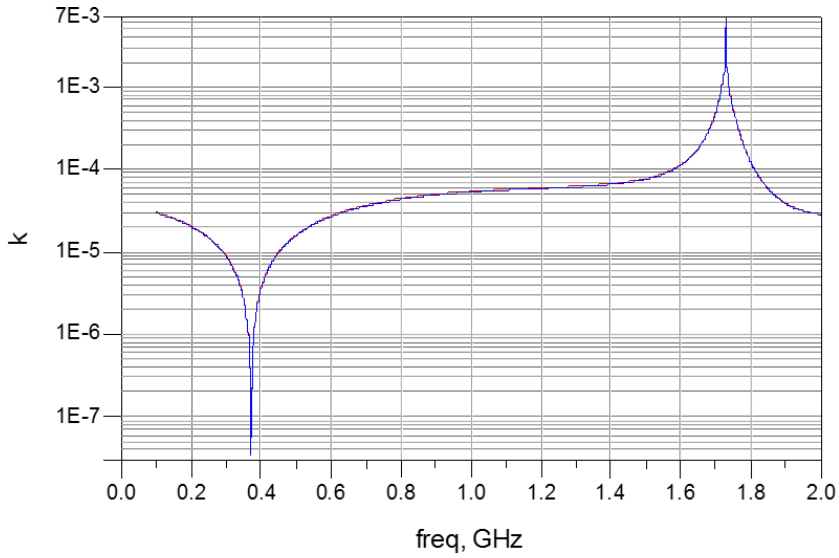
3.2.3 Simulation of the PA-VCO Magnetic Coupling Path

To confirm that magnetic coupling between the PA and VCO inductors was responsible for frequency pulling, the transmit half of the K-State Microtransceiver (minus the fractional-N frequency synthesizer) was imported into Agilent ADS. A transient simulation was performed of the microtransceiver running open-loop while transmitting 10 kbps BPSK and QPSK. To model the interaction between inductors, the inductors in the VCO, 100 mW PA, and resonant T/R switch were replaced with the 8-port S-parameter model extracted from ADS Momentum.

Figure 3.12 compares the simulated open-loop output transmit frequency of the microtransceiver for different BPSK and QPSK symbols. The microtransceiver's output frequency remained constant for all BPSK symbols, indicating no LO pulling. However, changing between adjacent QPSK symbols (from an output phase of $\phi = 0$ or π to an output phase of $\phi = \frac{\pi}{2}$ or $\frac{3\pi}{2}$) produced an 80 kHz change in open-loop



(a)



(b)

Figure 3.10: *Extracted M and k between the resonant T/R switch and the upper (blue) and lower (red) VCO inductors.*

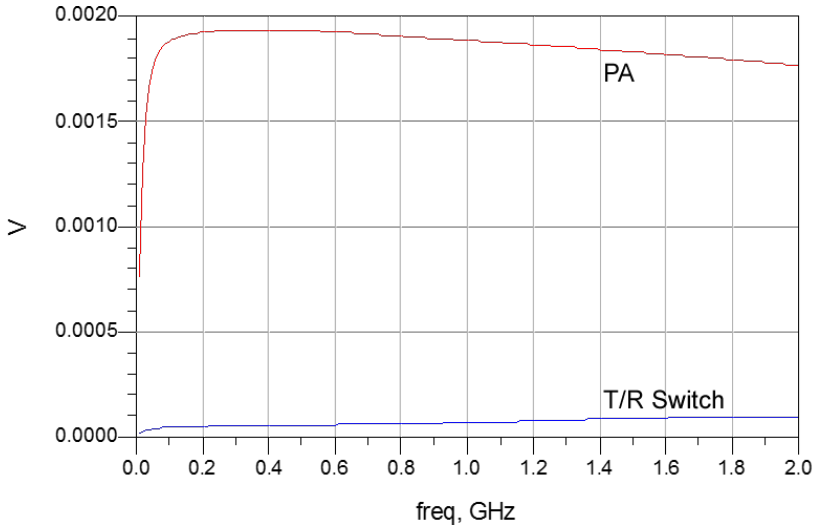


Figure 3.11: *Voltage induced in the VCO inductors by the PA and by the T/R switch.*

output frequency. Since the microtransceiver was simulated transmitting constant-envelope phase modulation, the total accumulated phase error over one symbol period T_s produced by a change in frequency Δf is given by

$$\Delta\phi = \int_0^{T_s} 2\pi \cdot \Delta f \, dt = 2\pi \cdot T_s \cdot \Delta f \tag{3.2}$$

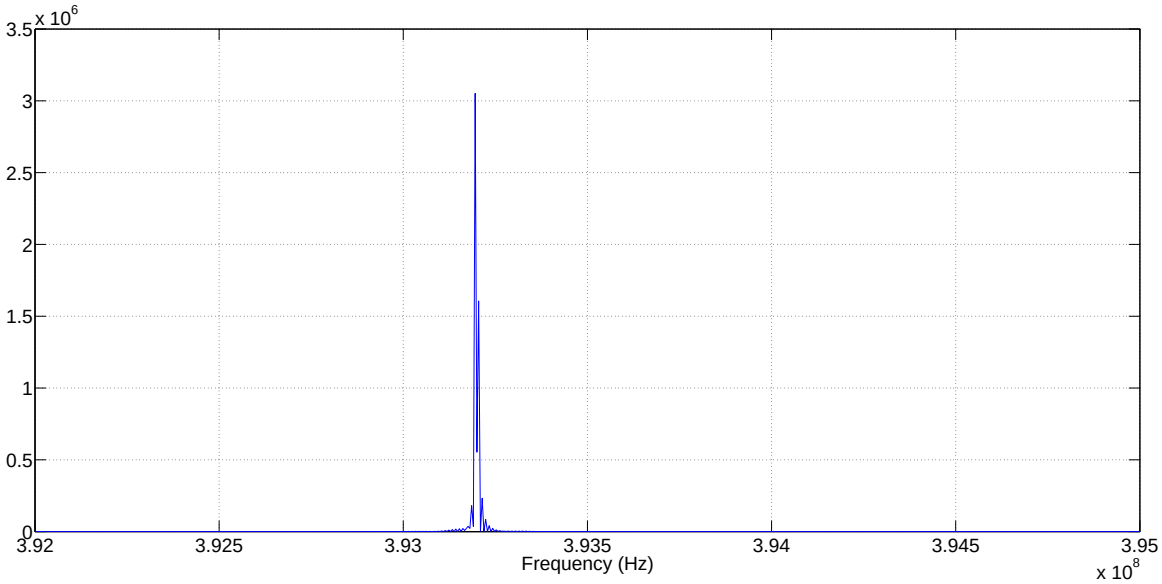
where T_s is the symbol period. Since the microtransceiver operates with a 100 kHz loop bandwidth, however, $T_s = 1 \times 10^{-5}$ for data rates less than 100 kHz. Applying Equation 3.2, the accumulated phase error created by the simulated 80 kHz jump in output frequency would be

$$\Delta\phi = 2\pi \cdot T_s \cdot \Delta f = 2\pi \cdot \frac{80\,\text{kHz}}{100\,\text{kHz}} = 5.02\,\text{rad} \tag{3.3}$$

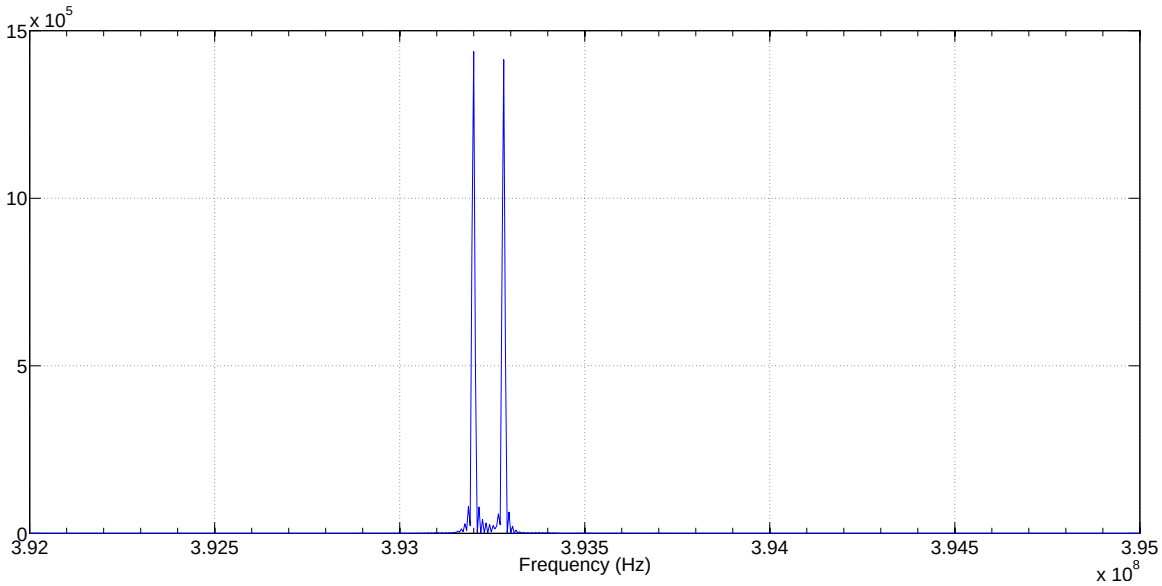
In Figure 3.4d, the observed accumulated phase error while transmitting 10 kbps RC-BPSK was between $\frac{\pi}{2}$ (1.571) and π (3.142) radians. Therefore, the simulation closely matches the measured performance of the microtransceiver and strongly indicated that magnetic coupling between the 100 mW PA and VCO is the dominant LO pulling mechanism.

3.3 Capacitive Coupling

When the K-State Microtransceiver was designed, a top-metal ground shield, shown in Figure 3.13, was implemented over the fractional-N synthesizer and digital pro-



(a) 10 kbps BPSK.



(b) 10 kbps RC-BPSK.

Figure 3.12: *Simulated open-loop output frequency when transmitting BPSK and RC-BPSK. Transitioning between RC-BPSK symbols produced a Δf of 80 kHz.*

gramming registers to prevent digital noise from capacitively or inductively coupling into the LNA and high-gain IF chain while the radio was operating in receive mode [1]. The close proximity of the Σ-Δ modulator to the PA required the shield to come within 60 μm of the PA inductor and 30 μm of the VCO inductors. Because of its close proximity to both the VCO and 100 mW PA inductors, it was speculated that fringing-field capacitance between the inductors and the non-zero impedance of the bondwire to ground allowed the PA output signal to capacitively couple from the outer windings of the PA inductor to the outer windings of the VCO inductors.

To determine its contribution to the QPSK pulling problem, the ground shield was added to the inductor layout in ADS Momentum, shown in Figure 3.13, and a 9-port S-parameter network was extracted to model the interaction between the VCO and 100 mW PA. The voltage induced in the VCO inductors by the PA was then simulated with a 10 nH bondwire inductance between the shield and ground. Figure 3.15 compares the voltage induced in the VCO inductors by the PA with and without the ground shield. Between 390 and 450 MHz, the shield contributes less than 200 μV of additional induced voltage across the VCO inductors, an increase of roughly 10%.

It was therefore concluded that, while some capacitive coupling exists between the PA and the VCO through the top-metal ground shield, it was likely not a significant contributor to the pulling problem. However, electric field coupling between the synthesizer ground shield and top-metal features in the receiver—including the outer windings of the LNA inductor—is responsible for the appearance of a 4.8 MHz divided-reference spur in the IF output. In Chapter 8, the synthesizer ground shield is redesigned to reduce metal-to-metal coupling between the shield and the receiver while still providing adequate shielding for the synthesizer. Additionally, the bondwire inductance between the synthesizer shield and ground resonates with the fringing-field capacitance of the shield and creates a resonant peak at 1.9 GHz, as seen in Figure 3.15. Care must be taken in such designs to insure that the shield-bondwire resonance remains outside the operating band of both the PA (390-450 MHz) and the VCO (620-1060 MHz).

3.4 Additional Coupling Paths

While the 100 mW PA was clearly the cause of LO pulling in the K-State Micro-transceiver, and magnetic coupling a clear contributor, the system-level coupling mechanisms identified in 2.5 were also considered. Due to the high current draw

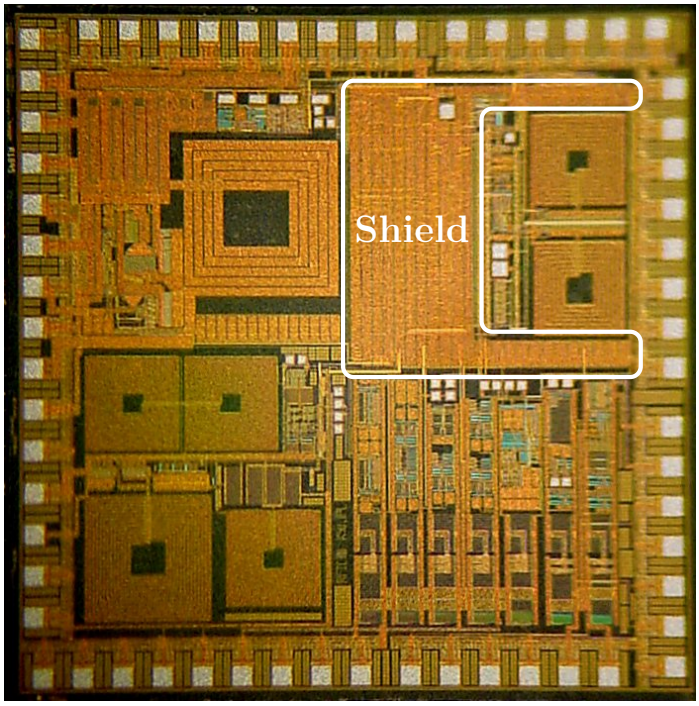


Figure 3.13: *Location of the top-metal synthesizer ground shield.*

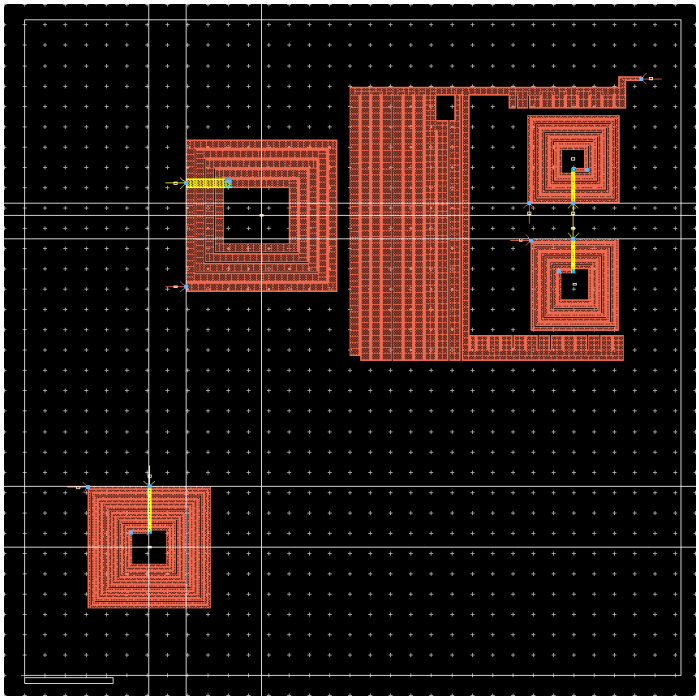


Figure 3.14: *ADS Momentum simulation of Fab 5 inductor S-parameters with top-metal synthesizer ground shield.*

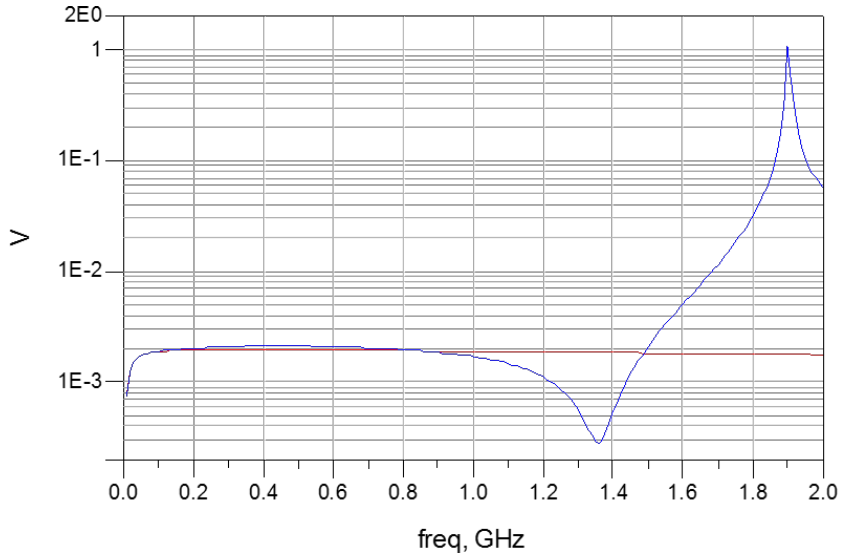


Figure 3.15: *Voltage induced in the VCO inductors by the PA, with (blue) and without (red) the top-metal synthesizer ground shield. Note the presence of the resonant peak at 1.9 GHz.*

of the 100 mW PA, power supply ripple and ground bounce were identified as possible coupling paths for the aggressor signal from the PA to couple back into the VCO. To assess the contribution of system-level coupling issues to the pulling problem, the microtransceiver was extensively tested, including

- testing on three different boards with different layouts,
- testing with different decoupling capacitance configurations, including removing all board-level decoupling on the VCO and PA,
- comparing the performance of the radio in TQFP and QFN packages to observe the effect of increased bondwire and lead inductance,
- comparing the performance of the radio in packages with and without ground down-bonds, and
- attempting to induce LO pulling by magnetically coupling the 10 mW output back into the loop filter.

Surprisingly, however, none of these tests produced any discernible change in the microtransceiver's BPSK or QPSK performance, nor were they able to produce LO pulling when the 100 mW PA was off. In general, the radio was found to be very robust. This indicated that the system-level and non-inductive coupling mechanisms

discussed in Section 2.5 had been well-addressed in the original design, and were not significant contributors to the QPSK pulling problem.

3.5 Summary

The BPSK and QPSK performance of the K-State Microtransceiver was tested in various operating modes to determine the cause of LO pulling. It was discovered that the microtransceiver could transmit both BPSK and QPSK without pulling using the 10 mW low-power amplifier, an exponential-horn pad driver. When the 100 mW class-C medium-power amplifier was activated, the microtransceiver experienced severe LO pulling when transmitting QPSK. At data rates faster than 10 kbps, LO pulling is so severe that the signal constellation cannot be demodulated. The radio's BPSK performance, however, is unaffected by the 100 mW PA.

The correlation between LO pulling and the 100 mW PA strongly suggested that an inductive coupling mechanism between the PA and VCO inductors was somehow responsible for the LO pulling. A series of design reviews identified two potential magnetic coupling paths between the PA and VCO. When the 100 mW PA is operating, the PA output is magnetically coupled into the VCO inductors from both the 100 mW PA inductor and the inductor in an integrated resonant T/R switch. The VCO, PA, and T/R switch inductors were simulated together in ADS Momentum, and an 8-port network of S-parameters was extracted to model the interaction between inductors. The PA and VCO inductors were found to be the dominant magnetic coupling path with an extracted coupling coefficient of 0.00036 at 420 MHz, implying that the 100 mW PA output would induce a 2 mV peak voltage in the VCO inductors. A potential capacitive coupling path between the PA and VCO inductors through a top-metal ground shield was also simulated and found not to be a strong contributor to the interaction between the PA and VCO.

To verify that magnetic coupling between the PA and VCO is the primary LO pulling mechanism, the transmit half of the microtransceiver was imported into Agilent ADS. The microtransceiver was simulated transmitting both BPSK and QPSK at 10 kbps, using the extracted 8-port S-parameter network to model the interaction between integrated inductors. As expected, the microtransceiver's output frequency remained constant for all BPSK symbols, indicating no LO pulling. However, changing between adjacent QPSK symbols (from an output phase of 0 or π to an output phase of $\frac{\pi}{2}$ or $\frac{3\pi}{2}$) produced an 80 kHz change in output frequency, corresponding to an accumulated phase error of 5 radians over one symbol period. This closely agrees with

the microtransceiver's observed QPSK performance. It was therefore concluded that magnetic coupling between the PA and VCO inductors is the primary LO pulling mechanism. The mechanisms of this pulling, together with the reason the microtransceiver's BPSK performance is unaffected by magnetic coupling between the PA and VCO, are studied in the following chapters.

Chapter 4

The Differential Cross-Coupled LC VCO

Having identified magnetic coupling between the 100 mW PA and VCO as the primary LO pulling mechanism in the K-State Microtransceiver, the operation of the VCO was closely scrutinized. This chapter presents a circuit-level analysis the microtransceiver's differential LC VCO in preparation for the analysis of a VCO under magnetic coupling in Chapter 5. Since the constellation smearing observed in QPSK mode is caused by frequency pulling, this chapter focuses on the frequency tuning mechanisms in the microtransceiver, specifically the small-signal and large-signal operation of the VCO's MOS varactors.

4.1 The K-State Microtransceiver VCO

The K-State Microtransceiver employs the differential cross-coupled LC VCO topology shown in Figure 4.1. Inductors L_c and L_d are named in accordance with the labeling in Figure 3.5. The polarities of both inductors are oriented to minimize coupling onto the differential-mode VCO outputs. Transistor M_1 is a standard PMOS current source, and cross-coupled FETs M_{2a} and M_{2b} form the negative-resistance compensating the losses in the LC tank. Transistor M_3 is sized to bias the VCO outputs at half the supply voltage for maximum output voltage swing.

Coarse frequency tuning is accomplished using a binary-weighted bank of switched MIM capacitors, shown in Figure 4.2a, and analog frequency tuning is accomplished using inversion-mode MOS (I-MOS) varactors, shown in Figure 4.2b. In order to span the 390-450 MHz band, the VCO tunes from 620-1060 MHz and a quadrature divide-by-two is used to generate differential I and Q signals.

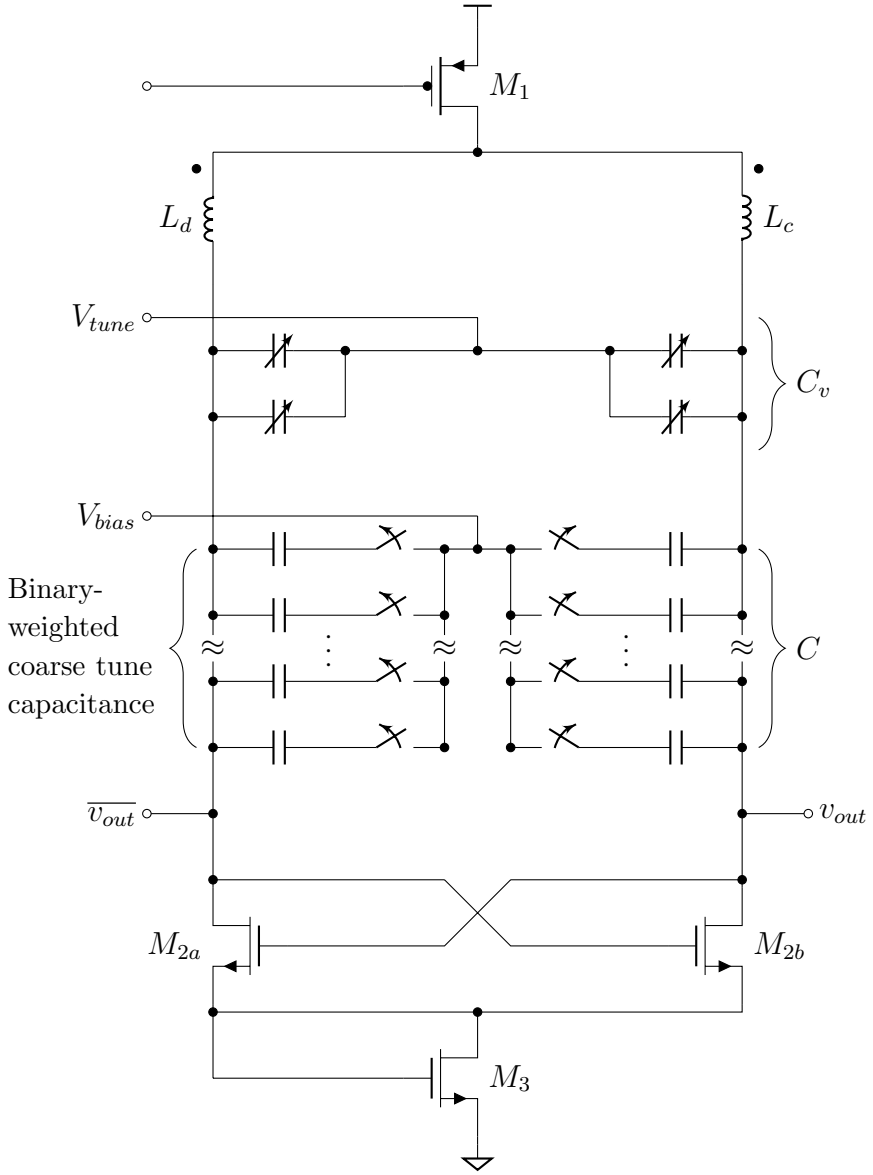


Figure 4.1: *Schematic of the K-State Microtransceiver VCO.*

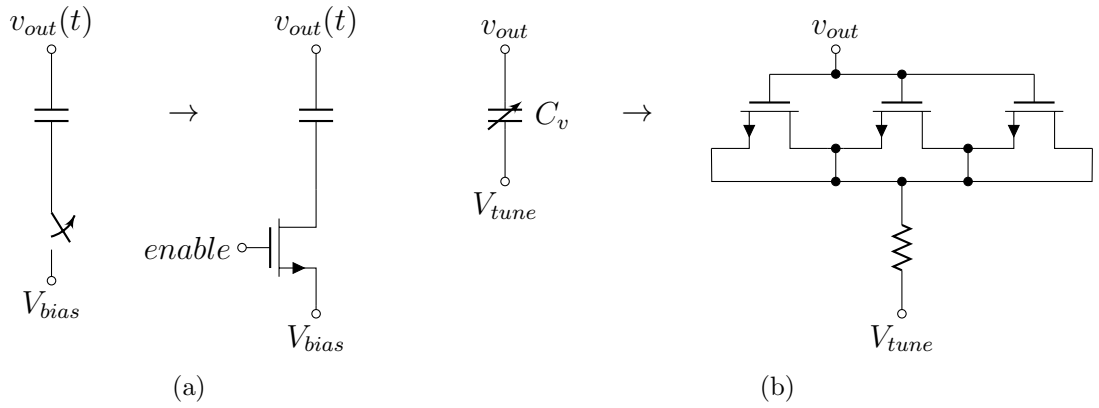


Figure 4.2: *Detail of the Fab 5. (a) Switched MIM capacitors for coarse frequency tuning. (b) MOS varactors for analog frequency tuning.*

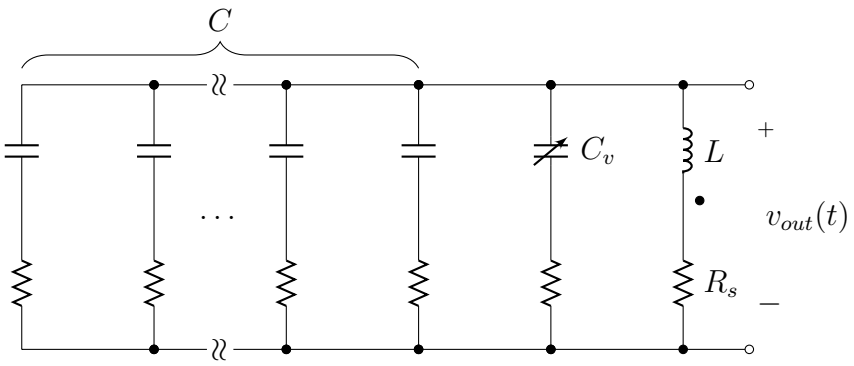


Figure 4.3: *Series-resistance half-circuit representation of the Fab 5 VCO LC tank.*

4.1.1 LC Tank Properties

Figure 4.3 illustrates the half-circuit representation of the LC tank with losses modeled by series resistance. To a first order, the single-ended output voltage is a sinusoid

$$v_{out}(t) = V_0 \sin(\omega_c t + \theta) + V_{DC} \tag{4.1}$$

with peak amplitude V_0, angular frequency ω_c, phase offset θ, and DC bias V_{DC}. The series-resistance representation more closely represents the physical losses in integrated inductors and capacitors. For convenience, however, Figure 4.3 can be transformed into the parallel-resistance representation in Figure 4.4 and collect the parallel resistance terms of all components into R_p.

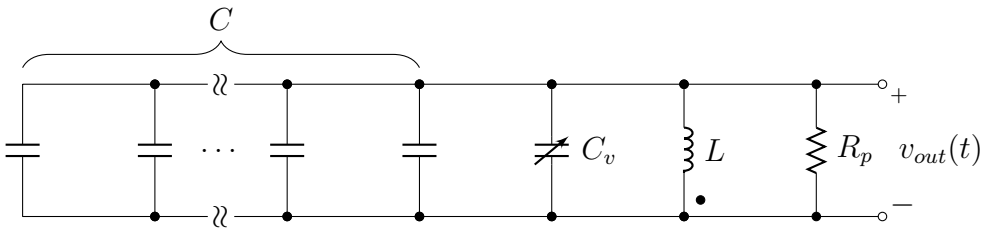


Figure 4.4: *Parallel-resistance half-circuit representation of the Fab 5 VCO LC tank.*

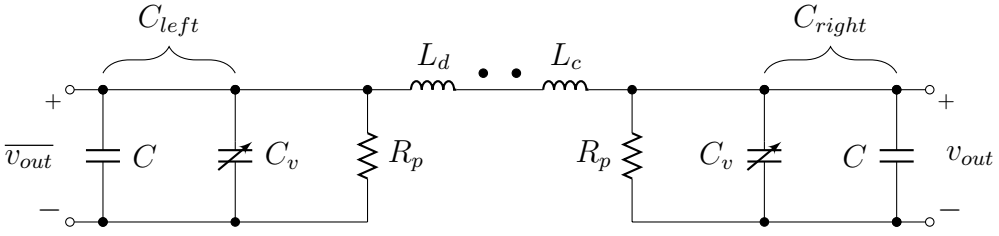


Figure 4.5: *Full resonant circuit representation of the Fab 5 VCO LC tank.*

4.1.2 Frequency of Oscillation

If the left and right tank capacitances in a differential LC VCO are equal, the LC tank reduces to the half-circuit shown in Figure 4.4, and the frequency of oscillation is given by

$$\omega_c^2 = \frac{1}{L\left(C + C_v\right)} \tag{4.2}$$

However, if the left and right tank capacitances are unequal, the LC tank can be treated as the full resonant circuit shown in Figure 4.5. The frequency of oscillation is then given by

$$\omega_c^2 = \frac{1}{2L}\left(\frac{1}{C_{left}} + \frac{1}{C_{right}}\right) \tag{4.3}$$

where C_{left} and C_{right} are the total capacitances on each half of the tank. Chapters 5 and 6 will discuss situations in which asymmetric tank capacitance helps to reduce frequency pulling.

4.2 Inversion-Mode MOS Varactors

The Fab 5 K-State Microtransceiver uses two sets of 420 fF MOS varactors (shown in Figure 4.2b) connected in parallel for analog frequency tuning. Since silicon-on-sapphire IC processes have no body contacts, MOS varactors are constructed simply by tying the drain and source of a transistor together. When $V_{GS} < V_{TH}$, the varactor

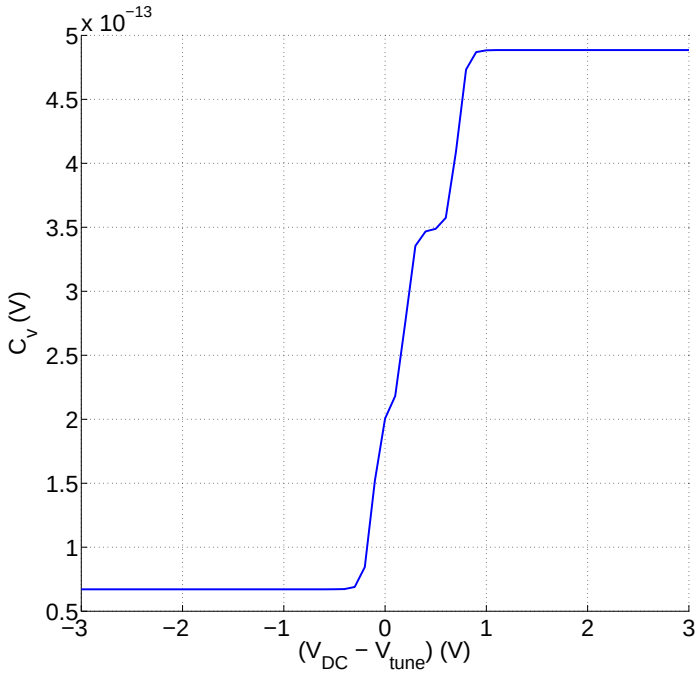


Figure 4.6: *Small-signal C-V curve of the 420 pF Fab 5 MOS varactor.*

capacitance is the sum of the parasitic C_{GS}, C_{GD}, and fringing field capacitance between gate-drain and gate-source interconnects. However, when $V_{GS} > V_{TH}$, the device operates in strong inversion mode, and the resulting capacitance increases by

$$C = W \cdot L \cdot \frac{\epsilon_{ox}}{t_{ox}} \tag{4.4}$$

where W and L are the width and length of the transistor gate, ϵ_{ox} is the dielectric constant of the gate oxide, and t_{ox} is the oxide thickness. Figure 4.6 illustrates the simulated DC/small-signal C-V curve of the I-MOS varactors in the K-State Microtransceiver. Three NMOS transistors with different threshold voltages were connected in parallel to allow the varactor to turn on piecewise and smooth the small-signal C-V curve.

4.2.1 Large-Signal Varactor Capacitance

Small-signal C-V curves of MOS varactors, like those illustrated in Figure 4.6, typically show high on/off capacitance ratios and sharp, sudden transitions, suggesting to the inexperienced designer that a VCO tuned by MOS varactors will have a similar frequency tuning curve. However, when MOS varactors are utilized for frequency tuning in a VCO tank circuit, the voltage swing across the varactors is large, and the

instantaneous capacitance of the varactors varies continuously with time as the VCO output voltage moves along the C-V curve. The effective varactor capacitance seen by the LC tank is thus an average of the instantaneous varactor capacitance over one period of the VCO output waveform.

Let $C_v(v)$ denote the small-signal varactor capacitance as a function of voltage, and let $v(t)$ be the voltage across the MOS varactors shown in Figure 4.1, expressed as

$$v(t) = V_0 \sin(\omega_c t) + V_{DC} - V_{tune} \tag{4.5}$$

where V_{DC} is the DC bias on the VCO output and V_{tune} is the tuning voltage applied to the varactors. The average varactor capacitance over one period of the VCO output waveform is given by

$$C_{v_{avg}} = \frac{\omega_c}{2\pi} \int_0^{\frac{2\pi}{\omega_c}} C_v(v(t))dt \tag{4.6}$$

Substituting Equation 4.5 into Equation 4.6 yields

$$C_{v_{avg}} = \frac{\omega_c}{2\pi} \int_0^{\frac{2\pi}{\omega_c}} C_v(V_0 \sin(\omega_c t) + V_{DC} - V_{tune})dt \tag{4.7}$$

Since $C_v(v(t))$ depends on both the IC process and the design of the varactors, Equation 4.7 must be integrated numerically.

Figure 4.7 plots the DC/small-signal and large-signal C-V curves of the micro-transceiver's varactors together, using extracted values from Chapter 3. As previously mentioned, three MOS varactors with different V_T were connected in parallel to broaden the small-signal C-V curve in an attempt to produce a more linear VCO tuning characteristic. The three threshold voltages are clearly visible in the curves. When the large-signal excitation is considered, however, the curve naturally smooths out over a range of voltages determined by the VCO output amplitude.

From Figure 4.7 and Equation 4.7, we can observe that the VCO output amplitude directly affects the average varactor capacitance. When V_0 goes to zero,

$$\lim_{V_0 \to 0} C_{v_{avg}} = \frac{\omega_c}{2\pi} \int_0^{\frac{2\pi}{\omega_c}} C_v(V_{DC} - V_{tune})dt = C_v(V_{DC} - V_{tune}) \tag{4.8}$$

and $C_{V_{avg}}$ converges to the DC/small-signal C-V curve. Conversely, as V_0 increases, $v(t)$ swings over a wider portion of the C-V curve during one period of the VCO output, producing a greater smoothing effect. The VCO's output DC bias, V_{DC}, affects the point on the DC C-V curve around which the large-signal characteristic

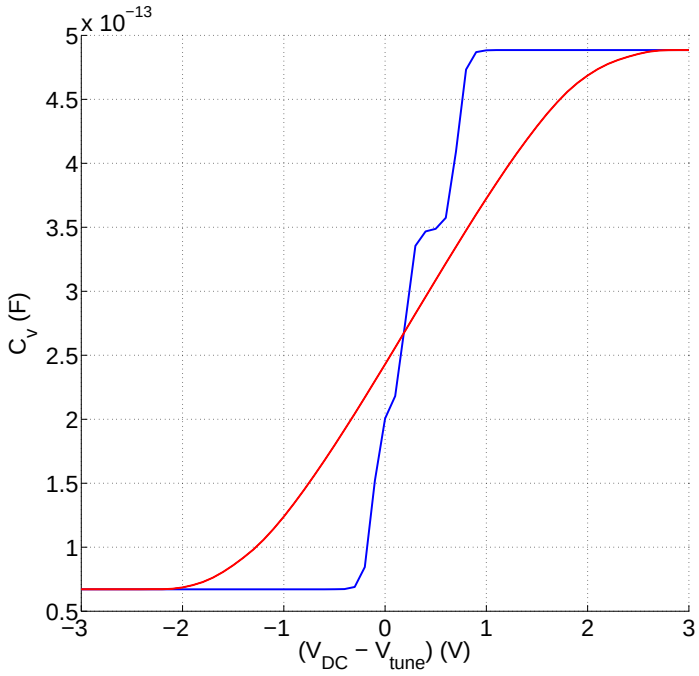


Figure 4.7: *Fab 5 DC/small-signal (blue) and large-signal (red) MOS varactor C-V curves.*

swings. This amplitude-dependent behavior will be found to play a significant role in the pulling problem in the following chapter.

Chapter 5

Frequency Pulling in an LC VCO Under Magnetic Coupling

The K-State Microtransceiver has seven integrated inductors on a 3.2×3.2 mm die. While magnetic coupling was considered in the original design, the specific interactions between the inductors were not fully investigated, and in Chapter 3, we saw that magnetic coupling between the 100 mW PA and VCO induces a 2 mV peak voltage change across each of the VCO inductors. This chapter expands on the analysis in Chapter 3 to show how an aggressor signal magnetically coupled into the LC tank time-modulates the varactor capacitance to produce frequency pulling in the VCO and analyzes how aggressor signals with different modulation schemes affect pulling. While the procedure in [31] could also be applied with identical results, this chapter offers a simplified, more intuitive approach to understanding the problems created by the large-signal behavior of MOS varactors and its application to reduction of pulling. This chapter also identifies the reason why the microtransceiver's BPSK performance is unaffected by magnetic coupling between the PA and VCO.

5.1 Analysis of a VCO Under Magnetic Coupling

Figure 5.1 is a schematic diagram of the VCO in the K-State Microtransceiver illustrating a magnetic coupling path between an aggressor inductor and the inductors in the LC tank. The current flowing in the aggressor inductor induces voltages across the inductors in the LC tank which sum with the VCO output voltages by superposition. To begin analyzing the LC VCO under magnetic coupling, first consider the equivalent parallel half-circuit in shown in 5.2. Let C_v denote the capacitance of the MOS varactors on each side of the tank, and let C denote the total remaining

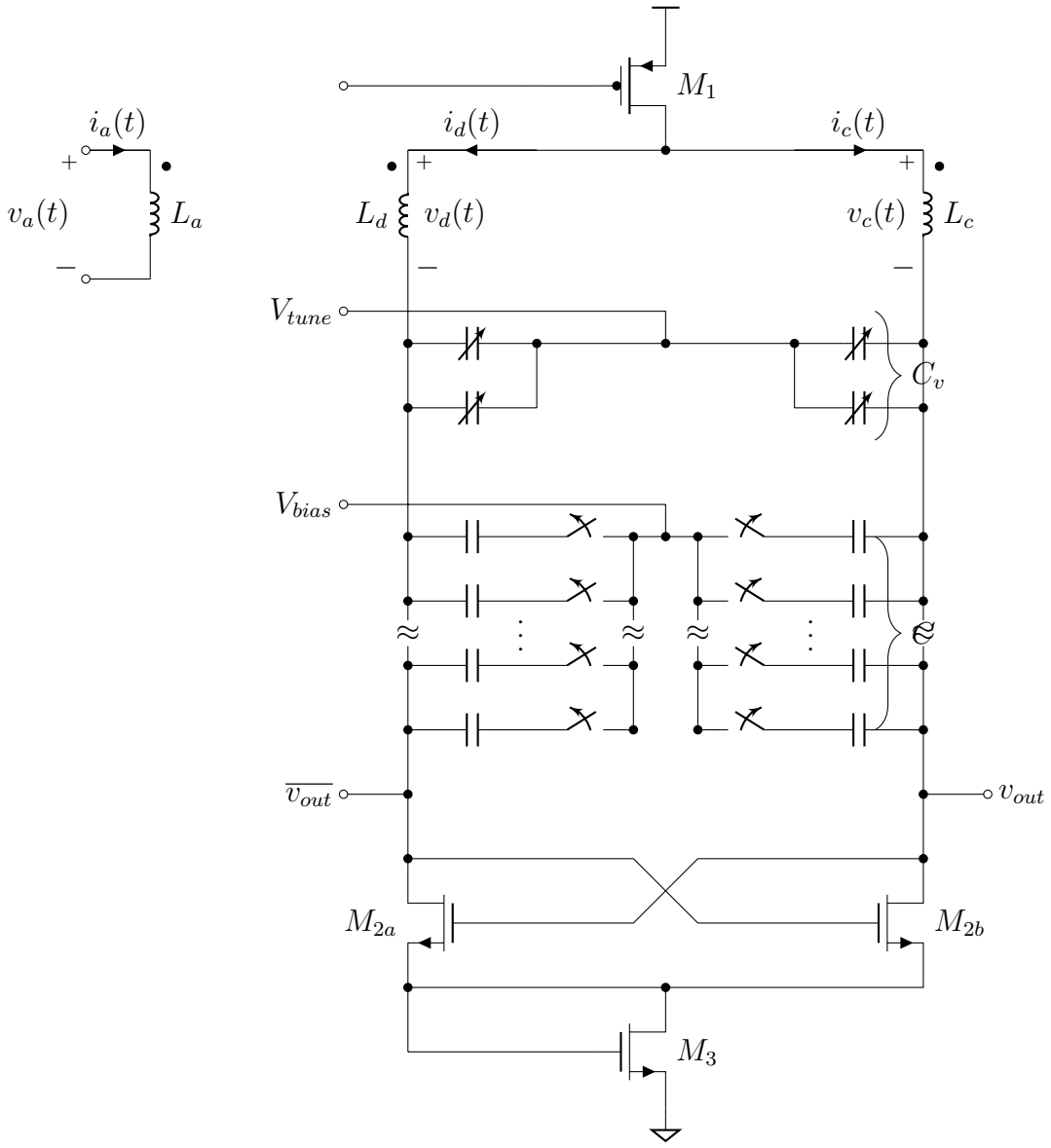


Figure 5.1: *Schematic of the Fab 5 VCO magnetically coupled to an aggressor inductor.*

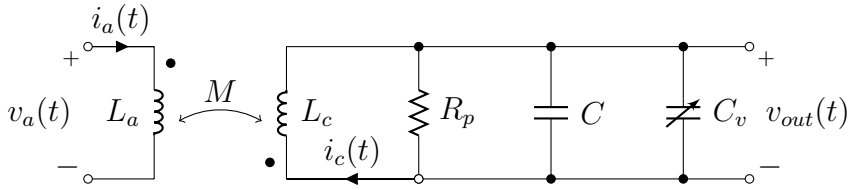


Figure 5.2: *Parallel half-circuit of the Fab 5 VCO magnetically coupled to an aggressor inductor.*

tank capacitance, including coarse-tune capacitance and all other parasitics. Let $v_a(t)$ be the voltage across the aggressor inductor L_a, and M be the mutual inductance between L_a and the inductors in the VCO tank. Note the location of the mutual inductance dots. Following the dot convention, the oscillator's single-ended output voltage can be expressed as

$$v_{out}(t) = V_0 \cdot \cos(\omega_c t) + V_{DC} - M \cdot \left(\frac{\mathrm{d}i_a(t)}{\mathrm{d}t}\right) \tag{5.1}$$

or

$$v_{out}(t) = V_0 \cdot \cos(\omega_c t) + V_{DC} - \left(\frac{M}{L_a}\right) \cdot v_a(t) \tag{5.2}$$

Continuing the analysis in Chapter 4, the voltage across the varactors is given by

$$v(t) = V_0 \cdot \cos(\omega_c t) + V_{DC} - V_{tune} - \left(\frac{M}{L_a}\right) \cdot v_a(t) \tag{5.3}$$

Since the quantity $\frac{M}{L_a}$ is unitless, Equation 5.3 can be written as

$$v(t) = A \cdot \cos(\omega_c t) + B + K \cdot v_a(t) \tag{5.4}$$

where A is the peak amplitude of the VCO, B is the total DC voltage across the varactors, and K is a constant between -1 and 1 representing the amplitude of the aggressor signal $v_a(t)$. From Equation 4.7, the average varactor capacitance is given by

$$C_{v_{avg}} = \frac{\omega_c}{2\pi} \int_0^{\frac{2\pi}{\omega_c}} C_v(A \cdot \cos(\omega_c t) + B + K \cdot v_a(t))dt \tag{5.5}$$

While the analysis in this chapter will begin by focusing on magnetic coupling, writing Equation 5.5 in terms of A, B, and K instead of M and L allows us to apply the analysis to other coupling mechanisms as well, including capacitive coupling and system-level mechanisms like power supply and ground bounce.

5.2 Frequency Pulling due to Modulation

The intent of this analysis is to determine whether a given aggressor signal $v_a(t)$ will produce frequency pulling. Since $C_v(v)$ must be integrated numerically, it is impossible to find an analytical expression for the average varactor capacitance as a function of $v_a(t)$. However, in order for frequency pulling to not occur, the average varactor capacitance must remain constant, no matter how $v(t)$ is perturbed by $v_a(t)$.

In other words,

$$\frac{\omega_c}{2\pi}\int_0^{\frac{2\pi}{\omega_c}} C_v(v(t))dt = \alpha \tag{5.6}$$

where α is a constant for all $v_a(t)$. Since the small-signal C-V curve of an I-MOS varactor can be considered to be monotonically increasing,

$$\frac{\omega_c}{2\pi}\int_0^{\frac{2\pi}{\omega_c}} C_v(v(t))dt = \alpha \implies \frac{\omega_c}{2\pi}\int_0^{\frac{2\pi}{\omega_c}} v(t)dt = \gamma \tag{5.7}$$

where γ is a constant for all $v_a(t)$. Equivalently,

$$\frac{\omega_c}{2\pi}\int_0^{\frac{2\pi}{\omega_c}} A\cdot\cos(\omega_c t) + B + K\cdot v_a(t)dt = \gamma \tag{5.8}$$

Therefore, we can determine if a given aggressor signal will produce frequency pulling by examining the average voltage across the varactors over one period of the VCO output waveform.

5.2.1 Amplitude Modulation

Since the motivation of this research was to identify and fix the pulling problem in the K-State Microtransceiver, constant-envelope phase modulation will be the primary focus of this analysis. However, we immediately see from Equation 5.4 that if the amplitude and/or phase of $v_a(t)$ are asynchronous with $v_{out}(t)$, the average varactor voltage $v_{avg}(t)$ and average varactor capacitance $C_{v_{avg}}$ will change with time, producing a constantly-changing VCO frequency. Unfortunately, this implies that amplitude-modulation schemes, including QAM and ASK, will produce frequency pulling.

5.2.2 Constant-Envelope Phase Modulation

Due to the presence of the inverter-based 10 mW PA, the K-State Microtransceiver transmits constant-envelope BPSK, QPSK, and FSK (synthesized with external IQ modulator inputs). As discussed in Chapter 3, the VCO operates at twice the output frequency and generates I and Q waveforms using a quadrature divider. Therefore, $v_a(t)$ is a constant-envelope phase-modulated waveform with a phase and frequency relationship to the VCO. Taking the phase of the VCO as reference, we define N, the

quadrature divider ratio, as

$$N = \frac{f_{vco}}{f_{out}} \tag{5.9}$$

This allows us to simplify Equation 5.4 to

$$v(t) = A \cdot \cos(\omega_c t) + B + K \cdot \cos\left(\frac{\omega_c}{N} t + \theta + \phi(t)\right) \tag{5.10}$$

where θ is a constant phase offset and $\phi(t)$ is the phase of the modulated waveform. Since the microtransceiver transmits constant-envelope phase modulation, ϕ changes instantaneously and remains constant for the duration of the symbol period. Equation 5.10 becomes

$$v(t) = A \cdot \cos(\omega_c t) + B + K \cdot \cos\left(\frac{\omega_c}{N} t + \theta + \phi_i\right) \tag{5.11}$$

The integral of $v(t)$ over one period of the VCO output must be constant and unchanging for all ϕ_i values created in the modulating process to prevent frequency pulling.

$$\frac{\omega_c}{2\pi} \int_0^{\frac{2\pi}{\omega_c}} A \cdot \cos(\omega_c t) + B + K \cdot \cos\left(\frac{\omega_c}{N} t + \theta + \phi_i\right) dt = \gamma \tag{5.12}$$

Solving the integral in 5.12 yields

$$B + \left(\frac{K \cdot N}{\pi}\right) \sin\left(\frac{\pi}{N}\right) \cos\left(\theta + \frac{\pi}{N} + \phi_i\right) = \gamma \tag{5.13}$$

This relationship is satisfied only when

$$\phi_i = \frac{2\pi \cdot n}{N}, \; n = 0, 1, 2, ... \tag{5.14}$$

Equation 5.14 is the reason why the microtransceiver's BPSK performance is unaffected by magnetic coupling between the PA and VCO. Since the microtransceiver uses a VCO operating at twice the output frequency, $N = 2$, and the average varactor voltage will remain constant when transmitting $\phi_i = 0$ or π. However, when the microtransceiver attempts to transmit QPSK, using symbols with $\phi_i = \frac{\pi}{2}$ or $\frac{3\pi}{2}$, the average varactor voltage changes, producing the frequency jump observed in the QPSK simulations in Chapter 3. Another way of expressing the relationship in Equation 5.14 is

$$N = \frac{2\pi}{\phi_{min}} \tag{5.15}$$

where ϕ_{min} is the phase angle between adjacent symbols in the signal constellation. Therefore, a 4× VCO is required to transmit QPSK ($\phi_{min} = \frac{\pi}{2}$) without experiencing

pulling from the on-chip PA.

5.2.3 Band-Limited Modulation

In order to satisfy the Nyquist inter-symbol interference (ISI) criterion, linear modulation schemes like ASK and QAM—as well as spectrally-efficient variants of FSK and PSK—are modulated with shaped I and Q waveforms. The field of band-limited modulation is very complex, and an in-depth study of band-limited modulation is outside the scope of this thesis. However, the effects of band-limited modulation on VCO pulling can be clearly seen from Equation 5.16. If the I and Q waveforms are not rectangular pulses, the amplitude and phase of the transmitted waveform no longer change instantaneously with time, and the voltage across the varactors becomes

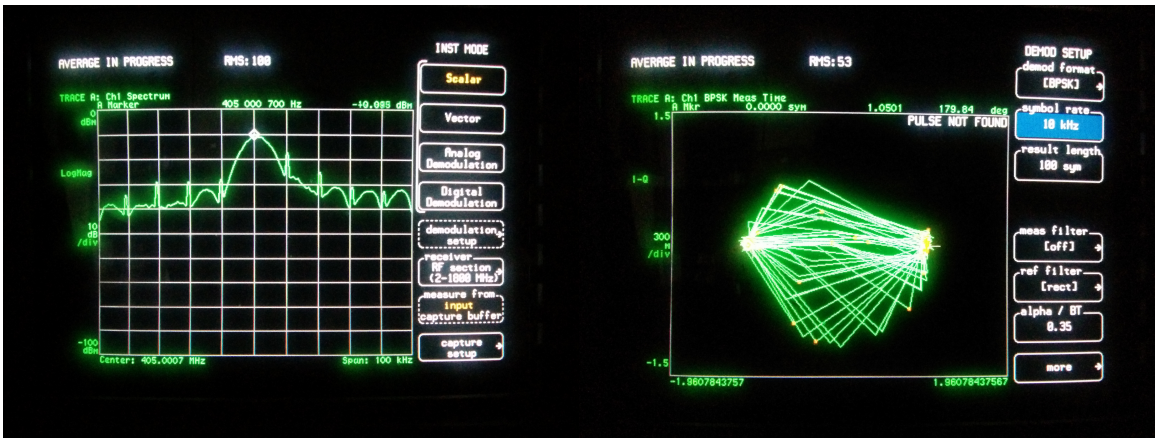
$$v(t) = A \cdot \cos(N \cdot \omega_0 t) + B + K(t) \cdot \cos(\omega_0 t + \theta + \phi(t)) \tag{5.16}$$

Since $K(t)$ and $\phi(t)$ vary with time, $v(t)$ is not constant over the entire symbol period, and the VCO will experience frequency pulling on each symbol transition. This implies that the microtransceiver would experience VCO pulling while transmitting band-limited BPSK, despite being able to transmit constant-envelope BPSK without experiencing pulling.

To validate the conclusion that band-limited modulation will produce VCO pulling, the microtransceiver was tested transmitting 10 kbps band-limited BPSK with the 100 mW PA. Because an arbitrary waveform generator capable of synthesizing phase-coherent band-limited I and Q data waveforms was not accessible, a simple shaped data waveform was synthesized by passing the PRBS output of the Agilent 33220A Function/Arbitrary Waveform Generator through a 10 kHz lowpass filter. Figure 5.3 compares the output spectrum and constellation of the microtransceiver transmitting band-limited BPSK. As predicted, severe frequency pulling was observed when transmitting band-limited BPSK.

5.3 Additional Coupling Paths

So far, this analysis has focused on frequency pulling due to magnetic coupling. However, an aggressor signal will pull the VCO according to the analysis in this chapter if it couples onto the varactors through any coupling mechanism, including electric field coupling, power supply ripple, and ground bounce. Only the value of K, the attenuation constant, and the phase offset in $v_a(t)$ are changed.



(a) 10 kbps band-limited BPSK spectrum. (b) 10 kbps band-limited BPSK constellation.

Figure 5.3: *Fab 5 10 kbps band-limited BPSK performance using the 100 mW PA.*

Metal-to-metal capacitance between large metal features, such as bond pads, power and ground traces, and inductor windings, can create unwanted coupling paths between aggressor circuits and the VCO. The top-metal synthesizer ground shield investigated in Chapter 3 is an example of one such potential coupling path. Fortunately, while some fringing-field capacitance between the PA and VCO inductors and the shield was present, the shield was not a significant coupling path. In addition to direct inductive and capacitive coupling paths, power supply disturbances and ground bounce must also be considered when mitigating VCO pulling. An aggressor signal present on the VCO supplies can potentially produce a common-mode disturbance on the varactors and cause frequency pulling. The susceptibility of VCO topologies to pulling from power supply and ground bounce is outside the scope of this thesis. However, designers can take steps to eliminate these problems from the start by following the system-level coupling mitigation strategies outlined in Chapter 2.

Chapter 6

Pulling Mitigation Strategies in Integrated Transceivers

The issue of frequency pulling due to output modulation extends from the system level to the circuit level and is affected by both the design and layout of the transceiver. This chapter distills the results of the analysis in Chapter 5 into system-level strategies for mitigating pulling. In addition to VCO operating frequency, several inductor topologies, including counterwound and non-counterwound VCO inductors, and a novel figure-8 inductor topology, are discussed.

6.1 Operating Frequency

Chapter 5 examined the relationship between PA output frequency, VCO frequency, and modulation to determine the susceptibilities of a VCO to pulling from aggressor signals with different modulation schemes. Chapter 5 concluded that if the amplitude, frequency, or phase of the aggressor signal were asynchronous with the VCO output, the average varactor voltage would vary with time, causing the VCO frequency to shift. This implies that amplitude-modulation schemes like QAM and ASK, as well as band-limited modulation, will always produce frequency pulling in a differential LC VCO.

However, Chapter 5 showed that if the aggressor signal is a constant-envelope phase modulated waveform, VCO pulling can be eliminated by choosing a VCO operating frequency and quadrature VCO divider ratio N so that Equation 5.15 is satisfied. This suggested that a VCO operating at $4\times$ output transmit frequency would be naturally immune to pulling from both BPSK and QPSK-modulated constant-envelope carrier waves.

6.1.1 Frequency Upconversion

While this thesis has focused on transceiver topologies where a divided VCO output is used to generate I and Q reference phases, it is useful to briefly consider frequency upconversion as a potential technique for mitigating oscillator pulling. In [10], a 2.4 GHz frequency-doubling PA was designed and fabricated in 0.18 μm CMOS. [10] explains that the frequency-doubled PA configuration was designed to prevent pulling from injection locking. While this claim is technically true, the microtransceiver's frequency-divided VCO is also immune to pulling from injection-locking simply by virtue of the fact that it does not operate near the output frequency of the PA.

The PA in [10] is very non-linear and is only suitable for transmitting constant-envelope modulation. In this case,

$$v_a(t) = \sin(N \cdot \omega_c t + \theta + \phi_i) \tag{6.1}$$

and Equation 5.10 becomes

$$v(t) = A \cdot \sin(\omega_c t) + B + K \cdot \sin(N \cdot \omega_c t + \theta + \phi_i) \tag{6.2}$$

Because the frequency of the aggressor signal is an integer multiple of the VCO operating frequency, $v_a(t)$ is always periodic over one period of $v(t)$. Therefore, the average varactor capacitance will remain constant for any ϕ_i, regardless of the value of N or the number of symbols in the constellation. A transmitter with internal frequency doubling like the one described in [10] could transmit any constant-envelope phase modulation scheme without producing pulling in the VCO.

Frequency upconversion appears to be a simple solution to prevent frequency pulling without having to implement custom inductors or increase the VCO operating frequency. However, it presents additional challenges to designers seeking to mitigate magnetic coupling. [10] acknowledges that frequency multipliers generate harmonics, which may couple into the VCO and PA and produce mixing spurs. Additionally, frequency multipliers with integrated inductors will interact with other magnetically-resonant circuits, including the VCO and PA, adding another dimension to the complex interactions of multiple integrated inductors. Further research into on-chip frequency upconversion techniques and their susceptibility to magnetic coupling is required before the effectiveness of this technique at mitigating LO pulling can be assessed.

6.2 Inductor Counterwinding

During the original design of the microtransceiver, the VCO inductors were counterwound so that an external B-field would produce a common-mode disturbance on the VCO outputs. Since the differential VCO is naturally insensitive to common-mode disturbances, it was thought that this would make the VCO less sensitive to pulling. Figure 6.1 illustrates both counterwound and non-counterwound VCO inductor arrangements.

Counterwinding the VCO inductors relative to the aggressor inductor produces a common-mode disturbance on the VCO outputs, which therefore produces a common-mode disturbance on the varactors. Let $v(t)$ and $\overline{v}(t)$ denote the varactor voltages on the non-inverting and inverting sides of the LC tank, respectively. From Equation 5.4, $v(t)$ and $\overline{v}(t)$ are given by

$$\begin{aligned} v(t) &= A \cdot \sin(\omega_c t) + B + K \cdot v_a(t) \\ \overline{v}(t) &= -A \cdot \sin(\omega_c t) + B + K \cdot v_a(t) \end{aligned} \tag{6.3}$$

As the voltage across one varactor increases, the voltage across the other varactor decreases. This implies that an aggressor signal $v_a(t)$ coupling into counterwound VCO inductors will cause the left and right varactor capacitances to change in opposite directions. Since the tank capacitance is asymmetrical, the VCO can be simplified to the full-resonant circuit in Figure 4.5. Let $C_{v_{left}}$ and $C_{v_{right}}$ be the average varactor capacitances on the left and right sides of the LC tank, each with normal average capacitance $C_{v_{avg}}$ If a given aggressor signal $v_a(t)$ produces a change ΔC_v in average varactor capacitance,

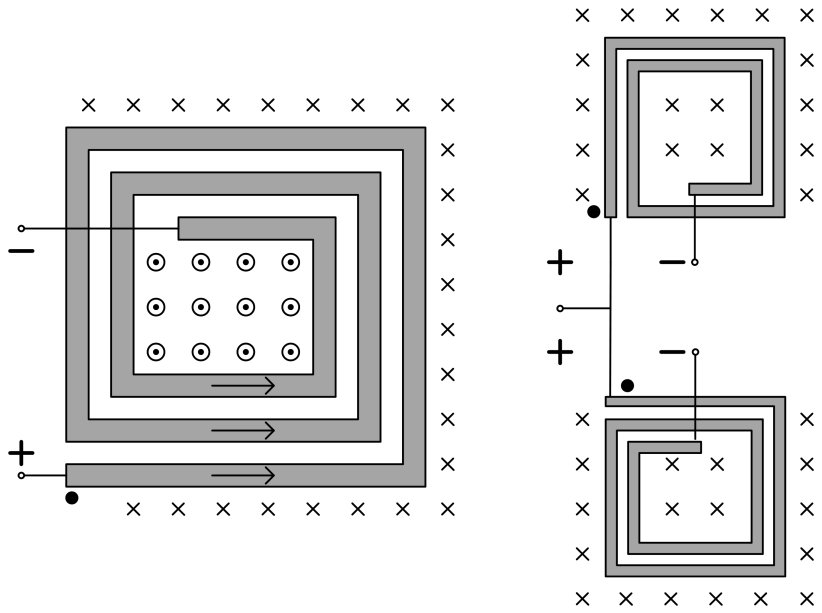
$$\begin{aligned} C_{v_{left}} &= C_{v_{avg}} - \Delta C_v \\ C_{v_{right}} &= C_{v_{avg}} + \Delta C_v \end{aligned} \tag{6.4}$$

From Figure 4.5 and Equation 4.3, the frequency of oscillation of a VCO with counterwound inductors is given by

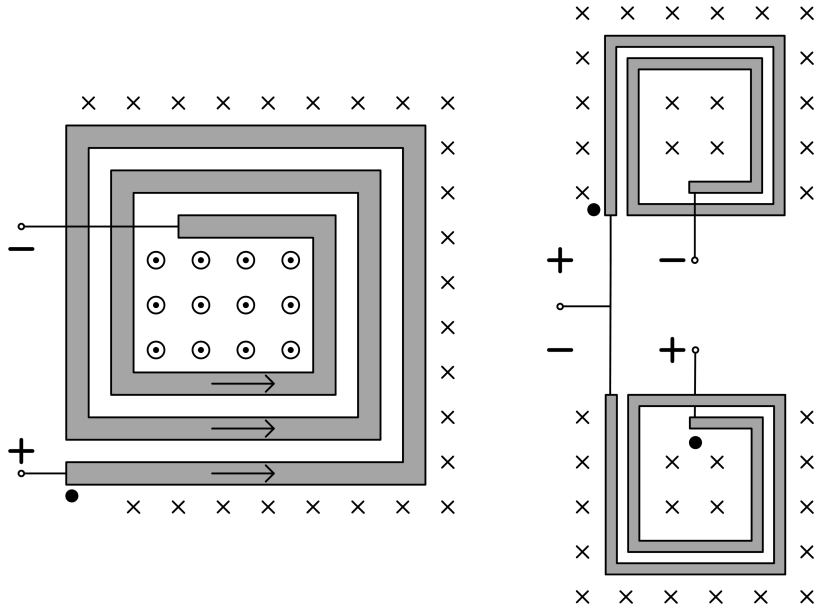
$$\omega_c^2 = \frac{1}{2L}\left(\frac{1}{C + C_{v_a vg} + \Delta C_v} + \frac{1}{C + C_{v_a vg} - \Delta C_v}\right) \tag{6.5}$$

which simplifies to

$$\omega_c^2 = \frac{1}{2L}\left(\frac{2(C + C_{v_{avg}})}{(C + C_{v_{avg}})^2 - (\Delta C_v)^2}\right) \tag{6.6}$$



(a) Counterwound VCO inductors.



(b) Non-counterwound VCO inductors.

Figure 6.1: *Illustration of counterwound and non-counterwound VCO inductors.*

Therefore, for counterwound VCO inductors,

$$\omega_c^2 \propto \frac{1}{(\Delta C_v)^2} \tag{6.7}$$

For non-counterwound VCO inductors, the aggressor signal produces a differential disturbance on the VCO outputs.

$$\begin{aligned} v(t) &= A \cdot \sin(\omega_c t) + B + K \cdot v_a(t) \\ \overline{v}(t) &= -A \cdot \sin(\omega_c t) + B - K \cdot v_a(t) \end{aligned} \tag{6.8}$$

Because $v_a(t)$ and $v_{out}(t)$ have the same sign, the varactor capacitances on both sides of the tank will both change in the same direction. For a given $v_a(t)$, both capacitances will either increase or decrease together. This means that the capacitance on both sides of the LC tank is symmetric, and the VCO's frequency of oscillation is given by

$$\omega_c^2 = \frac{1}{L}\left(\frac{1}{C + C_{v_{avg}} + \Delta C_v}\right) \tag{6.9}$$

Therefore, for counterwound VCO inductors,

$$\omega_c^2 \propto \frac{1}{\Delta C_v} \tag{6.10}$$

Comparing Equations 6.7 and 6.10 suggests that, a VCO with counterwound inductors will experience a smaller change in frequency—and therefore less severe frequency pulling—than a VCO without counterwound inductors for the same $v_a(t)$. Using extracted capacitance and inductance values, Figure 6.2 plots the simulated change in output frequency for a change in varactor capacitance for Fab 5 VCOs with both counterwound and non-counterwound inductors.

To validate the advantage of counterwound VCO inductors, the ADS Momentum layout used to simulate inductor coupling coefficients in Chapter 3 was modified so that the VCO inductors were no longer counterwound, and a new 8-port network of inductor S-parameters was extracted. The microtransceiver was again simulated running open-loop while transmitting BPSK and RC-BPSK with and without counterwound VCO inductors. With counterwound inductors, transitioning between QPSK symbols produced a Δf of 80 kHz. Without counterwound VCO inductors, however, changing between adjacent QPSK symbols produced a Δf of 1.3 MHz. This is consistent with the mathematical analysis and validates the assumption made during the microtransceiver's original design.

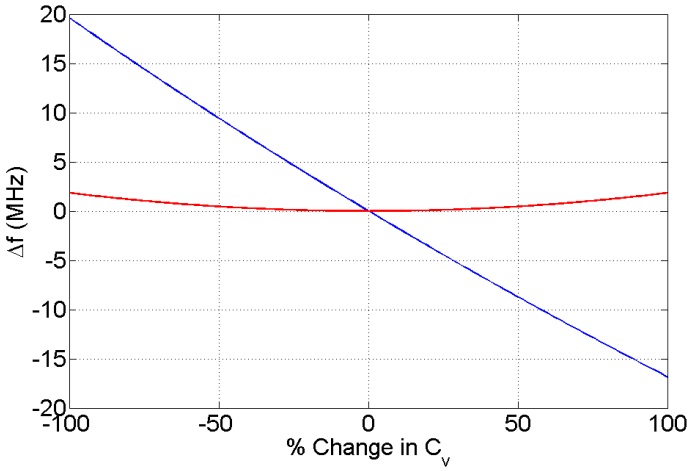


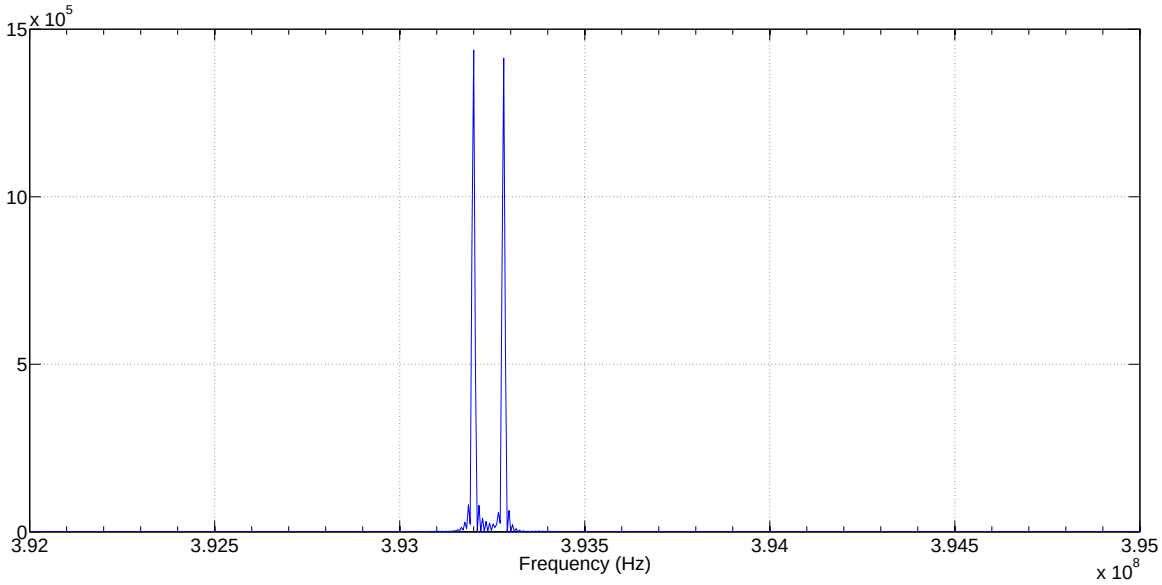
Figure 6.2: *Simulated change in Fab 5 output frequency versus change in varactor capacitance withVCO inductors.*

6.3 Figure-8 Inductors

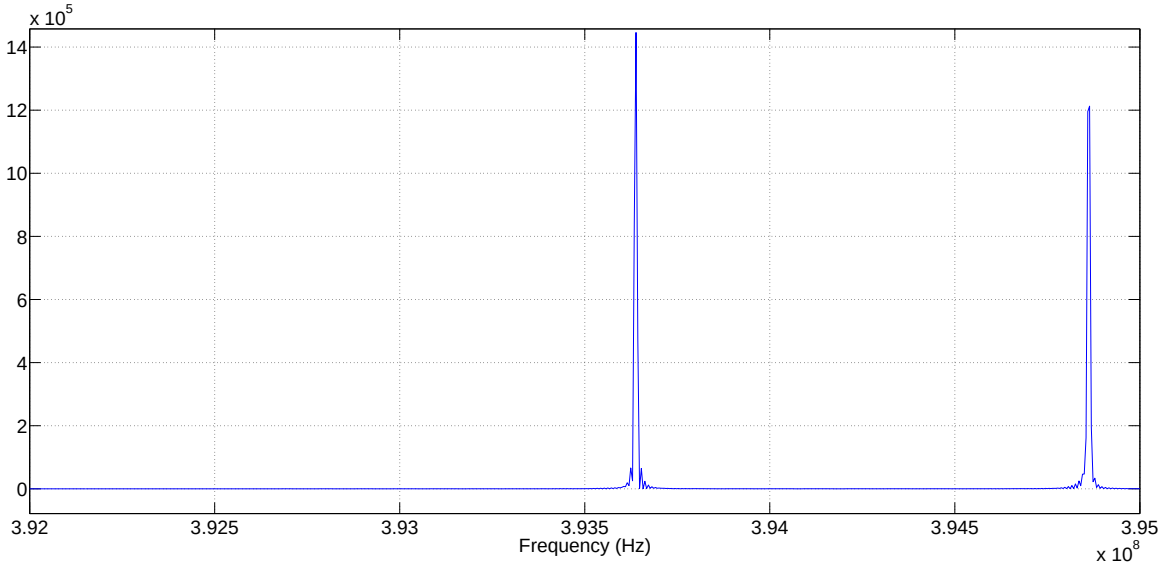
While counterwound VCO inductors help reduce pulling from an on-chip PA, they cannot eliminate it. Planar spiral inductors can be oriented to cancel either common-mode or differential induced voltages, but not both. However, a figure-8 inductor topology, illustrated in 6.4a, will experience no common-mode or differential induced voltage from an external B-field. The figure-8 inductor can be considered as a set of four series-connected inductors with opposite orientations. When subjected to a uniform external B-field, the induced voltages cancel, producing no net induced voltage across the inductor terminals. In the same manner, a current flowing in the figure-8 inductor produces B-fields with opposite directions in each half of the coil. The flux in the top and bottom halves of the coil boost each other, increasing the effective inductance of the inductor. This means that a figure-8 inductor will induce no net B-field along its axis of symmetry.

The B-field immunity of the figure-8 inductor topology has been demonstrated in [20], who utilize this property to make a 2.4-to-5.3 GHz dual-core VCO in 65 nm CMOS. The dual-core VCO uses two VCOs to cover the entire tuning range; by overlaying two VCOs with figure-8 inductors, placing the smaller inductor inside the larger inductor along its axis of symmetry. The B-field immunity of the figure-8 inductor allows both VCOs to operate simultaneously without interference, with only a slight reduction in inductor Q caused by minor layout mismatches and capacitive coupling between the two inductors [20].

A 14 nH figure-8 inductor, shown in Figure 6.5 was developed as part of an effort

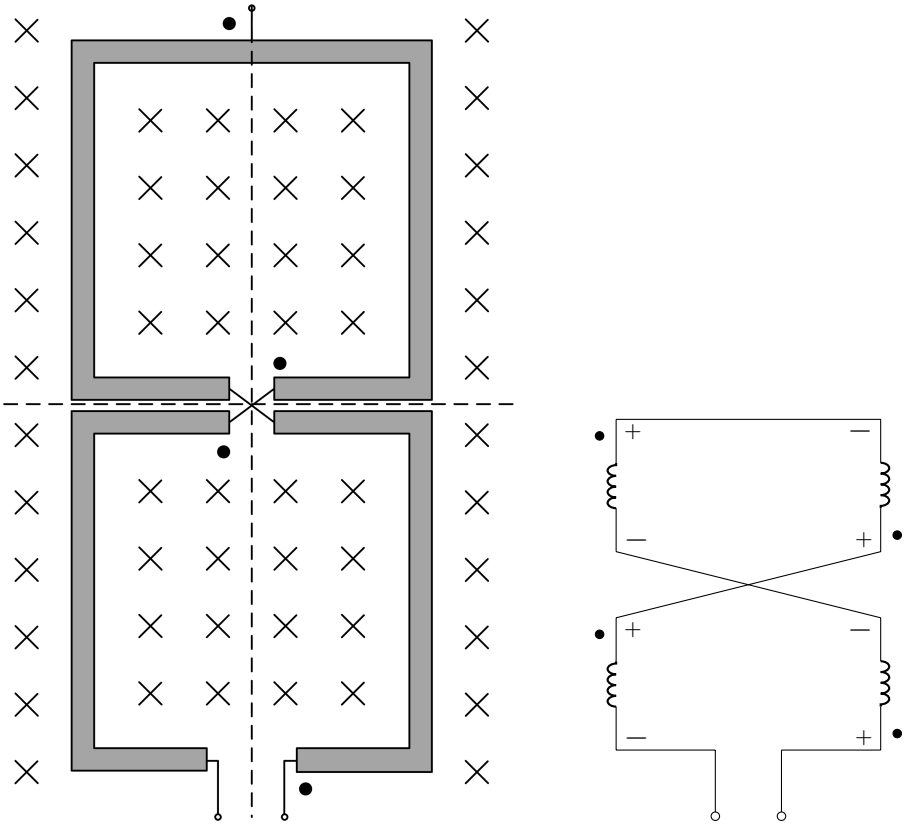


(a) 10 kbps RC-BPSK with counterwound VCO inductors. $\Delta f = 80\,\text{kHz}$



(b) 10 kbps RC-BPSK without counterwound VCO inductors. $\Delta f = 1.3\,\text{MHz}$

Figure 6.3: *Simulated Fab 5 open-loop RC-BPSK output frequency with counterwound (red) and non-counterwound (blue) VCO inductors.*



(a) *Figure-8 inductor in a uniform B-field.* (b) *Equivalent schematic.*

Figure 6.4: *Illustration of the figure-8 inductor topology.*

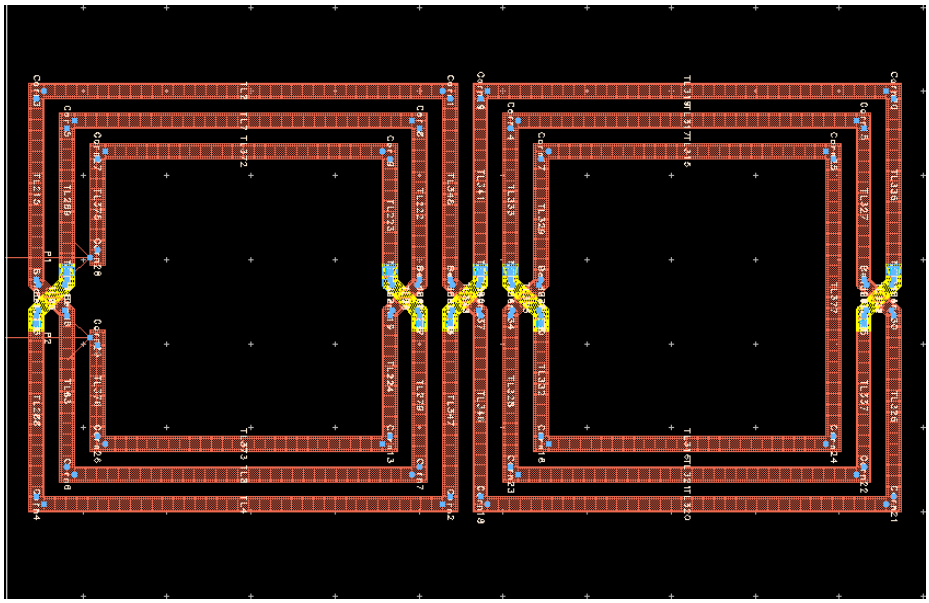
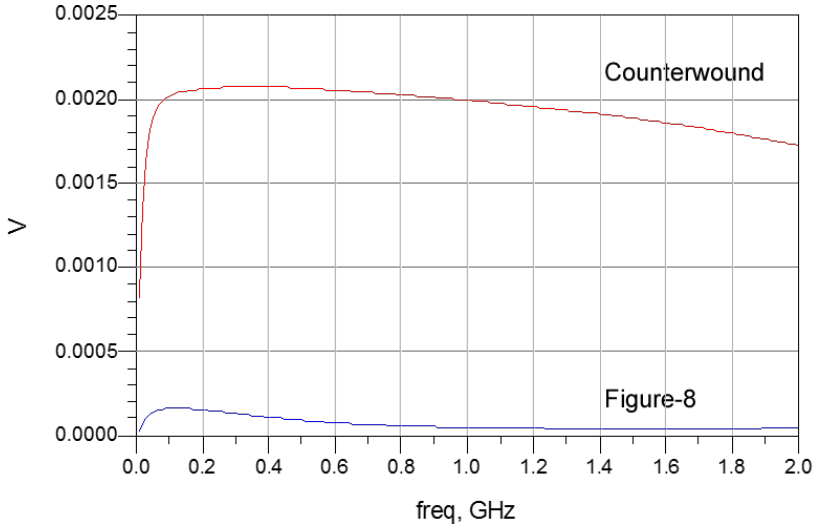


Figure 6.5: *Layout of a 14 nH figure-8 inductor designed for a 4× microtransceiver VCO.*

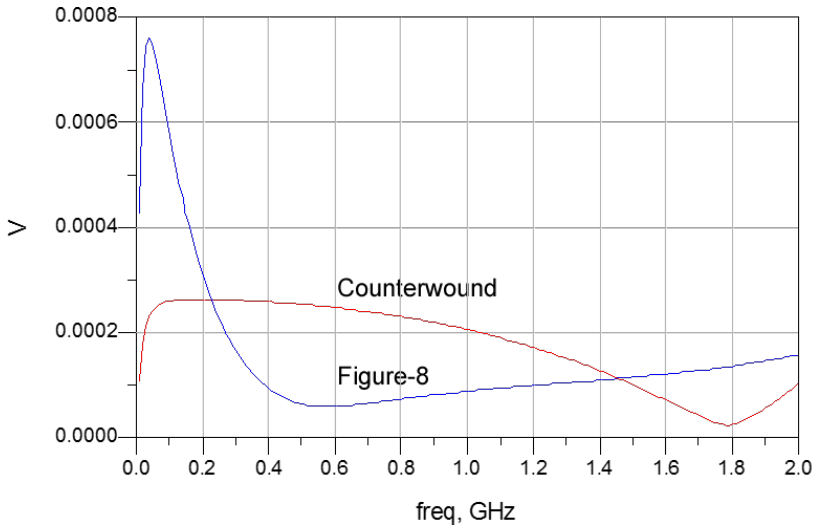
to design a 4× VCO for the K-State Microtransceiver. It was necessary to wind additional turns inside each half to achieve the large inductance required for operation at 1.4-2.0 GHz in the existing Fab 5 layout area. The 14 nH center-tapped figure-8 inductor was simulated in Agilent ADS and found to have a self-resonant frequency of 3.6 GHz and a simulated Q of 18 at 2.0 GHz.

To confirm that the figure-8 inductor topology would cancel both common-mode and differential disturbances on the varactors and thereby eliminate VCO pulling in the K-State Microtransceiver, the 14 nH figure-8 inductor was simulated in ADS Momentum in place of the existing Fab 5 VCO inductor network. Figure 6.6 compares the common-mode and differential voltages induced in the VCO inductor by the PA for the counterwound Fab 5 inductors and the new figure-8 inductor. At 420 MHz, the 100 mW PA induced a 100 μV common-mode voltage and an 80 μV differential voltage across the terminals of the figure-8 inductor, compared to a 2 mV common-mode voltage and an 200 μV differential voltage across the terminals of the Fab 5 counterwound inductor network—increasing common-mode and differential disturbance rejection by factors of 20 and 2, respectively.

While the 14 nH figure-8 inductor designed in this thesis was not implemented in the most recent revision of the microtransceiver discussed in Chapter 8 (Rev 6b), it demonstrated that the figure-8 topology eliminates frequency pulling by canceling both differential and common-mode induced voltages. The figure-8 inductor will likely be used in conjunction with a 4× VCO in future versions of the microtransceiver to



(a) *Common-mode voltage induced by 100 mW PA output.*



(b) *Differential voltage induced by 100 mW PA output.*

Figure 6.6: *Comparison of common-mode and differential voltages induced in counterwound and figure-8 VCO inductors by the 100 mW PA output.*

provide maximum isolation between the PA and VCO while enabling the radio to transmit both constant-envelope and band-limited modulation.

6.4 PA Topology

If the designer is unable to implement any of the pulling mitigation strategies outlined in this chapter, and the transceiver is required to use a modulation scheme that will produce pulling in the VCO, the designer must consider moving the integrated PA inductor off-chip to increase the separation between the PA and VCO inductors. In Chapter 8, a revision of the K-State Microtransceiver designed to allow the Class-C PA to use an external chip inductor to eliminate coupling between the PA and VCO is discussed. Alternatively, an inductorless PA topology could be implemented to eliminate magnetic coupling between the PA and VCO altogether.

6.5 Summary

This chapter identified several strategies to mitigate VCO pulling due to magnetic coupling. First, if the aggressor signal responsible for frequency pulling is a constant-envelope phase modulated waveform, VCO pulling can be eliminated by choosing a VCO operating frequency and quadrature VCO divider ratio N so that Equation 5.15 is satisfied. In the case of the microtransceiver, this suggested that a VCO operating at 4× output transmit frequency would be naturally immune to pulling from both BPSK and QPSK-modulated carrier waves. Frequency upconversion also appears to prevent pulling from all constant-envelope phase modulation schemes, regardless of the VCO operating frequency or the number of symbols in the constellation. However, the challenges associated with on-chip frequency upconversion require further study before this technique can be advocated as a way to mitigate frequency pulling.

Designers can also manipulate the inductors in the PA or VCO to mitigate pulling. Counterwinding the VCO inductors to produce a differential disturbance on the varactors has been shown to reduce frequency pulling, confirming an assumption made during the original design of the microtransceiver. If the designer is able to implement custom inductors, the figure-8 topology in [20] can be implemented in the VCO and/or the PA to create an inductor that is relatively immune to external B-fields, potentially enabling the use of amplitude modulation and band-limited modulation in fully-integrated transceivers. A 14 nH figure-8 inductor designed for a potential 4× version of the microtransceiver VCO was shown to reduce the common-mode and

differential voltages induced on the VCO outputs by the 100 mW PA by factors of 20 and 2, respectively, compared to the microtransceiver's current counterwound inductors. Finally, moving the PA inductor off-chip or implementing an inductorless PA should be considered if none of the other pulling mitigation strategies in this chapter are feasible.

Chapter 7

Design of a Prototype 2×/4× VCO QPSK Transmitter IC

According to the analysis in Chapter 5, a VCO operating at four times the output transmit frequency would be immune to pulling from constant-envelope BPSK and QPSK-modulated carrier waves. To test this theory, a prototype IC containing a pair of QPSK transmitters was designed and fabricated in 0.18 μm SOI. The transmitters—one utilizing a 2× VCO, one utilizing a 4× VCO—consisted of a differential LC VCO, an integer-N synthesizer, an IQ modulator, an exponential-horn pad driver, and an integrated class-C PA. This chapter discusses the design and measurements of the prototype 2×/4× transmitter IC.

7.1 Transmitter Architecture

Figure 7.2 is a block diagram of the 2×/4× VCO QPSK transmitter IC. The transmitters use a differential LC VCO operating at either twice or four times the output transmit frequency. Quadrature dividers are used to generate differential I and Q signals for modulation, and a simple integer-N synthesizer with fixed N and R divider ratios is used to synthesize a fixed output transmit frequency of 432 MHz using an off-chip 27 MHz reference. Each transmitter has an 2 mW exponential-horn pad driver, and an integrated class-C PA positioned to deliberately couple back into the VCO.

Substrate and electric field coupling mitigation strategies in [8] were utilized extensively to ensure that magnetic coupling was the dominant coupling path between the PA and VCO. Transistors, resistors, and MIM capacitors were surrounded with substrate contact guard rings, and deep trench grids were used at all levels to isolate

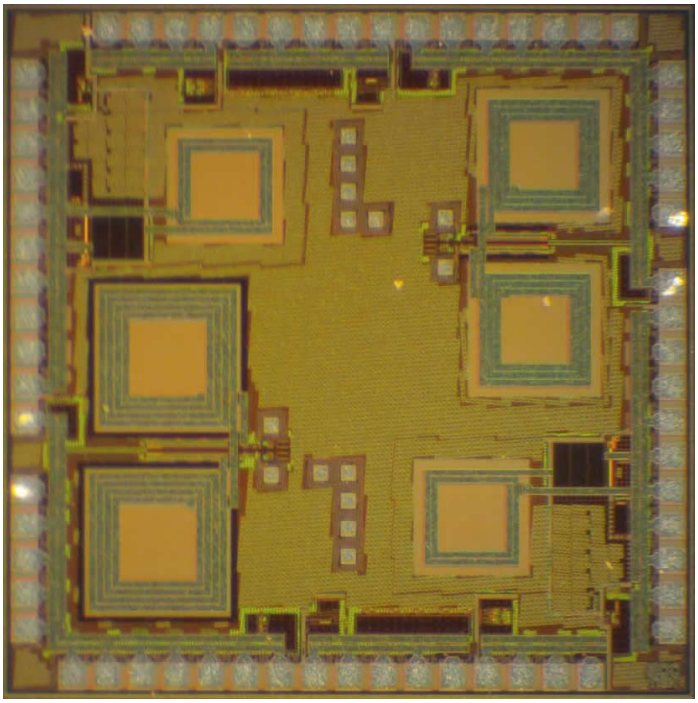


Figure 7.1: *2×/4× VCO QPSK transmitter IC die photograph.*

devices, sub-circuits, and power and ground domains. Deep-trench grids were also added under integrated inductors to reduce eddy-current loss and increase inductor Q. Additionally, on-chip bypass capacitance was used to reduce power supply ripple in the charge pump, frequency synthesizer, IQ modulator, and class-C PA. A custom 1 pF MIM-capacitor cell with integrated power and ground busses was arrayed throughout the transceiver to provide on-chip decoupling and increase metal fill density in empty areas of the chip.

7.1.1 2× and 4× VCOs

Both the 2× and 4× LO utilize the cross-coupled LC VCO topology shown in Figure 4.1. Like the microtransceiver, coarse frequency tuning is performed by a bank of 15 switched MIM capacitors, and analog frequency tuning is performed by an array of I-MOS varactors. Both tuning capacitances were sized so that both VCOs would have approximately the same K_v as the VCO in the K-State Microtransceiver while still tuning over the entire 390-450 MHz band. D-latch based quadrature frequency dividers are used to generate differential divided I and Q outputs to drive the frequency synthesizer and IQ modulator.

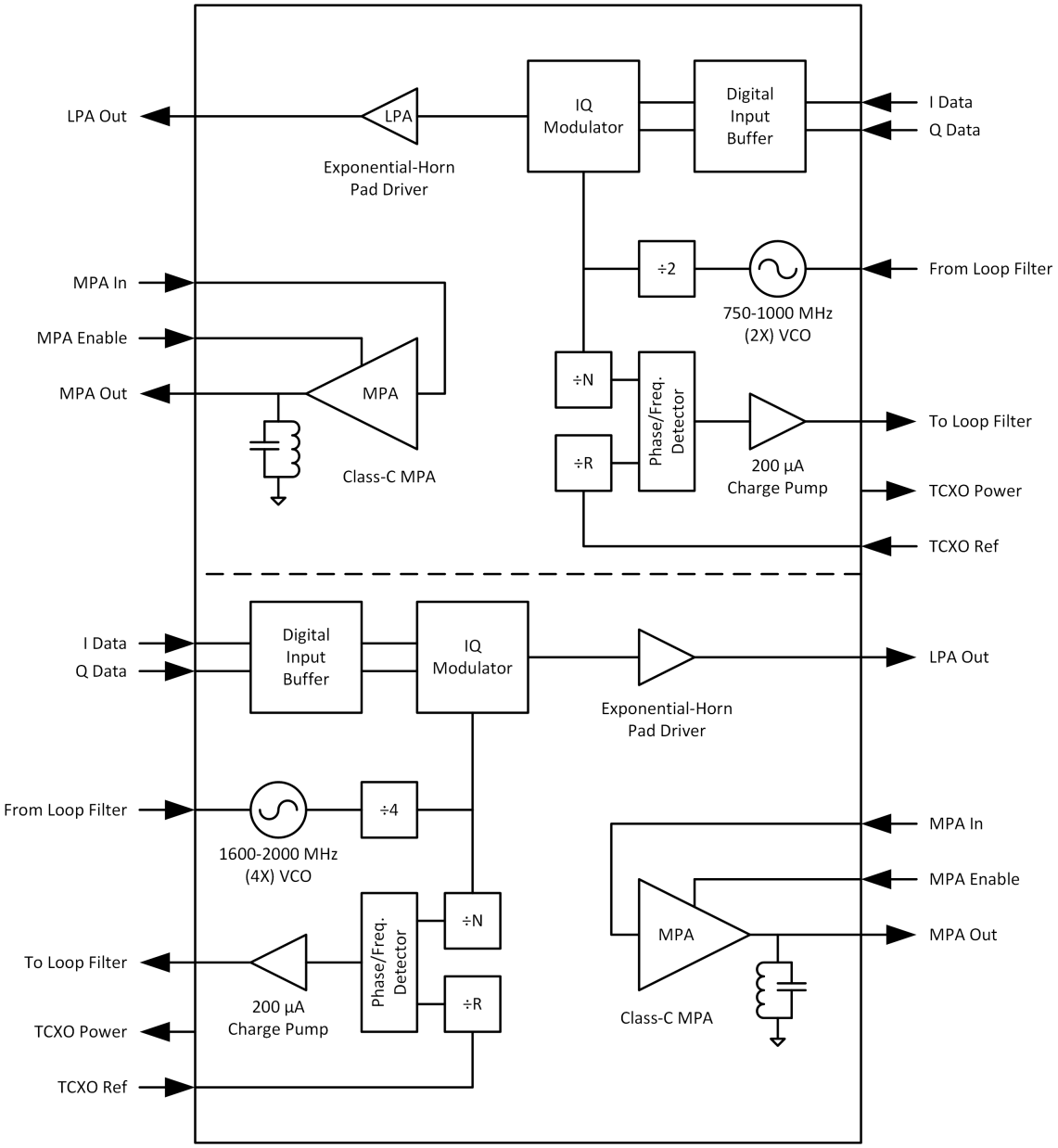


Figure 7.2: *Block diagram of the 2×/4× QPSK transmitter test chip.*

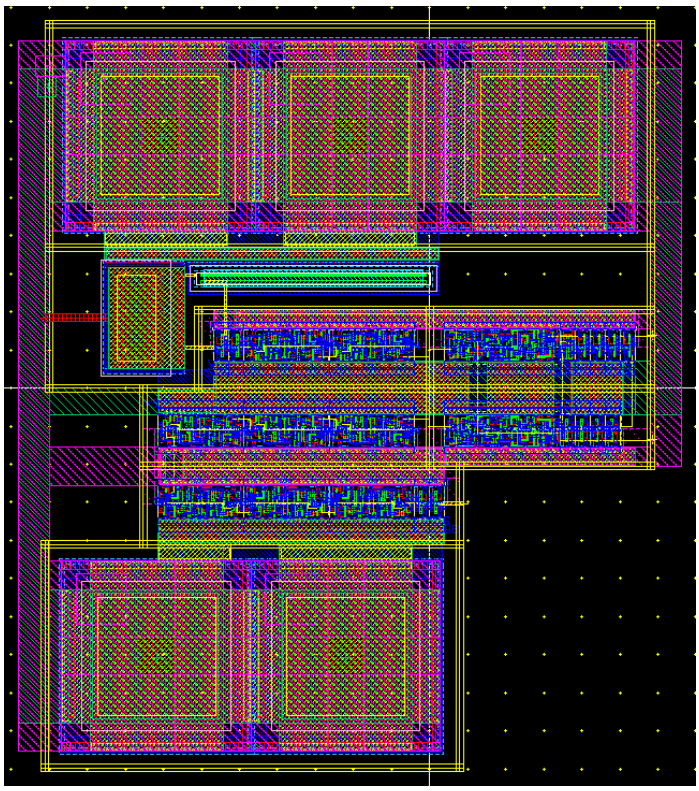


Figure 7.3: *Integer-N frequency synthesizer layout*

7.1.2 Frequency Synthesizer

An integer-N frequency synthesizer with fixed divider ratios was implemented using standard-cell digital logic. The synthesizer operates at a divided reference frequency of 6.75 MHz (compared to 4.8 MHz in the K-State Microtransceiver) using an external 27 MHz reference oscillator and fixed N and R values of 64 and 4, respectively. Both the N and R dividers are D-flip-flop ripple counters. To prevent board-level return current interference from injecting noise into the reference oscillator, power and ground for the TCXO are supplied from the transceiver.

A simple 200 μA current-mirror charge pump was implemented in the frequency synthesizer. The charge pump consists of a PMOS current source and an NMOS current sink, switched by up and down tuning lines from the phase/frequency detector to source/sink current to/from the loop filter. Because of its current-mirror topology, the charge pump output current is a strong function of supply voltage, and the charge pump can only drive the loop filter voltage to within one threshold voltage of either rail. Figure 7.4 shows the layout of the charge pump and its on-chip bypass capacitance.

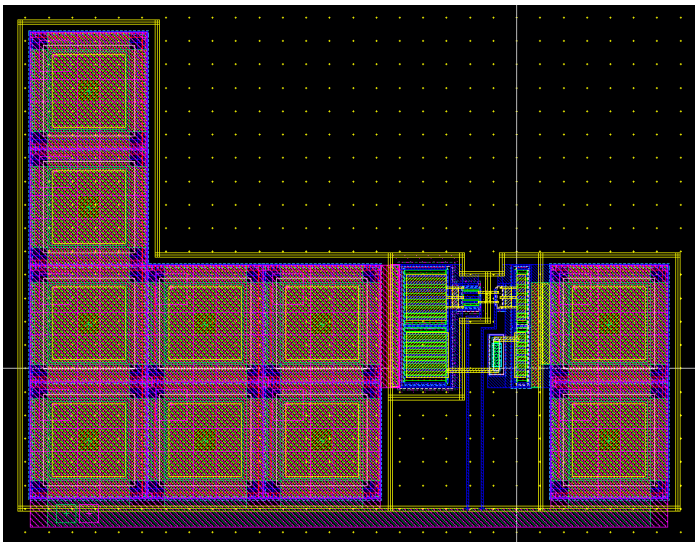


Figure 7.4: *200 μA charge pump layout.*

7.1.3 I/Q Modulator

The differential I/Q modulator, shown in Figure 7.5, is created from two Gilbert-cell mixers driven by the differential I and Q outputs of the VCO. The outputs of each mixer are additively combined to form the final I/Q-modulated output waveform. I and Q data inputs are digitally buffered on-chip.

7.1.4 Exponential-Horn Pad Driver

Because the 2×/4× IC had no output power requirements and operated on a relatively low-voltage supply, a lower-power 2 mW exponential-horn pad driver was designed instead of a 10 mW PA. The pad driver, shown in Figure 7.6, is sized so that the on-resistance of the output stage is matched to 50 Ω. The 900 mV output is sufficient to observe the modulated signal and drive the input of the Class-C PA. In bench testing, the 2 mW pad driver delivers a measured +3 dBm into 50 Ω.

7.1.5 Class-C Power Amplifier

The class-C power amplifier, shown in Figure 7.7 was designed to closely match the characteristics of the PA in the K-State Microtransceiver. Because the 0.18 μm SOI process had a supply voltage of 1.8 V, it was impossible to design an identical 100 mW class-C PA due to lower FET breakdown voltages and a lower output voltage swing. Instead, the PA was designed to provide the same peak switching current as the microtransceiver PA—100 mA—in order to produce the same $^{di(t)}/_{dt}$ in the PA

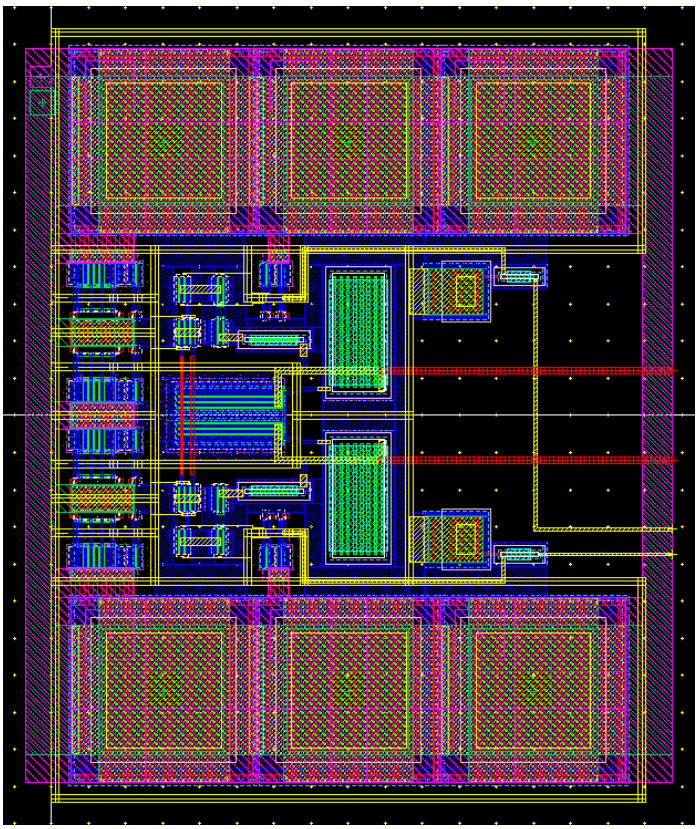


Figure 7.5: *I/Q modulator layout.*

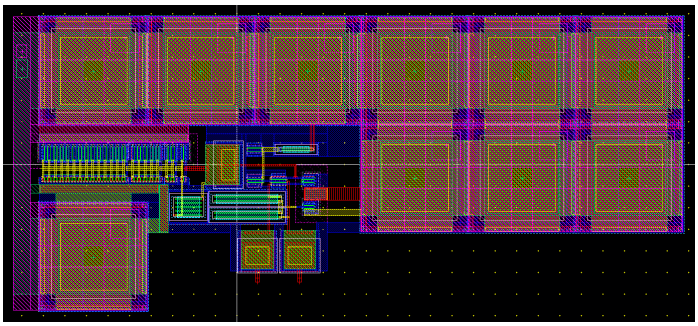


Figure 7.6: *10 mW PA layout.*

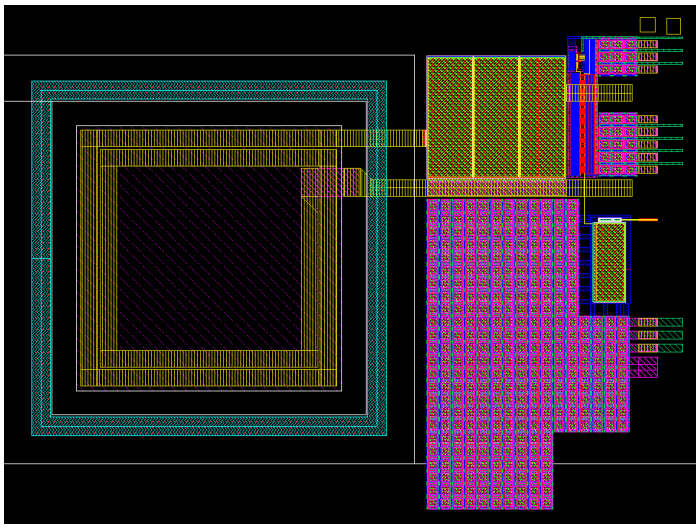


Figure 7.7: *100 mW PA layout.*

inductor. Output matching and current upconversion are performed by the 10 nH series output bondwire inductance and a 15 pF shunt capacitor. The class-C PA has a simulated output voltage swing of nearly 2 V. However, due to poor output matching, the PA only delivers a measured +7 dBm into 50 Ω.

Figure 7.8 shows the top-level layout of the 2×/4× VCO transmitter test chip. The transmitters are laid out in a mirrored fashion so that the chip has 180° rotational symmetry.

7.2 Performance

Both transmitters were first tested using the circuit board shown in Figure 7.9a. During testing, the D-latch-based frequency dividers were found to oscillate at the nominal supply voltage of 1.8 V. Reducing the supply voltage to 1.7 V allowed the dividers to operate without oscillating. However, since the entire chip was powered from the same board-level supply, reducing the supply voltage also reduced the VCO tuning gain, charge pump gain, the amplitude of the reference oscillator signal, and the output power of the class-C PA. This made it difficult for the frequency synthesizer to lock at certain VCO tuning codes. A second test board, shown in Figure 7.9b, was designed to bring each on-chip power domain out to a separate header. By configuring the frequency synthesizer to operate at 1.7 V and the rest of the chip at 1.8 V. the frequency synthesizer locks reliably each time.

Figure 7.10 compares the 2× VCO's 10 kbps BPSK and RC-BPSK performance using the exponential-horn pad driver. Like the microtransceiver, the transmitter

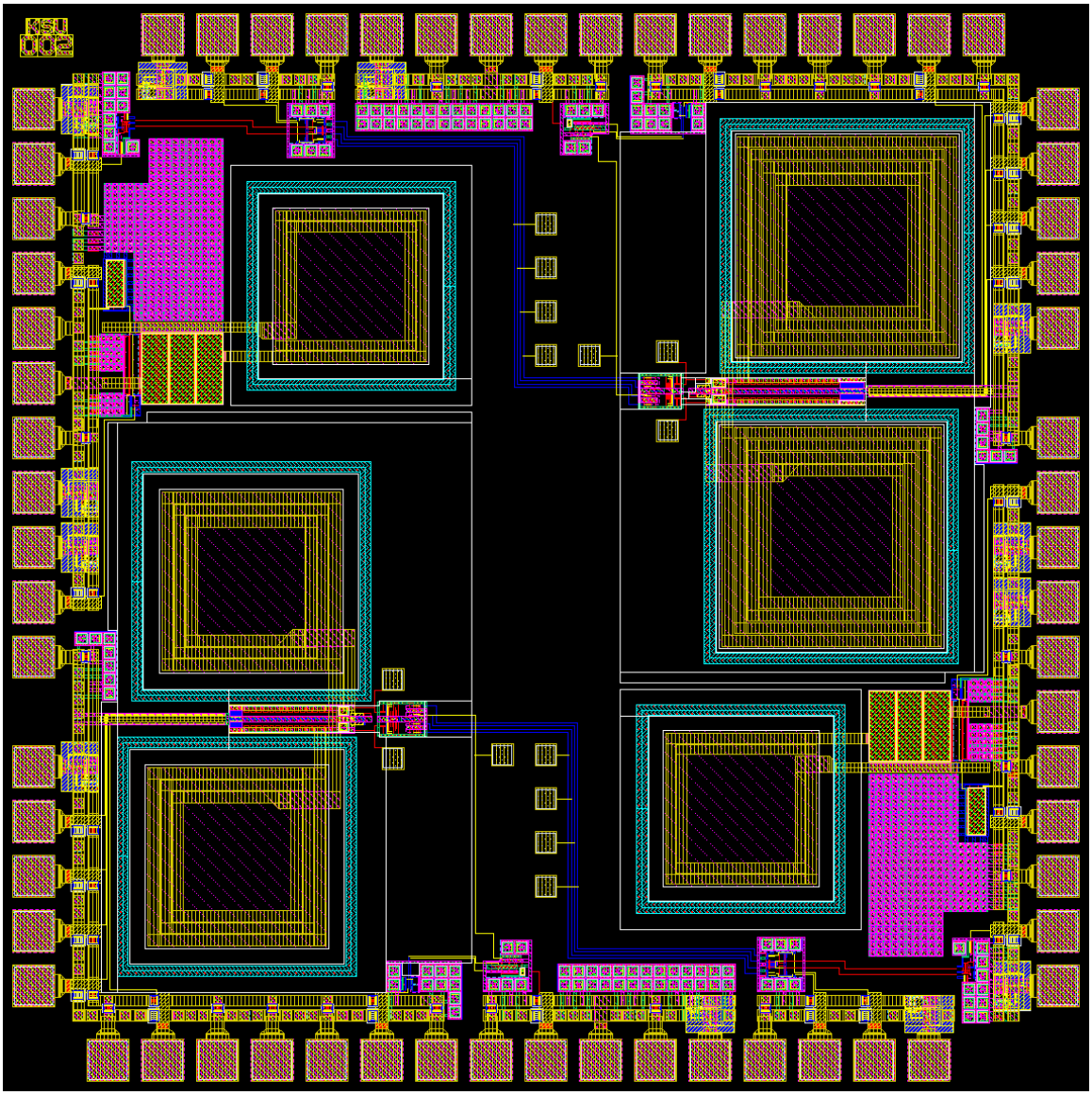
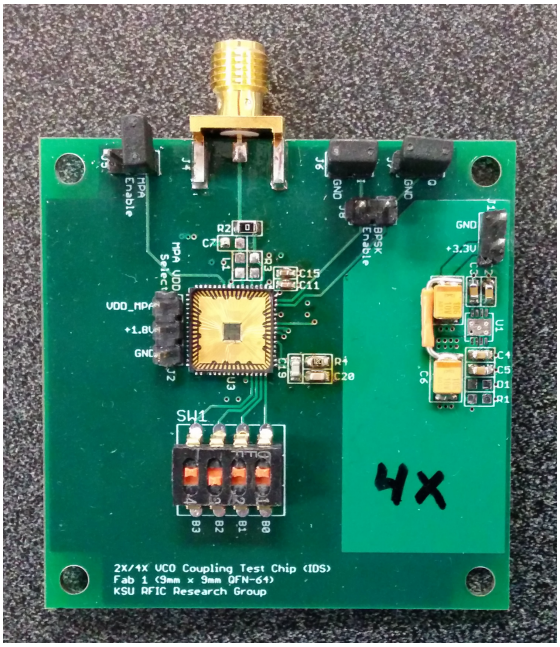
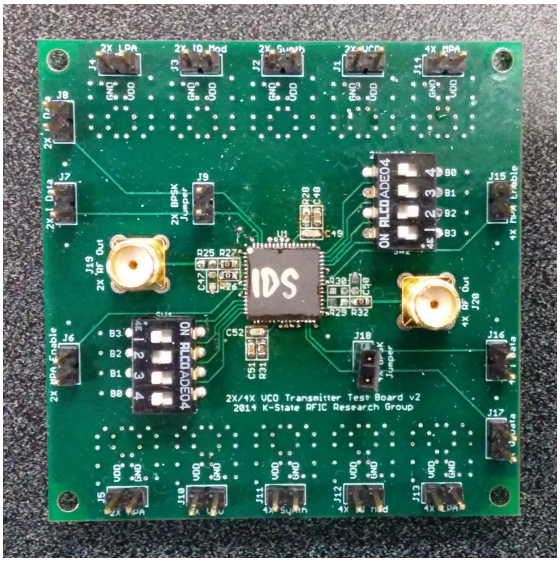


Figure 7.8: *2×/4× VCO QPSK transmitter IC top-level layout.*



(a) *Revision 1*



(b) *Revision 2*

Figure 7.9: 2×/4× VCO transmitter IC test boards.

with the 2× VCO does not experience pulling with either modulation scheme when the class-C PA is not in use.

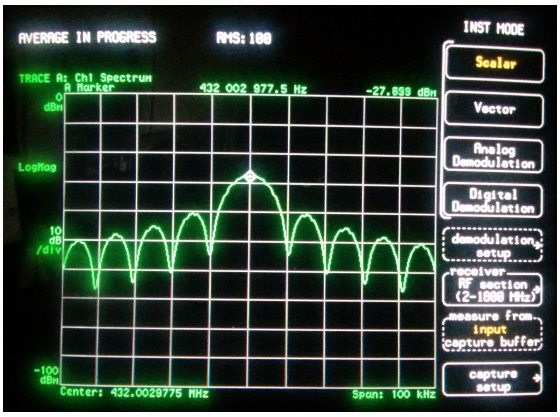
Figure 7.11 compares the 4× VCO's 10 kbps BPSK and RC-BPSK performance using the exponential-horn pad driver. As expected, the transmitter with the 4× VCO does not experience pulling with either modulation scheme when the class-C PA is not in use.

Figure 7.12 compares the 2× VCO's 10 kbps BPSK and RC-BPSK performance using the class-C PA. As expected, the transmitter with the 2× VCO experiences moderate pulling while transmitting RC-BPSK, but its BPSK performance is not affected.

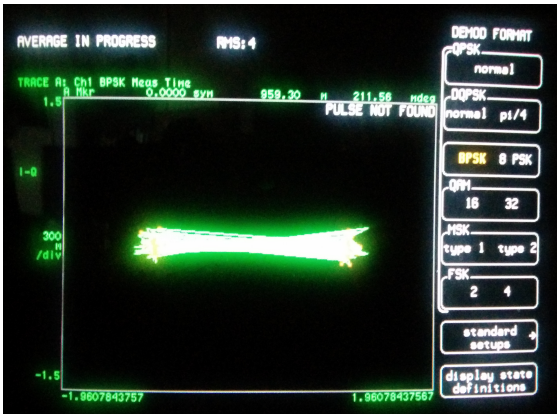
Figure 7.13 compares the 4× VCO's 10 kbps BPSK and RC-BPSK performance using the class-C PA. The transmitter with the 4× VCO is able to transmit RC-BPSK, and therefore QPSK, without pulling, thereby confirming the analysis in Chapter 5.

7.3 Summary

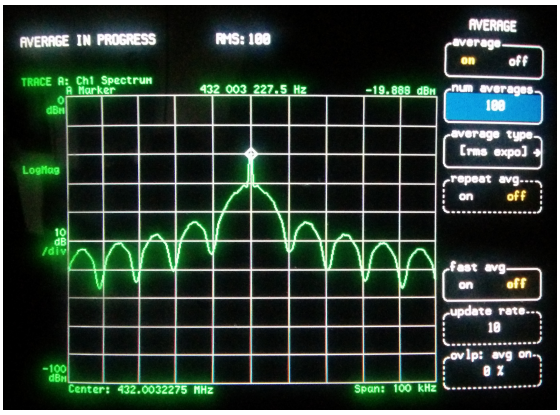
A prototype IC containing a pair of QPSK transmitters—one utilizing a 2× VCO, one utilizing a 4× VCO—was designed and fabricated in 0.18 μm SOI to verify whether or not a transmitter with a 4× VCO is immune to pulling from QPSK-modulated carrier



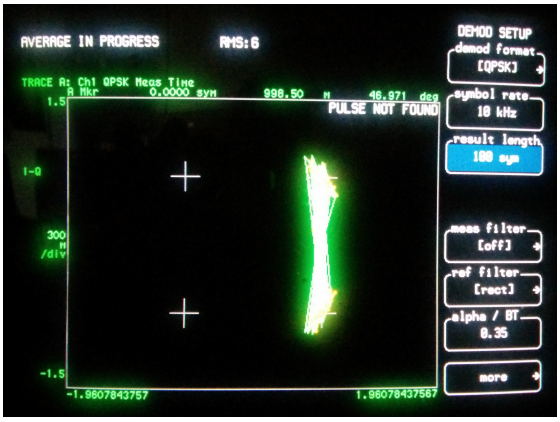
(a) *10 kbps BPSK spectrum.*



(b) *10 kbps BPSK constellation.*

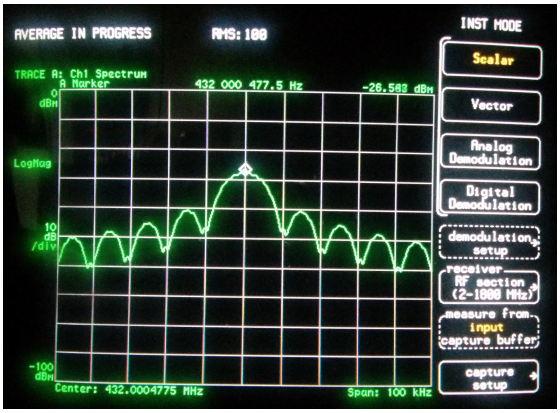


(c) *10 kbps RC-BPSK spectrum.*

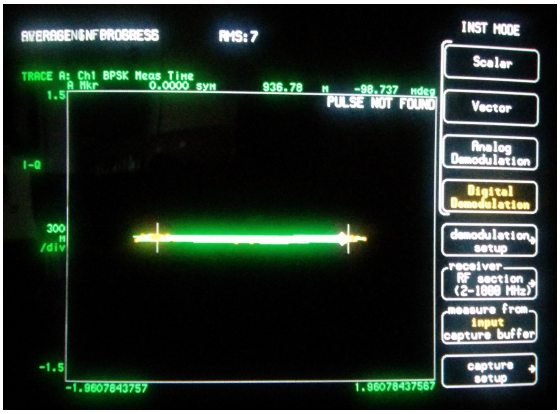


(d) *10 kbps RC-BPSK constellation.*

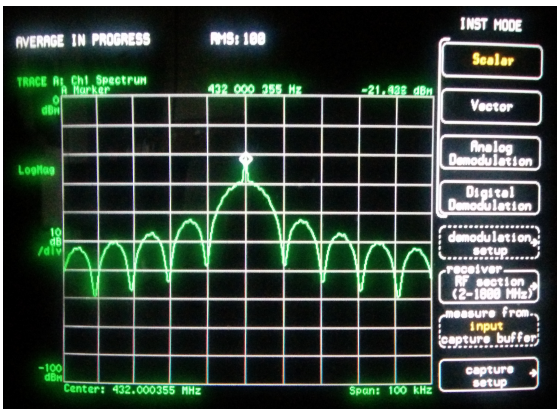
Figure 7.10: *2× VCO BPSK and RC-BPSK performance at 10 kbps using the transmitter's exponential-horn pad driver.*



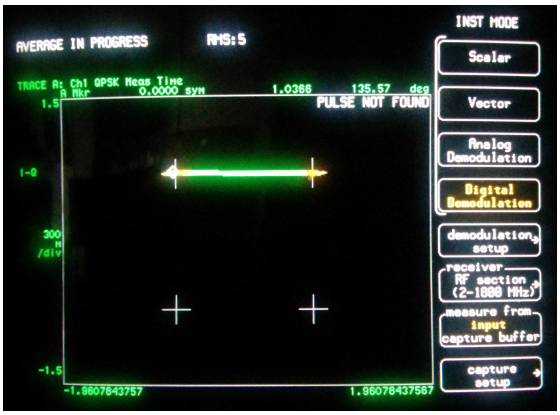
(a) *10 kbps BPSK spectrum.*



(b) *10 kbps BPSK constellation.*

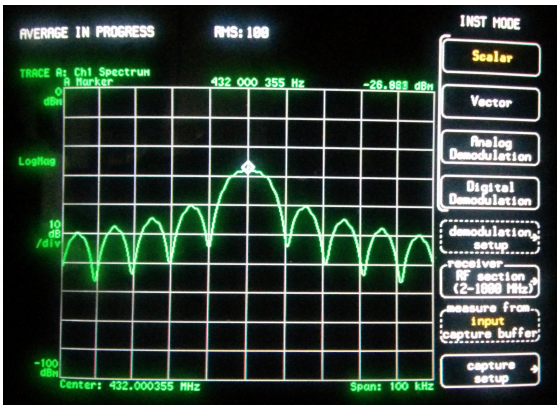


(c) *10 kbps RC-BPSK spectrum.*

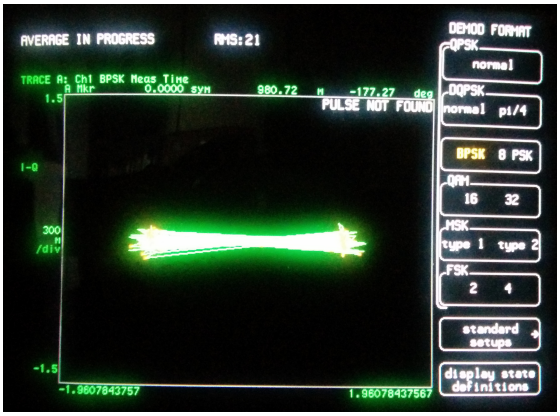


(d) *10 kbps RC-BPSK constellation.*

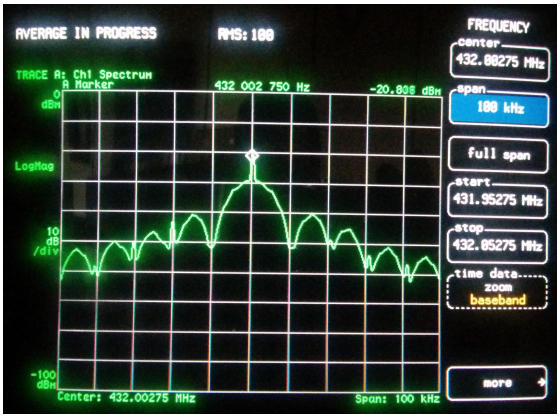
Figure 7.11: *4× VCO BPSK and RC-BPSK performance at 10 kbps using the transmitter's exponential-horn pad driver.*



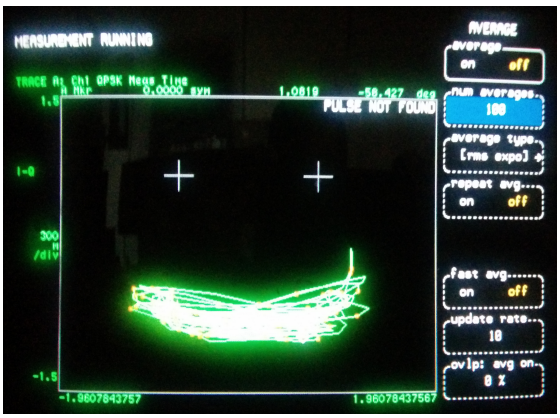
(a) *10 kbps BPSK spectrum.*



(b) *10 kbps BPSK constellation.*

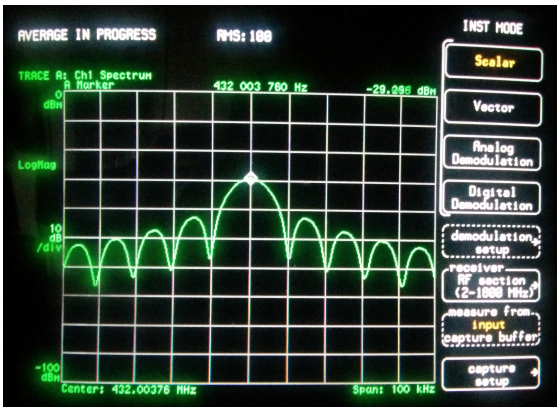


(c) *10 kbps RC-BPSK spectrum.*

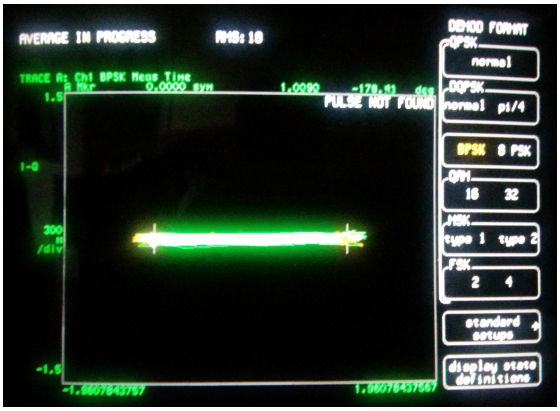


(d) *10 kbps RC-BPSK constellation.*

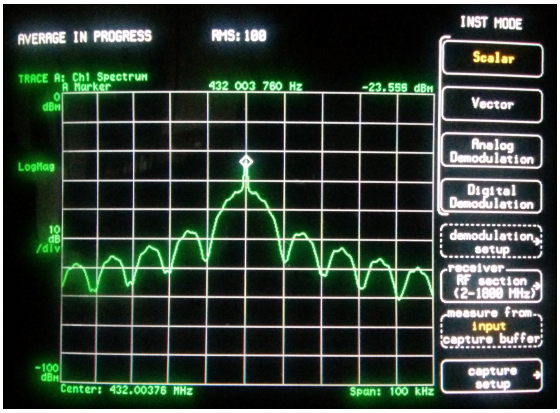
Figure 7.12: *2× VCO BPSK and RC-BPSK performance at 10 kbps using the transmitter's class-C PA.*



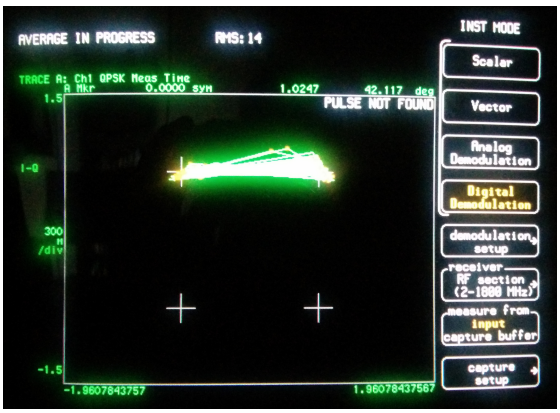
(a) *10 kbps BPSK spectrum.*



(b) *10 kbps BPSK constellation.*



(c) *10 kbps RC-BPSK spectrum.*



(d) *10 kbps RC-BPSK constellation.*

Figure 7.13: *4× VCO BPSK and RC-BPSK performance at 10 kbps using the transmitter's class-C PA.*

waves. The transmitters consisted of a differential LC VCO, an integer-N synthesizer, an IQ modulator, an exponential-horn pad driver, and an integrated class-C PA, and were designed to closely mimic the performance of the K-State Microtransceiver. In testing, the transmitter with the 2× VCO experienced pulling from RC-BPSK modulation, but the transmitter with the 4× VCO did not, thereby confirming the analysis in Chapter 5 and validating a critical coupling mitigation strategy for use in future versions of the microtransceiver.

Chapter 8

Revisions to the K-State Microtransceiver

Having identified the cause of the pulling problem in the K-State Microtransceiver, analyzed the pulling mechanism to determine its effect on the microtransceiver's modulated output, and having successfully tested several pulling mitigation strategies, the results in this work were applied to the microtransceiver. Two new revisions of the microtransceiver—Rev 6a and Rev 6b—were designed in the course of an independent study class , each implementing different pulling mitigation strategies so that future K-State researchers can test their effectiveness.

8.1 K-State Microtransceiver Revision 6a

The first revision of the microtransceiver—Rev 6a—was designed in 0.5 μm SOI with a 2× VCO and a modified 100 mW PA layout, allowing the Class-C PA to use an external chip inductor to eliminate coupling between the PA and VCO. Figure 8.1 is a block diagram of Rev 6a, and Figure 8.4 shows the completed top-level layout.

8.1.1 External 100 mW PA Inductor

In an attempt to enable the microtransceiver to transmit QPSK without a drastic redesign of the frequency synthesizer, the 100 mW PA layout was modified to use an external inductor. By moving the PA inductor off-chip, pulling of the 2× VCO by the PA will be significantly reduced.

Figure 8.2 is a close-up of the 100 mW PA showing the modified inductor layout. The connection between the class-C PA output and the integrated PA inductor was

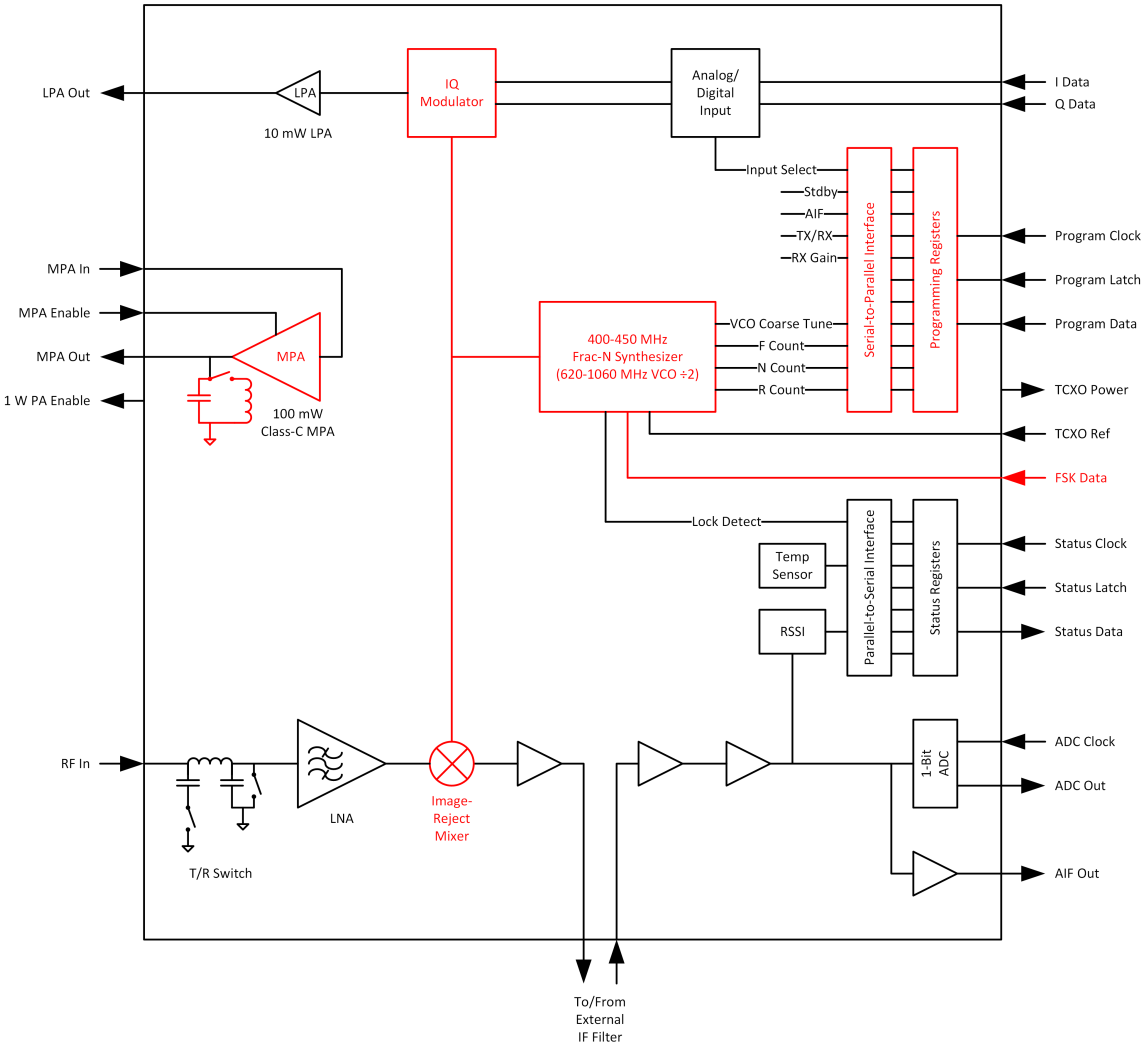


Figure 8.1: *K-State Microtransceiver Rev 6A block diagram. Circuits in red were designed or modified in the course of this thesis.*

rerouted through a thin metal loop. The width and length of the loop trace were chosen to tolerate currents of over 300 mA (a 3× safety margin) and contribute negligible series resistance to the PA inductor (0.2 Ω) while still being thin enough to cut by scribing the chip with a diamond cutter or a probe tip. This would allow testing with the on-chip inductor first and then off-chip to get a precise comparison.

8.1.2 Attenuating the 4.8 MHz Divided-Reference Spur

The 4.8 MHz divided-reference spur identified in Chapter 3 is caused by capacitive coupling between the top-metal synthesizer ground shield and nearby top-metal features in the receiver, including power and ground busses, DC blocking capacitors, and the outer windings of the LNA inductor. This allows the divided-reference frequency to capacitively-couple into the output of the LNA and the input of the image-reject mixer. After downconversion, the 4.8 MHz spur is amplified by 26 dB before appearing in the unfiltered IF output.

Two design modifications were introduced to Rev 6a to attenuate the divided reference spur. First, the lower corner frequency of the image-reject mixer in the receiver was increased from 10 kHz to 32 MHz to provide an additional 40 dB attenuation of the divided-reference spur. Second, the top-metal synthesizer ground shield was dramatically reduced in size. In Rev 5, the shield covered both the frequency synthesizer and the digital programming registers. While the frequency synthesizer is a proven noise source, the programming registers are not clocked after initialization and do not generate any digital noise. Therefore, the size of the ground shield can be reduced to cover the frequency synthesizer. Shrinking the ground shield increased the separation between the shield and top-metal features in the receiver from 60 μm to 240 μm. Figure 8.3 compares the size and position of the top-metal ground shields in Fab 5 and Rev 6a.

8.1.3 Direct-Modulation FSK

The K-State Microtransceiver has been used as both a BPSK and FSK radio link in several medium-power applications. The microtransceiver's differential I and Q data inputs make it easy to utilize the radio in constant-envelope BPSK mode. However, operating the radio in FSK mode requires either a test board with an FPGA acting as a digital modem or the equipment to generate accurate shaped IQ waveforms, neither of which are available in the low-power applications currently being researched. For that reason, the effects of pulling on FSK modulation were not experimentally tested

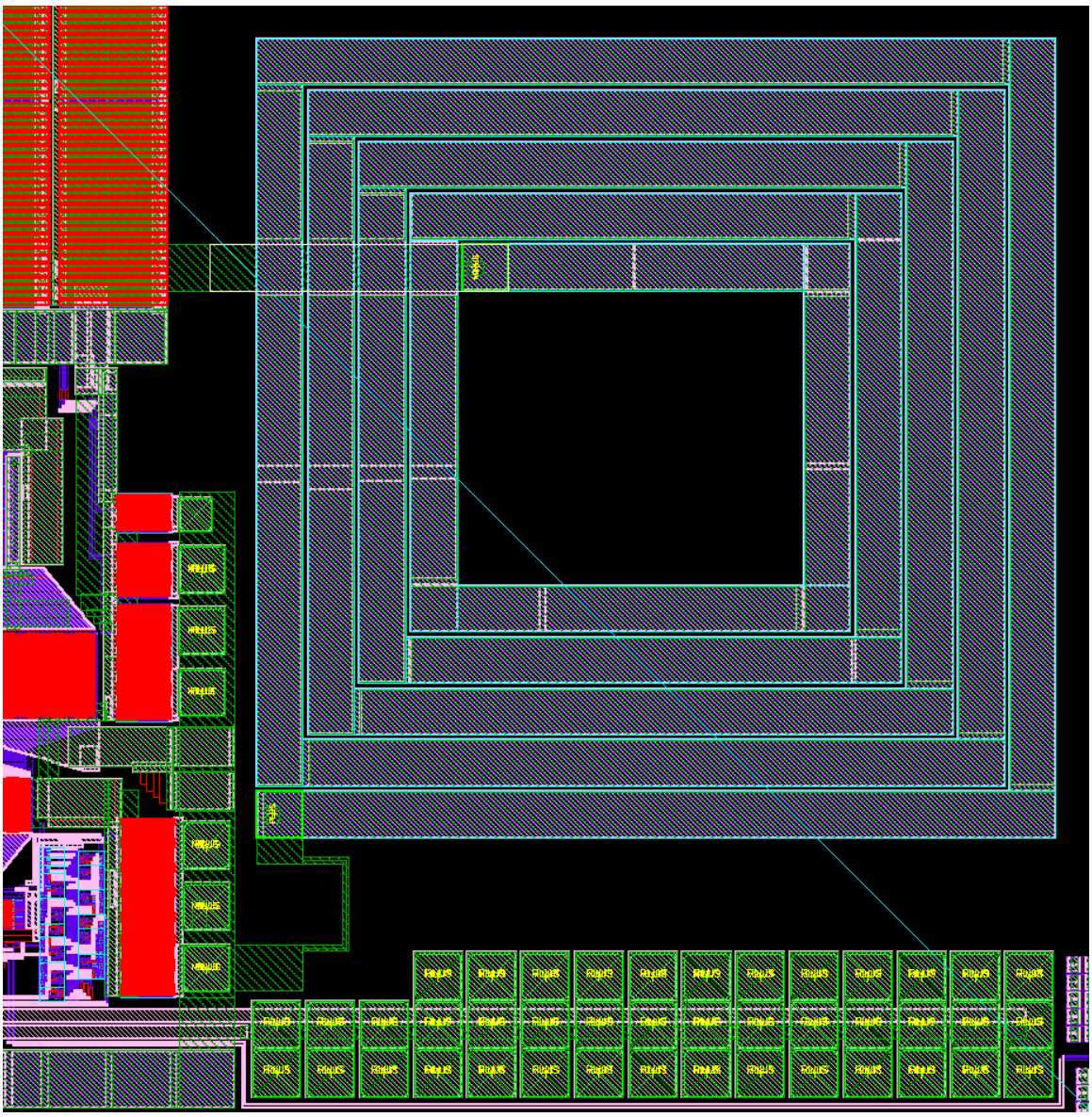
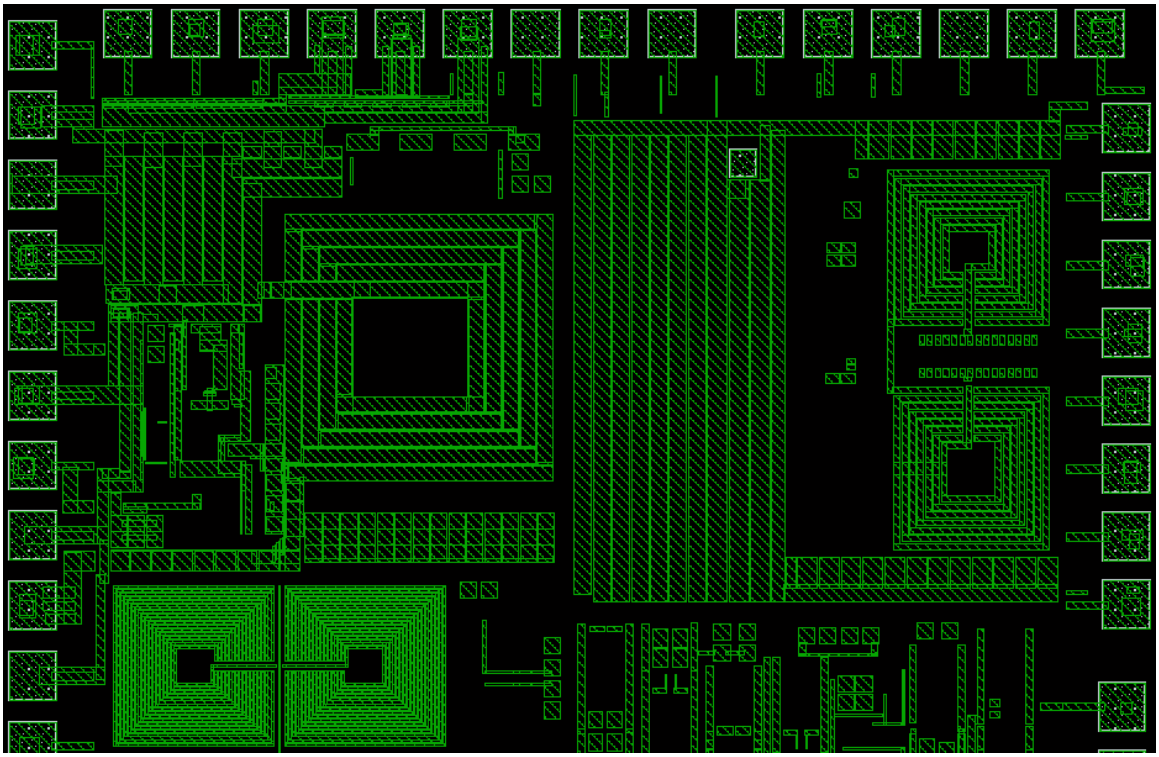
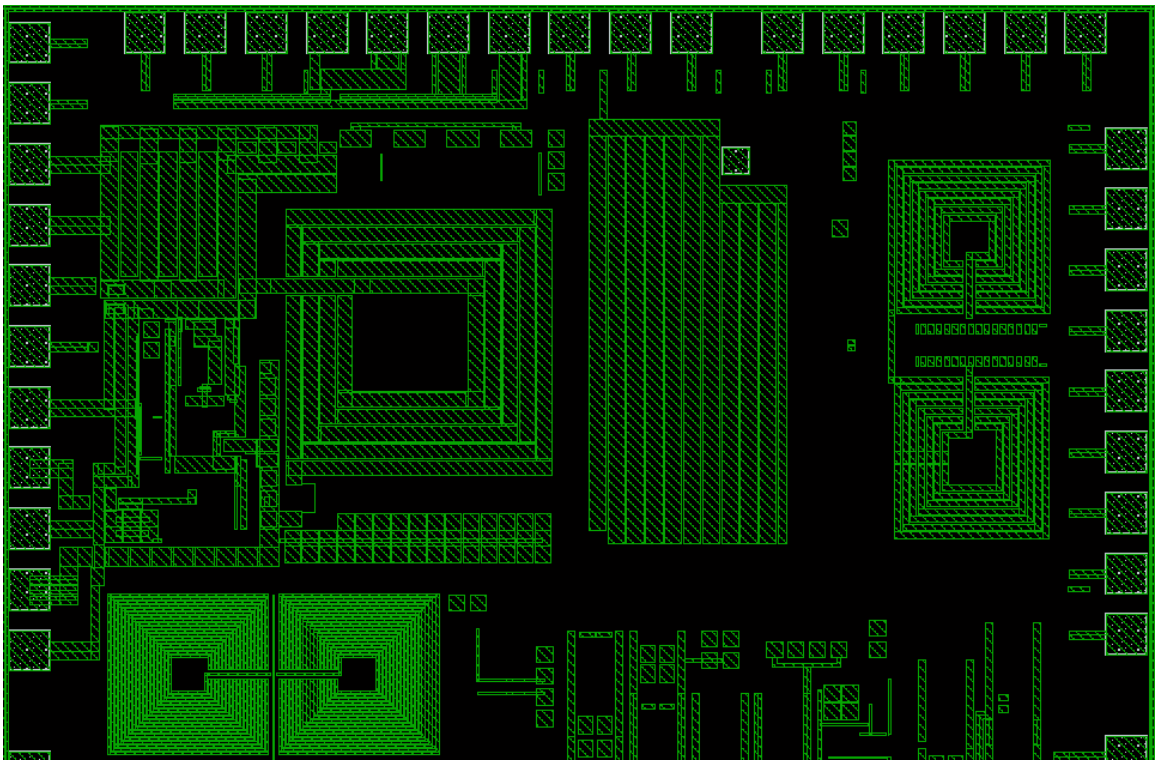


Figure 8.2: *Detail of the modified 100 mW PA inductor in Rev 6A. The internal PA inductor can be disconnected by scribing the top-metal loop (lower left) with a diamond cutter or a probe tip.*



(a)



(b)

Figure 8.3: *Comparison of (a) Fab 5 and (b) Rev 6a top-metal synthesizer ground shields.*

in this research.

A simple FSK modulator was implemented in the Rev 6a layout to enable the microtransceiver the be used as an FSK radio link without an on-board FPGA. The FSK modulator operates by toggling a bit in the fractional-divider (F) register to perform direct-modulation FSK. The fractional frequency step caused by toggling a bit in the F register of the microtransceiver's 10-bit fractional-N synthesizer can be expressed as

$$\Delta f = \left(\frac{f_{ref}}{2^R}\right)\left(\frac{2^F}{1024}\right) \tag{8.1}$$

where f_{ref} is the reference oscillator frequency, R is the value in the reference divider register, and F is the bit being toggled in the fractional division register. To produce 100 kHz FSK, a dedicated FSK data pin bypasses the IQ modulator and directly toggles bit 4 in the F register.

8.1.4 Additional Improvements

In addition to the external 100 mW PA inductor, attenuation of the 4.8 MHz divided-reference spur, and the addition of direct-modulation FSK, the following improvements were incorporated into the Rev 6a design and layout:

- The Rev 5 phase/frequency detector and charge pump were replaced with improved versions with better linearity and decreased dead-band to reduce fractional-N spurs.
- Layout size of the fractional-N synthesizer and digital programming registers was reduced by 30%.
- Pad size was reduced from 150 μm to 100 μm and pin count increased from 60 pins to 64 pins. Each power and ground domain now has a separate ESD protection diode bias pin to eliminating potential cross-domain coupling through the ESD bias bus.

8.2 K-State Microtransceiver Revision 6b

A second revision of the K-State Microtransceiver—Rev 6b—is being designed in Peregrine Semiconductor's 0.25 μm SOS UltraCMOS process as part of a NASA/EPSCoR project and an independent study by the author. Instead of a 2× VCO, Rev 6b utilizes a 4× VCO with a figure-8 tank inductor for maximum insensitivity to pulling

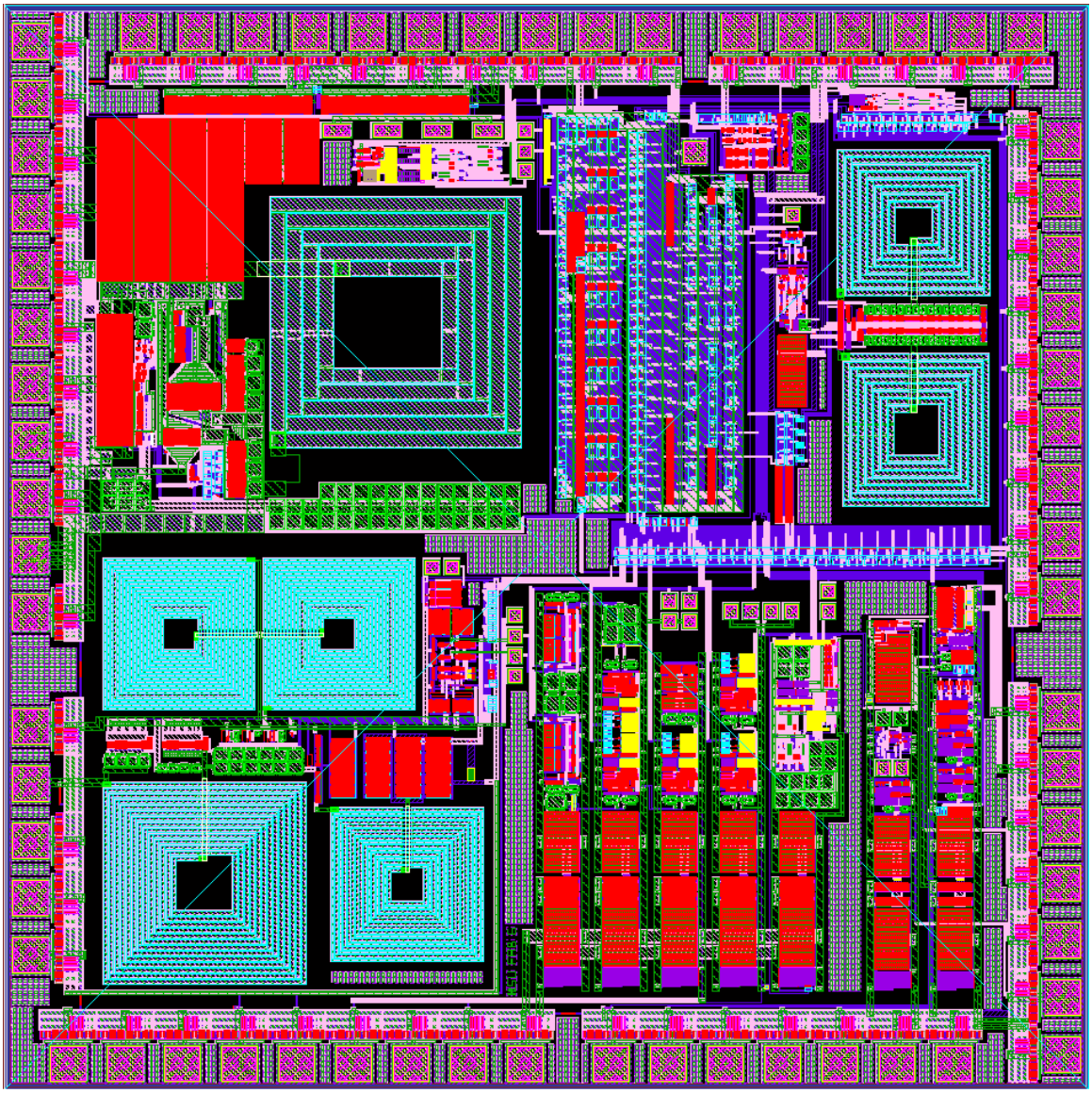


Figure 8.4: *K-State Microtransceiver Rev 6a top-level layout.*

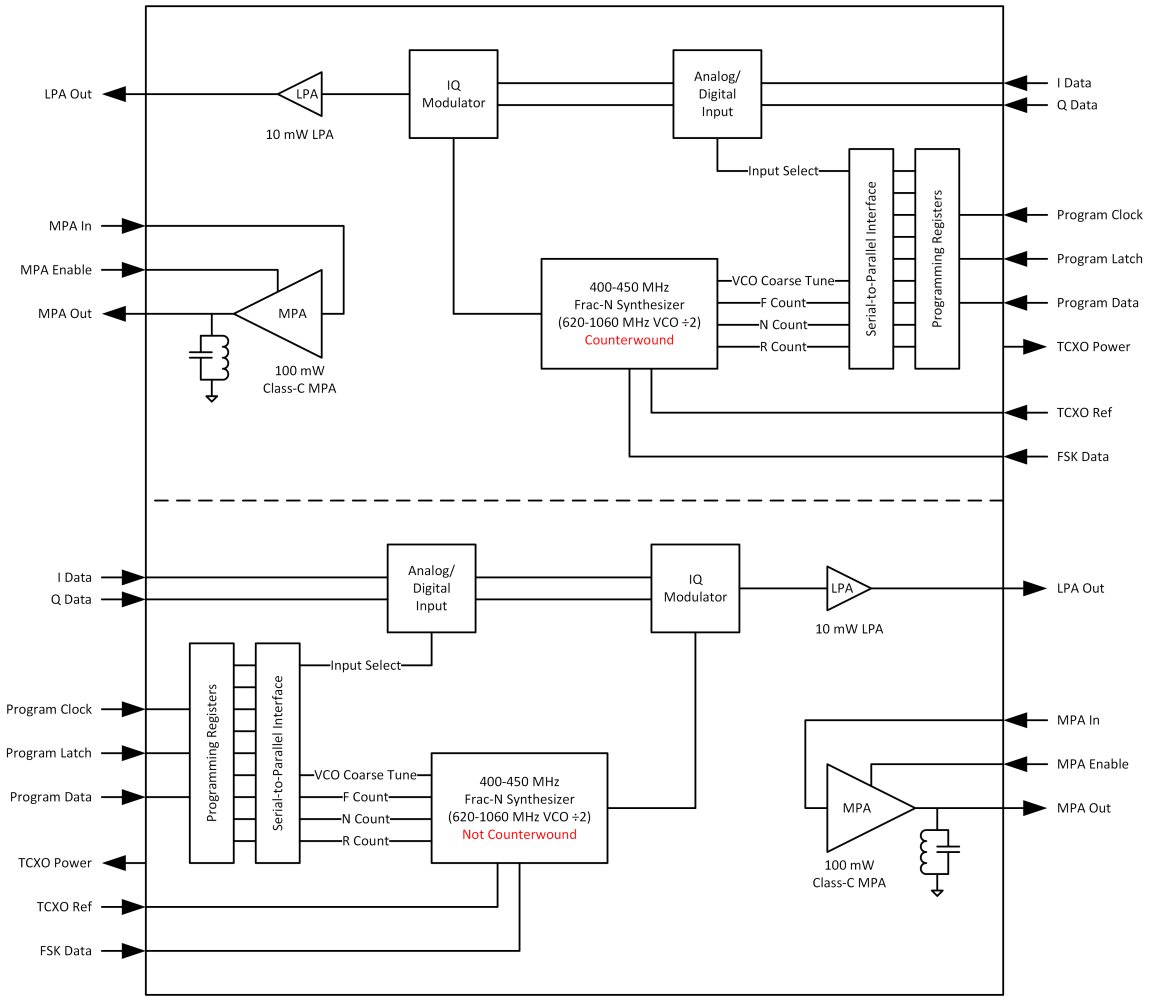


Figure 8.5: *K-State Microtransceiver revision 6b block diagram. Circuits in red were designed or modified in the course of this thesis.*

from the 100 mW PA. The figure-8 inductor topology will enable the radio to transmit both constant-envelope and band-limited IQ modulation. This revision of the microtransceiver is targeted for fabrication in early 2015 and will enable future researchers to validate the effectiveness of inductor counterwinding and to focus on system-level applications of highly-integrated medium-power transceivers where fully-functioning IQ modulation is needed with shaped IQ waveforms as well as basic QPSK.

Figure 8.5 is a block diagram of Rev 6b. While the microtransceiver circuit topology is largely unchanged from Rev 6a, converting the design to 0.25 μm SOS reduced the supply voltage from 3.3 V to 2.5 V and changed the threshold voltages for several flavors of transistor. As a result, each circuit is being redesigned and optimized for operation at a lower supply voltage. While the topology of the microtransceiver remains unchanged, the reduced supply voltage and increased threshold voltages re-

quire each circuit to be redesigned. In addition to the modifications made to Rev 6a, the following additional improvements are being implemented in Rev 6b:

- Both the 10 mW and 100 mW power amplifiers are being redesigned and optimized for the lower 2.5 V supply voltage. Vestigial duty-cycle control logic was removed, and the amplifier layouts are being redone to minimize the length of the interconnects between the IQ modulator and the PA.
- The physical separation between the 100 mW PA inductor, resonant T/R switch inductor, and 4× VCO inductors were increased.
- The length of the pseudo-random bit sequence (PRBS) generator in the Σ-Δ modulator was increased from 15 bits to 21 bits to further attenuate fractional-N spurs caused by dithering.
- An under-performing temperature sensor and received-signal strength indicator (RSSI) were removed to free up additional layout to address the coupling issues described in this thesis.

Chapter 9

Conclusion

This thesis examined a situation in which magnetic coupling between the PA and VCO in a fully-integrated UHF microtransceiver prevented the use of QPSK modulation at certain data rates. The literature reviewed in Chapter 1 showed limited treatment of this subject. This thesis makes the connection between frequency pulling, VCO operating frequency, PA output frequency, and output modulation. It also demonstrates that it is possible to design a robust, fully-integrated transceiver, even in the presence of unavoidable coupling, by identifying potential on-chip coupling mechanisms and tailoring the transceiver architecture to be naturally insensitive to them.

To identify the source of the QPSK pulling problem, all major on-chip coupling mechanisms, including substrate, electric field, and magnetic coupling, were analyzed. While substrate and electric-field coupling are present in the microtransceiver to some degree, extensive testing described in Chapter 3 demonstrate that these mechanisms, as well as system-level coupling issues like ground bounce and power supply ripple, were well-addressed in the original design.

Unlike substrate and electric field coupling, magnetic coupling is difficult to mitigate because magnetic shielding techniques significantly reduce the Q of integrated inductors. The most straightforward magnetic coupling mitigation strategy is to decrease the flux linkage between inductors by increasing their physical separation. However, the maximum separation—and therefore the maximum isolation—is restricted by the size of the inductors, the size of the die, and other layout constraints. Although magnetic coupling was also considered during the original design, it was ultimately found to be the cause of frequency pulling. When the microtransceiver's 100 mW class-C PA is operating, the 100 mW output magnetically couples from the PA inductor into the LC tank circuit of the VCO, time-modulating the varactor capacitance and pulling the VCO off-frequency.

Chapters 4 analyzed the operation of a differential LC VCO and developed a model for the large-signal operation of inversion-mode MOS varactors commonly used for analog frequency tuning. Chapters 5 and 6 expanded the analysis to a VCO under magnetic coupling from an aggressor inductor like the one in the microtransceiver's class-C PA. If the aggressor signal is amplitude-modulated, aperiodic, or band-limited, VCO pulling can be mitigated by using a figure-8 inductor topology for the aggressor inductor, the VCO inductor, or both. Chapter 6 demonstrates that the figure-8 inductor topology produces no net far-field flux when excited, and no net voltages are induced in the inductor by coupling from far-field aggressors. The figure-8 inductor topology was found to provide an additional 50 dB of isolation between the PA and VCO over the counterwound spiral inductor topology implemented in Fab 5. If it is impossible to implement a figure-8 inductor, LO pulling can be reduced (but not eliminated) by simply counterwinding the VCO inductors so that the voltage induced in the VCO by the aggressor signal creates a common-mode disturbance on the VCO output. As demonstrated in Chapter 5, a common-mode disturbance produces a much smaller change in output frequency than a differential disturbance due to the series-connected nature of the varactors. This validates an assumption made in the original design of the microtransceiver.

Chapters 5 and 6 also illuminated the special set of circumstances where VCO pulling can be eliminated by exploiting the frequency and phase relationship between the aggressor signal and the VCO. In the case of the K-State Microtransceiver, where the aggressor signal is a constant-envelope, phase-modulated waveform, and a quadrature divider is used to generate I and Q outputs for modulation, LO pulling can be eliminated—even in the presence of strong coupling—by choosing the VCO operating frequency and quadrature divider ratio N so that the following relationship is satisfied:

$$N = \frac{f_{vco}}{f_{out}} = \frac{2\pi}{\phi_{min}} \tag{9.1}$$

where ϕ_{min} is the phase angle between adjacent symbols in the signal constellation.

Based on this analysis, it was concluded that a VCO operating at 4× the transmit frequency would be naturally insensitive to pulling from BPSK and QPSK-modulated carrier waves. In Chapter 7, a pair of QPSK transmitters was designed and fabricated in 0.18 μm SOI to validate this result. Testing confirmed that the transmitter with the 2× VCO experienced frequency pulling when transmitting QPSK, but the transmitter with the 4× VCO did not, thereby confirming the analysis in Chapters 5 and 6.

Finally, the pulling mitigation strategies identified in this research were applied

to two redesigns of the K-State Microtransceiver. Two revisions—Rev 6a and Rev 6b—were designed, each implementing different pulling mitigation strategies. In Rev 6a, the 100 mW PA inductor layout was modified so that the on-chip inductor can be disconnected from the PA by scribing through a thin top-metal trace. This would allow the microtransceiver to be operated with an external PA inductor to determine if simply moving the PA inductor off-chip reduces the flux linkage between the PA and VCO inductors enough to eliminate pulling. A capacitive coupling path between the synthesizer ground shield and the receiver responsible for the appearance of a 4.8 MHz divided reference spur in the IF output was mitigated using two methods detailed in Chapter 8. In addition to the modified class-C PA, Rev 6a also received an improved charge pump, and a hardware FSK modulator with a dedicated FSK data pin. In addition to the improvements made to the Rev 6a transmitter, Rev 6b is being designed in 0.25 μm SOS, allowing critical circuits such as the quadrature dividers, to take advantage of the higher f_t of the smaller process to support operation of the VCO at the needed 4× frequency. Rev 6b focuses on the use of the 4 × VCO solution developed in this research and laying the groundwork for investigating use of the figure-8 inductor to mitigate pulling from diverse modulation schemes.

9.1 Future Work

This research presents two avenues for future work. First, Rev 6b of the microtransceiver must be tested to measure the effects of counterwound and figure-8 inductors on LO pulling, and to validate the other modifications described in Chapter 8. Of particular interest are the robustness of the VCO and quadrature dividers in the new 0.25 μm process, and the performance of the new FSK modulator, which was added specifically to support the research in [5].

Second, the current NASA/EPSCoR research could benefit from the realization of a 2.4 GHz fully-integrated transceiver IC with full IQ waveform capability. The primary roadblock to achieving this has been the maximum operating speed of the VCO frequency dividers used to generate I and Q in the 0.5 μm process. Traditional D-latch based frequency dividers have not functioned reliably at 2.4 GHz. Other division methods, including injection-locked frequency dividers, were considered, but ultimately not pursued because of their complexity and susceptibility to magnetic coupling. However, when combined with the coupling mitigation strategies identified in [8], the pulling mitigation techniques presented in this thesis could enable researchers to design a fully-integrated 2.4 GHz medium-power transceiver with full

IQ modulation.

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