ECS Journal of Solid State Science and Technology, **2** (5) N110-N114 (2013)
2162-8769/2013/2(5)/N110/5/$31.00 © The Electrochemical Society

Influence of Atomic Layer Deposition Temperatures on TiO_2/n-Si MOS Capacitor

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This paper reports on the influence of deposition temperature on the structure, composition, and electrical properties of TiO_2 thin films deposited on *n*-type silicon (100) by plasma-assisted atomic layer deposition (PA-ALD). TiO_2 layers ~20 nm thick, deposited at temperatures ranging from 100 to 300°C, were investigated. Samples deposited at 200°C and 250°C had the most uniform coverage as determined by atomic force microscopy. The average carbon concentration throughout the oxide layer and at the TiO_2/Si interface was lowest at 200°C. Metal oxide semiconductor capacitors (MOSCAPs) were fabricated, and profiled by capacitance-voltage techniques. The sample prepared at 200°C had negligible hysteresis (from a capacitance-voltage plot) and the lowest interface trap density (as extracted using the conductance method). Current-voltage measurements were carried out with top-to-bottom structures. At −2 V gate bias voltage, the smallest leakage current was 1.22×10^{-5} A/cm^2 for the 100°C deposited sample.
 [DOI: 10.1149/2.010305jss]

Manuscript submitted December 5, 2012; revised manuscript received February 25, 2013. Published March 8, 2013.

Titanium oxide thin films have many applications such as photocatalyst,[1] solar cells,[2] gate insulators,[3] and dielectrics.[4] With the potential of achieving an extraordinarily high dielectric constant [up to 130 for rutile TiO_2,[5,6] 2000 for $SrTiO_3$[7]], TiO_2 is also an appealing dielectric for capacitors in the dynamic random access memory (DRAM), the main memory device in modern computers. Since the capacity and performance of DRAM greatly affects the working speed of a computer, much attention has been given to optimize DRAM. As proposed by the International Technology Roadmap for Semiconductors (ITRS),[8] DRAM capacitors with higher capacitance, thinner equivalent oxide thickness (EOT)[9] and smaller leakage current density are highly desirable. The insulator deposition temperatures should be below 500°C, because capacitors are expected to be deposited after transistors formation.[10] However, further research on the high dielectric materials is needed to fulfill those requirements.

In the present study, plasma-assisted atomic layer deposition (PA-ALD) was employed to deposit thin insulating TiO_2 films, because it offers excellent atomic level control of layer thickness with good uniformity and conformality.[11] With an O_2 plasma, the deposition can be conducted at a lower temperature and with a shorter purge time in cold-wall reactors than a conventional thermal ALD system.[12] These characteristics are particularly suitable for growing capacitor dielectrics for use in DRAM, as it uses a three dimensional structure with a high aspect ratio to increase the effective surface area.[13]

The present work reports on the impact of the deposition temperature on the properties of TiO_2 films prepared by PA-ALD and on the performance of said films in silicon MOSCAPs. By correlating the oxide structure, surface morphology and impurity concentration with electrical properties (hysteresis, interface trap density and leakage current), an optimal deposition temperature is identified.

Experimental

TiO_2 ALD Film growth and metal contact deposition.— Before deposition, the *n*-type Si (100) substrates were cleaned with acetone and isopropyl alcohol (IPA) for 5 minutes at 40°C. TiO_2 was deposited by PA-ALD in an Oxford Instruments FlexAL ALD reactor with tetrakisdimethylamino titanium (TDMAT) kept at 39°C as the titanium precursor, and oxygen plasma as the oxidizing agent. The ALD growth temperatures were 100°C, 150°C, 200°C, 250°C and 300°C. All ALD depositions consisted of 400 cycles and each ALD cycle included a 0.4 second dose of TDMAT followed by a 4 second purge with Ar gas, and a 3 second exposure to the oxygen plasma followed by a 3 second purge. The plasma power and pressure during exposure was set to 400 Watts and 15 mTorr, respectively, with an O_2 flow rate of 60 sccm. Circular capacitors (50–300 μm diameter) with Ni/Au (20/100 nm) metal contacts on top of the oxide were created by standard photolithography and E-beam evaporation methods. The current-voltage test structures consisted of the top capacitor contact and the bottom contact which was bare silicon held on the conductive measuring stage with constant vacuum pumping at the center of the sample.

TiO_2 Film characterization.— The TiO_2 film morphology was measured by atomic force microscope (AFM, Digital Instrument MultiMode SPM from Veeco Instruments Inc) operating in tapping mode.

Elemental compositions of the oxides were measured as a function of depth by X-ray photoelectron spectroscopy (XPS) with argon ion sputtering using a K-Alpha XPS from Thermo Scientific. The K-Alpha XPS uses monochromatic Al k-alpha X-rays to generate photoelectrons that pass through a double-focusing hemispherical electron energy analyzer onto a 128-channel detector. Depth profiling was carried out using 3 KV Ar-ions and set to a known sputtering rate for SiO_2, which is 6 nm/min, as calibrated on a SiO_2 standard.

The thickness and refractive index of the TiO_2 films was measured using a spectroscopic ellipsometry (alpha-SE model from J.A.Woollam Co. Inc.) at three incident angles, 65°, 70°, and 75°. The spectral range of the ellipsometry was from 380–900 nm (1.3–3.25 eV), and measured data were fitted with the Cauchy layer model[14] to determine the thickness of the ALD films.

The structure of the thin films was characterized by X-ray diffraction (XRD, PANalytical X'Pert Pro MPD) using a Cu-Kα radiation source. Measurements were taken over the range of 5–80° with a step size 0.0167° and a count time of 2 seconds. To avoid the high intensity peak of the Si (100) substrate, the samples were offset by 2° in omega.

C-V measurements were taken on the TiO_2/Si MOS capacitors using a Keithley 4200 semiconductor characterization system operating at 1 MHz at room temperature. To evaluate charge trapping in the oxide layers from the hysteresis behavior of the oxide, the bias was applied by sweeping the dc voltage back and forth between +10 V and −10 V at a sweep rate of 0.1 V/sec. The same results were obtained regardless of the sweep direction. The interface trap density, D_{it}, (at the oxide-dielectric interface) was determined by the ac conductance method[15] using an HP 4284A precision LCR meter, and conductance was measured from 20 Hz to 1 MHz with a long integration time at room temperature. The I-V measurements were taken by sweeping the voltage from +4 V to −4 V, and leakage current densities of each sample were compared at −2 V gate bias voltage.

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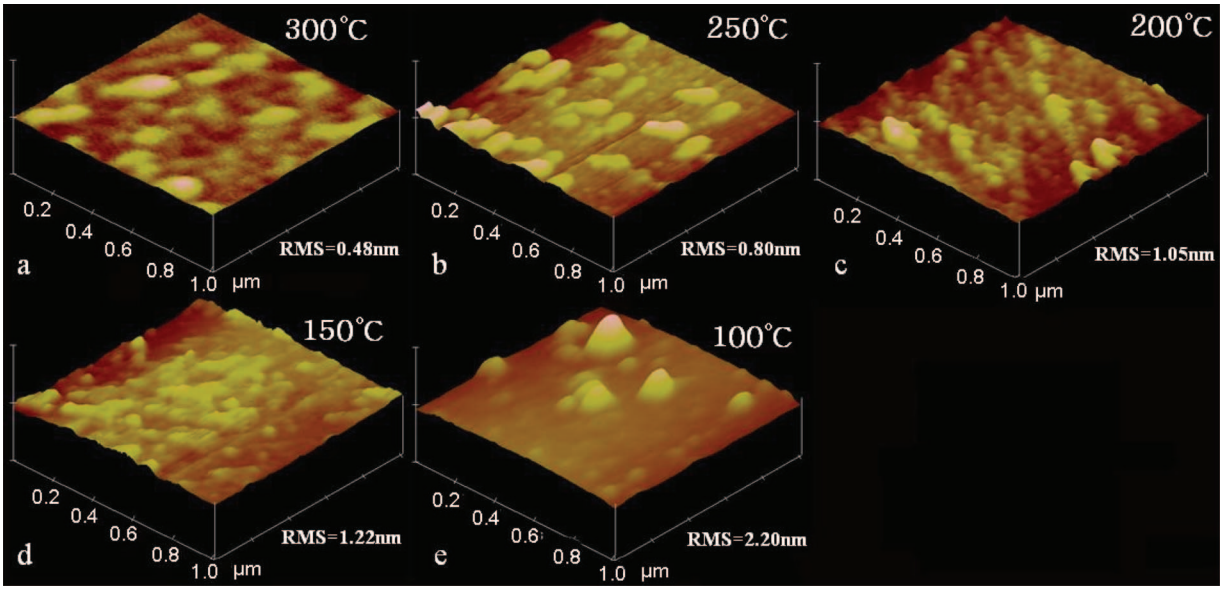

Figure 1. Three-dimensional AFM images of TiO_2 on Si deposited at different ALD temperatures. The Z height is 30 nm for all images. (a) 300°C (RMS = 0.48 nm), (b) 250°C (RMS = 0.80 nm), (c) 200°C (RMS = 1.05 nm), (d) 150°C (RMS = 1.22 nm), and (e) 100°C (RMS = 2.202 nm).

Results and Discussion

The surface of the TiO_2 film deposited at 200°C was the most uniform, as it had the highest density of nucleation sites as determined by AFM. The next most uniform samples were those prepared at 250 and 300°C (Fig. 1). By contrast, random, isolated islands formed at 150°C and 100°C, indicating a lower nucleation density at lower temperatures. The root mean square (RMS) surface roughness decreased with the growth temperature. Lee et al.[16] reported a similar trend for TiO_2 grown on amorphous Si by metal-organic chemical vapor deposition (MOCVD).

On all TiO_2 sample surfaces, nitrogen was detected by XPS. However, it disappeared after sputtering for 30 seconds, suggesting it was solely surface contamination. At the interface, silicon oxide was also observed. The average ratio of oxygen and titanium was calculated (Table I) in the steady region in depth profile (Fig. 2a). The sample deposited at 200°C had the O/Ti stoichiometry closest to 2/1 of TiO_2 followed by the 100 and 150°C samples. 250 and 300°C deposition temperatures lead to oxygen-rich titanium oxide films. The signal from the Ti 2p transition was also monitored in the depth profile (Fig. 2b). A single doublet, suggesting the presence of metallic titanium, was present at the oxide/Si interface for all samples, then disappeared away from the interface into the film. The observation of metallic titanium could be from the reduction during Ar^+ sputtering. Carbon was detected throughout the oxide films. Figure 3 plots

Table I. Oxygen and titanium ratio, average carbon concentration, thickness, dielectric constant of TiO_2 and calculated values of D_{it} for TiO_2/Si samples prepared at different ALD temperatures.

ALD temperature (°C)	O:Ti Ratio	Average C concentration (%)	TiO_2 thickness (nm)	Dielectric constant	D_{it} (1×10^{13} $eV^{-1}cm^{-2}$)
300	2.24	3.20	19.7	29.6	1.7–4.0
250	2.32	2.79	19.0	42.5	3.8–4.7
200	2.08	2.61	19.2	55.6	1.1–1.5
150	2.12	3.12	17.9	47.1	2.5–3.9
100	2.10	3.74	19.3	41.3	1.5–2.2

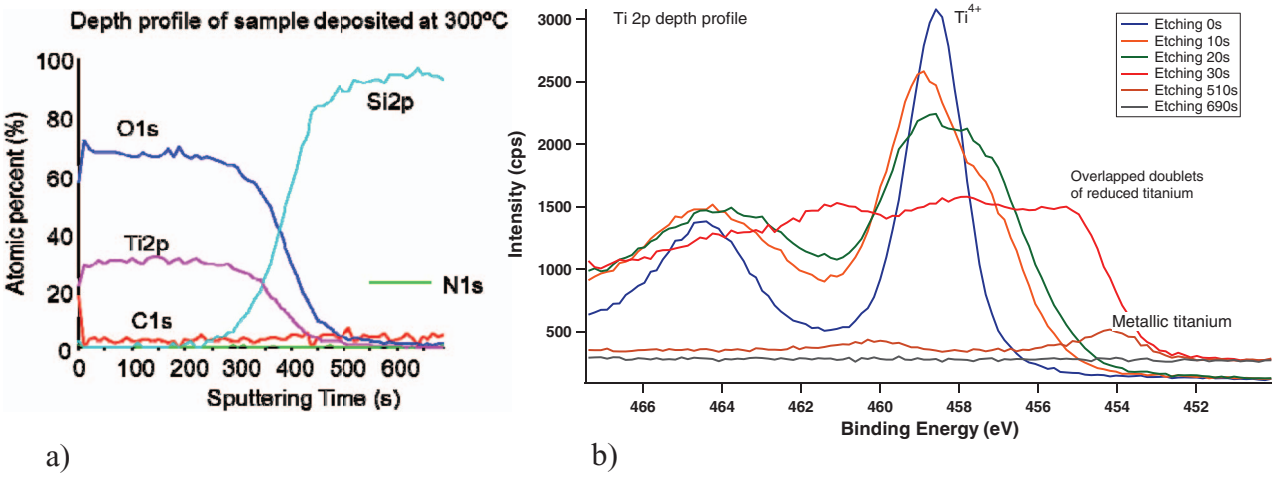

Figure 2. (a) XPS depth profile of sample deposited at 300°C. (The shape of the depth profiles is similar for all the samples. Only one is demonstrated.) (b) XPS depth profile of Ti2p at different sputtering times. The 2p3 of Ti^{4+} and metallic Ti peaks are 458.5 eV at 0 seconds and 454.2 eV at 510 seconds.

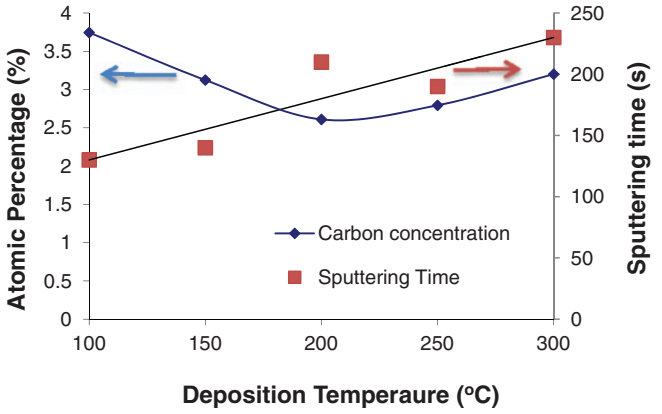

Figure 3. (Left axis) Average atomic carbon concentration in the TiO_2 layers versus ALD temperature. (Right axis) Sputtering time to remove the oxide layer and expose the Si substrate versus ALD deposition temperature.

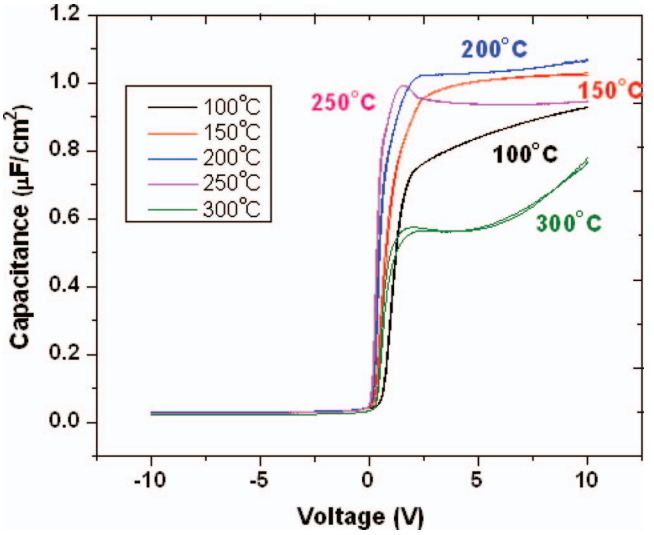

Figure 4. C-V measurement for TiO_2/Si MOS capacitors at different ALD temperatures.

the average carbon concentration in the oxide layers as a function of the ALD deposition temperature. The minimum carbon concentration (2.6%) occurred at 200°C (Table I).

The TiO_2 thickness was similar for all samples, 19 ± 1.2 nm (Table I), as measured by ellipsometry. However, the time to sputter through the oxide layers increased with increasing deposition temperature (Fig. 3). This suggests that the oxide film increased in density and was more resistant to sputtering as the deposition temperature was increased.[17] The TiO_2 films were amorphous, since no TiO_2 crystalline peaks were detected by X-ray diffraction.

The dielectric constant was calculated using the relationship $C = \varepsilon_r \varepsilon_0 A/d$, where C is the capacitance of the material, ε_r is dielectric constant, ε_0 is permittivity of free space and d is layer thickness. The TiO_2 and SiO_2 thin films were treated as capacitors in series, and it was assumed that the ε_r and thickness of SiO_2 are 3.9 and 1.9 nm respectively. The dielectric constant of TiO_2 (Table I) was calculated from C-V plots using the equation:

$$\frac{1}{C_m} = \frac{1}{C_{TiO_2}} + \frac{1}{C_{SiO_2}} \quad [1]$$

where C_m is the measured capacitance in the accumulation region. A wide range of ε_r for amorphous TiO_2 [ε_r = 16–86] has been reported,[18,19] and our values [ε_r = 29–56] were similar to those reported by Alexandrov et al.[18]

All TiO_2/Si samples had negligible hysteresis, similar to the observations of Fuyuki et al.[19] for TiO_2 grown on Si by chemical vapor deposition (CVD) between 200 and 400°C. For the 200°C sample, the oxide saturation capacitance (C_{ox}) was observed and the transition from accumulation to depletion region was sharp compared to the rest of the curves (Fig. 4), which is indicative of having a better interface quality. At 250 and 300°C, a bump at approximately 1.0 V is seen in the C-V plot, due to drift in mobile charge.[20] At different bias voltages, the samples deposited at 100, 150 and 300°C did not show saturation of oxide capacitance (C_{ox}). An explanation of this phenomenon will require further examination.

To calculate D_{it} as a function of energy in the bandgap of Si, the series resistance and interface state conductance $G_P(\omega)$ were extracted as a function of angular frequency at a fixed voltage within the depletion region using an ac equivalent parallel circuit model as shown in Figure 5a. The parallel conductance (G_P) represents an energy loss due to interface traps and is a function of measured capacitance (C_m),

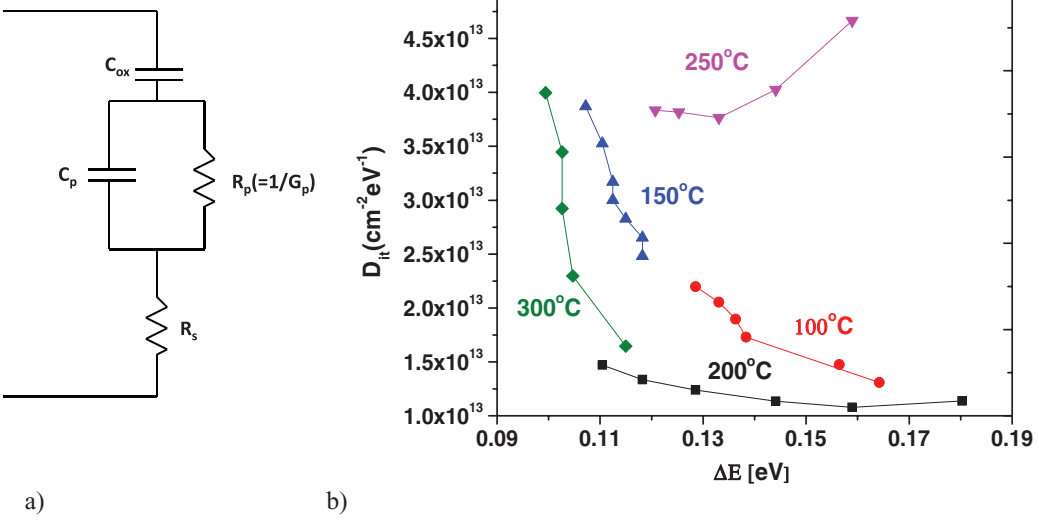

Figure 5. (a) Simplified circuit of MOS capacitor including series resistance. (b) Interface trap density distributions of ALD samples at different deposition temperatures.

angular frequency (ω), series resistance (R_s), measured conductance (G_m) and oxide capacitance (C_{ox}). Capacitance and conductance data were corrected due to inclusion of series resistance. The series resistance was calculated using the relation[15]

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \quad [2]$$

Here G_{ma} and C_{ma} are the measured conductance and capacitance in the strong accumulation region respectively. Calculated values of R_s are similar to previously published results (i.e. 2000–2500 Ω) by Pakma et al.[21] Corrected capacitance, C_c, and corrected equivalent parallel conductance, G_c, are given by[15]

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2} \quad [3]$$

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2} \quad [4]$$

where a is given by

$$a = G_m - \left(G_m + \omega^2 C_m^2\right) R_s \quad [5]$$

G_P can be expressed after inclusion of corrected conductance and capacitance as

$$G_p = \frac{\omega^2 C_{ox}^2 G_c}{G_c^2 + \omega^2 (C_{ox} - C_c)^2} \quad [6]$$

The characteristic trap response time ($\tau = 2\pi/\omega$) is expressed by the Shockley-Read-Hall statistics of capture and emission rates by the following equation:[22]

$$\tau = \frac{\exp\left[\frac{\Delta E}{k_B T}\right]}{\sigma v_{th} D_{dos}} \quad [7]$$

where ΔE is the energy difference between the majority carrier band edge energy (E_{CB}) and the trap level E_T, k_B is the Boltzmann constant, v_{th} is the average thermal velocity of the majority charge carriers ($v_{th} = \sqrt{(3k_B T/m^*)} = 2.68 \times 10^7$ cm/s), D_{dos} is the effective density of states of the majority carriers ($D_{dos} = 2(2\pi m^* k_B T/h^2)^{3/2} = 2.07 \times 10^{18}$ cm^{-3}), and T is the temperature. σ is the capture cross section of the trap (1×10^{-16} cm^{-2} [23]), which is assumed to be constant due to the dominance of the exponential term of Equation 7. Errors in the capture cross section by three orders of magnitude only made 0.18 eV energy difference within the bandgap of the semiconductor.[24] The trap level can be identified as the energy position from the frequency at which G_p/ω is maximum. Also, based on the maximum conductance from the measurement, an approximate equation to calculate interface trap density is given by:[25]

$$D_{it} = \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{max} \quad [8]$$

where A is the capacitor area. The calculated values of interface trap density are on the order of 10^{13} eV^{-1}cm^{-2} (Table I) and are distributed between 0.09 eV to 0.18 eV energy range from the conduction band edge of the Si bandgap. They were similar to the results of Kumar et al.[26] in which a single value $D_{it} = 1.2 \times 10^{13}$ eV^{-1}cm^{-2} was reported. The D_{it} distribution of the 200°C ALD sample is lower than that of the rest of samples (Fig. 5b). Results also show that $qD_{it} > Cox$. In this case the conductance method becomes insensitive to the trap density and D_{it}, and it could be overestimated by an order of magnitude.[27] Figure 6 shows that the capacitance of the sample deposited under 200°C increases in the accumulation region when the frequency is decreased due to the effect of series resistance and localized interface states at the Si/TiO_2 interface.[21] Similarly, the capacitance also increases in the depletion region with decreasing frequency due to recombination and generation from the interface states.[28] This frequency dispersion in C-V characteristics is negligible in the inversion region.

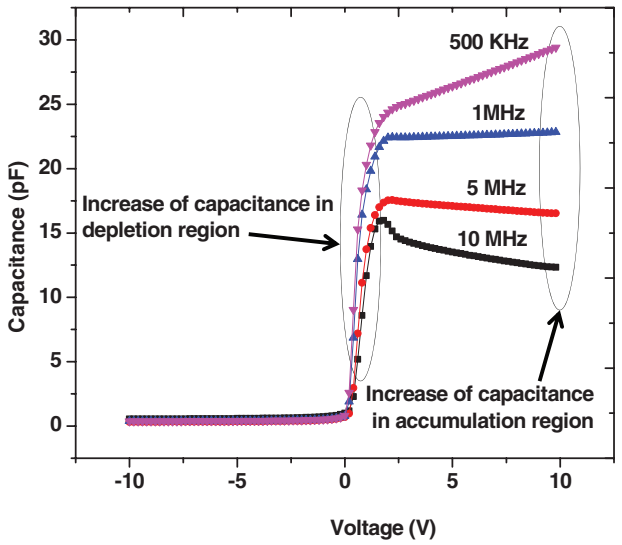

Figure 6. Measured capacitance vs gate voltage as a function of frequency for the TiO_2/Si at 200°C deposition temperature.

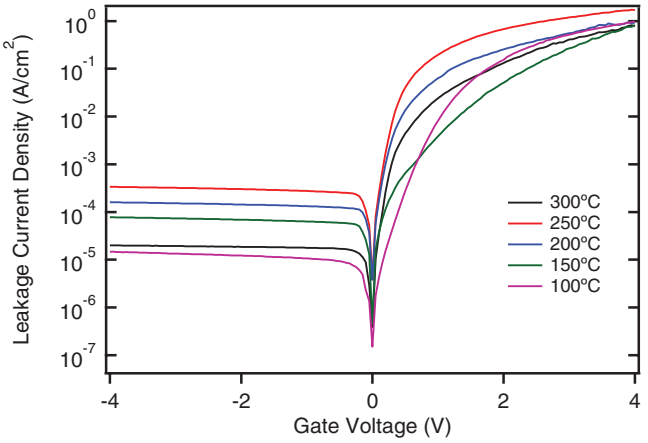

Figure 7. I–V characteristics of TiO_2/Si MOS capacitor at different ALD temperatures.

Figure 7 shows the current-voltage characteristics under positive and negative biases at room temperature for samples prepared at different ALD temperatures. The plots in Figure 7 (semi-logarithmic scale) are linear at low gate bias voltages, but deviate from linearity at high voltages, which is attributed to the series resistance effect on the TiO_2 film.[21] The leakage current densities were on the order of 10^{-5}~10^{-4} A/cm^2 at −2 V, which is 2 orders of magnitude lower than that of the reactive sputtered TiO_2 film [58 nm] reported by Albertin et al.[29] and CVD grown TiO_2 film [20 nm] reported by Bae et al.[30]

Conclusion

In this work, the influence of substrate temperature during plasma-assisted ALD on surface morphology, stoichiometry, impurity concentration and electrical properties of TiO_2/Si MOS capacitors is reported. Both surface morphology and roughness of the oxide layer were affected by the growth temperature. The impurity concentration at the oxide-silicon interface varied randomly with temperature. The TiO_2 dielectric constants are between 29 and 56, as obtained from C-V measurement, but the hysteresis in C-V plot did not change with temperature. The current density improved by two orders of magnitude compared to previous studies. Comparing the results of the TiO_2 film with different ALD temperatures, the optimal deposition temperature of TiO_2 is 200°C as this produces the highest dielectric constant, most

uniform coverage and stoichiometry. This ALD temperature also has the lowest impurity concentration and lowest D_{it} at the interface, indicating a better quality sample. These results confirm that TiO_2 is a promising high k material for silicon devices.

Acknowledgments

We are grateful for the support for this project from the Office of Naval Research, grant N00014-09-1-1160, Paul Maki, program manager. XPS and XRD were conducted through the Oak Ridge National Laboratory's High Temperature Materials Laboratory User Program, sponsored by the U. S. Department of Energy, Office of Energy Efficiency and Renewable Energy, Vehicle Technologies Program. Work at the U.S. Naval Research Laboratory is supported by the Office of Naval Research.

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