ELECTROSTATIC DISCHARGE DAMAGE DETECTION METHOD

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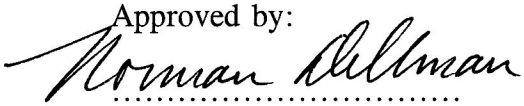

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ABSTRACT

Electrostatic discharge (ESD) damage is a major problem in electronic industry. Among the damages caused from ESD, latent damage is the most difficult to detect. Latent damaged or degraded devices shows no signs of function failures at the time of the ESD damage. However, frequent exposure of ESD will degrade the devices and may eventually cause a malfunction and failure of the equipment. All commercial CMOS devices incorporated an ESD protective network to the input pads. Diode leakage in the input protective networks has been used to study the ESD damage.

By studying the slope of forward-biased ESD diode I-V characteristics, a new method is proposed to detect the ESD damage degraded devices before the circuit fails functionally. From the I-V characteristics of the ESD diode, ideality factor has been calculated from experimental results for before and after ESD exposure. It was found that the ideality factor increases with the ESD exposure voltage. From this method, the amount of ESD exposure can be predicted even though the circuit performs normally. This method can be used effectively to detect ESD degraded devices that would indicate improper handling during manufacturing or later.

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1. INTRODUCTION

When two dissimilar insulating materials are brought in contact by rubbing or are separated rapidly, one tends to attract electrons away from the other. As a result of the charge separation each develops a different voltage level. Certain combinations of materials when rubbed together or separated can achieve potential differences of thousands of static voltages.

Electrostatic discharge (ESD) occurs when a highly charge body approaches a conducting or oppositely charged object. The most dramatic and dangerous form of ESD is atmospheric lighting. ESD strikes take only a fraction of microsecond and can destroy electronic devices or weaken the device so they will fail prematurely. Most people have had experience with ESD on cold, dry winter days when the relative humidity in the room is less than 40 percent. Simply walking on a carpeted floor and touching a metal doorknob or key can result in a stinging shock on the finger closest to the metal object. Electrostatic charge on a body can be imparted to another object through induction and conduction It is very common for a person to have a voltage of 8 kv to 10 kv [1]. Unfortunately humans cannot feel fields or discharges less than a few thousand volts, but 2 kv is certainly more than sufficient to damage many electronic items.

Electrostatic discharge accounts for a majority of over stress transients, most of them used to occur in factories that make electronic devices. In the past, electrostatic discharge was most commonly generated by assembly line workers who

acquired a static charge in handing devices or circuit boards. The devices themselves may become electrically charged when they slide through plastic storage tubes, then discharge when they hit a conducting surface or person who unpacked without any ESD protection. Most companies have very good ESD protection programs today and damage in production is now very unlikely.

ESD damaged semiconductor devices can latch-up computer systems. Manufactures are under pressure to design and add more functions on a IC resulting in more transistors per unit area. In addition all designers are working toward higher speed and lower power consumption per device particularly in very large integrated circuits. Smaller devices and thinner oxides make modern complementary metal oxides semiconductors (CMOS) and GaAs devices even more susceptible to destruction then the earlier generation of bipolar devices.

In the past, ESD damage in electronic devices was one of the most significant problems plaguing the electronic industry. Some cases of damage can still happen due to handling errors. In end products such as medical or life support equipment failure of system could result in losing life, in process control equipment, it could cause property damage.

Therefore, original equipment manufactures provide external and internal networks to protect from ESD damage. Even these networks do not provide complete protection because they can be damaged or destroyed by voltages more than 2000 volts, but still below the human perception level. The network might provide only 'one-shot' protection and a component could be destroyed by the first over voltage

encountered. After that the device is no longer protected for ESD even from a lower second transient.

All CMOS devices incorporate various ESD protective circuits for signal input and output. The most widely used protective networks are a combination of diodes, resistors, capacitors, latching devices, and field FET's. In a typical input protective network for a CMOS device, forward-biased diodes that shunt unwanted transients to the supply or to ground. The pulse is clamped at the gate to safe levels less than 20 volts for today's digital devices. These protective networks can be made quite effective, but there is a tradeoff between the amount of protection on the one hand, and device speed and packing density on the other.

Normally, ESD protective networks will protect the more sensitive internal gate structure and not degrade the circuit performance after repeated exposures to ESD. However, exposures to ESD can cause direct, indirect and latent failures in semiconductor devices [2]. Direct failure can be defined as physical destruction or degradation of a device which results from either high amplitude current or voltage ESD pulse and the damage is irreversible. In this case, the damaged device has to be replaced with a good one. For indirect failures, the faults such as false triggering, are introduce as a result of conducted or radiated electromagnetic interference from ESD. Recovery is possible from indirect faults since the device can be reset to its proper state by removing the device power for few seconds. A latent failure is a time dependent failure that produces no detectable degradation of the device at the time of ESD damage. But it may results in a hard failure with subsequent use in normal

operation. This is the most dangerous and hard to detect damage resulting from ESD.

A view of the literature publish on the latent ESD failure shows that there are two different opinions. The first group of researches believe that latent effects occurs only with a very low probability. Other group have reported evidence to support the presence of latent effect by investigating the physics of surfaces and interfaces of MOS devices.

Woodhouse et al [3] reported the failure analysis by exposing devices to approximately 90% of their Human Body Model (HBM) ESD threshold. Although severe physical damage was caused by ESD, no evidence of a latent failure phenomena was found.

However, a model for latent failure due to the cumulative build-up of thermoelectric strains induced by low-level ESD pulses has been proposed by Neellakantaswamy [4]. Dielectric breakdown of MOS capacitors occurs when significant charge is injected into the oxide and this work is reported by Wolters et al [5-6]. The breakdown of thin SiO_2 gate dielectric have been measured [7-8]. The dependence of ESD voltage on device structures of p-n junctions and insulated films has been reported by Meada [9]. Therefore, degraded devices due to latent failures are a major concern because they are not easy to detect like damage parts, but may significantly affect the reliability of an entire system.

Two methods, namely quiescent current (I_{DDQ}) and capacitance-voltage (CV) measurements, have been used to detect the degraded devices due to latent failures. The quiescent current measurement method measures the power supply current during

the circuit quiescent state [10-11]. Typically, in CMOS technology this current is less than 10 nA and defects such as charge trapping, gate oxide shorts, and parasitic transistor leakages in the circuit can increase the quiescent current. Therefore, this method is not a good method to detect the degraded devices due to ESD damage.

CV measurement can disclose the doping profiles of the material used in the devices and the oxide and interface characteristics which may be influences by stress, device damage, annealing or interface traps [12-13].

These two methods help to detect the degraded devices but are not useful to isolate the ESD damage. This paper describes a method to detect minor ESD exposure and correct handling problems before they become serious. Basic ESD protected circuits contain few ESD diodes either connected to the positive power supply (V_{DD}) or connected to the negative power supply (V_{SS}) voltage. Figure 1.1 shows a simple ESD protected circuit connected to the input pad. Input and output pads are critical because they can be contacted directly by external sources such as ESD.

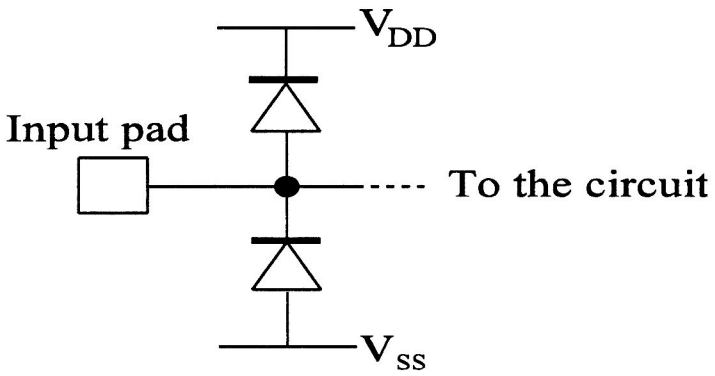

Figure 1.1. Typical input protective network.

These ESD diodes are the major parts in the input protective network that shunt the ESD pulse to the ground or to the power supply. Even though less intense ESD pulses are unable to damage the ESD diodes it will degrade the ESD diode to some extend. Previous research on p-n junctions exposed to ESD pulses shows degradation of the p-n junction [9,14].

For this investigation the forward-biased ESD diode characteristic will be studied to determine how much the diode deviates from ideal performance due to the exposure of ESD. The human body model is used to generate the ESD[15]. Increased reverse current leakage is a common indication of a damaged diode junction but this parameter is very sensitive to temperature and subject to drift with time and from device-to-device due to process variations. The slope of the I-V characteristic of the ESD diodes will be calculated over a range of voltages. The ideality factor 'n' will be calculated and compared with before and after ESD damage. For a ideal diode n is approximately one. Simple circuits have been proposed to measure this parameter independent of temperature effects and absolute current levels.

2. THEORETICAL BASIS

Consider the forward biased ideal diode equation. The ideal diode equation is given in equation 1.

$$i_D = i_O \left[e^{\frac{v_D q}{nkT}} - 1 \right] \qquad (1)$$

Where i_D is the diode current, v_D is the voltage across the diode, k is Boltzmann constant, T is the absolute temperature in degree Kelvin, and q is the charge in coulombs. Here 'n' ideality factor has been introduced to the diode equation. It is a measure of a deviation from the ideal behavior. The diode is more closely approximated to the ideal behavior when n equals one. The reverse saturation current i_O is very unpredictable for real devices due to the surface leakage current and very sensitive to temperature.

Figure 2.1 shows the current voltage characteristic of a ideal pn junction. The diode breakdown occurs when $v_D < -v_k$. Normally at room temperature T=293.16 ^{0}K, k=1.38 x 10^{-23} J/ ^{0} K, and q=1.6 x 10^{-19} C gives kT/q=25.3 mV. In the forward biase region where $v_D \approx 0.4$ to 0.6 volts equation 1 can be approximated to the equation 2. Where $v_D >> nkT/q$

$$i_D = i_O \, e^{\frac{v_D q}{nkT}} \qquad (2)$$

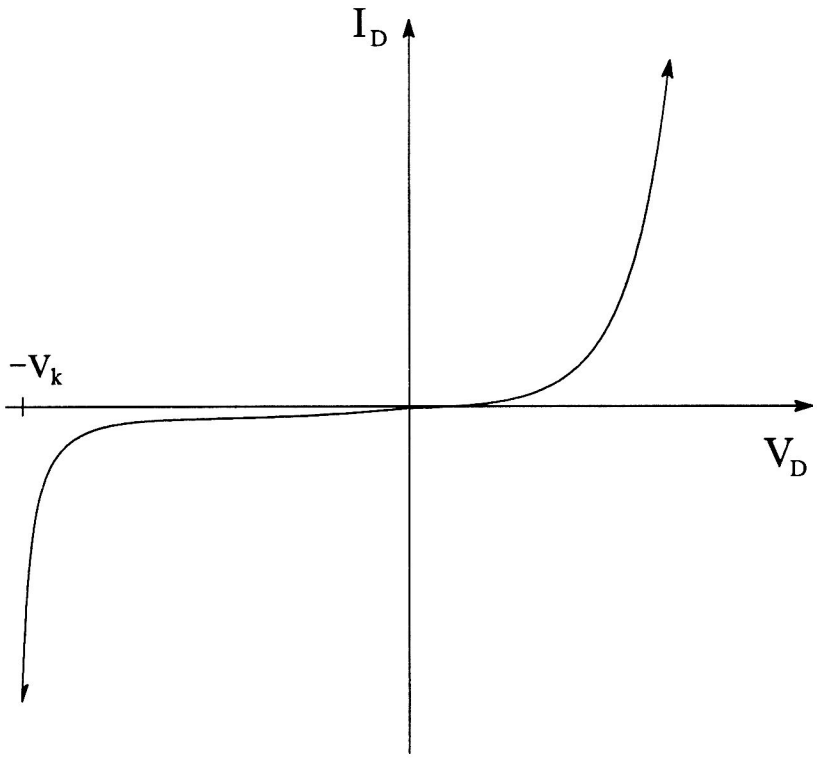

Figure 2.1 The I-V characteristic of an ideal p-n junction diode

By taking the natural logorithemic of both sides of the equation 2, we can write equation 3.

$$\ln(i_D) = \frac{q}{nkT} v_D + \ln(i_0) \qquad (3)$$

There is normally a linear region in the plot of $\ln(i_D)$ vs v_D when $0.4 < v_D < 0.6$ volts. Slope$=d[\ln(i_D)]/dv_D$ of that linear region (q/nkT) can be used to calculate the ideality factor 'n'. During the experiment the room temperature is measured and used to calculate the kT/q factor. Therefore 'n' is given from the equation 4.

$$n = \frac{1}{slope \ \frac{kT}{q}} \qquad (4)$$

The ideality factor 'n' can be determined before ESD exposure and after ESD exposure. By comparing the n values (before and after ESD) for a particular device for a particular input pad we can determine if a pin has been exposed to ESD.

3. EXPERIMENTAL METHOD

For this study CMOS inverters (part # HEF4049BP) were used. These IC's were selected because it has a simple input protective network and also it is easy to check the gate functionality. In the first part of the experiment unexposed new devices were obtained and unpacked. Unpacking and all device handling is done on a grounded ESD protective mat and wearing a grounded wrist band. In this way devices were transferred to a metal box which is initially ground to earth. These necessary ESD precautions were taken so that all devices were unexposed to the ESD damage once it arrived to the lab. After careful handling each gate is characterized by measuring I-V curves. The circuit diagram for the I-V measurements is shown in the figure 3.1.

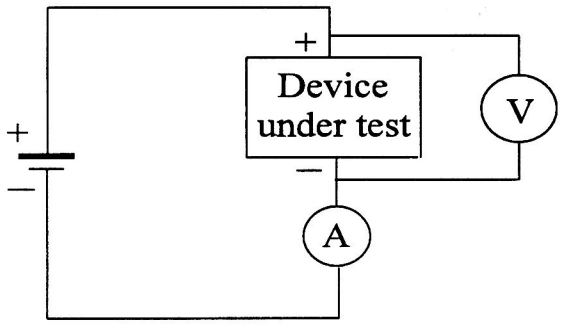

Figure 3.1. Circuit diagram to measure I-V characteristic

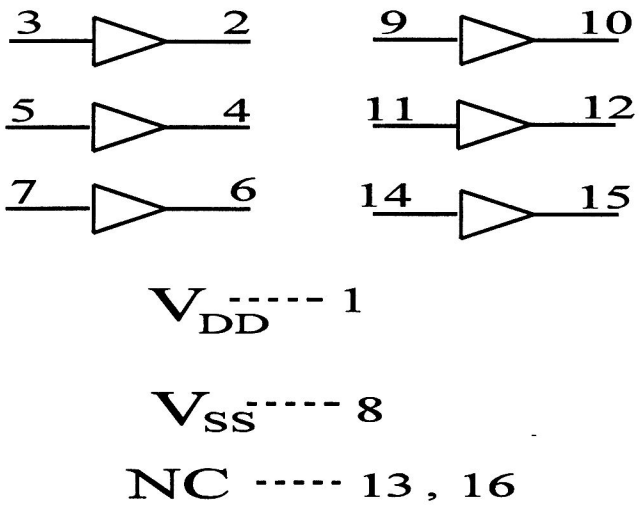

Figure 3.2a. Pin connection for the IC # HEF4049BP, inverters.

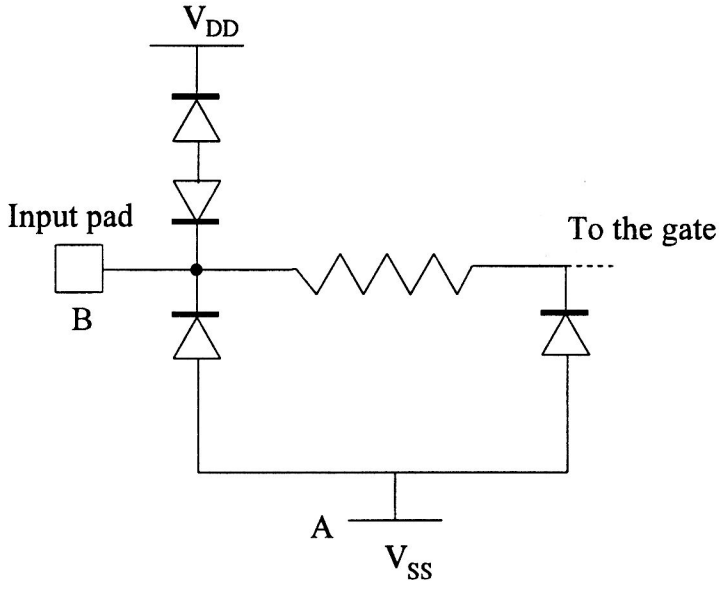

Figure 3.2b. Input protective network in HEF4049BP.

The sample space contained 12 IC's and each IC has six inverters. The protective network and the pin layout is shown in the figures 3.2a and 3.2b. These IC's were marked from device #1 to #12 for identification. The voltage across A-B (as shown in Fig.3.2b) and the current flow through the diode was measured using a volt meter (Keithley 199 DMM) and a ammeter (Fluke 8050A DMM, 200μA range). A plot of $\ln(i_D)$ vs v_D for the devices numbered 1, 6, and 12 and input pad #3 is shown in figure 3.3.

The ideality factor 'n' is calculated and tabulated in table 3.1 by fitting a straight line for the linear region of the $\ln(i_D)$ vs v_D curves. Linear region is chosen from 0.40 to 0.58 volts for all devices.

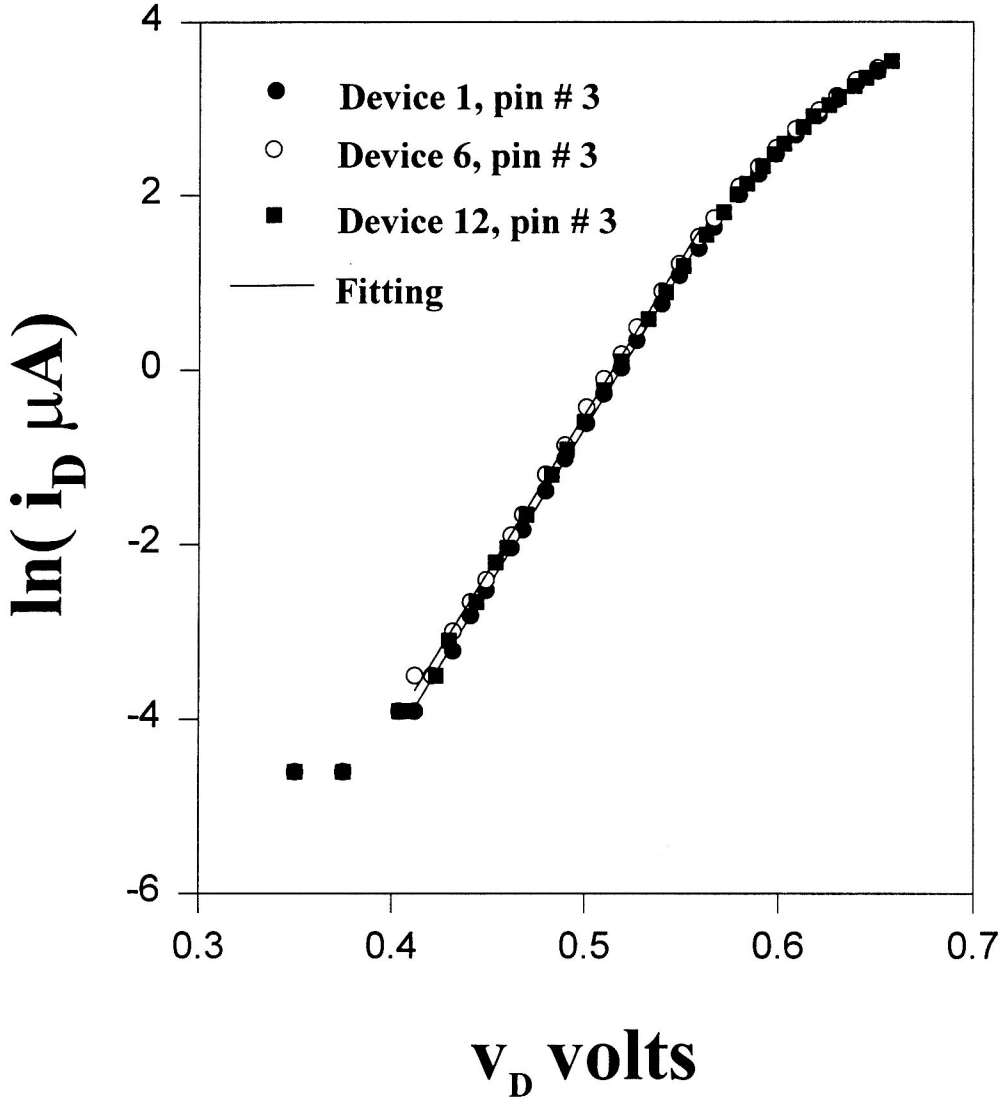

Figure 3.3. A plot of $\ln(i_D)$ vs v_D for three devices (1, 6, and 12) before ESD application. Here current i_D is in micro amperes.

Device Number	Ideality Factor 'n'							
	Device Input Pad Number							
	3	5	7	9	11	14	Average	Std.Dev.
1	1.08	1.09	1.08	1.09	1.08	1.08	1.083	0.005
2	1.06	1.07	1.07	1.08	1.08	1.07	1.072	0.007
3	1.09	1.09	1.09	1.09	1.09	1.09	1.090	0.000
4	1.09	1.09	1.09	1.09	1.09	1.09	1.090	0.000
5	1.09	1.09	1.09	1.09	1.08	1.09	1.088	0.004
6	1.08	1.08	1.09	1.09	1.09	1.09	1.087	0.005
7	1.18	1.18	1.18	1.18	1.17	1.18	1.178	0.004
8	1.16	1.16	1.15	1.15	1.16	1.16	1.157	0.005
9	1.15	1.15	1.16	1.15	1.15	1.16	1.153	0.005
10	1.09	1.10	1.10	1.09	1.09	1.09	1.093	0.005
11	1.18	1.18	1.17	1.18	1.18	1.18	1.178	0.004
12	1.07	1.07	1.08	1.08	1.07	1.07	1.073	0.005

Table 3.1. Calculated n values before ESD application.

These measurements were done at room temperature ($22^0 \pm 1^0$ C) and this temperature was used for the 'n' value calculations. Figure 3.3 and Table 3.1 shows that the ideality factor 'n' change from device to device is insignificant. For a ideal diode this value should be one. However, for a real diode this can differ from one. The average value calculated for the above listed gates was 1.11 ± 0.04. Standard deviation also a good parameter to check the ESD exposure. In this case, small

standard deviation implies that devices are unexposed to ESD.

There are three generalized models that describe the type of ESD affecting semiconductors. When the charged object is a person, this is called the Human Body Model (HBM). In the second part of the experiment human body model is used to "zap" the devices. Simple HBM circuit is shown in figure 3.4.

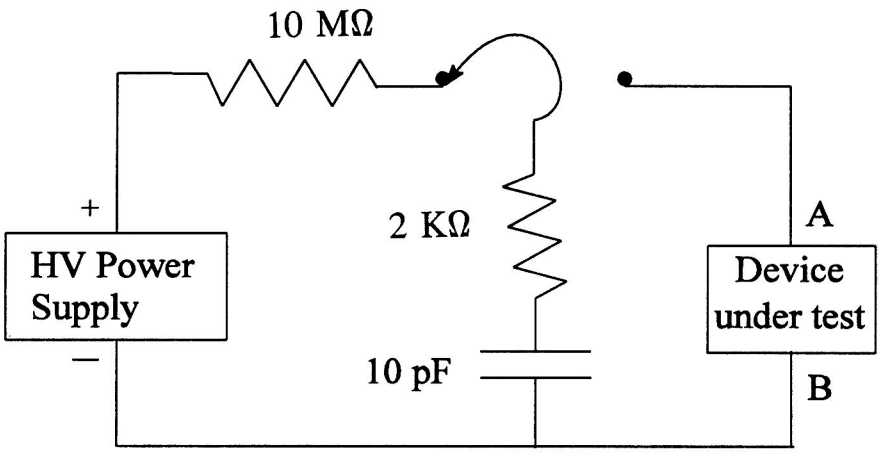

Figure 3.4. Human Body Model used to generate the ESD (manual control switch).

Electrostatic discharge from a human body can be modeled by using a high-voltage, low leakage capacitor (10 pF) and a resistor (2KΩ) in series and charging to the required voltage. A high voltage power supply was used to charge the capacitor through a 10MΩ resistor and then discharge to the device under test. The switching between charging and discharging was done by manually. This may not consistent because of the leakage of the capacitor voltage and a switch is recommended Table

3.2 shows the voltage applied to each device.

ESD Voltage (volts)	Device Number
500	1, 2, 3
1000	4, 5, 6
1500	7, 8, 9
1800	10, 11, 12

Table 3.2. Applied ESD voltage for each device.

In each ESD test three devices were exposed to the voltage shown in the table 3.2. In each device, all input pins were zapped except the pin #14. This way, each device has one gate that is not exposed to the ESD. To zap a input pin, first connected the input pin to the ground and apply the discharge voltage (ESD) through the pin # 8 (pin # 8 is v_{SS}). In this way ESD diode is in forward baise for the positive ESD pulse. After the ESD damage all devices were left at room temperature for 24 hours. This will ensure that the heat generated from the ESD damage will dissipate and the temperature of the gates inside the IC is same as the room temperature.

All devices were again tested for the I-V characteristics and the behavior is shown in figures 3.5 and 3.6. In each plot before and after ESD damage is shown for a particular device and pin # 3. Solid line is a linear fit for the data points in the voltage range (v_D) 0.4 to 0.58 volts.

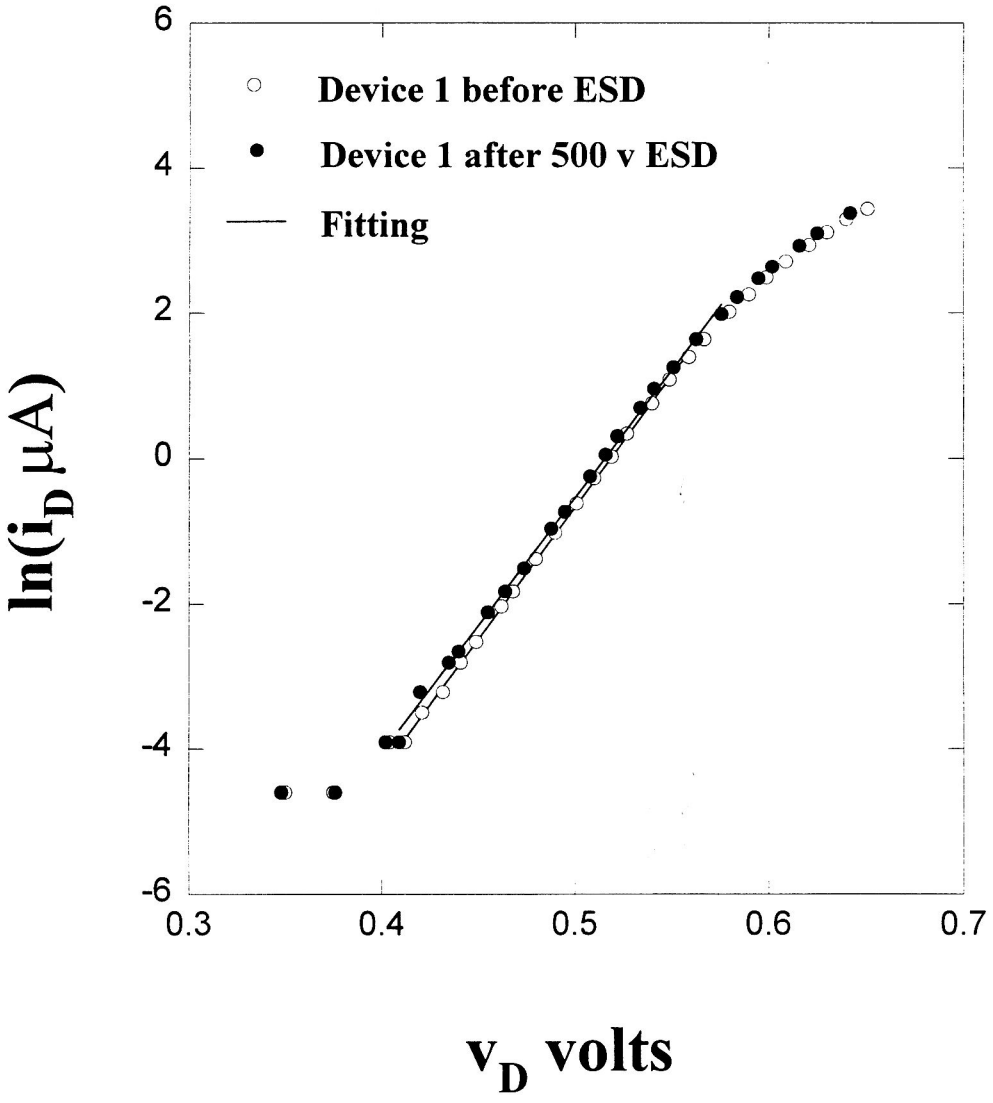

Figure 3.5. A plot of $\ln(i_D)$ vs v_D for devices #1 before and after ESD exposure showing little damage. Here current i_D is in micro amperes.

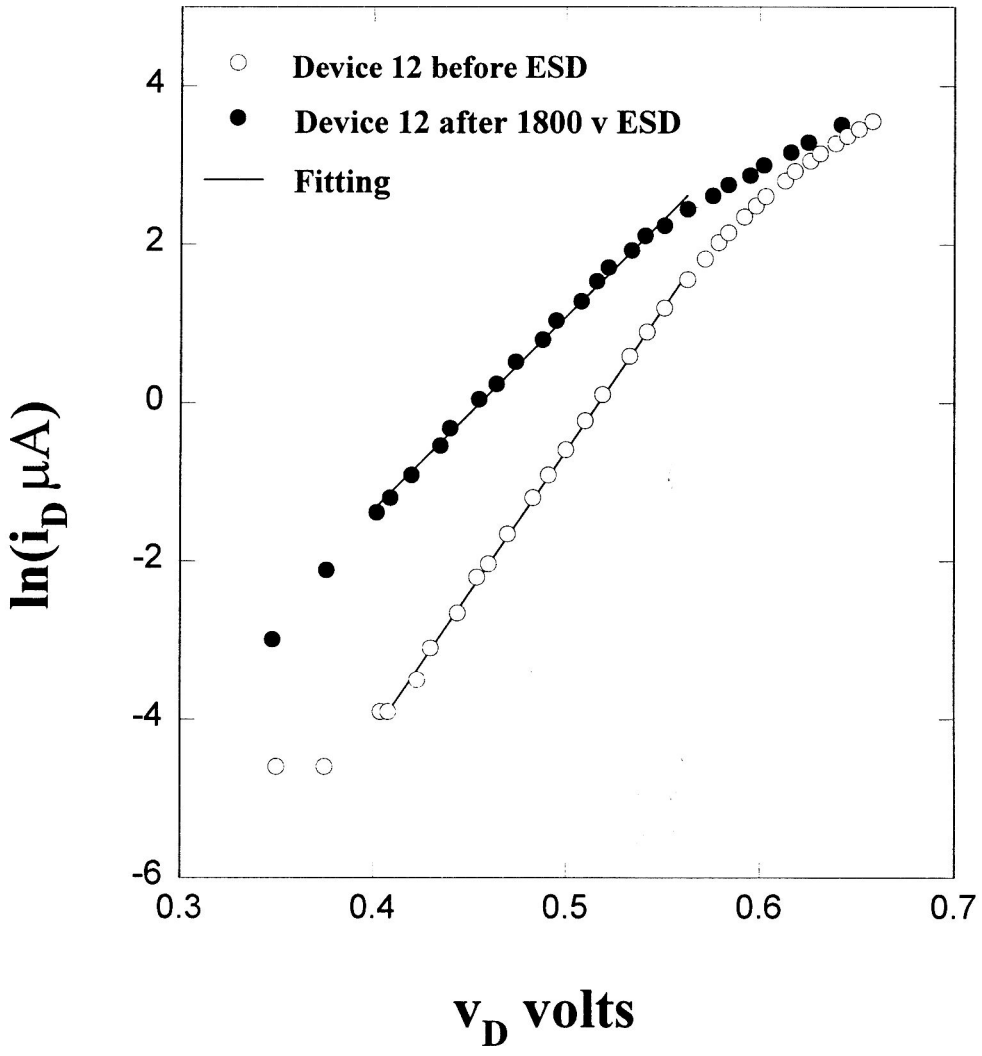

Figure 3.6. A plot of $\ln(i_D)$ vs v_D for devices #12 before and after ESD exposure.

Figure 3.6 is obtained for the device #12 and applying a 1800 volts of ESD. It shows that I-V characteristic has changed due to permanent ESD damage.

4. RESULTS

Figure 3.6 clearly shows that after application of ESD that the slope decreased and 'n' is inversely proportional to the slope. Therefore value of n increases with the ESD exposure above a threshold of about 500 volts. The average value for n is calculated and compared with before and after ESD damage. Results are tabulated in table 4.1.

ESDVoltage volts	Average 'n' before the ESD	Average 'n' after the ESD
500	1.08	1.13
1000	1.09	1.66
1500	1.17	3.08
1800	1.11	4.12

Table 4.1 Calculated average values for n.

From the table 4.1 it is clear that ideality factor 'n' has increased due to the ESD exposure. Only other factor that can change the slope is the temperature. This possibility is ruled out because we checked the I-V characteristics after 24 hours from ESD damage. For an apparent change of n from 1.09 to 1.66 the device has to be at temperature of about 200 C. Therefore, the observed change of n is only due to the ESD exposure. From all devices used in this experiment only two gates were not

functional damaged after ESD exposure. Also the unexposed pin #14 in each device was check for the 'n' values and found that it is close to the value found before ESD exposure. Calculated values of n for each device were tabulated in appendix A.

The amount of ESD exposure depends on several factors. Specially it depends on the ESD voltage. The discharge voltage from the HBM may not be as high as the charging voltage due to the capacitor leakage. As a result, 'n' can be fluctuate from one gate to another for a particular ESD voltage (see Appendix A). This could be minimize by using a switch to control the charging and discharging instead of manual control. By calculating a average value for n for a particular ESD voltage, we can compare the ESD exposure. Figure 4.1 shows the relation between the average n and the ESD voltage. The solid curve is a fitting using $n = A \exp(Bv)$, where A and B are fitting parameters, v is the ESD voltage, and n is the ideality factor. The fitted values were A=0.6193 and B=0.00106. Perfect fit to the data points suggest that ideality factor is exponentially increased with the ESD exposure voltage. These results can be used to predict the amount of ESD exposure of a particular device by just measuring the value of n.

The approximation $v_D >> nkT/q$, is made under the assumption that n is closed to one. However, higher ESD voltages will increase the value of n. For larger values of ESD exposure we can used the eqa. 1 without any approximations to fit the data and from the fitting n can be calculated. The damage to the diode will create leakage and other problems that will make the diode equation less valid, but the change in the effective value of n is still a good indication of ESD exposure.

This experiment performed only for one type of IC. In future this experiment could be extended to check different types and manufacturers of devices and also building a simple circuit to measure the value 'n' independent of temperature.

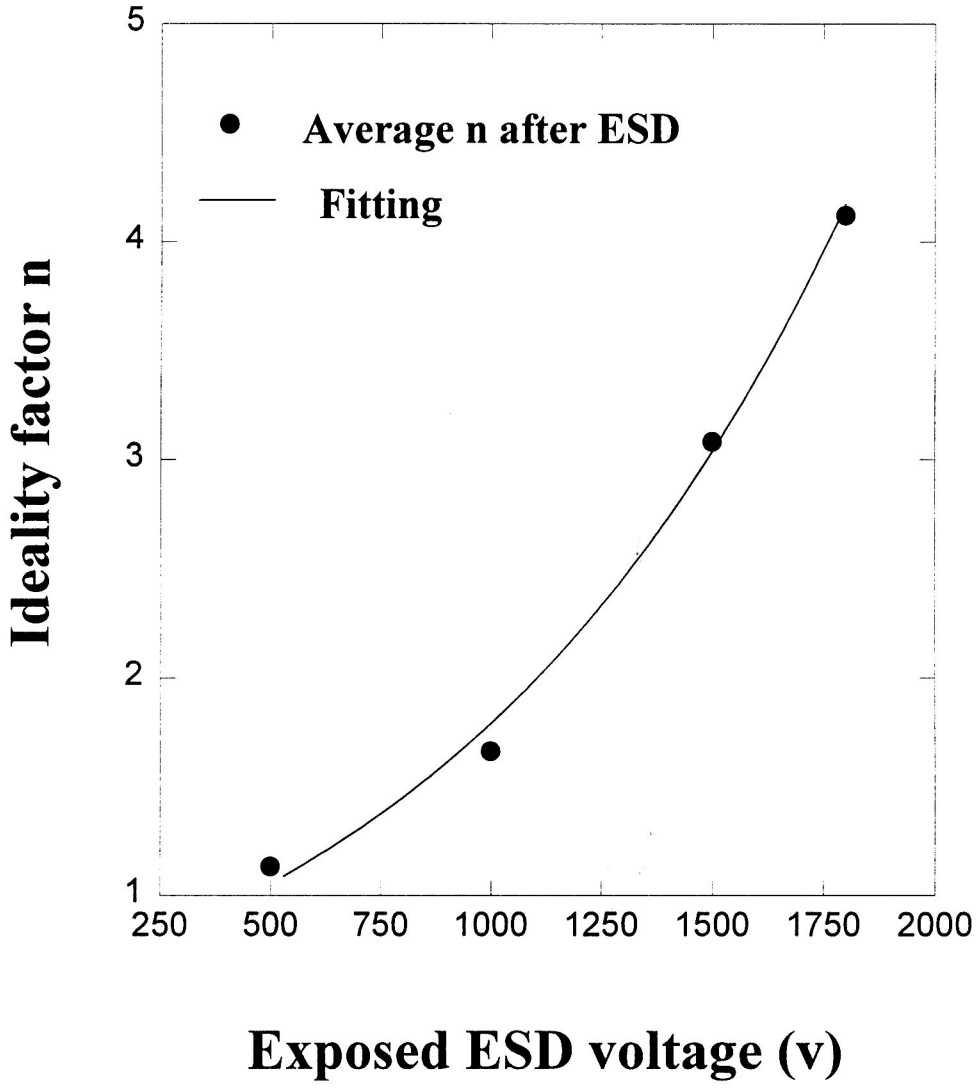

Figure 4.1. A plot of average n vs ESD voltage (after ESD exposure).

5. CONCLUSIONS

The input protective network in CMOS devices was used to predict the ESD exposure. I-V characteristics of the ESD diodes were used to calculate the ideality factor before and after ESD exposure. The calculated ideality factor, before the ESD exposure, was close to the expected value one. As expected, after ESD exposure the ideality factor increased to a higher value. It was found that the ideality factor 'n' was exponentially proportional to the applied ESD voltage. As a conclusion, ESD diodes in the input protective network can be used to determine if a device input pin has been exposed to ESD. Devices will function properly after modest ESD exposure but this method will provide a valuable audit tool to sample products to monitor ESD prevent methods used during fabrication, testing and shipping.

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APPENDIX A.

Calculated n values for all devices before and after ESD exposure. Pin # 14 is unexposed to ESD.

Device #1, ESD=500 v			Device # 2		Device # 3	
Pin #	Before	After	Before	After	Before	After
3	1.08	1.15	1.06	1.14	1.09	1.10
5	1.09	1.15	1.07	1.14	1.09	1.09
7	1.08	1.15	1.07	1.14	1.09	1.11
9	1.09	1.14	1.08	1.14	1.09	1.08
11	1.08	1.14	1.08	1.19	1.09	1.09
14	1.08	1.09	1.07	1.10	1.09	1.08

Device # 4, ESD=1000v			Device # 5		Device # 6	
Pin #	Before	After	Before	After	Before	After
3	1.09	1.60	1.09	1.57	1.08	2.36
5	1.09	1.48	1.09	1.54	1.08	1.87
7	1.09	1.67	1.09	1.63	1.09	1.27
9	1.09	1.67	1.09	1.27	1.09	1.85
11	1.09	1.77	1.08	1.66	1.09	1.74
14	1.09	1.07	1.09	1.08	1.09	1.10

Device #7, ESD=1500 v			Device # 8		Device # 9	
Pin #	Before	After	Before	After	Before	After
3	1.18	2.18	1.16	Bad	1.15	1.87
5	1.18	1.64	1.16	4.91	1.15	1.78
7	1.18	1.4	1.15	13.08	1.16	1.63
9	1.18	1.68	1.15	1.64	1.15	1.71
11	1.17	1.66	1.16	3.91	1.15	1.31
14	1.18	1.11	1.16	1.15	1.16	1.15

Device #10,ESD=1800v			Device # 11		Device # 12	
Pin #	Before	After	Before	After	Before	After
3	1.09	2.45	1.18	1.64	1.07	1.51
5	1.10	6.45	1.17	1.21	1.07	1.61
7	1.10	3.19	1.18	18.12	1.08	3.27
9	1.09	5.61	1.18	1.64	1.08	1.96
11	1.09	4.93	1.18	Bad	1.07	1.57
14	1.09	1.15	1.18	1.15	1.07	1.12