

**INTERFACE DESIGN FOR HIGH SPEED DATA TRANSMISSION AMONG
A TI AD CONVERTER, A NOVA 1200 COMPUTER, AND A PEC RECORDER**

by

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CHAPTER I

INTRODUCTION

The purpose of this paper is to study the interface design among a TI Model 848 Analog-to-Digital Converter with Multiplexer, a PEC Model 2807-9 Incremental Write Tape Transport (Recorder), and a DGC Nova 1200 Computer for high speed data transmission.

The AD converter can be operated in Addressable Mode or Sequential Mode. In addressable mode operation, external clock must be used; in sequential mode operation, either external clock or internal clock may be used. The maximum sampling rate is 25641 samples per second for 14-bit data word. The recorder can be operated in speeds from 0 up to 700 steps per second. Nine-track tape must be used. The Nova 1200 computer is a general-purpose minicomputer. It is equipped with a data channel for automatic data transfers. The maximum rates in transfers per second are 833,333 (for data in) and 555,555 (for data out). It is also equipped with an interrupt system allowing any input-output device to interrupt the normal program flow on a priority basis.

The interface designed in this paper is divided into three parts: the Receivers with Device Select Gates, the AD Converter Interface, and the Recorder Interface. The receivers are mainly

used for matching the computer output characteristics. The device selection gates are used for decoding the device selection lines to generate a select level that ensures that only the single addressed device responds to the program. The AD converter and recorder interfaces, each is equipped with a Data Channel Request network, an Interrupt Request network, a Current Address register, a Word Count register, and other devices, are used for the AD converter and the recorder for selfcontrol in addition to being used for matching the input-output characteristics of the machines which they connect to.

In sequential mode with external clock operation, the computer only needs to load the necessary data into the interface, to set ADC BUSY and MTA BUSY, and to treat ECE (Echo Check Error) and TNT (Tape Not Tensioned) if they happen.

Sequential mode with internal clock operation is the same as sequential mode with external clock operation except that the AD converter must be started manually.

In addressable mode operation, except those mentioned in the sequential mode with external clock operation, the computer only needs to offer a new channel address to the AD converter interface or the recorder interface and to set ADC BUSY or MTA BUSY, each time it is asked for such service.

In all types of operations, the data is transferred from the AD converter interface to the computer and from the computer to the recorder interface through the automatic data channel.

To operate this data processing system, either test program or interrupt program may be used, depending on the sampl-

ing rate and the operation mode. In sequential mode or addressable mode with low sampling rate operation, other input-output devices may be included in this system to ~~make~~ use of the large amount of the computer's free time.

This report is comprised of four chapters. Chapter I is the introduction. Chapter II gives the necessary data for the interface design. All data are based on the machines which are now used in the Electrical Engineering Department Digital Computer Laboratory at Kansas State University. Chapter III specifies the interface design. Chapter IV specifies the operation theory and the programming. Two programming examples are given at the end of Chapter IV.

CHAPTER II

INTERFACE REQUIREMENTS

2.1 Analog-to-Digital Converter with Multiplexer

2.1.1 Electrical Specifications

AD Converter

Total system cycle time	39 usec
Paralell digital output	Single rail, 14 bits
Digitization complete output	Level. Occurs after least significant bit established. Remains until next AD command.
Sample pulse width output	Occurs synchronously with sample-and-hold sample pulse

Multiplexer

Number of channel	16, single-ended
Maximum recommended source resistances	1000 ohms
Control inputs	

Characteristics

Logic level	-6v=1, 0v=0
Rise time	≤ 0.5 usec
Pulse width	≥ 2 usec
Fall time	≤ 0.5 usec
Maximum current	± 2 ma at either level
input load	≥ 2.7 kilohms shunted by 50 pf

Signals

Channel address	7-line, single-rail, binary for operation in addressable mode
Address set command	External clock
Sample initiate	Generated internally or supplied externally. Turns selected analog channel on.
External reset	Reset register to channel 0
Mode select	Uses in EXT mode. True level for addressable mode, false level for sequential mode.

Control output

Characteristics

Level	-6v = 1, 0v = 0
Rise time	≤ 0.3 usec
Fall time	≤ 0.3 usec
Maximum current	± 3 ma at either level

Signals

Address set ready	Level
Sample initiate ready	Level
Clock output	3 usec pulse. Occurs 1.5 usec after internal clock or address set command.

2.1.2 External Connections

Data Output

SIGN	J117-2
Bit 1	4

Bit 2	J117-6
Bit 3	8
Bit 4	10
Bit 5	12
Bit 6	14
Bit 7	16
Bit 8	18
Bit 9	20
Bit 10	22
Bit 11	24
Bit 12	26
Bit 13	28
Digitization complete	36

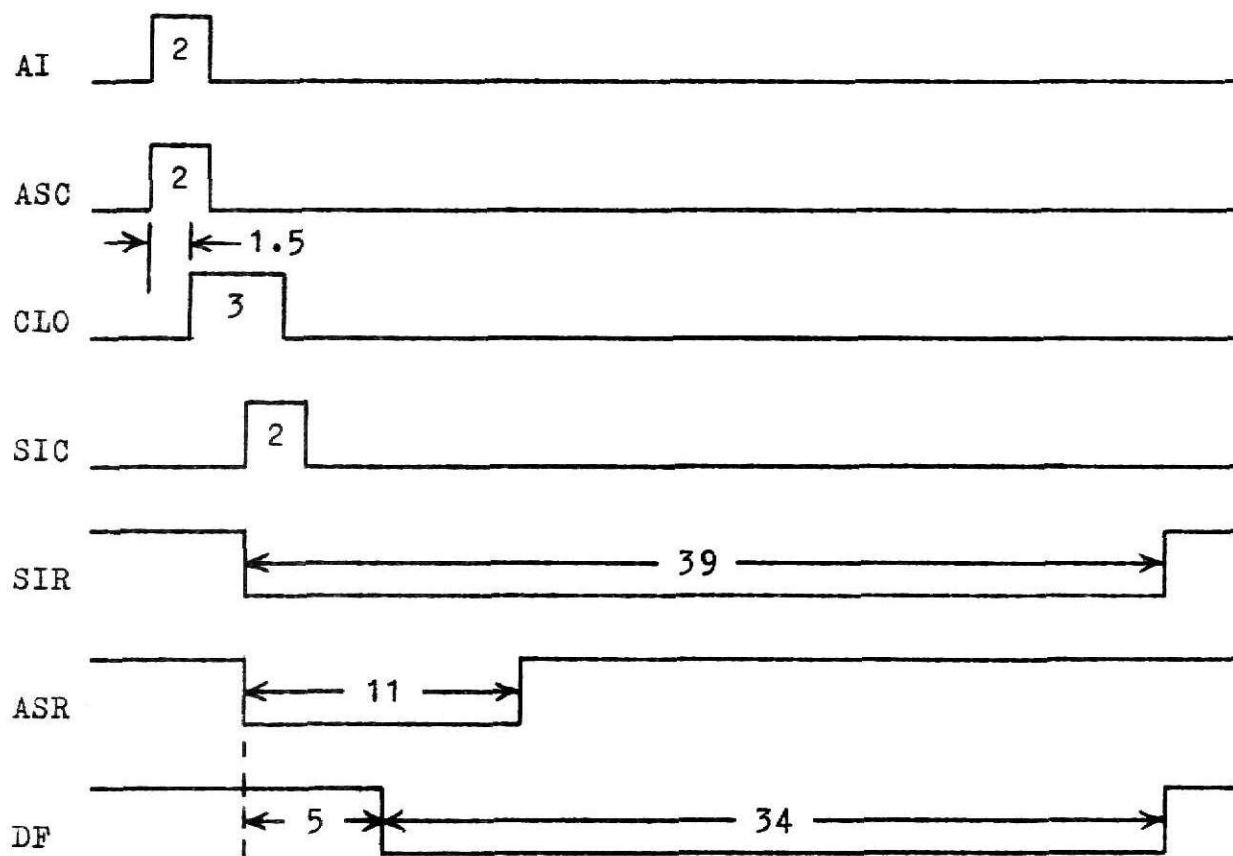
Channel Address and Control Signals

J118-5 ...	2^3
6 ...	2^2
7 ...	2^1
8 ...	2^0
17 ..	Address set ready
18 ..	Address set command
19 ..	Sample initiate ready
20 ..	Sample initiate command
22 ..	External reset command
23 ..	Clock output
25 ..	Mode select

2.1.3 Timing Consideration

Figure 2.1 shows the timing relationships of the various signals which are concerned with the interface design. AI, ASC, CLO, SIC, SIR, ASR, and DF are Address Input, Address Set Command, Clock Output, Sample Initiate Command, Sample Initiate

Ready, Address Set Ready, and Digitization Finish respectively. All times are in microseconds.



(Times not to scale)

Fig. 2.1. Timing diagram ADC

2.2 Nova 1200 Computer

2.2.1 Bus Signals and Connections

The signals are tabulated in TABLE 1 below. For each signal the table lists the direction and panel pin. Any level between 0 and 0.4 volt is regarded as low, more positive than 2.2

volts is regarded as high. A low true signal is indicated by its complement. The direction is indicated by B (bidirectional), D (from processor to device), and P (from device to processor).

TABLE 1
COMPUTER BUS SIGNALS AND CONNECTIONS

Signal	Direction	Pin	Description
CLR	D	A50	Clear
<u>DATA0</u>	B	B62	DATA0-15: Data
<u>DATA1</u>	B	B65	
<u>DATA2</u>	B	B82	
<u>DATA3</u>	B	B73	
<u>DATA4</u>	B	B61	
<u>DATA5</u>	B	B57	
<u>DATA6</u>	B	B95	
<u>DATA7</u>	B	B55	
<u>DATA8</u>	B	B60	
<u>DATA9</u>	B	B63	
<u>DATA10</u>	B	B75	
<u>DATA11</u>	B	B58	
<u>DATA12</u>	B	B59	
<u>DATA13</u>	B	B64	
<u>DATA14</u>	B	B56	
<u>DATA15</u>	B	B66	
DATIA	D	A44	Data In A. Place the A buffer in the device selected by DS0-5 on the data lines.
DATIB	D	A42	
DATIC	D	A54	
DATOA	D	A58	Data Out A. Load the data into the A buffer in the device selected by DS0-5.
DATOB	D	A56	
DATOC	D	A48	
<u>DCHA</u>	D	A60	Data Channel Acknowledge

TABLE 1 -- Continued

<u>DCHI</u>	D	B37	Data Channel In
<u>DCHMO</u>	P	B17	Data Channel Mode **
<u>DCHM1</u>	P	B21	
<u>DCHO</u>	D	B33	Data Channel Out
<u>DCHP IN</u>	D *	A94	Data Channel Priority
<u>DCHP OUT</u>	D *	A93	
<u>DCHR</u>	P	B35	Data Channel Request
<u>DS0</u>	D	A72	DS0-5: Device Selection
<u>DS1</u>	D	A68	
<u>DS2</u>	D	A66	
<u>DS3</u>	D	A46	
<u>DS4</u>	D	A62	
<u>DS5</u>	D	A64	
<u>INTA</u>	D	A40	Interrupt Acknowledge
<u>INTP IN</u>	D	A96	Interrupt Priority
<u>INTP OUT</u>	D	A95	
<u>INTR</u>	P	B29	Interrupt Request
<u>IOPLS</u>	D	A74	I/O Pulse
<u>IORST</u>	D	A70	I/O Reset
<u>MSKO</u>	D	A38	Mask Out
<u>OVFLO</u>	D	B39	Overflow
<u>RQENB</u>	D	B41	Request Enable
<u>SELB</u>	P	A82	Selected Busy
<u>SELD</u>	P	A80	Selected Done
<u>STRT</u>	D	A52	Start
Power on	D		

* Jumper pin A93 to A94 and A95 to A96 if the computer is operated with an interface board removed.

** DCHMO=0 (H) DCHM1=0 (H) Data out
 DCHMO=1 (L) DCHM1=0 (H) Data in

2.2.2 Matching

Every transmitter for transmitting signals to the computer input-output bus should be an NPN transistor which is capable of maintaining a maximum saturated output voltage of 0.5 v and sinking 45 ma. The emitter of the transistor should be grounded, and the collector should be connected to the panel pin directly. An open collector NAND gate which has the same characteristics as mentioned above can be used for this purpose.

Every receiver for receiving signals from the computer input-output bus should be a TTL NAND gate or inverter.

The maximum transmission distance is 50 feet including signal path length inside device and within the processor.

2.3 Incremental Write Tape Transport

2.3.1 Input-Output Signals and Connections

The signals are tabulated in TABLE 2 below. All signals are low-true type. Minimum input pulse width is one microsecond.

TABLE 2

RECORDER INPUT-OUTPUT SIGNALS AND CONNECTIONS

Logic level:

Output: 0 to 0.4v = 1 +5v = 0
 Input: 0 to 0.4v = 1 +3v and above = 0

Signal	I/O	Pin	Description
LFC	I	A	Load Forward Command, level
RWC	I	U	Rewind Command, level
RYC	I	K	Ready Command, pulse
RRS	I	c	Remote Reset, level for duration of reset
DMC	I	m	Disable Manual Control, level

TABLE 2 -- Continued

RGC	I	v	Inter-Record Gap Command, pulse
FGC	I	AD	File Gap Command, pulse
WSC	I	AN	Write Step Command, pulse
WDO	I	AX	WDO-7: Write Data, level coincident with WSC
WD1	I	BF	
WD2	I	BR	
WD3	I	BZ	
WD4	I	CJ	
WD5	I	B	
WD6	I	L	
WD7	I	V	
ECR	I	n	Echo Check Reset, level for duration of reset
EOT	O	D	End of Tape, level for duration of EOT tab
BOT	O	N	Beginning of Tape, level for duration of BOT tab
TNT	O	X	Tape Not Tensioned, level
TRR	O	g	Transport Ready, level
B1B	O	q	Buffer 1 Busy, level while data to be recorded is in Buffer 1 or Buffer 2
GIP	O	y	Gap in Processing, level
ECE	O	AH	Echo Check Error, level

2.3.2 Matching

Every transmitter for transmitting signals to the recorder should be a power NAND gate with a 180-ohm pull-up resistor connected to a +5v source.

Every receiver for receiving signals from the recorder should be an inverter or NAND gate.

The maximum path is 20 feet. The ground side of each twisted pair should be grounded within a few inches of the interface board to which it is connected.

2.3.3 Timing Consideration

Since the interface designed in this paper is mainly designed for high speed operation, the transport will usually run at its rated speed of 700 steps per second. Fig. 2.2 shows the waveforms and timing relationships of Write Step Command, Buffer 1 Busy, Transport Ready, and Encoder Pulse at 700 SPS operation. All times are in microseconds except those time units are indicated.

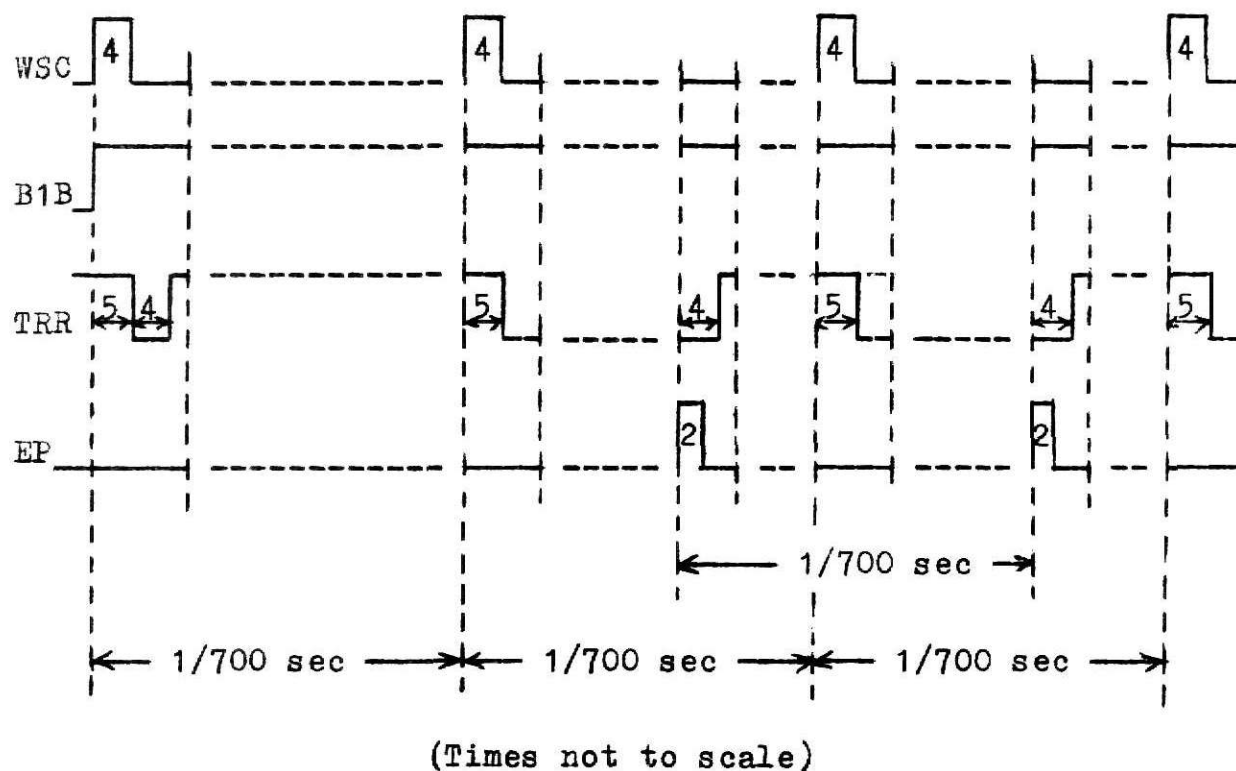


Fig. 2.2. Recorder timing diagram for 700 sps operation

CHAPTER III

INTERFACE DESIGN

3.1 Specifications

The interface design is based on the TI Model 848-B1A-16B-A36 AD Converter with Multiplexer, the Nova 1200 Computer, and the PEC Model 2807-9 Incremental Write Tape Transport with low-true, fast interface. The interface is divided into three parts, the Receivers with Device Select Gates, the AD Converter Interface, and the Recorder Interface.

SN7438 open collector NAND gates are used as transmitters for transmitting signals to the computer. They are also used in the priority circuits. DTL 944 power gates are used as transmitters for transmitting signals to the recorder. 2N2635 PNP and 2N706 NPN transistors are used to change the voltage levels of the signals from or to the AD converter. DGC 4-bit binary counters are used for all counters. SN7495 4-bit shift registers and SN7496 5-bit shift registers are used for data channel buffers. SN series 7400 integrated circuits are used for all other logics.

A small circle at the open end of a line denotes a external connector pin.

3.2 Receivers with Device Selection Gates

Figure 3.1 shows the receivers with device selection gates. Stages 1-20 are the same. Stages 21-40 are the same except stages 21-28 connect to MTAS (Magnetic Tape Select), stages 29-34 connect to ADCS (AD Converter Select), stage 35 connects to MTADS (MTA Data-channel Select), stage 36 connects to ADCDS (ADC Data-channel Select), and stages 37-40 do not connect to any one of the above four lines. Two-input NAND gates are suitable for stages 37-40.

3.3 AD Converter Interface

Figure 3.2 is a signal flow block diagram of the AD converter interface. Figures 3.3-3.9 show the details of the AD converter interface.

Figure 3.3 shows the ADC output signal receivers. Stages 1-17 are the same.

Figure 3.4 shows the ADC input signal transmitters and the analog channel select register (ACSR) with address set command generator. Stages 1-8 are the same.

Figure 3.5 shows the current address register (CAR) with input buffer B (IBB). Stages 1-16 are the same. The 4-input power gate and the 16 open collector NAND gates form the input buffer B.

Figure 3.6 shows the word count register (WCR) with the addressable mode flipflop (AM), sample finish flipflop (SF), and sample initiate command generator. The word count register uses three 4-bit binary counters interconnected as shown in

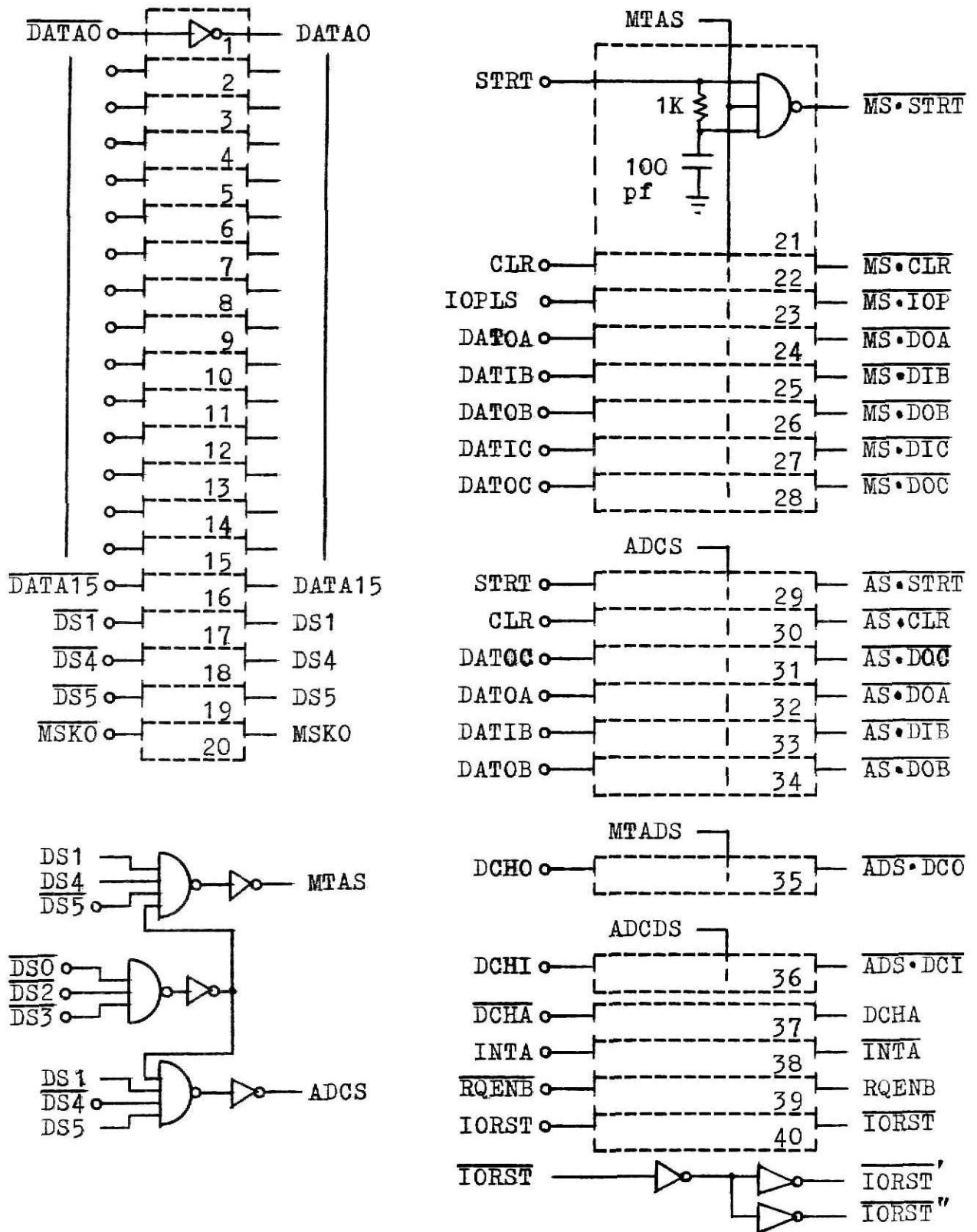


Fig. 3.1. Receivers with Device Selection Gates

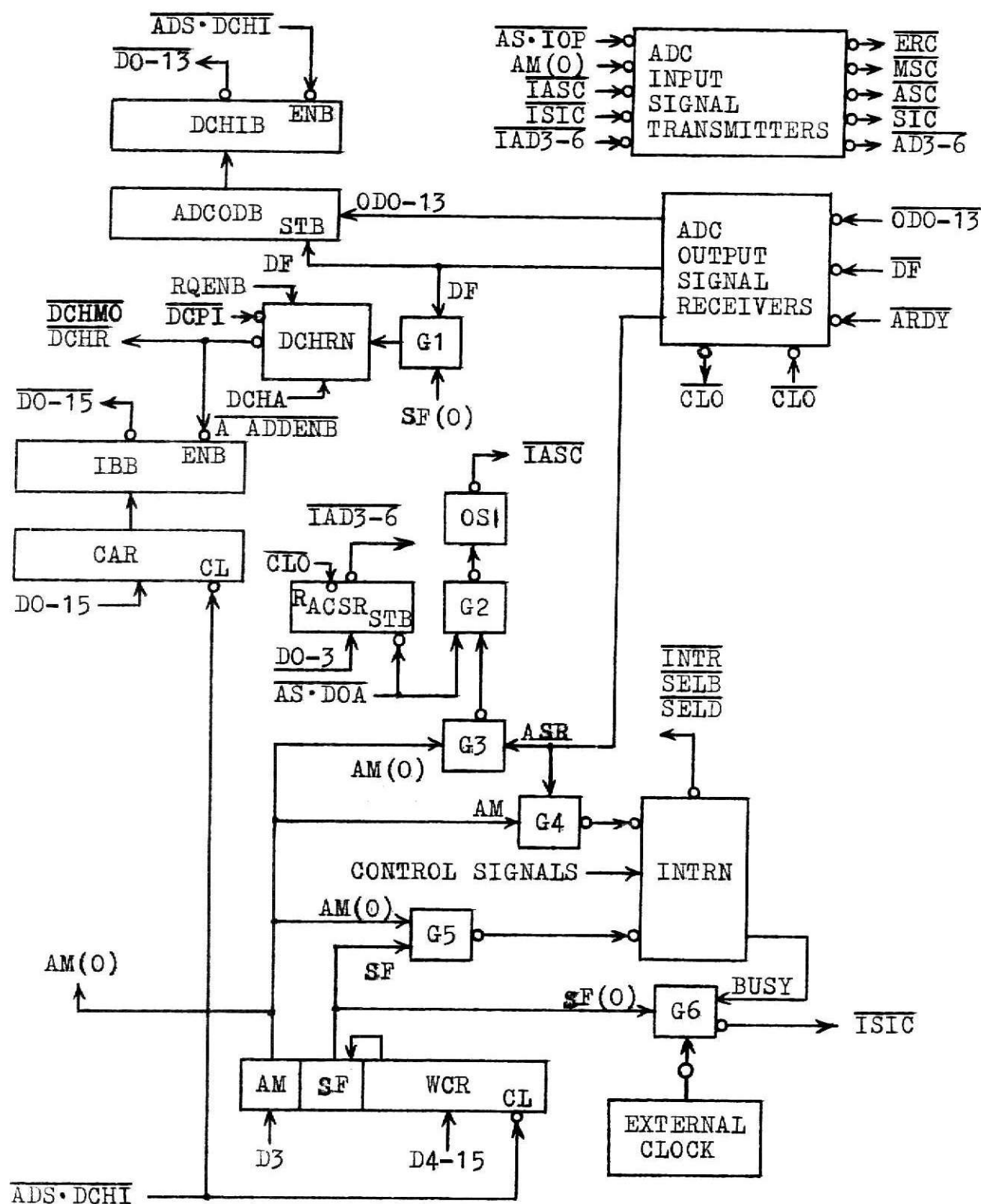


Fig. 3.2. Signal flow block diagram of ADC interface

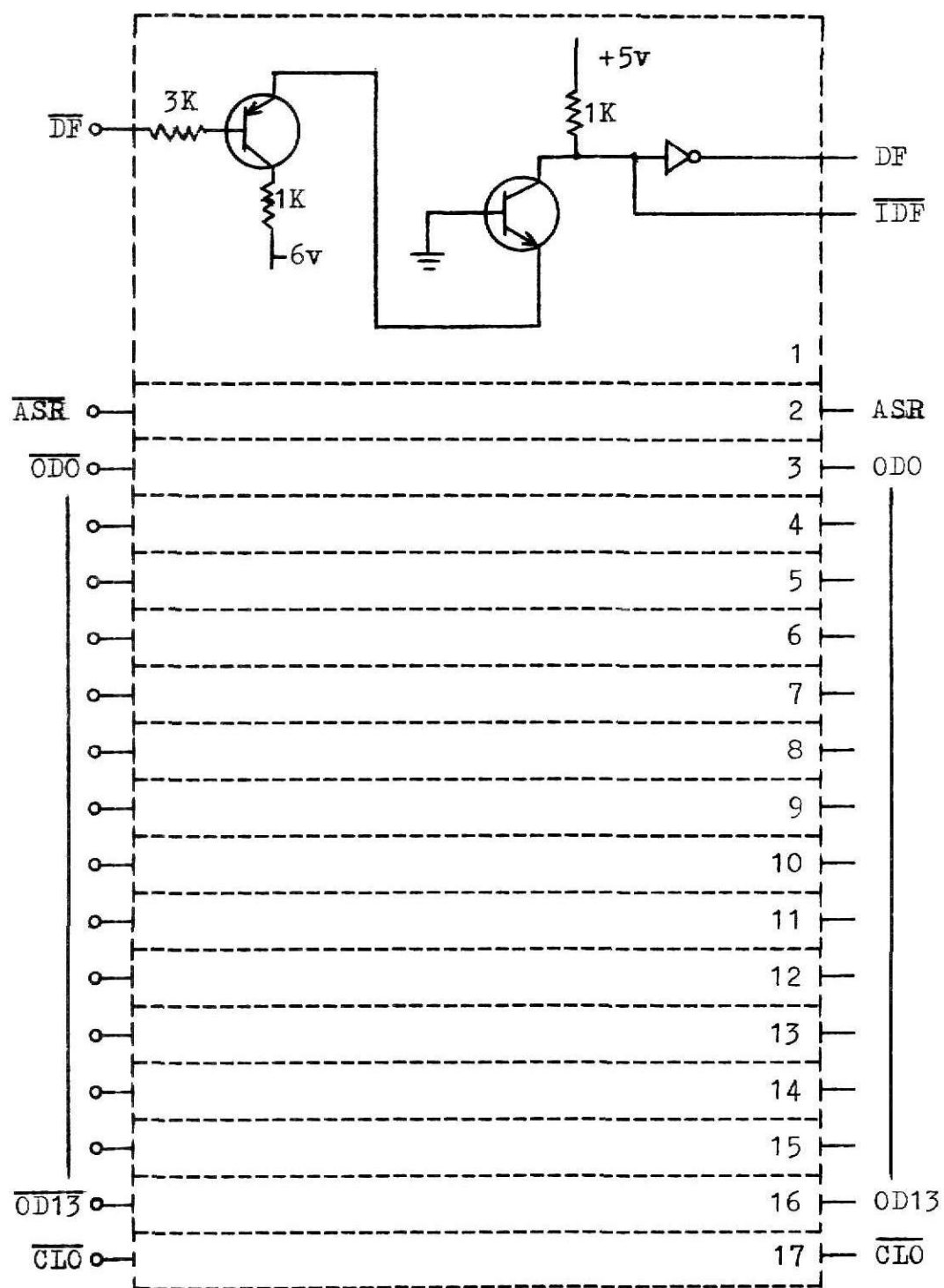


Fig. 3.3. ADC output signal receivers

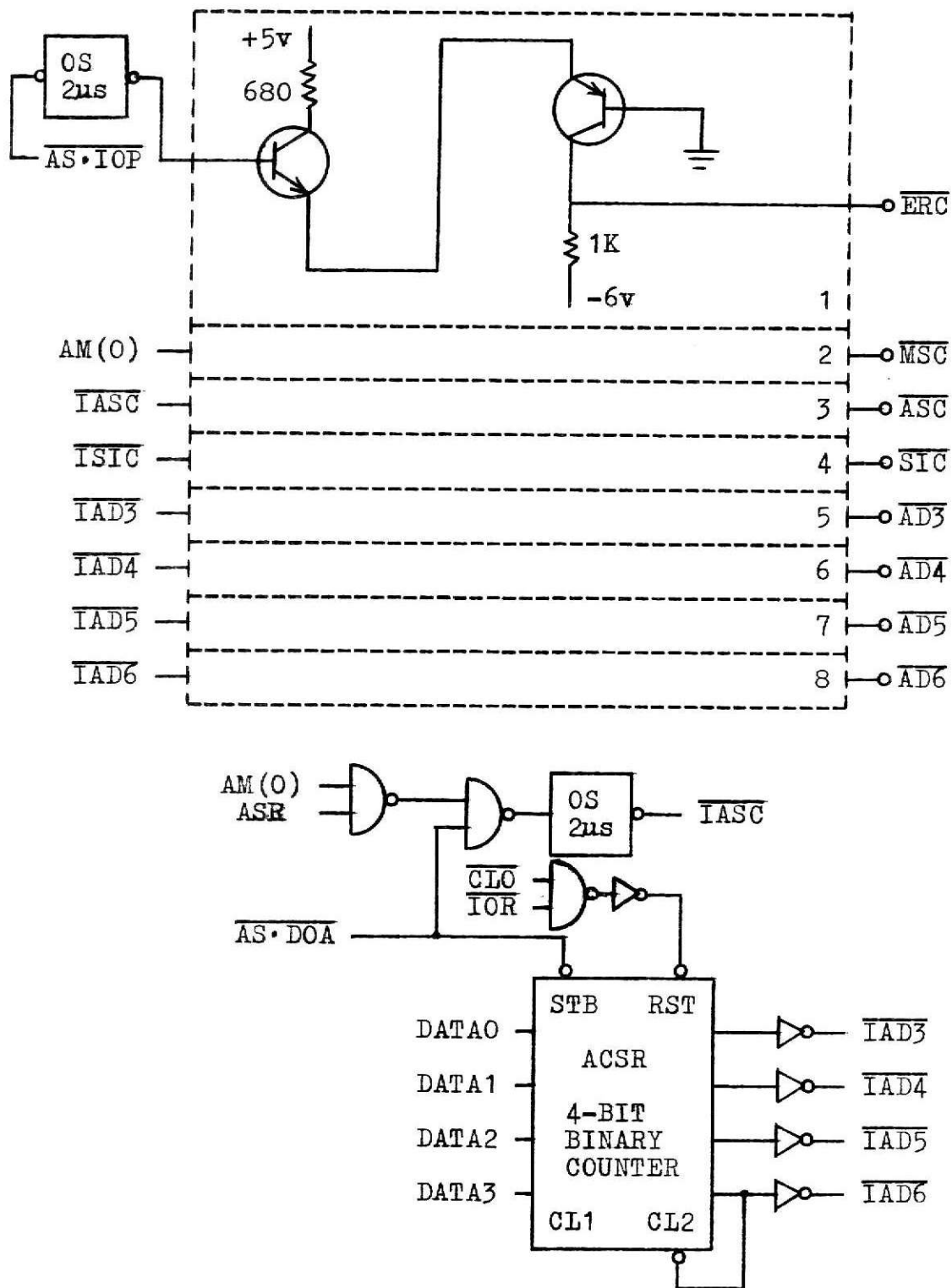


Fig. 3.4. ADC input signal transmitters and analog channel select register with ASC generator

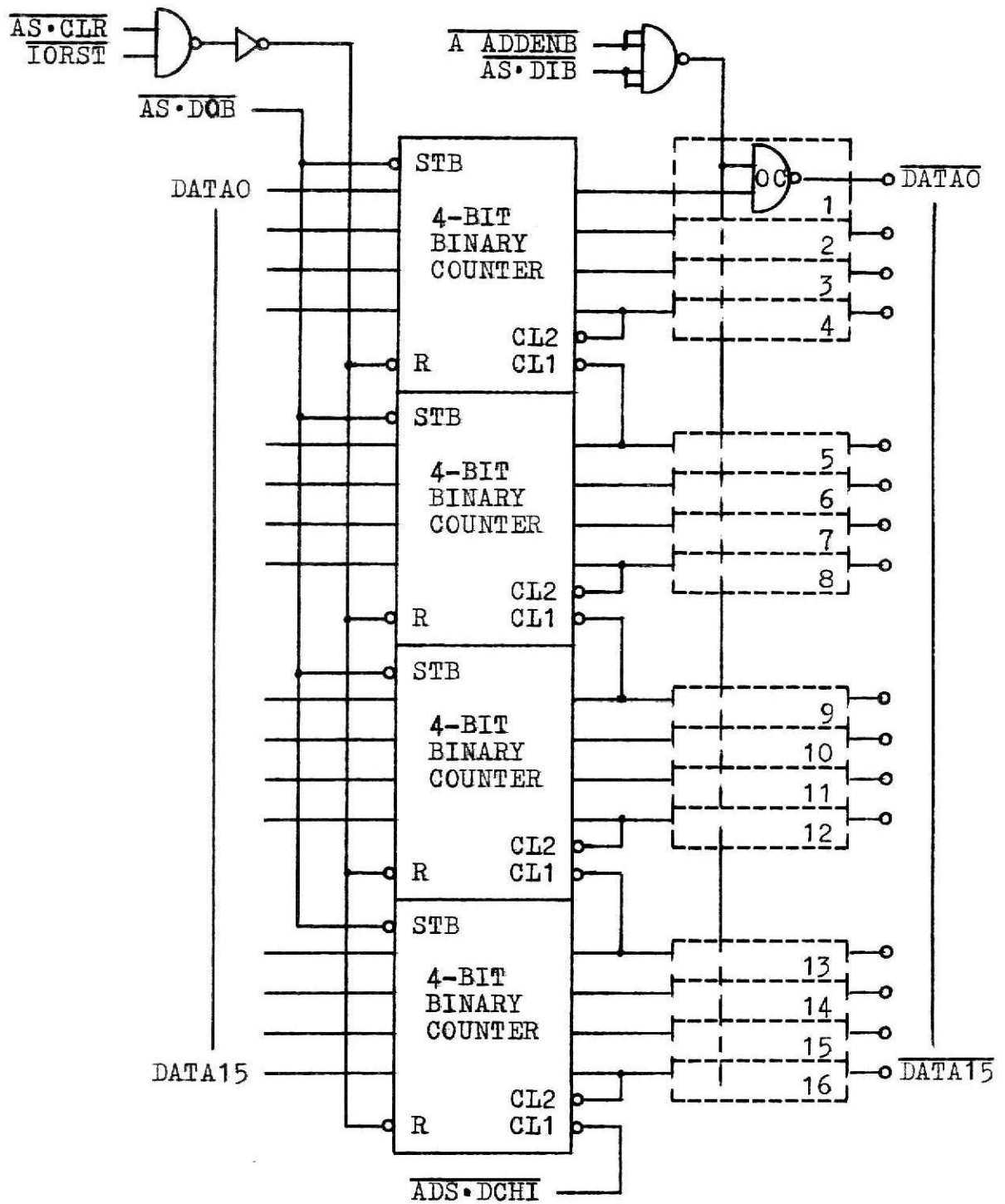


Fig. 3.5. Current address register with input buffer B-ADCI

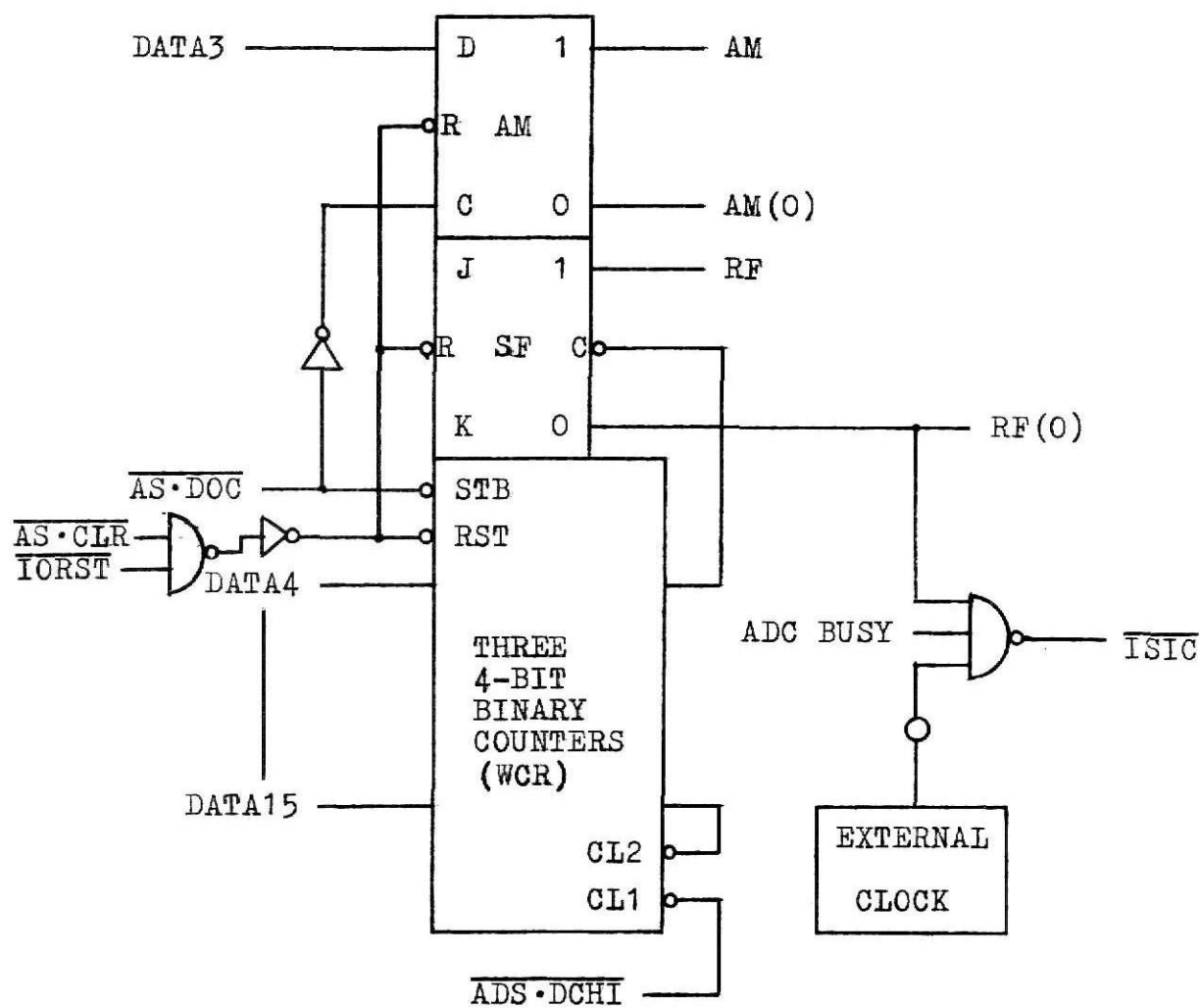


Fig. 3.6. Word count register with AM, SF, and SIC generator
-ADCI

Fig. 3.5. The external clock should be capable of generating 2-microsecond, 3-volt positive pulses.

Figure 3.7 shows the AD converter output data buffer (ADCODB) with data channel input buffer (DCHIB). Stages 1-14 are the same. The bottom inverter and the 14 open collector NAND gates form the data channel input buffer.

Figure 3.8 shows the data channel request network (DCHRN). The data channel synchronous flipflop becomes set after each digitization finishes. This process continues until all samples finish.

Figure 3.9 shows the interrupt request network (INTRN). In addressable mode the done flipflop becomes set each time Address Ready becomes true. In sequential mode the done flipflop becomes set only after all samples finish.

3.4 Recorder Interface

Figure 3.10 is a signal flow block diagram of the recorder interface. Figures 3.11-3.19 show the details of the recorder interface.

Figure 3.11 shows the recorder output signal receivers (ROSR) with input buffer C1 (IBC1). Stages 1-6 are the same. The top inverter and the 7 open collector NAND gates form the IBC1.

Figure 3.12 shows the command register. Stages 1 and 2 are the same. Stages 3-5 are the same too. Ready Command ($\overline{RYC}$) and Rewind Command ($\overline{RWC}$) are 2-microsecond negative pulses. Remote

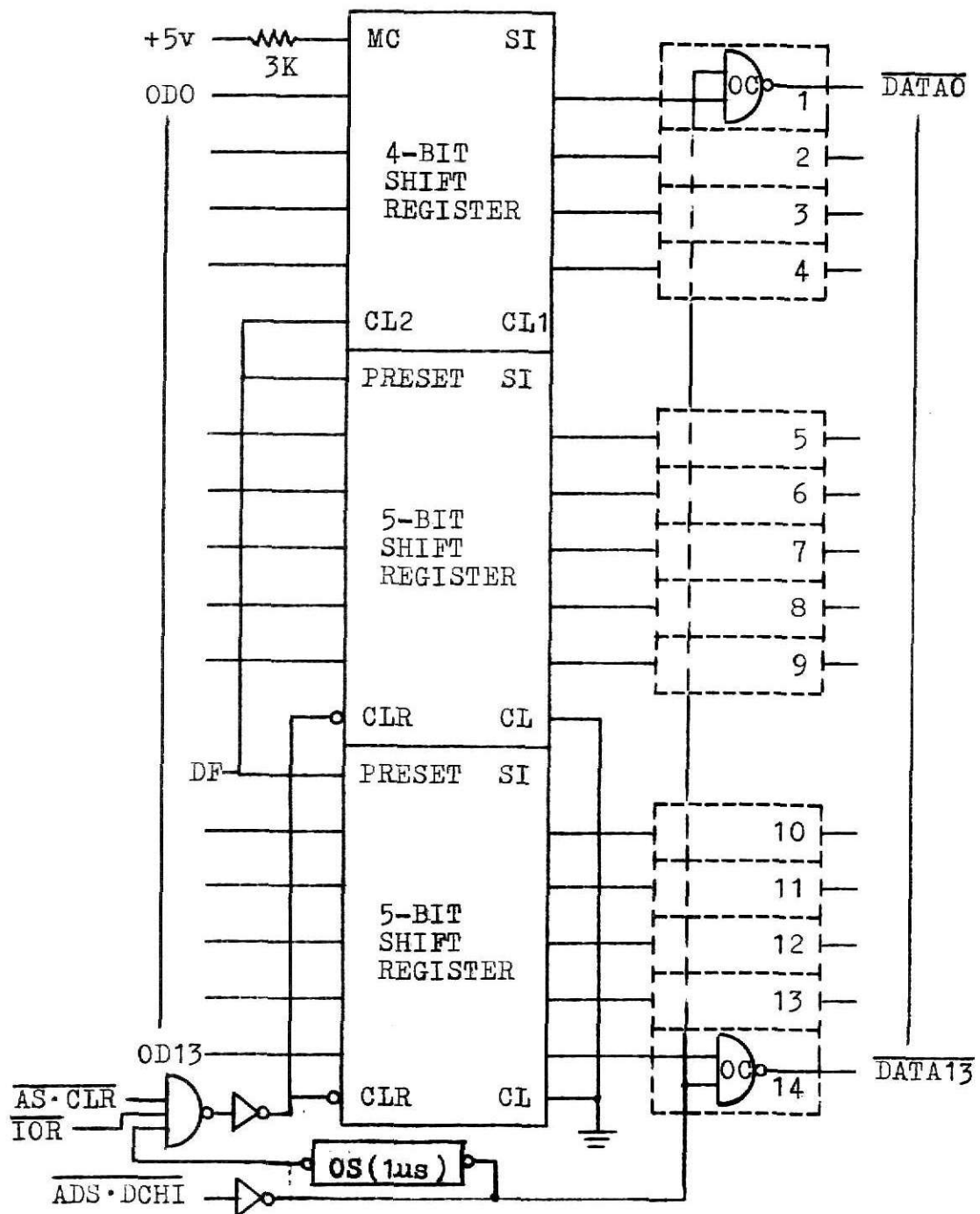


Fig. 3.7. ADC output data buffer with data channel input buffer

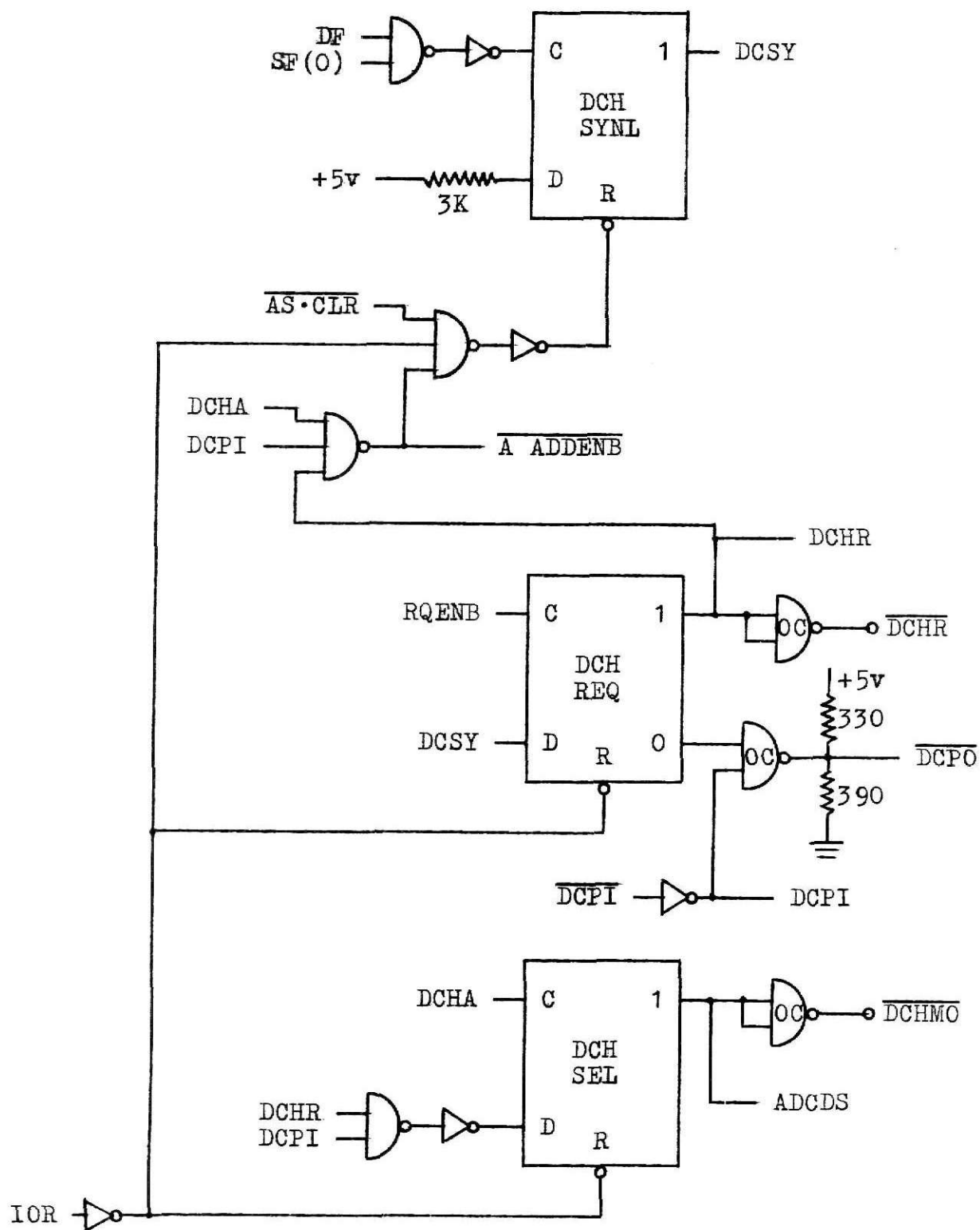


Fig. 3.8. Data channel request network-ADCI

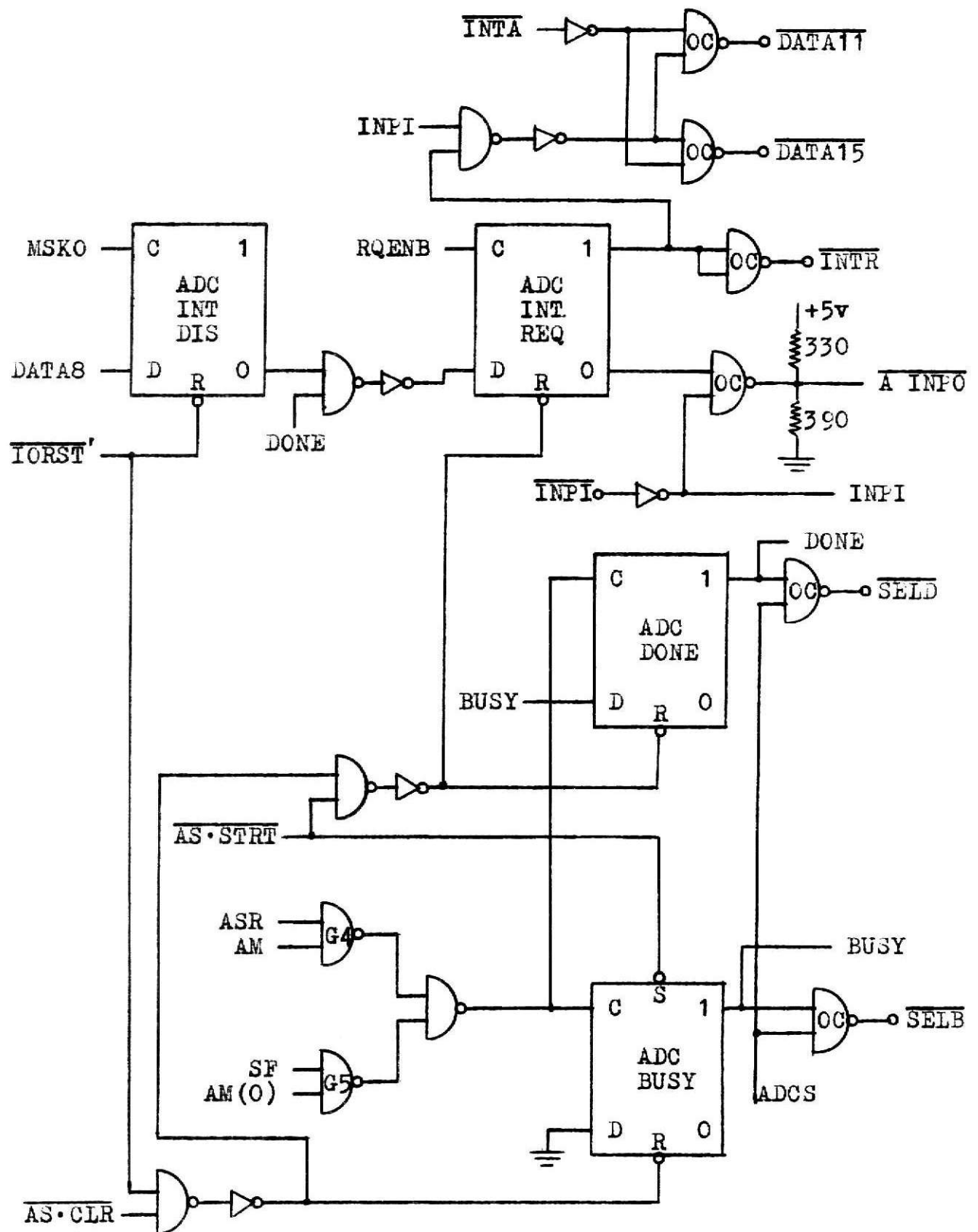


Fig. 3.9. Interrupt request network-ADCI

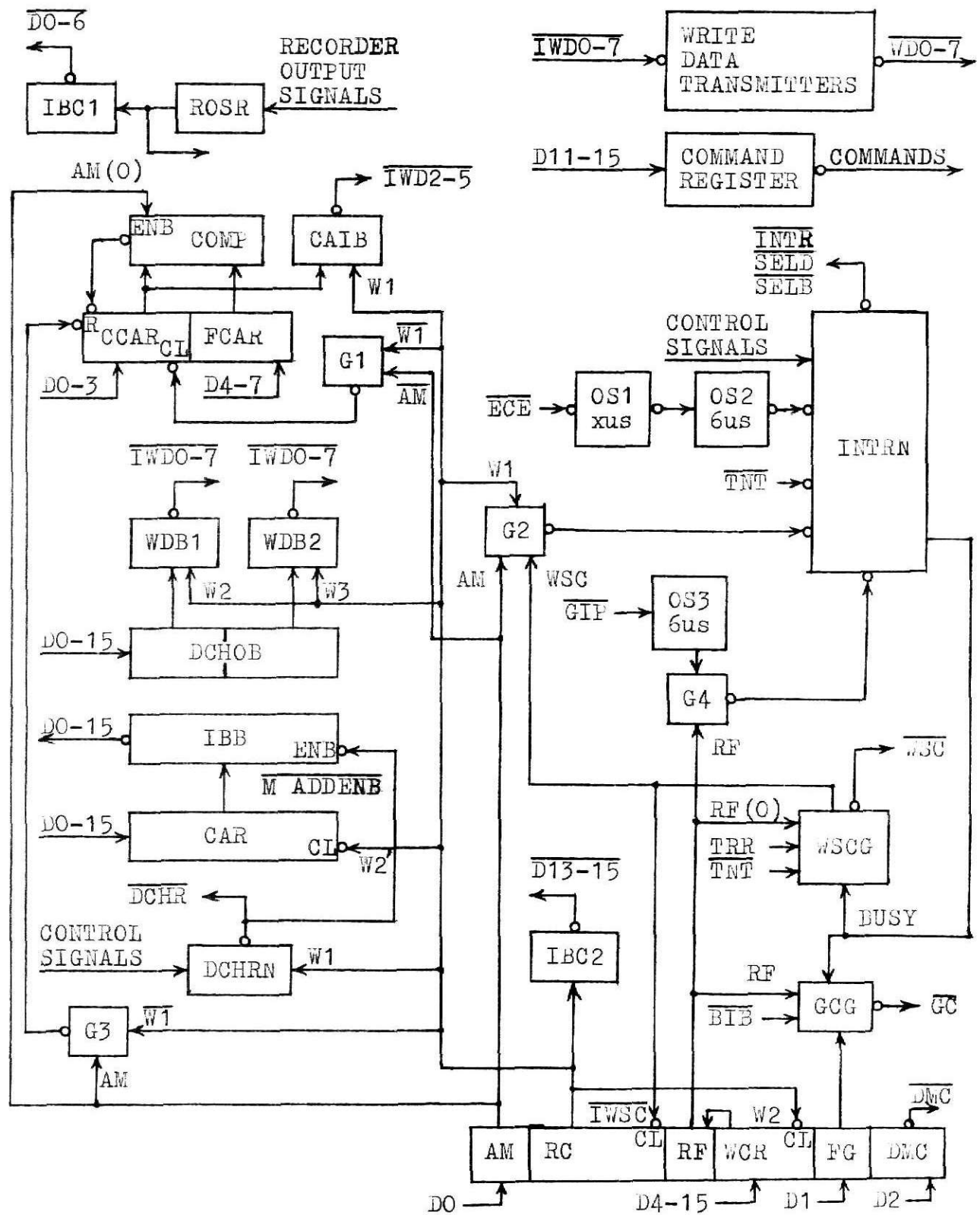
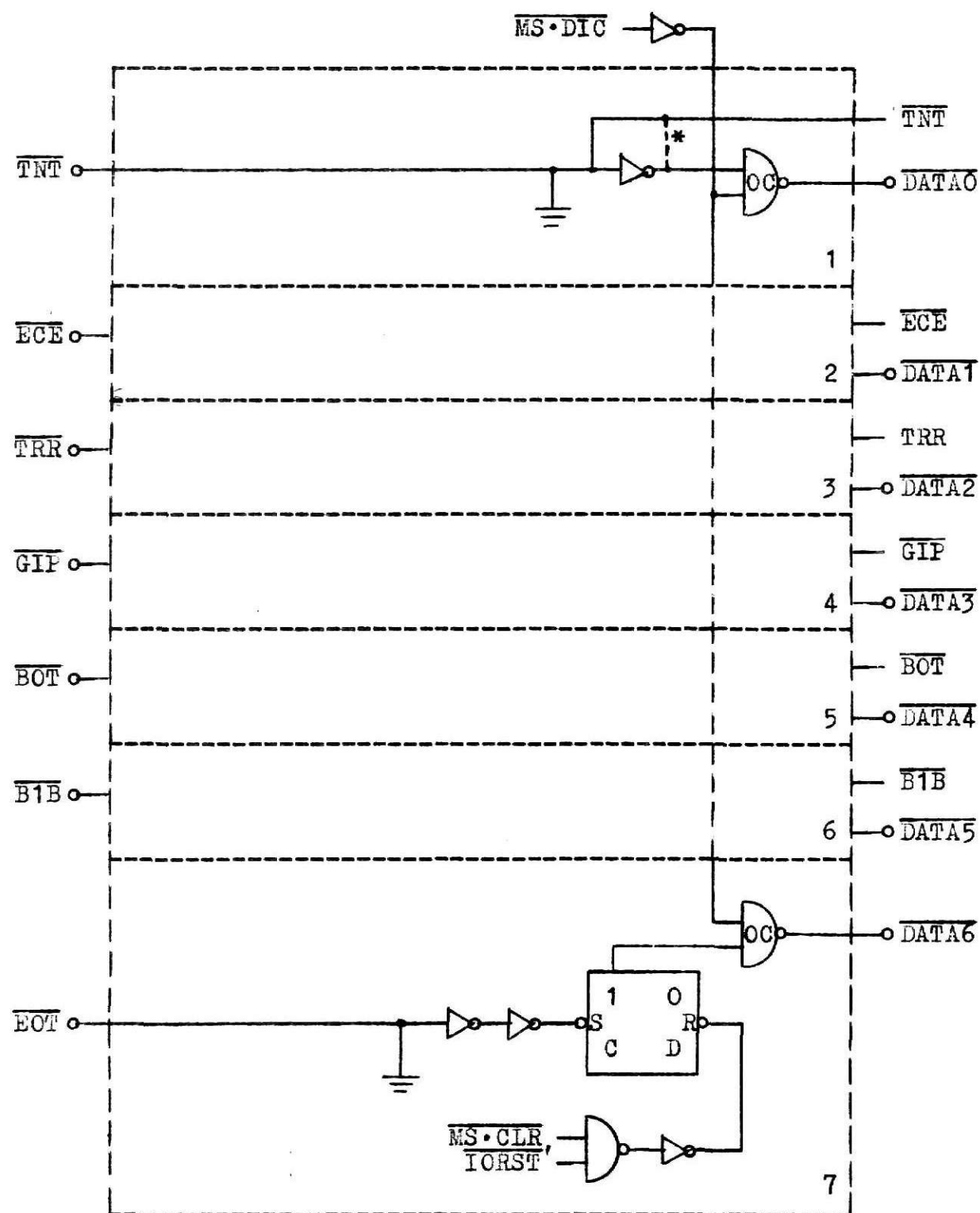


Fig. 3.10. Signal flow block diagram of MTA interface



(*): HIGH TRUE THROUGH PATH ----.

Fig. 3.11. Recorder output signal receivers with input buffer C1

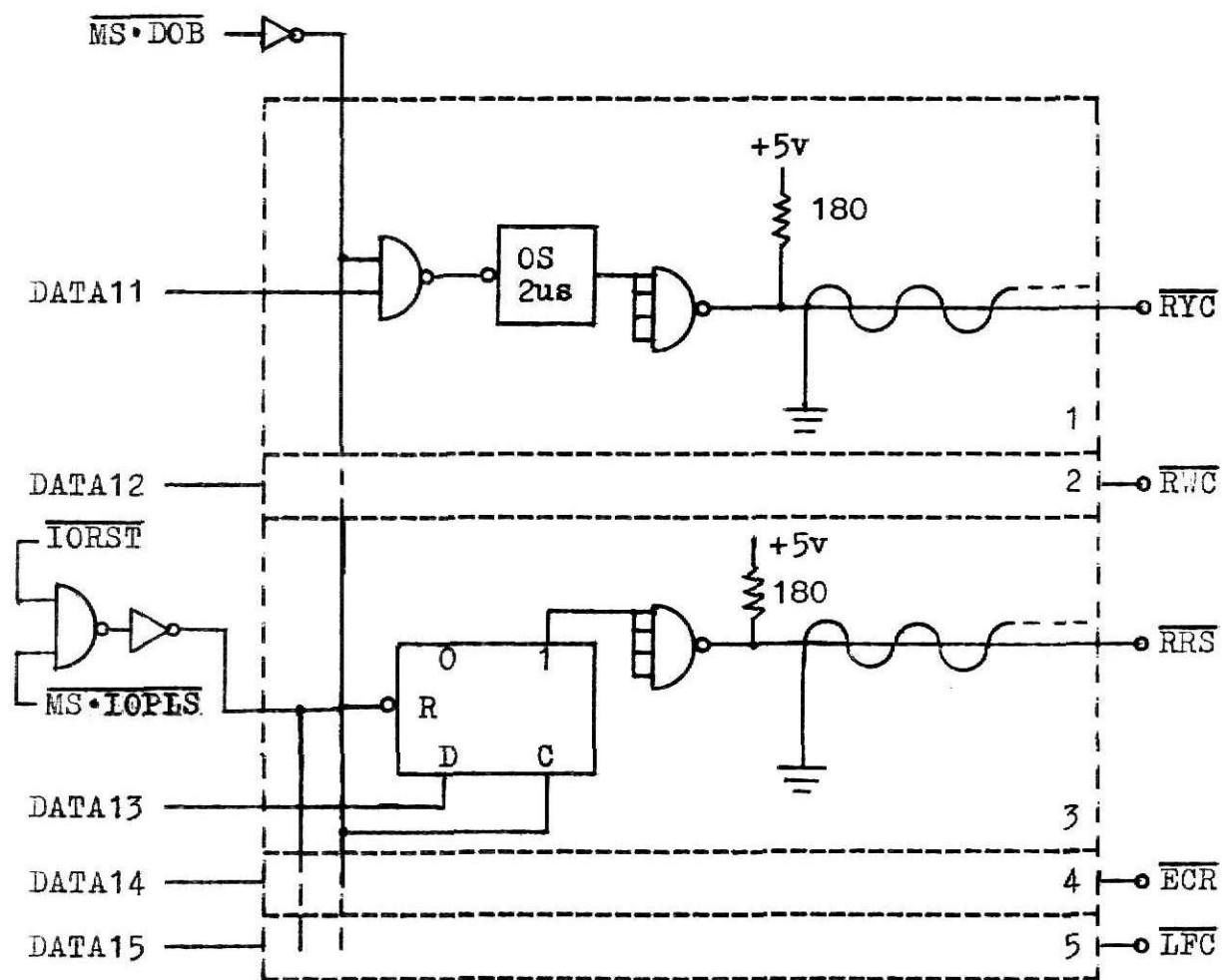


Fig. 3.12. Command register-MTAI

Reset ($\overline{RRS}$), Echo Check Reset ($\overline{ECR}$), and Load Forward Command ($\overline{LFC}$) are negative levels. During operation the three flipflops in stages 3-5 must be reset by the $\overline{MS \cdot IOPLS}$ signal when they need to.

Figure 3.13 shows the write-step command generator and the write data transmitters. One-shot 4 in the write step command generator is used for preventing the recorder to operate over rated speed. Its pulse width is the pulse width (TRR true) of the TRR waveform in the steady rated speed operation minus 5 microseconds. In the write data transmitters, stages 1-8 are the same.

Figure 3.14 shows the current channel address register (CCAR) with final channel address register (FCAR), comparator (COMP), and channel address input buffer (CAIB). Stages 1-4 are the same. Stages 5-8 are the same too. The four open collector NAND gates in stages 1-4 form the channel address input buffer. One-shot 6, gate 2 (a 4-input OR gate), and the four exclusive-OR gates in stages 5-8 form the comparator.

In sequential mode operation, $AM(0)$ is high. The current channel address is advanced one count each time $\overline{WI}$ becomes high. When the address in the CCAR becomes the same as that in the FCAR, the output of gate 2 becomes low. As the current channel address is advanced one count again, the output of gate 2 becomes high, triggering OS6 to generate a positive pulse which resets the CCAR to channel 0 through gate1, gate 3 and inverter 4.

In addressable mode operation, AM is high and $AM(0)$ is low.

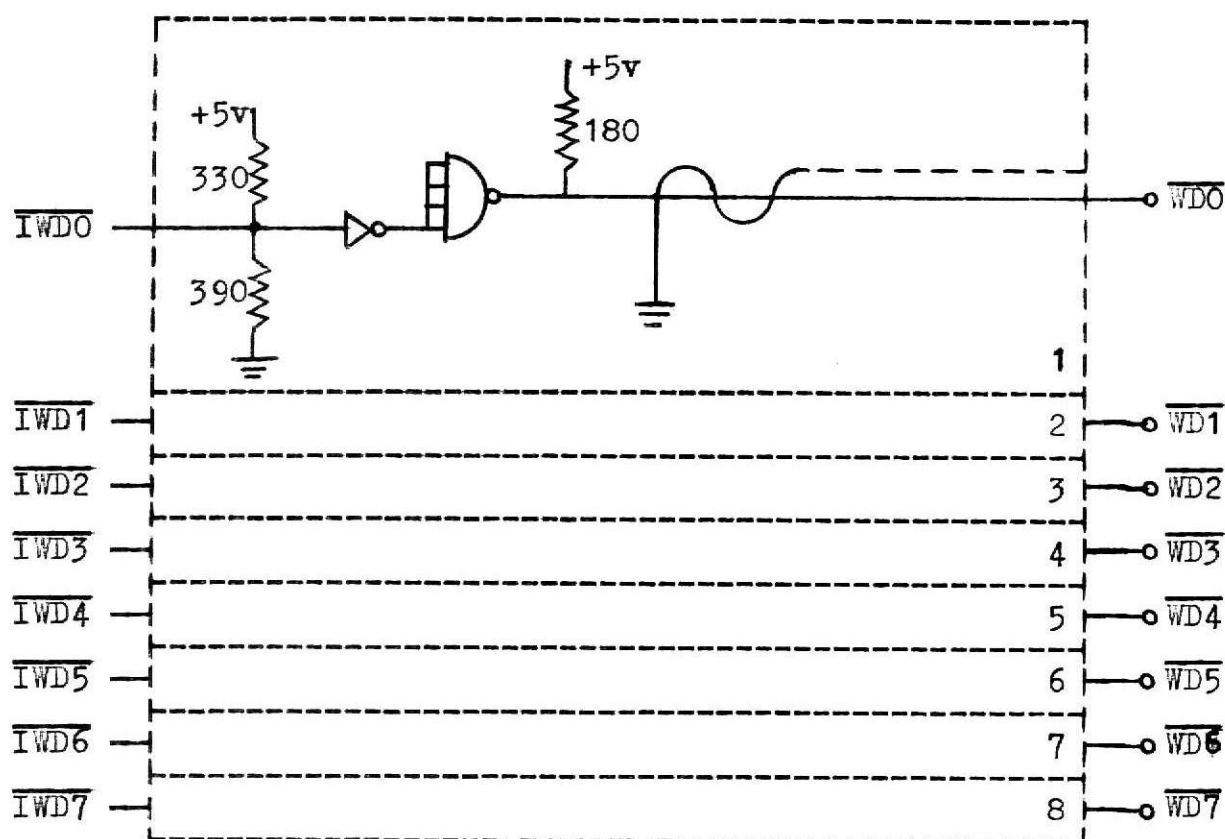
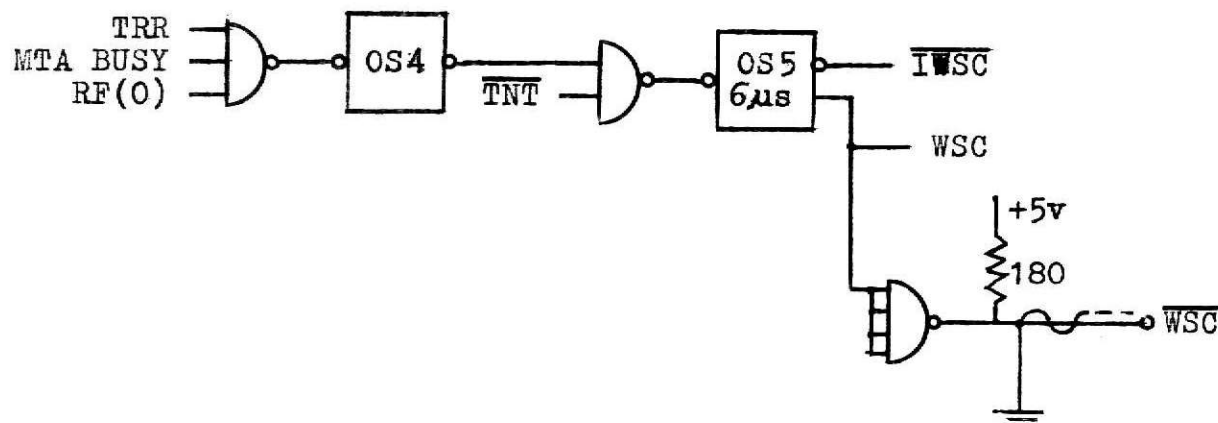


Fig. 3.13. Write step command generator and write data transmitters-MTAI

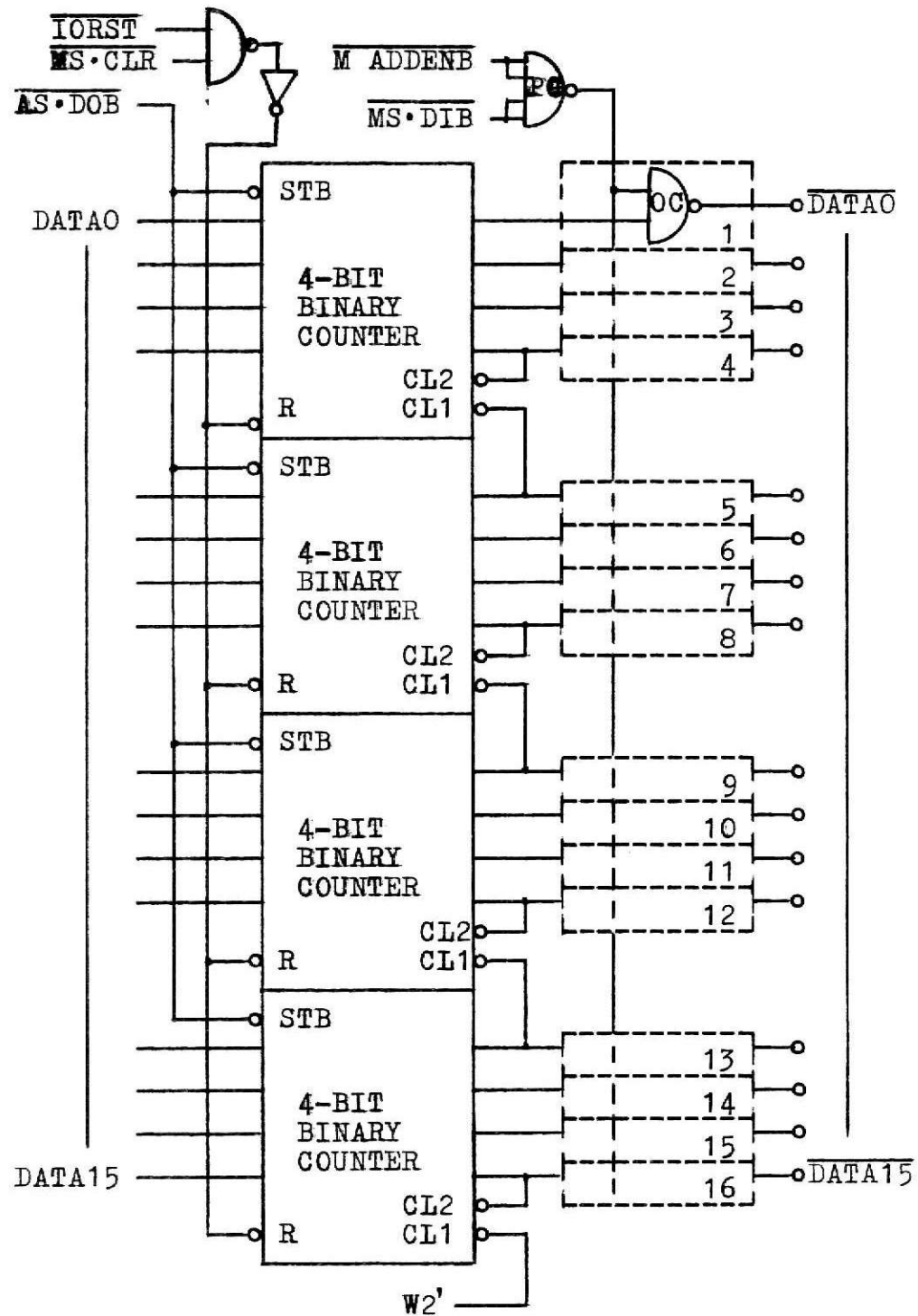


Fig. 3.15. Current address register with input buffer B-MTAI

Gate 1 and G1 are disabled. The CCAR is clear each time $\overline{W1}$ becomes high.

Figure 3.15 shows the current address register (CAR) with input buffer B (IBB). It is the same as that in the ADC interface. The beginning address is loaded into the ADC CAR and the recorder CAR at the same time by the $\overline{AS \cdot DOB}$ signal.

Figure 3.16 shows the word count register (WCR) with ring counter (RC), input buffer C2 (IBC2), gap command generator (GCG), and the control flipflops AM (Addressable Mode), FG (File Gap), DMC (Disable Manual Control), and RF (Record Finish). W1, W2, and W3 form the ring counter. Gates 8-10 and inverter 11 form IBC2. Gates 5-7 and one-shot 7 (OS7) form the GCG.

The WCR must be reset before it is loaded. When the WCR and the control flipflops are loaded, W3 is automatically set, while W1 and W2 are still reset. The RC changes state each time $\overline{IWSC}$ goes low, ie when the WSCG generates a Write Step command.

Figure 3.17 shows the data channel output buffer (DCHOB) with write data buffer 1 (WDB1) and write data buffer 2 (WDB2). Stages 1-16 are the same except stages 1-8 connect to W2 and stages 9-16 connect to W3. Stages 1-8 and stages 9-16 form WDB1 and WDB2 respectively.

Figure 3.18 shows the data channel request network (DCHRN). It is the same as that in the ADC interface. The DCH SYNL flip-flop is set each time W1 becomes high.

Figure 3.19 shows the interrupt request network (INTRN) with one-shots 1-3 (OS1-3), G2, and G4. When the output of gate

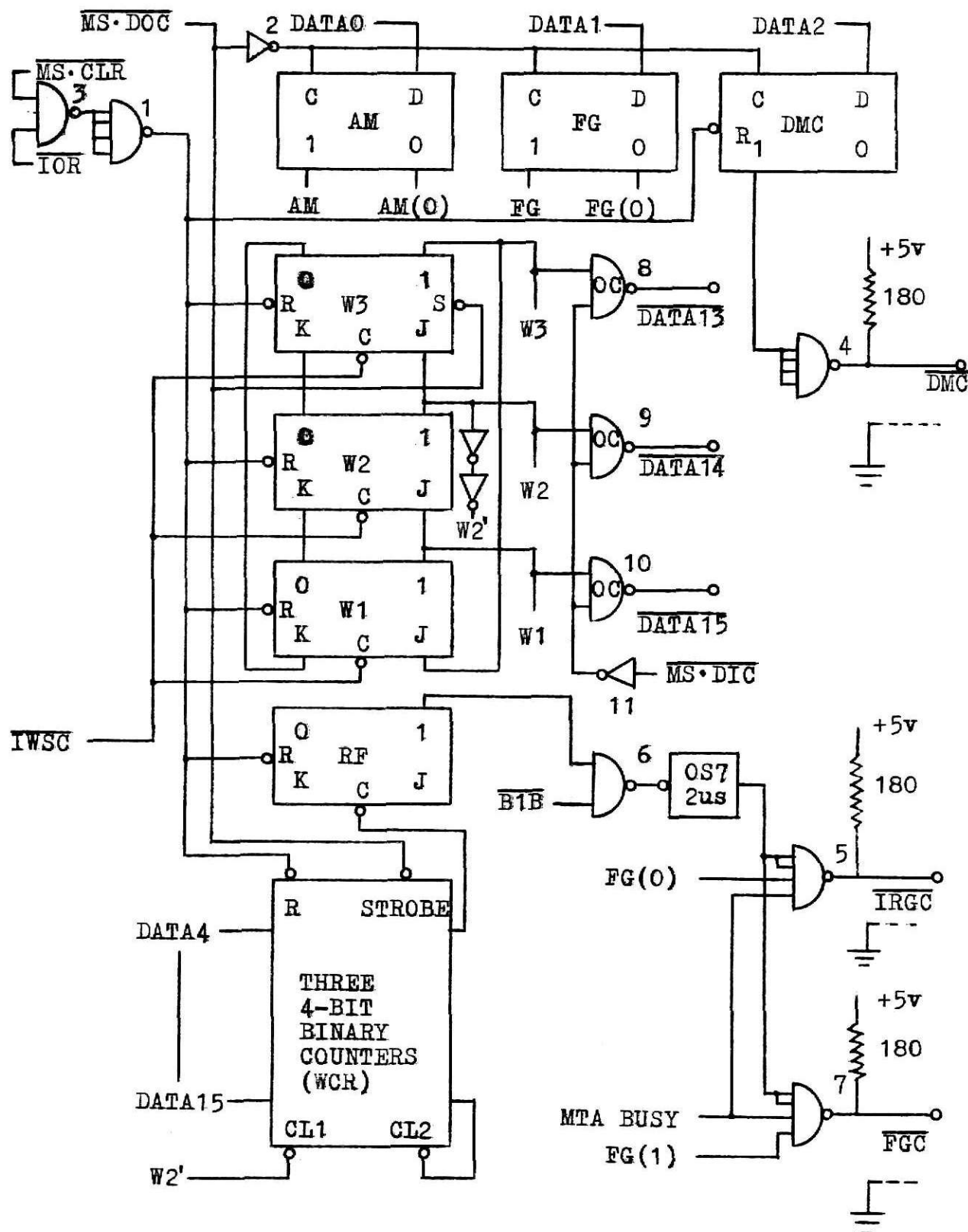


Fig. 3.16. Word count register with AM, FG, DMC, ring counter, input buffer C2, and GC generator-MTAI

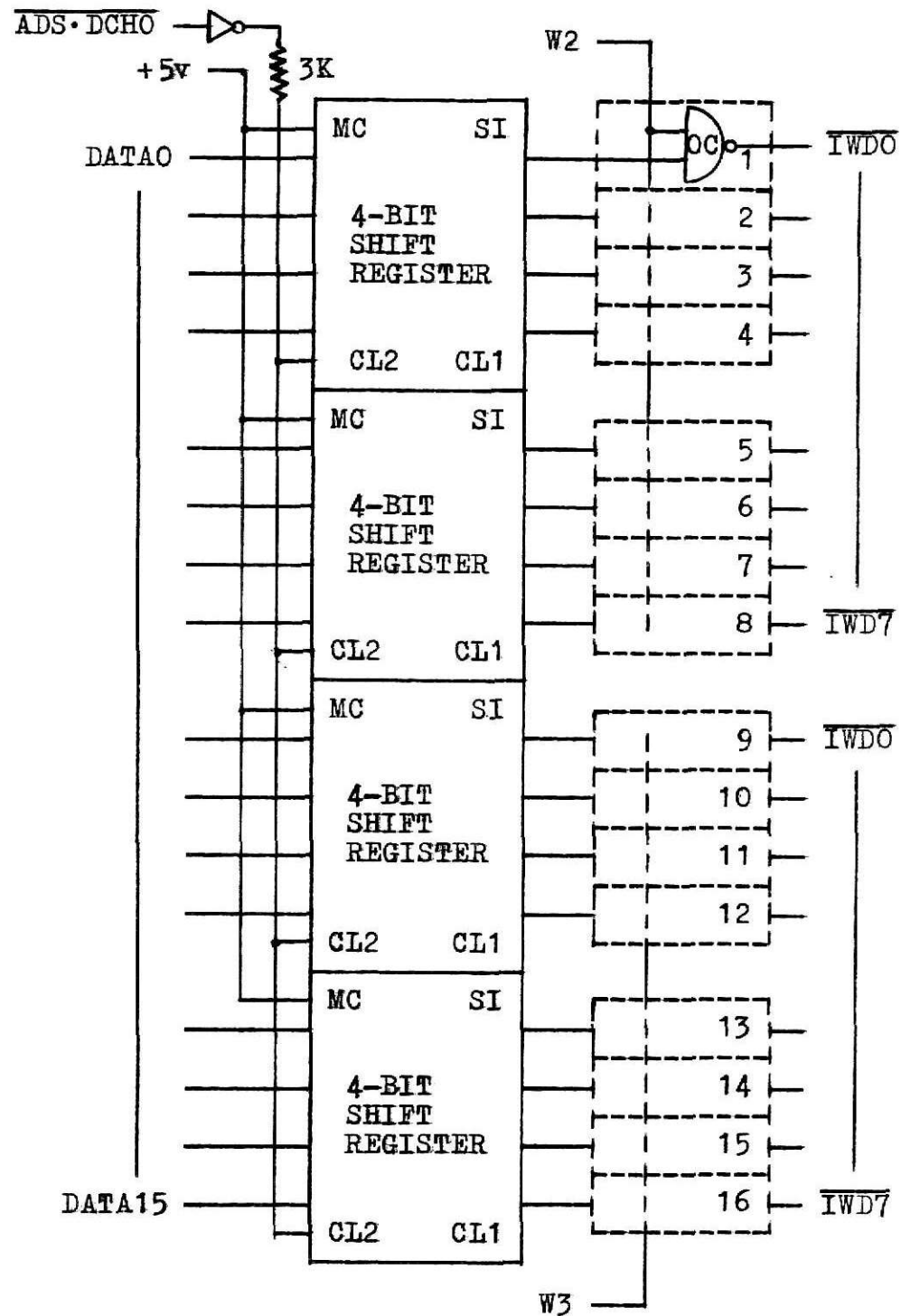


Fig. 3.17. Data channel output buffer with write data buffer 1 and write data buffer 2-MTAI

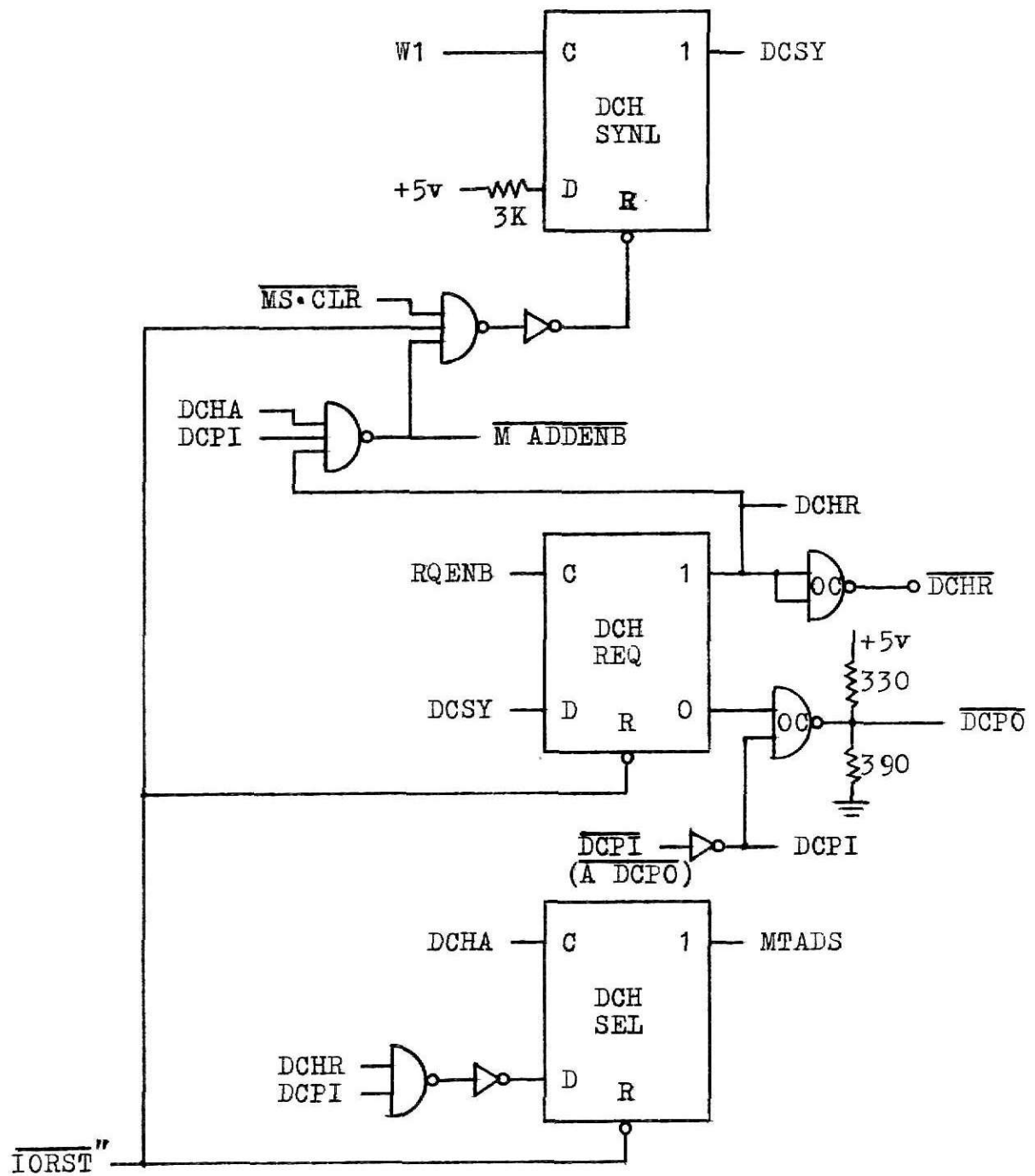


Fig. 3.18. Data channel request network-MTAI

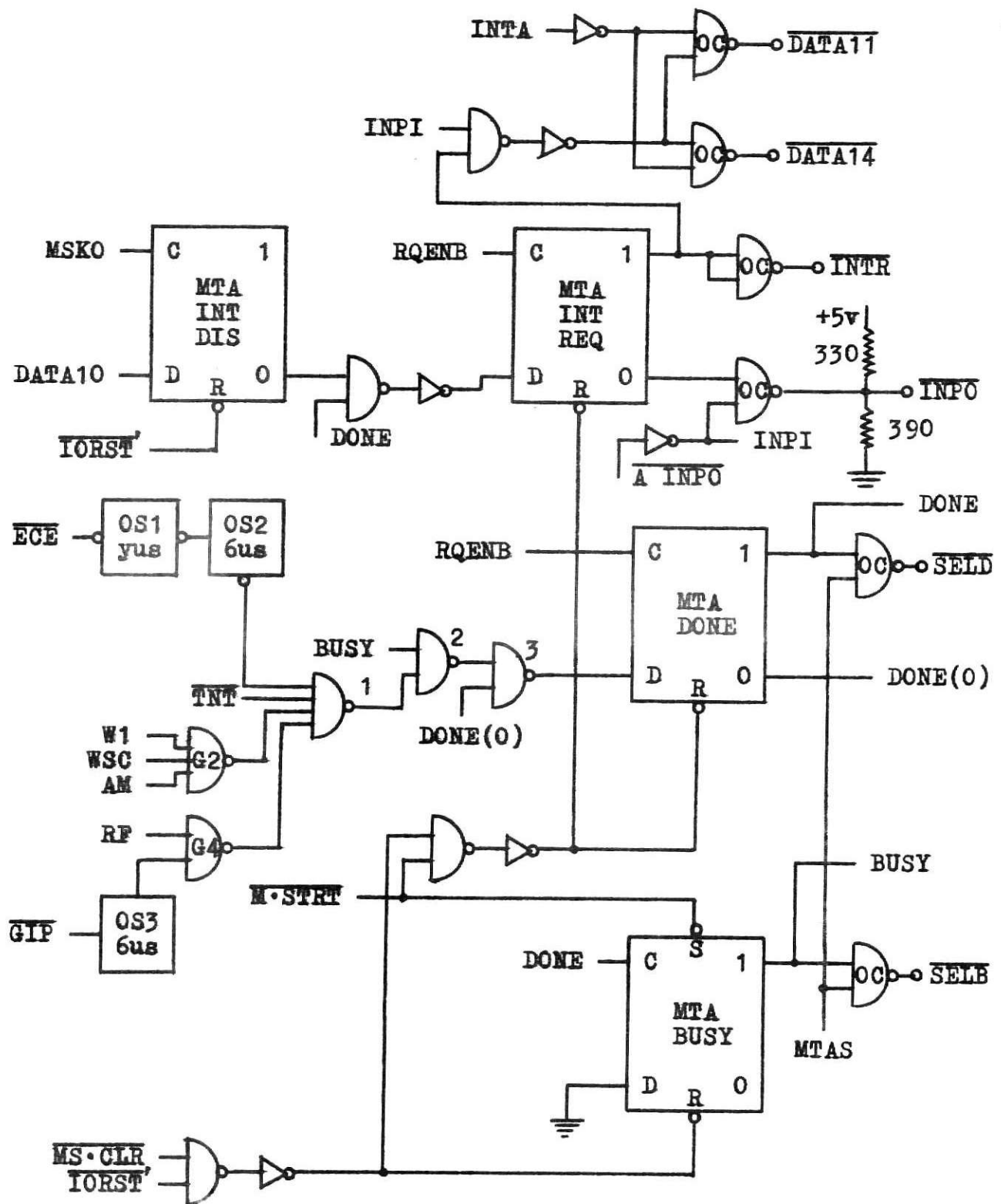


Fig. 3.19. Interrupt request network with one-shots 1-3, G2 and G4-MTAI

1 is high, the output of gate 3 is high if BUSY is set. Therefore the next RQENB signal sets DONE, clearing BUSY, resulting in disabling the WSCG. After DONE is set, another RQENB signal sets INT REQ if INT DIS is clear. As soon as INT DIS is set or DONE is reset, the next RQENB signal clears INT REQ. If the output of gate 3 still continues to be high when DONE is reset, the INTRN will make another interrupt request by the same process as mentioned above. RQENB is generated by the processor of the computer at the beginning of every memory cycle. The maximum interval between the leading edges of two consecutive RQENB signals is 4.5 microseconds. Therefore, in order that DONE can be set in any situation, the output of gate 3 must go high for at least 4.5 microseconds.

The pulse width of OS1 is 4 microseconds less than that of OS4 in the WSC generator. OS1 and OS2 are used for delaying the Echo Check Error signal such that $\overline{ECE}$ (low true) causes the output of gate 3 to go high for 6 microseconds just as the ring counter changes state.

3.5 Assignments for Input-Output Buffers

AD Converter Interface

ACSR (0-3)	Output Buffer A
CAR (0-15)	Output Buffer B
AM (0) and WCR (4-15)	Output Buffer C

Recorder Interface

CCAR (0-3) and FCAR (4-7)	Output Buffer A
Command Register	Output Buffer B

Command:	RYC	RWC	RRS	ECR	LFC
Bit :	11	12	13	14	15

AM (0),FG (1),DMC (2),and WCR (4-15) Output Buffer C

IBC1 (0-6) and IBC2 (13-15) Input Buffer C

IBC1:	TNT	ECE	TRR	GIP	BOT	B1B	EOT
Bit :	0	1	2	3	4	5	6

IBC2:	W1	W2	W3
Bit :	15	14	13

CHAPTER IV

OPERATION

4.1 Types of Operations

Three types of operations involve in this data transfer system: Sequential Mode with AD Converter Using External Clock, Sequential Mode with AD Converter Using Internal Clock, and Addressable Mode. In addressable mode operation, the AD converter must use the external clock.

4.2 Operation Instructions

1. Set up the whole system and turn on the power supplies.
2. Turn the computer power switch to ON and send an IORST signal to reset all relevant logics in the interface.
3. Turn the AD converter front switches to the proper positions according to the type of operation, and then turn the AD converter power switch to ON. For sequential mode operation, after turn on the power, push the RESET pushbutton to reset the channel register in the Multiplexer to channel 0, and then set up the final channel address in the CHANNEL SELECT switches.
4. Load the program into the computer. The program must include an interface loading program to load the following data into the interface.

A. Selected mode (1 for AM, 0 for SM) and number of

words in 2's complement into ADC Output Buffer C.

B. First channel address into ADC Output Buffer A (for AM operation only).

C. Initial address into ADC Output Buffer B. And set ADC BUSY (the MTA CAR is automatically loaded at the same time).

NOTE

In external clock operation, after ADC BUSY is set, the AD converter is started by the external clock; in internal clock operation, ADC BUSY is set for interrupt request only, the AD converter must be started manually by pushing the SAMPLE pushbutton.

D. Selected mode (1 for AM, 0 for SM), gap type (1 for FG, 0 for IRG), control type (1 for DMC), and number of words in 2's complement into MTA Output Buffer C.

E. First channel address (AM operation) or final channel address (SM operation) into MTA Output Buffer A.

F. Set MTA BUSY according to the following specifications:

i. In internal clock operation, set MTA BUSY after the first Digitization Finish.

ii. In external clock operation:

a. For sampling rates greater than

$1/(X - 39 \times 10^{-6})$ sps (samples per second), set MTA BUSY in step E. X is the pulse width of OS4 in the WSC generator. Usually X is less than 0.2 msec.

b. For sampling rates not greater than $1/(X - 39 \times 10^{-6})$ sps but not less than 350 sps, set MTA BUSY after the first DF (SM operation) or the first ADC DONE (AM operation).

c. For sampling rates less than 350 sps, set MTA BUSY after the Nth DF (SM operation) or the Nth ADC DONE (AM operation).

$$N = 2 - 2R/700 \quad \text{or} \quad w(1 - 3R/700) + 4R/700$$

depending on which is larger. Take the greater integer for numbers with fractions. Where

R: sampling rate in samples per second

w: number of words per record

5. Bring the recorder to the operational status. This may be done manually or by the program.
6. Send the analog signals.
7. Start the program.
8. Push SAMPLE pushbutton (internal clock operation only).

4.3 Operation Theory

4.3.1 Sequential Mode with AD Converter Using External Clock

4.3.1.1 AD Converter Interface

Refer to Fig. 3.2 Signal flow block diagram ADCI and Figs. 2.1 and 3.3-3.9. In sequential mode operation, AM(0) and AM are high and low respectively, SF(0) and SF are high and low respectively until the WCR overflows. Therefore, G3 and G4 are

always enabled and disabled respectively, G1 and G6 are enabled until the WCR overflows, and G5 is disabled until the WCR overflows.

After ADC BUSY is set, the first 2-usec, 3v positive external clock pulse causes G6 to become low for 2 usec, thus the SIC transmitter sends a 2-usec, 6v negative pulse to the $\overline{\text{SIC}}$ input. This sample initiate command causes ASR to become low for 11 usec. Five microseconds after $\overline{\text{SIC}}$ becomes low, DF becomes low (false) for 34 usec. As ASR becomes high, OS1 is fired to generate a address set command which advances the channel register inside the AD converter one count to the next channel address. As DF becomes high, it strobes the AD converter output data into the ADCODB, and sets ADC DCH SYNL via G1. Thus the next RQENB signal sets ADC DCH REQ. If the $\overline{\text{DCPI}}$ signal entering this interface is low, the high true DCHA signal, which is generated by the computer in every data channel transfer cycle, sets ADC DCH SEL, resets ADC DCH SYNL, and causes $\overline{\text{A ADDENB}}$ to go low which enables IBB. As DCHA terminates, the outputs of IBB is strobed into the memory address register and DCHI is turned on. $\overline{\text{ADS} \cdot \text{DCHI}}$ becomes low, advancing the CAR and the WCR one count each, and enabling the DCHIB. At the end of DCHI the computer strobes the outputs of the DCHIB into its memory buffer and generates RQENB again, which resets ADC DCH REQ. The AD converter starts the next cycle when the next external clock pulse arrives. This process continues until the WCR overflows. Then SF(0) goes low disabling G6, SF goes high setting ADC DONE and resetting ADC BUSY. If ADC INT DIS is

clear, the next RQENB signal sets ADC INT REQ. By the program the computer reads the contents of the CAR into its processor through IBB, and checks this number to make sure that the whole sampling process has been finished.

4.3.1.2 Recorder Interface

Refer to the Signal flow block diagram MTAI (Fig. 3.10), and Figs. 2.2 and 3.11-3.19. AM(0) and AM are the same as that in the ADC interface. RF(0) and RF are equivalent to SF(0) and SF respectively. In sequential mode operation, after MTA Output Buffer C is loaded, G1 and the comparator are always enabled, G2 and G3 are always disabled, the WSC generator is enabled until the WCR overflows, and G4 and the GC generator are disabled until the WCR overflows. In the ring counter (RC), W1 and W2 are low, W3 is high.

Since the recorder has been already brought to the operational status, TRR is high. Thus when MTA BUSY is set, OS4 in the WSC generator (see Fig. 3.13) is triggered to generate a x-usec negative pulse whose back edge firing OS5 if $\overline{\text{TNT}}$ is high (Tape Not Tensioned false). Once OS5 is fired, the 1 output of OS5 goes high for 6 usec, causing the power gate to send a 6-usec negative pulse to the $\overline{\text{WSC}}$ input. As soon as $\overline{\text{WSC}}$ becomes low, $\overline{\text{B1B}}$ goes low (BUFFER 1 BUSY true) until there is no data in buffer 1 and buffer 2 is waiting to be recorded. On the other hand, the 0 output of OS5 goes low for 6 usec, shifting the ring counter. Thus W3 and W1 go low and high respectively, while W2 remains low. As W1 goes high, MTA DCH SYNL is set.

Therefore the next RQENB signal sets MTA DCH REQ. If only the AD converter and the recorder use the computer and the program does not contain indirect addressing, a data word will be transferred from the memory to the data channel output buffer (DCHOB) within 8.2 usec after MTA DCH SYN1 is set. As long as W1 is high, the channel address input buffer (CAIB) is enabled, holding the channel address at the write data inputs via the write data transmitters.

After a 5-usec delay, the first write step command causes the recorder to generate a 2-usec pulse which strobes the channel address into buffer 2 and turns off TRR. Since there is no data in buffer 1 waiting to be recorded at this time, the channel address is transferred to buffer 1 and TRR is turned on 4 usec later.

As TRR is turned on, OS4 in the WSC generator is triggered again. Thus x usec later, the WSCG generates the second write step command and shifts the ring counter. W1 goes low, disabling the CAIB. While W2 goes high, enabling write data buffer 1 (WDB1), thus holds the first character of the output data at the write data inputs via the write data transmitters. As foregoing, 5 usec later the first character of the output data is strobed into buffer 2 and TRR is turned off.

Approximately 2 msec after MTA BUSY is set, the recorder generates the first encoder pulse whose leading edge strobes the contents of buffer 1 into the write-waveform generator. This pulse is also delayed 4 usec, and then strobes the contents of buffer 2 into buffer 1 and turns on TRR. Thus x usec

later, the WSCG generates the third write step command and shifts the ring counter. W2 goes low, disabling WDB1 and advancing the CAR and the WCR one count each. While W3 goes high, enabling write data buffer 2 (WDB2), thus holds the second character of the output data at the write data inputs via the write data transmitters. As foregoing, 5 usec later the second character of the output data is strobed into buffer 2 and TRR is turned off.

Approximately $1/700$ sec after the first encoder pulse, the recorder generates the second encoder pulse to transfer the data in buffer 1 and buffer 2 and to turn on TRR as before.

As the WSCG generates the fourth write step command, the ring counter begins the next cycle. And hereafter the write step commands will be generated at intervals of $1/700$ second unless Tape Not Tensioned happens.

After the final channel address has been read into buffer 2, the next write step command causes the comparator to generate a negative pulse which resets the current channel address register (CCAR) to channel 0 as mentioned on page 28.

The above process continues until the WCR overflows. Once the WCR overflows, RF is set, disabling the WSC generator and enabling the gap command generator (GCG).

When the last character is strobed into the write-waveform generator, $\overline{B1B}$ goes high, firing OS7 in the GC generator (see Fig. 3.16) to generate a 2-usec positive pulse applied to gates 5 and 7. If FG is set, gate 7 generates a file gap command, otherwise gate 5 generates a interrecord gap command. In either

case $\overline{GIP}$ goes low.

As soon as gapping is finished, $\overline{GIP}$ goes high, firing OS3 to generate a 6-usec negative pulse applied to gate 1 in the INTR network. Thus the INTR network makes an interrupt request as mentioned on pages 32 and 37. By checking the current address, the fact that the whole recording process has been finished can be identified. Before this interface is clear, the program should check MTA Input Buffer C Bit 6. A 1 appears at this bit if the tape is beyond the EOT mark.

During operation, if Tape Not Tensioned happens, $\overline{TNT}$ goes low, disabling the WSC generator and making an interrupt request through the INTR network. By the program, the computer will find out this trouble and treat it. The current address and the status of the ring counter at this time should be stored into the selected addresses for reference. After the recorder is brought to the operational status again, setting MTA BUSY will continue the recording process from the next ring counter state. In this case two to three characters are missed.

If parity error happens, ECE is turned on 4 usec after TRR has been turned on. As soon as ECE is turned on, $\overline{ECE}$ goes low, firing OS1 to generate a $(X - 4)$ -usec negative pulse, whose back edge fires OS2 to generate a 6-usec negative pulse applied to gate 1 in the INTR network, thus resulting in clearing MTA BUSY, disabling the input of the WSC generator, and setting MTA INT REQ as mentioned before. On the other hand, almost at the same time as OS2 is fired, OS5 in the WSC generator is fired to shift the ring counter and to generate a write step command as

usual. Since when the ECE signal makes an interrupt request via the INTR network, two other write step commands have been already generated and the data belonging to them are still waiting to be recorded. Therefore if ECE signal is found out by the program when W3 is high, the error is in the channel address; when W1 is high, the error is in the first character; when W2 is high, the error is in the second character. The address in which the error happened is the current address minus one, because the CAR has been already advanced one count when the ECE signal is found out by the program. ECE must be turned off within $1/700$ sec after it is detected by the recorder. If MTA BUSY is set again within 1.424 msec after ECE is turned on, the recorder will continue to run at its rated speed.

4.3.2 Sequential Mode with AD Converter Using Internal CLOCK

Except for starting and clocking the AD converter, the operation of sequential mode with AD converter using internal clock is the same as that of sequential mode with AD converter using external clock.

In internal clock operation, the Address Set and Sample Initiate inputs of the AD converter are disabled by the AD converter internal circuits. ADC BUSY is set for interrupt request only. The AD converter must be started manually by pushing the SAMPLE pushbutton. Once it is started, it will continue to run until the operator stops it. When the word count register overflows, the DCHR network is disabled by the 0 output of the SF

flipflop, thus the ADC interface stops transferring the ADC output data to the computer, although the AD converter still continues to run. The 0 output of the SF flipflop also makes an interrupt request via the INTR network to inform the computer that the required samples are finished.

4.3.3 Addressable Mode

Except those specified in the following, addressable mode operation is the same as sequential mode with external clock operation.

A. AD Converter Interface

- * G3 and G5 are disabled; G4 is enabled.
- * The first selected channel address is set into the AD converter when the ACSR (ADC Output Buffer A) is loaded.
- * The ACSR is cleared by the low true $\overline{\text{CLO}}$ (Clock Out) signal approximately 1.5 usec after each Sample Initiate command is generated.
- * Each time ASR goes high, the INTR network makes an interrupt request.
- * The computer sends a new channel address to the AD converter via the ACSR after it receives an ADC INTR.
- * After the word count register overflows, no new Sample Initiate command can be generated, ASR remains high, therefore no new interrupt request can be generated.

B. Recorder Interface

- * G1 and the comparator are disabled; G3 and one input of G2 are enabled.
- * The first channel address is loaded into the CCAR before MTA BUSY is set.
- * Each time $\overline{W1}$ goes high, clearing the CCAR via G3 instead of advancing it via G1.
- * Each time W1 goes high, requesting a data channel transfer via the DCHR network and an interrupt via G2 and the INTR network. Since WSC is a 6-usec positive pulse, G2 is enabled for 6 usec only, thus only one interrupt request can be generated when W1 is high.
- * The computer sends a new channel address to the CCAR after it receives a MTA INTR and identifies that W1 is high.

4.4 Programming

To operate this data transfer system, either interrupt program or test program may be used, depending on the sampling rate and mode. In low sampling rate or sequential mode operation, other input-output devices may be included in this system to make use of the large amount of the computer's free time. Especially in sequential mode operation, the program actually is doing nothing after MTA BUSY is set, if ECE and TNT do not happen.

The following two programs are suitable for any sampling rate, if only the AD converter and the recorder use the computer. Program 1 is used for addressable mode; Program 2 is used

for sequential mode.

Program 1

```

00000: 000000          ;Save location 0 for saving PC
00001: JMP    STMP      ;Put beginning address of STMP in loca-
                        ;tion 1; this instruction will be
                        ;changed to 'JMP ADCSV' by the program
                        ;after MTA BUSY is set

IFLP:  LDA    3,NCHL    ;Enter here, store number of channels
                        ;in use in AC3
        LDA    2,CHALL  ;Store CHAL-1 (1 before address stored
                        ;second channel address) in AC2
        LDA    1,CINTP  ;Store 'JMP ADCSV' in AC1
        LDA    0,CMASK  ;Get disable MTA INT mask
        DOBS   0,CPU    ;MSKO and turn on interrupt
        LDA    0,ADOCL  ;Get data for ADC Output Buffer C
        DOC    0,ADC    ;and send it out
        LDA    0,IAL    ;Get initial address
        DOB    0,ADC    ;and send it to current address regis-
                        ;ters
        LDA    0,MDOCL  ;Get data for MTA Output Buffer C
        DOC    0,MTA    ;and send it out
        LDA    0,CHAL+m ;Get first channel address
        DOAS   0,ADC    ;send it to ADC interface and set ADC
                        ;BUSY
        DOA    0,MTA    ;also send it to MTA CCAR
TEST:  SKPDN  MTA      ;Wait till ADC INTR or MTA DONE
        JMP    .-1
        DIC    1,MTA    ;Read recorder output signals into AC1
        MOVL   1,0,SZC  ;Check TNT

```

```

      JMP      TNTP          ;Yes, treat it
      MOVL     0,0,SZC      ;No, check ECE
      JMP      ECEP        ;Yes, treat it
      MOVR     1,0,SZC      ;No, check W1
      JMP      ADDP        ;Yes, treat it
      DIB      2,MTA        ;No, must be operation finished; read
                           ;MTA final address into AC2 for checking
      DIB      3,ADC        ;Read ADC final address into AC3 for
                           ;checking
      HALT                     ;Stop processor; operator checks ACs
                           ;1-3; a 1 appears at AC1 Bit 6 if the
                           ;tape is beyond the EOT mark

TNTP:  DSZ      NTNTL        ;Reach number of TNTs allowed?
      JMP      .+7          ;No, go to get LOAD FORWARD command
      DIB      0,ADC        ;Yes, read ADC current address into ACO
      LDA      1,FAL        ;Get final address
      SUB      0,1,SNR      ;AD converter operation finished?
      HALT                     ;Yes, stop the processor
      NIOC     MTA          ;No, clear MTA
      JMP      TEST        ;Let AD converter operate along
      LDA      0,LFCL       ;Get LOAD FORWARD command
      DOA      0,MTA        ;and send it to the recorder
      DIB      0,MTA        ;Get MTA current address
      STA      0,@TNTD      ;and store it
      STA      1,@TNTD      ;Store ring counter status
      LDA      1,RYCL       ;Store READY command in AC1
      DIC      0,MTA        ;Read MTA output signals into ACO
      MOVL     0,0,SZC      ;Still TNT?
      JMP      .-2          ;Yes, wait till not TNT

```

```

      NIOP  MTA          ;No, turn off LFC
      DOBS  1,MTA        ;Send READY command to the recorder and
                        ;set MTA BUSY
      JMP   TEST         ;Go to wait ADC INTR or MTA DONE

ECEP:  DSZ    NECEL      ;Reach number of ECEs allowed?
      JMP    .+2         ;No, go to get ECHO CHECK RESET command
      JMP    TNTP+2      ;Yes go to check AD converter operation
                        ;finished or not
      LDA    0,ECRL      ;Get ECR command
      DOBS  0,MTA        ;send it to the recorder and set MTA
                        ;BUSY
      DIB    0,MTA        ;Get MTA current address
      STA    0,@ECED     ;and store it
      STA    1,@ECED     ;Store ring counter status
      MOVR   1,0,SZC     ;W1 high?
      JMP    ADDP        ;Yes, treat it
      JMP    TEST        ;No, go to wait ADC INTR or MTA DONE

ADDP:  LDA    0,@CHALL+2 ;Get next channel address
      DOAS  0,MTA        ;send it to MTA CCAR and set MTA BUSY
      DSZ    NCHL+2      ;Channel cycle finished?
      JMP    TEST        ;No, go to wait ADC INTR or MTA DONE
      STA    3,NCHL+2     ;Yes, restore number of channels in use
                        ;in NCHL+2
      STA    2,CHALL+2    ;Restore 'CHAL-1' in CHALL+2
      JMP    TEST        ;Go to wait ADC INTR or MTA DONE

STMP:  DSZ    NDR        ;Reach number of ADC DONEs required for
                        ;setting MTA BUSY
      JMP    ADCSV        ;No, go to ADCSV routine
      STA    1,1         ;Yes, change location 1 to be 'JMP ADCSV'

```

```

      NIOS  MTA           ;Set MTA BUSY

ADCSV: LDA    0,@CHALL+1 ;Get next channel address
      DOAS  0,ADC        ;send it to ADC and set ADC BUSY
      INTEN                ;Turn on interrupt
      DSZ   NCHL+1       ;Channel cycle finished?
      JMP   TEST         ;No, go to wait ADC INTR or MTA DONE
      STA   3,NCHL+1     ;Yes, restore number of channels in use
                        ;in NCHL+1
      STA   2,CHALL+1    ;Restore 'CHAL-1' in CHALL+1
      JMP   @0           ;Return to interrupted program

LFCL:  LOAD FORWARD command (000001)
RYCL:  READY command (000020)
ECRL:  ECHO CHECK RESET (000002)
IAL:   Initial address
ECED*: 1 before beginning address for storing ECE data
TNTD*: 1 before beginning address for storing TNT data
CMASK: Disable MTA INT (000040)
CINTP: JMP   ADCSV
CHALL: CHAL-1
      *   CHAL-1
      *   CHAL-1
CHAL:  Second channel address
      ...
      ...
      ...
      Final channel address

```

First channel address

FAL: Final address

NDR: 1 for $R \geq 350$ sps; N for $R < 350$ sps (R and N are defined on page 41)

NTNTL: Number of TNTs allowed

NECEL: Number of ECEs allowed

NCHL: Number of channels in use

Same as above

Same as above

ADOCL: AM and number of words per record in 2's complement

MDOCL: AM, gap and control types, and number of words per record in 2's complement

*: Autoincreasing address

Program 2

```
IFLP: INTDS           ;Enter here, turn off interrupt
      LDA 0,ADOCL      ;Get data for ADC Output Buffer C
      DOC 0,ADC         ;and send it out
      LDA 0,IAL        ;Get initial address
      DOBS 0,ADC        ;send it to CARs and set ADC BUSY
      LDA 0,MDOCL      ;Get data for MTA Output Buffer C
      DOC 0,MTA        ;and send it out
      LDA 0,FCHAL      ;Get final channel address
      DOA 0,MTA        ;and send it to MTA FCAR
      LDA 1,ASTML      ;Get address from which MTA BUSY can be
                        ;set
      DIB 0,ADC        ;Read ADC current address into ACO
      SUBO 1,0,SZC     ;Reach address for starting MTA?
```

```

        JMP      .-2          ;No, go back to check again
        NIOS     MTA          ;Yes, set MTA BUSY
TEST:    SKPDZ   MTA          ;MTA DONE?
        JMP      MTASV       ;Yes, serve it
        SKPDZ   ADC          ;No, try ADC
        JMP      .-3          ;Neither, go back to TEST
        DIB     3,ADC         ;Yes, read ADC current address into AC3
        LDA     0,FAL         ;Get final address from memory
        SUB     3,0,SZR       ;ADC CAR reaches final address?
        HALT                    ;No, something wrong, stop the process-
                                ;or; operator checks ACs 1-3
        LDA     0,EML         ;Yes, get 'EM'
        DOAS    0,TTO         ;Type out 'EM' to inform the operator
                                ;to stop the AD converter
        JMP     TEST          ;Go back to TEST

MTASV:   DIC     1,MTA        ;Read MTA output signals into AC1
        MOVL    1,0,SZC       ;TNT?
        JMP     Tntp          ;Yes, go to treat it
        MOVL    0,0,SZC       ;No, check ECE
        JMP     ECEP          ;Yes, go to treat it
        DIB     2,MTA         ;No, must be operation finished, read
                                ;MTA final address into AC2
        HALT                    ;Stop the processor; operator checks ACs
                                ;1-3; a 1 appears at AC1 Bit 6 if the
                                ;tape is beyond the EOT mark

ADOCL:   SM and number of words per record in 2's complement
MDOCL:   SM, gap and control types, and number of words per re-
        cord in 2's complement
FCHAL:   Final channel address
ASTML:   Initial address if  $R > 1/(X - 39 \times 10^{-6})$  sps

```


Initial address plus 1 if

$$350 \text{ sps} \leq R \leq 1/(X - 39 \times 10^{-6}) \text{ sps}$$

Initial address plus octal number of N if $R < 350 \text{ sps}$

EML: EM (000231)

ECEP: Same as ECEP routine in the AM program except that omit
ECEP+8 and ECEP+9

All the other routines and data used in the SM program are the
same as that in the AM program.

Note: For internal clock operation, after start the program,
push the SAMPLE pushbutton to start the AD converter.

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INTERFACE DESIGN FOR HIGH SPEED DATA TRANSMISSION AMONG
A TI AD CONVERTER, A NOVA 1200 COMPUTER, AND A PEC RECORDER

by

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ABSTRACT

The purpose of this paper is to study the interface design for high speed data transmission among a TI AD converter, a NOVA 1200 computer, and a PEC recorder.

The interface is divided into three parts: the Receivers with Device Selection Gates, the AD Converter Interface, and the Recorder Interface. The receivers are mainly used for matching the computer output characteristics. The device selection gates are used for decoding the device selection lines to generate a select level that ensures that only the single addressed device responds to the program. The AD converter interface and the recorder interface, each includes a Data Channel Request network, an Interrupt Request network, a Current Address register, a Word Count register, and other devices, enable the AD converter and the recorder to control themselves by using their own output signals.

In sequential mode with external clock operation, the computer only needs to load the necessary data into the interface, to set ADC BUSY and MTA BUSY, and to treat ECE (Echo Check Error) and TNT (Tape Not Tensioned) if they happen.

Sequential mode with internal clock operation is the same as sequential mode with external clock operation except that the AD converter must be started manually.

In addressable mode operation, except those mentioned in the sequential mode with external clock operation, the computer only needs to offer a new channel address to the AD converter

interface or the recorder interface and to set ADC BUSY or MTA BUSY each time it is asked for such service.

In all types of operations, the data is transferred from the AD converter interface to the computer and from the computer to the recorder interface through the automatic data channel.

To operate this data transfer system, either test program or interrupt program may be used, depending on the sampling rate and the operation mode. In sequential mode or addressable mode with low sampling rate operation, other input-output devices may be included in this system to make use of the large amount of the computer's free time.

In internal clock operation, set MTA BUSY after the first DF (Digitization Finisf).

In external clock operation, set MTA BUSY

- (1) after ADC BUSY is set if $R > 1/(X - 39 \times 10^{-6})$ sps
- (2) after first DF (SM operation) or first ADC DONE (AM operation) if $350 \text{ sps} \leq R \leq 1/(X - 39 \times 10^{-6})$ sps
- (3) after Nth DF (SM operation) or Nth ADC DONE (AM operation) if $R < 350$ sps

$$N = 2 - 2R/700 \quad \text{or} \quad w(1 - 3R/700) + 4R/700$$

depending on which is larger. Take the greater integer for numbers with fractions.

R: sampling rate in samples per second

X: pulse width of OS4 in the WSC generator in seconds

w: number of words per record