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Effect of GaN surface treatment on Al_2O_3/*n*-GaN MOS capacitors

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The surface preparation for depositing Al_2O_3 for fabricating Au/Ni/Al_2O_3/*n*-GaN (0001) metal oxide semiconductor (MOS) capacitors was optimized as a step toward realization of high performance GaN MOSFETs. The GaN surface treatments studied included cleaning with piranha (H_2O_2:H_2SO_4 = 1:5), $(NH_4)_2S$, and 30% HF etches. By several metrics, the MOS capacitor with the piranha-etched GaN had the best characteristics. It had the lowest capacitance–voltage hysteresis, the smoothest Al_2O_3 surface as determined by atomic force microscopy (0.2 nm surface roughness), the lowest carbon concentration (∼0.78%) at the Al_2O_3/*n*-GaN interface (from x-ray photoelectron spectroscopy), and the lowest oxide-trap charge ($Q_T = 1.6 \times 10^{11}\,cm^{-2}eV^{-1}$). Its interface trap density ($D_{it} = 3.7 \times 10^{12}\,cm^{-2}eV^{-1}$), as measured with photon-assisted capacitance– voltage method, was the lowest from conduction band-edge to midgap. © *2015 American Vacuum Society*.
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I. INTRODUCTION

GaN-based metal–insulator–semiconductor structures, such as metal oxide semiconductor (MOS) capacitors, are the basic building blocks for field effect transistors. High quality structures are essential to support large gate voltage swings, and high temperature operation with minimum gate leakage. Successful coupling of high-κ dielectrics with high mobility III-N semiconductor requires careful substrate cleaning.[1] The quality of the insulator/GaN interface strongly affects the electrical properties of devices; therefore, good cleanliness and low roughness of the GaN surface prior to the deposition of the insulator is key.[2]

Gallium nitride is the semiconductor of choice for high power, high temperature, and high frequency electronic devices, because of its wide bandgap (3.43 eV at 300 K), high breakdown field, high electron mobility (in 2D electron gas at AlGaN/GaN interface), thermal conductivity, and radiation hardness.[3] Al_2O_3/GaN structures are being incorporated into normally off high-voltage power switching devices.[4,5] Finding a suitable gate oxide is essential to fabricate GaN-based MOS devices with outstanding performance. In selecting the gate oxide, a band offset larger than 1 eV is needed to suppress leakage currents.[6] In this respect, Al_2O_3 is an excellent high-κ dielectric, due to its high permittivity (8–10), large bandgap (8.9 eV), and high energy conduction band edge offset with GaN [2.13 eV (Ref. 2)], which prevents current tunneling.[7] Al_2O_3 gate dielectrics are typically deposited by atomic layer deposition (ALD) because of its perfect 3D conformality, 100% step coverage, and pinhole-free films.[8] The major obstacle to using Al_2O_3 deposited on III–V semiconductors is its high-interface trap density ($D_{it} > 10^{13}\,cm^{-2}eV^{-1}$).[9] These trap states are caused by rough interfaces, incomplete and unsatisfied chemical bonds, and impurities.[10]

This paper verifies the effectiveness of an *ex situ* wet chemical etching of GaN prior to ALD of Al_2O_3. Since the insulating dielectric must be deposited and is not produced by thermal oxidation, cleaning prior to the oxide deposition must remove native oxides, carbon, and other contamination while leaving the surface smooth. Therefore, reducing contamination (particulate, metallic, and chemical) is extremely important for manufacturing high performance semiconductor devices, as this prevents gate oxide breakdown, reduces contact resistance, minimizes MOS transistor threshold voltage shift, and maximizes peak channel mobility.[11]

GaN surface preparation prior to Al_2O_3 deposition has been studied by just a few researchers.[12,13] Studying various wet chemical treatment of GaN prior to ALD Al_2O_3 deposition, Nepal *et al.*[12] found treating the GaN surface by piranha etching produced the lowest total trapped charge density and smoothest Al_2O_3 films. Their findings motivated our study to investigate the effect of surface pretreatment on the average density of all oxide trapped charge as well as Al_2O_3/GaN interface trap density.

Machuca *et al.*[14] used wet etching in H_2O_2:H_2SO_4 (1:4) followed by annealing at ultrahigh vacuum ($\leq 10^{-10}$ Torr) at 700 °C to remove carbon and oxygen. Lee *et al.*[11] removed residual carbon contamination from photolithography process and residual chlorine or fluorine after surface acid treatment by UV/O_3 exposure. HF solutions remove native oxides from GaN and passivate its surface by binding the exposed dangling bonds with hydrogen.[15] Also, HF-based solutions remove both carbon and oxygen from the GaN surface.[16] $(NH_4)_2S$ effectively eliminates the native oxide and protects GaN surface from immediate reoxidation by creating Ga-S monolayer.[17]

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In this study, various wet-etching methods for cleaning the GaN surface, and the concentrations and energies of defects (oxide-trap charge and interface trap charge) were quantified as functions of process parameters, to provide guidance for improving the reliability of MOS devices. The impacts of both the surface and interface chemistry and roughness on the electrical properties were considered.

II. EXPERIMENT

Ga-polar *c*-plane wurtzite GaN epilayers on sapphire were employed for the fabrication of Al_2O_3/*n*-GaN MOS capacitors. The epilayers consisted of 1.5 μm thick, *c*-plane GaN grown on *a*-plane sapphire via metal-organic chemical vapor deposition, using a 25 nm thick AlN buffer layer. The GaN epilayers were deposited at 1050 °C and 150 Torr, using a V/III ratio of 3500. The precursors for the GaN epilayers were trimethylgallium and ammonia. Silicon doping, on the level of 1×10^{18} cm^{-3}, was achieved through the addition of silane.

Al_2O_3 was deposited by ALD at 280 °C using trimethylaluminum (TMA) and deionized water in a Cambridge NanoTech Savannah 200 ALD System.[13] Ultrahigh purity nitrogen (99.999%) flowing at 20 sccm was the carrier gas for the precursors. An ALD cycle consisted of a 0.015 s TMA pulse followed by a 20 s purge with N_2; and a 0.015 s pulse of deionized water followed by a 20 s purge. The 20 s purging step with ultrahigh purity nitrogen between precursor exposure was intended to remove unreacted precursors and reaction by-products from the ALD chamber and thereby ensure a true ALD mode (self-limited surface reaction limited). A total of 250 ALD cycles were employed. For all of these samples, the Al_2O_3 thickness was approximately 20 nm.

Four surface preparations were evaluated. Three samples were cleaned using piranha (H_2O_2:H_2SO_4 = 1:5), $(NH_4)_2S$, and 30% HF etches; the fourth sample was left untreated. Circular capacitors of four different diameters (50, 100, 150, and 300 μm) were created by photolithography. Ni/Au (20/100 nm) metal contacts were deposited by e-beam evaporation.

The Al_2O_3/GaN MOS capacitors were electrically characterized by capacitance–voltage (C-V) measurements at 1 MHz using a Keithley 4200 SCS parameter analyzer. C-V hysteresis of the MOS capacitors was quantified by the shift in flatband voltage.[18] For hysteresis measurements, the voltage on the metal oxide semiconductor capacitors was swept from zero to accumulation (+3 V), accumulation to deep depletion (−8 V), and from deep depletion back to accumulation (+3 V). From the flatband capacitance (C_{FB})[19] obtained at each voltage sweep, the flatband voltage (V_{FB}) was calculated from the C-V plot based on the following equation:

$$C_{\mathrm{FB}} = \frac{\varepsilon_s C_{\mathrm{ox}}}{C_{\mathrm{ox}}\lambda + \varepsilon_s}, \tag{1}$$

where ε_s is the permittivity of GaN and C_{ox} the oxide capacitance at accumulation. The Debye length λ can be expressed by $\lambda = \sqrt{(\varepsilon_s KT)/(q^2 N_D)}$, where N_D is donor concentration in GaN, q is an electron charge, and K is the Boltzmann constant. The average electron trap density (Q_T) along the GaN bandgap (E_g) was obtained from C-V hysteresis based on the following equation:[20]

$$Q_T = \frac{C_{\mathrm{ox}}\Delta V_{\mathrm{FB}}}{E_g}. \tag{2}$$

Because of its wide energy band gap, the thermal generation rate of electron–hole pairs is insignificant for GaN at room temperature.[21] Thus, GaN enters deep depletion in C-V plots due to the low minority carrier (holes) generation rate; an inversion layer is not formed within the time frame of practical C-V measurements. According to Shockley–Read–Hall statistics, the emission time constant increases exponentially with distance from the GaN band edge and, as a result, electrons captured deep in the bandgap of GaN cannot emit to the conduction band.[22] Surface states cannot be estimated at room temperature by the Terman or conductance technique because electrons are unavailable to be captured in inversion region. Consequently, photon-assisted[23,24] or high temperature C-V is needed to estimate the interface trap density. From C-V measurements at higher temperatures (up to 400 °C, if leakage currents is not too large) the defects energies that are deep within the bandgap can be estimated.

In this study, the photon-assisted high frequency capacitance voltage procedure developed by Swenson[24] was applied to measure interface state density. In this method, exposure to UV light shifts the deep depleted region of the Al_2O_3/GaN C-V plot to inversion. In this manner, the leakage current coming from the gate in depletion mode causes interface states to ionize. For this study, a monochromatic (365 nm) UV light source (photon flux 2×10^{19} photon/s cm^2) was employed. If the semiconductor is in inversion instead of deep depletion, then any interface states that ionize will almost immediately capture inversion electrons. In this procedure, first the dc voltage was swept at 100 mV/s from deep depletion to the accumulation region under complete darkness at 1 MHz to collect a C-V plot. Next, the sample was illuminated by the monochromatic UV light source, and bias was applied for a hold time of 8 min at −8 V (pre-soak voltage at deep depletion). A second before completion of the hold time, the UV light was turned off and dc voltage was swept from deep depletion to accumulation (−8 V to 3 V) at a dc voltage sweep rate of 100 mV/s. The ideal C-V plot was obtained by shifting the dark curve by the difference in built-in potential between dark- and post-UV C-V plots.[25] This difference in built-in potential includes the interface state and fixed charges in Al_2O_3. dV is the voltage difference at a constant capacitance between the ideal C-V plot and the post-UV C-V plot, and it is proportional to the interface state charge. If the GaN doping concentration was assumed to be constant, then the amount of band bending or semiconductor surface potential was determined by $\psi_s = (q\varepsilon_s\varepsilon_0\bar{N}_d A^2)/2C_{\mathrm{sc}}^2$, where $\bar{N}_d$ is the average doping concentration, $C_{\mathrm{sc}} = (C_{\mathrm{ox}}C_m)/(C_{\mathrm{ox}} - C_m)$, the depletion capacitance and ε_0 is the permittivity in vacuum. D_{it} was calculated based on the following equation:[24]

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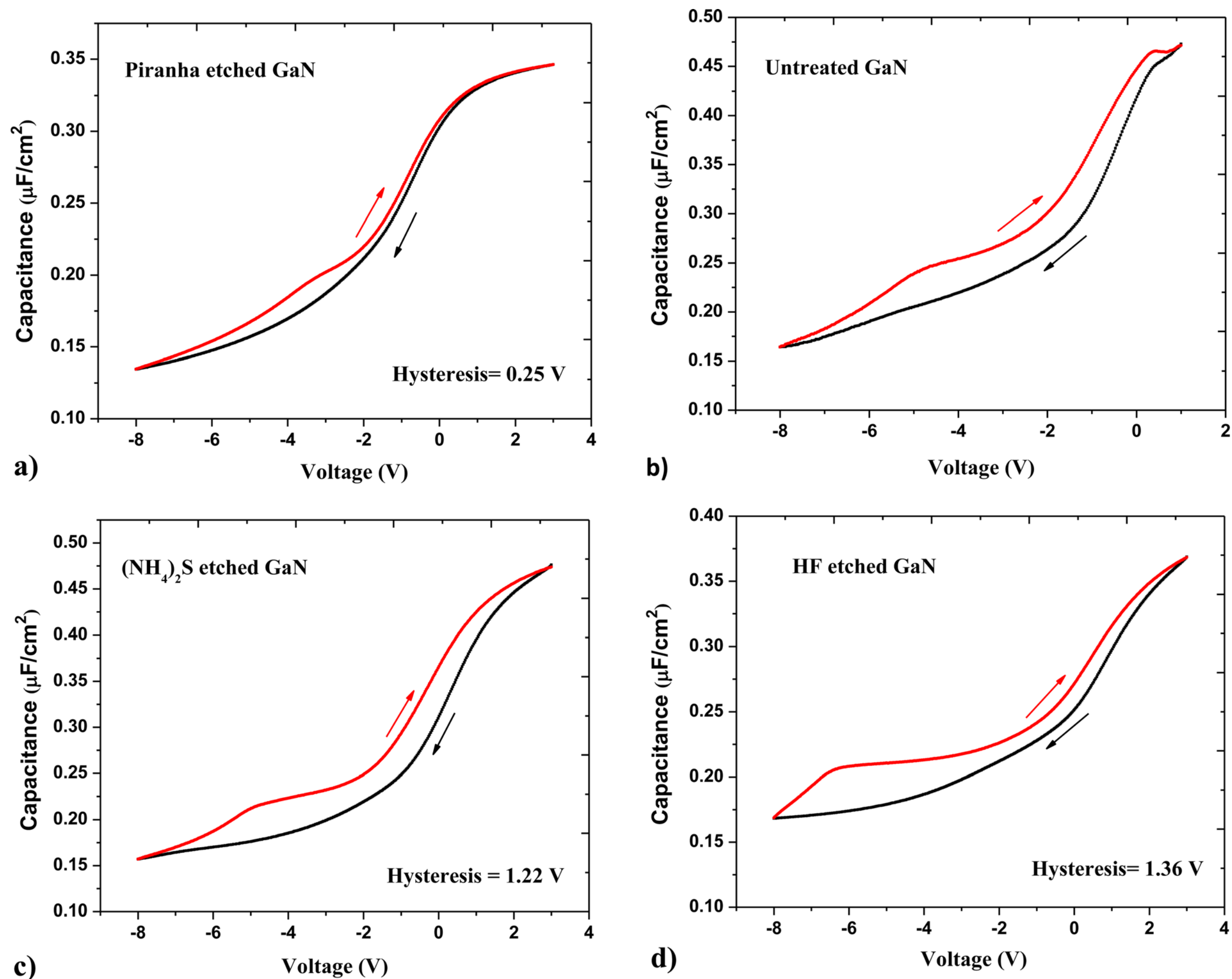

FIG. 1. (Color online) Capacitance–voltage hysteresis plots of Al_2O_3/GaN for (a) piranha, (b) no treatment, (c) $(NH_4)_2S$, and (d) 30% HF surface treatments.

$$D_{\text{it}} = \frac{C_{\text{ox}}}{qA}\left(\frac{d\Delta V}{d\psi_s}\right). \quad (3)$$

The electrical performance attributes of the Al_2O_3/GaN MOS capacitors were connected to the physical and chemical properties of the devices. The Al_2O_3 surface roughness was assessed by atomic force microscope (AFM, Digital Instrument MultiMode SPM from Veeco Instruments, Inc.) operating in tapping mode. Identification of Al_2O_3 surface contaminants and their relative concentrations were measured as a function of depth by x-ray photoelectron spectroscopy (XPS) with argon ion sputtering using a K-Alpha XPS from Thermo Scientific.

III. RESULTS AND DISCUSSION

The C-V hysteresis plots show that capacitors with piranha-treated GaN surface exhibited the least hysteresis (0.25 V) (Fig. 1).

The small shift in flatband voltage and small hysteresis window indicates a low interface trap density. The C-V hysteresis for $(NH_4)_2S$ and HF etched MOS capacitors were 1.22 and 1.36 V, respectively. The GaN surface without treatment exhibited the largest hysteresis. It was not possible to perform a voltage sweep of more than 1 V on the untreated MOS capacitor as the capacitance appeared to decrease sharply beyond 1 volt due to dielectric breakdown and was not quantified due to its different dc voltage sweep range. The lowest average density of all trapped electrons ($Q_T = 1.6 \times 10^{11}\,\text{cm}^{-2}\text{eV}^{-1}$) occurred with the piranha-etched sample (Table I).

The piranha-treated GaN surface produced the smoothest Al_2O_3 surface with minimum roughness (RMS = 0.2 nm); the surface roughness of $(NH_4)_2S$, HF, and untreated samples were rougher (Fig. 2).

For comparison, when Nepal *et al.*[12] deposited Al_2O_3 on GaN at 260 °C, their Al_2O_3 surface roughness was 0.37 nm for the piranha-treated GaN surface. The carbon concentration

TABLE I. C-V characteristics showing effect of GaN surface treatment.

GaN surface treatment	Hysteresis at flatband voltage (ΔV_{FB})	Average density of all trapped electrons, $Q_T \times 10^{11}$ ($\text{cm}^{-2}\text{eV}^{-1}$)
$(NH_4)_2S$	1.22	10.7
HF	1.36	9.2
Piranha	0.25	1.6
Untreated GaN	1.52	11.7

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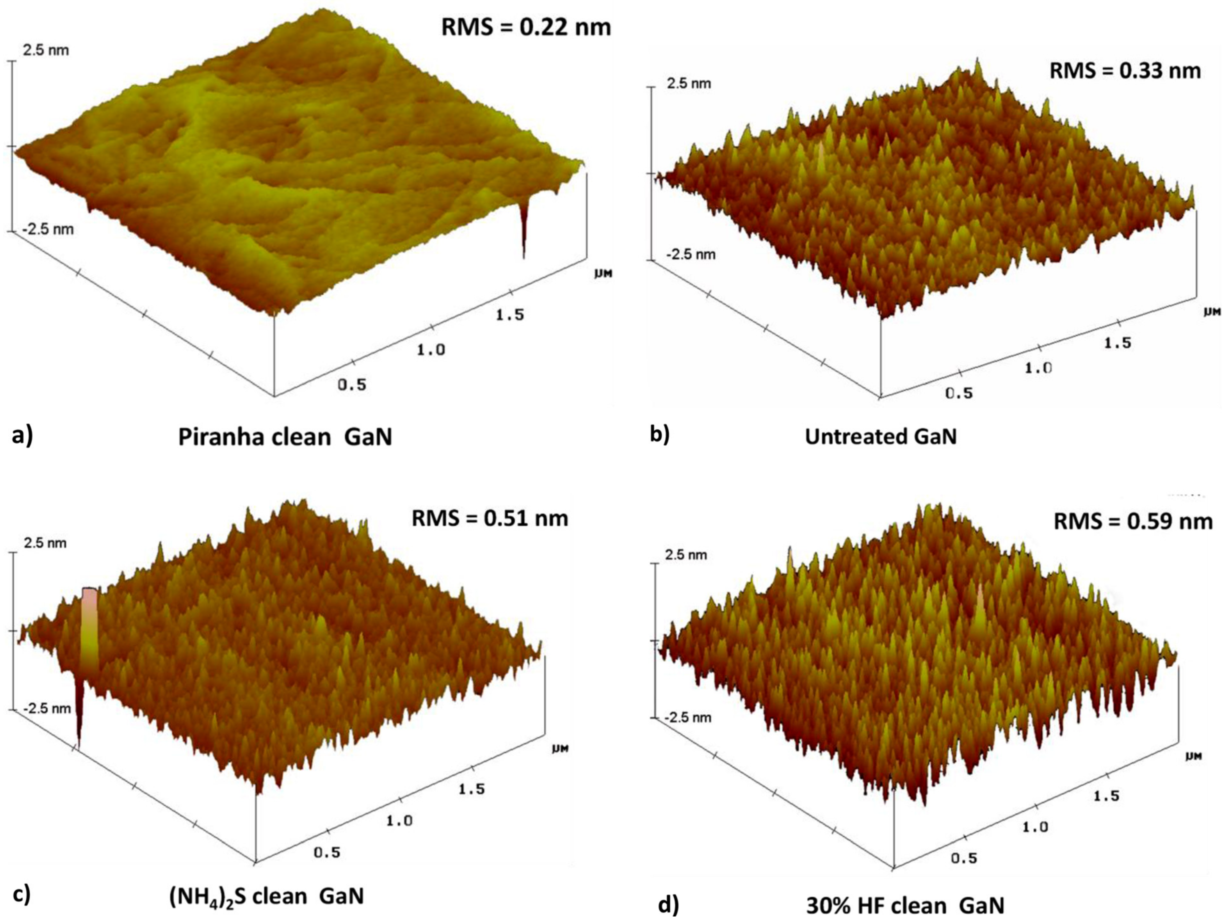

FIG. 2. (Color online) Atomic force microscopy images of Al_2O_3 on GaN where GaN surfaces cleaned by (a) piranha, (b) no treatment, (c) $(NH_4)_2S$, and (d) 30% HF.

was lowest for the piranha-treated sample in the bulk oxide and at the Al_2O_3/GaN interface (Table II).

For the piranha-treated sample, the average carbon concentration was 0.2 and 0.78 at. % in the bulk and at the Al_2O_3/GaN interface, respectively. The carbon in the Al_2O_3 was attributed to residuals from the ALD precursor (TMA) and not surface contamination from exposure to air.

During photon-assisted high-frequency capacitance–voltage characterization, there was an upward shift of the deep depletion in the C-V plot due to the UV illumination. This shift was highest for the piranha treated sample [Fig. 3(a)] and can be attributed to the generation of minority carriers in excess of the thermal equilibrium concentration. For the untreated GaN sample [Fig. 3(b)], the shift is relatively small compared to the treated samples due to low generation of the minority carriers.

TABLE II. XPS analysis showing atomic percentage of carbon concentration in oxide and at Al_2O_3/GaN interface.

GaN surface treatment	Carbon concentration in oxide (%)	Carbon concentration at interface (%)
$(NH_4)_2S$	0.60	4.14
HF	0.32	3.75
Piranha	0.20	0.78
Untreated GaN	0.55	4.27

From Fig. 4, the average D_{it} for piranha, $(NH_4)_2S$, HF, and untreated samples were 3.7×10^{12}, 8.0×10^{12}, 1.2×10^{13}, and $1.7 \times 10^{13}\,cm^{-2}eV^{-1}$, respectively. From the trend of the D_{it} distribution along the bandgap, both $(NH_4)_2S$ and Piranha etched sample was close to each other and D_{it} distribution of $(NH_4)_2S$ is slightly lower compared to Piranha. But based on average values of the data points along the bandgap, the average interface trap density ($D_{it} = 3.7 \times 10^{12}\,cm^{-2}eV^{-1}$) along the bandgap of GaN was minimum for piranha-treated GaN sample compared to the rest of the samples. For the untreated sample, the D_{it} distribution was relatively high (on the order of $10^{14}\,cm^{-2}eV^{-1}$) at the conduction band edge. Beyond 0.6 eV from the conduction band of GaN, it was not possible to acquire D_{it} distribution for the untreated sample and this is attributed to the depletion capacitance, C_{sc} extracted from Fig. 3(b).

IV. CONCLUSIONS

This study is concerned with developing the best electrically performing ALD Al_2O_3/GaN interface. The piranha-treated GaN surface exhibited the lowest hysteresis; and, as a result the lowest average density of trapped electrons. The average interface trap density ($D_{it} = 3.7 \times 10^{12}\,cm^{-2}eV^{-1}$)

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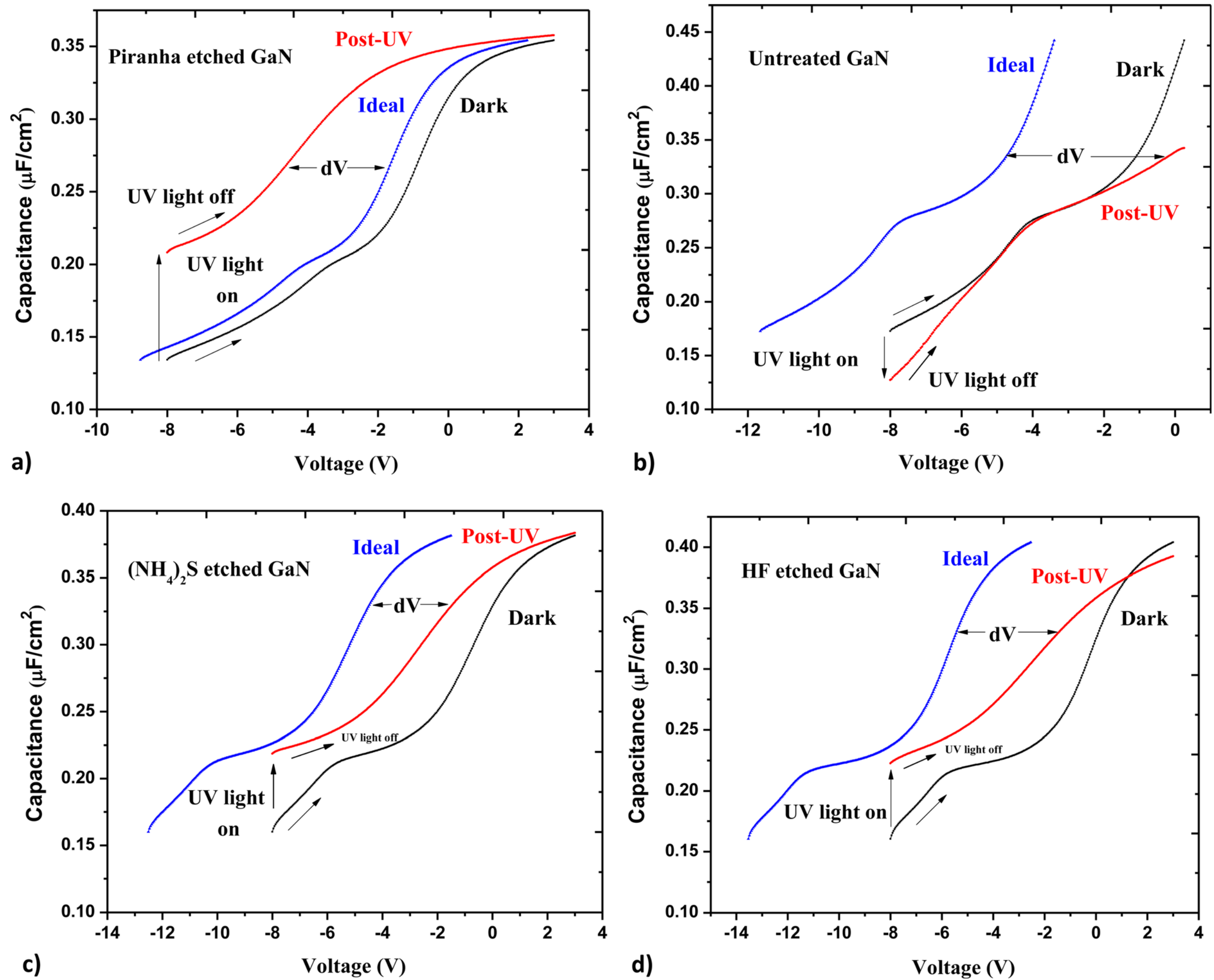

FIG. 3. (Color online) C-V plots measured at dark, post-UV exposure and ideal C-V plot for MOS capacitors with (a) piranha, (b) untreated (c) $(NH_4)_2S$, and (d) 30% HF treated GaN surface before oxide deposition.

along the bandgap of GaN was lowest for the piranha-treated GaN sample although the trend of D_{it} distribution for $(NH_4)_2S$ was lower. D_{it} for samples treated with HF, and the untreated sample were higher. These electrical characteristics were strongly supported with the findings from surface morphology. Carbon concentration was the lowest for piranha-treated sample and the smoothest Al_2O_3 surface was produced on the piranha-treated GaN.

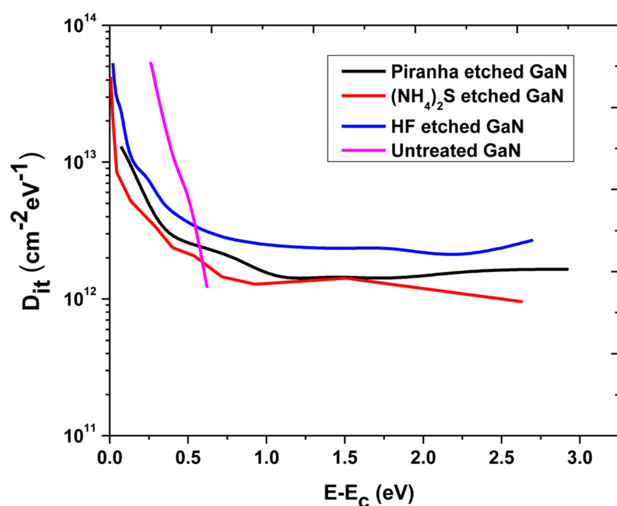

FIG. 4. (Color online) Plots of D_{it} ($cm^{-2}eV^{-1}$) vs energy (eV) from the conduction band (E_c) of Al_2O_3/GaN for no treatment, 30% HF, $(NH_4)_2S$, and piranha surface treatments.

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