IMPROVEMENTS IN RADIATION DETECTION ELECTRONICS

by

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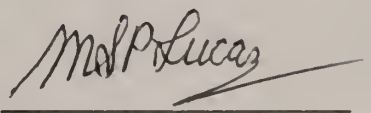

Major Professor

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

This thesis is primarily concerned with the design, construction, and testing of a low-power, high-accuracy, dual-rate integrating analog-to-digital converter (ADC) with a relatively fast conversion rate. Such ADCs are useful for applications in digital audio systems, radiation detection electronics, and portable digital filtering systems. However, in this thesis, attention is focused on improving the radiation detection electronics.

Two types of ADCs that have commonly been used in radiation detection electronics are the Wilkinson-type ADCs and the successive approximation ADCs. The Wilkinson-type ADCs are popular because of their simple circuits and relatively fast conversion rate. The successive approximation ADCs are used because of their high speed. However, where high accuracy is required in radiation detection electronics, these two types of ADCs require correction circuits. Several correction circuit techniques have been reported and are described in the thesis. Unfortunately these correction circuits require more components and therefore increase the power consumption.

The dual-rate integrating ADC is able to provide high accuracy by taking advantage of its linear and continuous analog-to-digital conversion behavior which depends on using accurate sample-hold circuit, accurate and stable system clock and accurate switching control logic. In this

thesis, each of this circuit part will be studied in detail. Another advantage of this converter includes the good input voltage noise rejection since the input voltage is sampled first into the hold capacitor. Because the sampling time is required in addition to the conversion time, a fast and accurate sample-hold circuit with small capacitor size can be used to reduce the sampling time.

This thesis will also look at how to reduce the conversion time using the dual-rate integrating technique. Three methods to be discussed include using smaller size hold capacitor, using larger integrating currents while maintaining their ratio and reducing the absolute threshold voltage of the coarse count comparator. Moreover, because this ADC circuit can be made simpler through careful design and the correction circuit for it is redundant, a low-power ADC system can be built. Because of the several advantages of this ADC, it can possibly be used to replace the commonly-used Wilkinson-type ADC in radiation detection electronics especially where high-accuracy, low-power and relatively fast conversion rate are required.

CHAPTER 1. EXISTING RADIATION DETECTION ELECTRONICS TECHNIQUES

1.1. The Wilkinson-Type ADC

The Wilkinson-type ADC has been widely accepted in radiation detection electronics because it is a simple, relatively fast and has better differential linearity than successive approximation ADC.

1.1.1 Operating Principle of the Wilkinson-Type ADC

The operating principle of the Wilkinson-type ADC is shown graphically in Figure 1. The input pulse (a) of amplitude Vamp is first stretched to pulse (b) with the same amplitude as pulse (a) using a pulse stretcher circuit. The amplitude information of pulse (a) is therefore retained in pulse (b). At the amplitude of input pulse (a), a voltage ramp (c) of constant slope and good linearity is produced from a linear ramp generator. Simultaneously, a gate signal (d) is produced and turned on. The gate signal is turned on until the comparator senses the ramp voltage (c) as equal to the stretched waveform (b) amplitude. The pulses are counted during the time the gate signal is on. The number of pulses counted or recorded is proportional to the gate signal (d) turn-on time which is also proportional to the input pulse amplitude. Therefore, the number of pulses recorded is a measure of the amplitude of the input pulse signal.

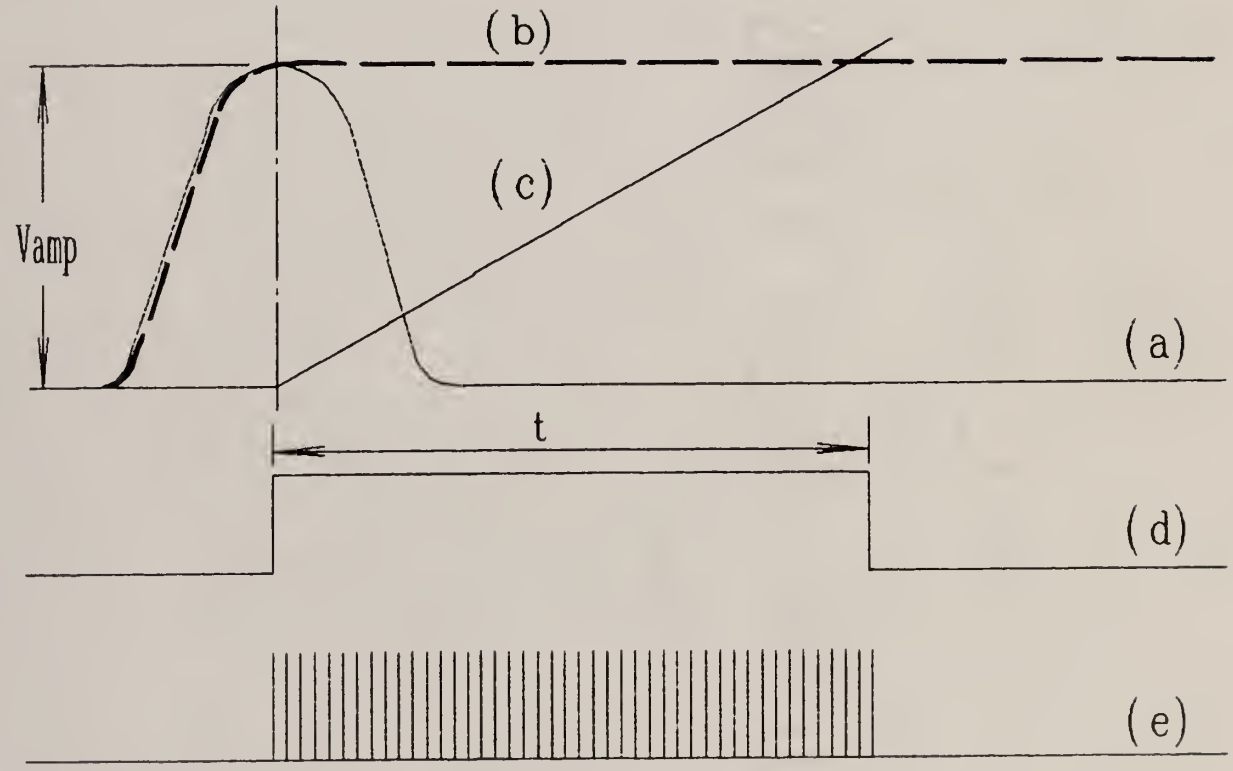


Fig.1. Wilkinson-type ADC waveforms. (a)Input pulses; (b)Stretched input pulses; (c)Linear ramp; (d)Gate signal; (e)Clock pulses.

1.1.2 Disadvantages of the Wilkinson-Type ADC

Though this type of converter circuit is simple, it has three main error sources, namely:

a). The stretched pulse is not identical in height to the input pulse,

b). The linearity of the ramp and the slope stability,

c). The stability of the pulse generator/counting clock frequency.

Moreover, the speed of conversion of this type of converter is slower than that of the successive approximation ADC.

1.1.3 Improvements in the Wilkinson-Type ADC

In a publication entitled, "Increase in speed of Wilkinson-type ADC and improvement of differential non-linearity", by Kinbara[1], a method called Variable Digital Digital Offset (VDDO) is developed. It can be seen from the Wilkinson-type ADC spectra in Figure 2, there is a large variation in the width of the odd-even channel. According to the author, this is the result of the changes in the triggering level of the channel scalar between the odd and even positions. In other words, the channel scalar interacts with the whole counting system during either the odd number or even number positions, resulting in different triggering level of the channel scalar when in odd and even channel positions. This problem results in differential

non-linearity. The VDDO method which is similar to the sliding-scale technique can be used to improve the differential non-linearity of the Wilkinson-type ADC by distributing the odd-even errors in the Wilkinson-type ADC over a number of channels. The result is a reduced differential non-linearity value to +/-0.043 % (See Figure 3), with an increased clock rate of 300 Mhz but this complicates the Wilkinson-type ADCs by requiring more components. This means increase the power consumption at higher clock frequency.

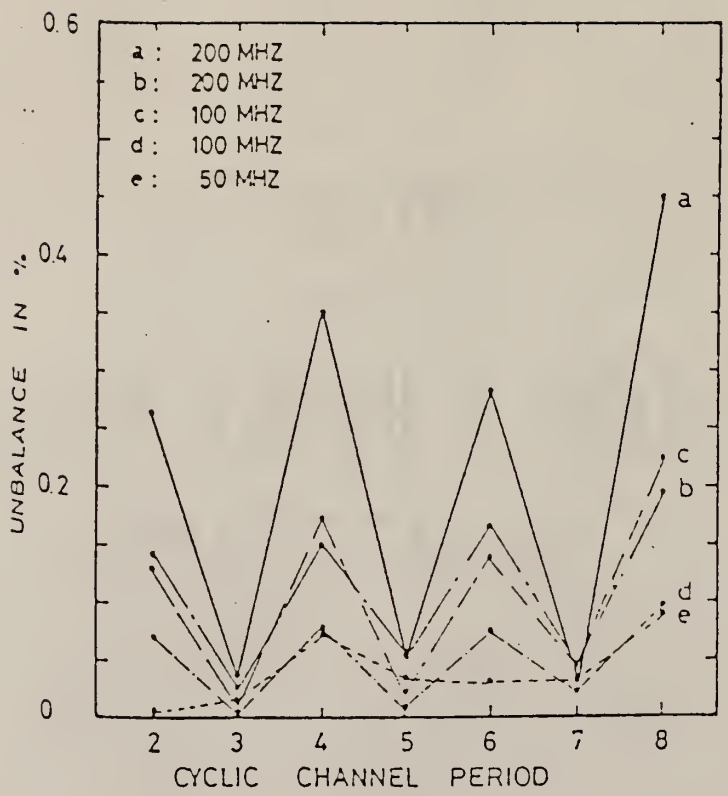


Fig.2. Periodicity unbalance of ordinary Wilkinson-type ADC (after Kinbara[1]).

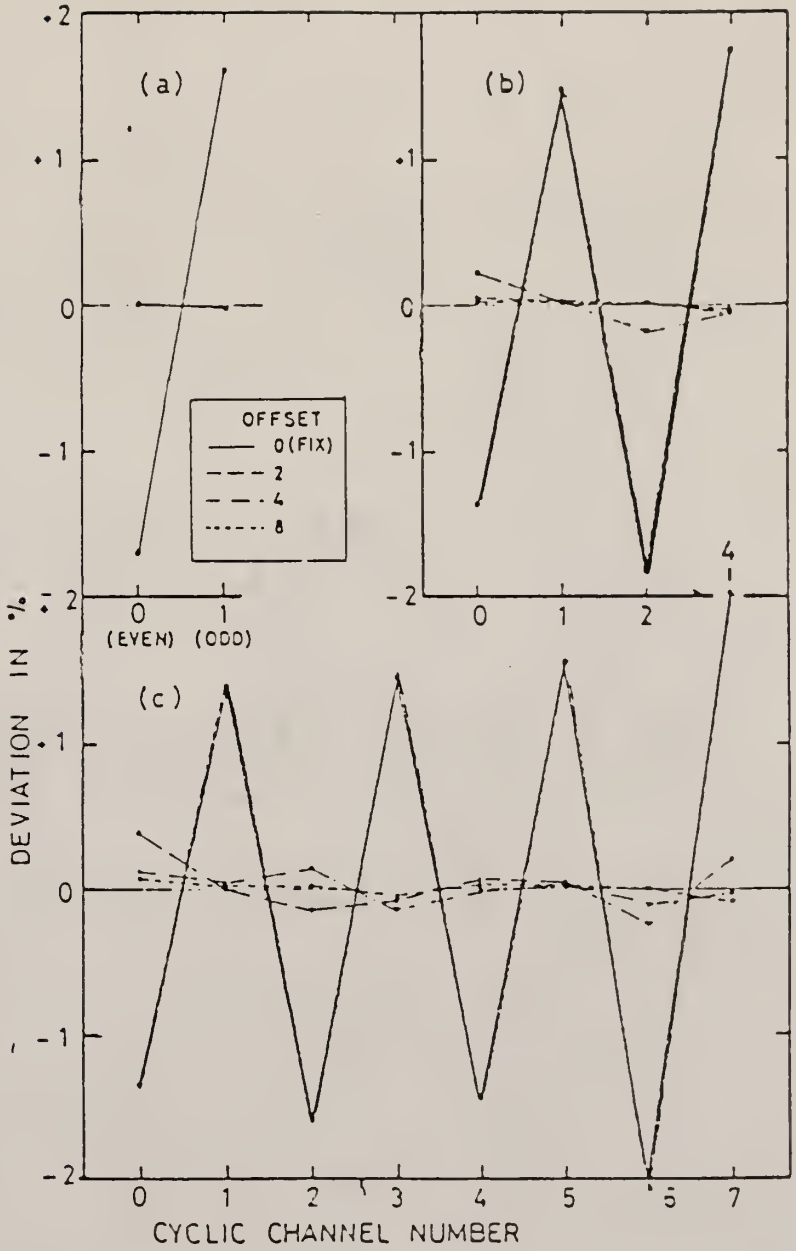


Fig.3. Cyclic channel deviation of the spectrum obtained with the VDDO method (after Kinbara[1]).

1.2 The Successive Approximation ADC

Besides the Wilkinson-type ADC, the successive approximation ADC is also commonly used in the radiation detection electronic because of its very fast conversion rate.

1.2.1 Operating Principle of the Successive Approximation ADC

The successive approximation ADC consists of the digital-to-analog converter (DAC), a comparator and a successive approximation register as shown in Figure 4. The DAC and the successive approximation register are placed in the feedback loop with the comparator.

The DAC output is compared with the analog input pulse amplitude, starting from the high order bit to the least order bit, one bit by one bit. The bit is first set to 1. If the DAC output is greater than the input, the bit is set to zero. However, if the DAC output is less than the input, the bit is left at one. The register then moves on to the next bit. At the end of the conversion, those bits left in the one state cause a current to flow at the output of the DAC. This current should equal the current Iin to within +/- 1/2 LSB. These techniques are capable of high speed conversion because an 'n' bit conversion requires only 'n' trials (typically 100,000 conversion per second).

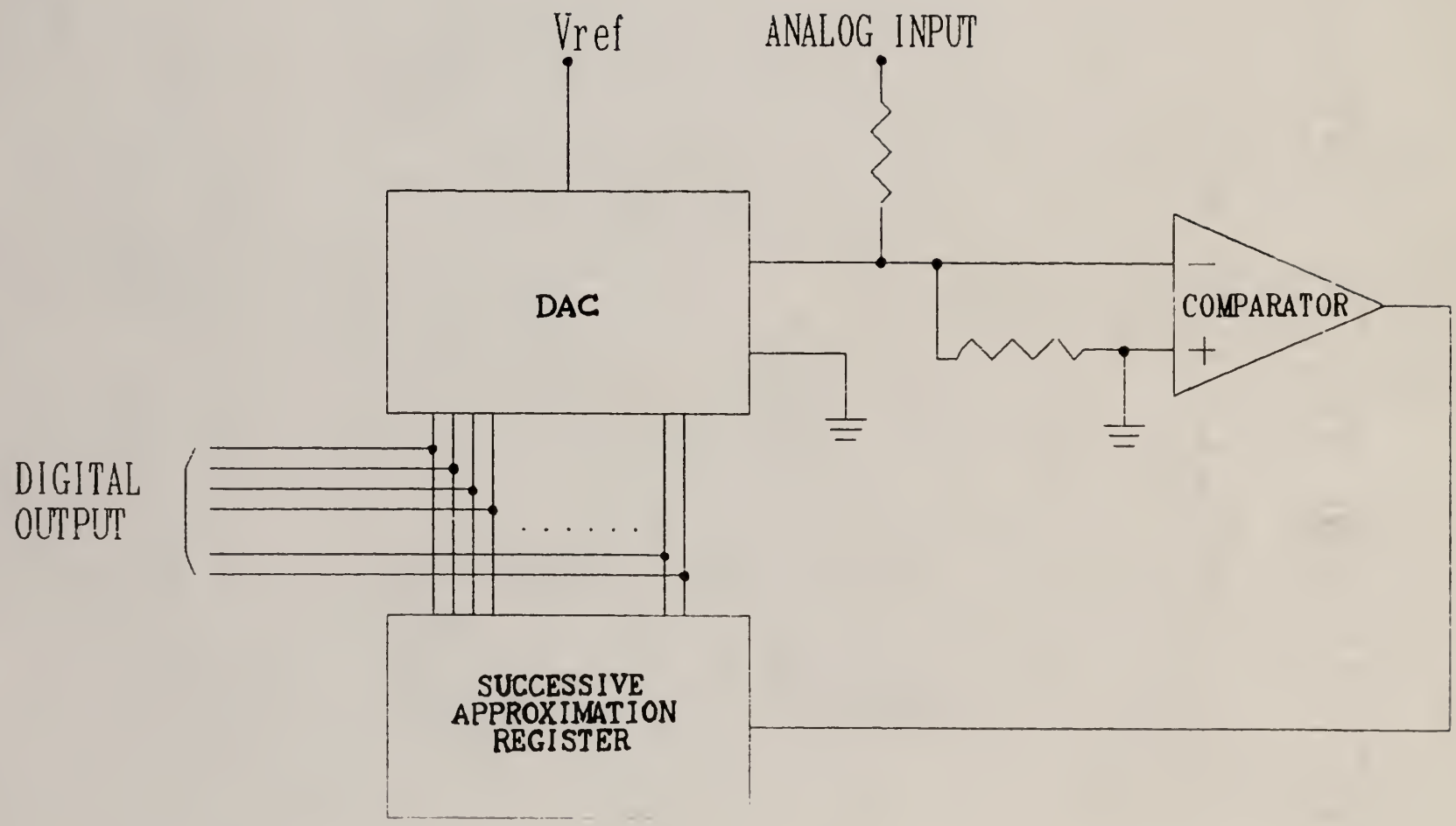


Fig.4. Typical successive approximation ADC schematic.

1.2.2 Disadvantages of Successive Approximation ADC

Despite that the successive approximation ADC conversion time is faster than the Wilkinson-type ADC for larger number of analyzer channels (the conversion time of successive approximation ADC increases as the logarithm of the number of channels compared with the conversion time of the Wilkinson-type ADC which increases linearily with the number of analyzer channels), it has some disadvantages.

a). Its linearity and differential linearity is worse than that of the Wilkinson-type ADC. This accuracy is affected by the cumulative errors arising in the subtraction process.

b). Critical components are required for achieving circuit linearity. These components may be costly. Components matching to achieve accuracy is also very important.

c). It must be used in conjunction with a sample and hold when the input is an AC signal.

1.2.3 Improvements in Successive Approximation ADC

Since the dominant accuracy error of the successive approximation ADC is its differential nonlinearity, methods to improve the differential linearity of the successive approximation ADCs have been reported.

One method known as the Gatti method[2] or the sliding-scale method, subtracts a random level ranging up to a few

bits from the analogue signal while adding the equivalent digital code to the digital output. The error in channel widths produced by variations in the components that make the digital to analog comparison is distributed over several channels, thereby improving the differential linearity.

Another method, the cycling or the interactive technique method, is reported by Kandiah et al[3]. In this method, a smaller number of precision resistors is used than in the conventional successive approximation method. The stretcher input signal is held in the first sample-hold circuit. This signal is compared with a voltage that is equal to the most significant bit voltage. A voltage equal to the most significant bit is subtracted from the signal voltage if the signal voltage is more than the most significant bit voltage. The difference is then precisely amplified by a factor of two. The resulting signal is stored in the second sample-hold circuit. The first sample-hold circuit is cleared. The signal from the second sample-hold circuit is then transferred to the first sample-hold circuit. The process is repeated for the next bit until all the bits are processed. The disadvantages of this method are:

a). The subtracting signal and the transients in the sample -hold circuit must settle before the next cycle can begin.

b). Time is wasted during the transfer from one sample

-hold circuit to the other.

Another method as reported by Gobbur et al[4] has the improved successive approximation ADC shown in Figure 5 below. This method allows faster coding than the other two methods described above. The allowable bit setting time for the major bits has been increased without adding to the total coding time by allowing the initial accuracy of the setting of the major bits to be within eight channels. This error is corrected to an accuracy of a fraction of a channel towards the end of the coding time, when the major bits have settled. The author claims that this scheme can achieve a differential nonlinearity of better than 20 % in the basic encoder which is a large error and a total coding time of 4 microseconds, and if this scheme is combined with the 6-bit sliding register (Gatti's method), a differential nonlinearity less than 0.5% results.

Another method of improving the differential nonlinearity of the successive approximation ADC was reported by Brendle[5]. The scheme is as shown in Figure 6. A correction circuit which consists of the programmable read-only memory (PROM) and a correction DAC is added to the conventional successive approximation ADC. The PROM contains the correction numbers. When the digital word is fed into the main DCA, the PROM input is also addressed. The required main DAC accuracy and hence the correction

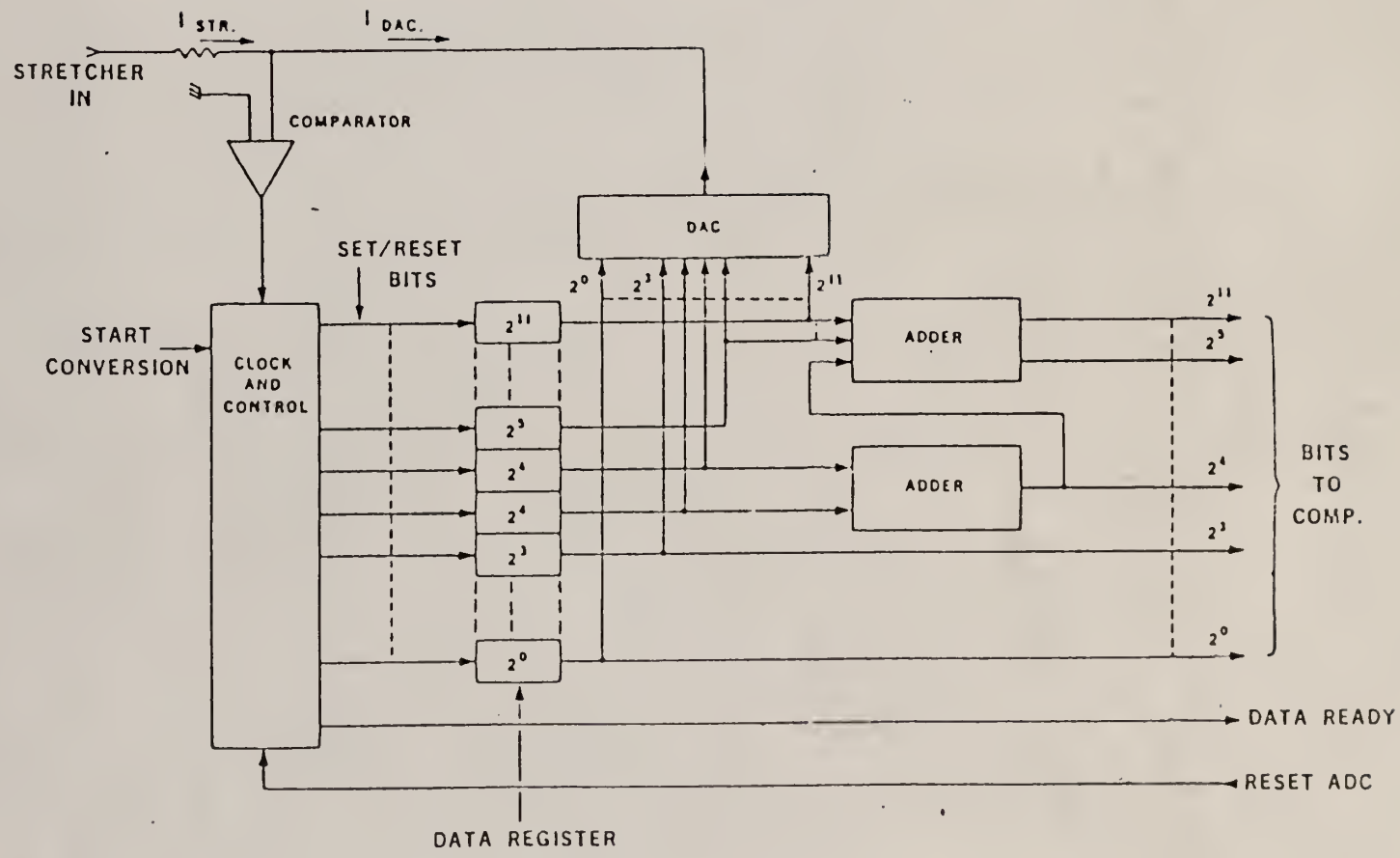


Fig.5. A simplified block diagram of a successive approximation ADC (after Gobbur[4]).

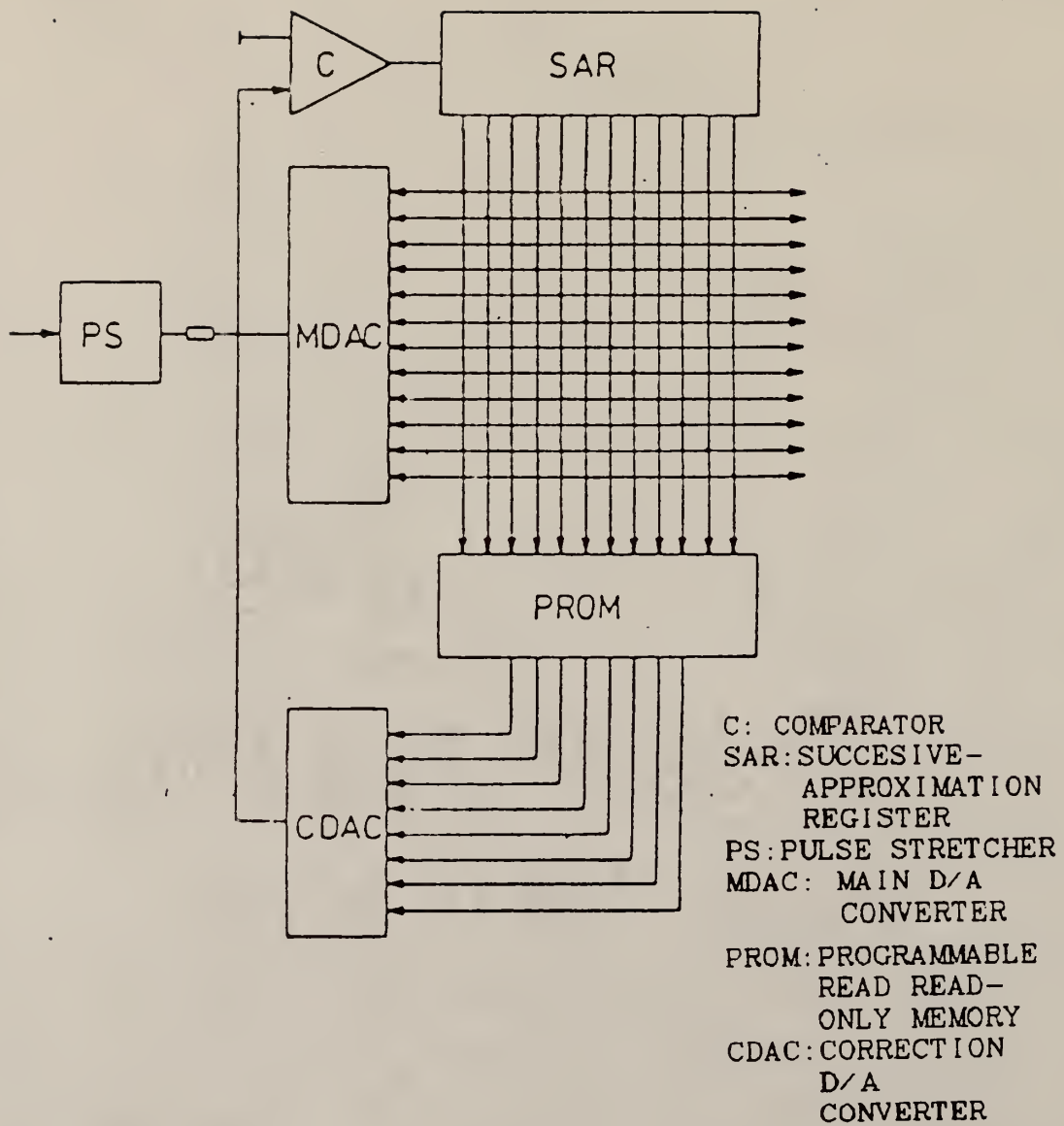


Fig.6. Circuit schematic of successive-approximation ADC with nonlinearity correction (after Brendle[5]).

accuracy, determines the correction number word length, and usually 8 bits will be enough. The correction DAC is used to convert the selected correction number. The output from the correction DAC is superimposed on the main DAC's output. The determination of the correction numbers to be stored in the PROM is described by the author.

A recent method for reducing the differential nonlinearity (DNL) of the nuclear ADC is reported by Vaidya, et al[6]. The method uses the interpolation technique to derive the quantisation steps corresponding to the last n bits of the digital code by dividing the quantisation steps due to higher significant bits of the DAC, using a chain of resistors. These quantisation steps are then compared with the analog voltage to be digitized,Va using the comparators. Va is applied as a voltage shift at both ends of the chain. The output states of the comparators' define the n bit code. A method to neutralize the comparators errors is given by the authors. The authors report a DNL of less than +/- 1% over most of the channels for a 12 bit ADC and a conversion time of about 4.5 microsecond. For further reduction of DNL, Gatti's sliding-scale technique is added. This method requires many comparators and resistors which need to be matched. The correction circuit added increases the power dissipation and the mathematical interpretations of the circuit operation are tedious too.

CHAPTER 2. NEW RADIATION DETECTION ELECTRONICS TECHNIQUES

The Wilkinson-type ADCs and the successive approximation ADCs that have commonly been used in the radiation detection electronics require additional circuits to improve their differential linearity. This requires more components and increases the power dissipation. Another method known as the dual-rate or the coarse-fine integrating method, is able to achieve high accuracy and resolution without complex circuitry. When CMOS integrated circuits are used to fabricate the dual-rate integrating ADC, the power dissipation is greatly reduced.

A high-speed, high-resolution and low-power dual-rate integrating ADC has been reported by Liu and Niu[7] for the radiation detection electronic application. Similar or slight variations of the coarse-fine integrating ADCs have also been reported by Sugawara et al[8], Taha[9], and Kayanuma et al[10].

2.1 Principle of Operation of Dual-Rate Integrating ADC

The block diagram of a basic coarse-fine integrating ADC is as shown in Figure 7. The circuit diagram is shown Figure 8.

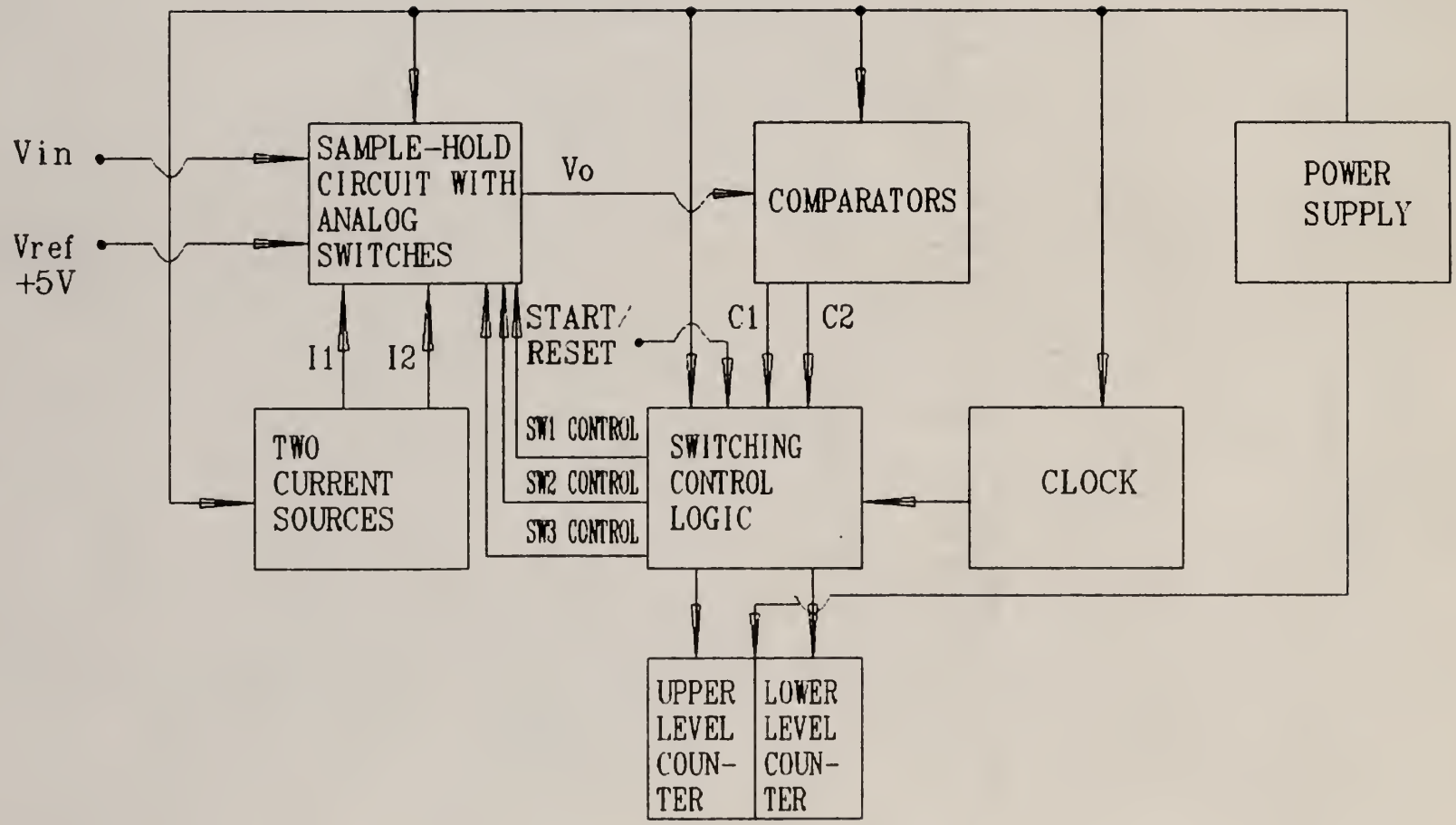


Fig.7. Block diagram of dual-rate integrating ADC.

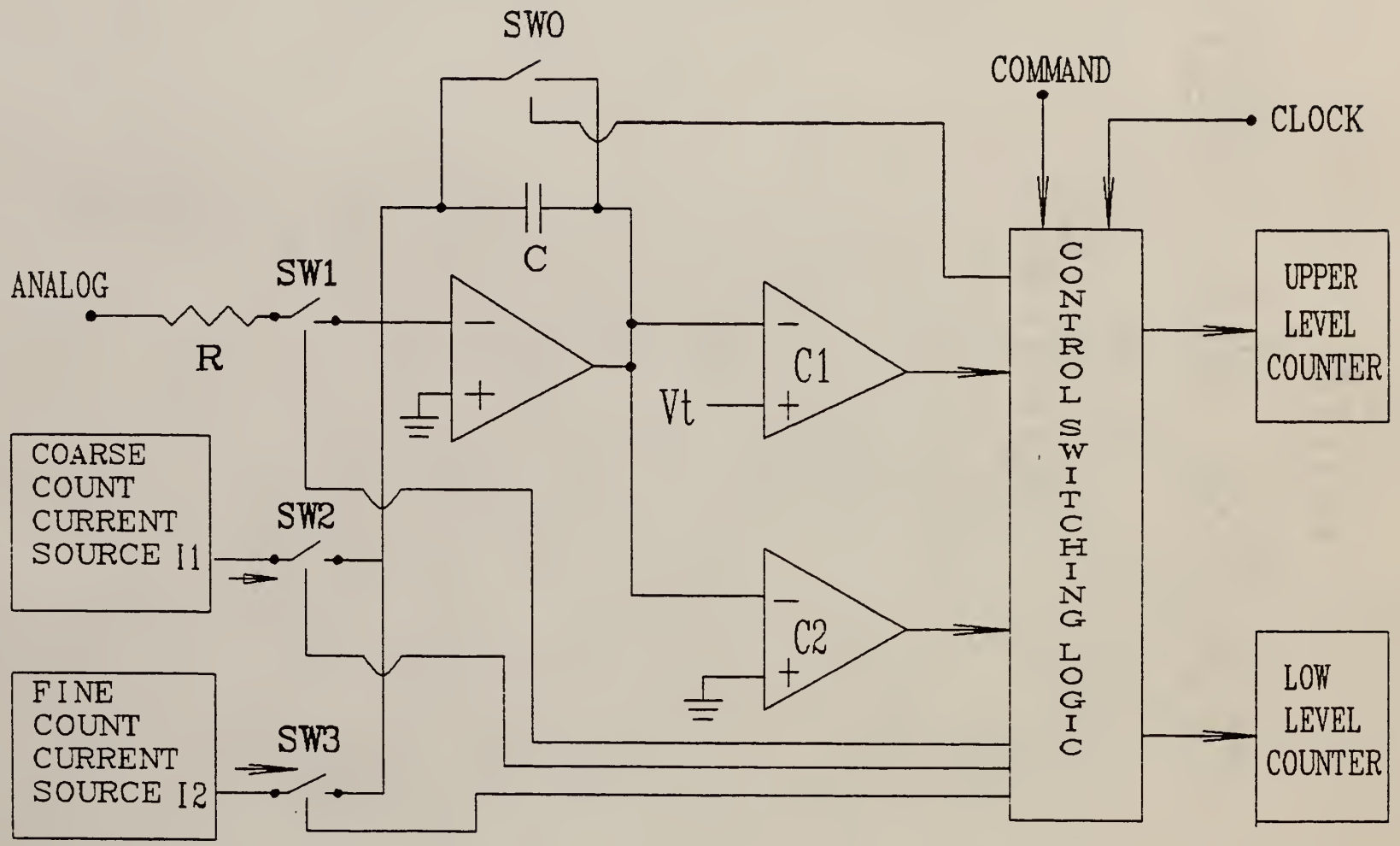


Fig.8. Circuit diagram of dual-rate integrating ADC.

2.1.1 Sampling of Input Voltage Amplitude of Dual Rate Integrating ADC

Initially all the switches SW0 - SW3 are opened. With the START/RESET command, switch SW0 is closed and the hold capacitor C, is zeroed to eliminate offset errors. When SW0 is opened, a sample of the preamplified analog input pulse is ready. With the closing of SW1, the analog input pulse of a certain voltage amplitude is transferred into the hold capacitor C by the integration process as shown in Figure 9. A sample-hold circuit can also replace the integrator circuit. After C has been charged up during a fixed sampling period, the maximum voltage on C is proportional to the sampled analog input pulse voltage amplitude.

The maximum voltage on C can also have a reverse polarity to the analog input voltage amplitude, depending on the summing and amplification logic circuit used before the sample-hold circuit. The utilisation of the summing and amplification circuit however does not alter the input voltage amplitude information because of the proportional relationship of the capacitor maximum voltage (the amount of charge stored in C) to the input pulse voltage amplitude. The input pulse voltage amplitude information is thus stored in C for as long as all the switches are opened, assuming negligible current leakages of the switches in the 'off' state and a low dielectric absorption

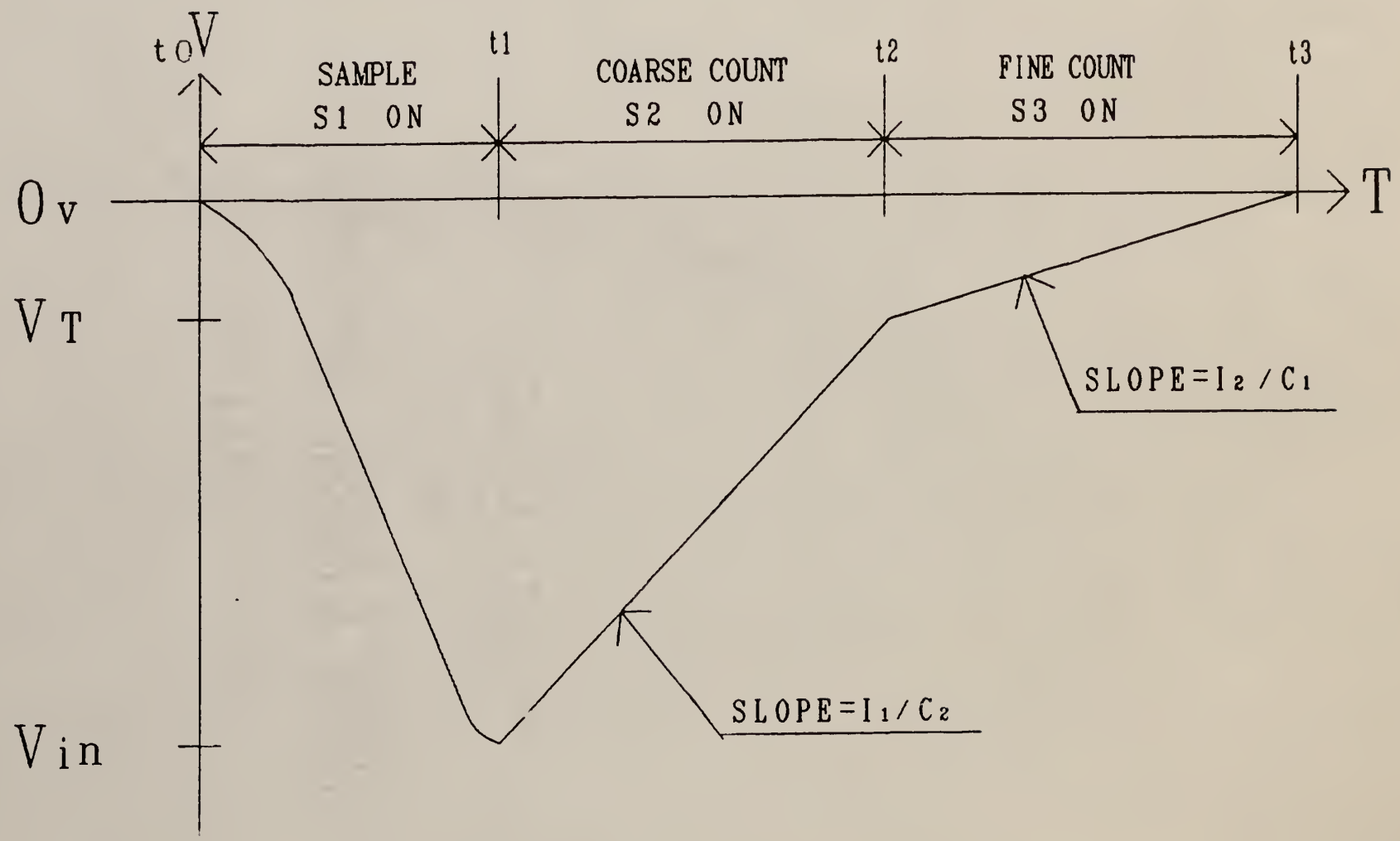


Fig.9. Dual-rate integrating ADC conversion.

capacitor. This helps to stabilise the input pulse amplitude information when conversion takes place later.

2.1.2 Analog-to-Digital Conversion of Dual-Rate Integrating ADC

The conversion of the analog input to digital form takes place when switch SW1 is opened and SW2 is closed. SW2 provides a larger current I1 flow to C than when SW3 is closed. This current allows a faster discharge of the capacitor inorder to speed up the conversion. Since the rate of change of voltage across the capacitor is proportional to the current through the capacitor if the capacitor is fixed. As C discharges, the voltage drop across C is compared to the threshold voltage Vt of the first comparator C1. As long as C voltage is less than that of Vt, the output voltage from C1 enables the upper level counter to count. When C voltage exceeds Vt, the upper level counter stops counting and the control logic causes SW2 to open and SW3 to close simultaneously if high accuracy counting is required. The closing of SW3 allows a smaller current I2 to discharge C. This means conversion occur at slower rate inorder to maintain accuracy for low order bits where noise becomes significant compared to the input voltage level. The discharge of C proceeds and the voltage across C is compared with that of the second comparator C2. The low level counter is enabled until C is completely discharged to zero threshold voltage. SW3

then opens and SW0 closes to zero the capacitor and the sample and conversion cycle is repeated.

2.2 Concepts of Dual-Rate Integrating Techniques

2.2.1 Sampling Theory of Dual-Rate Integrating ADC Techniques

Figure 9 shows graphically the analog input pulse amplitude to digital conversion. During the time interval (t1 - t0), the input pulse is sampled by the integrator. For a positive amplitude input pulse, output voltage of the integrator Vo will have negative polarity.

$$Vo = - (1 / (R * C)) * \int Vin\ dt$$ (assuming switch SW1 'on' resistance is negligible)

$$dVo / dt = - Vin / (R * C)$$

The rate of sampling depends on the size of the values of R and C. If smaller values of R and/or C are used, obviously the rate of sampling of the input pulse increases. If the time interval (t1 - t0) is made equal to 16-2/3 msec (when operating on 60 Hz power lines), integration of the input pulse occurs for exactly one cycle of the power-line frequency, giving a good rejection of power-line interference. This, however, restricts the speed of conversion of the input pulse. If faster sampling of the input pulse is required, good shielding and

filtering can be used to reduce the noise effect from external sources.

2.2.2 Conversion Theory of Dual-Rate Integrating Techniques

From Figure 9, because Vo has negative polarity, the capacitor C is said to be charged up negatively during the time interval (t1 - t0). During the time interval (t2 - t1), when switch SW2 is closed, C integrates with a constant current I1. If Q is the original charge stored in C at time t1, with constant current I1,

$$\Delta V = \Delta Q / C = (I * \Delta t) / C$$

$$\Delta V / \Delta t = \text{Slope 1} = I1 / C \qquad \text{.....(1)}$$

Thus the slope of integration can be kept constant if the current I1 is kept constant since C is fixed. Similarly when SW2 is closed during the time interval (t3 - t2), the slope of integration, slope 2, is kept constant with constant current I2.

$$\text{Slope 2} = I2 / C \qquad \text{.....(2)}$$

The fact that slope 1 and slope 2 are maintained constant with constant currents I1 and I2 respectively, is to obtain linear slopes for accurate coarse and fine counting of the clock pulses as the total number of clock pulses counted for the coarse and fine count is to be proportional to the input pulse amplitude.

2.2.3 Derivation of Threshold Voltage of Dual-Rate Integrating Techniques

To determine the channel number or channel address in the multi-channel analyzer for pulse-height analyses, the current ratio I1/I2 has to be equal to 2^n, where n is the lower level counter number of bits. This means

$$I1 = 2^n * I2 \qquad \text{.....(3)}$$

Also the threshold voltage Vt has to be related to the upper and lower level counter number of bits. Referring to Figure 9, if m is the number of bits of upper level counter and for 2^m clock cycles count, Vo = Vomax

$$\text{Slope 1} = (Vt - Vo) / (t2 - t1) = I1 / C \qquad \text{.....(4)}$$

$$\text{Slope 2} = (0 - Vt) / (t3 - t2) = I2 / C \qquad \text{.....(5)}$$

From (3) $I1 = 2^n * I2$

(4) div. by (5)

$$= ((Vt - Vo) * (t3 - t2)) / (- Vt * (t2 - t1))$$

$$= 2^n$$

$$(Vt - Vo) = - ((t2 - t1) * 2^n * Vt) / (t3 - t2)$$

$$Vo = Vt * (1 + ((t2 - t1) * 2^n) / (t3 - t2))$$

$$Vt = Vo / (1 + ((t2 - t1) * 2^n) / (t3 - t2)) \qquad \text{.....(6)}$$

Since the two phases are synchronized by a main counting clock, let tclk represents the counting clock period and

N1 = no. of clock pulses during time interval (t2 - t1)

N2 = no. of clock pulses during time interval (t3 - t2)

Then, (t2 - t1) = N1 * tclk

and (t3 - t2) = N2 * tclk

For Vo = Vomax, $N1 = 2^{m}$, $N2 = 2^{n}$

$$Vt = (Vomax * (2^{n} - 1)) / (2^{(m + n)} - 1)$$

$$Vt = Vomax / (1 + 2^{m}) \quad \text{if } m = n$$

With an n-bit lower level counter and a m-bit upper level counter, a total of $2^{(m + n)}$ channels for the multi-channel analyzer is possible. The channel width for the coarse count is 2^{n} times the channel width for the fine count. Therefore the address register for the coarse count advances through 2^{n} channels from one address to the subsequent address. The channel width of the multichannel analyzer for the fine count is therefore Vomax / ($2^{(m + n)}$ - 1). The multichannel analyzer channel distribution is shown in Figure 10.

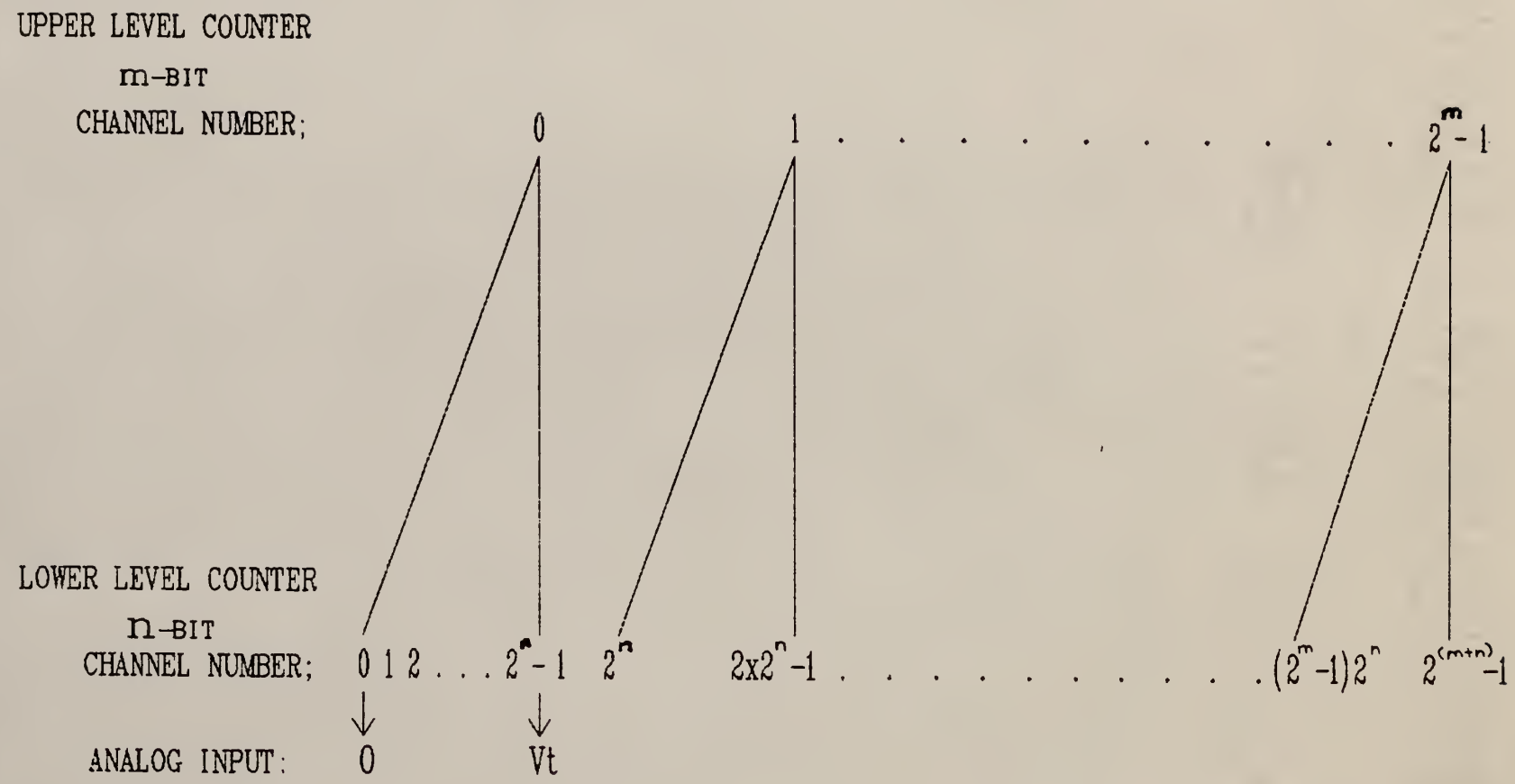


Fig.10. Multichannel-analyser channel distribution.

2.3 Error Sources of Dual-Rate Integrating Techniques

Several factors can contribute to the errors in the dual- rate integrating ADCs. These errors affect the linearity of this type of converter and hence its accuracy. However, these errors can be minimized as will be discussed in the latter part of the thesis.

2.3.1 Offset Error

This type of error is due to offsets in the input circuits, the operational amplifiers and the comparators used. The voltage droop across the hold capacitor also introduces offset error into the ADCs. This voltage droop is due to leakage current through the capacitor, the analog switches in 'off' state, the high input bias current of the operational amplifier, and the stray capacitance. The result is a relative shift in error of the input pulse amplitude by a factor of the offset value as shown in Figure 11.

2.3.2 Gain Error

Gain error occurs if the digital code output value is a scaled factor of the actual digital code output value corresponding to the input pulse amplitude. The gain error results from the error in the gain of the operational amplifier used or the error in the constant current value used to discharge the capacitor. Graphically, the gain

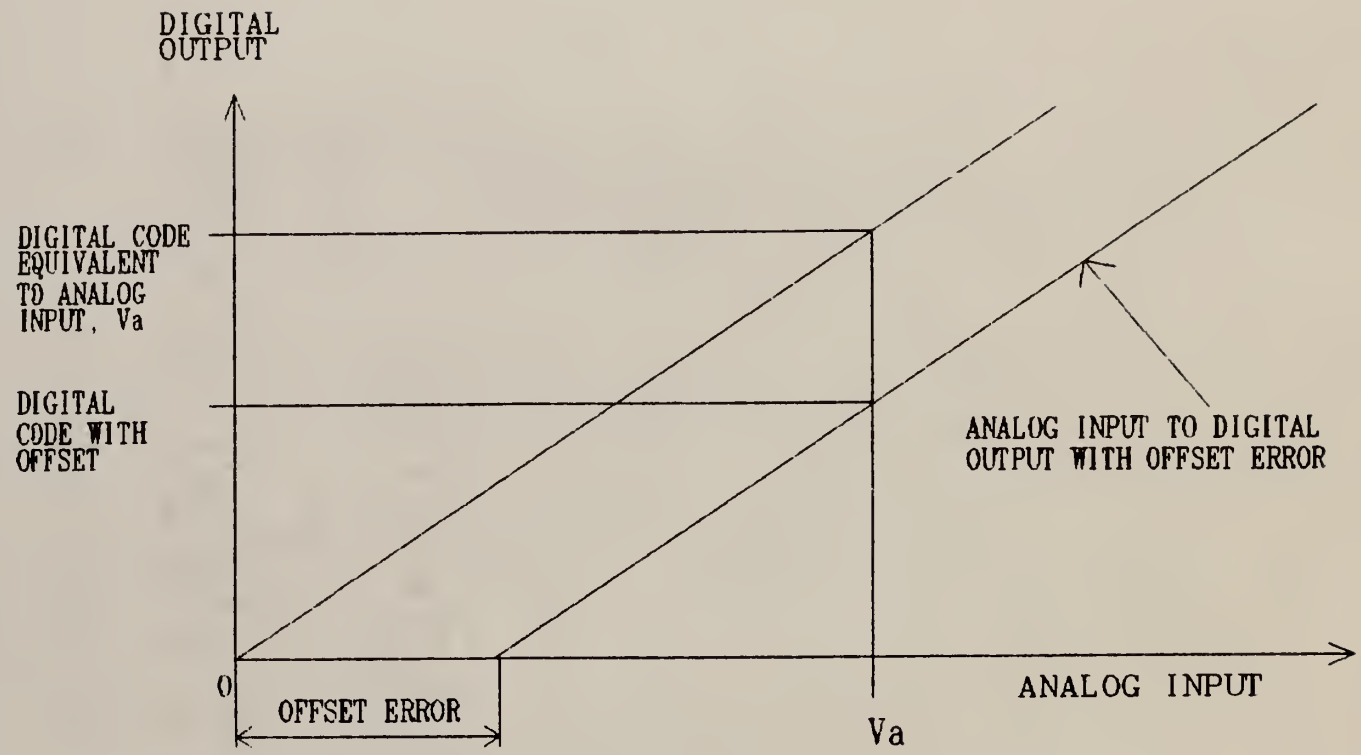


Fig.11. Dual-rate integrating ADC's error due to voltage offset.

error effect is as shown Figure 12.

2.3.3 Hold Capacitor Dielectric Absorption

Some types of capacitors have high dielectric absorption. This uses up a very small percentage of the charge in rearranging the charges within the capacitor and does not appear as a voltage drop across the capacitor. The assumption that the voltage change across the capacitor is exactly proportional to the integral of the current through the capacitor, is no longer valid. A high quality capacitor with low dielectric absorption is therefore recommended.

2.3.4 Error due to Noise

Noise is introduced into the circuit from the power supply lines, from component pick-up, from the control voltage transition spikes of the analog switches, etc. These noise sources can be classified as interference noise sources and intrinsic noise sources which includes popcorn noise, 1 / f (flicker or contact) noise, thermal (Johnson) noise, and shot noise. The noise generated causes errors in the comparators and switching logic circuit and result in coding errors.

2.3.5 Linearity Error

The linearity of the coarse-fine integrating techniques is determined by the main/counting clock jitter, and clock stability and the current ratio accuracy.

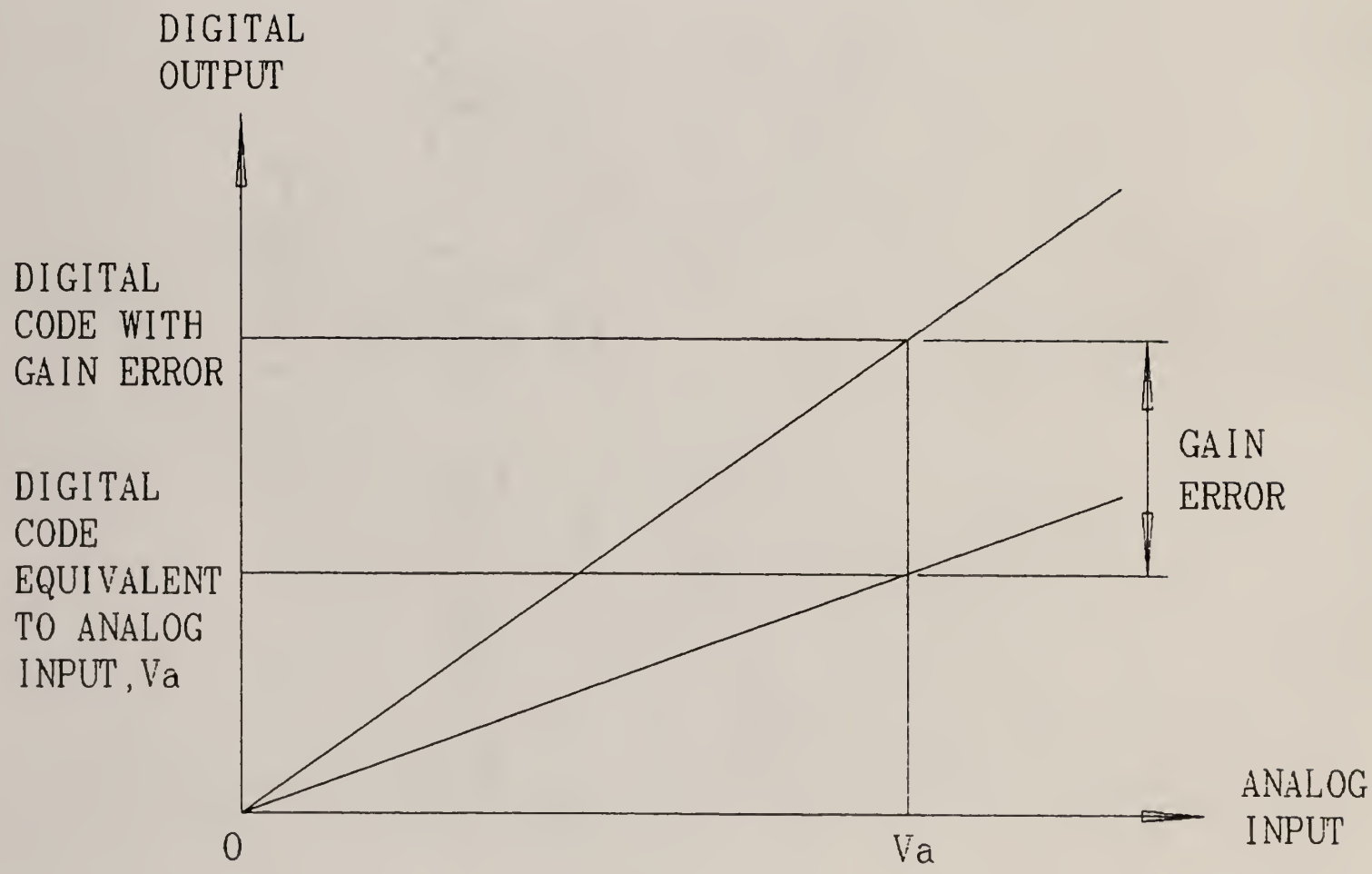


Fig.12. Dual-rate integrating ADC's error due to gain factor.

2.4 Advantages of Dual-Rate Integrating ADC

a). The dual-rate integrating ADCs are popular because they give a good differential linearity. This is possible because of the integrating behavior of this type of converters that frees the analog input function from discontinuities during conversion. Also, all codes can inherently exist since these codes are generated by a clock and a counter.

However, the successive approximation ADC has missing codes due to components mismatching in the DAC used, which is difficult to overcome. Also, the offset error in the comparator contributes to the error. The Wilkinson-type ADC has differential nonlinearity due to unbalance of the even numbered periods caused by the action of interference resulting from operation of a channel scalar as explained in section 1.1.3

b). The dual rate integrating ADCs exhibit a good noise rejection compared to the other type of ADCs eventhough complete noise rejection in not possible. Thus this type of converters are preferred in noisy environment.

c). The circuit for the integrating ADCs can be simple and require fewer components than the successive approximation ADC because no correction circuit for differential nonlinearity is required. This reduces the power dissipation of the circuit.

CHAPTER 3. DESIGN OF DUAL-RATE INTEGRATING ADC

3.1 Design Specifications

A coarse-fine integrating ADC was designed for pulse height multichannel analyzer based on the following specifications:

1. Power supplies : + 7.5V, - 7.5V, and + 5.0V
2. Input voltage range : [-5, +5] V
3. A/D conversion voltage range : [-5, 0] V
4. Resolution of 12 bits.
5. Maximum sampling rate of 10,000 samples/second.
6. Maximum integral linearity error of +/- 1 LSB

3.2 Use of CMOS Integrated Circuits

CMOS logic levels and integrated circuits are used in the circuit development in order to achieve low-power dissipation. Besides, CMOS integrated circuits generate fewer and lower voltage spikes during voltage transitions and therefore reduce the noise due to voltage transitions.

3.3 Basic Circuit Parts of Design

The dual-rate integrating ADC developed consists essentially of the following basic parts as shown in the block diagram (Figure 7).

The five basic parts of the dual rate integrating ADC designed are:

1. Sample-hold circuit
2. Two current sources
3. Two comparators
4. Counting clock
5. Switching control logic

An electronic circuit analysis program named MICRO-CAP was used to aid in the analyses and design of the dual-rate integrating ADC.

3.3.1 Sample-hold Circuit Design

The sample-hold circuit is shown in Figure 13. A positive or a negative input voltage pulse, Vin, of amplitude between -5V to +5V is converted by the summing inverting amplifier using the operational amplifier OPAMP1 to obtain an amplitude voltage Vo of range -5V to 0V according to the following equation.

$$Vo = -(Vin + Vref) / 2 \quad \text{where } Vref = +5V \quad \ldots\ldots\ldots(8)$$

Graphically, the theoretical transfer function of the summing inverting amplifier is as shown in Figure 14.

OPAMP1 is a high input impedance and low output impedance amplifier. This is necessary to prevent the circuit from loading the source and to be able to drive the output load. To realise equation (8) above for Vo, the

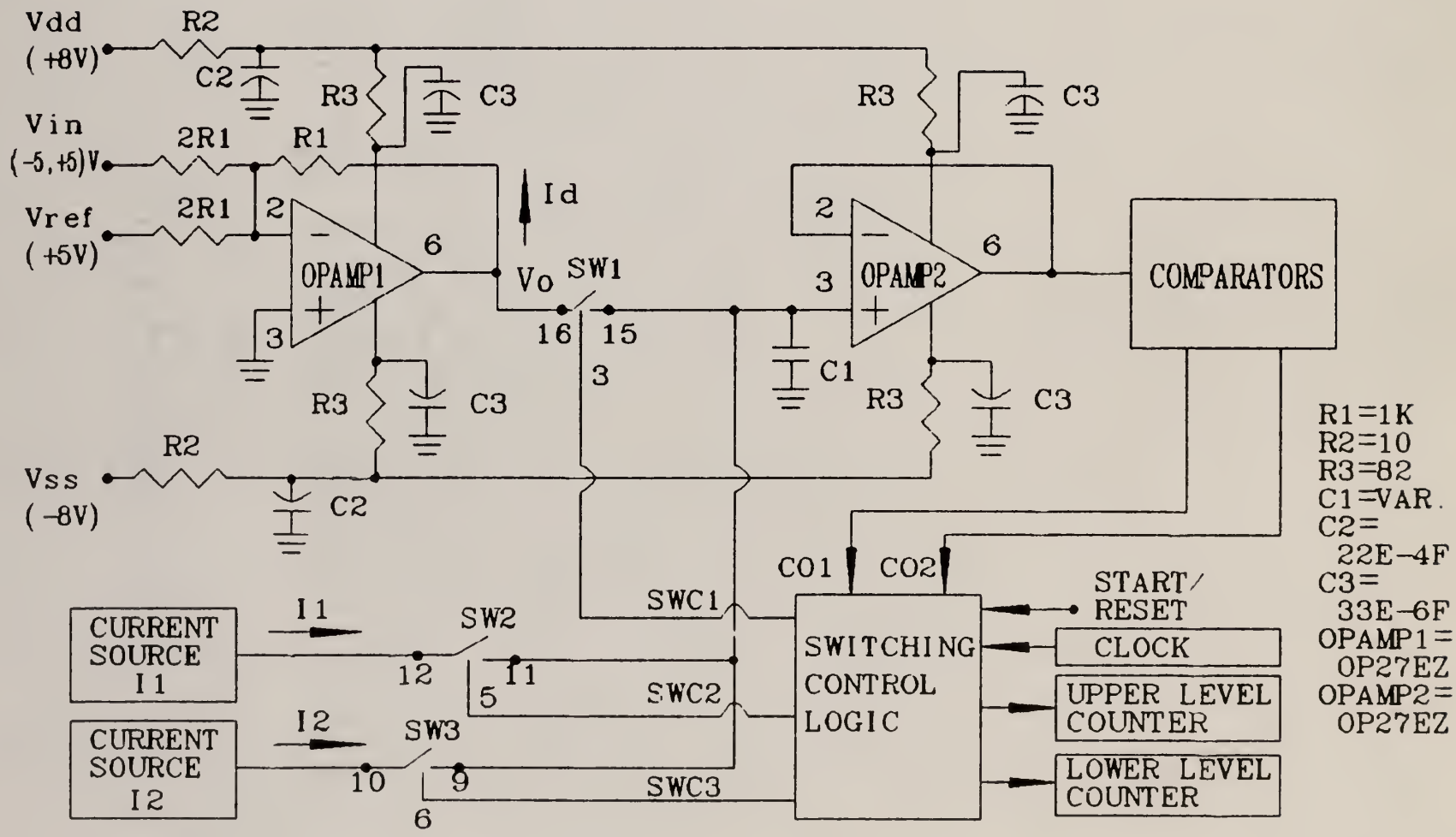


Fig.13. Sample-hold circuit part of dual-rate integrating ADC.

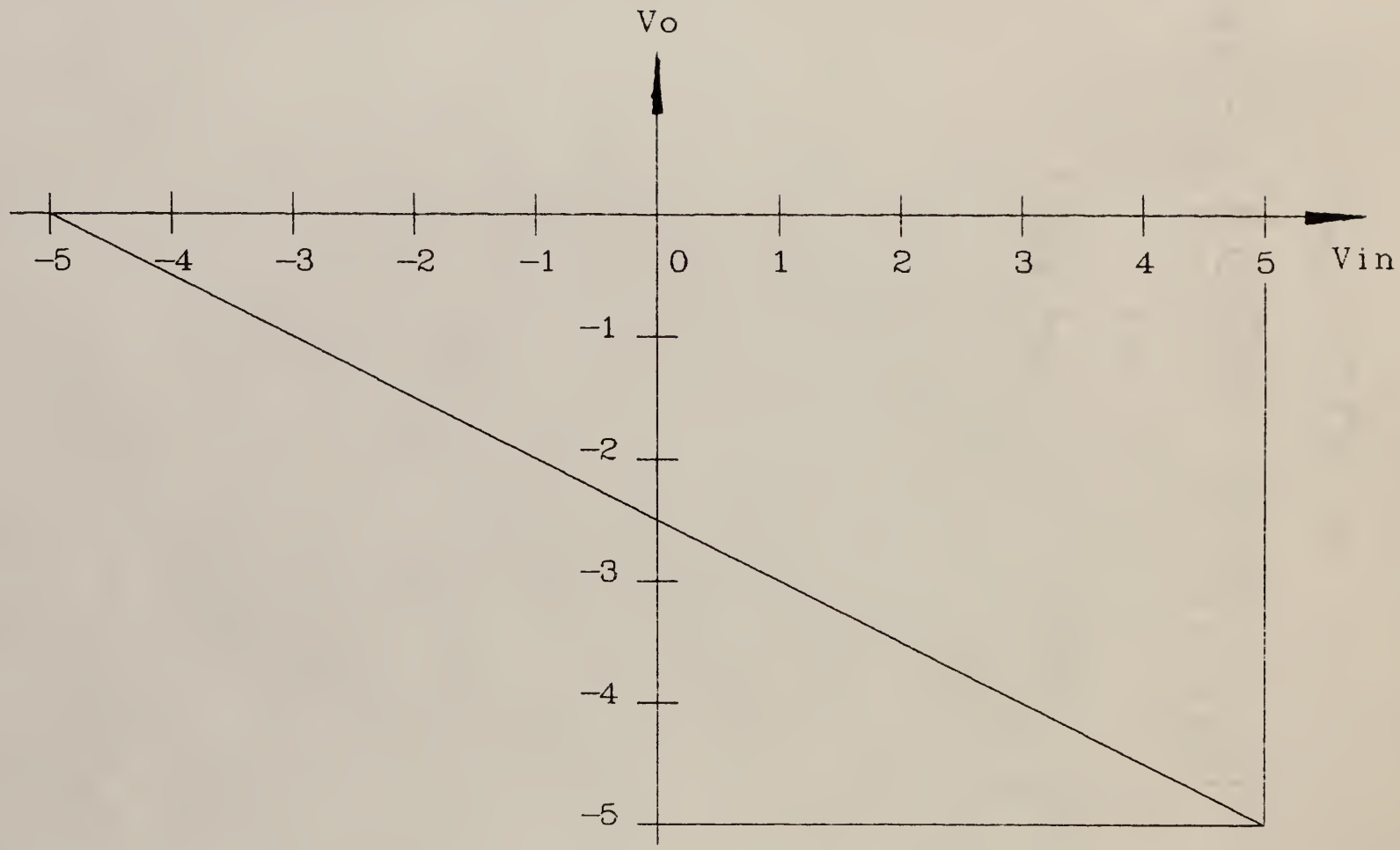


Fig.14. Transfer function of the summing inverting amplifier.

resistors value R1, and 2R1, should match. Vref should be stable at 5V and OPAMP1 should have a low input offset voltage (OPAMP1 with negligible offset is picked). The testing of the voltage offset of the operation amplifier is given in Appendix A.

With the closing of switch SW1, voltage Vo is transferred into the hold capacitor C1. The hold capacitor used is a high quality type (teflon) with low leakage current and low dielectric absorption.

Derivation of Sampling Transient Voltage of Sample-hold Circuit

By analyzing the sampling circuit shown in Figure 15, the sampling rate can be determined.

$$Vo = - (Vin + Vref) / 2 \qquad \text{from equation (8)}$$

$$Ic = C1 * (dVo' / dt) = (Vo - Vo') / Ron$$

$$\int dVo' / (Vo - Vo') = \int dt / (Ron * C1)$$

$$\ln (Vo - Vo') = - t / (Ron * C1) + K \qquad \text{where K is a constant}$$

$$Vo - Vo' = e^{-(t / (Ron * C1) + K)}$$

$$Vo' = Vo + A * e^{-(t/(Ron * C1))} \qquad \text{where A is a constant}$$

Assuming Vo' = 0 at t = 0, A = - Vo

$$Vo' = Vo * (1 - e^{-(t/(Ron * C1))})$$

$$= -((Vin + Vref) / 2) * (1 - e^{-(t/(Ron * C1))}) \quad \text{.....(9)}$$

The time t = 5 * Ron * C1 is the time required to reach 1% of the final voltage across C1. Since Ron depends on the analog switch turn-on resistance and is more or less constant for a CMOS analog switch, Vo' reaches its final value Vo faster if C1 is reduced. Figures 16 shows that by reducing the hold capacitor C1 value, the sampling rate increases. The sampling rate of the input voltage pulse therefore depends on the switch turn-on resistance Ron and the size of the capacitor. Obviously the sampling time decreases with the decrease in Ron and capacitor C1 value.

Voltage Follower of Sample-hold Circuit

Operational amplifier OPAMP2 serves as a voltage follower with high input impedance, low input bias current, low offset voltage and low output impedance. The high input impedance prevents the loading of the input circuit and together with the low input bias current prevents leakage current through the capacitor. The low input voltage offset of OPAMP2 is necessary to maintain accuracy of the circuit. The low output impedance of OPAMP2 allows the input circuit to drive the next stage circuit which consists of two comparators which have high input impedance. Therefore, a junction-FET input stage operational amplifiers are preferred.

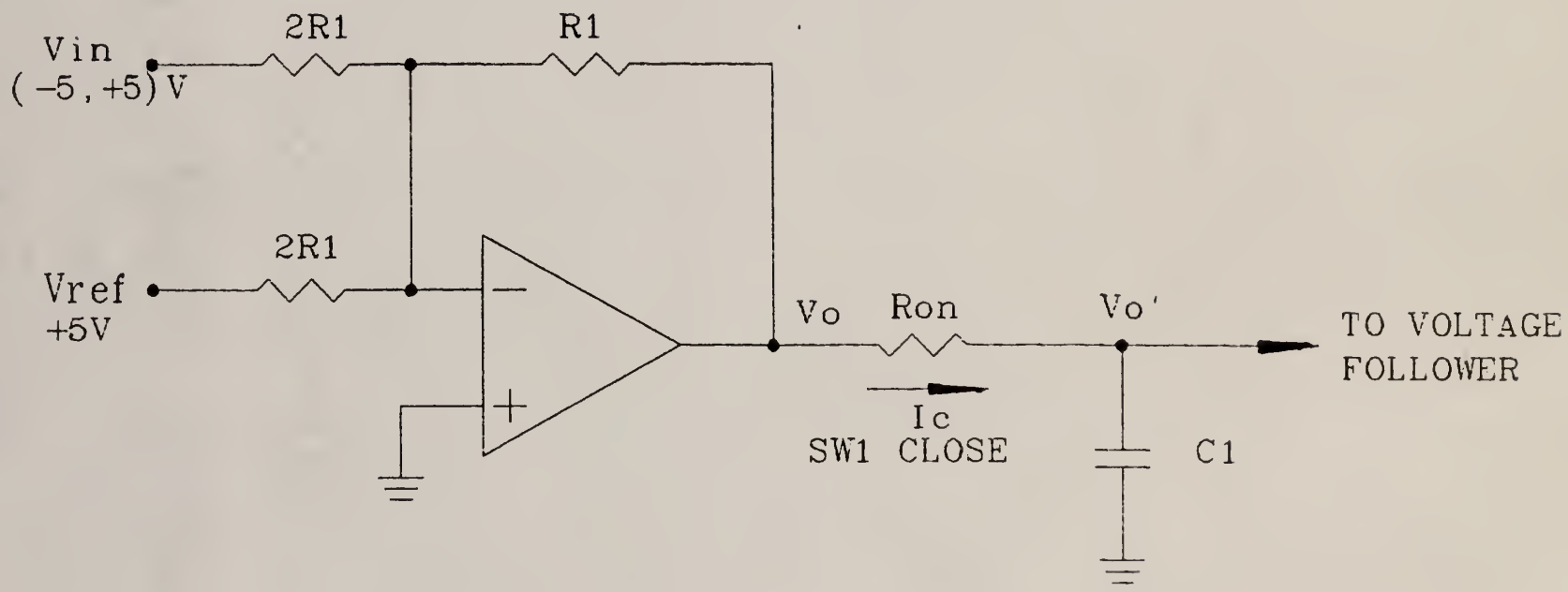


Fig.15. Sampling circuit using the summing inverting amplifier.

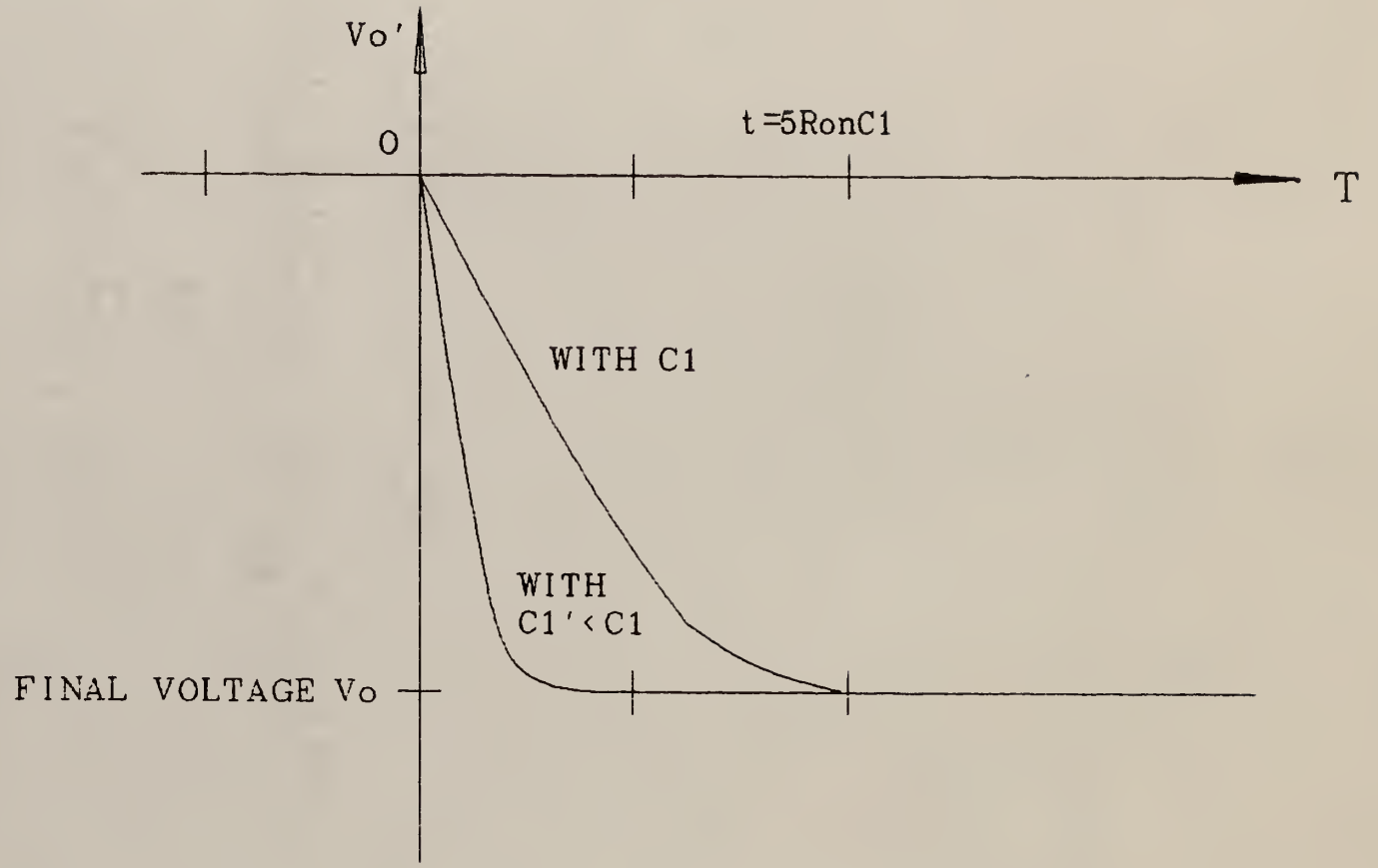


Fig.16. The effect of reducing hold capacitor C1 on the sampling rate.

Sources of Leakage Current of Sample-hold Circuit

Capacitor C1 is in hold mode when all the switches SW1, SW2 and SW3 are opened. During hold mode, leakage current through the capacitor is a major source of error. The sources of leakage current including the ones mentioned earlier are:

1). Leakage current through the capacitor C1 itself due to poor quality capacitor,
2). Leakage current through the operational amplifiers,
3). Leakage current through the analog switches in the switches 'off' states.

Advantages of Using CMOS Switches

CMOS analog switches having low turn-on and turn-off time, low current leakages, high 'off' resistance and low 'on' resistance are used for the following reasons.

1). Low power consumption,
2). Constant "on" resistance avoids signal distortion (See Appendix B),
3). Ability to switch signals that go nearly to the supply voltages,
4). Relatively low capacitive signal feedthrough because the charge contributions of the CMOS tend to cancel out.

3.3.2 Current Sources Design

The current sources (refer to Figure 17) used are the bidirectional Howland current pumps. These current sources are used because of their simple circuits, their easy application, and their capability to provide constant currents for larger output load. A theoretical description of the circuits is given elsewhere[11],[12]. The output current Iout of each current source is related by the following equations.

$$I_{out} = ((V2 - V1) * R5) / (R8 * R4) \quad mA \qquad .....(10)$$

$$\text{with } R4 / R6 = R5 / (R7 + R8) \qquad .....(11)$$

For V1 equals to ground voltage,

$$I_{out} = (V2 * R5) / (R8 * R4) \quad mA$$

$$= (V2 * 10K) / (0.1K * 100K) \quad mA$$

$$= V2 \quad mA \qquad .....(12)$$

Therefore by supplying a positive voltage V2 and by varying V2, a constant current Iout of desired value can be easily obtained.

A buffer at the input V2 is used to improve the current constancy and to prevent source loading. Two such current sources are used to supply two constant currents I1 and I2 to discharge the capacitor C1. Current I1 which has a larger value is supplied to C1 when switch SW2 is closed. This linearly discharges the capacitor at a faster rate and provides the coarse count. SW2 closes until the capacitor

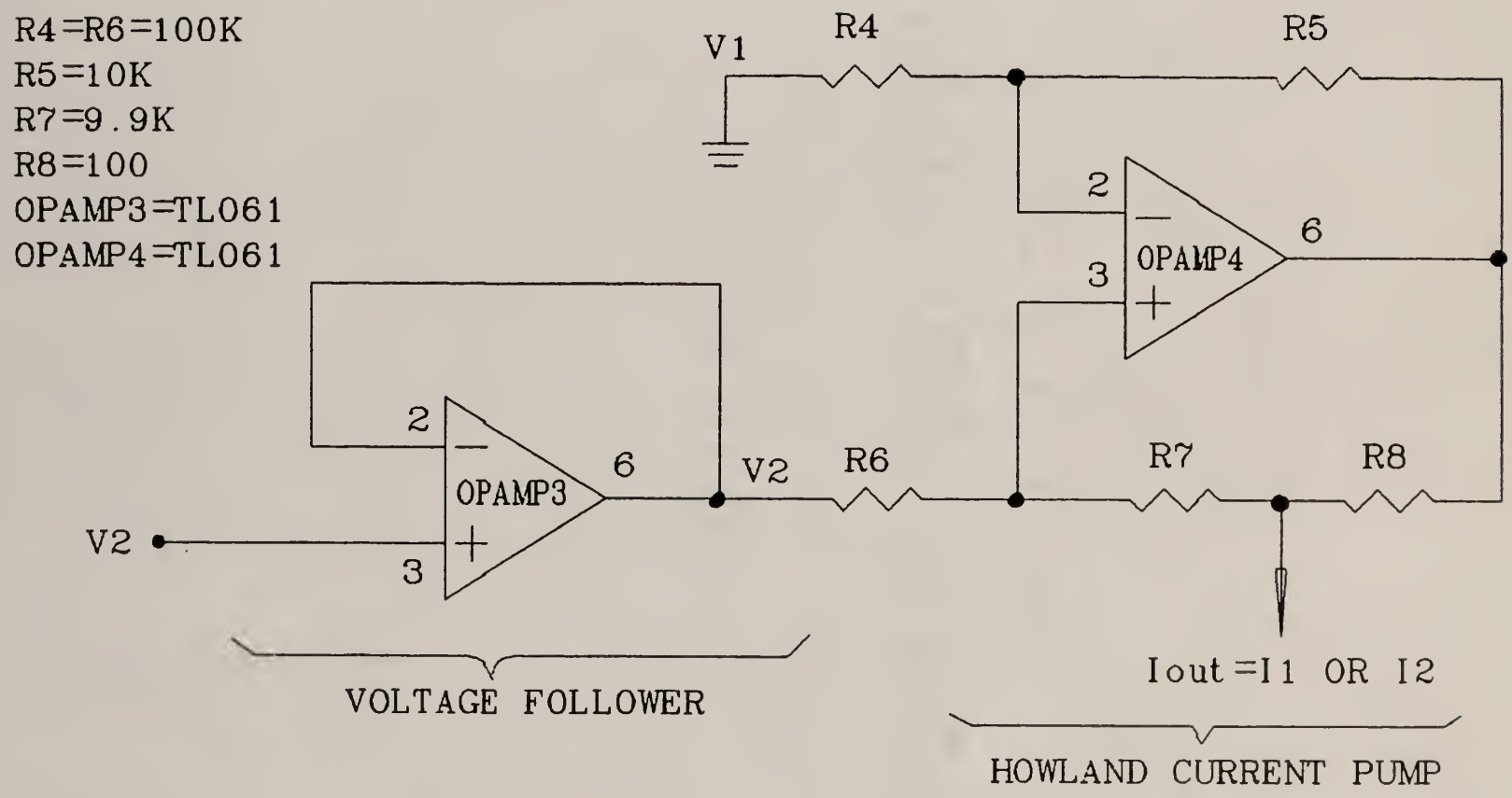


Fig.17. Howland current pump circuit schematic.

C1 discharges to the threshold voltage Vt, and then SW3 closes. This allows constant current I2 of smaller value to discharge C1 linearly until zero voltage and this provides a fine count. The ratio of I1 to I2 is equals to the number of bits for fine count. The ADC output for any Vin > Vt is as shown in Figure 9.

MICRO-CAP Analysis of Current Source

A MICRO-CAP analysis of the current source with an input voltage V2 of 5.16V and a capacitive load, C_L = 0.382E-6 F is shown in Figures 18a, 18b and 18c. The input voltage V2 is given by node 3, i.e. V_{N3} in Figure 18b. The output current, Iout is the sum of the currents flowing into node 4 from node 2 (i.e. $I_{N2/4}$) and node 5 (i.e. $I_{N5/4}$) as shown in Figure 18c. Iout = (0.05 + 5.167) mA = 5.12 mA. This agrees closely with equation (12).

Further MICRO-CAP analysis of the current source with the same input voltage but with a resistive load of R_L = 1K shows that the transient response of the current exhibits an overdamped characteristic with a slower settling time (Figure 19c) whereas with the capacitive load C_L = 0.382E-6 F, the transient response of the current exhibits an underdamped characteristic with a faster settling time (Figure 18c). Therefore this current source circuit is possibly suitable for the sample-hold circuit with a capacitive load.

a).

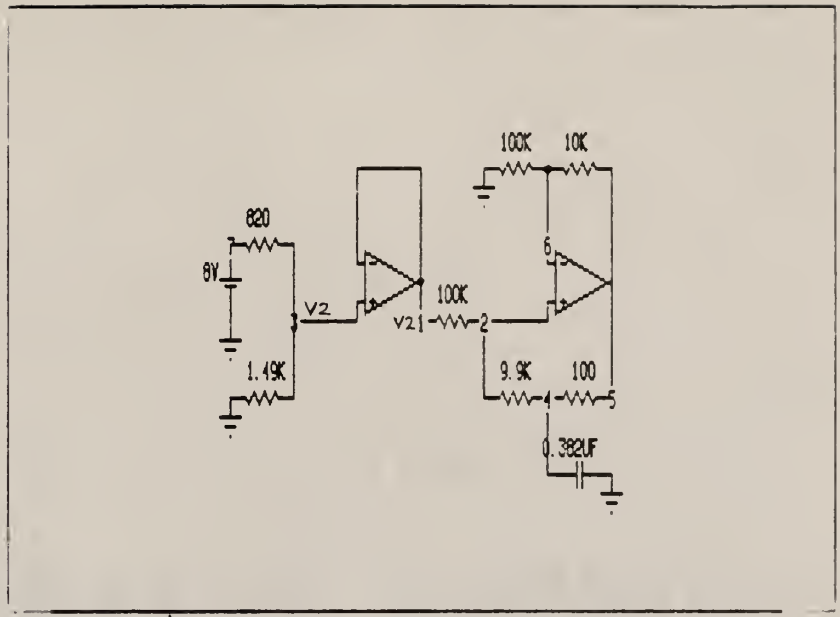


Fig.18a). Howland current source with C load.

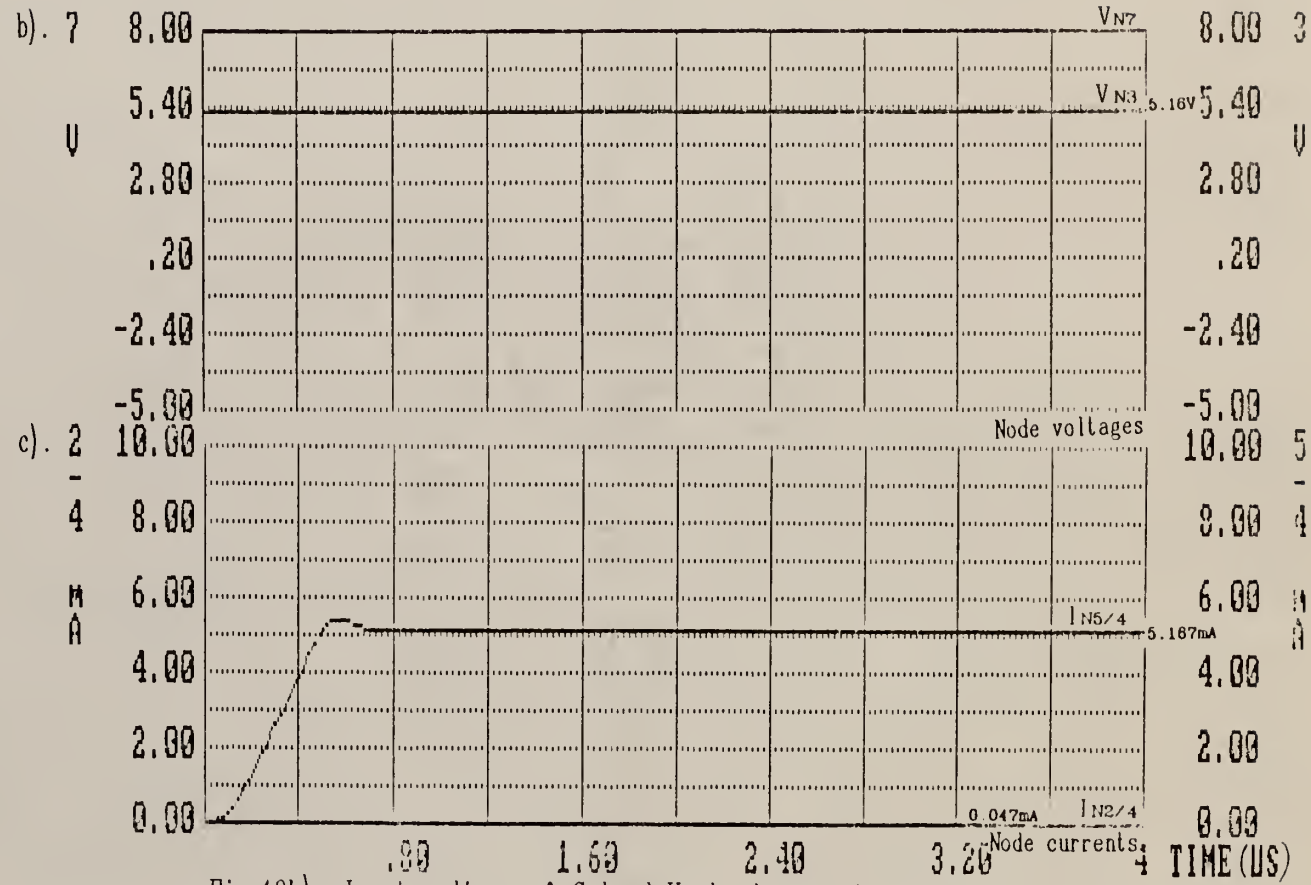


Fig.18b). Input voltage of C load Howland current source.

Fig.18c). Output current waveform of Howland current source.

a).

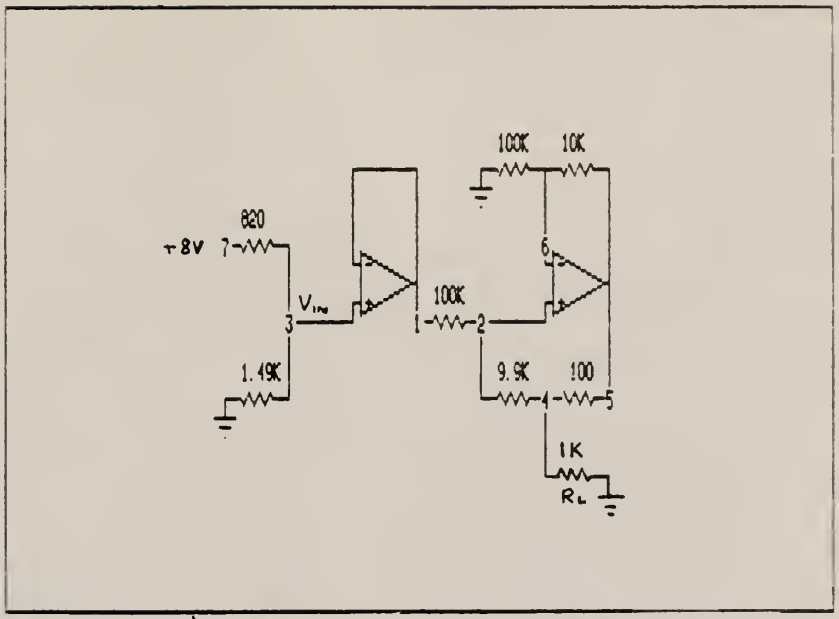


Fig.19a). Howland current source with R load.

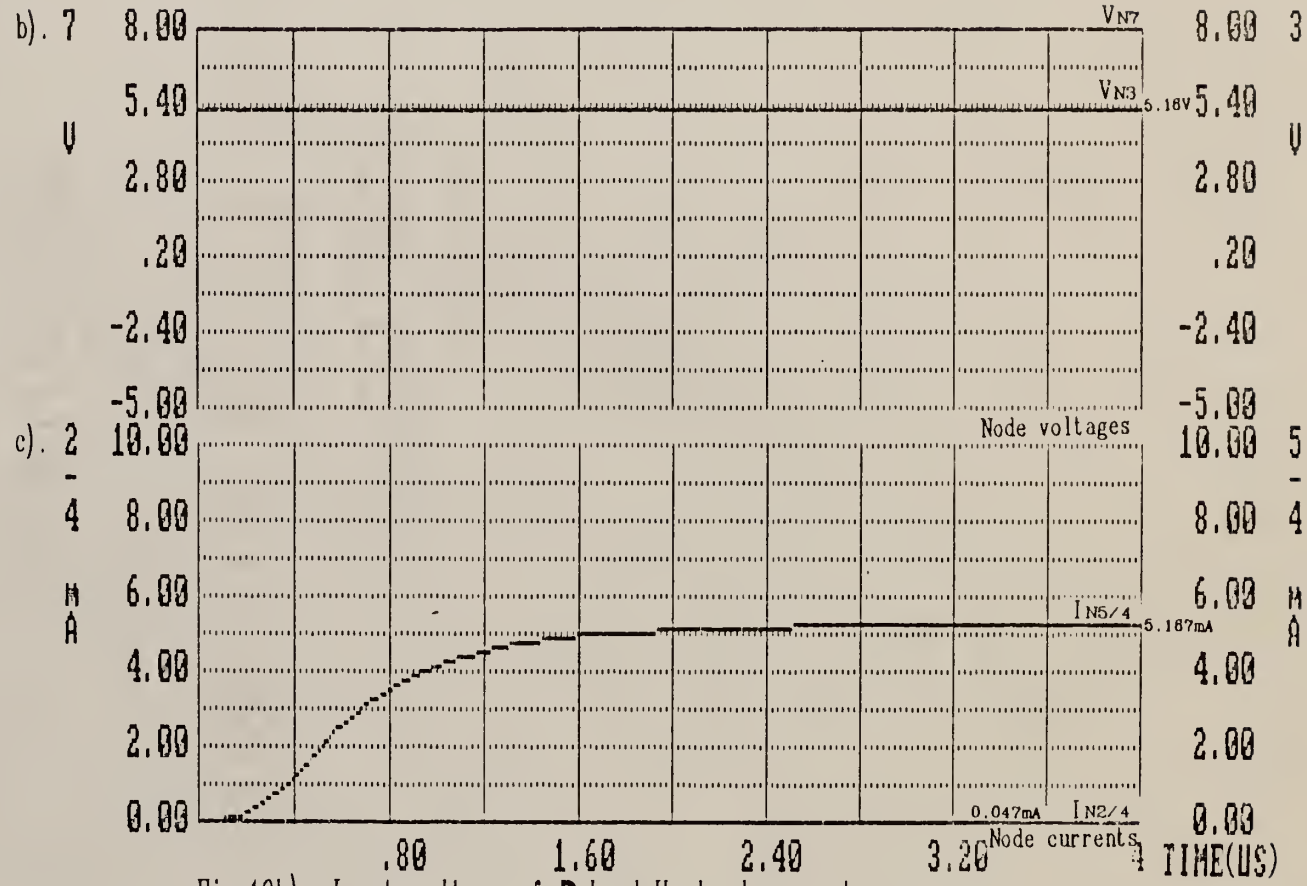
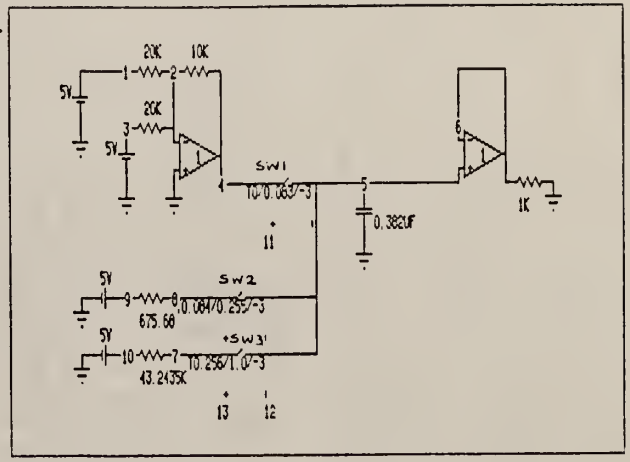


Fig.19b). Input voltage of **R** load Howland current source.

Fig.19c). Output current waveform of Howland current source.

A dual-rate integrating ADC using the simple current sources as shown in Figure 20a is analyzed using MICRO-CAP. The result in Figure 20b shows a non-linearity in the coarse count slope. A dual-rate integrating ADC using the Howland current source as shown in Figure 21a is also analyzed with the MICRO-CAP. The result as shown in Figure 21b has a linear coarse and fine slopes. However, the voltage droop effect becomes significant when switch SW1 opens and SW2 closes. This is due to the parameter values.

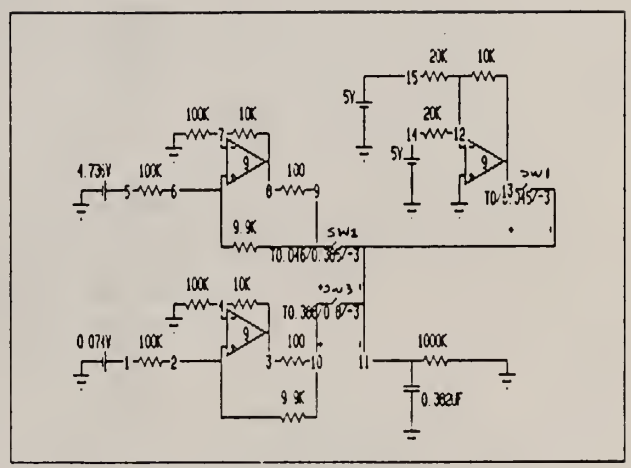
a).



b).6

Fig. 20a) Dual rate integrating ADC with volt-res. current sources
Fig.20b) MICRO-CAP analysis of Fig.20a.

a).



b).

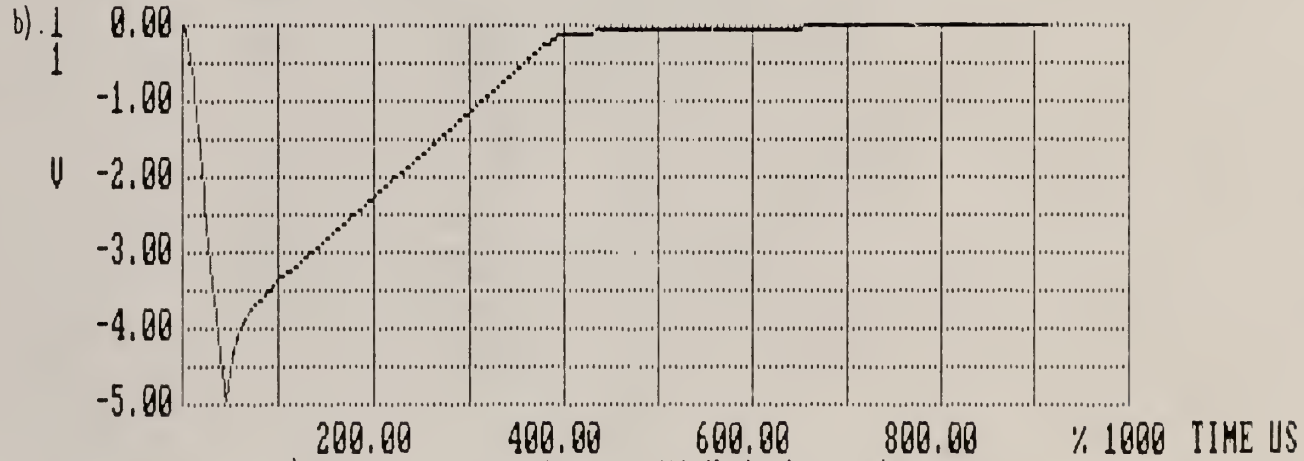


Fig. 21a) Dual rate integrating ADC with Howland current sources.
Fig.21b) MICRO-CAP analysis of Fig.21a.

3.3.3 Comparators Design

The comparators play an important role in the ADC. It is where the analog input signal is converted into the digital form . Therefore its proper operation is of major importance. In this dual-rate integrating ADC, analog to digital conversion occurs at two rates using two comparators. The circuit schematic for the comparators is shown in Figure 22.

Reducing Noise Effect in Comparators

Noise pick-up and instability of input voltages are the major causes of error in the comparators output. To overcome these problems, the positive and negative power supplies leads close to the comparators as well as the sample-hold operational amplifiers are by-passed with capacitors to filter out the noise. Stable Vt voltage for the threshold voltage of one comparator is ensured.

If the input to the comparator is noisy, the output may make several transitions as the input passes through the trigger point. Besides bypassing the power supplies to overcome the problem, positive feedback is also used. A large resistor is placed in the positive feedback path of the comparator to create a hysteresis with a lower and upper threshold voltage. This improves the output performance of the comparator. Moreover, the hysteresis provides a rapid output transition.

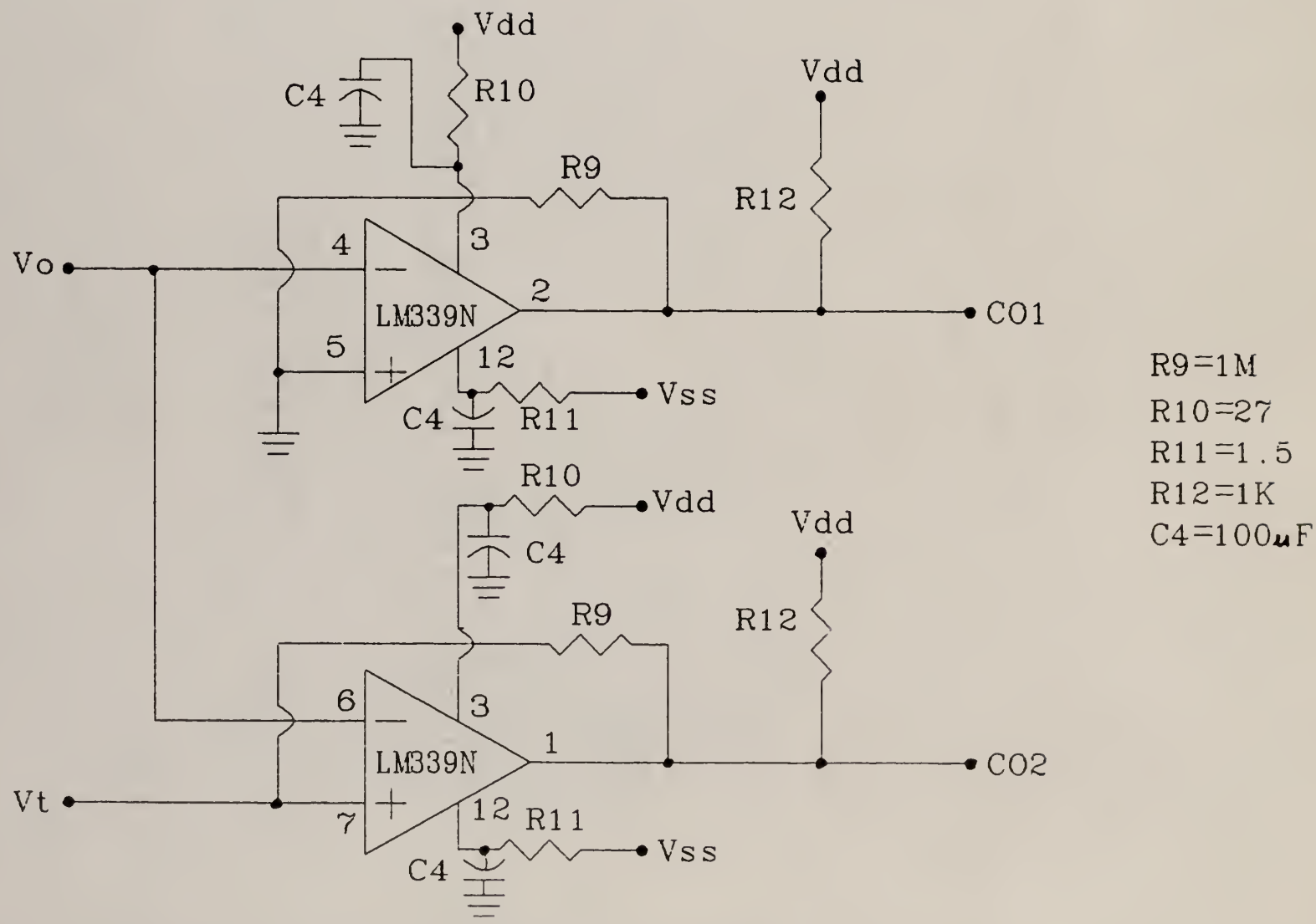


Fig.22. Circuit schematic for LM339 comparators.

Analysis of Comparators with Hysteresis

From Figure 23a, the upper and lower threshold voltage of the hysteresis is computed. For example, for a 6 bit high-order counter, the threshold voltage Vt = - 5 / 65 (from equation (7)) = - 0.07692 V. Therefore Rb = 97.0873 ohms. To determine the hysteresis upper threshold voltage Vtu, set CO2 = Vdd = + 8.0 V for Vo < Vt. Taking node voltages at pin 7, the following equation is obtained.

$$((Vtu + 8)/1E4) + (Vtu / 97.09) + ((Vtu - 8)/1E6) = 0$$

$$Vtu = - 0.07615 \quad \text{.....(13)}$$

To determine the hysteresis lower threshold voltage Vtl, set CO2 = Vss = - 8 V for Vo > Vt. Taking node voltages at pin 7, the following equation is obtained:

$$((Vtl + 8)/1E4) + (Vtl + 97.1) + (((Vtl + 8)/1E6) = 0$$

$$Vtl = - 0.0777V \quad \text{.....(14)}$$

Figures 23b and 23c show where the transitions occur for the output CO2 when a hysteresis with upper and lower thresholds is introduced. Figure 23d is a transfer function of the comparator with hysteresis.

Output Voltage Logic of Comparators

For its proper operation, a pull-up resistor is placed at the output of each comparator with the other end tied to the positive power supply. Smaller "pull-up" resistors

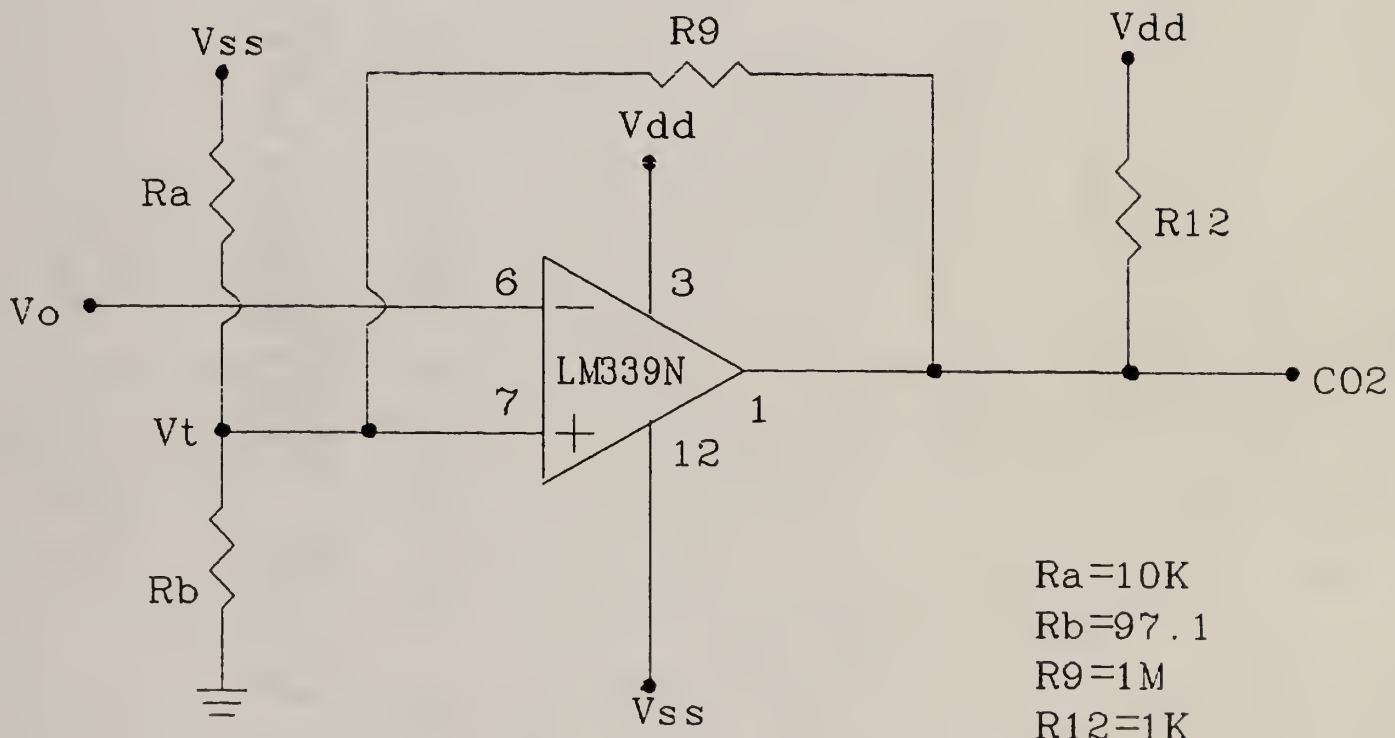


Fig.23a). A comparator with positive feedback/hysteresis.

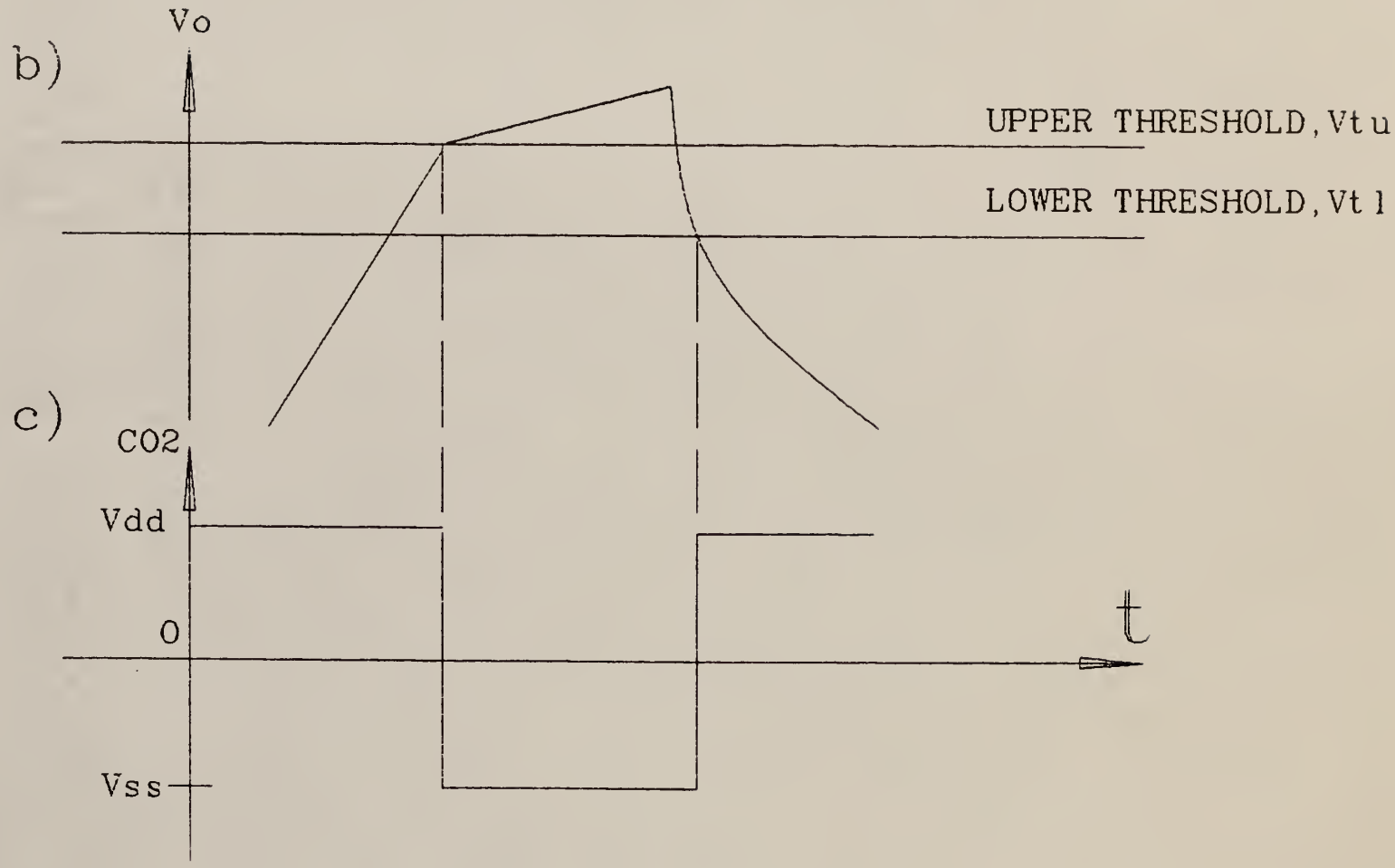


Fig.23b). Upper and lower threshold introduced with hysteresis.
c). Output of comparator showing where transistions occur.

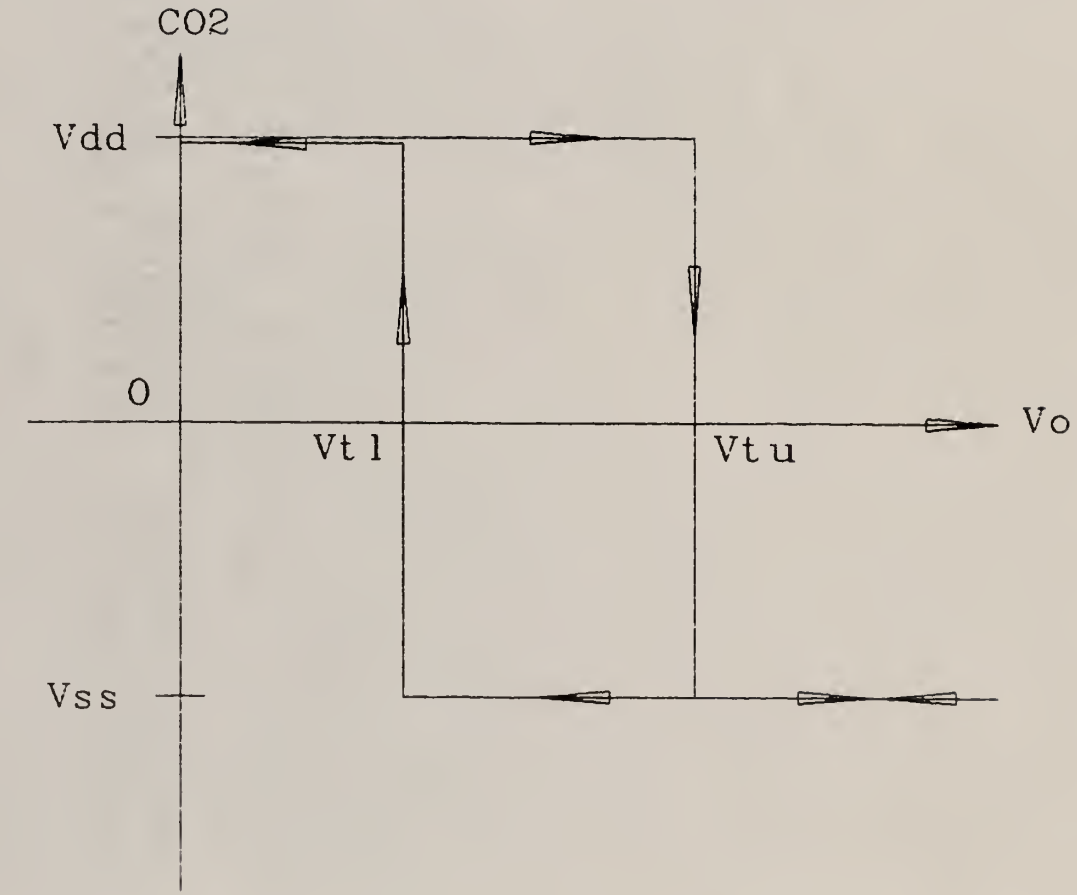


Fig.23d). Transfer function of comparator with hysteresis.

yields improved switching speed and noise immunity at the expense of increased power dissipation.

The circuit operation behaves as follows:

When Vo is less than the threshold voltage, the output of the comparator is pulled to the positive supply voltage. When Vo is greater than threshold voltage, the output of the comparator is pulled to the negative supply voltage.

3.3.4 RC Relaxation Oscillator/Clock Design

The clock used consists of a simple and cheap RC relaxation oscillator as shown in Figure 24.

This type of oscillator works as follows:

When the power is first applied, the operational amplifier output goes to say, positive saturation first. The capacitor C5 begins charging up towards the positive power supply voltage V_{dd}, with a time constant of R15 * C5. When the C5 voltage reaches one-half of V_{dd}, the operational amplifier switches into negative saturation (resembling a Schmitt trigger) and C5 begins discharging towards the negative supply voltage V_{ss} with the same time constant. The cycle repeats indefinitely with the charging and discharging of C5. This produces a square wave at the output of the operational amplifier with a period of approximately R15 * C5. With a careful design and by

selecting the values for C5 and R15, a desired, accurate and stable frequency can be obtained at the output.

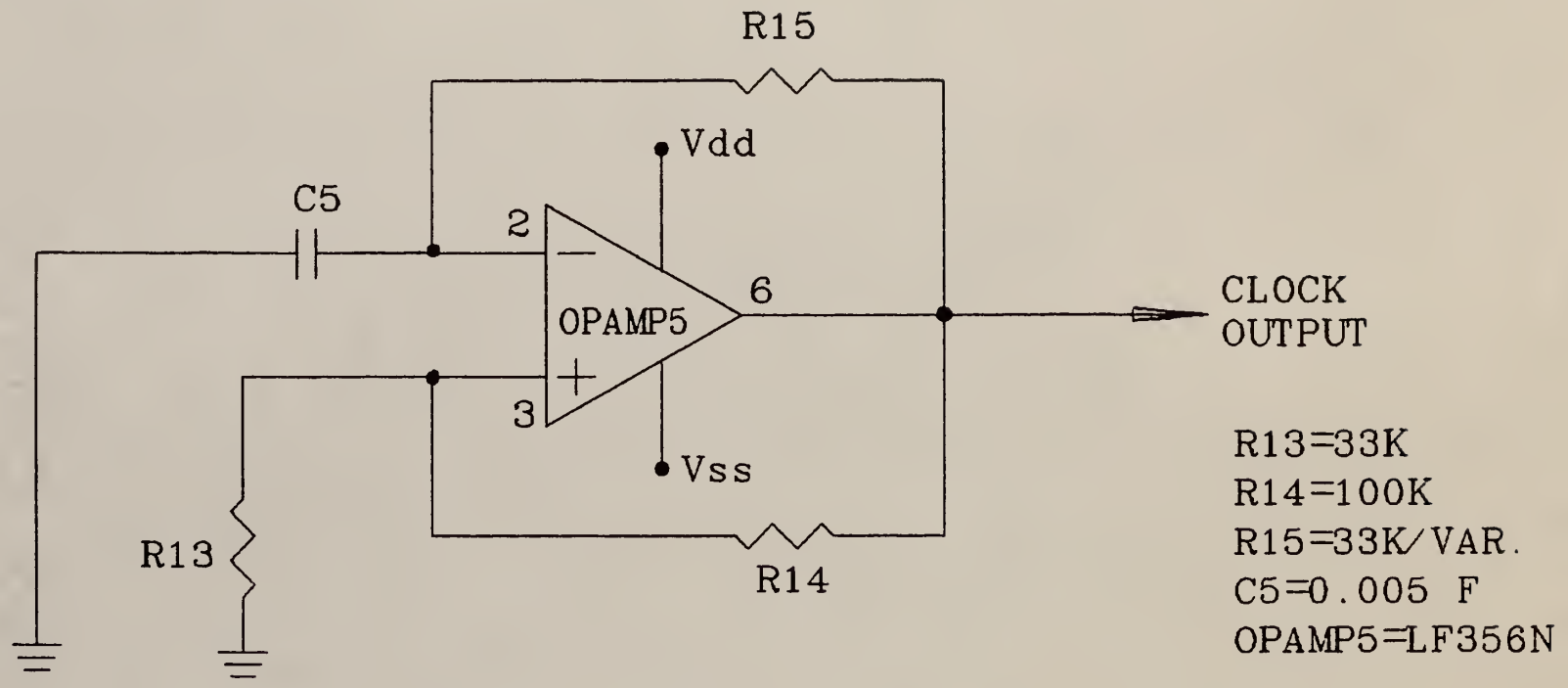


Fig.24. RC Relaxation oscillator / timer.

3.3.5 Switching Control Logic Design

The switching control logic of the dual-rate integrating ADC is shown in Figure 25. A external switch is provided for the ADC reset operation. A binary ripple counter is used to count the interval to charge up the capacitor instead of a monostable because a monostable has several disadvantages[13].

Operation of the Switching Control Logic

With the rising edge of a clock waveform at the clock input of the 1st D flip-flop, the output Q1 is set to logic 1. Q1' with a logic 0 then sets the binary ripple counter to count for a period T. During the counting period T, switch SW1 is closed and the hold capacitor is charged up. A high speed switching transistor is used to convert the CMOS logic to the TTL logic for each of the three switches turn on (logic 0) and turn off (logic 1). When the time period T is up, a pulse is present at the output of the counter. This pulse is used to reset the 1st D flip-flop to open the switch SW1.

As Q1' changes from low logic level to high logic level, a rising clock edge triggers the 2nd D flip-flop and sets the output Q2 to logic 1. Q2 is one input to the Nand gate and the output from the comparator is another input to the Nand gate. When both inputs are high, the low logic level output causes SW2 to be closed and the hold capacitor

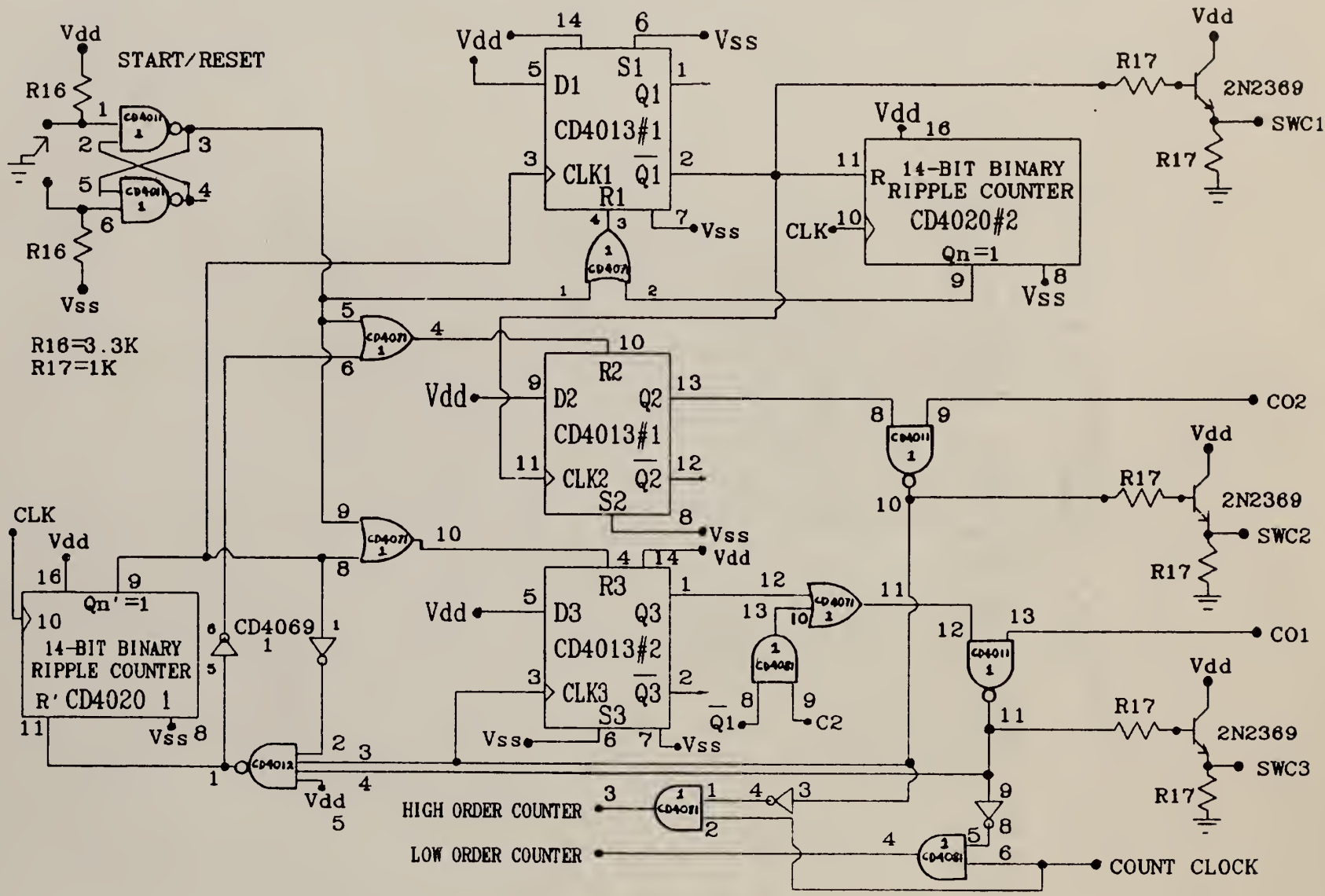


Fig.25. Switching control logic circuit

to discharge. SW2 is closed for as long as the voltage, which is across the hold capacitor, is less than the threshold voltage. As SW2 opens, a rising edge pulse triggers the third D flip-flop and sets the output Q3 to the logic 1 level. The output Q3 together with the output from the other comparator which has zero voltage threshold, go through an Nand gate. SW3 is closed for as long as the output from the Nand gate is low. When the capacitor voltage becomes zero, SW3 opens.

An Or gate is inserted between Q3 output and the input to the Nand gate. The function of this Or gate is to enable SW3 to close when the capacitor sampled voltage is less than or equals to the non-zero threshold voltage. In this case, SW2 will not be closed but only SW3.

When all the switches SW1 to SW3 are opened, all the D flip-flops will be reset. Another binary ripple counter is used to trigger a rising edge pulse to the first D flip-flop to restart the sampling and conversion cycle.

CHAPTER 4. IMPLEMENTATION AND TESTING OF DUAL RATE INTEGRATING ADC

4.1 Performance of Sample-hold Circuit

Since the sampling rate of 10,000 samples/sec is required, this means each sample requires 0.1 msec or 100E-6 seconds to be sampled, held and converted before another sample comes in. The sample-hold interval and conversion rate depends on the slew rate of the operational amplifier used. For instance, if the OP-27EZ operational amplifier with a slew rate of 2.8 V/microsecond is used, in order to slew 5 V, the minimum sample-hold interval, $T_{S\&H\ min}$ = 5 / 2.8 microseconds = 1.7857 microseconds. Usually a 2 : 1 safety factor is used, which means $T_{S\&H}$ = 3.571428 microseconds. The time left for conversion and resetting/zeroing the hold capacitor $T_{C\&R/Z}$ = 0.1 msec - 3.571428 microsecond = 96.43 microseconds.

More time can be left for conversion if the sample and hold time can be reduced. This requires using a higher slew rate operational amplifier. Usually with a faster rate of operation, the operational amplifier oscillates easily and it has to be frequency compensated.

4.1.1 Transfer Function of Sample-hold Circuit

Table 1 gives the input voltage Vin (V) and output voltage Vo (V) of the sample-hold amplifier using a hold capacitor C1 = 0.039E-6F over the input voltage Vin range [-5, +5] V.

Since operational amplifiers with very low voltage offset (data specification of 10 mV) are tested and chosen, the error due to voltage offset in the transfer function of the sample-hold circuit therefore appears exactly as in Figure 14. The output voltage therefore satisfies the equation Vo = - (Vin + Vref) / 2 : Vref = + 5V, for Vin = [-5, +5] V. This linear relationship is important if the dual rate integrating ADC high accuracy is required.

Table 1. Output voltages corresponding to input voltages* for the sample-hold circuit.

#	Input voltage amplitude Vin (V)	Output voltage Vo (V)
1.	5.00	-5.00
2.	4.01	-4.50
3.	3.01	-4.00
4.	2.01	-3.50
5.	1.01	-3.00
6.	0.00	-2.50
7.	-1.00	-2.00
8.	-2.02	-1.50
9.	-3.03	-1.00
10.	-4.00	-0.50
11.	-5.00	0.00

*experimental values

4.1.2 Effect of Hold Capacitor Size on Sampling Time and Output Performance

Table 2 shows the measured sampling time using different values of hold capacitor C1. Figure 26 shows that the sampling time increases linearly with the increase in hold capacitor value. Obviously, to reduce the sample-hold time, smaller hold capacitor is preferred.

Though smaller hold capacitor speeds up sampling, noise comes into effect and the current leakages from the capacitor become significant when the capacitor is discharged, resulting in voltage droop. This is shown in Figure 27 using C1 = 0.01E-6F. Therefore C1 should be large enough to minimise droop dVo' / dt = Ileakage / C1, and small enough if high-speed signals are to be followed accurately since the switch 'on' resistance Ron forms a low-pass filter in combination with C1.

Table 2. Sampling time of different size hold capacitor C1.*

#	Hold capacitor C1 (*E-6 F)	Sampling time tsh (*E-6 sec)
1.	0.010	5.0
2.	0.020	10.5
3.	0.039	20.0
4.	0.082	40.0
5.	0.150	70.0
6.	0.300	140.0
7.	0.382	176.0

* experimental values

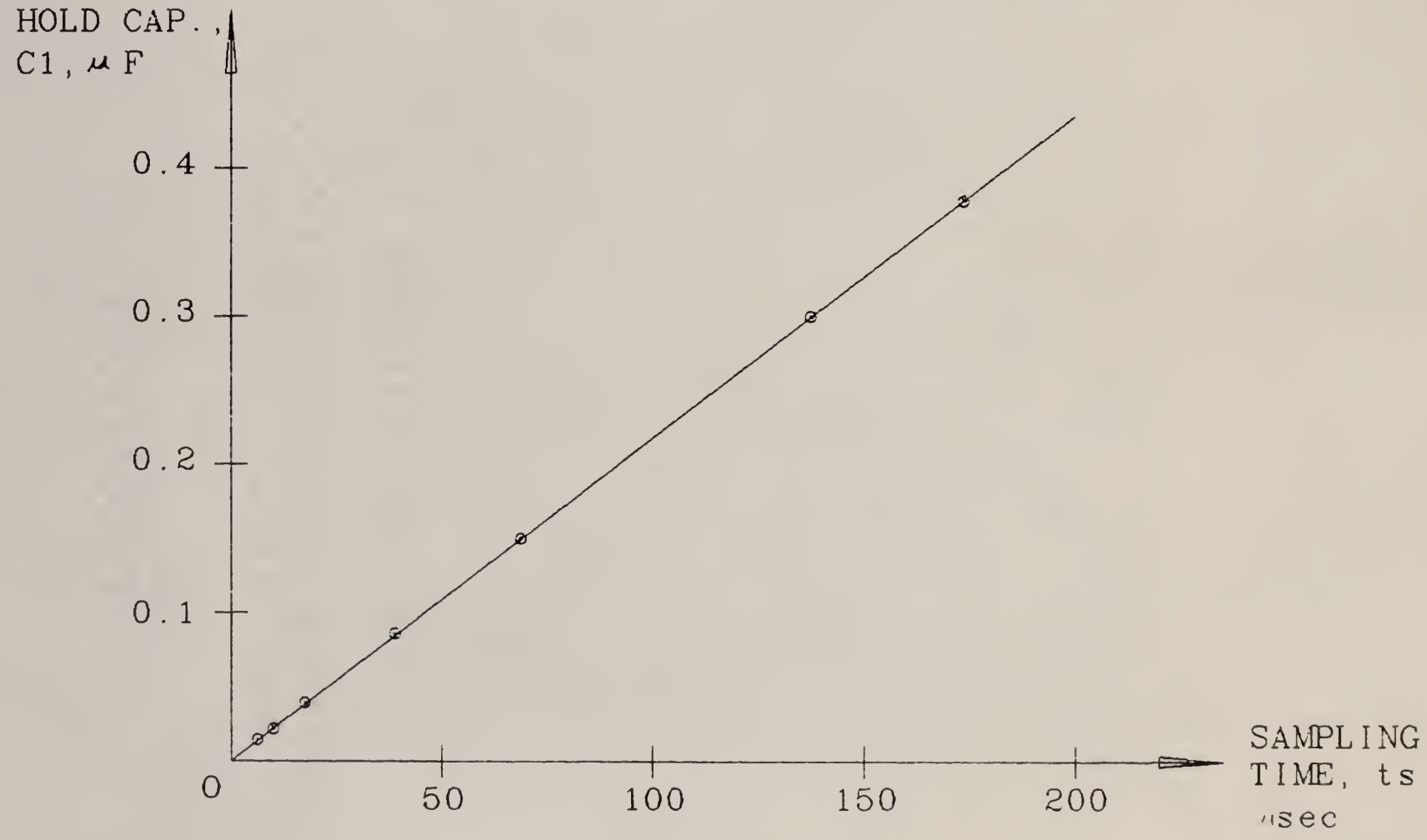


Fig.26. Hold capacitor (C1) vs. sampling time (ts)

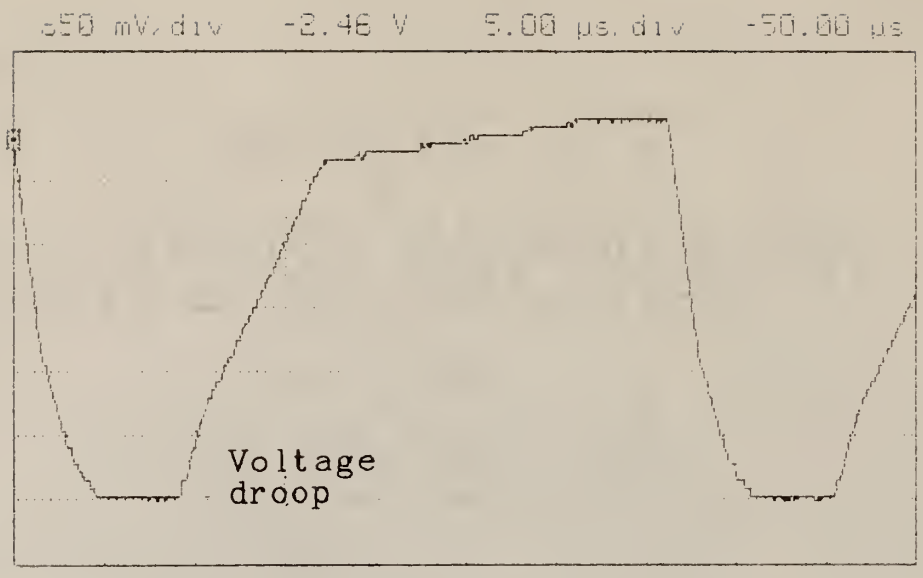


Fig.27. Voltage droop effect of dual-rate integrating ADC with small hold capacitor C1 = 0.01E-6F

4.2 Performance of Current Sources

Table 3 gives the output current Iout corresponding to the input voltage V2 with the other input voltage grounded. The maximum load resistance R_{Lmax} for less than 1 % change in the output current is also given in Table 3.

Figure 28 shows the output characteristics of the Howland current source. Graph 1 shows the linear relationship between the input voltage V2 and the output current Iout. This satisfies the equation Iout = V2 mA. Graph 2 shows that the maximum load resistance which results in approximately 1 % change in Iout increases exponentially with the decrease in Iout. This shows that for this kind of current source, a high output current will not be able to withhold its constant value for large load resistance. The reason is that the output current depends on the input voltage which is limited by the power supplies. In order to use larger output current for faster conversion rate, and to maintain its stable value, the power supplies can be increased at the expense of higher power dissipation and by reducing the size of the appropriate resistor value.

Table 3. Output current Iout and maximum load resistance Rlmax (for 1% change in Iout) corresponding to the input voltage V2 for Howland current source.

#	Input voltage V2 (V)	Iout (mA)	1% change in Iout (mA)	Rlmax (kohm)
1.	6.00	6.02	5.96	0.86
2.	5.00	5.02	4.97	1.07
3.	4.00	4.02	3.98	1.38
4.	3.00	3.00	2.97	1.92
5.	2.00	2.04	2.02	2.90
6.	1.04	0.99	0.98	6.17
7.	0.91	0.84	0.83	7.28
8.	0.80	0.74	0.73	8.37
9.	0.71	0.66	0.65	9.46
10.	0.59	0.53	0.53	11.67
11.	0.50	0.44	0.44	14.12
12.	0.40	0.33	0.33	18.71
13.	0.31	0.25	0.25	25.30

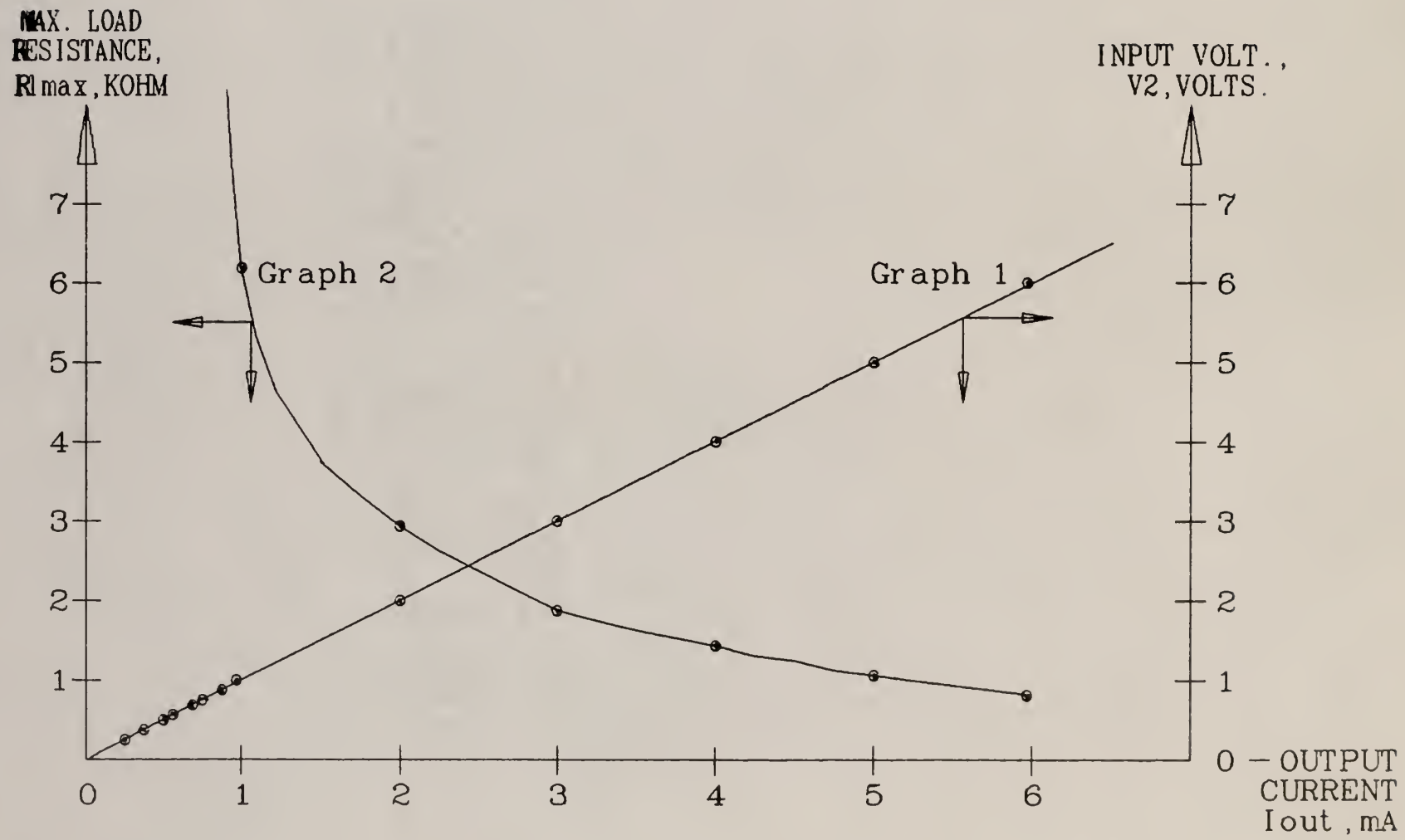


Fig.28. Output characteristics of Howland current source

The simple current sources constructed from the voltage supplies and resistors as shown in Figure 29 for the dual-rate integrating ADC is investigated.

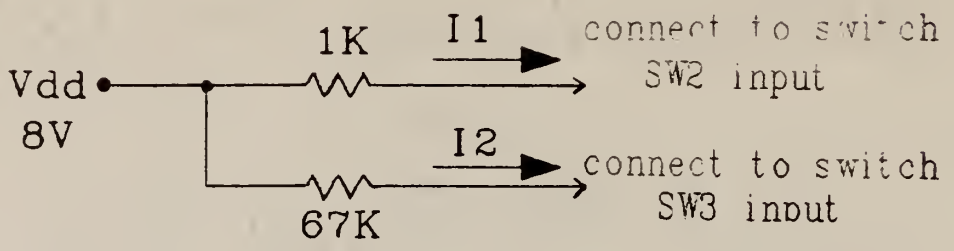


Fig.29. Simple current sources

The ADC conversion waveform as shown in Figure 30a using the current sources of Figure 29, shows the nonlinearity in the coarse-count slope. This rules out the possibility of using this kind of current source in the dual-rate integrating ADC because the capacitance load seriously affect the constant output current supplied. The Howland current source is used because of its simple circuit and easy application despite that its output current is limited by the power supplies. This limitation can be easily overcome. Figure 30b compares the linearity of the coarse and fine slopes using the Howland current source with that of Figure 30a. This result can also verify the MICRO-CAP analysis of section 3.3.2 (Figures 20 and 21).

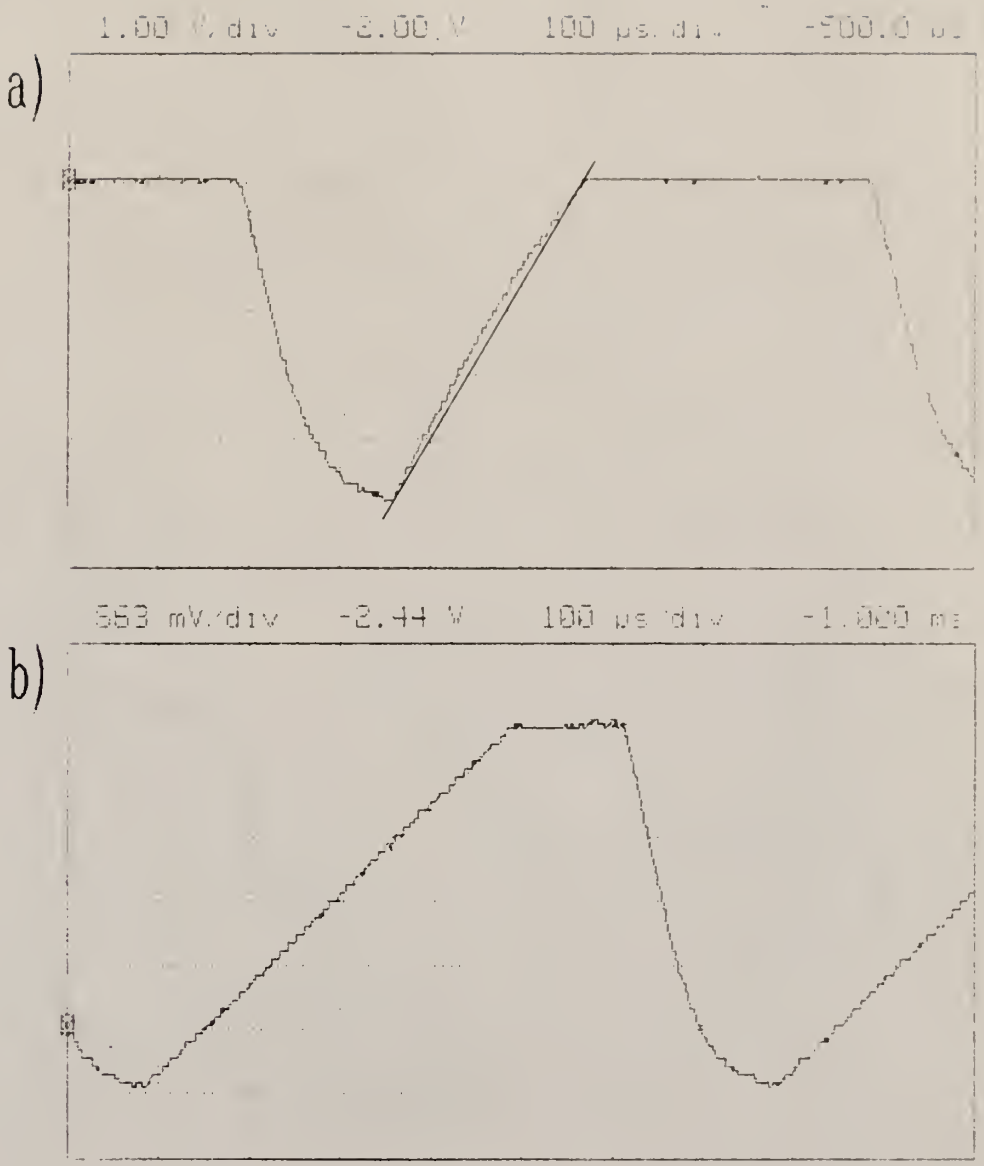


Fig.30. Dual-rate integrating ADC showing
a). nonlinearity in integrating slope using the current source of Fig.29.
b). linearity in integrating slope using the Howland current source.

4.3 Comparators Performance

For the 6-bit high and low order counters, this means for maximum analog input voltage, the conversion time using the coarse integrating current and the fine integrating current is the same. If this time is Tc / 2 and using C1 = 0.039E-6 F, from Table 6, Tc = 60.0 microseconds. Tc / 2 = 30.0 microsecs. For the high order comparator, the response time, Tr for a full scale output is (Tc / 2) / (2 * $(2^6 - 1)$) = 0.2381 microseconds. The slew rate for the high order comparator at the output is 14 / 0.2381 = 58.8 V/microsec. The gain of the comparator must be at least 7 / (5 / 126) = 176.4. With the LM339A comparator, the gain = 200 V/mV = 2E5 which is higher than required. The slew rate for a 20 mV overdrive = 4 / 0.0625 = 64 V/microsec., which is suitable for the high order comparator.

For the low order comparator, the smallest input overdrive is $5 / 2^{12}$ = 1.2 mV. The slew rate at the output of the low order comparator is 14 / 0.2381 = 58.8 V/microsecs. and the gain must be at least 5 / 1.22 V/mV = 4098.4. The LM339A comparator gain of 2E5 is suitable. The slew rate for a 5 mV overdrive is also 64 V/microsec. Therefore this comparator is suitable for this conversion rate using C1 = 0.039E-6 F.

For a larger hold capacitor C1, longer sample-conversion time is required but this improves the accuracy. For a hold capacitor C1 = 0.039E-6 F, the comparator is

tested and found to be able to perform the conversion to +/- 1 LSB of accuracy.

4.4 Performance of RC Relaxation Oscillator/Clock

From experiment, the RC relaxation oscillator output waveform is as shown in Figure 31a and the voltage across the capacitor is as shown in Figure 31b. The behavior of the RC relaxation oscillator waveforms and its principal operation is described in section 3.3.4. For R15 = 4K, and C5 = 0.005E-6F, the clock period as calculated is Tclk = R15 * C5 = 20E-6 seconds. Experimentally, the clock period = 20.42E-6 seconds which agrees closely to the calculated result, allowing for parameter errors. The duty cycle is 51 % as measured, which is close to 50 % duty cycle as expected of the RC relaxation oscillator. The frequency is observed to be stable. The slew rate is about 9.372E6 V / second which is fast enough. Clock frequency stability and minimum clock jitter are important especially for counting clock pulses because the pulse amplitude is linearly proportional to the number of clock pulses counted.

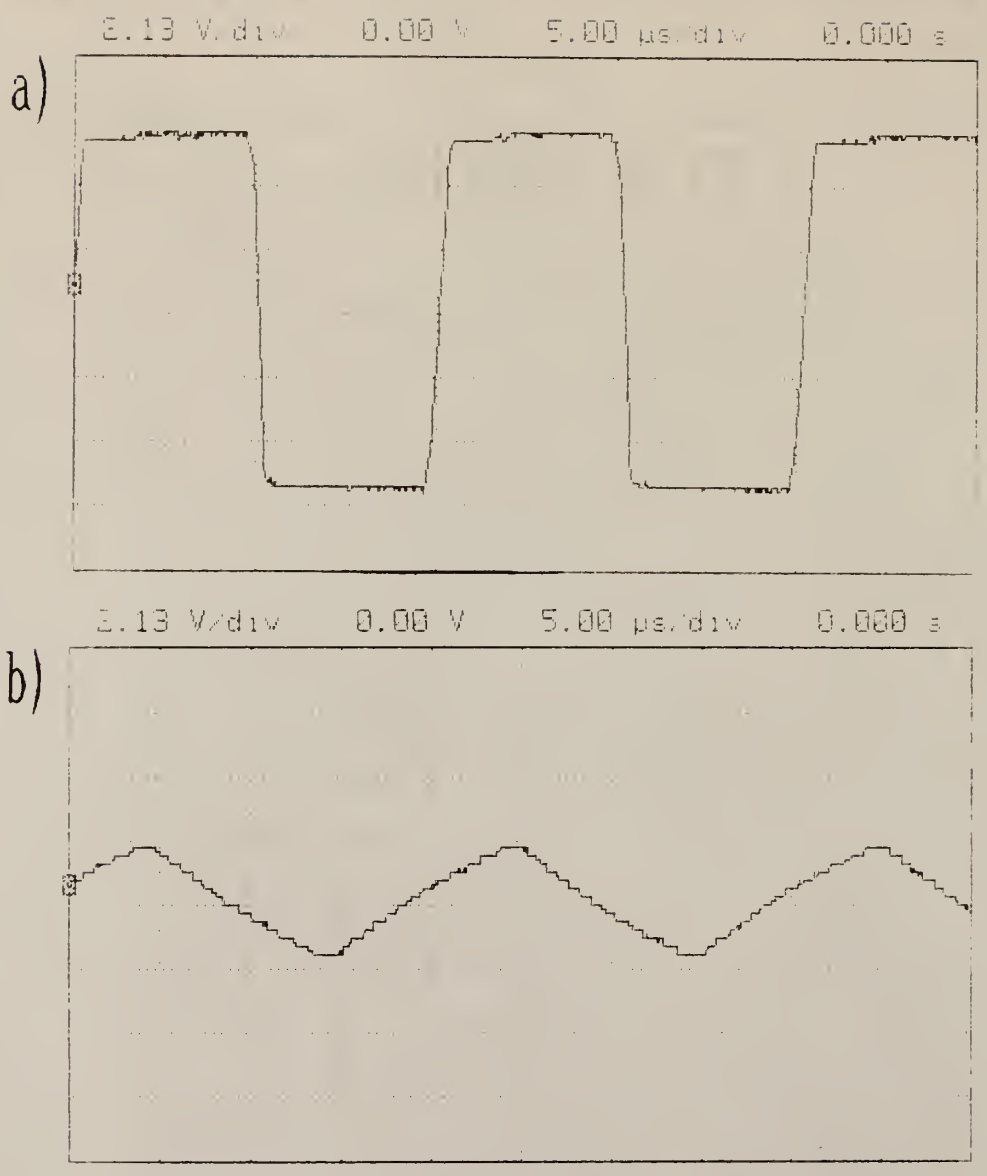


Fig.31. RC relaxation oscillator/timer
a). output waveform.
b). voltage across the capacitor C5 waveform.

4.5 Dual Rate Integrating ADC Performance

Using a hold capacitor C1 = 0.039E-6F and 6-bit high and low order counters, the threshold voltage for the first comparator is $Vt = -5 / (2^6 + 1) = -0.077$ V. The ADC conversion waveform is as given in Figure 32 with the coarse current I1 = 4.85 mA , I2 = 0.076 mA.

The slopes can be determined from Figure 32. The slope due to I1, S1 = (5 - 0.077) / 39.5E-6 V/s = 124633 V/sec. Theoretically S1 = I1 / C1 = 4.85 mA / 0.039E-6 sec = 124358.97 V/sec. The slope due to I2, S2 = 0.077 / 39.5E-6 V/sec = 1949.4 V/sec. Theoretically S2 = I2 / C1 = 0.0758 / 0.039E-6 V/sec. = 1943.6 V/sec. The experimental values of the two slopes agree closely with the theoretical values.

Table 4a gives the switch SW2 'on' interval, the integrating currents I1 and I2 values, and their ratio for different output voltages Vo corresponding to input voltage Vin in the range [-5, +5] V. Table 4b gives the switch SW3 'on' interval, the integrating currents I1 and I2 values and their ratio for different output voltage Vo corresponding to input voltage, Vin.

From Table 4a, the coarse count current I1 is more or less constant for Vin in the range [-5, +5] V, with a maximum variation of (|4.85 - 4.73| * 100) / 4.85 = 2.47 %. From Table 4b, the fine count current I2 is fairly constant

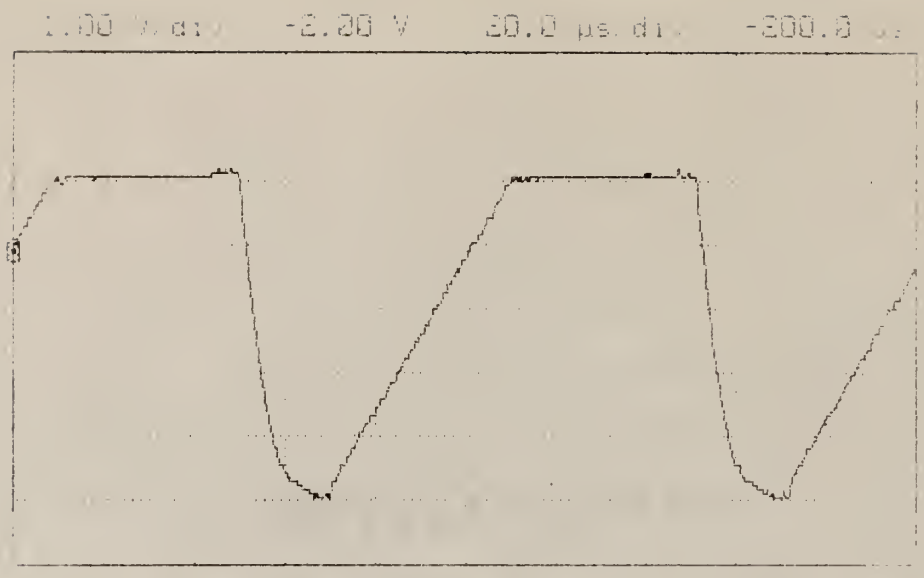


Fig.32. The dual-rate integrating ADC output waveform for hold capacitor C1 = 0.039E-6F, threshold voltage Vt = -0.077V and integrating currents I1 = 4.85 mA and I2 = 0.076 mA.

with a maximum variation of (|0.075 - 0.076| * 100) / 0.075 = 1.33 %. The small percentage error in the constancy of the two current values introduce very small error only.

The linear relationship of the coarse count interval (tSW2on) versus the analog voltage amplitude (Vo) and the linear relationship of the fine count interval (tSW3on) versus the analog voltage amplitude (Vo) can be verified from figures 33a and 33b respectively. Because the hold capacitor C1 value is fixed, a linear slope (I / C1) and hence the analog to digital conversion accuracy can be obtained only with constant discharging current.

Table 4a. Switch SW2 turn on interval, integrating currents I1, I2 and their ratio and output voltage Vo for input voltage,Vin in the range [-5, +5] V

#	Input voltage Vin (V)	Output voltage Vo (V)	Coarse Count I1 (mA)	Fine Count I2 (mA)	SW2 turn on time tsw2on (*E-6sec)	Ratio I1/I2
1.	5.00	-5.00	4.85	0.075	39.50	64.6
2.	4.00	-4.50	4.84	0.075	35.80	64.6
3.	3.00	-4.00	4.83	0.075	31.70	64.4
4.	2.00	-3.50	4.83	0.075	28.40	64.4
5.	1.00	-3.00	4.82	0.075	24.20	64.3
6.	0.00	-2.50	4.84	0.075	19.80	64.5
7.	-1.00	-2.00	4.84	0.075	16.10	64.5
8.	-2.00	-1.50	4.82	0.075	11.90	64.3
9.	-3.00	-1.00	4.81	0.075	7.70	64.1
10.	-4.00	-0.50	4.82	0.075	4.10	64.3
11.	-5.00	0.00	4.73	0.074	0.30	63.7

Table 4b. Switch SW3 turn on interval, integrating currents I1, I2 and their ratio and output voltage, Vo for corresponding input voltage, Vin.

#	Input Voltage Vin (V)	Output voltage Vo (V)	Coarse Count I1 (mA)	Fine Count I2 (mA)	SW3 turn on time tsw3on (*E-6sec)	Ratio I1/I2
1.	-4.80	-0.10	4.81	0.075	39.50	64.1
2.	-4.82	-0.09	4.79	0.075	39.50	63.9
3.	-4.84	-0.08	4.77	0.075	39.50	63.6
4.	-4.86	-0.07	4.79	0.075	36.80	63.9
5.	-4.88	-0.06	4.81	0.075	31.30	64.1
6.	-4.90	-0.05	4.81	0.075	26.10	64.1
7.	-4.92	-0.04	4.80	0.075	20.80	64.0
8.	-4.94	-0.03	4.79	0.075	15.50	63.9
9.	-4.96	-0.02	4.76	0.075	10.60	63.5
10.	-4.98	-0.01	4.75	0.075	4.90	63.3
11.	-5.00	0.00	4.73	0.076	0.20	62.2

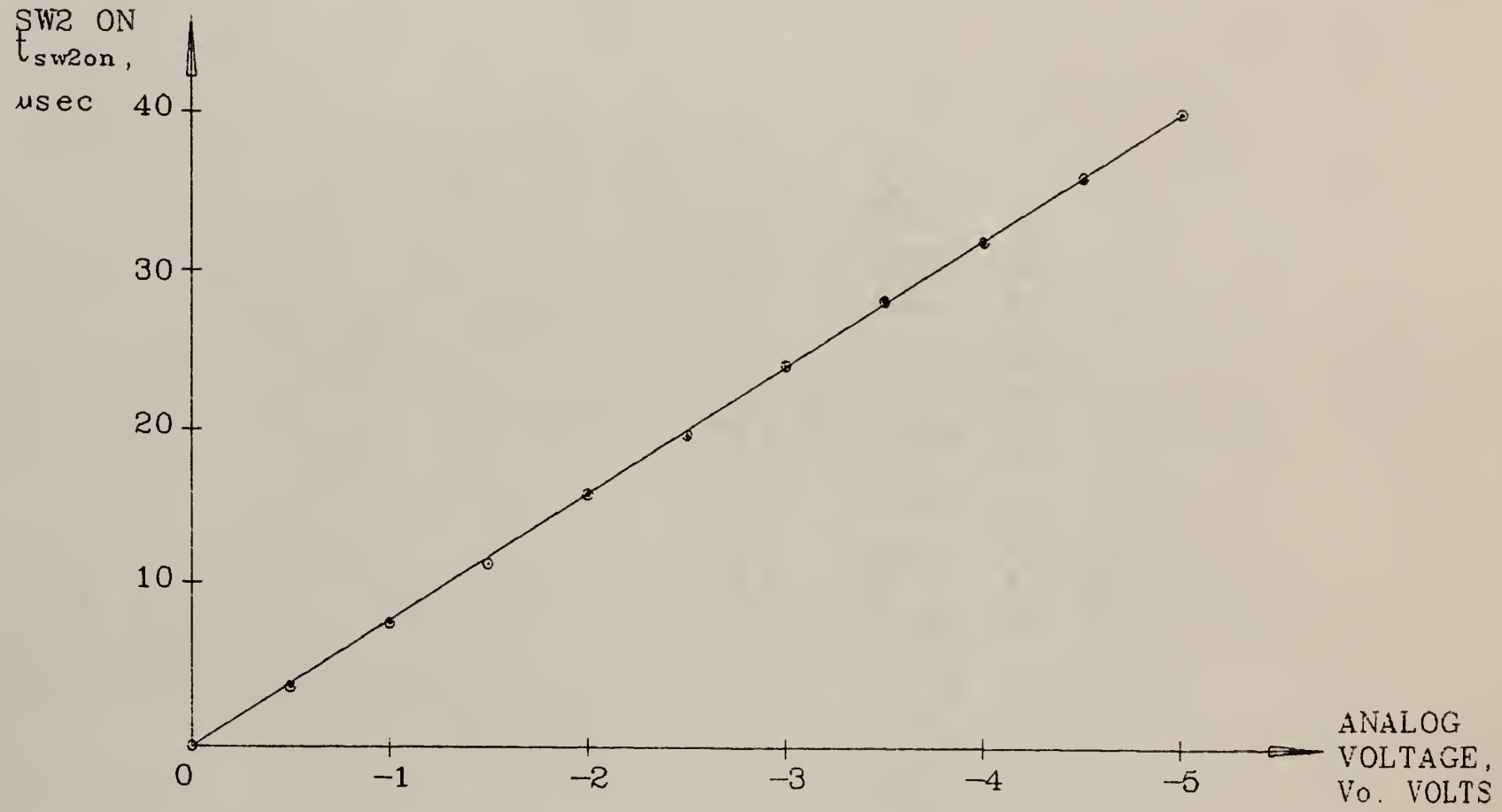


Fig.33a. Switch SW2 on time(tsw2on) vs. analog voltage(Vo).

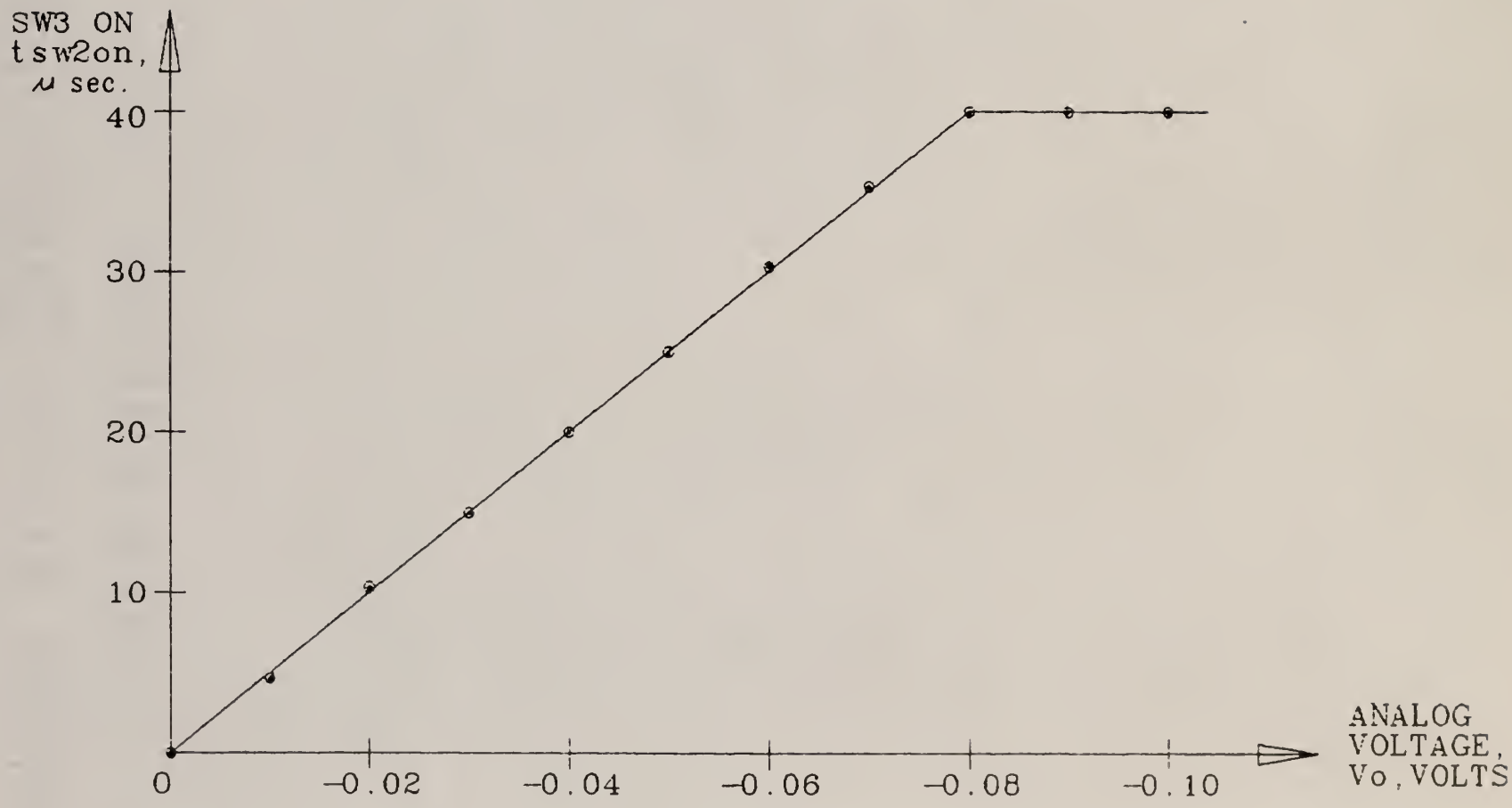


Fig.33b. Switch SW3 on time(tsw3on) vs. analog voltage(Vo).

Base on the theoretical slope value of 124359 V/sec. for the coarse count slope, and the theoretical slope value of 1943.6 V/sec. for the fine count slope, for Vin = +5 V, the accurate SW2 turn on time, tsw2on = (5 - 0.077) / 124359 = 39.587E-6 sec. and the accurate SW3 turn on time,tsw3on = 0.077 / 1943.6 = 39.617E-6 sec. Since 6-bit high and low order counters are desired, for a maximum input voltage, Vin = + 5 V, the maximum count for the high order and low order counters which is the same, is 63. Table 5 gives the SW2, SW3 and the total of SW2 & SW3 counts for various input voltages Vin in the range [-5, +5] V. The table also includes the theoretical total counts and the absolute error in the experimental total counts.

Figure 34a shows the total counts for SW2 and SW3 'on' time versus different input voltage Vin in the range [-5, +5] V. As can be observed from the plot of Figure 34a the total counts is linearly proportional to the input voltage. This means the dual-rate integrating ADC has a relatively high analog to digital conversion accuracy. Figure 34b gives a plot of the total count error for SW2 and SW3 'on' time versus the input voltage, Vin in the range [-5, +5] V. The error shows that the accuracy of the dual-rate integrating ADC is to +/- 1 LSB.

Table 5. Experimental SW2 & SW3 'on' time counts and their total counts, theoretical total counts and experimental total count error for various input voltage, Vin in the range [-5, +5] V.

#	Input volt. Vin (V)	SW2 on counts T2C	SW3 on counts T3C	SW2 & SW3 on total counts,TC T2C + T3C	SW2 & SW3 on theoretical counts,TTC	Measured total error,ETC TTC - TC
1	5.00	62.86	62.81	125.62	126.00	0.38
2	4.00	56.97	62.81	119.78	119.70	-0.08
3	3.00	50.45	62.81	113.26	113.40	0.14
4	2.00	45.20	62.81	108.00	107.10	-0.91
5	1.00	38.51	62.81	101.32	100.80	-0.52
6	0.00	51.51	62.81	94.32	94.50	0.18
7	-1.00	25.62	62.81	88.43	88.20	-0.23
8	-2.00	18.94	62.81	81.75	81.90	0.15
9	-3.00	12.25	62.81	75.06	75.60	0.54
10	-4.00	6.52	62.81	69.33	69.30	-0.03
11	-4.86	0.00	58.52	58.52	58.80	0.28
12	-4.88	0.00	49.77	49.77	50.40	0.63
13	-4.90	0.00	41.50	41.50	42.00	0.50
14	-4.92	0.00	33.08	33.08	33.60	0.52
15	-4.94	0.00	24.65	24.65	25.20	0.55
16	-4.96	0.00	16.86	16.86	16.80	-0.06
17	-4.98	0.00	7.80	7.80	8.40	0.60
18	-5.00	0.00	0.32	0.32	0.00	-0.32

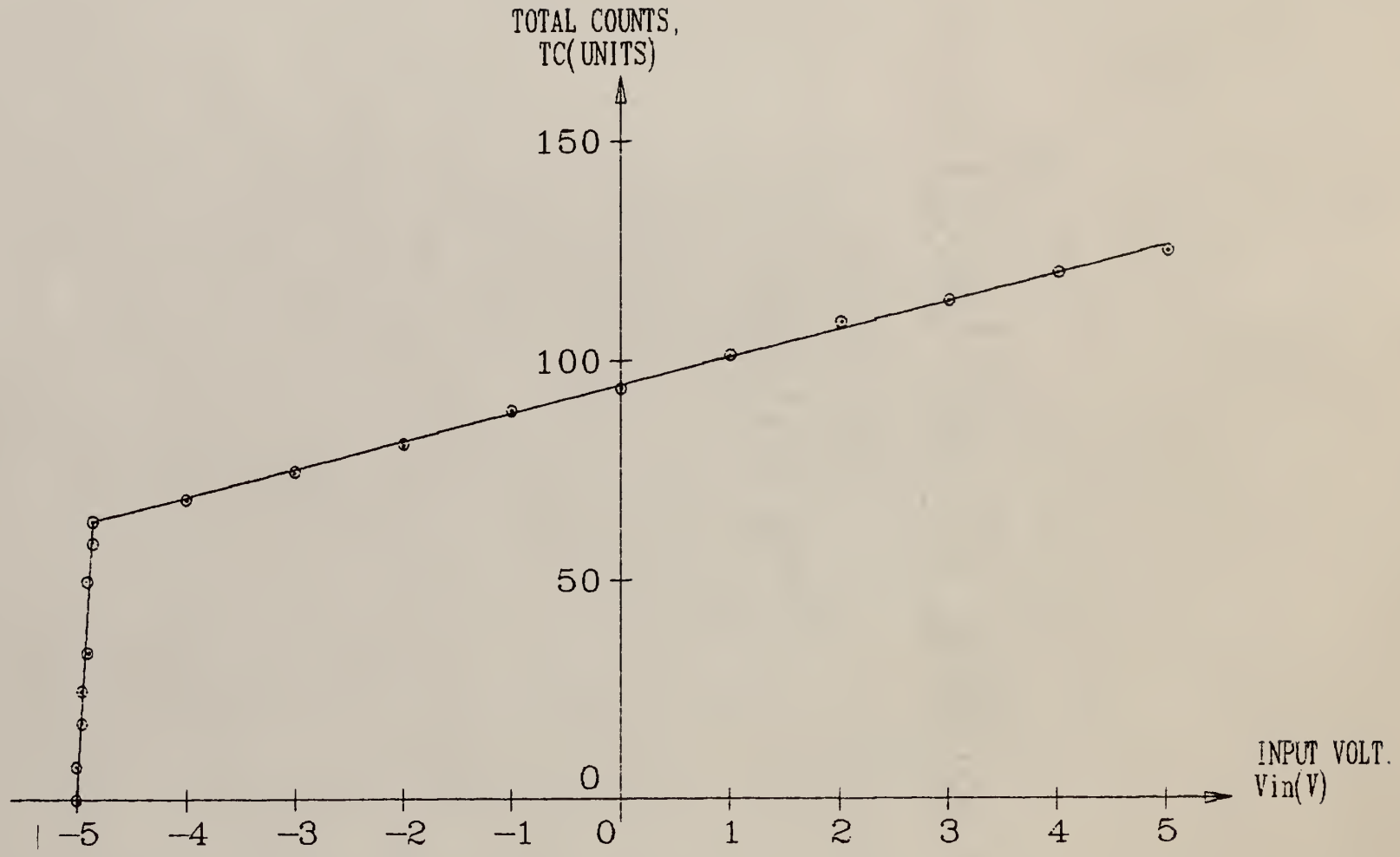


Fig.34a. Total counts for SW2 & SW3 on time(TC) vs. input voltage(Vin).

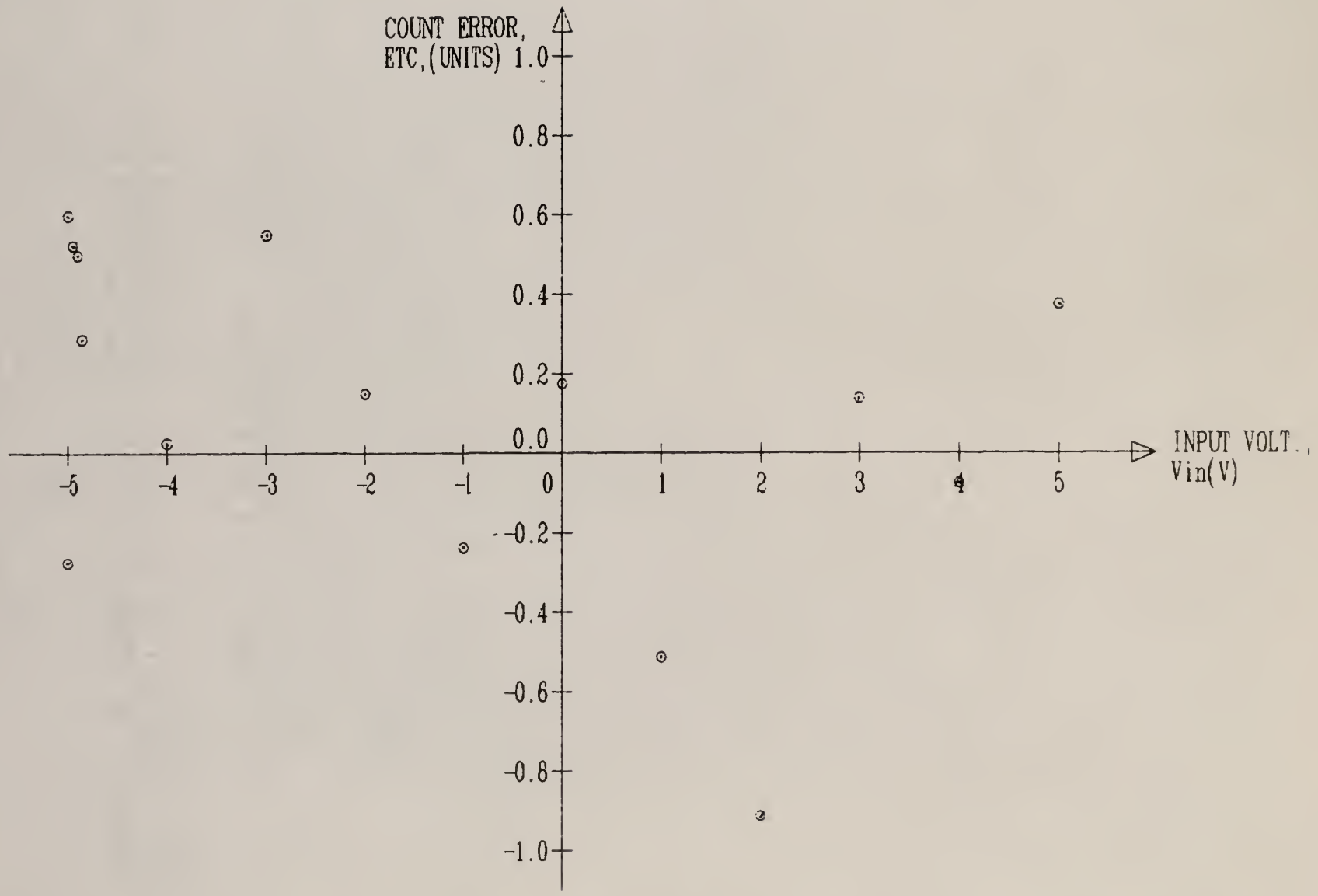


Fig.34b. Total count error for SW2 & SW3 on time(ETC) vs. input volt.(Vin)

4.6 Switching Control Logic Performance

Figure 35a shows the clock waveform with an adjustable clock period. The clock period is adjusted by varying the negative feedback resistor value in order to sample the input voltage amplitude in one clock period. The sampling follows the negative triggered clock edge. During that period, switch SW1 is on (logic low) for 1 clock period as shown in Figure 35c. When SW1 opens, the capacitor is discharged with current I1. Switch SW2 closes simultaneously (logic low). The coarse integrating slope occurs during the closing of SW2 (Figures 35b and 35d). When SW2 opens, SW3 closes simultaneously causing the fine integrating slope when C1 discharges with current I2 as shown in Figures 35b and 35e. There is a smooth transition of events without significant delay for the coarse-fine integrating ADC.

A more detailed switching waveforms for a repeated sampling and conversion of the coarse-fine integrating ADC is shown in Figure 36. This includes the D flip-flops resetting waveforms before the sample-convert cycle repeats.

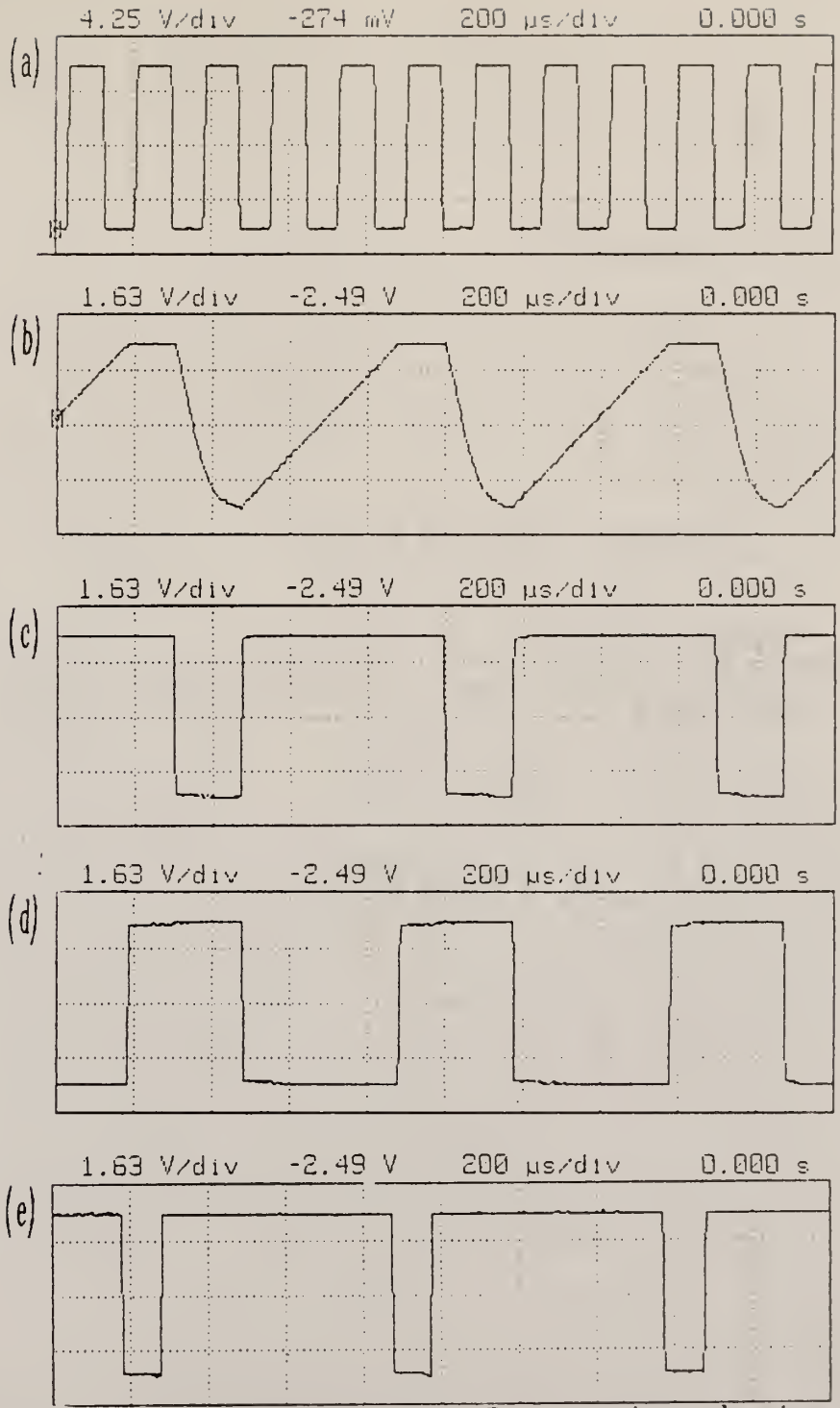


Fig.35. Dual rate integrating A/D converter showing (a) Switching clock waveform. (b) Dual rate integrating A/D converter waveform. (c) Switch SW1 switching waveform. (d) Switch SW2 switching waveform. (e) Switch SW3 switching waveform.

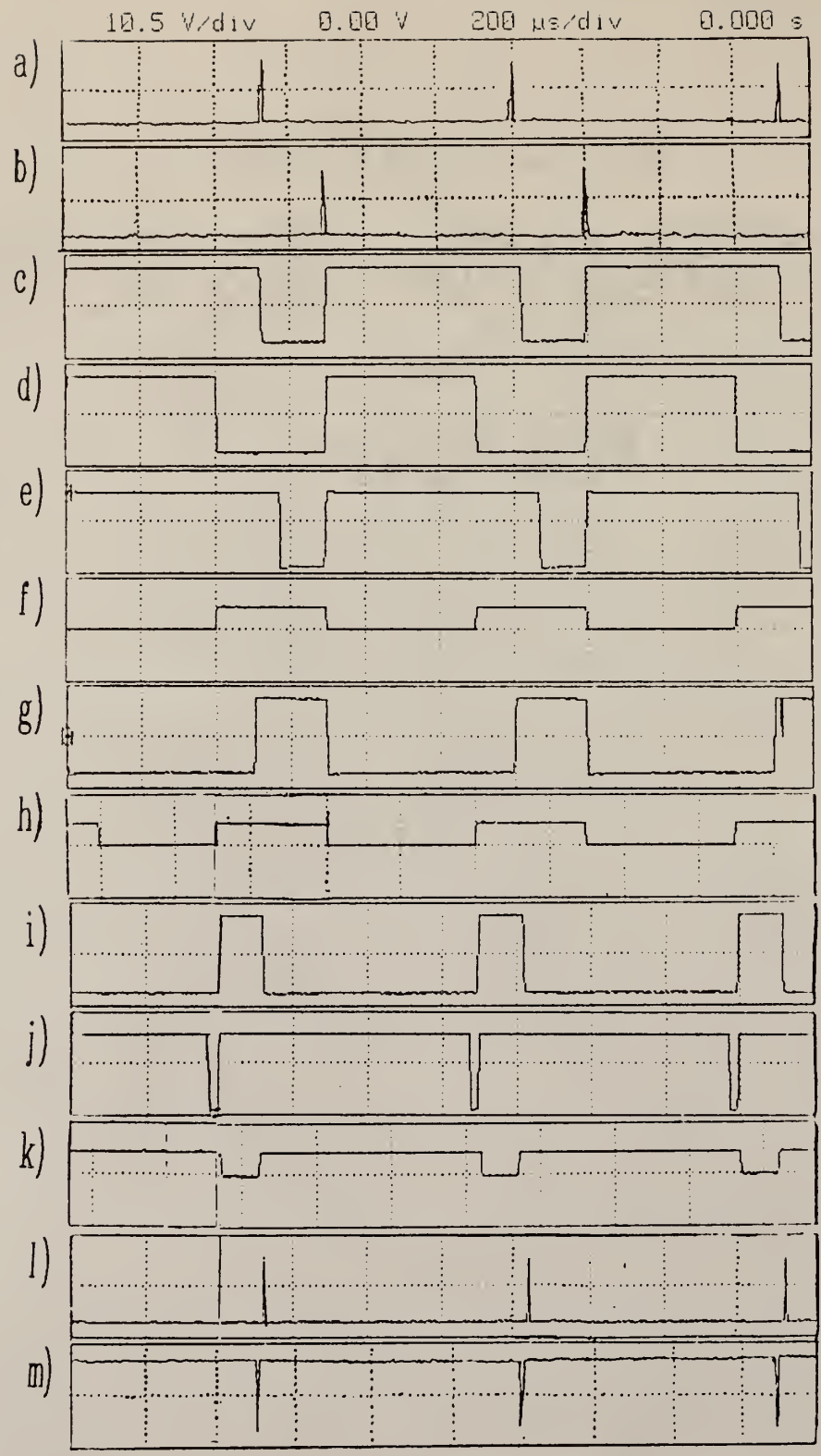


Fig.36. Timing diagram of dual rate integrating A/D converter.

a) CLK1 b) R1 c) SW1ON/Q1/CLK2 d) Q2 e) C2 f) SW2ON
g) R2 h) SW2ON/CLK3 i) Q3 j) C1 k) SW3ON l) R3 m) R'

4.7 Increase in Sampling and Conversion Rate of the Dual -Rate Integrating ADC

There are three methods to increase the rate of sampling and conversion of the dual rate integrating ADC.

4.7.1 Increase in Sampling and Conversion Rate Using Smaller Size Hold Capacitor, C1

The first method involves the use of a smaller size hold capacitor C1. Table 6 gives the different C1 values and the corresponding sample-hold time tsh, conversion time tc and the sample-conversion time tshc for an input voltage of +5 V ,the integrating currents of I1 = 6.4 mA and I2 = 0.1 mA, the current ratio I1 / I2 = 64, and a threshold voltage Vt = - 0.077 V. Figure 37 shows how the sample-conversion time tshc is reduced with a smaller size hold capacitor C1.

Table 6. The sample-hold time,tsh , conversion time,tc and sample-conversion time tshc for different size of hold capacitor C1.

#	Hold capacitor C1(*E-6 F)	Sample-hold time tsh(*E-6sec)	Conversion time tc(*E-6sec)	Sample-conversion tshc (*E-6sec)
1.	0.010	5.0	15.40	20.40
2.	0.020	10.5	30.80	41.30
3.	0.039	20.0	60.00	80.00
4.	0.082	40.0	126.21	166.21
5.	0.150	70.0	230.88	300.88

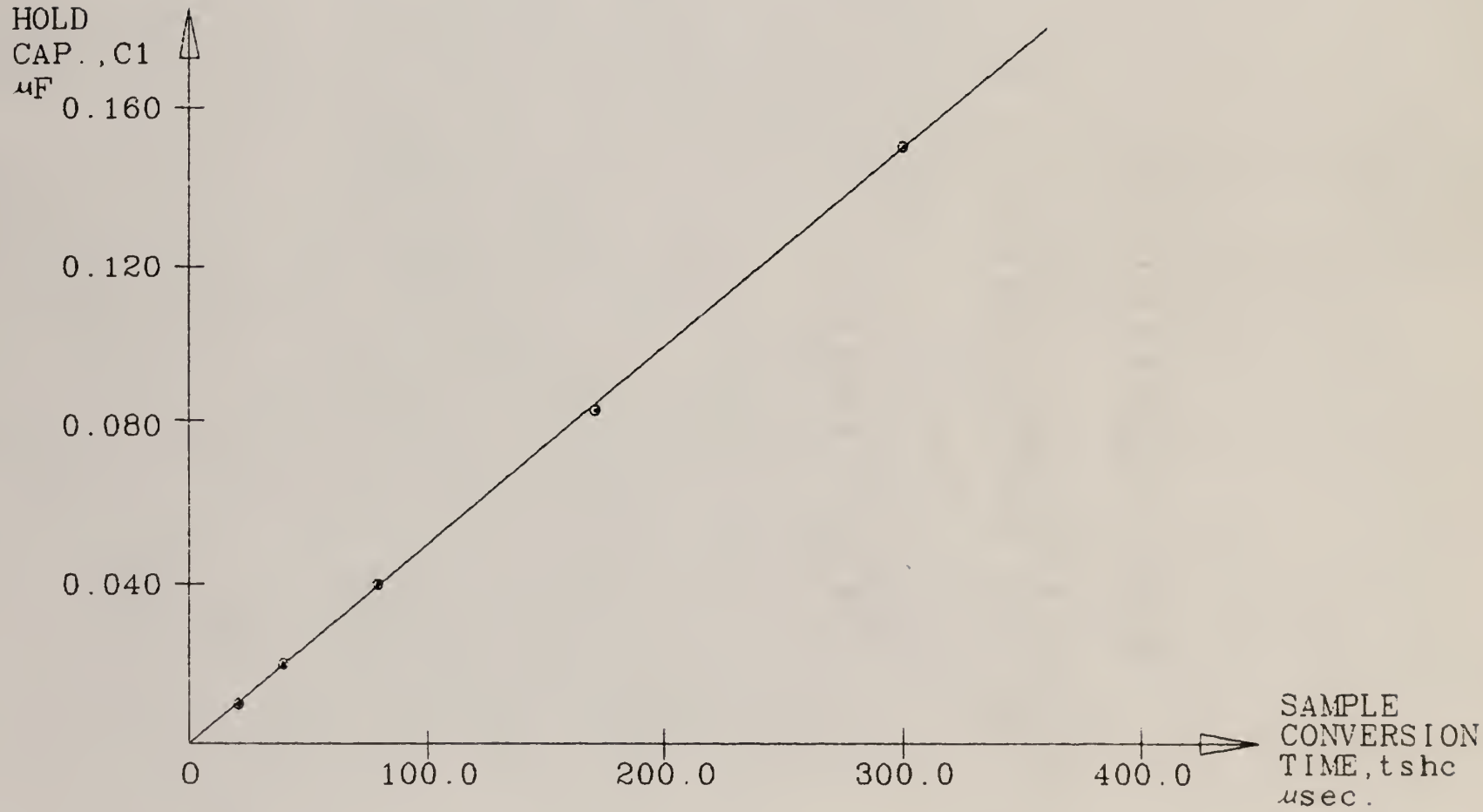


Fig.37. Hold capacitor (C1) vs. sample-conversion time (tshc)

4.7.2 Increase in Sampling and Conversion Rate Using Larger Integrating Currents

The second method to increase the speed of the dual rate integrating ADC is to increase the hold capacitor integrating currents I1 and I2 since these currents increase the integrating slopes. However, the two current ratio must be fixed. Using a hold capacitor C1 = 0.039E-6F for an input voltage of +5 V, and a threshold voltage Vt of -0.077 V, table 7 gives the sample-conversion time for 2 different pairs of current values while maintaining the current ratio I1 / I2. Figure 38b shows that the sample-conversion time is faster with larger integrating currents I1 and I2 compared with smaller integrating currents I1 and I2 as shown in Figure 38a.

Table 7. The sample-conversion time of the dual rate integrating ADC with different currents I1 and I2 values while maintaining the current ratio.

Coarse Integrating current I1 (mA)	Fine Integrating current I2 (mA)	Ratio I1/I2	Sample-conversion time tsc (*E-6 secs.)
4.85	0.075	64.66	99.6
6.40	0.100	64.00	80.0

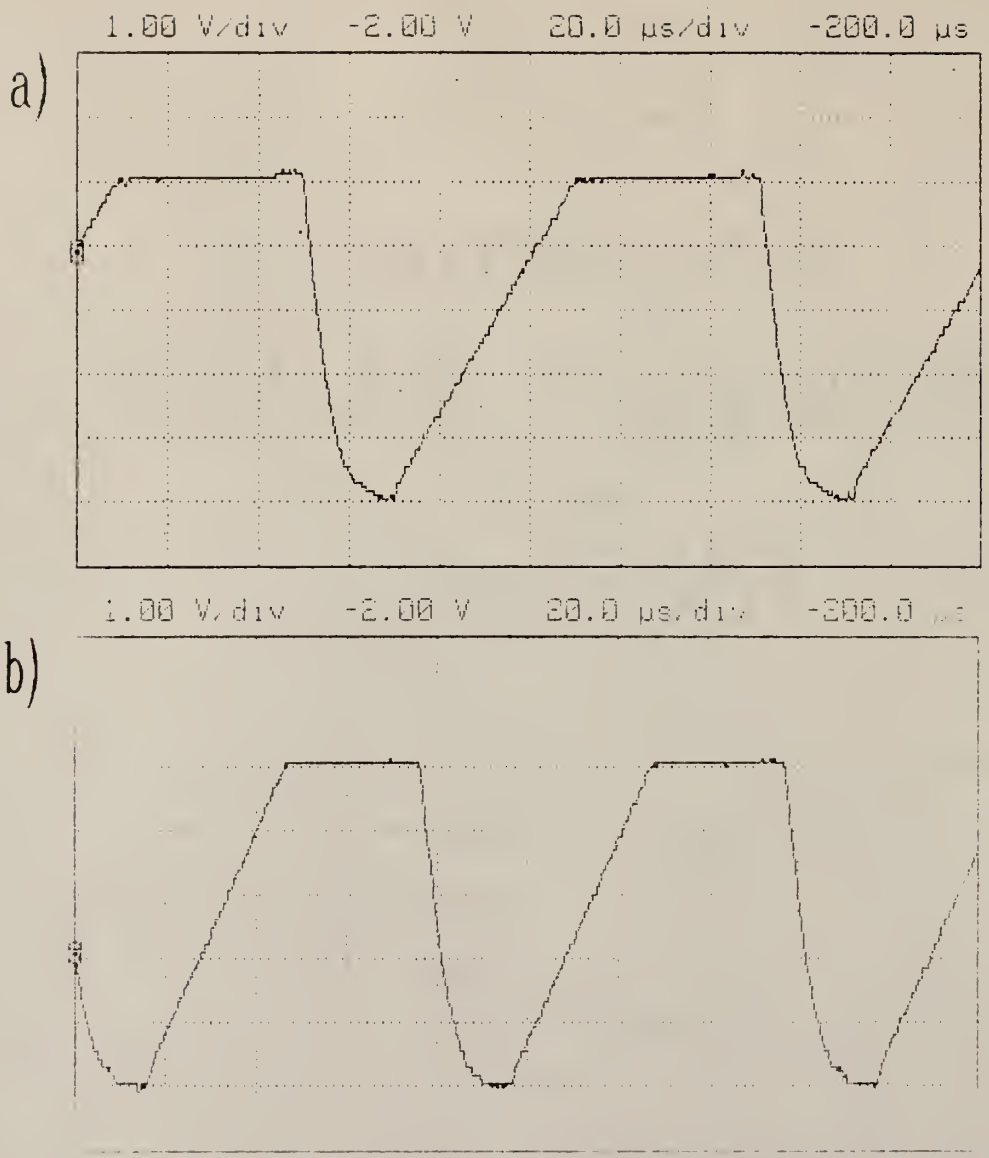


Fig.38. The dual rate integrating ADC showing
a). slower sample-conversion time with smaller integrating currents.
b). faster sample-conversion time with larger integrating currents.

4.7.3 Increase in Sampling and Conversion Rate by Reducing Threshold Absolute Voltage

The third method to increase the speed of the dual rate integrating ADC is to reduce the absolute value of the threshold voltage. This results from reducing the number of bits of the low order counter and increase the number of bits of the high order counter. This means the low order precision is reduced. Table 8 gives the integrating currents values, their ratio, the threshold voltage and the sample-conversion time.

Figure 39b shows that by increasing the absolute threshold voltage, the conversion time is significantly increased especially for the fine count. A faster dual rate integrating ADC usually has more number of bits for the high order counter than for the low order counter.

Table 8. The sample-conversion time corresponding to the current values, current ratio, and threshold voltage.

Coarse Integrating current I1 (mA)	Fine Integrating current I2 (mA)	Ratio I1/I2	Threshold voltage Vt (V)	Sample-conversion time tsc (*E-6 sec)
6.40	0.10	64.0	-0.077	80.00
6.40	0.05	128.0	-0.152	167.72

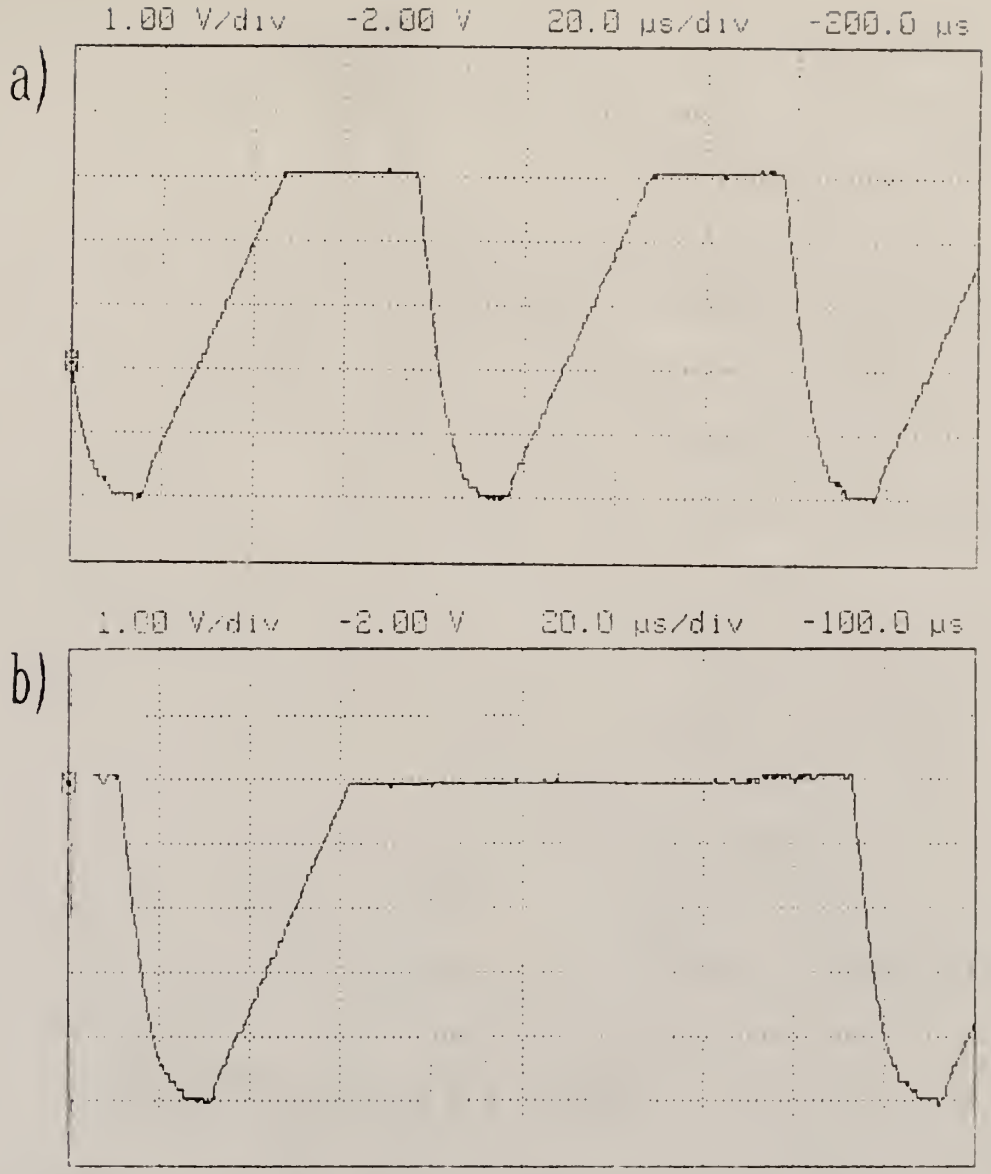


Fig.39. The dual-rate integrating ADC showing
a). faster sample-conversion time with smaller threshold absolute voltage.
b). slower sample-conversion time with bigger threshold absolute voltage.

4.8 Improving the Accuracy of the Dual-Rate Integrating ADC

The accuracy of the dual rate integrating ADC can be improved in several ways.

1. The coarse and fine integrating currents should be constant if good linearity and differential linearity of the dual-rate integrating ADC is required. Table 9a and 9b shows a 3.4% and a 1.96% maximum variations in the constant current values I1 and I2 respectively. Graphs (a) of Figure 40 and 41 do not show any significant linearity and differential linearity error. If higher percentage variations in the integrating currents occur resulting in linearity and differential error, the current sources have to be improved or replaced by a more suitable one.

2. The currents ratio should also be fixed by the ratio 2n where n is the number of bits of low order counter. This reduces the differential linearity error. From tables 9a and 9b, the currents ratio varies by 3.3 % and the problem can be reduced as mentioned in 1 above.

3. The offset errors for the data in Table 9a and 9b do not appear significant from the plots (a) and (b) of Figure 40 as well as Figure 41. This result from choosing operational amplifiers and comparators with very low offset voltages, low leakage analog switches and good quality hold capacitor.

However, if the offset error exist, it can be corrected in software by substracting the number of counts due to the offset.

4. Figure 40a is an accurate ADC's output. Figure 40b shows the presence of gain error for the data from Table 9a. Similar result is shown in Figure 41b. Gain error can be reduced by reducing the operation amplifier gain or by using software method as for the offset error.

5. By increasing the number of bits of resolution for the dual-rate integrating ADC, the accuracy can be improved.

6. Noise affects the accuracy of the dual rate integrating ADC during switching. Noise in the ADC system are reduced by:

1). By-passing the positive and negative power supplies close to the operational amplifiers and comparators.
2). Using short connecting leads as possible.
3). Twist the power supplies wires.
4). Provide feedbacks for the comparators and operational amplifiers where possible.

7. The clock frequency stability and the absence of clock jitter is important for accurate counting of clock pulses. A stable clock frequency should therefore be used.

Table 9a. The experimental and calculated switch SW2 'on' time (tsw2on) and integrating currents I1 and I2 values and their ratio corresponding to input voltage Vin (C1 = 0.039E-6F, Vt = - 0.077V)

Input voltage Vin (V)	Coarse count current I1 (mA)	Fine count current I2 (mA)	Ratio I1/I2	tsw2on with gain (*E-6sec)	tsw2on calcu-lated (*E-6sec)
5.0	6.40	0.102	62.8	20.5	30.0
4.5	6.40	0.102	62.8	19.5	28.5
4.0	6.40	0.102	62.8	18.5	27.0
3.5	6.40	0.102	62.8	17.5	25.5
3.0	6.40	0.101	63.4	16.5	24.0
2.5	6.39	0.101	63.3	15.5	22.5
2.0	6.38	0.101	63.2	14.5	21.0
1.5	6.39	0.101	63.3	13.5	19.5
1.0	6.39	0.101	63.3	12.5	18.0
0.5	6.37	0.101	63.1	11.2	16.5
0.0	6.35	0.101	62.9	10.3	15.0
-0.5	6.35	0.102	62.3	9.5	13.5
-1.0	6.34	0.102	62.2	8.0	12.0
-1.5	6.33	0.102	62.1	7.0	10.5
-2.0	6.33	0.102	62.1	6.0	9.0
-2.5	6.33	0.102	62.1	5.0	7.5
-3.0	6.32	0.102	62.0	4.0	7.0
-3.5	6.31	0.102	61.9	3.0	4.5
-4.0	6.34	0.102	62.2	2.0	3.0
-4.5	6.32	0.102	62.0	1.0	1.5
-5.0	6.20	0.100	61.8	0.0	0.0

Table 9b. The experimental and calculated switch SW3 'on' time tsw3on and integrating currents I1, I2 and their ratio corresponding to input voltage Vin. (C1 = 0.039E-6 F, Vt = -0.077 V)

Input voltage Vin (V)	Coarse count current I1 (mA)	Fine count current I2 (mA)	Ratio I1/I2	tsw3on with gain (*E-6sec)	tsw3on calcu-lated (*E-6sec)
-4.86	6.41	0.101	63.5	6.00	30.00
-4.88	6.40	0.101	63.4	5.00	25.71
-4.90	6.39	0.101	63.3	5.30	21.43
-4.92	6.36	0.101	63.0	3.40	17.14
-4.94	6.32	0.101	62.6	2.60	12.86
-4.96	6.31	0.101	62.5	1.80	8.57
-4.98	6.30	0.101	62.4	0.90	4.28
-5.00	6.35	0.100	63.5	0.00	0.00

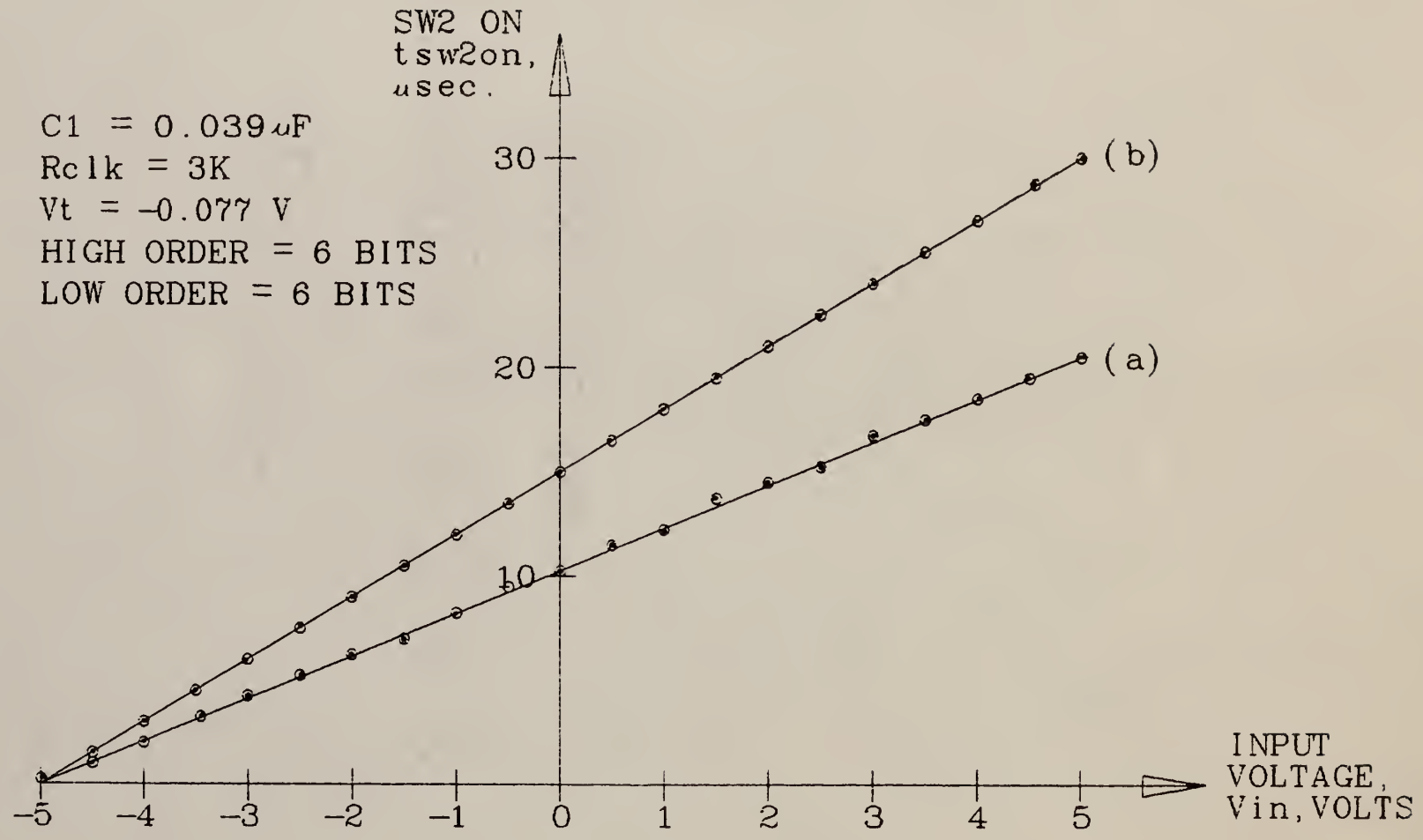


Fig.40.(a)Experimental & (b)Accurate SW2 on time,(tsw2on) vs. input volt.,(Vin)

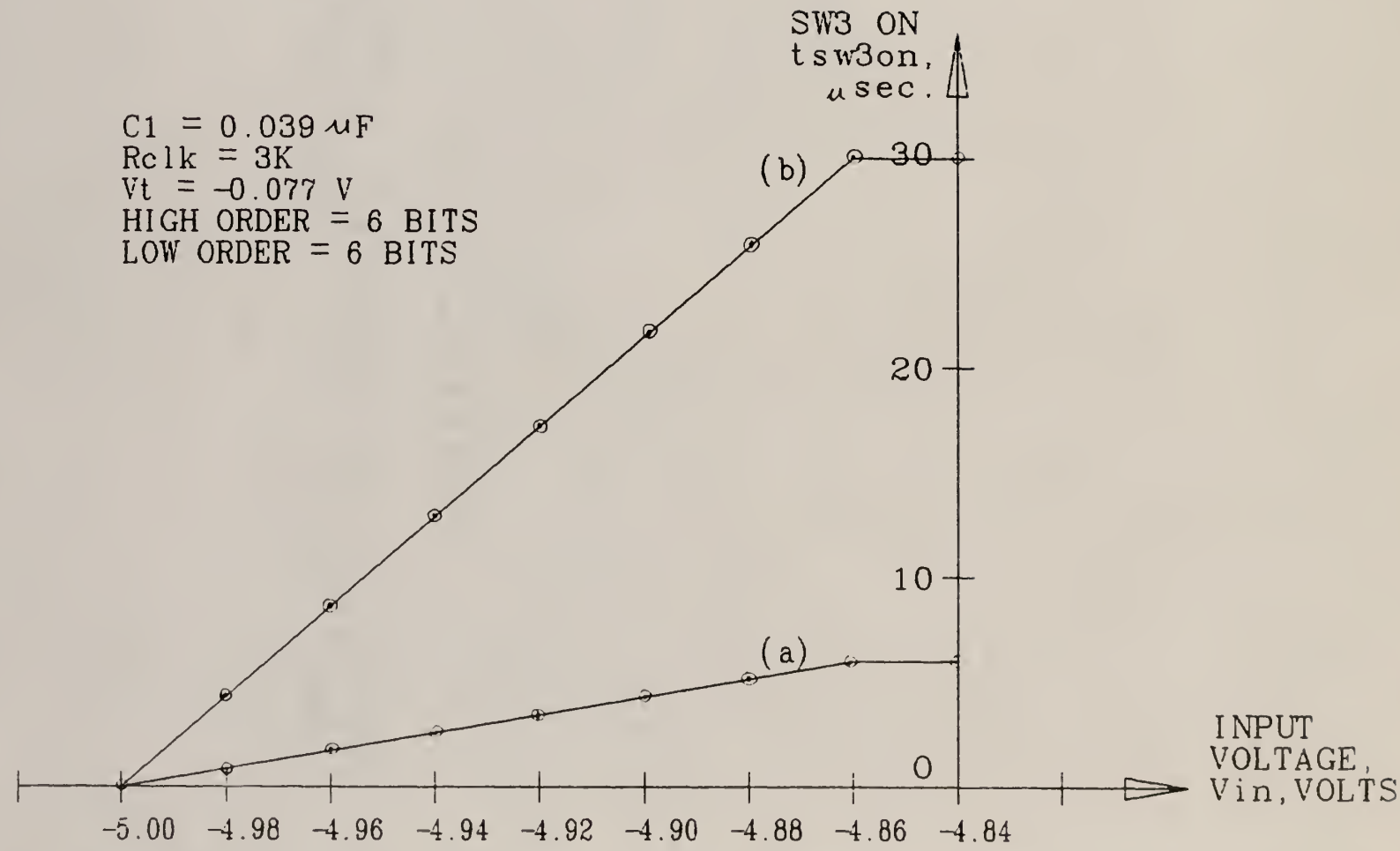


Fig.41. Experimental(a) & Accurate(b) SW3 on time,(tsw3on) vs. input volt,(Vin)

CONCLUSION

A 12 bit low-power, high-accuracy, dual-rate integrating ADC has been designed, constructed, and tested for a 4096-channel multichannel analyzer for the radiation detection. The low-power ADC system is achieved by using CMOS integrated circuits, + 7.5 V and - 7.5 V power supplies. Power consumption is also reduced by using the dual-rate integrating technique instead of the single rate integrating, the Wilkinson-type or the successive approximation techniques.

An accuracy of +/- 1 LSB can be obtained using the dual -rate integrating ADC without the use of correction circuit whereas the Wilkinson-type and the successive approximation ADCs require correction circuits for reducing differential non-linearity error. This complicates the circuitry by requiring more components and increase the power consumption too.

To increase the rate of conversion of the dual rate integrating ADC, three methods discussed are : using smaller hold capacitor, increasing the integrating currents and reducing the threshold voltage. Usually the rate of conversion is increased at the expense of increased power consumption. Because the sample-hold operational amplifier and comparators slew rate place limitation on the rate of sampling and conversion of this converter system, it is found that the best capacitor size to use is 0.039E-6 F

which yields a sample-conversion time of 80 microsecs. for a +5 V input voltage using a coarse integrating current I1 of 6.40 mA and the fine-integrating current I2 of 0.10 mA.

The dual rate integrating ADC is therefore a possible replacement for the commonly-used Wilkinson-type ADC in radiation detection electronic especially where high-accuracy and low-power is required. A dual channel system can be built to increase the rate of sampling and conversion and to improve the performance of the dual rate integrating ADC system. Further improvement on the rate of sampling and conversion can possibly be achieved by using the high speed CMOS integrated circuits.

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APPENDIX A

TESTING VOLTAGE OFFSET OF AN OPERATIONAL AMPLIFIER

Testing voltage offset of an operational amplifier is as shown in Fig. a.

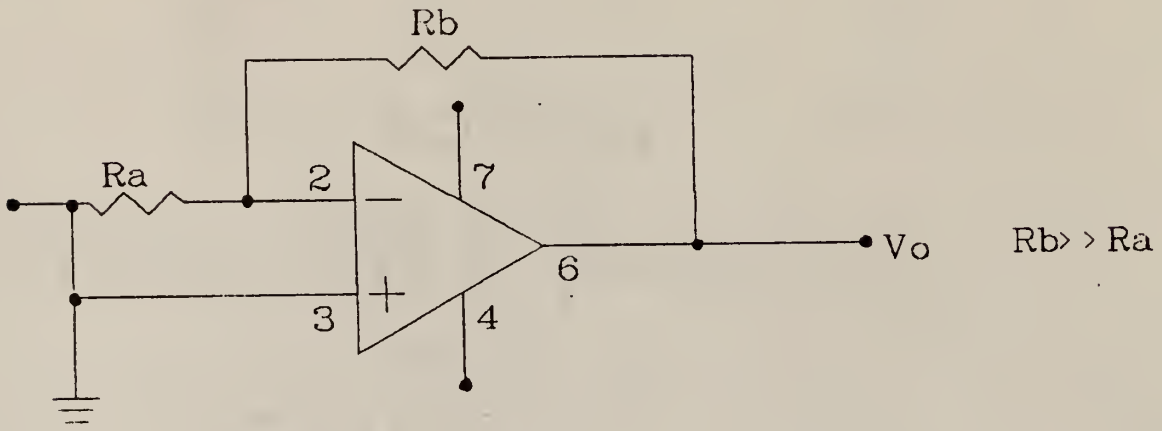

Fig. a

Voltage offset, Vos = Vo / (Rb / Ra)

APPENDIX B

CMOS SWITCH ON RESISTANCE

For a CMOS switch, the ON resistance is that resulting from a parallel combination of n- and p- channel devices. The effective resistance is almost constant over a wide analogue signal range as shown in Fig. b.

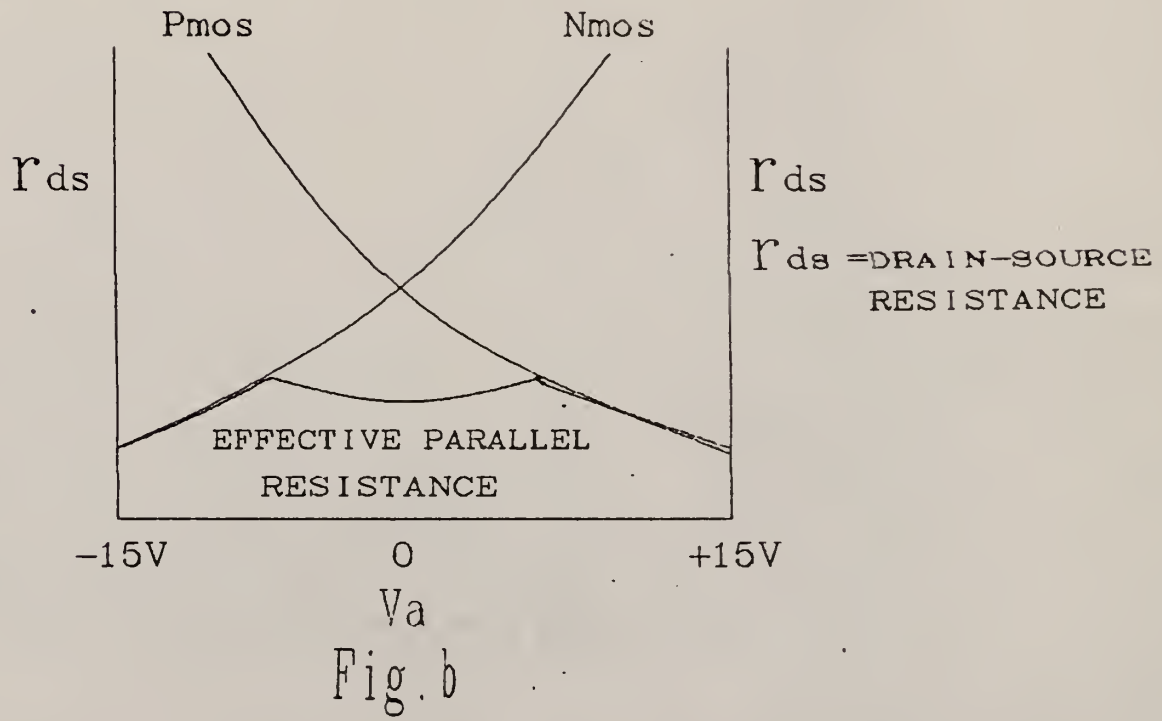

Fig. b

IMPROVEMENTS IN RADIATION DETECTION ELECTRONICS

by

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B. Sc., Iowa State University, 1986

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ABSTRACT

The design, construction, and test of a 12-bit, low-power, high-accuracy dual-rate integrating ADC system with a conversion time of 60 microsec. for a + 5 V input voltage for a 4096-channel multichannel analyser is described. Low-power consumption is achieved by using CMOS integrated circuits, low power supplies, dual rate integrating technique and simple circuit design. The integrating behavior of the ADC improves the conversion accuracy and rejects noise without requiring correction circuit. Three methods to increase the conversion rate include reducing the hold capacitor size, increasing the integrating currents and reducing the threshold voltage. However, the low-power supplies, the operational amplifiers, the comparators, and the current sources place limitations on the three methods. The concluding result is to use a hold capacitor size of 0.039E-6 F, the integrating currents of 6.40 mA and 0.10 mA and a threshold voltage of -0.077 V using a 6-bit high and low order counters. Comparisons are made between the dual rate integrating ADC and the Wilkinson-type ADC as to why the former is a better replacement for the later in radiation detection electronics.