THE DESIGN AND IMPLEMENTATION OF AN INTERFACE BETWEEN THE NOVA 1200 AND THREE PERIPHERALS: AN ANALOG-TO-DIGITAL CONVERTER, A DIGITAL-TO-ANALOG CONVERTER, AND AN INCREMENTAL TAPE TRANSPORT

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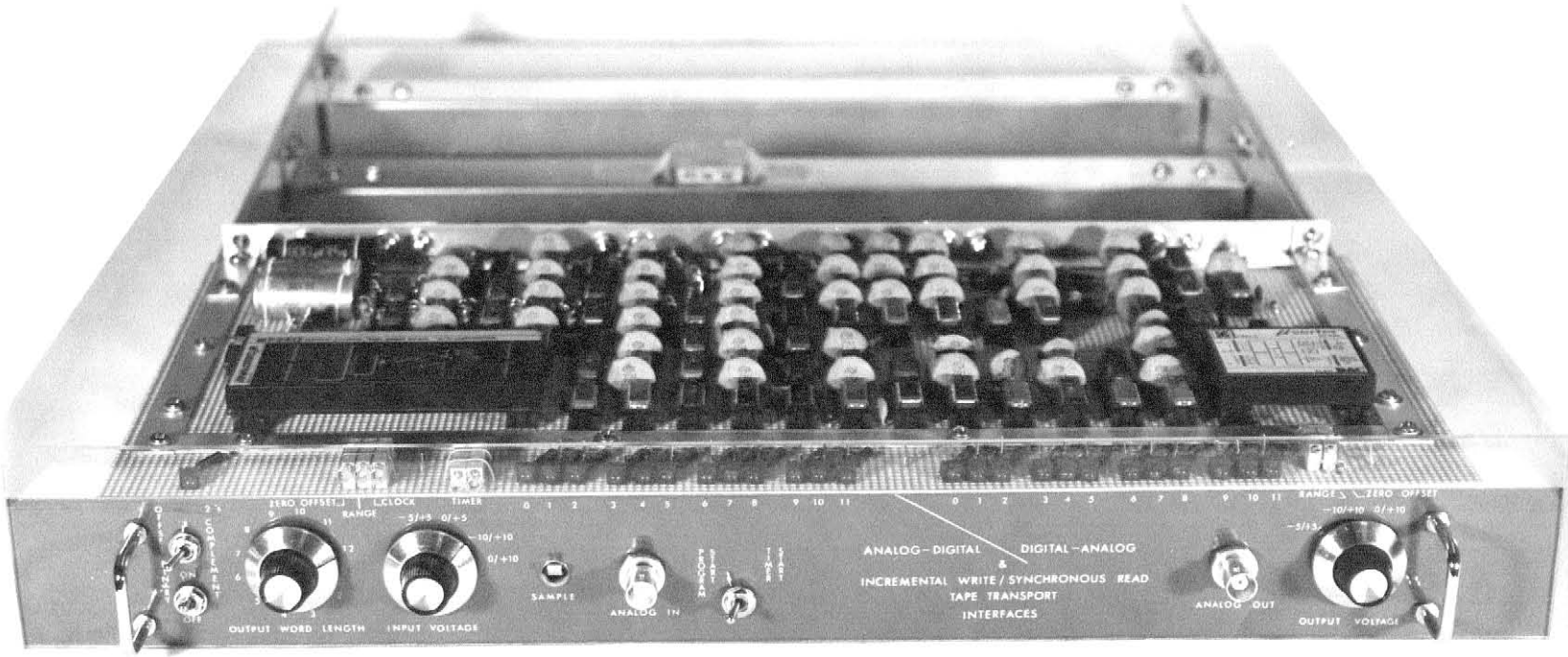
ANALOG-DIGITAL
DIGITAL-ANALOG
&
INCREMENTAL WRITE / SYNCHRONOUS READ
TAPE TRANSPORT
INTERFACES
OUTPUT WORD LENGTH
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SAMPLE
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CHAPTER I

INTRODUCTION

The Departments of Electrical Engineering and Speech at Kansas State University (KSU) are jointly interested in the analysis and synthesis of speech waveforms. To accomplish these functions digitally, it is first necessary to digitize speech waveforms and then to use digital signal processing techniques on the resulting digital data.

In the past, analog waveforms were digitized by a Texas Instruments Model 848 Analog-to-Digital Converter, while the control of the sampling rate and the fetching of the digital data were performed by an Athena computer, an ex-Air Force machine. The Athena then transferred the digital data to a Peripheral Equipment Corporation (PEC) Incremental Write Tape Transport. The output tape of the PEC tape transport was then taken to the KSU Computing Center, where it was made compatible with the pertinent formats of the IBM 370/158 computer. A detailed analysis of the digitized data was then carried out on the IBM 370/158 using a high level language, such as FORTRAN.

However, the above system was restricted by limitation of the Athena hardware to digitizing signals having a bandwidth of only a few hundred Hertz. Since typical speech signals have bandwidths of approximately 4 kHz., it was decided to obtain a data acquisition system capable of digitizing a variety of signals having bandwidths in excess of 10 kHz. This report concerns the design and implementation of such a system.

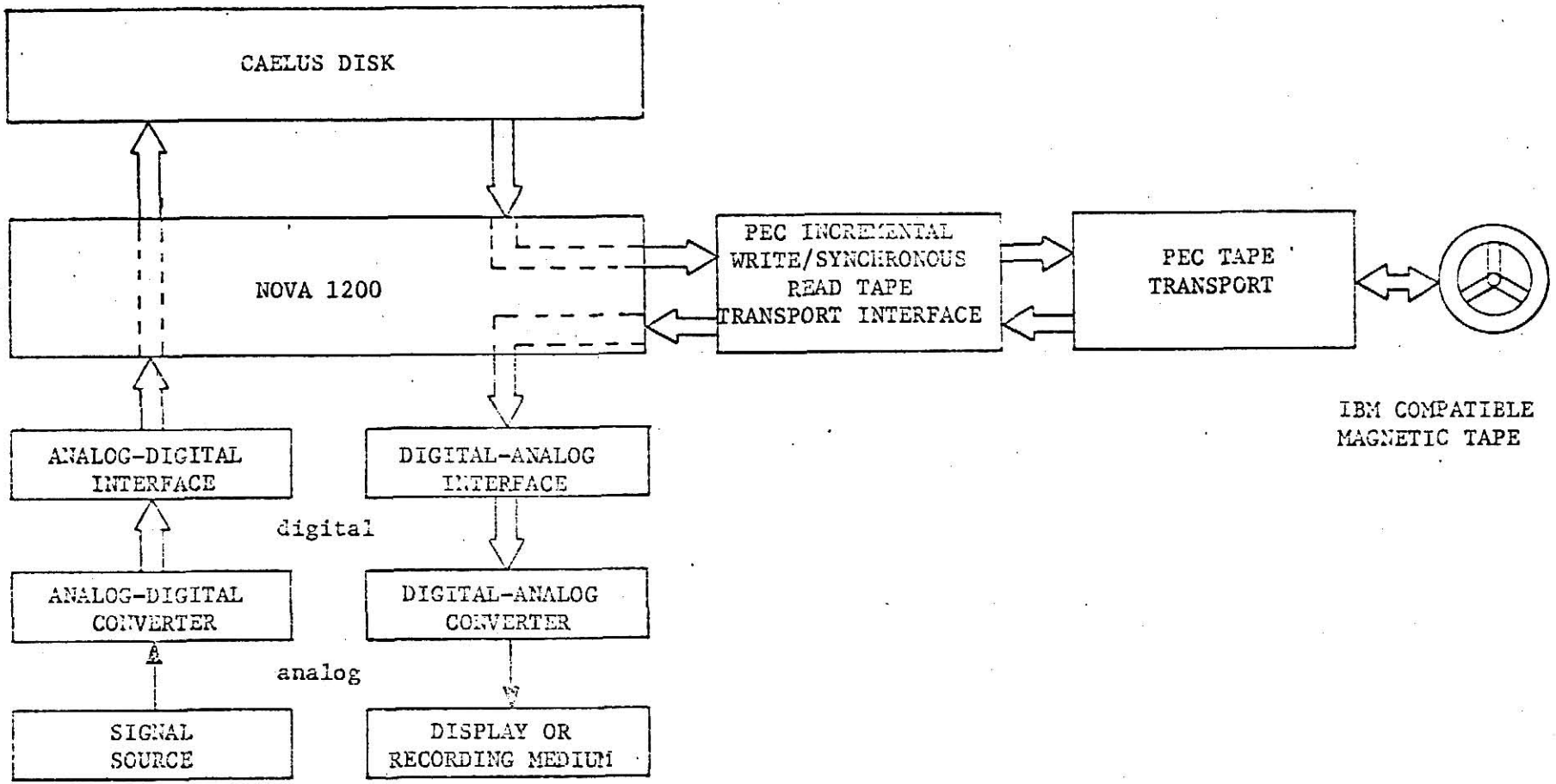


Fig. 1-1. Information flow diagram.

The desired data acquisition system employs the Electrical Engineering Department's Nova 1200 minicomputer for control purposes and its Caelus disk system for temporary storage of the digital data. Such a system would be limited only by the time required to position the disk recording head, if a sufficiently fast analog-to-digital converter were utilized. By transferring as large a block of data as possible for each disk head movement, real time conversion rates in excess of 10 kHz could be achieved. After the digital data had been recorded on the disk, a more leisurely transfer to the PEC incremental recorder could be accomplished, since the maximum rate at which one can write on the latter is 700 8-bit bytes/second. A digram that indicates the information flow in the overall system is shown in Fig. 1-1.

The operating instructions of Chapter II explain how the information flow of Fig. 1-1 is controlled by Nova software. This chapter will also serve as a prelude to the remaining chapters, which essentially describe the hardware implementation of the controlling input-output instructions. Chapter III presents a tutorial discussion on interfacing Nova computers, while Chapter IV shows how a basic interface was adapted for each of the three peripheral devices. The concluding chapter, Chapter V, presents some ideas with respect to the uses of this data acquisition system in the general area of digital signal processing. Suggestions related to additional hardware that might be built are also included. Finally, Appendices A and B contain, respectively, complete circuit diagrams and manufacturers' data sheets.

CHAPTER II

OPERATION

Preliminaries

Since the external bus terminators should have power applied whenever the Nova is in use, the toggle switch on the separate power supply should normally be in the REMOTE ON position. The ON position of the power supply toggle switch supplies power to the interface regardless of whether the Nova is on or off.

The ON-OFF switch on the interface itself may be turned ON or OFF when the interface is not in use. However, if there is another interface further out on the bus, the interface should be left ON in order to apply power to the priority logic.

A power supply schematic is in Appendix A; the manufacturer's data sheets in Appendix B.

Analog-to-Digital Conversion

The analog-to-digital conversion capability is almost identical to Data General's 12-bit A/D converter with their Basic A/D Interface, described in Section 6.1 of How to Use the Nova Computers [1].

To use the A/D converter:

1. The interface power should be ON.
2. Set the analog INPUT VOLTAGE range selector knob (labelled "INPUT VOLTAGE" on the front panel) so that the analog voltage to be input will always remain within the selected range.
3. Whenever the analog INPUT VOLTAGE full scale range is changed, the ZERO OFFSET trimmer potentiometer and the RANGE trimmer potentiometer need to be readjusted. Set the OFFSET BINARY-2's COMPLEMENT toggle switch to the OFFSET BINARY position, and follow the manufacturer's instructions on adjusting these trimmer potentiometers on page 3 of the Analogic data sheet attached in Appendix B.
4. Set the OFFSET BINARY-2's COMPLEMENT toggle switch to the desired position.
5. Connect the input voltage to the ANALOG IN coaxial connector.

The I/O instruction for the A/D converter has the same format as all Nova input-output instructions. (The reader may want to review at this time Section 2.3, "Input-Output," in How to Use the Nova Computers.) As in all I/O instructions, the Busy and Done functions are controlled by bits 8 and 9. The device code for the A/D ConVerter is 21_8; the mnemonic is ADCV. All of the program interrupt features of the Nova (interrupt request, priority, etc.) described under Section 2.4, "Program Interrupt," of How to Use the Nova Computers are implemented in the A/D converter interface. Interrupt

Disable is controlled by interrupt priority mask bit 8. The A/D converter follows the D/A converter on the interrupt priority chain but precedes the tape transport.

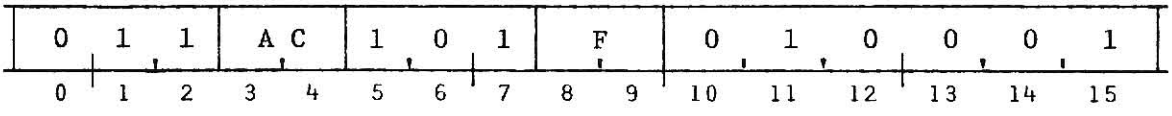
When the Start (S) command is issued, the Done flag is cleared, while the Busy flag is set. The Start command function can be coded as a mnemonic modifier or with a No Input-Output (NIO) instruction as NIOS. Setting the Busy flipflop starts the converter (if the PROGRAM START-TIMER START toggle switch on the front panel is in the PROGRAM START position). When one conversion has been completed, the Busy flipflop will be cleared and the Done flipflop set. The output from Done may either be sensed by a skip instruction or enable an interrupt request, depending on the control program structure. At this time the digitized output from the converter can be transferred into an accumulator by the Data In C (DIC) instruction. The digitized data is transferred into the computer as a 2's complement signed number or as an offset binary number, depending on the position of the OFFSET BINARY-2's COMPLEMENT toggle switch.

Placing the PROGRAM START-TIMER START toggle switch in the TIMER START position starts the converter in synchronization with a fixed time base. The Start (S) command must still be issued to set the Busy flipflop and clear the Done flipflop, thus permitting the A/D converter to clear Busy and set Done upon completion of the conversion. The setting of Done can then inform the control program of the completed conversion by a skip sense instruction or by an interrupt, depending on the program structure. The time base can be adjusted from 200 Hz to over 40 kHz by means of the two TIMER trimmer potentiometers, one of which is a coarse adjustment and the other fine. The time base can be monitored at the monitoring post located between the A/D converter's output lights and the D/A converter's input lights.

The Clear (C) modifier clears both Busy and Done. If the PROGRAM START-TIMER START switch is in the timer start position, the converter will continue converting in synchronization with the fixed time base, but there will be no effect on the Busy-Done flags as long as these flags have been cleared. The Pulse (P) modifier has no effect since the Data Channel is not implemented. Thus every conversion is under program control.

The format and function of the A/D converter interface instruction follows:

DIC -,ADCV Data In C, A/D Converter



Transfer the final value of the input analog sample as digitized by the converter from the interface into accumulator AC and perform the function specified by F. (The 12 A/D bits are placed in AC bits 0 through 11; bits 12 through 15 are cleared.)

Below is a sample program segment showing the use of the A/D converter interface instruction. The subroutine is entered after executing a JSR instruction in the main program.

```
        JSR     CNVRT           ;Get next quantized analog sample
        ---                     ;Return here with data in AC
        ---                     ;Continue program
CNVRT:  NIOS    ADCV            ;Start converter
        SKPDN   ADCV            ;Wait for end of conversion
        JMP     .-1
        DIC     AC,ADCV         ;Read converted data
        JMP     0,3             ;Return to main program
```

The Analogic converter on the interface can digitize a voltage to 12 bits in about 40 micro-seconds. To permit an even faster rate, the conversion speed trimmer potentiometer labelled "CLOCK" on the front panel can be adjusted. While performing the adjustment, the output of the Busy flipflop can be monitored on the monitor post next to the trimmer potentiometer. The Analogic data sheet (page 3) in Appendix B gives further information on the Conversion Speed Adjust.

An alternative way to digitze at a faster rate is to select an output word length of less than 12 bits by setting the OUTPUT WORD LENGTH selector knob on the front panel to the selected output word length. Monitoring the Busy flipflop output will indicate the effect of the shorter output word length.

The reader will notice from reading the Analogic data sheet that all the converter's possibilities have been implemented on the interface with the exception of Ratiometric A/D conversion and One's Complement Output.

Note 1: If an analog signal does not appear to be reaching the A/D converter, check the fuse on the input protection circuitry. The protection circuitry is quite sensitive and an accidental input voltage spike can activate the circuit and burn out the fuse.

Although the maximum correct input voltage is ± 10, the input is protected against higher voltages by a Zener diode and fuse circuit. Use only a Buss 1/200 amp or Buss 1/500 amp fuse for proper protection. A 1/200 amp fuse protects against voltages at least as high as 22 volts, while a 1/500 amp fuse protects against voltages at least twice that high.

Note 2: If the A/D interface "freeze's" up, such that the A/D converter does not respond to the SAMPLE button or the interface never goes Done, just toggle the RESET switch on the Nova front panel or execute a program IORST (I/O reset).

The setting of Done after each conversion is dependent on the arrival of the End Of Conversion (EOC) pulse from the A/D converter. If this pulse gets "lost," Done will never be set and the program

will wait forever for Done. There is one and only one way to "lose" the EOC pulse and that is to manually push SAMPLE at the same time a sampling program is executing. (Try it.) An IORST just resets all the flipflops including Done.

Digital-to-Analog Conversion

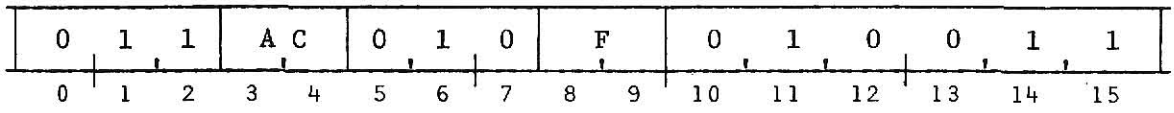
The digital-to-analog conversion capability differs from that of Data General in that only the D/A converter control and one D/A converter channel is supplied. Furthermore, unlike Data General, the Busy/Done logic has been completely implemented with interrupt, priority, etc.

The I/O instruction for the D/A converter has the same format as all Nova input-output instructions. The Busy and Done functions are controlled by bits 8 and 9. The device code for the D/A converter is 23_8; the mnemonic is DACV. Interrupt Disable is controlled by interrupt priority mask bit 7. The D/A converter has the first priority on the interrupt priority chain on the interface.

As soon as the offset-binary data is sent out to the D/A control by a DOA instruction, conversion starts immediately. When conversion is completed in 5 microseconds, the Busy flipflop is cleared, and, if the Busy flipflop had previously been set by the program, the Done flipflop is set. If the Busy flipflop had not been set, the completion of conversion has no effect on the Busy/Done logic. To set the Busy flipflop, a Start (S) command is issued, which also clears Done. The Start command can be coded as a mnemonic modifier or with a NIO instruction as NIOS. The output from the Done flipflop may either be sensed by a skip instruction or enable an interrupt request depending on the control program structure. The Clear (C) modifier clears Busy and Done, while Pulse (P) has no effect.

The format and function of the D/A converter interface instruction follows:

DOA -, DACV Data Out A, D/A Converter



Load the digital data word from accumulator AC into the D/A converter. Conversion starts automatically and immediately after data has been loaded. (AC bits 0 through 11 are converted; bits 12 through 15 are ignored.)

Below is the previous sample program segment modified to send back out the digitized data as an analog voltage again immediately after each A/D conversion.

```
        JSR     CNVRT           ;Get next quantized analog sample
        ---                     ;Return here with data in AC
        ---                     ;Continue program
CNVRT:  NIOS    ADCV            ;Start converter
        SKPDN   ADCV            ;Wait for end of conversion
        JMP     .-1
        DIC     AC,ADCV         ;Read converted data
        DOA     AC,DACV         ;Send back out as an analog voltage
        JMP     0,3             ;Return to main program
```

Output voltage ranges of -5 to +5 volts, -10 to +10 volts, and 0 to +10 volts may be selected by the OUTPUT VOLTAGE selector knob on the front panel. Whenever the output voltage is changed, the ZERO OFFSET and the RANGE should be readjusted according to Table 2 through 4 in the Zeltex data sheet attached in Appendix B.

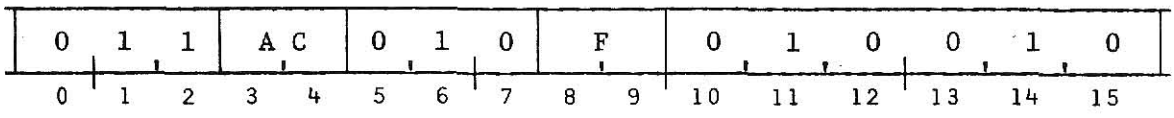
Incremental Write/Synchronous Read Tape Transport

The PEC tape transport capability differs considerably from that supplied by Data General. Not only is the tape transport incremental in the write mode, but the interface control logic has been minimized. As a result, few control functions are done automatically in this interface, but must be performed by the program. Section 3 of the PEC manual 1000/2000 Series Incremental Write/Synchronous Read Tape Transport [2] should be consulted for the operation of the tape transport, while this section will completely explain the use of the interface control.

The magnetic tape system uses four of the I/O transfer instructions. Busy and Done are controlled by bits 8 and 9 as in all I/O instructions. The device code for the tape transport is 22_8; the mnemonic is MTA. All of the program interrupt features of the Nova (interrupt request, priority, etc.) described under Section 2.4, "Program Interrupt," of How to Use the Nova Computers are implemented in the tape transport interface. Interrupt Disable is controlled by interrupt priority mask bit 10. The tape transport is last on the interrupt priority chain on the interface, since it is generally slower than the A/D or the D/A converter.

Tape movement, selection of the Read or the Write mode, and other control functions are each determined by a bit in the command register. The commands in the register are executed immediately upon each execution of the following instruction:

DOA -,MTA Data Out A, Magnetic Tape



Load the contents of AC bits 0-10 into the tape command register as shown, and perform the function specified by F. (Bits 11-15 are ignored.)

Tape Command Register

IRG	RESET	ECR	DISABLE	SPC	SRC	REWIND	DENSITY	FGC	LFC	W/R
0	1	2	3	4	5	6	7	8	9	10

A complete description of the interface commands are given in the PEC manual (Section 3) but a summary of each command bit follows:

Bit

0 If the INTER-RECORD GAP COMMAND (IRG) bit is a "1", the DOA command initiates the sequence of events necessary to generate an IBM-compatible Inter-Record Gap. If the bit is a "0", the DOA command has no effect.

1 If the REMOTE RESET is a "1", the DOA command resets all relevant flipflops in the tape transport control logic. If bit 1 is a "0", the DOA command has no effect.

2 If the ECHO CHECK RESET Command (ECR) bit is a "1", and if the transport is ready, the DOA command causes the Echo Check Error flipflop to be held reset. If the bit is a "0", the Echo Check Error flipflop is no longer held reset.

3 If the DISABLE MANUAL CONTROLS bit is a "1", the DOA command disables the manual controls. If the bit is a "0", the DOA command enables the manual controls.

4 If the SYNCHRONOUS FORWARD Command (SFC) bit is a "1" and the transport is ready, the DOA command causes tape to move forward at a constant velocity. If the bit is a "0", the DOA command causes the synchronous forward motion to stop.

Bit

5 If SYNCHRONOUS REVERSE Command (SRC) bit is a "1", and the transport is ready, the DOA command causes tape to move in the reverse direction at a constant velocity. If the bit is a "0", the DOA command causes the synchronous reverse motion to stop.

6 If the REWIND Command bit is a "1", the DOA command causes the tape to move in the reverse direction at 50 inches per second (ips). Upon passing the Beginning Of Tape (BOT) marker, the tape drive ceases and the tape decelerates to rest. If the bit is a "0", the DOA command has no effect.

7 The DATA DENSITY SELECT bit has no effect whatsoever in a 9-track transport, such as the one belonging to KSU.

8 If the FILE GAP Command (FGC) bit is a "1", the DOA command initiates the generation of a 3.8 inch IBM-compatible gap. The File Mark and its associated Longitudinal Redundancy Check Character (LRCC) are written in this gap. If this bit is a "0", the DOA command has no effect.

9 If the LOAD FORWARD Command (LFC) bit is a "1", the DOA command causes the tape to move forward at 12 ips. When the BOT tab reaches the photosensor the tape stops. Since the tape stops in the Read mode somewhat in advance of where it stops for the Write mode, so as to read the very first data, the program should establish the Read/Write mode simultaneous with the Load Forward Command. If a "0" is issued and then a "1" again, forward motion resumes. Tape motion stops when bit 9 is a "0" and a DOA command issued.

Note: An interface LFC bit once turned on by a DOA instruction, stays on until another DOA puts a "0" in bit 9 of the transport

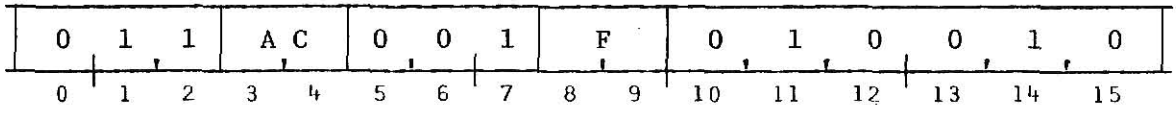
interface's command register. Thus, if the transport brings the tape to an automatic stop at the BOT, the interface Load Forward Command is still on. Since it is necessary to turn the command off and then back on to resume Load Forward motion; a DOA instruction has to first place a zero in the LFC bit 9, before a second LFC, manual or through the interface, can cause the Load Forward motion to resume.

10 If the WRITE/READ STATUS (W/R) bit is a "1", the DOA command establishes the transport in the Write mode; if the bit is a "0" the DOA command establishes the transport in the Read mode.

It is clear that several commands can be given with a single DOA command. Care should be exercised not to give a contradictory command such as a simultaneous Rewind and Load Forward.

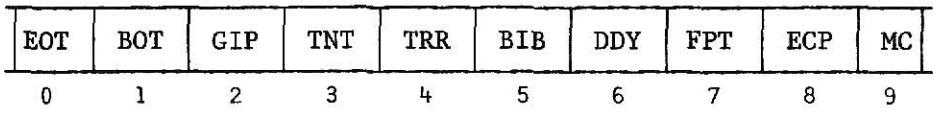
To determine the status of the tape transport, the following instruction is executed:

DIA -,MTA Data in A, Magnetic Tape



Read the status of the tape system into AC bits 0-9 as shown and perform the function specified by F. Clear bits 10-15.

Status Register



A complete description of the interface status bits are given in the PEC manual (Section 3) but a summary of each status bit is as follows:

Bit

0 The END OF TAPE (EOT) bit goes to "1" when the EOT tab is being detected. When the tab moves away from the detector, the bit goes back to "0".

1 The BEGINNING OF TAPE (BOT) bit goes to "1" when the BOT tab is being detected. When the tab moves away from the detector, this bit goes back to "0".

2 The GAP IN PROGRESS (GIP) bit goes to "1" when an IRG, File Gap or BOT sequence is in progress. The bit goes back to "0" when the sequence terminates.

3 The TAPE NOT TENSIONED (TNT) bit goes to "1" when the tape storage arms are not in the nominal operating position. The bit is "0" when the arms are in operating position.

4 The TRANSPORT READY (TRR) bit is "1" when the tape transport is in a condition to receive or transmit data. The bit is "0" when the transport is not ready.

5 The BUFFER 1 BUSY (B1B) bit is "1" as long as there are data to be recorded present in the transport's buffer system. The buffer stays full when the transport is writing at the maximum rate of 700 samples per second.

6 The DATA BUSY (DBY) bit is "1" when the transport is in the Write mode. When the transport is switched to the Read mode, a delay occurs prior to the DATA BUSY bit going false.

7 The FILE PROTECT (FPT) bit is "1" when power is on and a reel of tape, without a Write Enable ring installed, is mounted on the transport.

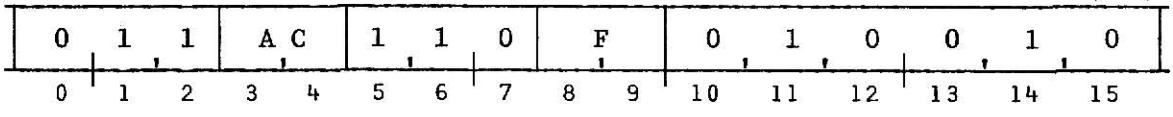
Bit

8 The ECHO CHECK PARITY ERROR (ECP) bit is "1", when a parity error in the echo check output is detected. This bit must be reset by the user with the ECHO CHECK RESET command.

9 The MOTION CHECK (MC) bit goes from "1" to "0" whenever the capstan shaft rotates through one bit space.

The data to be written is sent to the interface buffer upon execution of the following instruction:

DOC -,MTA Data Out C, Magnetic Tape



Load the contents of AC bits 0-7 into the write buffer, and perform the function specified by F. (AC bits 8-15 are ignored.)

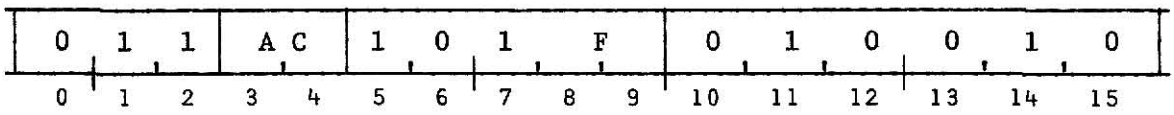
When the Start (S) command is issued, the Done flag is cleared, while the Busy flag is set. The Start command function can be coded as a mnemonic modifier or with a NIO instruction as NIOS. If the transport is in the Write mode, the setting of the Busy flipflop, cause the eight bits to be written. (A parity bit, a ninth bit, is automatically written by the transport as bit 8.) When the byte has been written, the Busy flipflop will be cleared and the Done flipflop set. The output from Done may either be sensed by a skip instruction or enable an interrupt request depending on the control program structure. The Clear (C) modifier clears Busy and Done, while Pulse (P) has no effect.

A typical write program segment follows:

```
CONST:  40                      ;A "1" in bit 10 for Write mode
        LDA     0,CONST         ;Put transport in Write mode
        DOA     0,MTA
        ...                     ;Get data and put in AC 1
        ...
        ...
        ...
        DOCS    1,MTA           ;Send data to interface and write it
        .
        .
        .
```

Data is read from the tape, when the transport is in the Read mode and is in synchronous forward or synchronous reverse motion, upon execution of the following instruction:

DIC -,MTA Data in C, Magnetic Tape



Transfer data bits 0-7 and parity bit 8 to AC bits 0-8 and perform the function specified by F. Clear AC bits 9-15.

If the Busy flipflop is set by the program, Busy will be cleared and Done set when the data is available for reading. Done may then be sensed by a skip instruction or an interrupt, just as in the write mode. (In fact, the same flipflops are used for Read as for Write.)

A typical read program segment follows:

```
CONST:  4000                ;A "1" in bit 4 for Synchronous Forward
        ...                 ;   and a "0" in bit 10 for Read mode
        ...
        ...
        LDA     0,CONST     ;Send command to transport
        DOAS    0,MTA       ;   and set Busy
NEXT:   SKPDN   MTA         ;Wait for data
        JMP     .-1
        DICS    1,MTA       ;Get data and set Busy again
        .                   ;Have 50-60 microseconds before the next data
        .                   ;   arrive
        .
        JMP     NEXT        ;Go read next data
```

Note: The transport must be ready and in the Read mode to get a Read Data Strobe (RDS) pulse. This pulse is used to set Done to inform the program that the next byte is available for reading. Thus, if the transport is not ready or is in the Write mode, the synchronous forward or reverse motion will be present, but no RDS pulse and no setting of Done.

CHAPTER III

INTERFACING A NOVA

Chapter Objective

A prerequisite to a good understanding of this chapter is a general understanding of interfacing any small computer obtained, for example, from section 6-7, "Interfacing a Small Computer," in John B. Peatman's book, The Design of Digital Systems [3]. In addition, a preliminary reading of the "Input-Output" and "Program Interrupt" sections of How to Use the Nova Computers will indicate the requirements placed upon the I/O logic design by the Nova programming structure or software. The material in this chapter can then be used to design and implement specific Nova interfaces.

A subsequent study of Appendix A of How to Use the Nova Computers will have fully equipped the reader to successfully design and build his own interfaces for the Nova. Specific examples of interfaces for three devices: analog-digital, digital-analog, and an incremental write/synchronous read tape transport follow in the next chapter.

I/O Bus

A commonly employed method for a computer to communicate with peripheral devices, I/O devices in particular, is the use of a group of conductors, called a bus, that run to every device and that carry electrical signals among the components of a computer system. The Nova bus carries to every peripheral:

1. Sixteen bidirectional data lines $\overline{\text{DATA15}}$ ... $\overline{\text{DATA0}}$,
2. Six device selection lines from computer to devices $\overline{\text{DS5}}$ ... $\overline{\text{DS0}}$,
3. Nineteen control lines from processor to devices such as, for example, the Start command,
4. Six control lines from devices to processor such as, for example, the Interrupt Request ($\overline{\text{INTR}}$).

Since the same bus lines run to every peripheral device and each peripheral is different at least in its device selection code (for example, primary disk and secondary disk), each peripheral must have a control or interface between the bus and itself as illustrated in Fig. 3-1. As shown, some controls can fit inside the computer mainframe. For additional controls, the bus can be extended to form an external bus as has been shown for the A/D, D/A, and PEC tape transport controls.

When an external bus is connected, those control signals that originate in the processor and that drive devices must be terminated as shown in Fig. 3-2. The signal receivers are often inverters such as the one shown. The voltage divider circuit at the end of each bus line gives the correct termination. Note that each bus line is a twisted pair.

Bidirectional signals, such as the data lines, and signals from devices to processor, such as Interrupt Request, must be terminated as in Fig. 3-3.

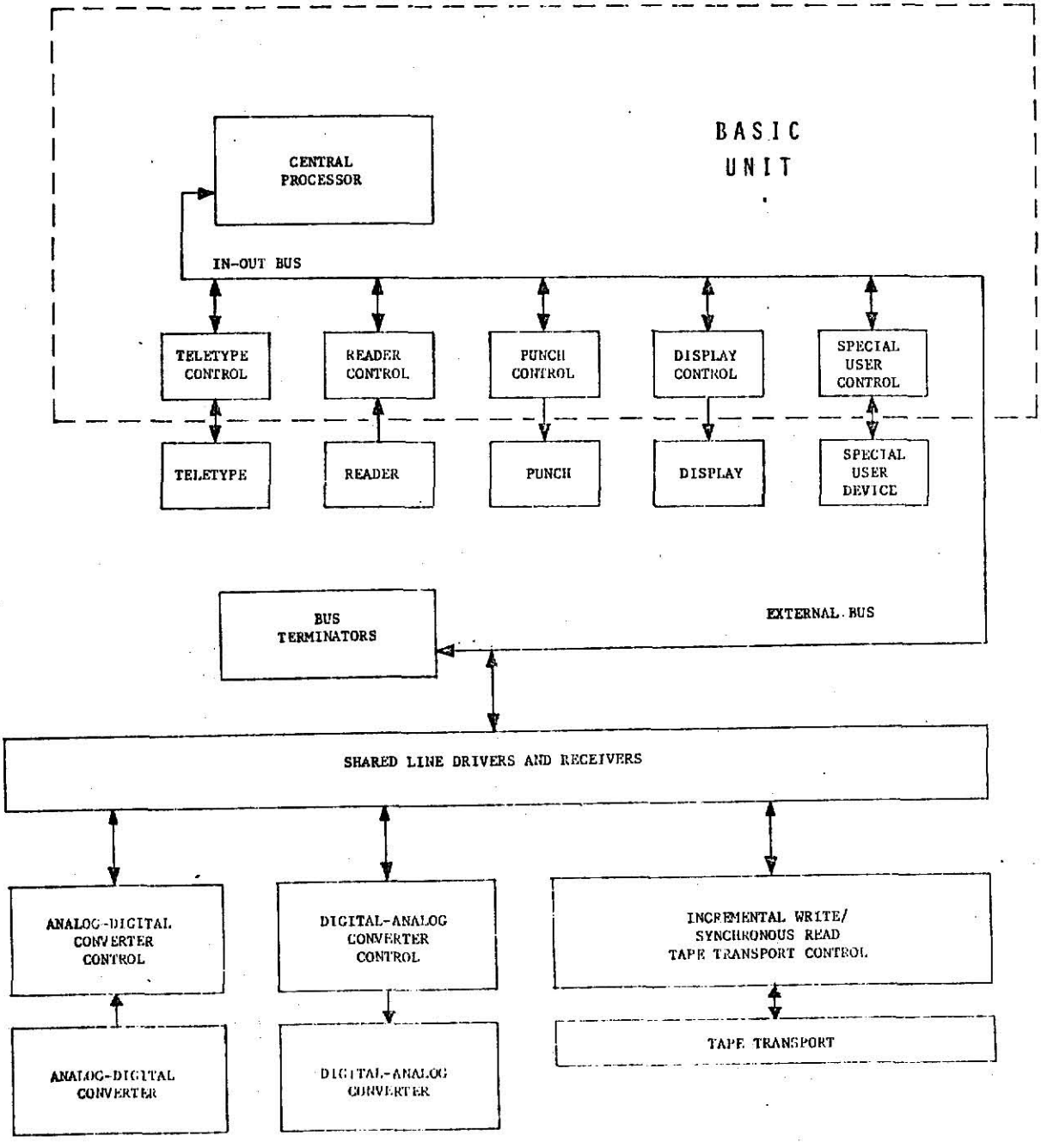


Fig. 3-1. Nova System Configuration.

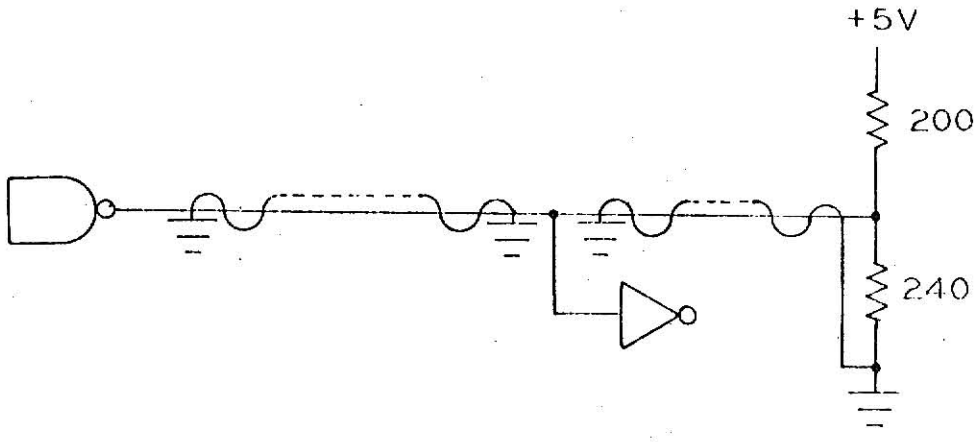


Fig. 3-2. Termination for an external bus line from processor to device.

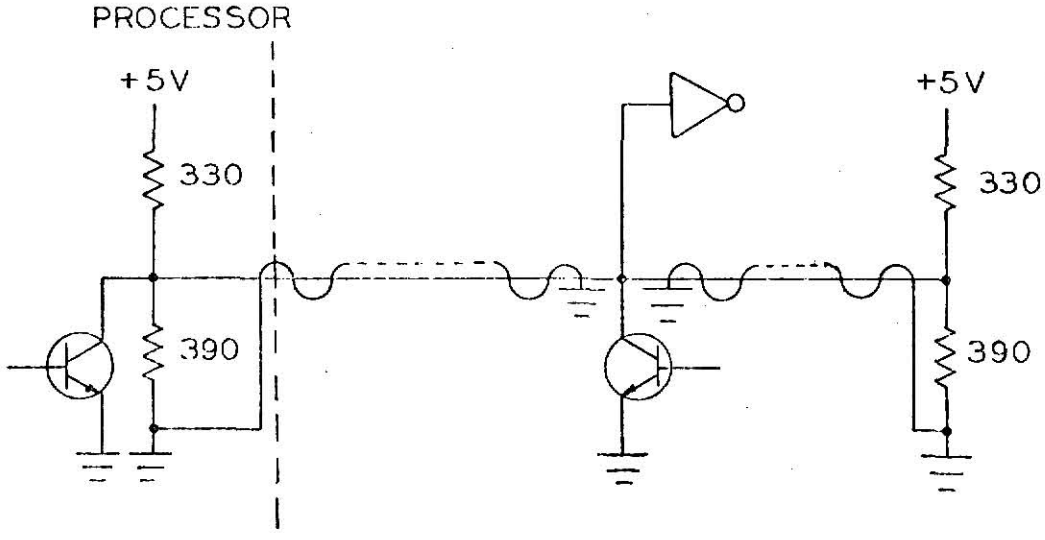


Fig. 3-3. Termination for an external bidirectional bus line or for an external bus line from device to processor.

The receivers of those signals are again often inverters. Since the line is pulled low to put a signal on the line, the output transistor of an open collector gate, such as the SN7438 is shown for the line transmitter. When all the collector transistors on the bus are off, no signal is on the line and the 330 ohm load resistor pulls the line high to 2.7 volts as determined by the voltage divider.

Additional information on bus lines, such as decoupling the +5 volts can be found in Chapter V, "Noise Considerations," of Texas Instruments' book Designing with TTL Integrated Circuits [4].

Bus Receivers

Since it is good practice to minimize the load on each bus line, Data General Corporation terminates each bus line only once per subassembly board with a receiving gate, usually an inverter. From the receiver, the signal may then branch out to other gates or even other interfaces on the same board, as seen in the case of the Device Select lines $\overline{DS0}$ ... $\overline{DS5}$ in Fig. 3-4. (The bar over a signal name means that the signal is on when the line is pulled to a low voltage.)

Note: Within the mainframe of most of their computers, Data General replaces the inverter receiver on certain bus lines with a filter and gate, as shown in Fig. 3-5. This is done to improve noise margins. Note that the lower input filters out the high frequency noise, since the capacitor cannot charge up fast enough to give the second logical 1 input.

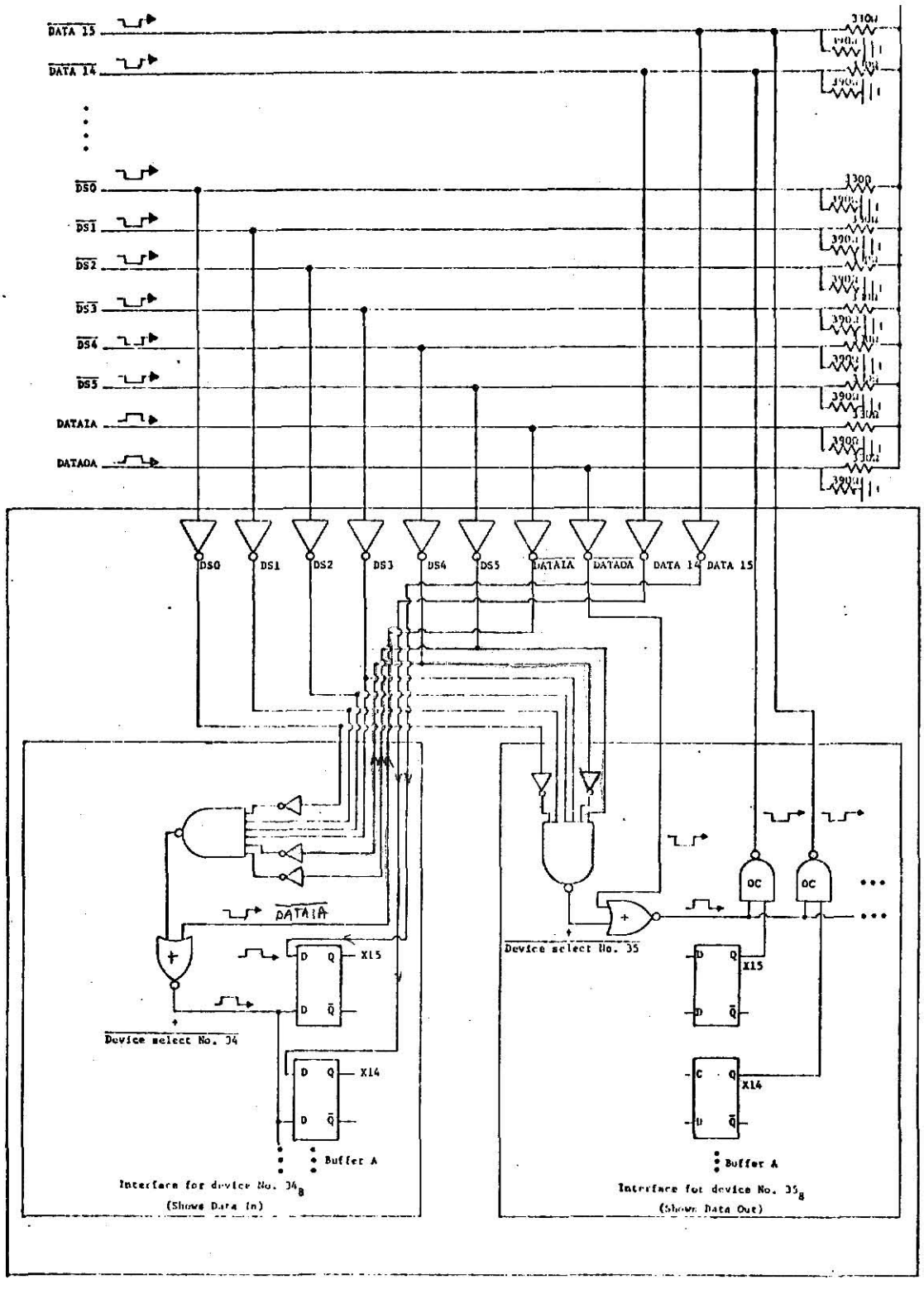


Fig. 3-4. Interface subassembly that holds more than one interface per board.

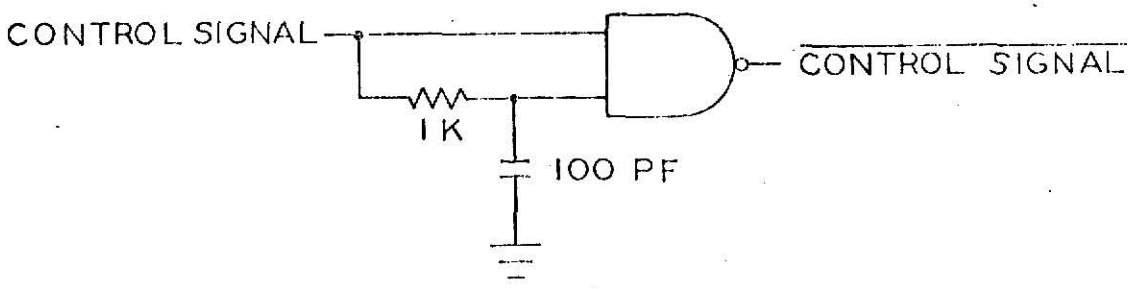


Fig. 3-5. The receiver for some control signals.

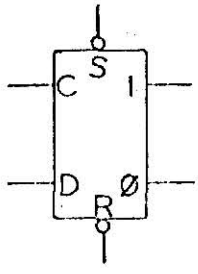


Fig. 3-6. A D-flipflop.

Device Selection and Data Transfer

Figure 3-4 also shows that those control signals such as Data In A (DATIA) which should affect only the one device addressed must be gated with a device select signal derived from the device select bus lines. Note that a Nor gate can perform as a negative logic AND gate: Both inputs must be logical 0 to output a logical 1. The three Data In lines (DATIA, DATIB, DATIC) input data from one of three interface registers into the central processor, while the three Data Out lines (DATOA, DATOB, DATOC) output data to interface registers. A DATIA and a DATOA are shown in Fig. 3-4. Timing of the data transfer is handled by the signals on the bus lines -- taken care of by the manufacturer.

D-Flipflops

The standard control flipflop used in Nova interfaces is the type D flipflop of Fig. 3-6. When the D input is high, the leading edge of a positive pulse at C sets the 1 output high and the complementary output Ø low. A low D input resets the 1 output to a low voltage at a positive transition of C. A ground level at S or R sets or resets the flipflop respectively, regardless of the clocked input. A small circle at the D input implies that the flipflop is set when D is low, cleared when D is high; or in other words, the set or clear condition is interpreted in terms of the Ø output rather than the 1 output (see the DEV INT REQ flipflop in Fig. 3-8). A typical control flipflop is the SN 7474.

Interrupt Request

The flipflop control network in the device interface that specifies the state of the device and requests interrupts contains four flipflops (Busy, Done, Interrupt Disable, and Interrupt Request). Busy and Done are shown in Fig. 3-7. When a device is ready for service, it sets a Done flipflop in its interface. The computer can learn of the device's need for service by periodically checking the Selected Done ($\overline{\text{SELD}}$) line which is brought low when the device's Done flipflop and its device select line are both on. A skip-on-done instruction in the program can initiate this check. The computer can alternatively learn of the need for service by an interrupt. During each processor cycle, at a time when the computer is ready to be interrupted, the Request Enable (RQENB) line is pulsed. One or more devices needing service will then pull the Interrupt Request (INTR) line low.

When interrupted, the program can run through a chain of skip-on-done instructions to determine which device needs service. Alternatively, the program can issue an Interrupt Acknowledge (INTA) instruction so that the device interface places on the data lines $\overline{\text{DATA10}}$ - $\overline{\text{DATA15}}$ the device code of the device needing service. The device code of the device in Fig. 3-7 is 65_8.

Note that a particular device code goes on the data lines only if:

1. An Interrupt Acknowledge (INTA) is issued
2. The device is requesting an interrupt
3. As explained below, it is the physically closest device to the computer which needs servicing.

The Interrupt Priority In line ($\overline{\text{INTP IN}}$) entering an interface is low if no previous device needs service. If the device does not need service, the Interrupt Priority Out ($\overline{\text{INTP OUT}}$) line goes out low again to the next

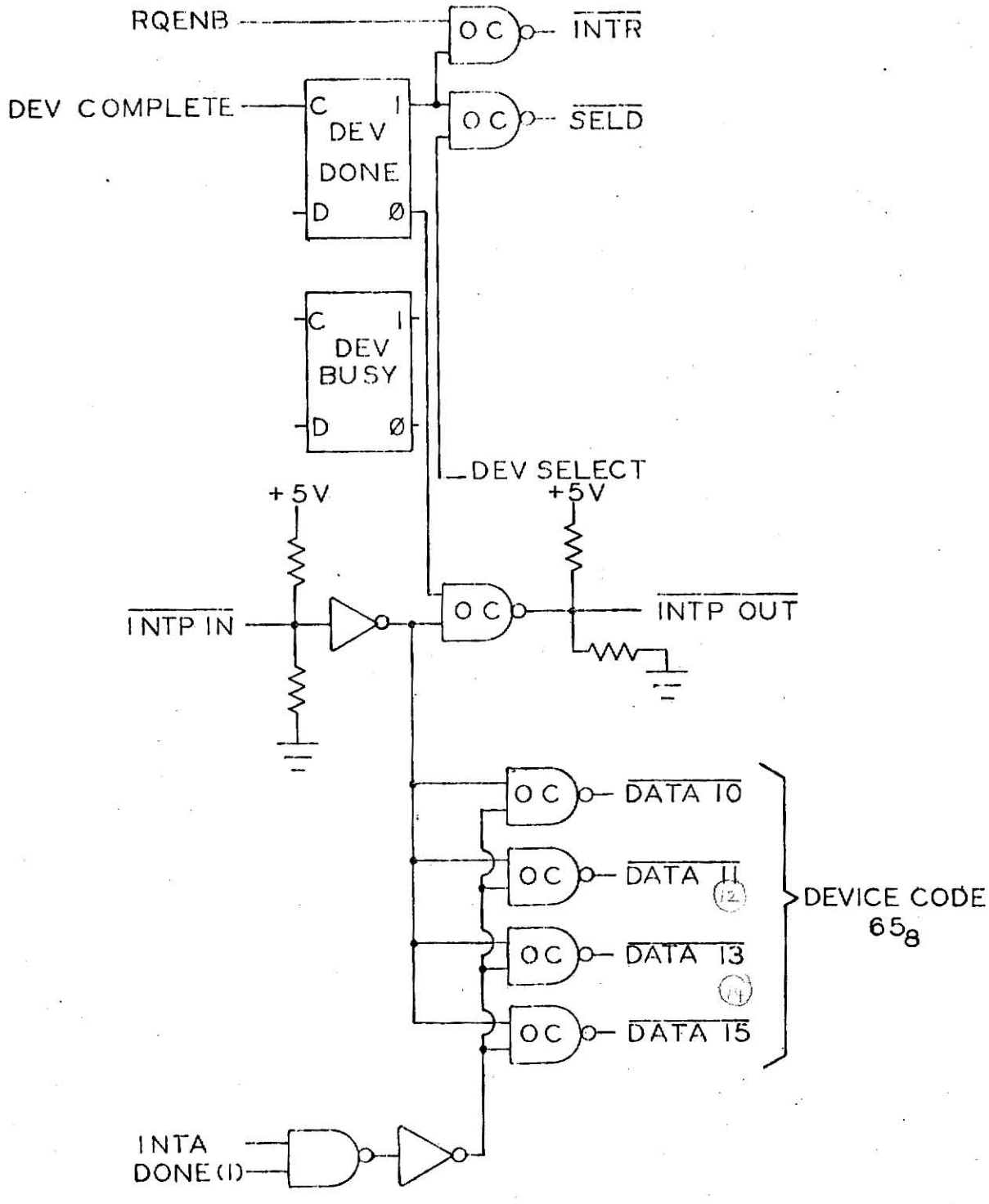


Fig. 3-7. Initial interrupt design.

interface. On the other hand, if the device is Done, the Interrupt Priority Out ($\overline{\text{INTP OUT}}$) goes out high, and the Interrupt Priority line goes in high and out high at every remaining interface on the bus. As a result, only the interrupting device closest physically to the Nova is permitted to place its device code on the data lines $\overline{\text{DATA10}}$ - $\overline{\text{DATA15}}$, for the DEV INTP signal will be low in all interfaces having $\overline{\text{INTP IN}}$ high. The voltage divider terminators shown are necessary only where the priority signal goes in and out of a subassembly board. Usually several interfaces are on a single board, and the single stage shown is replaced by a chain with terminators at each end.

The reader may have noticed a fault in the initial design of Fig. 3-7. This occurs when an additional device of higher priority (physically closer to the computer) goes Done at the same time an Interrupt Acknowledge is putting the first device's code on the data lines $\overline{\text{DATA10}}$ - $\overline{\text{DATA15}}$. Since the gates on the interrupt priority chain will then be in the process of passing along the new priority signal, it will be uncertain as to what device code goes on the lines. Placing an Interrupt Request (INT REQ) flipflop (Fig. 3-8) between the output from the Device Done flipflop and the Device Interrupt Request (INTR) insures that the only device interface placing its device code on the data lines is that device that had priority at the time of the latest Request Enable pulse.

Figure 3-8 also includes a device Interrupt Disable flipflop controlled by the Mask Out bus line and a selected data bit. Placing a logical 1 in an accumulator at that bit position and executing a Mask Out instruction prevents that device from interrupting the computer. The priority of the devices on the bus can thus be changed. The 16 data bits are each assigned

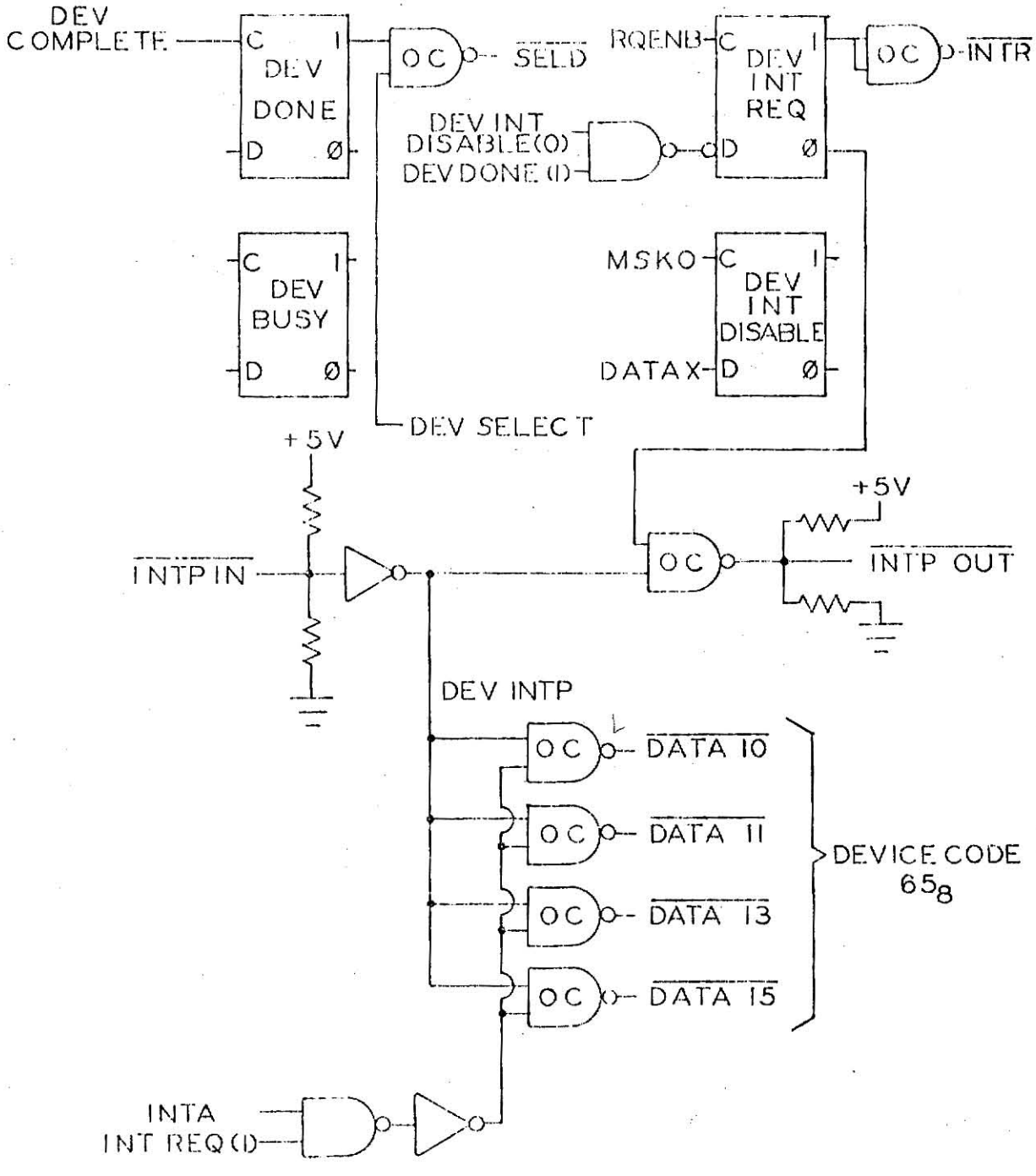


Fig. 3-8. Revised interrupt design with Interrupt Request and Interrupt Disable flipflops.

to one priority group and several groups can be masked out at a time. The priority of devices within a group cannot be changed.

Since a device can be in three states, Idle, Busy, or Done, these states are represented by two flipflops, Busy and Done, as follows:

Busy	Done	
0	0	device is idle
1	0	device is busy
0	1	device is done
1	1	not used

The setting of Busy by the program starts the device. (Done is cleared automatically.) The completion of the device operation clears Busy and sets Done. The program idles the device by clearing both Busy and Done.

Figure 3-9 includes the remaining Busy/Done Control signals. The I/O Reset (IORST) signal, generated by the I/O Reset instruction or the console reset switch, resets all interface flipflops and is connected in all interfaces to all four flipflops either directly or through OR-function gates. (Remember that some of the Nand gates in Fig. 3-9 perform inverted input OR functions: The output is high if either or both inputs are low.) The Clear line is ORed with the I/O Reset and, when activated by a Clear instruction, clears all the flipflops except Device Interrupt Disable. The Start line, activated by the Start instruction, clears Done and Device Interrupt Request and sets Busy to restart the device. The Start and Clear lines are gated with the device select output so that only the one device selected can be started or cleared at a time. The reader should remember that all the control signals such as Start, Clear, I/O Reset, and Request Enable, usually do not come directly from a bus line but indirectly through a set of receivers shared by all interfaces on a subassembly board.

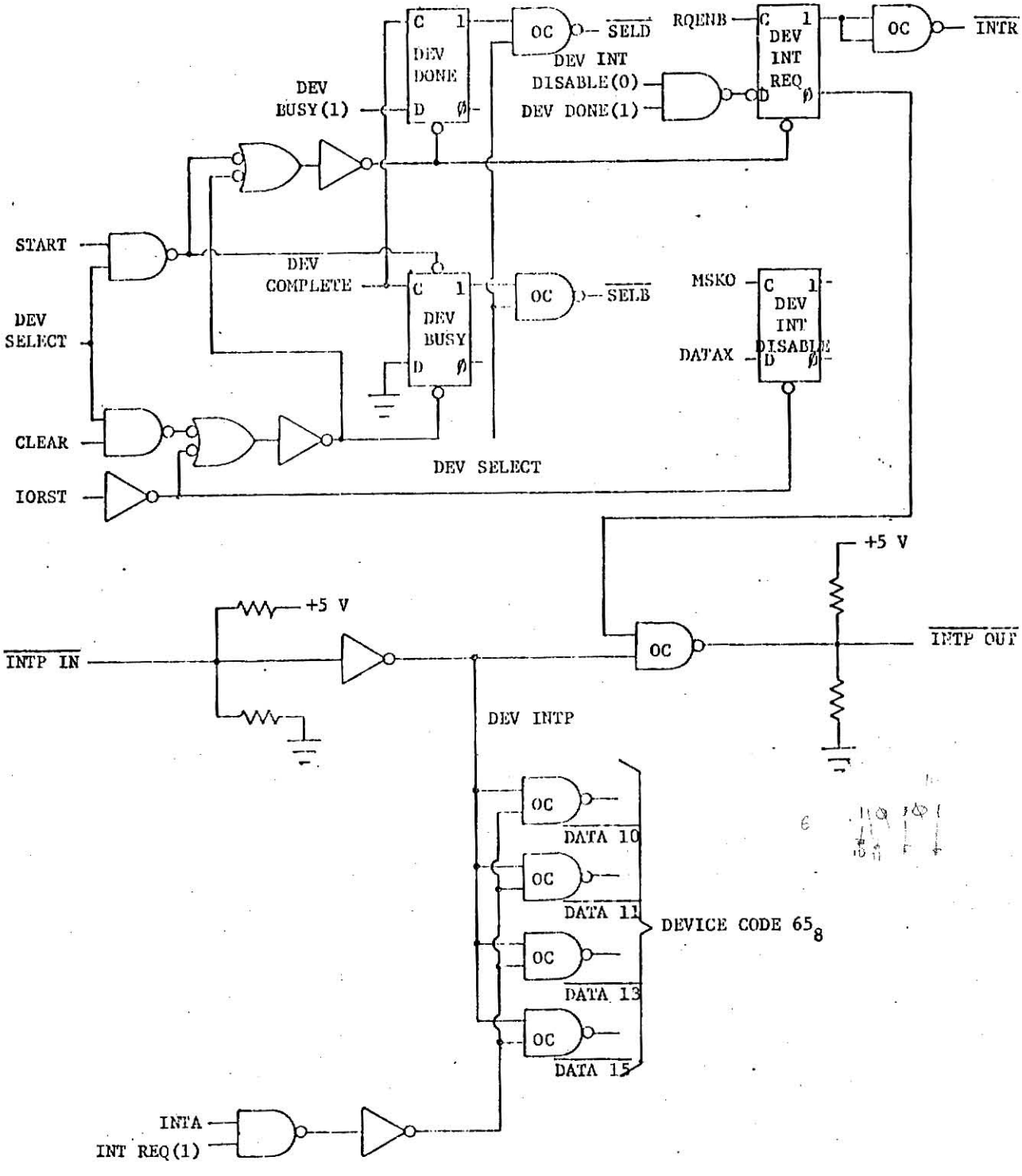


Fig. 3-9. Final interrupt design with Busy/Done logic completely implemented.

With the Busy/Done and interrupt logic just described, the computer is interrupted for each data transfer. To minimize lost processing time in going through an interrupt service routine, a block of data may be transferred per interrupt directly to or from memory by use of the data channel. The data channel logic, which is very similar to the Busy/Done and interrupt logic, handles the data transfers within a data block, while the interrupt system interrupts the computer at the end of each block transfer. To keep track of the number of words within a block that have already been transferred, a word counter register must be added. An address register keeps track of the next available memory location. See Appendix A of How to Use the Nova Computers for the complete details.

CHAPTER IV

THREE INTERFACES

Introductory Remarks

This chapter presents the design details related to three interfaces which were actually constructed. These interfaces are as follows: an analog-to-digital converter control, a digital-to-analog converter control, and a PEC tape transport control. The reader may wish to periodically examine the related circuit diagrams presented in Appendix A in order to get an idea of the actual implementation.

The Shared Logic

As shown earlier in Fig. 3-1, the three interfaces are connected to the external bus through a single set of shared bus drivers and receivers. Although it is not necessary to share the bus drivers, it is definitely advantageous to share the receivers wherever possible, so as to minimize the load each bus line has to drive.

A single receiver, composed of an inverter or the filter and Nand gate combination of Fig. 3-5, terminates each data line or each control signal from the computer to the three interfaces. On the other hand, each bus driver receives its input from a gate that ORs together either data signals or device-to-computer control signals from the three interfaces. Fig. 4-1 shows a bus driver and receiver for a typical data bus, while Fig. 4-2 shows a driver for a typical device-to-computer control signal.

Since an Interrupt Acknowledge instruction places a device code on the data bus lines $\overline{\text{DATA10}}$ - $\overline{\text{DATA15}}$, there is an additional input to some of the drivers of these six bus lines. The device codes of the A/D converter, the

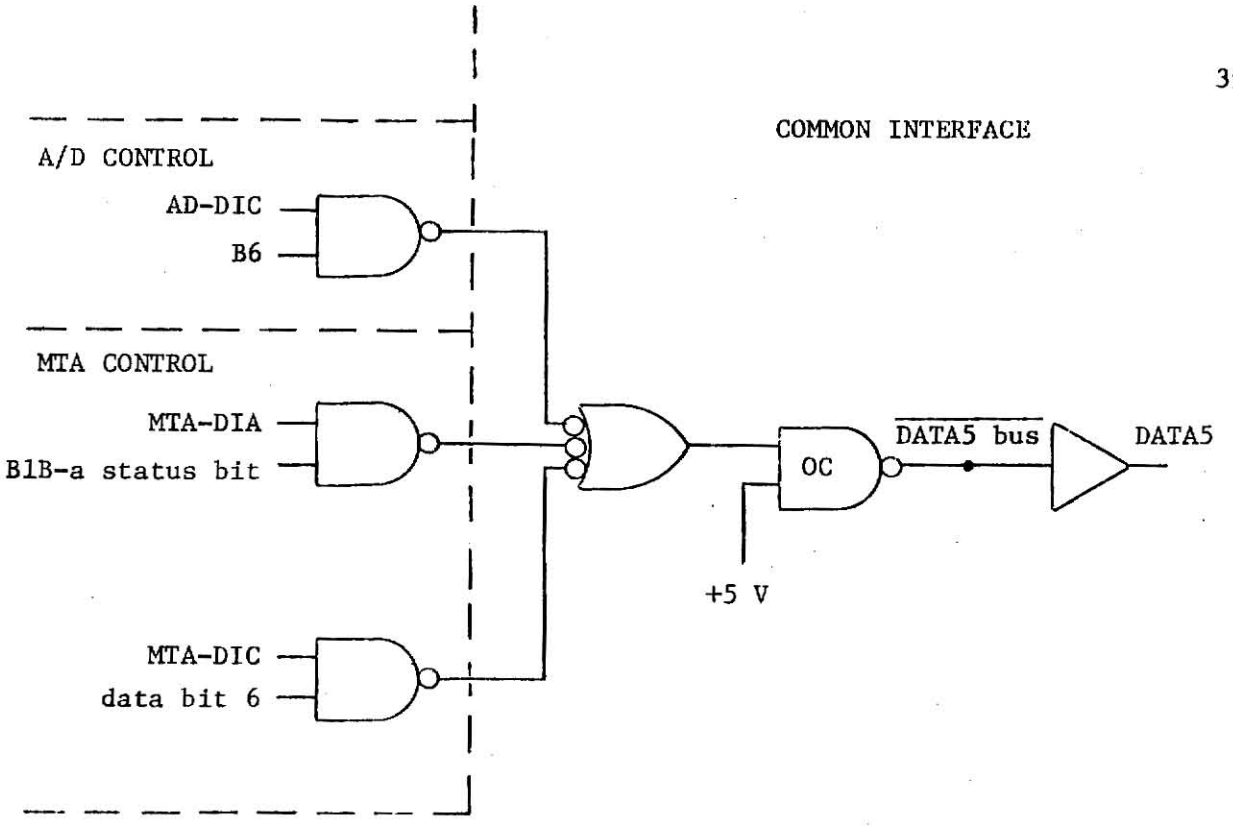


Fig. 4-1. A typical shared data bus driver and receiver.

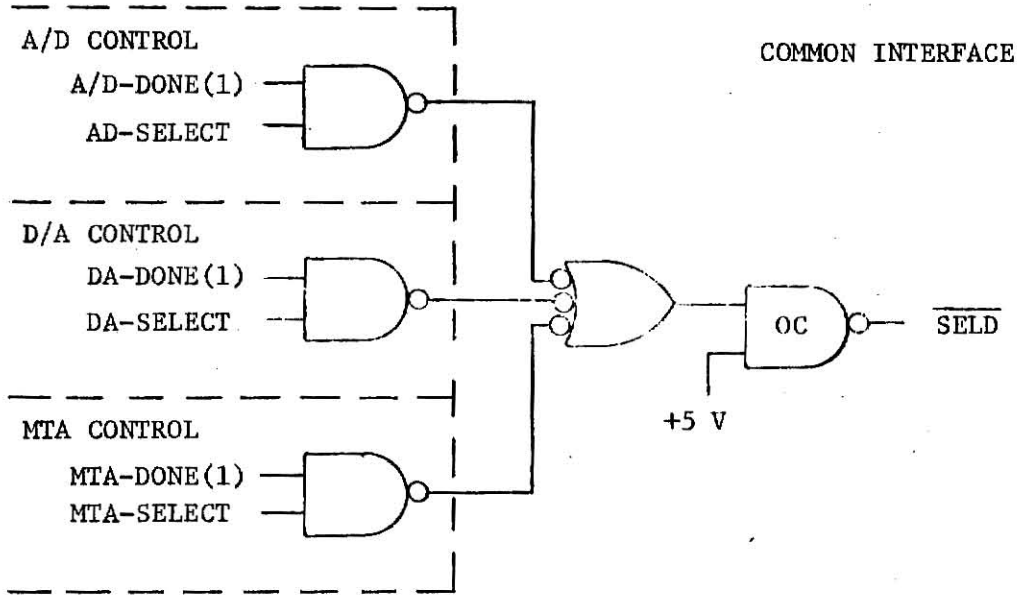


Fig. 4-2. A typical shared driver for a control bus line from the interface to the computer.

D/A converter, and the tape transport are respectively, 21_8, 23_8, and 22_8. Thus, for these interfaces $\overline{\text{DATA11}}$, $\overline{\text{DATA14}}$, and $\overline{\text{DATA15}}$ only are affected. To put the correct device codes on the data lines, each device ANDs the INTP IN signal from its portion of the priority chain with the INT REQ(1) output from its Interrupt Request flipflop, as shown for $\overline{\text{DATA11}}$ in Fig. 4-3. Each of the three resulting signals are brought from their respective interfaces to the common logic, where they are appropriately ORed together for each data bus, so as to turn on the correct bus lines for all the device codes. Gating these code signals with the INTA control signal enables the Interrupt Acknowledge instruction to determine the time when a device code goes on the six low order data lines.

From the common interface, the shared control logic branches out to the separate interfaces. Some of the control signals, such as Start, Clear, and Data In or Out refer to only one device at a time. Thus, these must be gated in each interface with a device select code developed from the six Device Select lines by an 8-input Nand gate. The control signals, both those gated with a device select code and those that are not, control the Busy/Done logic and the input-output of data in each interface. Occasionally, when the fanout from a control signal's gate would exceed 10 loads, a second identical gate is used for the same control signal. This is done in order to keep the load on each gate within the maximum limit. An example of a duplicated control signal gate is the added Data In C gate in the A/D converter interface. Attention will now be focused on the unique aspects of each interface.

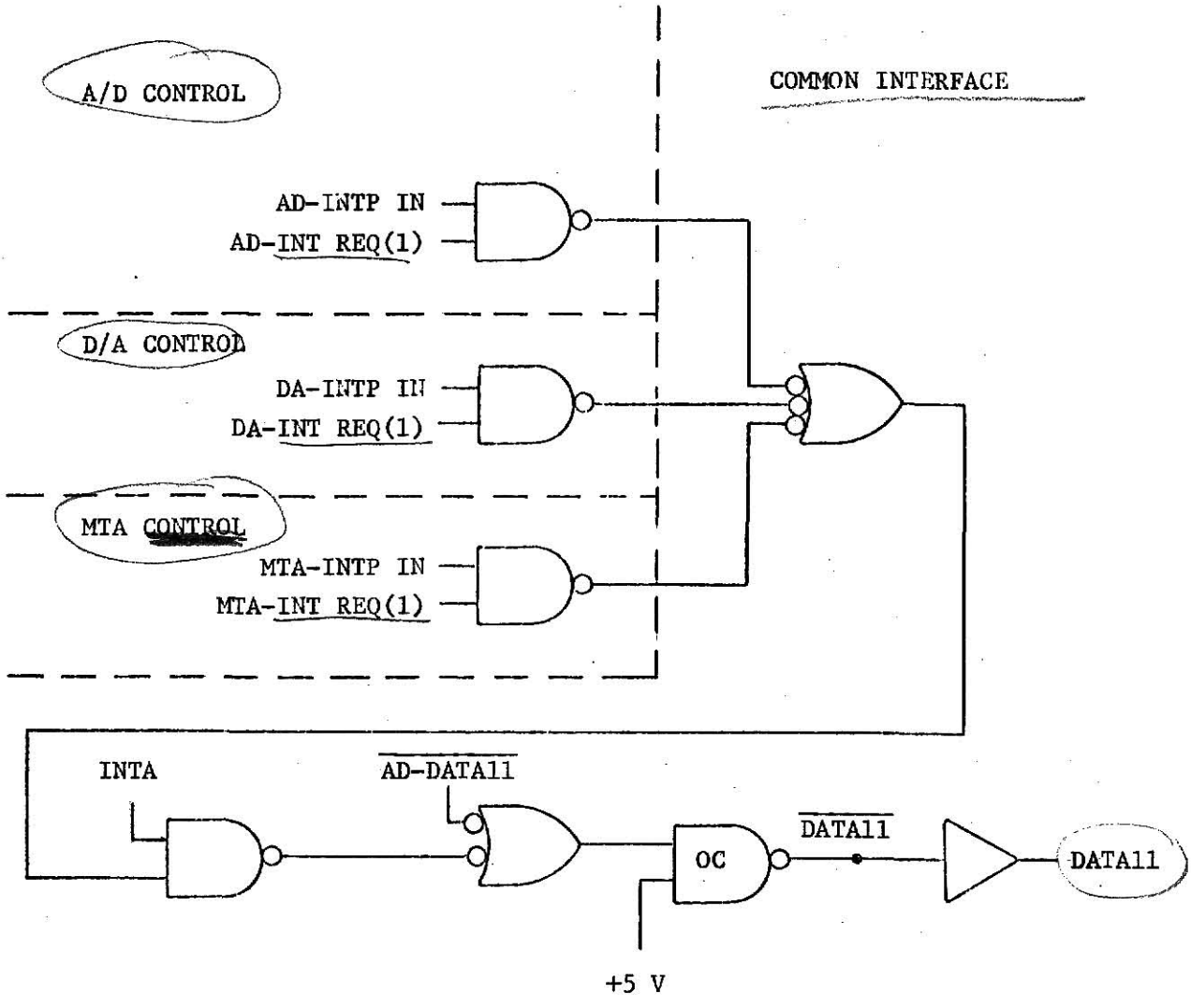


Fig. 4-3. A data bus that also carries a device code bit.

Analog-to-Digital Control

Since the setting of the Busy flipflop with a Start function should start the A/D converter, the output of the Busy flipflop must trigger the A/D converter. The minimum pulse width required by the Analogic converter for leading edge triggering is 50 nanoseconds; see Fig. 3 of the Analogic data sheet in Appendix B. Thus, to obtain the desired negative going pulse which has a duration of 50 nanoseconds, the invertered output from the Busy flipflop is connected to one of the low voltage OR inputs of a N74121 monostable; see Fig. 4-4. The other OR input is grounded by the SAMPLE pushbutton for manual sampling. The negative going output pulse from the monostable's complementary output triggers the A/D converter at the converter's TRIG IN pin.

At the start of conversion, the End Of Conversion (EOC) voltage level from the converter's EOC output pin goes high. When conversion is completed in about 40 microseconds, the EOC voltage level returns to the low state. By inverting the negative going transition to a positive going transition, the Done flipflop may be clocked (Fig. 4-4). Clocking the Done flipflop sets it if the Busy flipflop was still on (Busy could have been cleared by a Clear function, or the SAMPLE push button could have sampled without Busy ever having been on).

Note: If the reader looked at the D input of the Done flipflop in any interface's circuit diagram in Appendix A, he would have noticed some additional logic instead of just the Busy(1) voltage. This unnecessary logic will be removed in the interface serial #2! Since this extra logic has no effect at all, even its removal did not justify the time and retesting involved.

The 12 digital output registers of the Analogic converter transfer their contents into the computer when gated by the Data In C control signal.

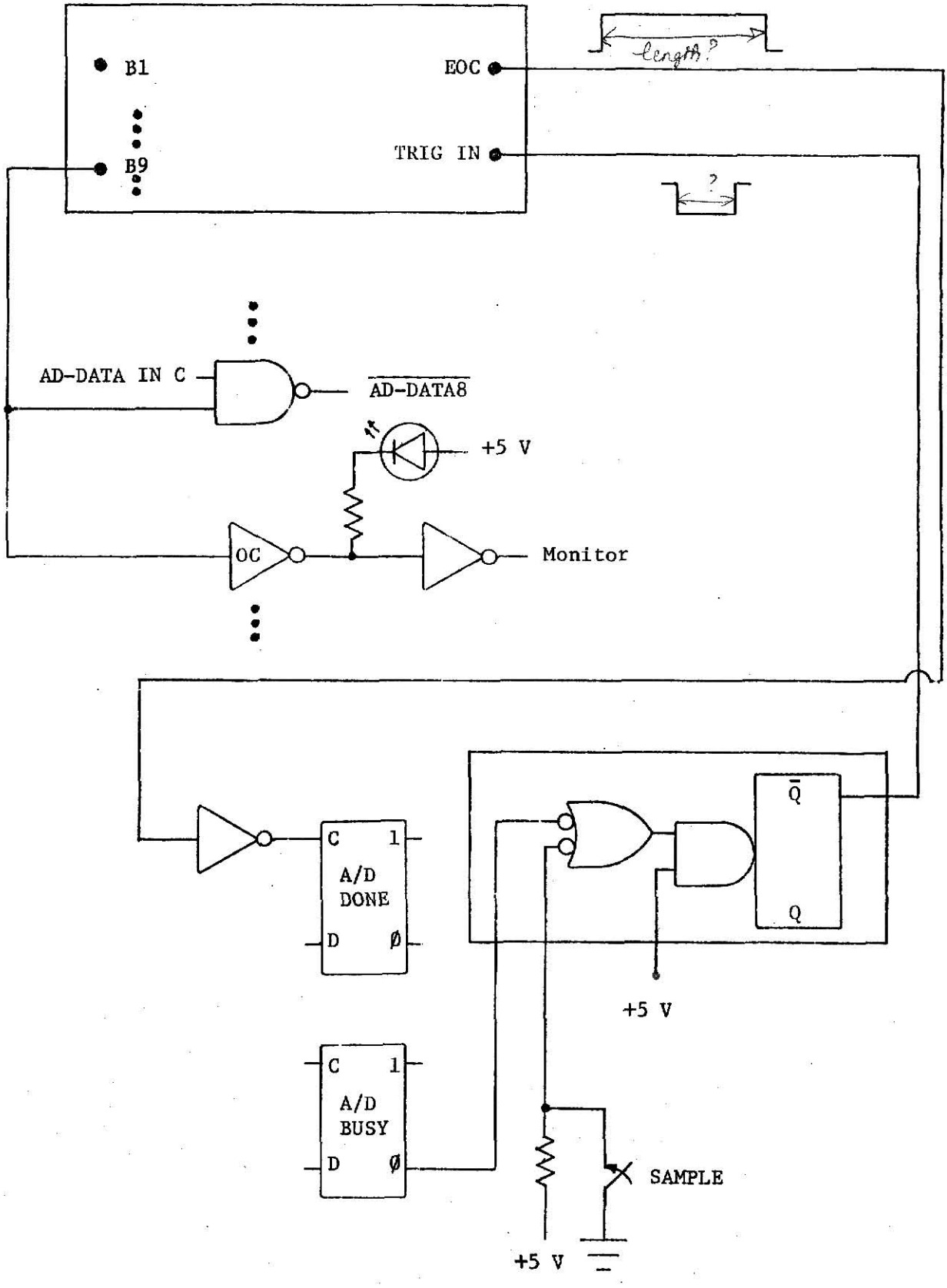


Fig. 4-4. The A/D connections to Busy/Done.

Each of the 12 bits that is at a high voltage turns on its corresponding light emitting diode (LED), driven by an open collector inverter. In addition, each output bit may be monitored at a monitoring post that is buffered from the converter for protection purposes by a pair of inverters (one of which is the LED driver).

The few remaining electrical connections shown on the circuit diagrams of Appendix A are not discussed here. These connections implement the options available with the Analogic converter such as different input voltages, different output word lengths, adjustable zero offset, etc. Since these connections do not concern the interfacing with a Nova, the discussion in the Analogic data sheet will suffice in explaining their implementation in the circuit diagrams.

The final topic of the A/D interface is the extra protection circuitry on the analog input; see Fig. 4-5. Since the maximum correct input voltage range is $\pm$10 volts, while the Analogic converter is internally protected to +15 volts, a pair of 12-volt Zener diodes is connected to hold the voltage within a safe range until a fuse in series with the input burns out. A unity-gain operational amplifier follower circuit is necessary to prevent the additional resistance of the fuse (about 250 ohms for a 1/200 amp fuse, 800 ohms for a 1/500 amp fuse) from adding to the input impedance of the converter (2,500-10,000 ohms, depending on the selected input voltage range) and thus offsetting the digital output beyond the adjustable range of the ZERO OFFSET Control.

Digital-to-Analog Control

A characteristic of most D/A converters, including the ZD 442 Zeltec, fast settling, 12-bit converter in this interface, is that they asynchronously transform the digital inputs to the analog output without waiting for a

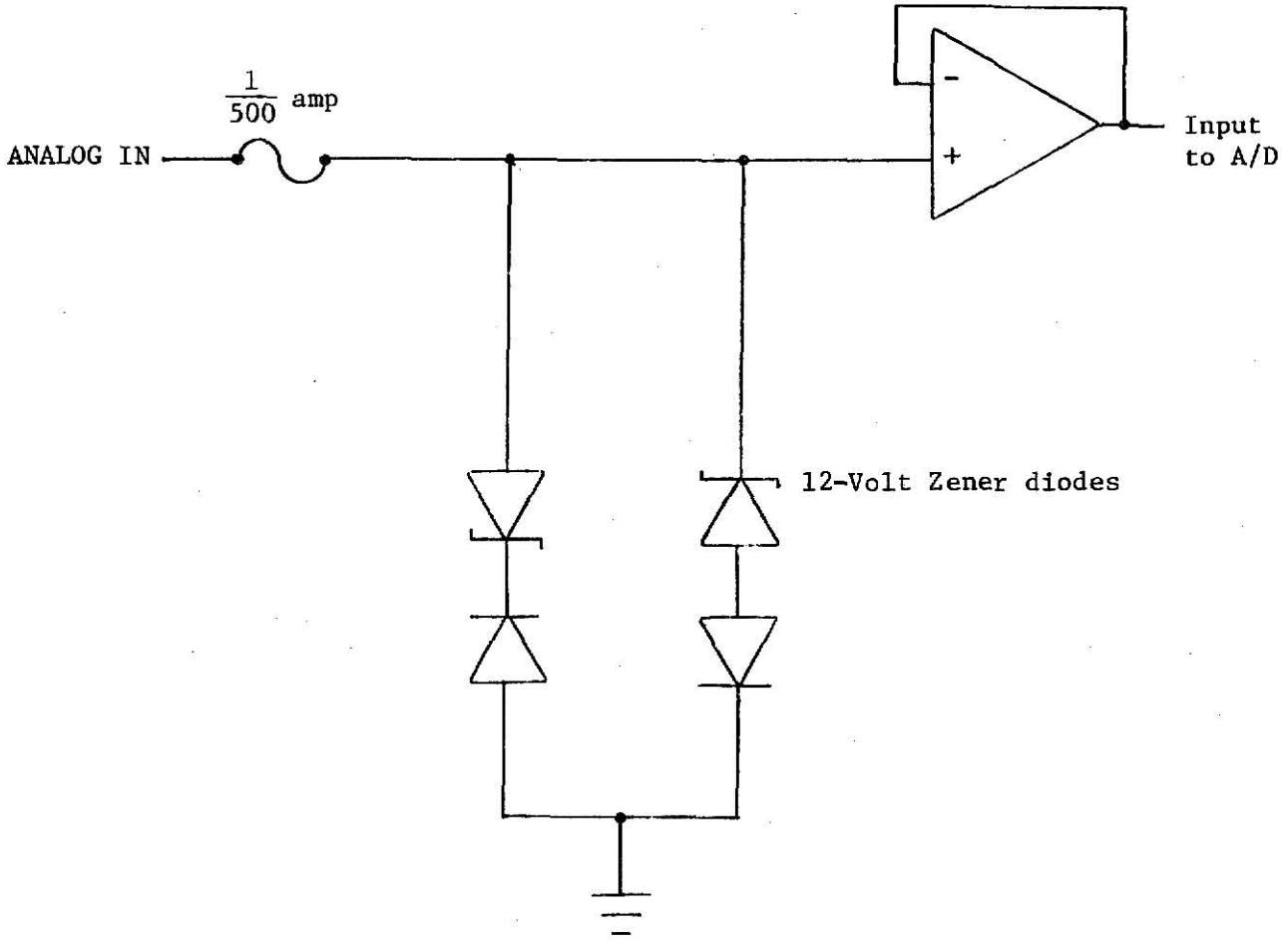


Fig. 4-5. Analog input protection circuitry.

starting signal. If it were desired that conversion take place only upon receiving the Start signal as in other devices, it would have been necessary to clock the digital inputs into a set of additional input registers using the output of Busy. The additional registers required were not considered to be justified. Instead, as actually implemented, conversion is initiated by the arrival of new data and the Data Out A instruction. Therefore, the setting of Busy by a program has no effect on the start of conversion but is used only to allow Done to be set at the completion of conversion, thus informing the program of the conversion's completion. However, a completion signal needed for the setting of Done is, again unlike most peripheral devices, not available from a D/A converter. The solution employed for the setting of Done is to create a completion signal using a pair of monostables; see Fig. 4-6. These monostables clock the Done flipflop after the 5 microsecond needed for conversion. (The explanation for using a pair of monostables is deferred until the next section covering the magnetic tape transport.) Of course, there is a real design question as to whether a Busy/Done network is really needed when the 5 microsecond conversion time is equal to the total execution time of 2 or 3 instructions. Perhaps the Busy/Done logic should just as well have been left off entirely.

The 12 digital inputs are held during conversion in latches gated by the Data Out A control signal. Light emitting diodes and monitor posts are connected to each output bit. In accordance with the Zeltec data sheet in Appendix B, some additional circuitry is implemented in order to make use of the D/A converter's options such as variable voltage outputs, adjustable zero offset, adjustable full-scale ranges, etc. Finally, a unity-gain

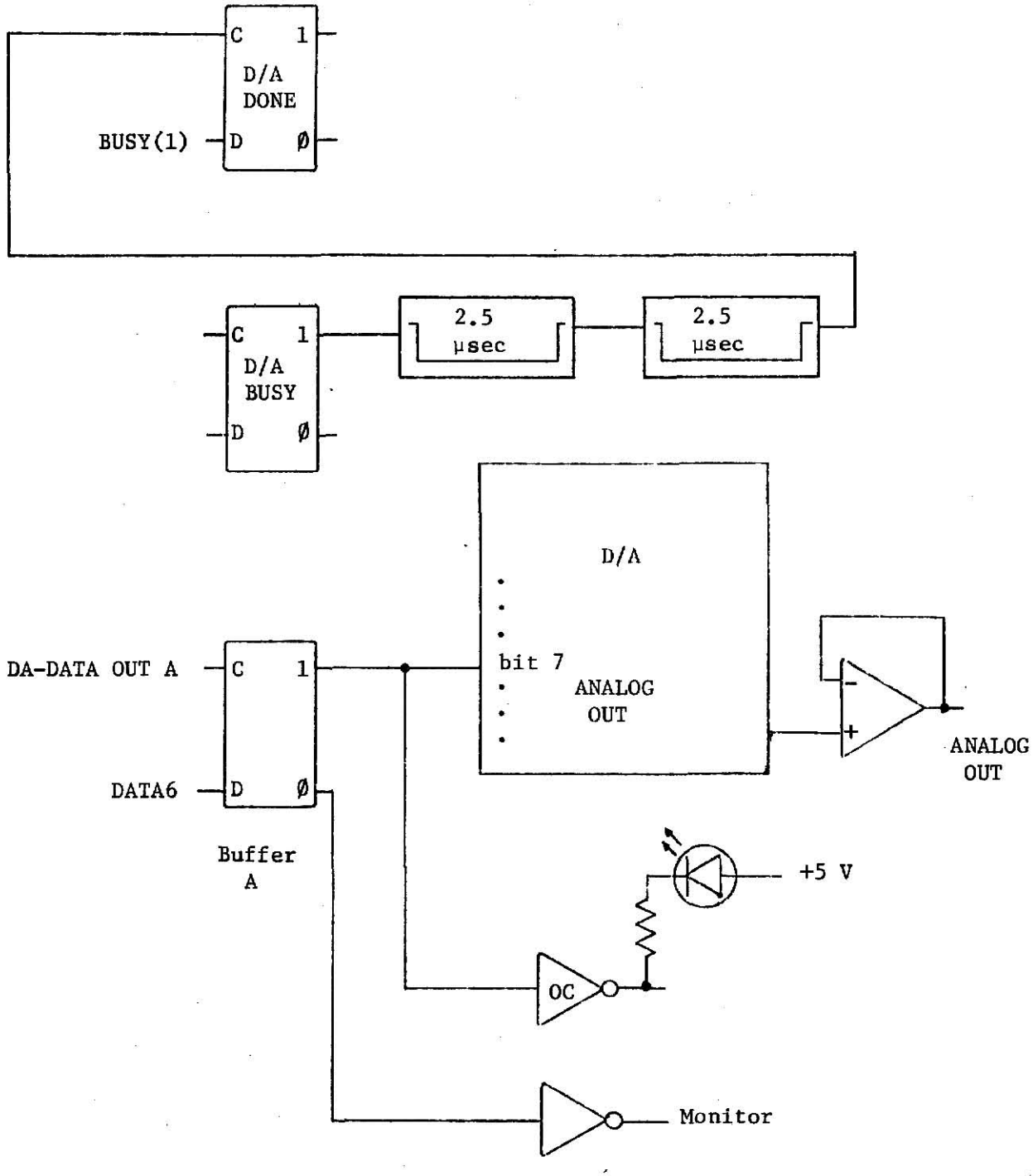


Fig. 4-6. The D/A input latches and completion signal.

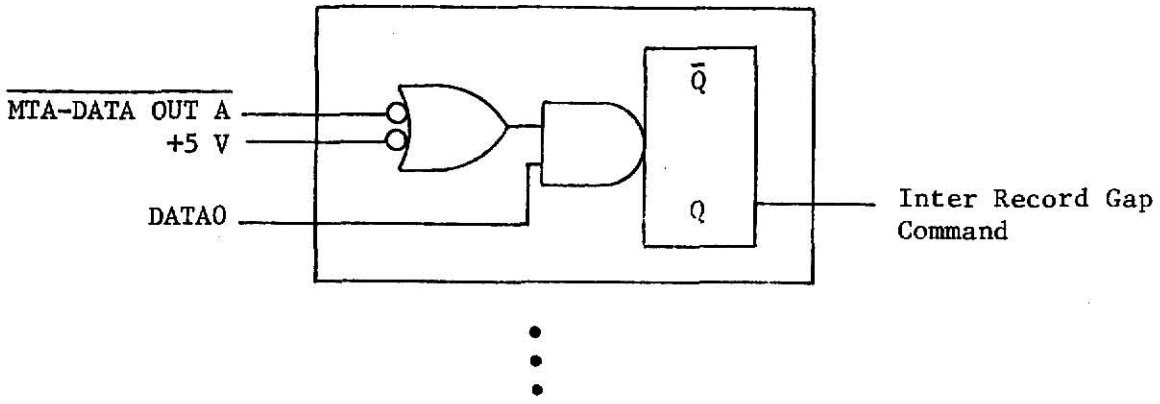
operational amplifier follower circuit on the D/A converter's output increases the available current at the ANALOG OUT coaxial connector from 5 to 25 milliamperes. In addition it serves to protect the converter.

PEC Tape Transport Control

Since the design philosophy of the PEC tape transport interface has been to make the hardware as simple as possible and the software control of the transport as flexible as possible, it was decided to assign a data bit to each transport command. Thus, placing a logical one in one or more accumulator bit positions and executing a Data Out A (DOA) instruction executes the transport commands assigned to those bits. Since the transport requires a pulse for some commands, while other command functions respond to voltage levels, a command register composed of monostables and latches has been implemented; see Fig. 4-7. Those command functions requiring a pulse are connected to the output of command register monostables; those requiring a level are connected to the outputs of latches. The data bits provide the input to the latches or one of the inputs to the monostables, while the DOA instruction either provides the second input required for the monostable to pulse or just clocks the latch. The commands to the transport are all implemented through the command register, except the Write Step Command which is connected to the output of Busy as described later.

The transport not only accepts commands but also returns status information. By gating each of the transport's status lines with the Data In A control in the interface and assigning each line to a data bus line (Fig. 4-8), the status of the transport can be read into an accumulator.

To transfer the eight bits of data to the transport for writing, the data signals DATA0 - DATA7 form the inputs to eight latches clocked by the Data Out C control; see Fig. 4-9. The outputs of the latches hold the data inputs to the transport high or low during the PEC Write sequence.



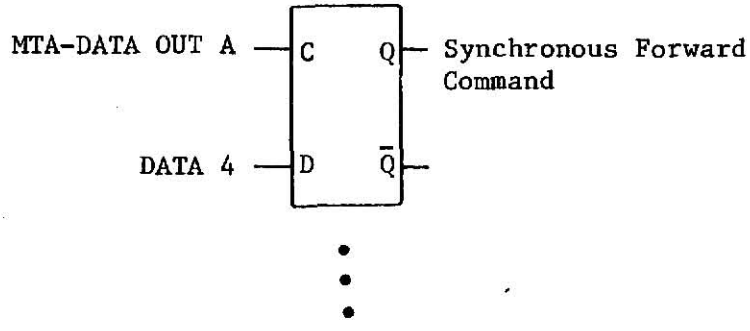


Fig. 4-7. The command register.

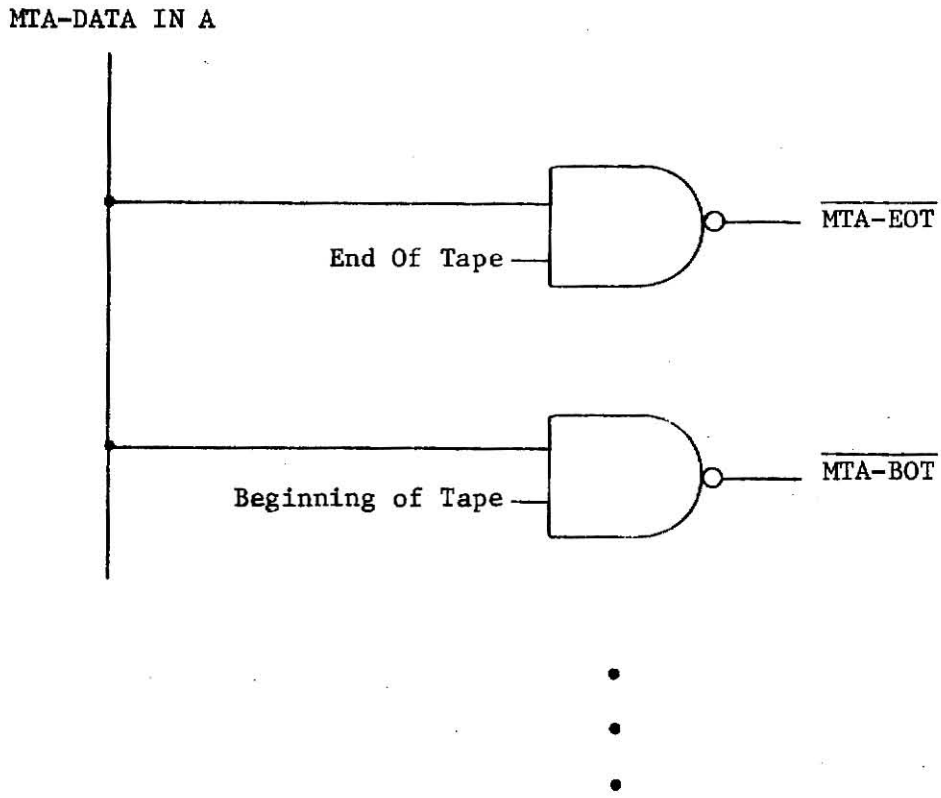


Fig. 4-8. Gating the status bits.

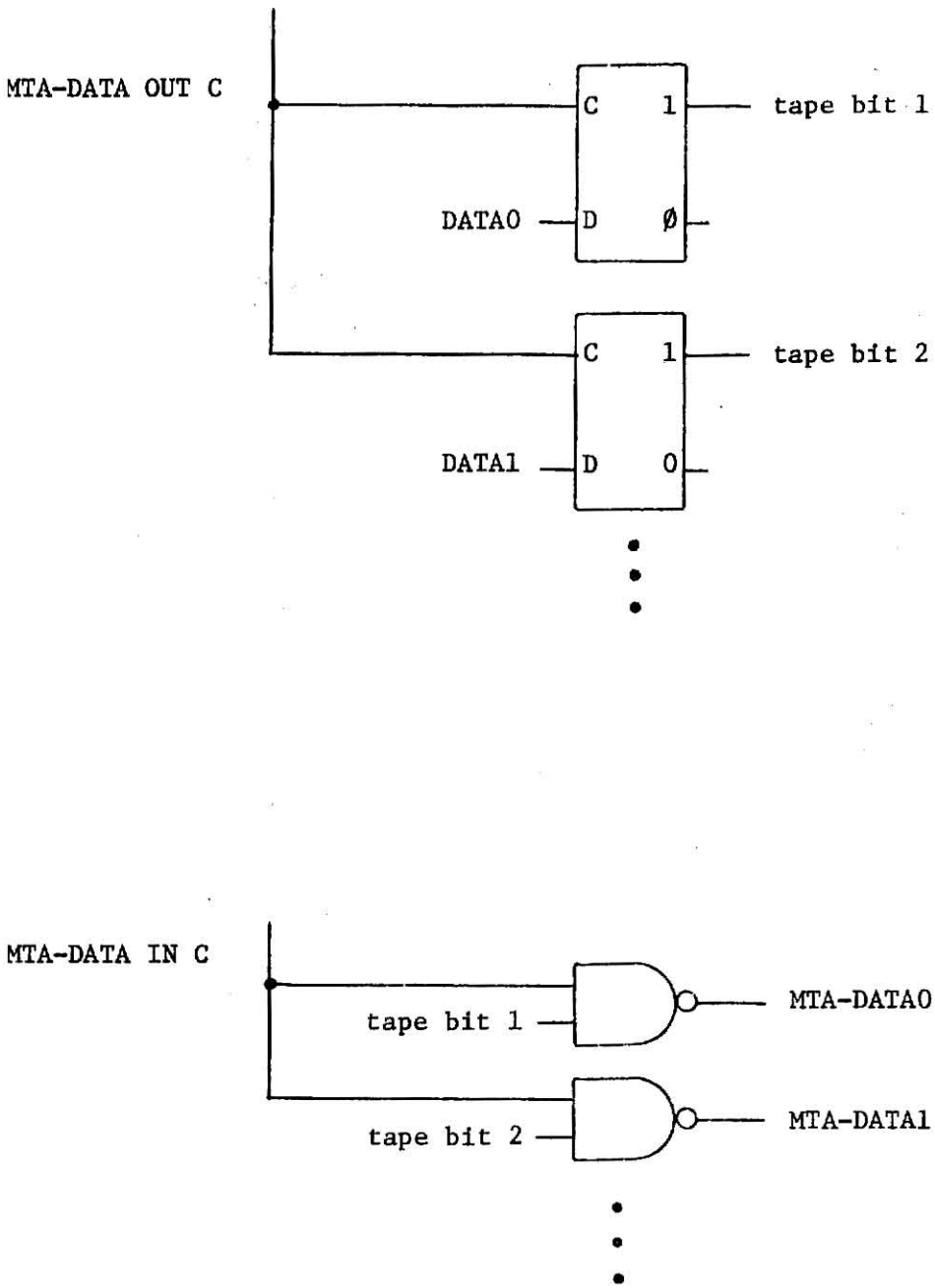


Fig. 4-9. Data transfer in the tape transport.

To permit the setting of the Busy flipflop to initiate the write sequence, the Busy output forms one of the inputs to a monostable whose pulse output is connected to the PEC tape transport's Write Step Command input; see Fig. 4-10. Another monostable input comes from the output of the Write/Read Mode latch. Without the latter connection, tape stepping motion could occur regardless of whether or not write current was flowing in the recording head and the data was actually written. With such a connection, tape stepping motion can occur only when data is actually being written. During the write sequence, the transport automatically writes the ninth bit on the tape. This bit serves as a parity bit.

When the data has been written, the Done flipflop must be set to inform the computer that the next set of data can be presented to the transport and written. However, the transport provides no signal when it is ready to write the next byte of data, although it is known from the specifications that the transport can write up to 700 bytes per second. Thus to clock the Done flipflop, a pair of monostables must be set for a combined pulse width of 1/700 seconds and connected between the output of Busy and the clock input of Done. A pair of monostables must be used here (just as is done in the D/A interface) because it is possible when writing at the transport's maximum rate, to exceed a single monostable's maximum duty cycle of 90% on. Since the pulse would be on for 1/700 seconds and off for only the 10-20 microseconds needed for a few computer instructions to get the next data to be written, the timing components would never fully return to their reset states. Exceeding a monostable's duty cycle results in a non-uniform pulse width and causes excessive pulse jitter.

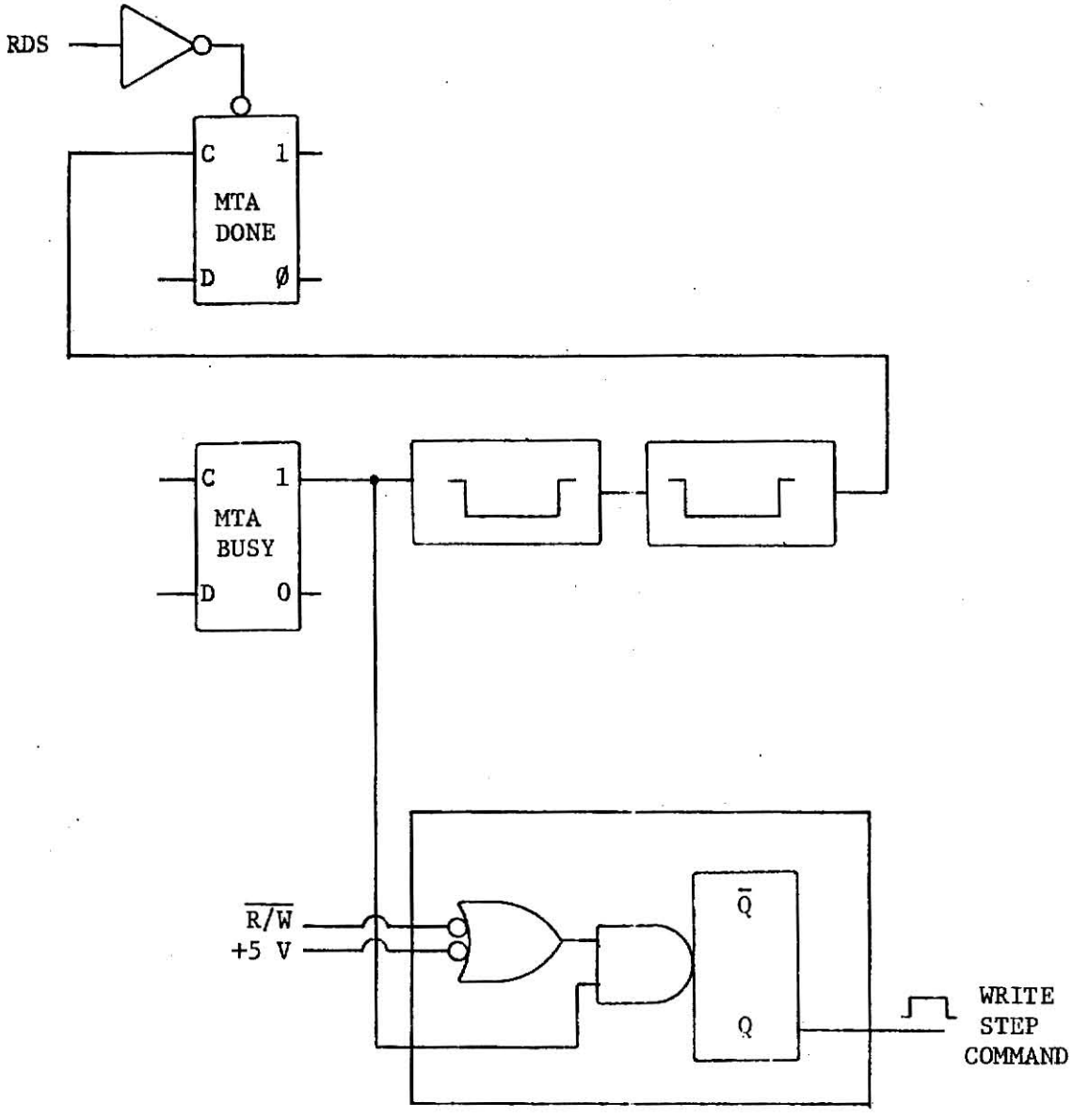


Fig. 4-10. Tape transport connections to Busy/Done.

To read data, the transport is placed in the Read mode and the tape set in Synchronous Forward or Synchronous Reverse motion. As the tape moves, bytes of data are successively placed on the transport's read lines, at approximate intervals of 80 microseconds. When a new byte of data is ready for reading, the transport sends out a Read Data Strobe (RDS) pulse. (If the transport is not in the Read mode, there are no RDS pulses.) Gating the read data on to the data bus lines $\overline{\text{DATA0}}$ - $\overline{\text{DATA8}}$ with a Data In C signal (Fig. 4-9), and connecting the RDS line to the preset input of the Done flipflop (Fig. 4-10), enables the computer to gate the data into an accumulator when the RDS pulse sets Done. Of course, for Done to set, Busy must have been previously set by the program. The setting of Busy by the program has no other effect on the transport in the read mode, except to allow the setting of Done. The reader is reminded that the Write Step Command monostable tied to the output of Busy pulses only when the transport is in the Write mode.

A Note on Grounding

To conclude this chapter, the reader's attention should be directed to the fact that all analog returns join at a common point, which is in turn tied to the digital signal ground. See, for example, the section "Installation and Grounding" in the Analog-Digital Conversion Handbook, pp. II-163 to II-166 [5].

CHAPTER V

CONCLUSION -- IDEAS AND SUGGESTIONS

The availability of a one channel digitizing capability can be used to good advantage for various digital signal processing applications. Research efforts can be initiated via spectral analysis, digital filtering and correlation techniques of various types of signals, thereby increasing the potential for interdisciplinary research efforts.

The above system can also be used to good advantage for pedagogical purposes. For example, the system can serve as a laboratory tool to complement the digital signal analysis/filtering techniques covered in the Digital Network Theory course (EE 647). For example, analog signals can be synthesized, digitized, filtered, converted back to analog form, and then displayed. If speech signals are involved, one can qualitatively assess the effect of filtering them by hearing the reconstructed speech.

A useful source for ideas pertaining to research and pedagogical applications in the Analog Devices' Analog-Digital Conversion Handbook.

For those interested in further hardware design, there are a number of worthwhile projects. A real-time clock would find use in the timing of program loops or in fixed delays. If there is a demand for special-purpose interfaces, the equivalent of the General Purpose I/O Interface board in the Nova could be reproduced but outside on the external bus. Such boards may also be purchased at a reasonable price (Douglas Electronics, Inc., 718 Marina Blvd., San Leandro, Calif. 94577). Printed circuit board slots with power available could be pre-wired to the bus. One spare, printed

circuit, general purpose interface board could be printed and the IC's implementing the Busy/Done logic soldered on. To construct a new special purpose interface, one would need only to take an available board, solder on the data channel IC's if desired, any registers, and wire-wrap the special purpose logic. Debugging the new interface would be mostly confined to the specialized logic that was wire-wrapped. If a spare general purpose interface board were always available, then an interface for a specific application could be readily developed.

In conclusion, the PEC incremental tape transport can be used not only for data acquisition but also for backup program and disk storage. The calculations shown below give some idea as to an incremental transport's relative usefulness for program storage:

Approximate time to write 8 K of memory to tape:

$$8192 \text{ words} \times \frac{2 \text{ bytes}}{\text{word}} \div \left(\frac{700 \text{ bytes}}{\text{sec}}\right) = 23 \text{ sec}$$

Approximate time to read 8 K of memory from tape:

$$8192 \text{ words} \times \frac{2 \text{ bytes}}{\text{word}} \times \frac{80 \times 10^{-6} \text{ sec}}{\text{byte}} = 1.3 \text{ sec}$$

Approximate time to write 1 disk to tape =

$$\frac{256 \text{ words}}{\text{sector}} \times \frac{12 \text{ sectors}}{\text{track}} \times \frac{2 \text{ tracks}}{\text{cylinder}} \times \frac{203 \text{ cylinders}}{\text{disk}}$$

$$\times \frac{2 \text{ bytes}}{\text{word}} \div \frac{700 \text{ bytes}}{\text{sec}} \times \frac{1 \text{ min}}{60 \text{ sec}} = 59 \text{ min.}$$

Approximate time to read 1 disk from tape =

$$\frac{256 \text{ words}}{\text{sector}} \times \frac{12 \text{ sectors}}{\text{track}} \times \frac{2 \text{ tracks}}{\text{cylinder}} \times \frac{203 \text{ cylinders}}{\text{disk}}$$

$$\times \frac{2 \text{ bytes}}{\text{word}} \times \frac{80 \times 10^{-6} \text{ sec}}{\text{byte}} \times \frac{1 \text{ min}}{60 \text{ sec}} = 3.3 \text{ min.}$$

APPENDIX A

Circuit Diagrams

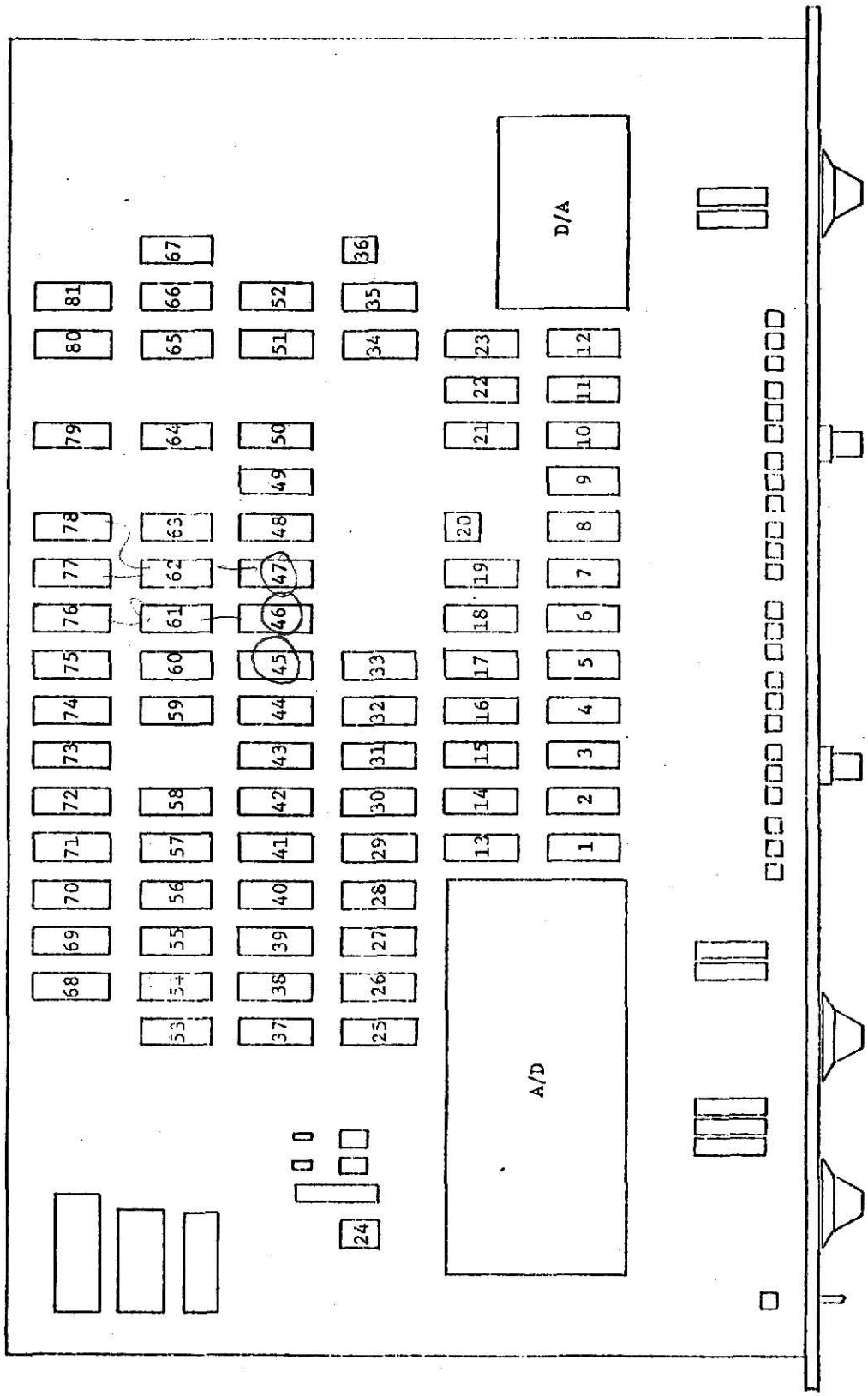


Fig. A-1. Interface component map

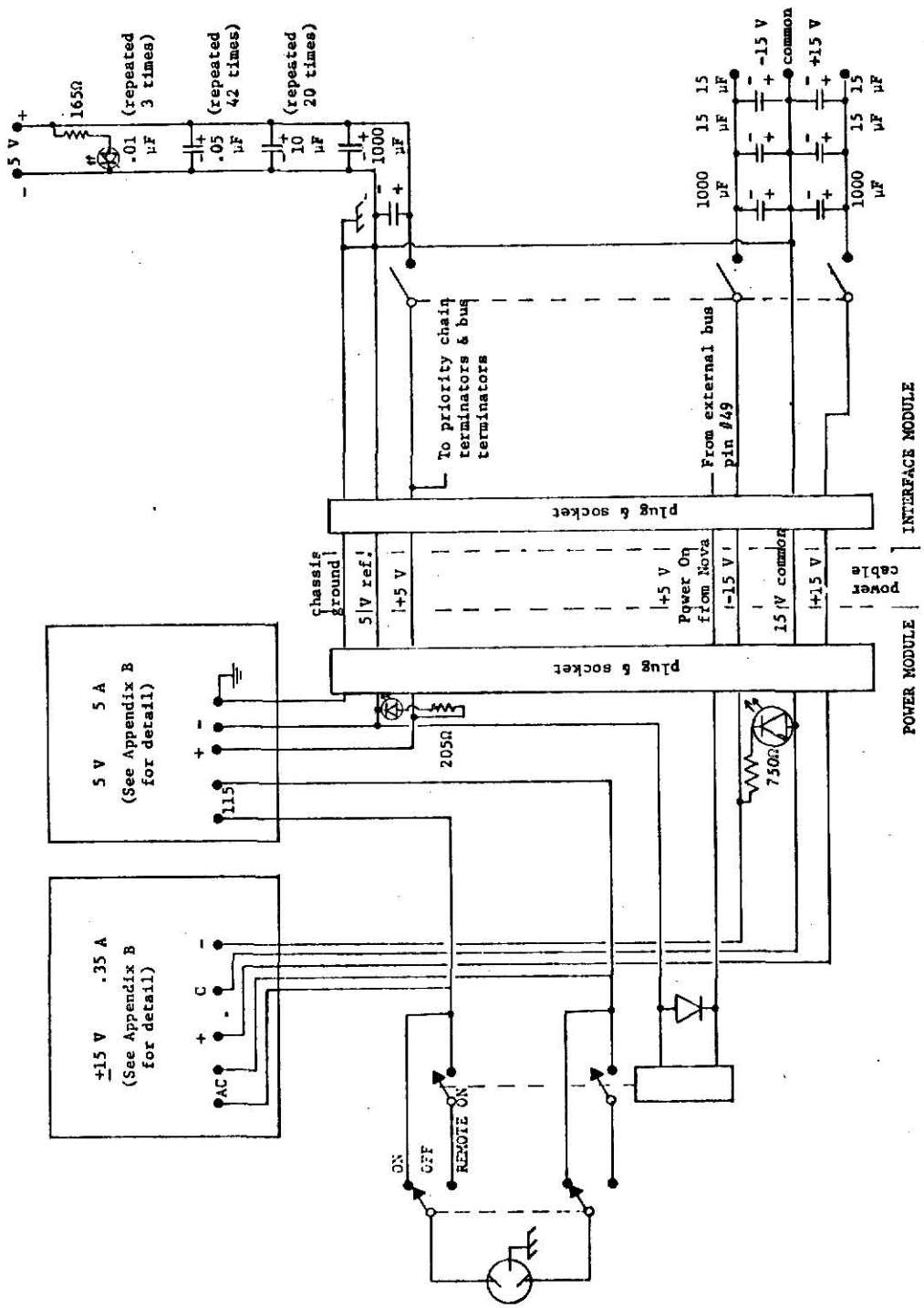


Fig. A-2. The power module

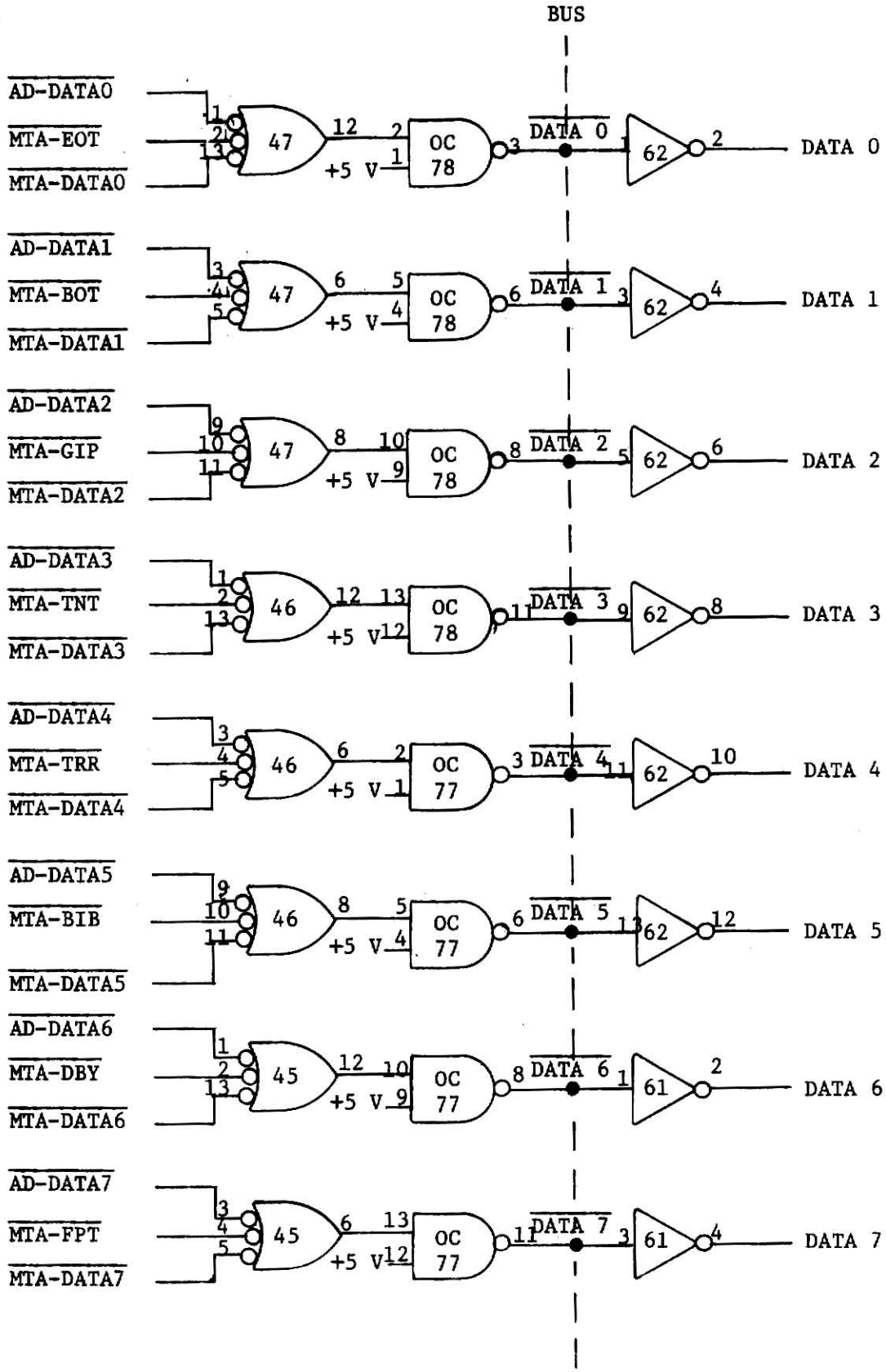


Fig. A-3. Common logic: connections to data bus lines 0-7

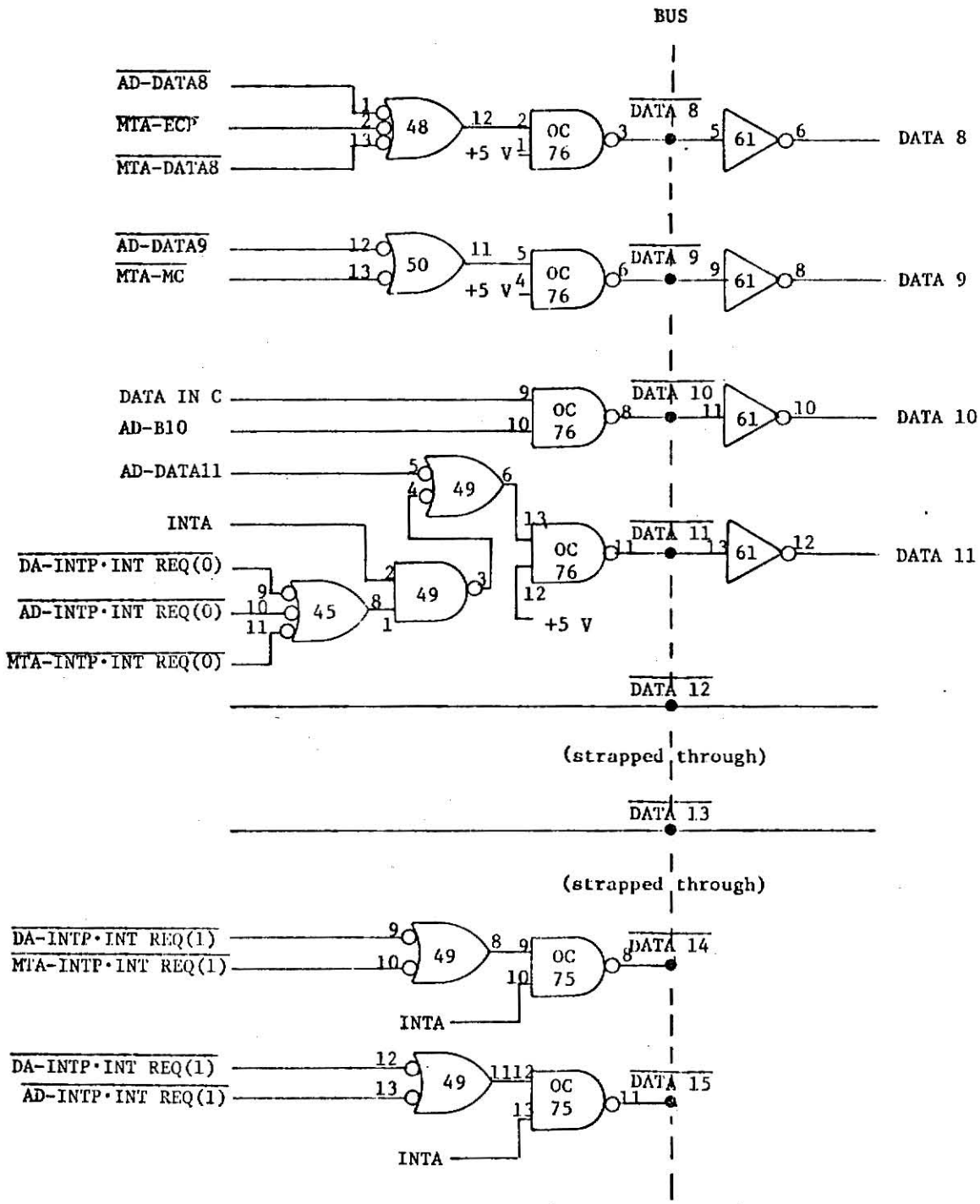


Fig. A-4. Common logic: connections to data bus lines 8-15

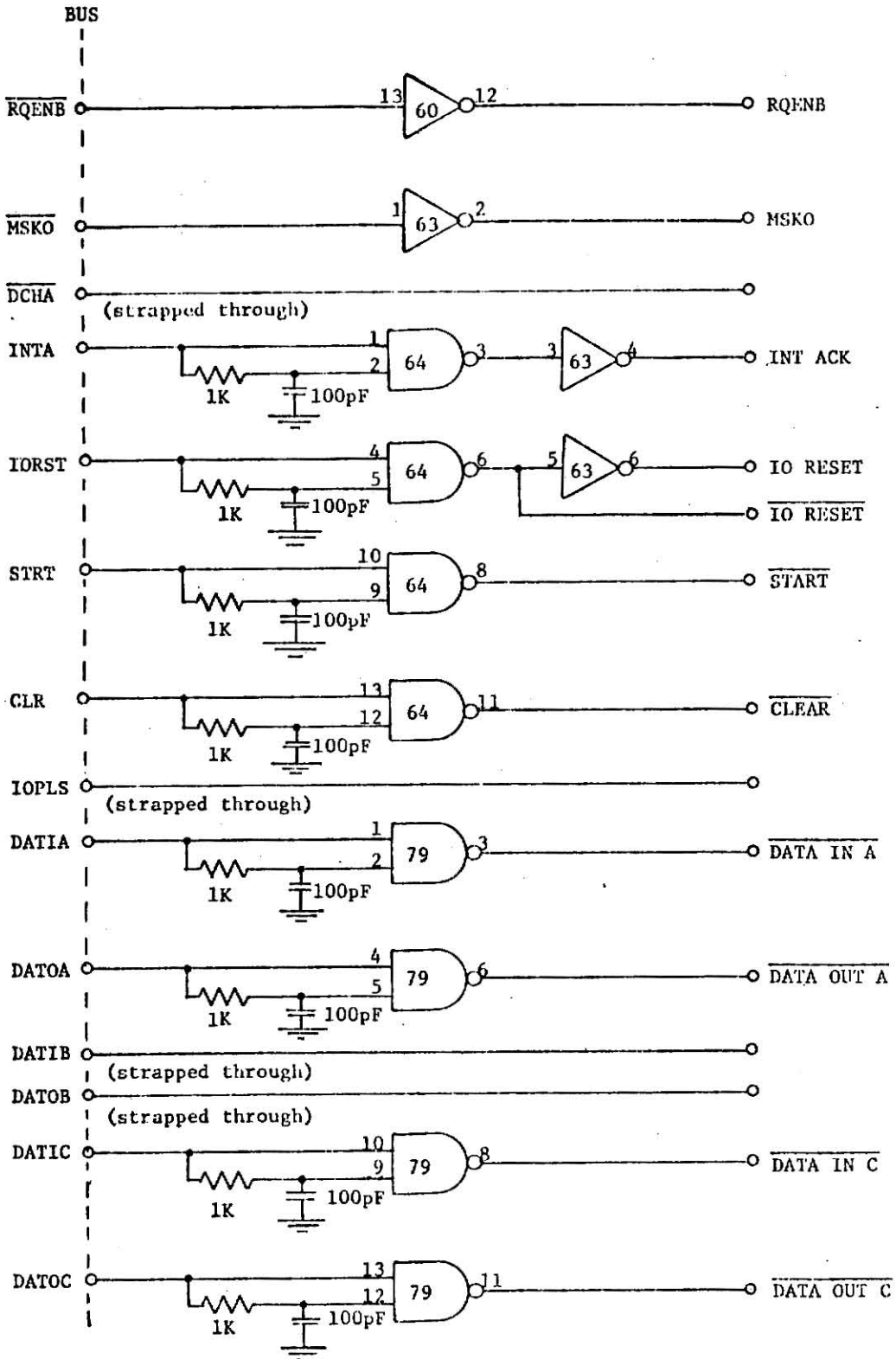


Fig. A-5. Common logic: control signals to the devices

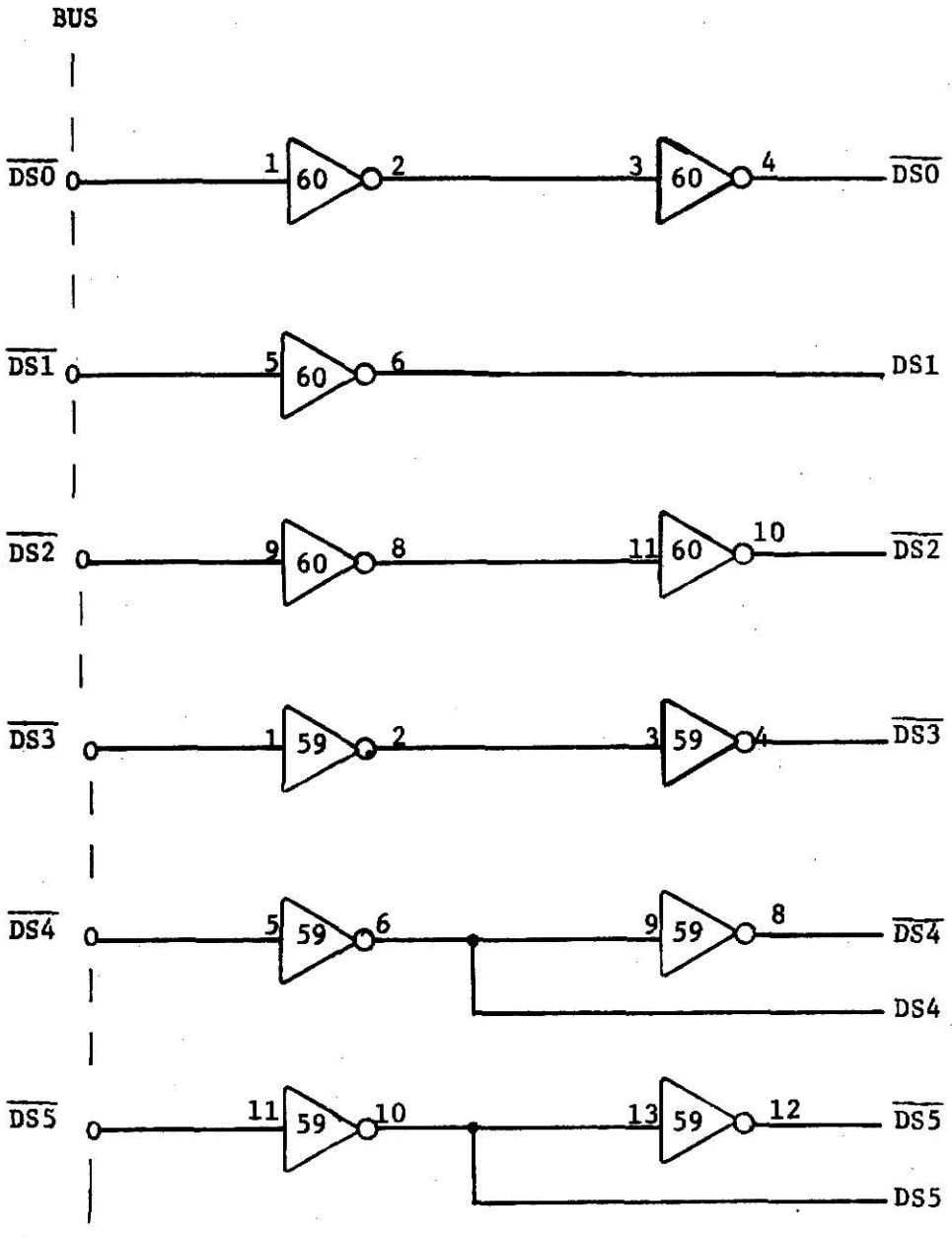
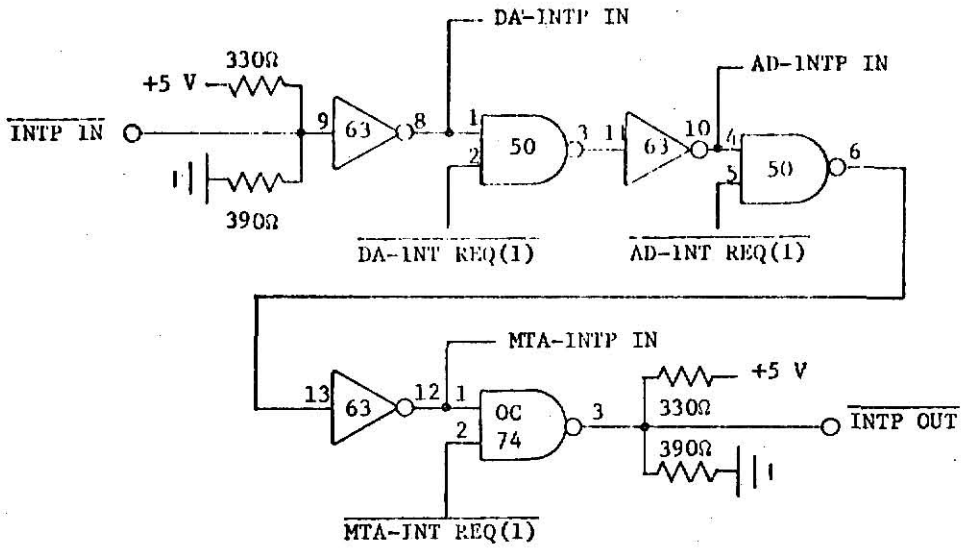


Fig. A-6. Common logic: device select receivers



(data channel priority chain is strapped through)

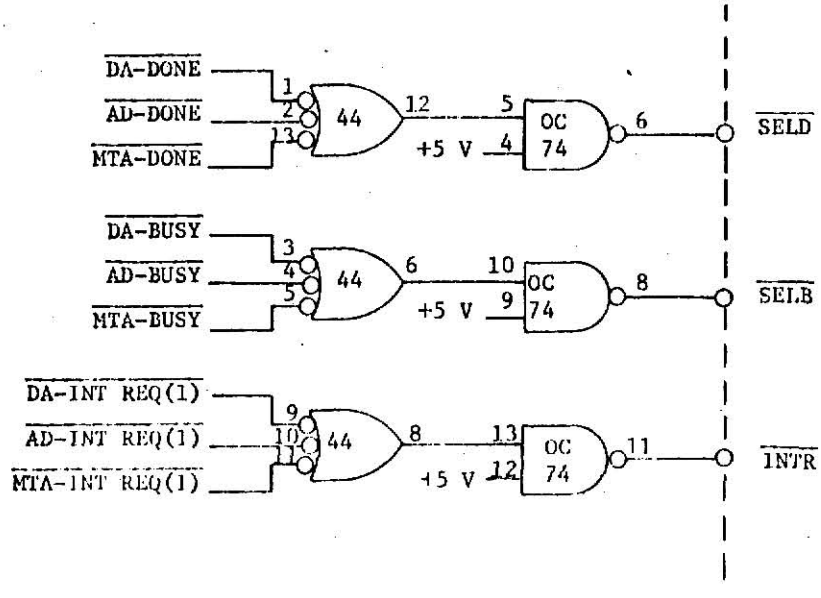


Fig. A-7. Common logic: interrupt priority chain and control signals from the devices

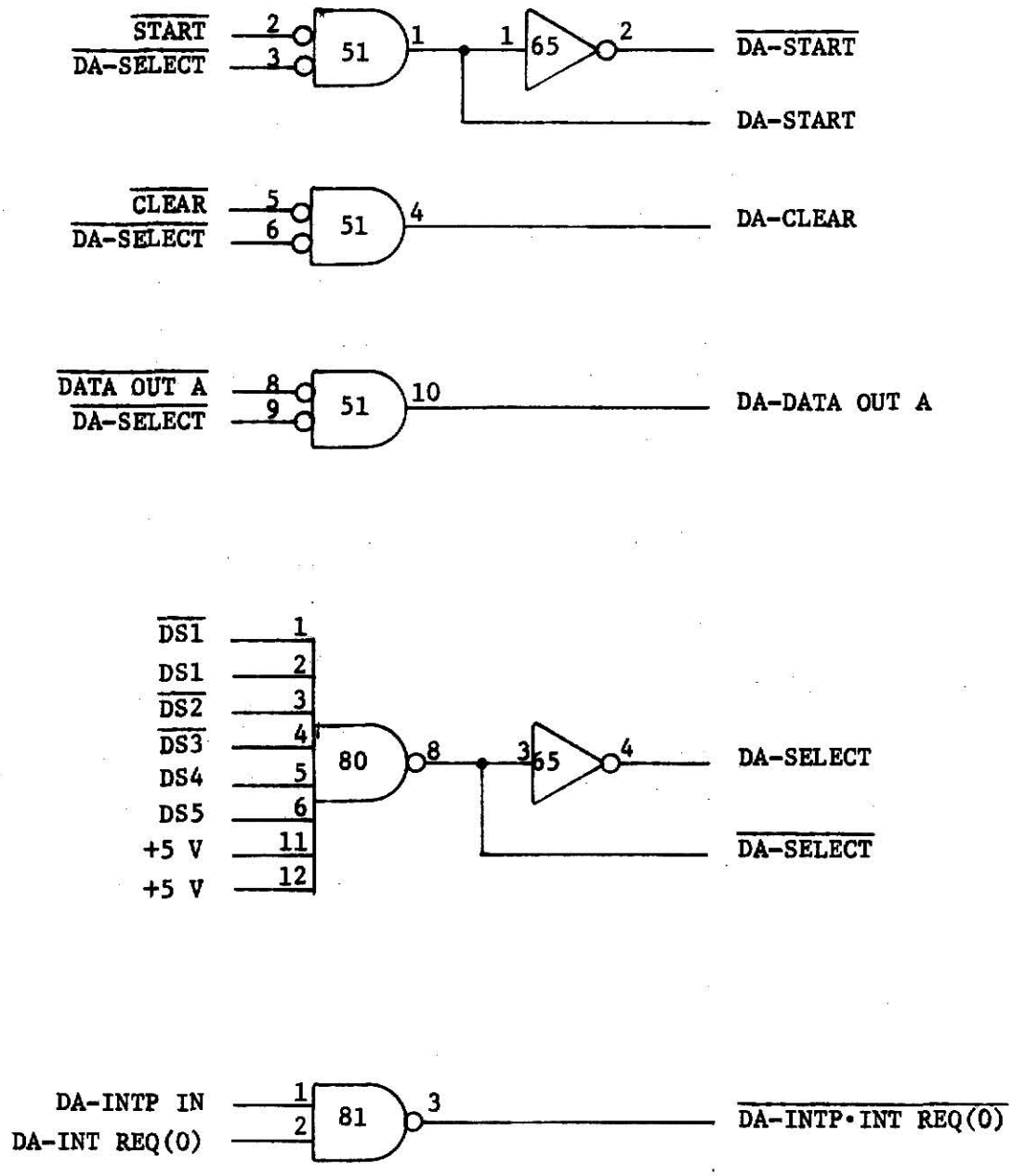


Fig. A-8. Digital-analog control signals from the common logic

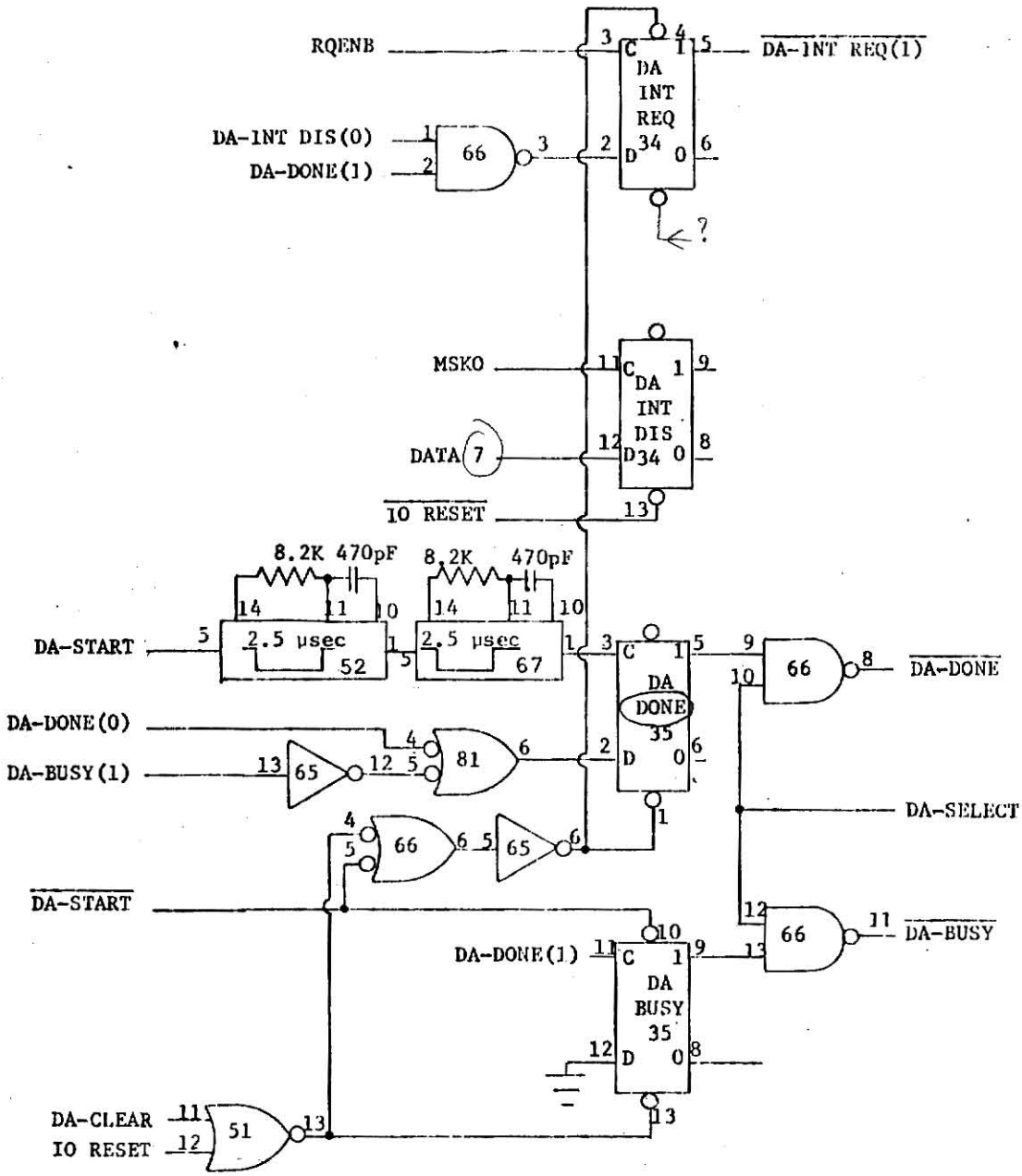


Fig. A-9. Digital-analog Busy/Done implementation

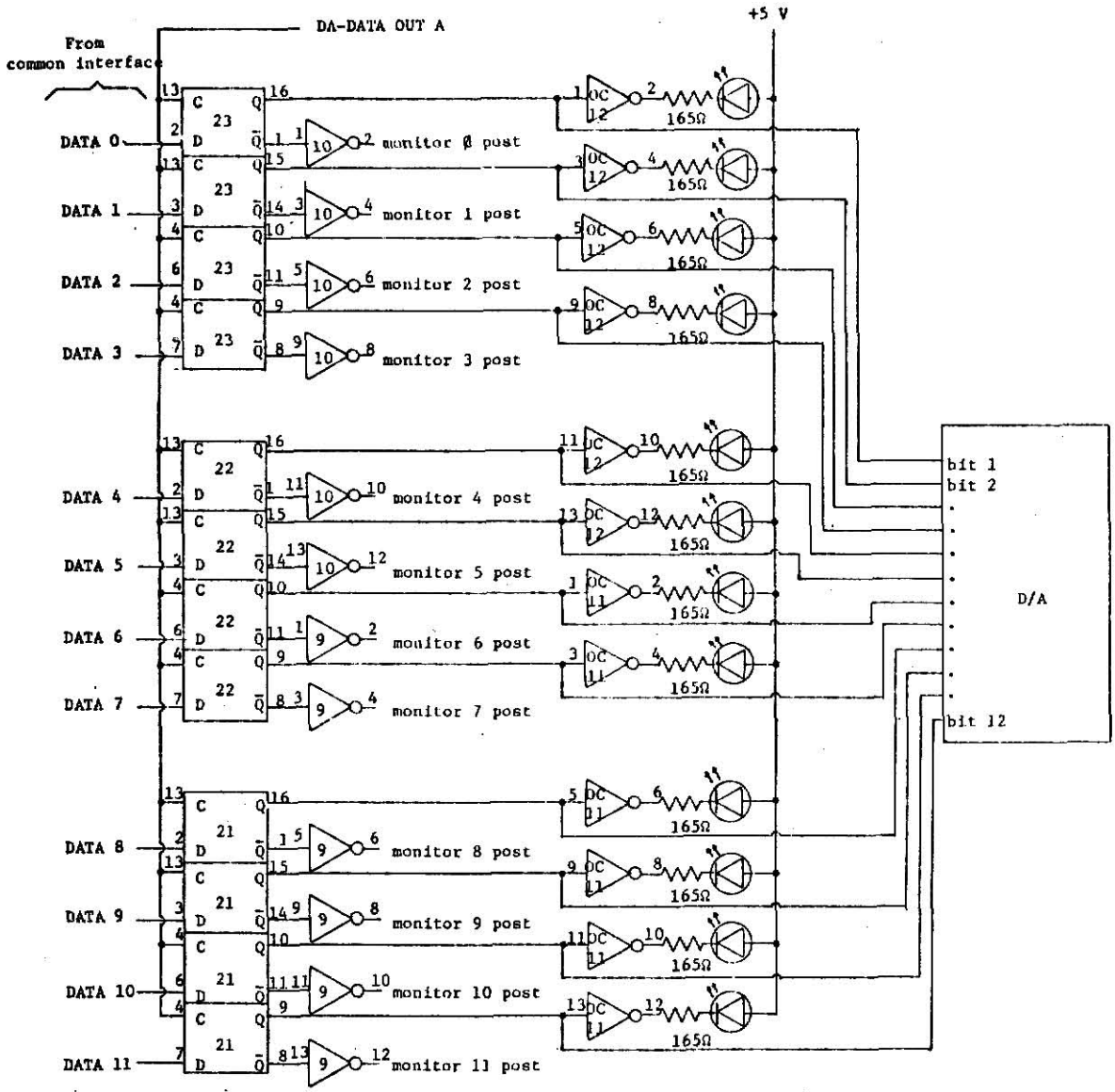


Fig. A-10. Digital-analog data input register

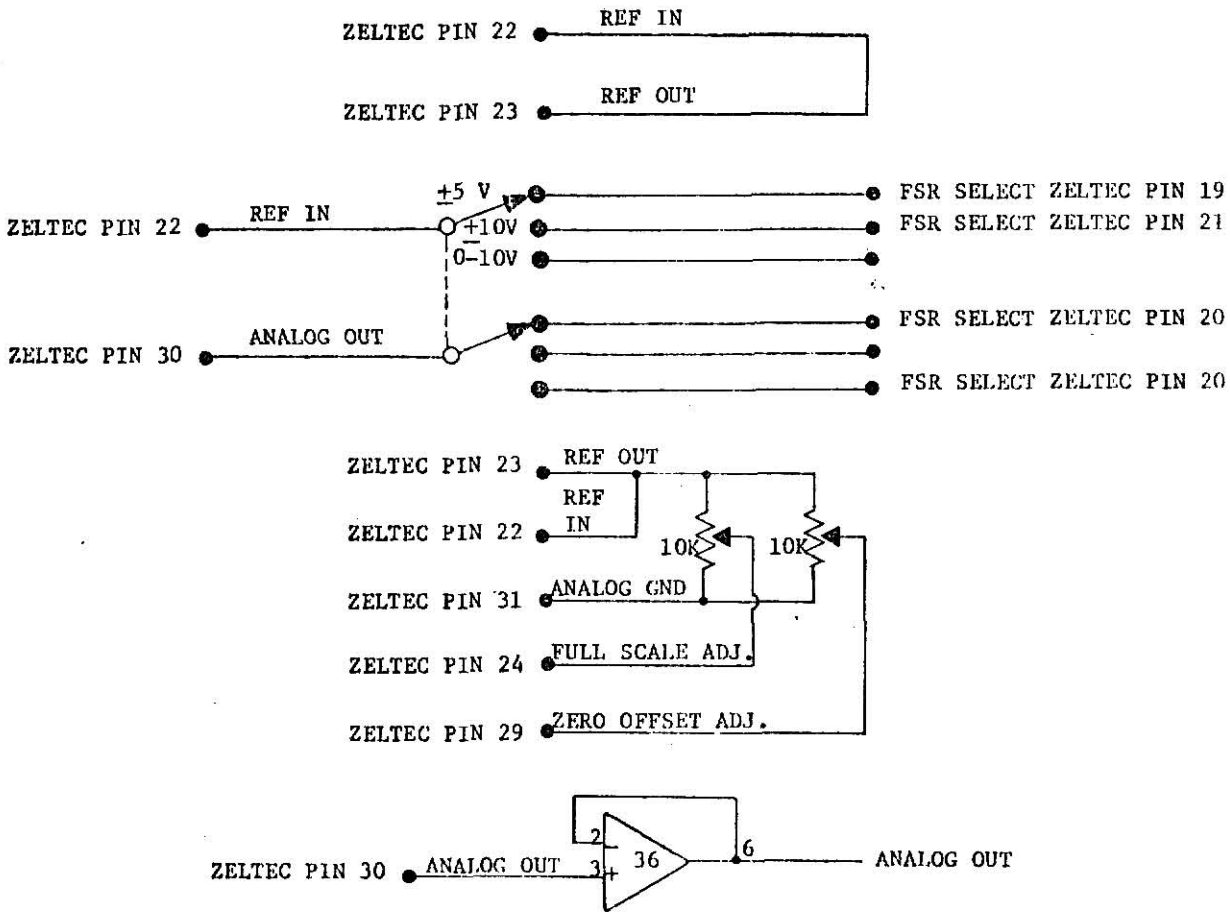


Fig. A-11. Digital-analog OUTPUT VOLTAGE selector switch, trimmer potentiometers, and output operational amplifier

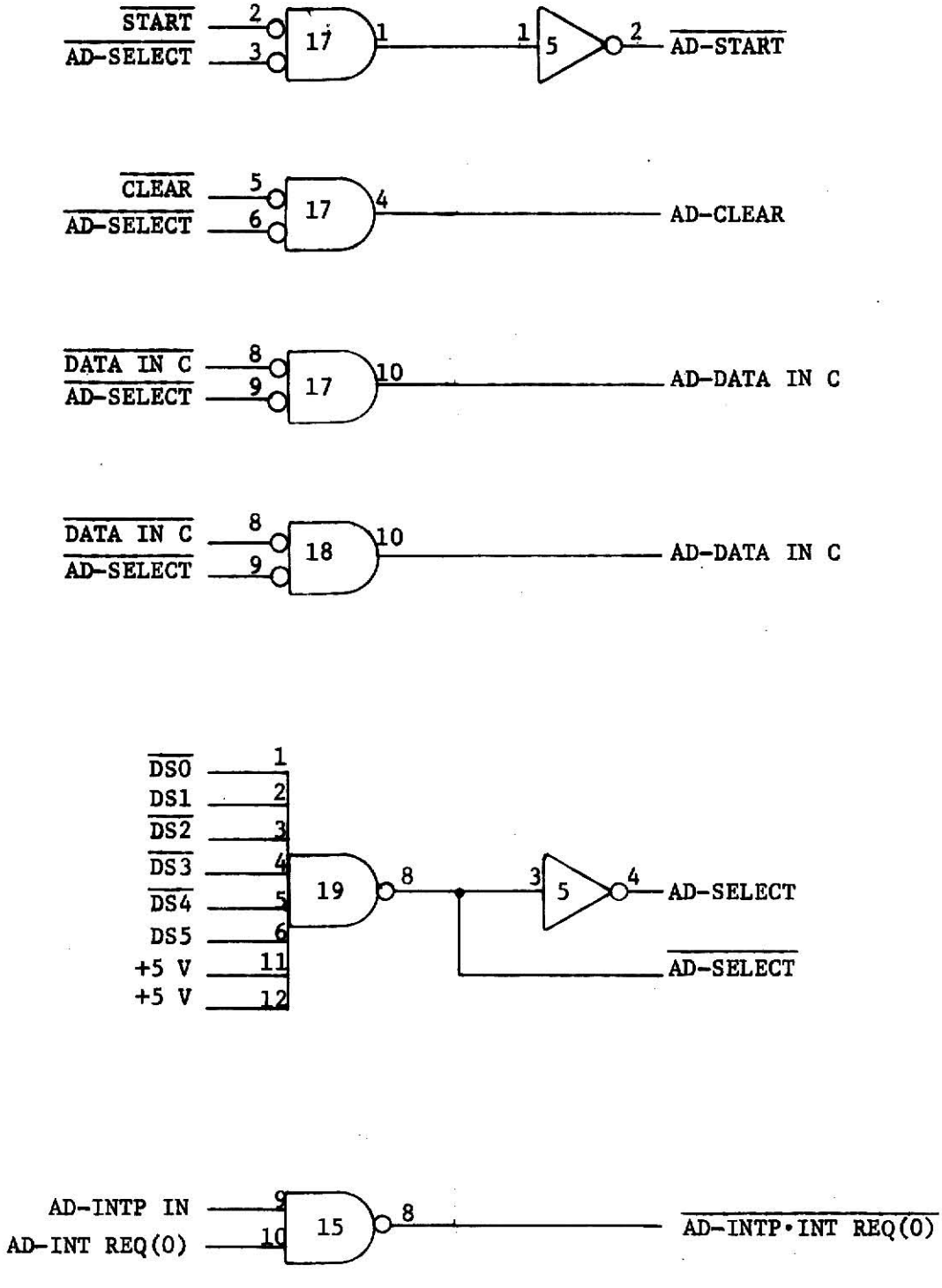


Fig. A-12. Analog-digital control signals from the common logic

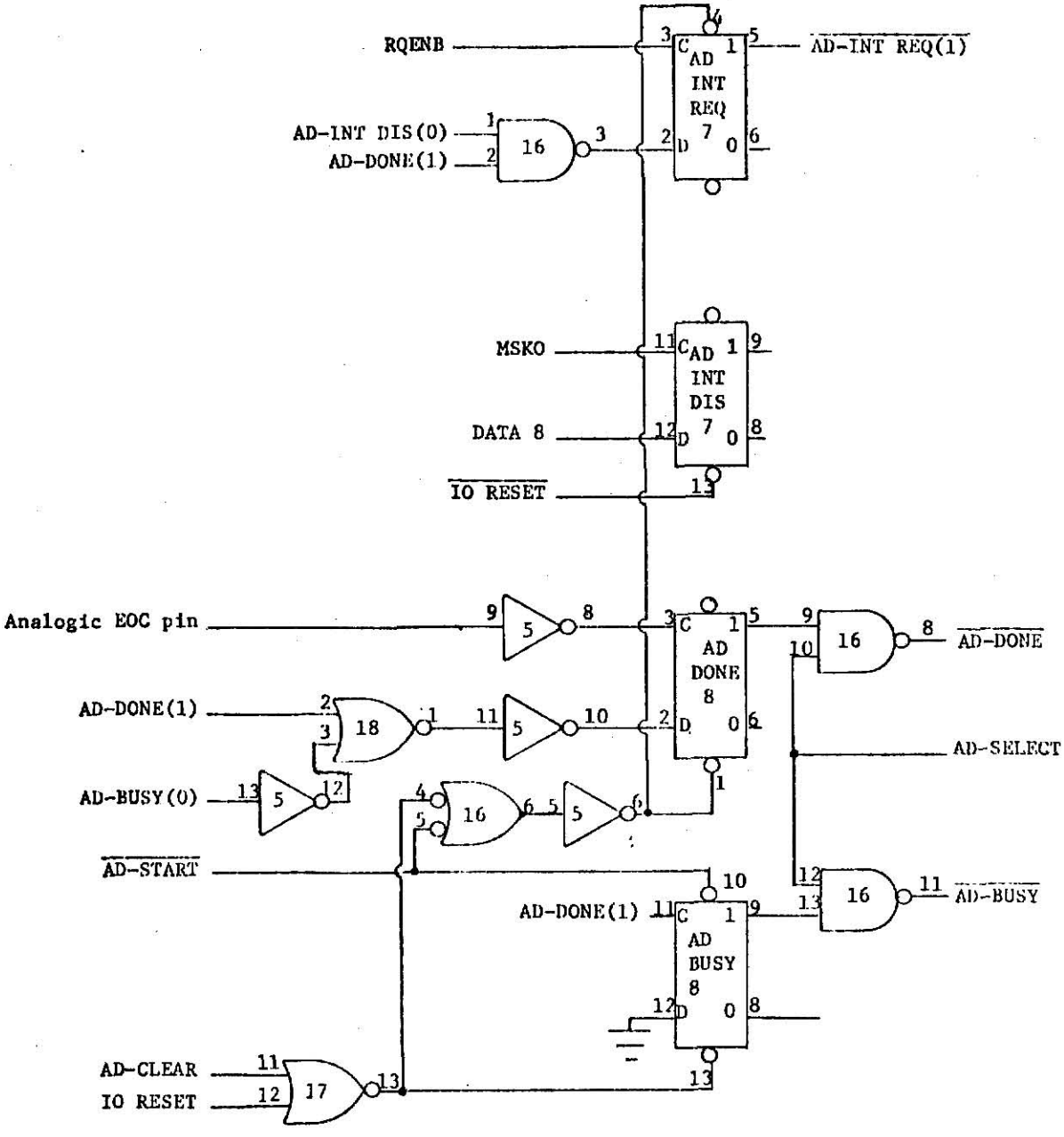


Fig. A-13. Analog-digital Busy/Done implementation

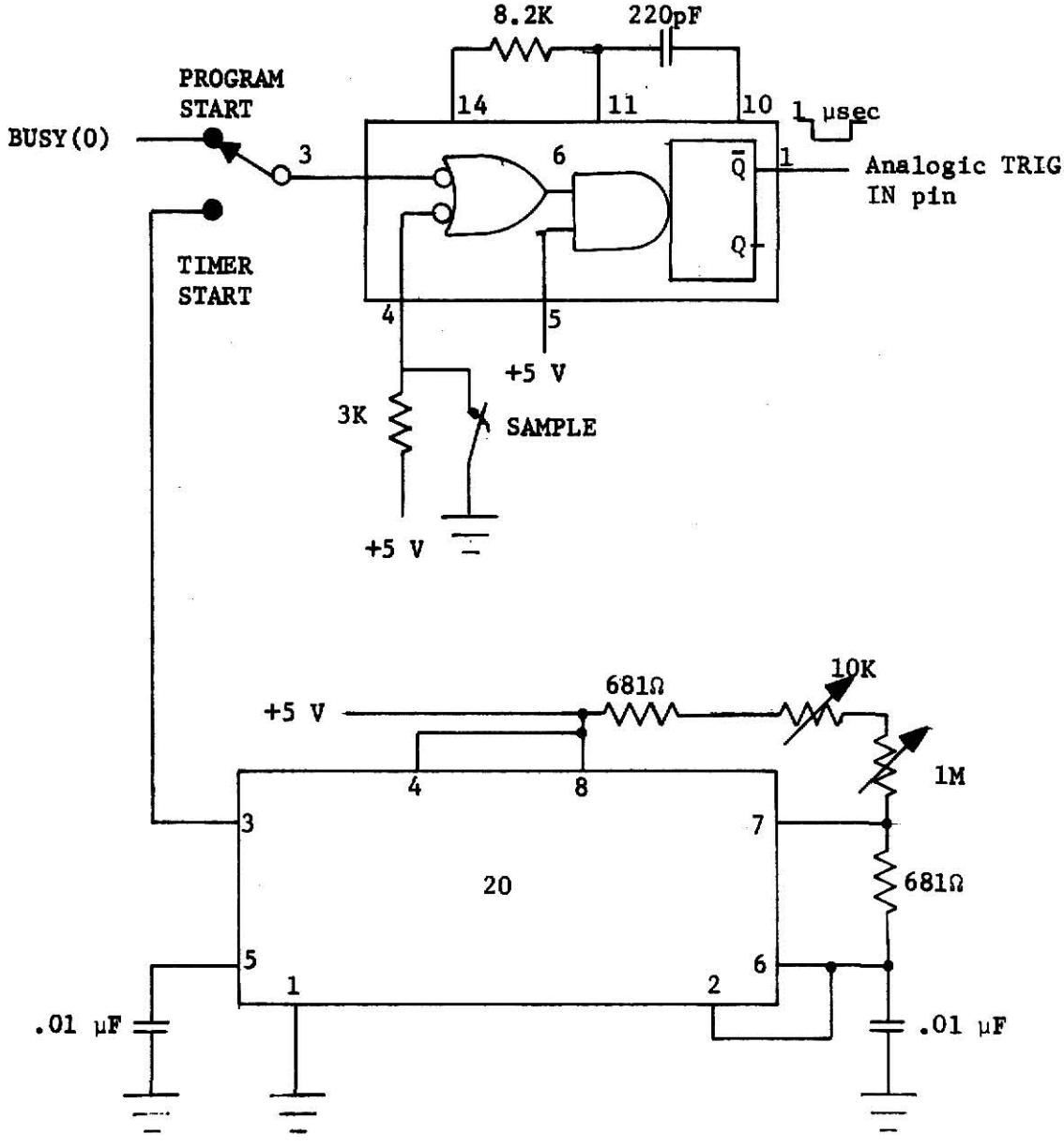


Fig. A-14. Analog-digital TIMER and connections to the Analogic trigger input

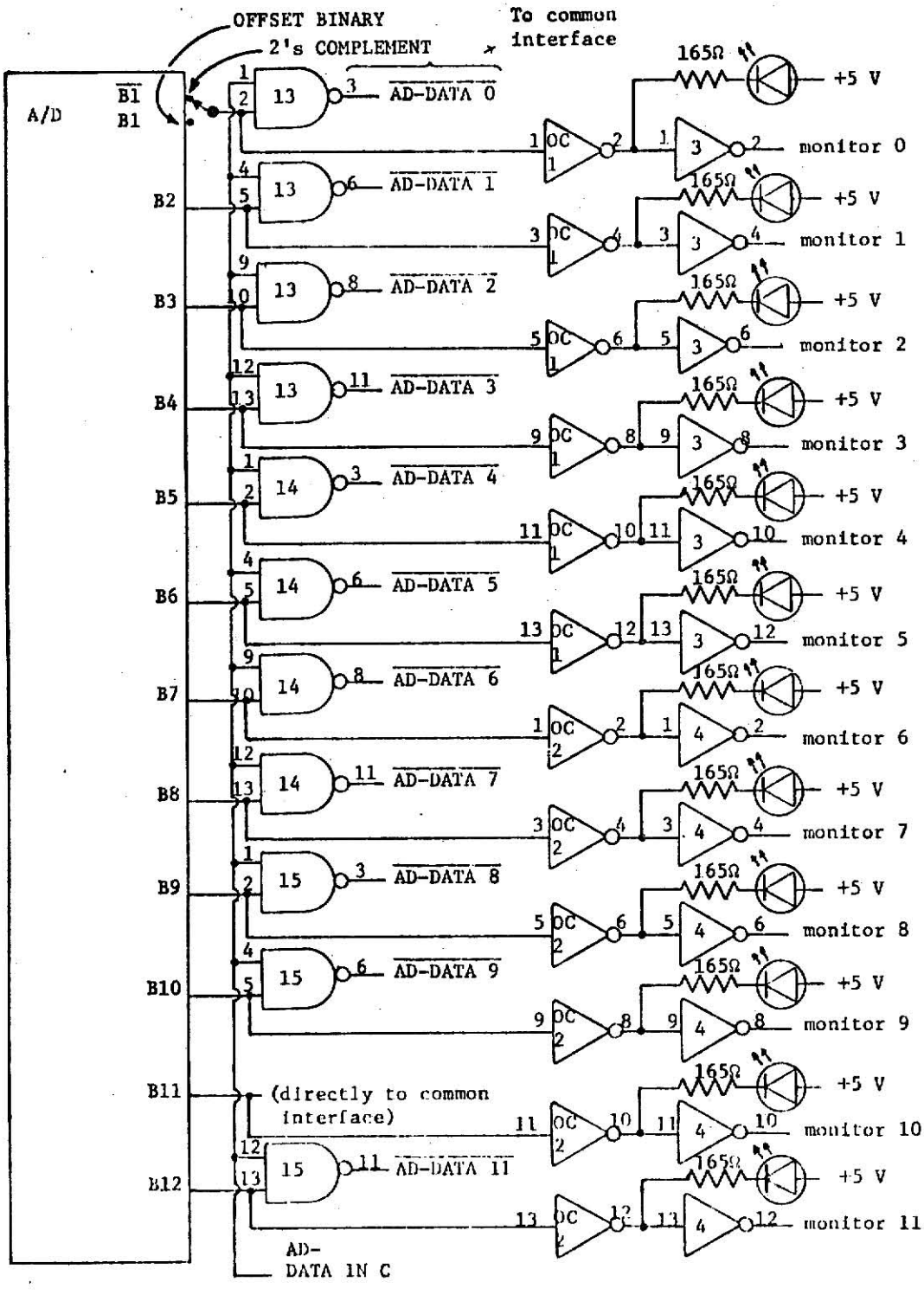
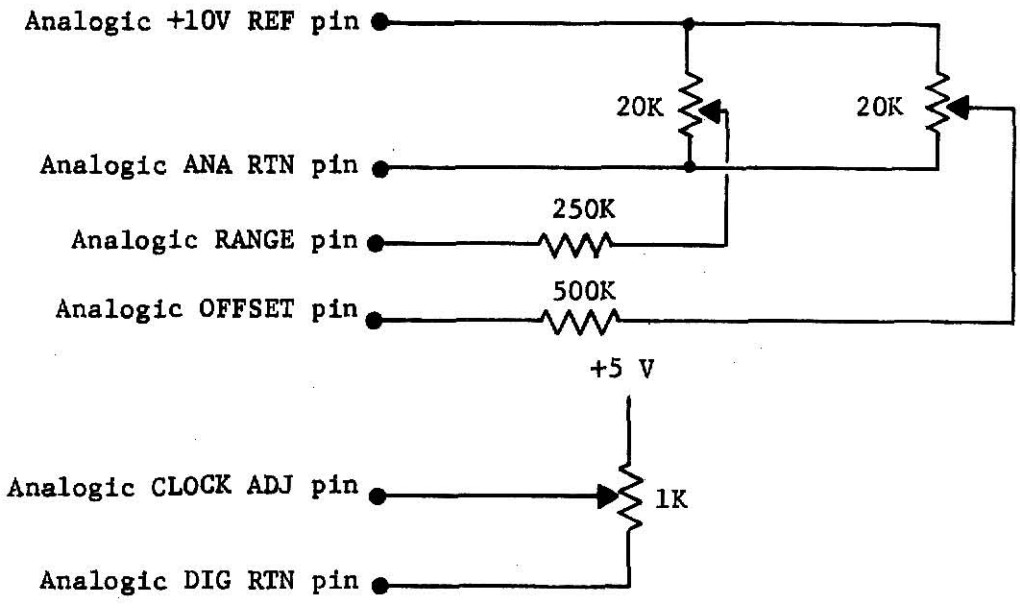


Fig. A-15. Analog-digital output gates



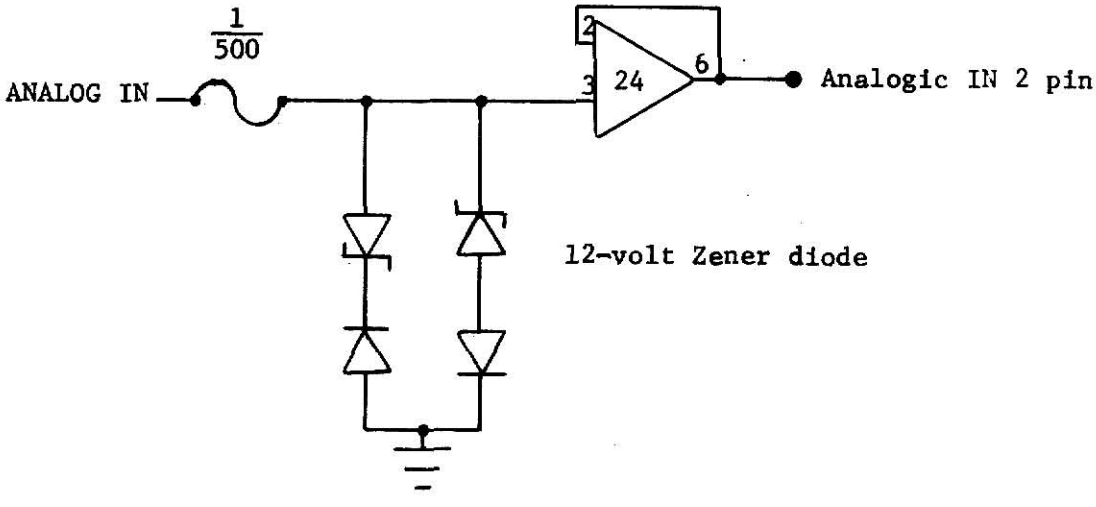
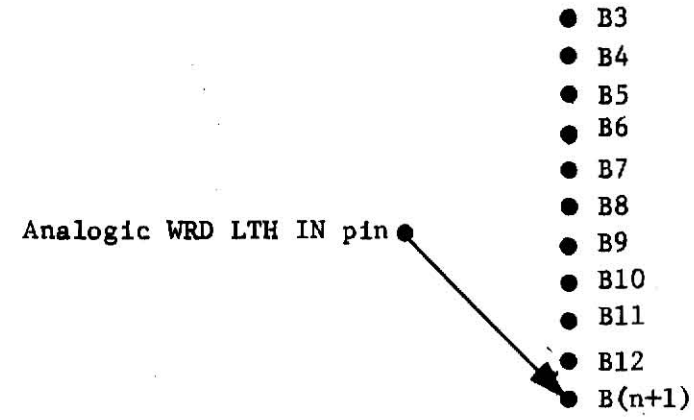


Fig. A-16. Analog-digital trimmer potentiometers and input protection circuitry



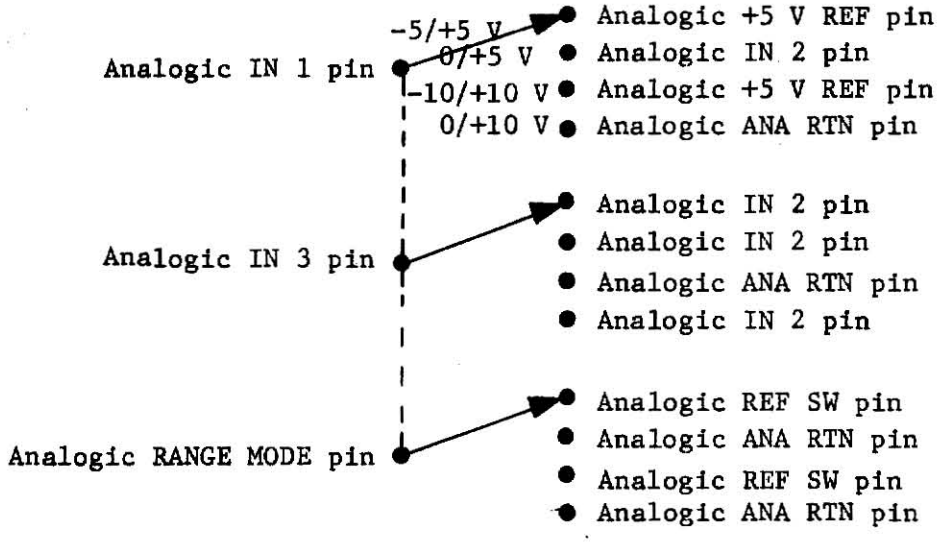


Fig. A-17. Analog-digital OUTPUT WORD LENGTH and INPUT VOLTAGE switches

INTERFACE CONNECTOR PIN	TRANSPORT CONNECTOR / MATING CONNECTOR: LIVE PIN	GROUND PIN	SIGNAL (Winchester MRAC 104S-J6 / Winchester MRAC 104P-JTC6II)
			→ Interface Input
			← Interface Output
2	v	z	→ INTER-RECORD GAP Command (IRGC)
3	AD	AJ	→ FILE GAP Command (FGC)
4	AN	AT	→ WRITE STEP Command (WSC)
5	AX	BB	→ WRITE DATA 0 (WD0)
6	BF	BL	→ WRITE DATA 1 (WD1)
7	BR	BV	→ WRITE DATA 2 (WD2)
8	BZ	CD	→ WRITE DATA 3 (WD3)
9	CJ	CN	→ WRITE DATA 4 (WD4)
10	B	F	→ WRITE DATA 5 (WD5)
11	L	R	→ WRITE DATA 6 (9-channel system only) (WD6)
12	V	Z	→ WRITE DATA 7 (9-channel system only) (WD7)
13	n	s	→ ECHO CHECK RESET (Optional) (ECR)
22	q	u	← BUFFER 1 BUSY (B1B)
23	y	AC	← GAP IN PROCESS (GIP)
24	AH	AM	← ECHO CHECK PARITY ERROR (Optional) (ECP)
25	D	J	← END OF TAPE Marker (EOT)
26	N	T	← BEGINNING OF TAPE Marker (BOT)
27	X	b	← TAPE NOT TENSIONED (TNT)
28	g	k	← TRANSPORT READY (TRR)
29	AS	AW	← READ DATA 0 (RD0)
30	BA	BE	← READ DATA 1 (RD1)
31	BK	BP	← READ DATA 2 (RD2)
32	BU	BY	← READ DATA 3 (RD3)
33	CC	CH	← READ DATA 4 (RD4)
34	CM	CS	← READ DATA 5 (RD5)
35	C	H	← READ DATA 6 (9-channel system only) (RD6)
36	M	S	← READ DATA 7 (9-channel system only) (RD7)
37	W	a	← READ DATA P (Parity) (RDP)
38	f	j	← READ DATA STROBE (RDS)
39	P	t	← DATA BUSY (DBY)
40	x	AB	← SPARE
14	CB	CF	→ DATA DENSITY SELECT (Optional) (DDS)
15	A	E	→ LOAD FORWARD Command (LFC)
16	U	Y	→ REWIND Command (RWC)
17	c	h	→ REMOTE RESET (RRS)
18	m	r	→ DISABLE MANUAL CONTROLS (DMC)
19	w	AA	→ SYNCHRONOUS FORWARD Command (SFC)
20	AE	AK	→ SYNCHRONOUS REVERSE Command (SRC)
41	BW	AU	← -5 volts } For monitoring only; not
42	CA		← +5 volts } for customer use
43	CE		← 0 volt
44	CP		← CHASSIS GROUND
45	CL		← -10 volts } For monitoring only; not
46	CR		← +10 volts } for customer use
47	AF	AL	← FILE PROTECT (FPT)
21	AP		→ WRITE/READ STATUS (WRS)
48	AR	AV	← MOTION CHECK

Fig. A-18.
Incremental Write/Synchronous Read DTL Interface Signals

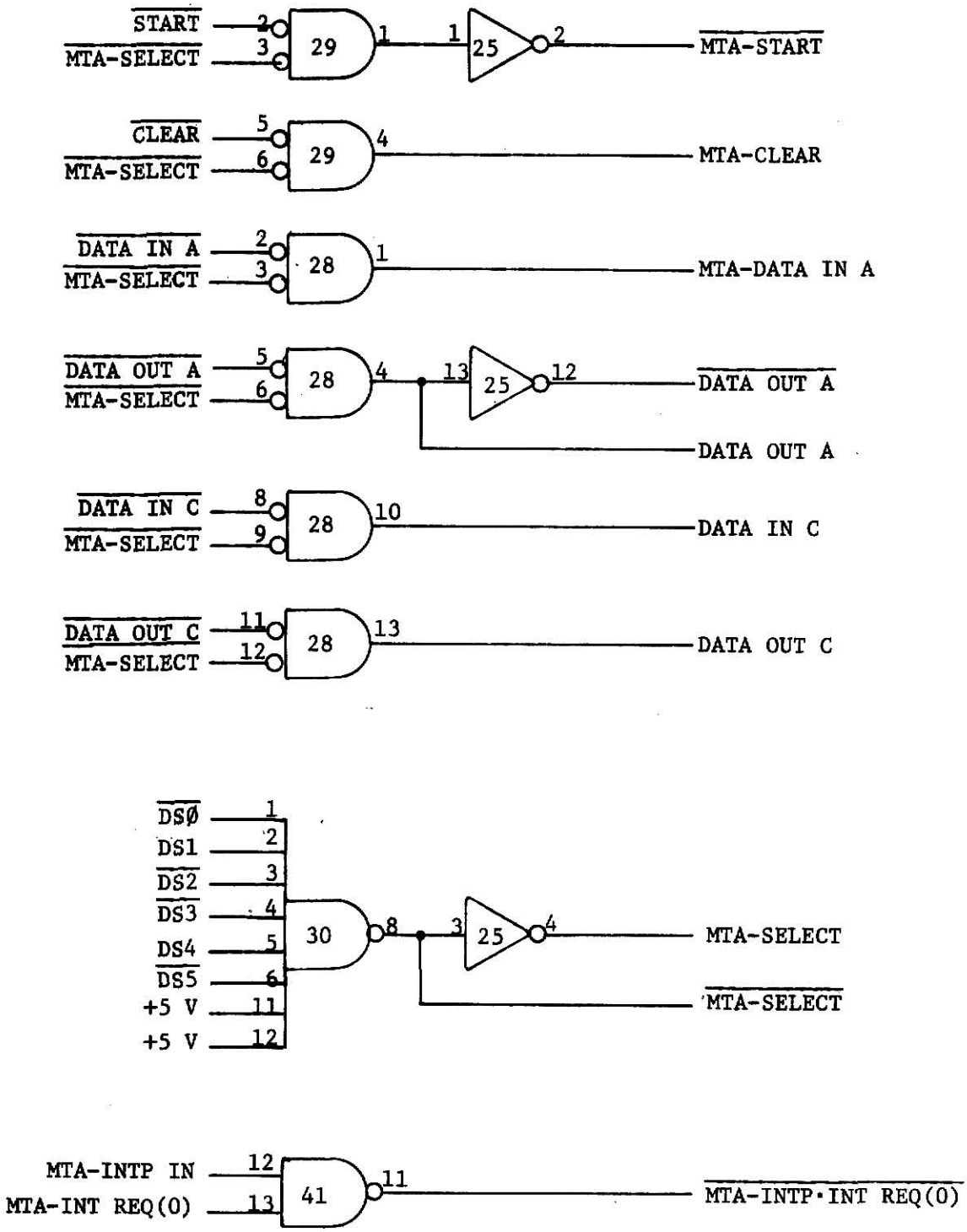


Fig. A-19. Tape transport control signals from the common logic

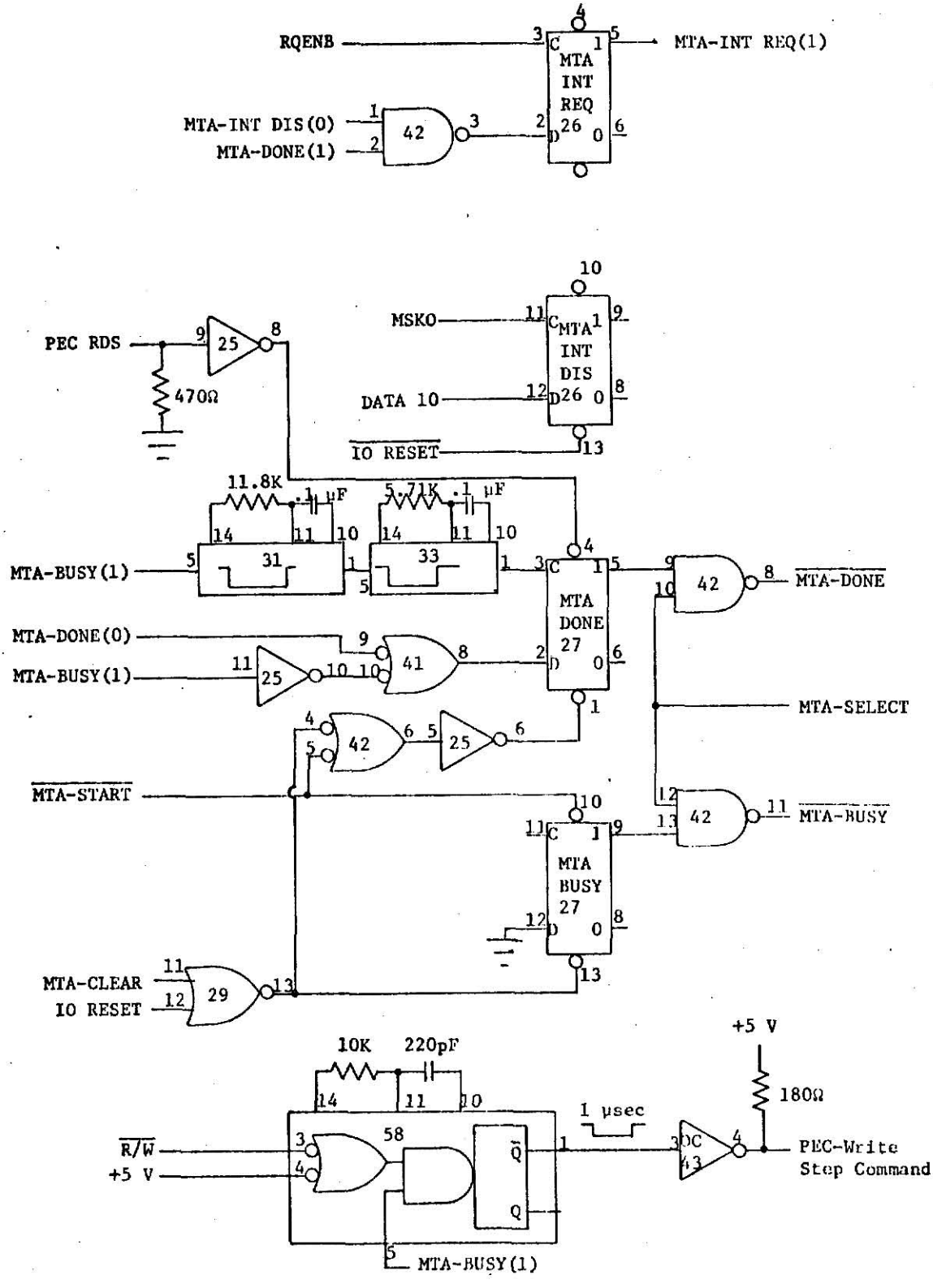


Fig. A-20. Tape transport Busy/Done implementation

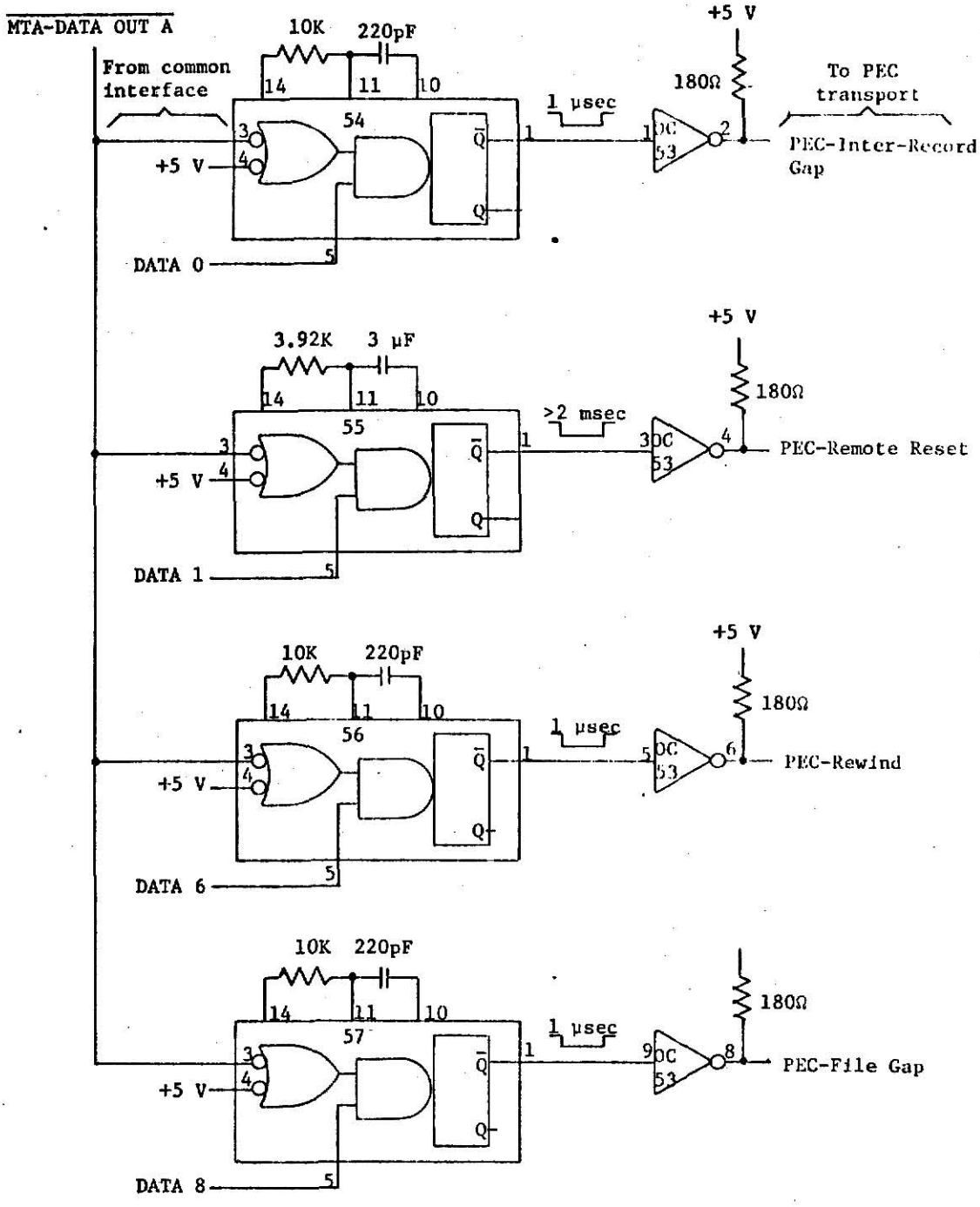


Fig. A-21. Tape transport command register monostables

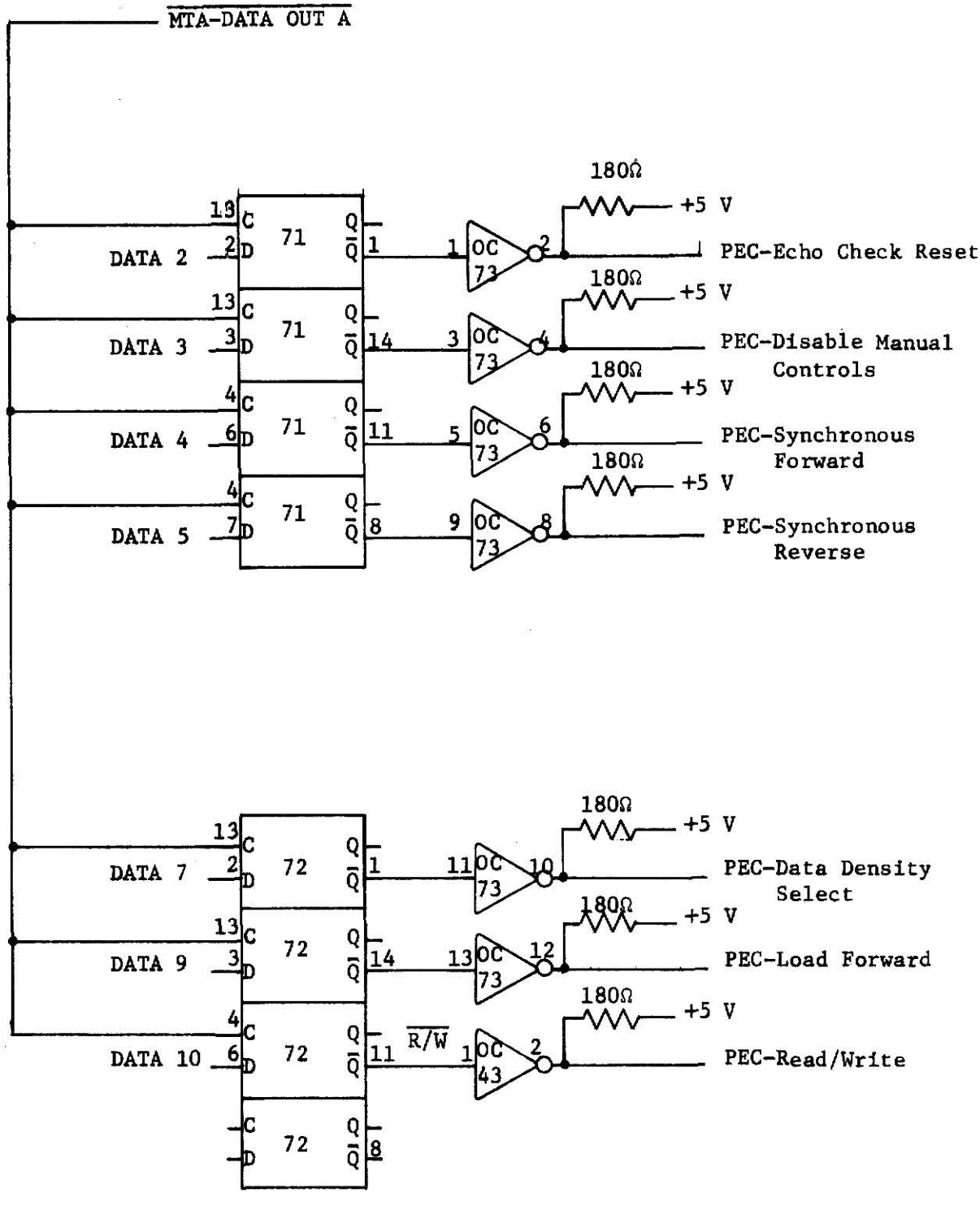


Fig. A-22. Tape transport command register latches

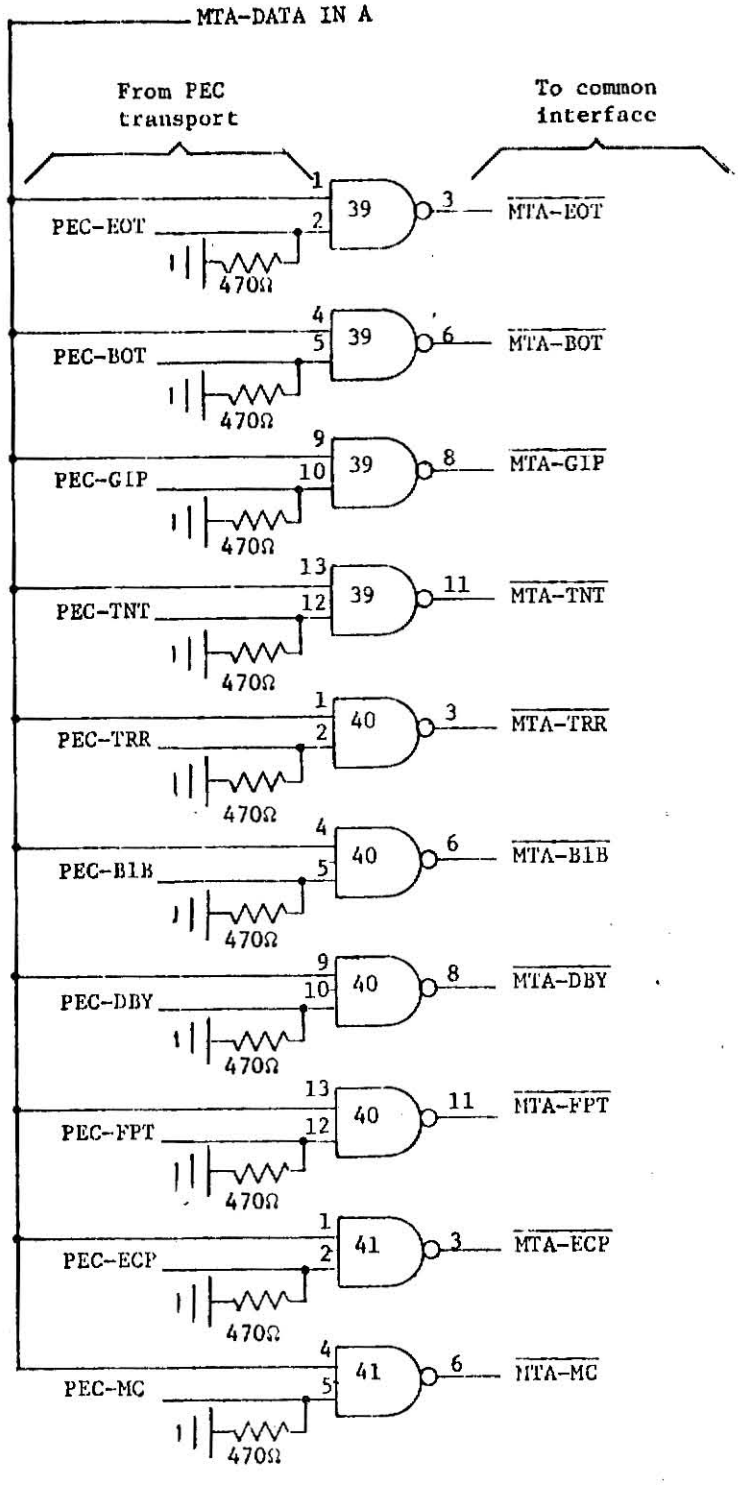


Fig. A-23. Tape transport status gates

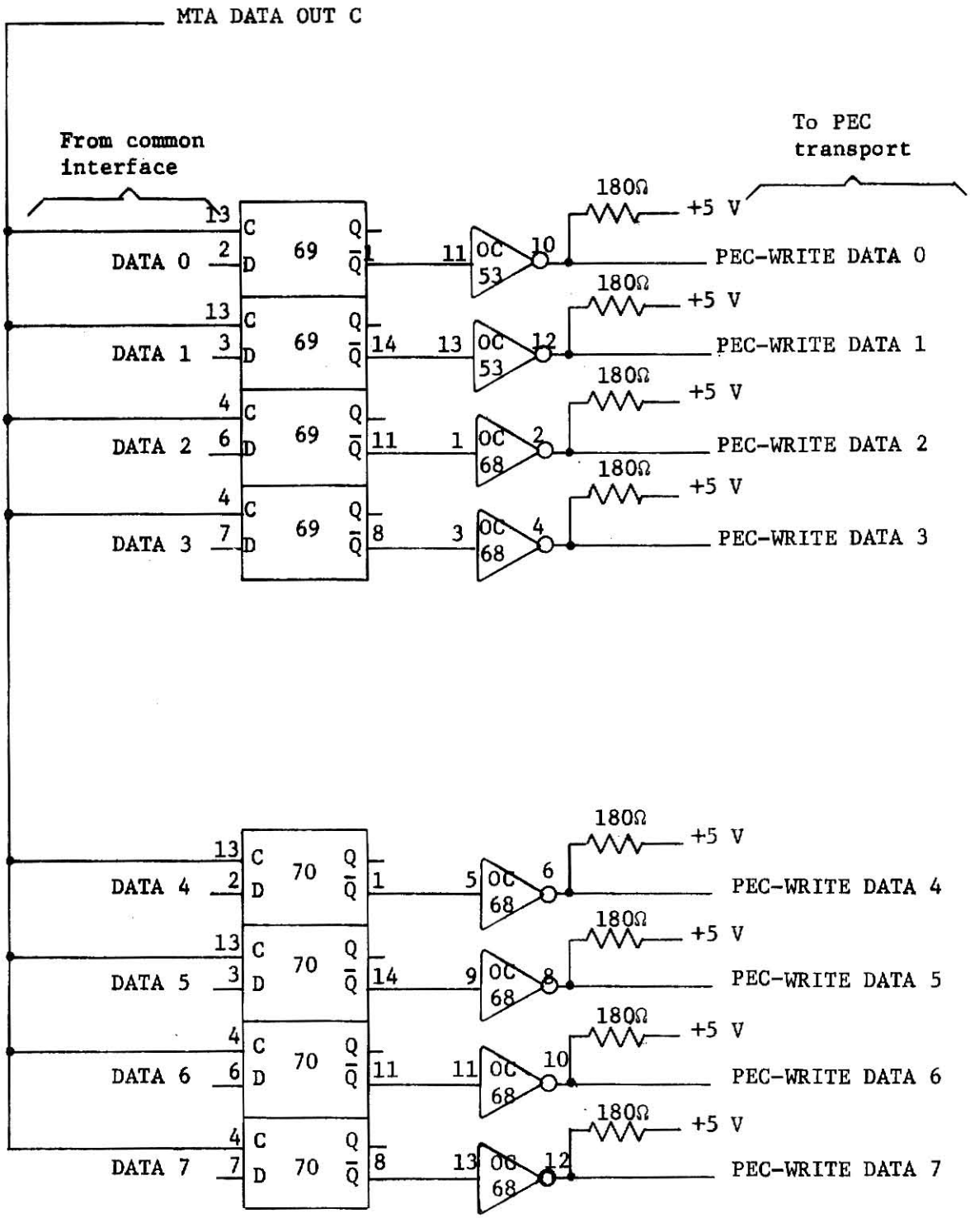


Fig. A-24. Tape transport data output registers

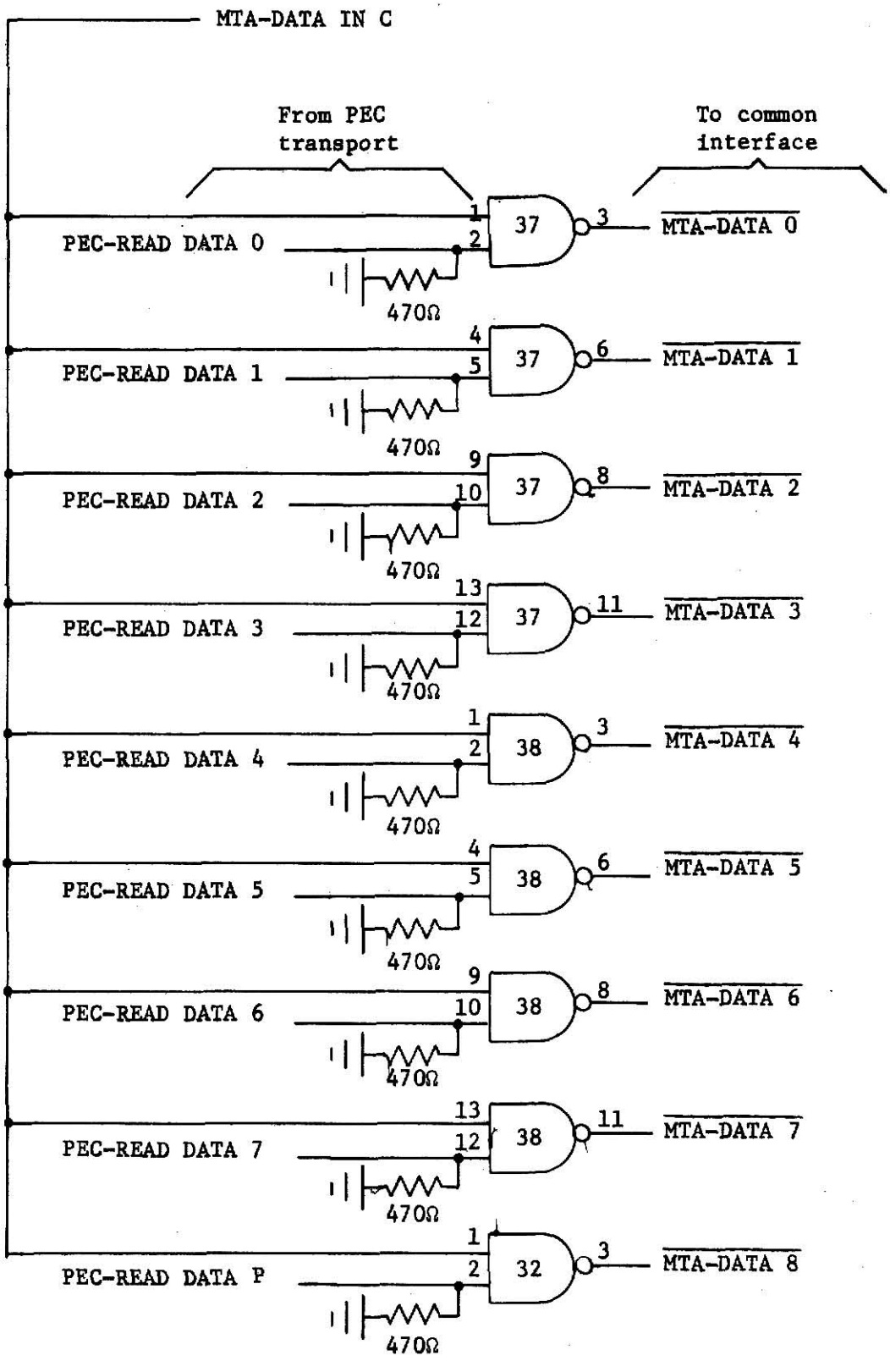


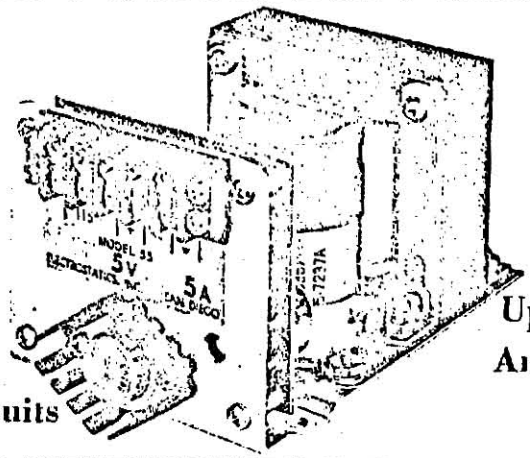
Fig. A-25. Tape transport data input registers

APPENDIX B

Manufacturers' Data Sheets

MODEL 55 DC POWER SUPPLIES

SINGLE VOLTAGE $59



DUAL VOLTAGE $69

Designed especially for use with Integrated Circuits

Up to 60 Watts Any DC Voltage 3 to 30

DELIVERY FROM STOCK

ONE YEAR WARRANTY

FOR SAN DIEGO

SATISFACTION GUARANTEED

Electrical Specifications:

INPUT: 105-125 VAC. 50—420 Hz
REGULATION: LINE —0.005% OR 2 MV MIN (10 VOLT CHANGE)
LOAD: 0.05% OR 10 MV MIN (FULL LOAD CHANGE)
RIPPLE: LESS THAN 250 MICROVOLTS
IMPEDANCE: 100 Hz — 0.001 OHMS
1 KHz — 0.005 OHMS
10 KHz — 0.01 OHMS
100 KHz — 0.1 OHMS
RECOVERY TIME: 25 MICROSECONDS
OVERSHOOT: NONE ON TURN ON OR OFF
TEMPERATURE: OPERATING −40 TO +71°C
STORAGE −65 TO +85°C
COEFFICIENT 0.01%/°C MAX
CURRENT LIMITING: FIXED · FOLDBACK TYPE · AUTOMATIC RECOVERY
OUTPUT: FLOATING.
SEMICONDUCTORS: SILICON
CAPACITORS: COMPUTER GRADE — 10 YEAR LIFE
OVERVOLTAGE PROTECTION: FIXED CROWBAR · OPTIONAL
WEIGHT: 4.25 LBS

Ordering Information:

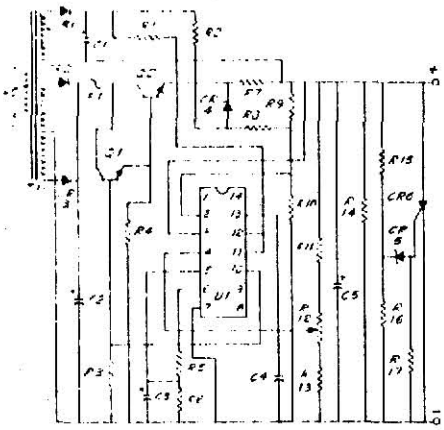
SINGLE OUTPUT (Models 55 · 3 thru 55 · 30)	PRICE	WITH OVERVOLTAGE
1 · 9	$59 ea.	$65 ea.
10 · 24	$56 ea.	$60 ea.
DUAL OUTPUT (Models 55 · 1212 thru 55 · 1818)		
1 · 9	$69 ea.	$79 ea.
10 · 24	$65 ea.	$74 ea.

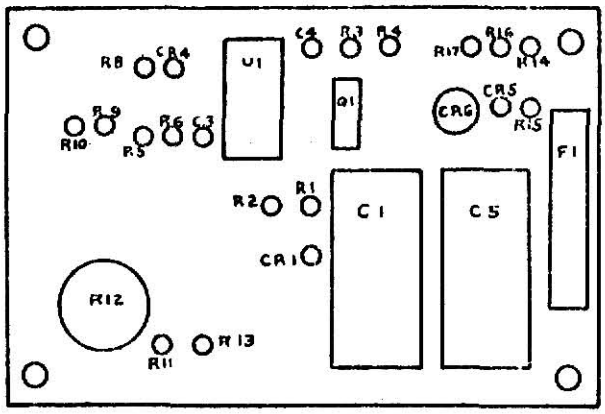
Model	Voltage	Amps
55 · 3	2.5 · 3.5	5.0
55 · 4	3.5 · 4.5	5.0
55 · 5	4.5 · 5.5	5.0
55 · 6	5.5 · 6.5	4.5
55 · 7	6.5 · 7.5	4.5
55 · 8	7.5 · 8.5	4.5
55 · 9	8.5 · 9.5	4.0
55 · 10	9.5 · 10.5	4.0
55 · 11	10.5 · 11.5	4.0
55 · 12	11.0 · 13.0	3.0
55 · 14	13.0 · 15.0	3.0
55 · 16	15.0 · 17.0	3.0
55 · 18	17.0 · 19.0	2.5
55 · 20	19.0 · 21.0	2.0
55 · 22	21.0 · 23.0	2.0
55 · 24	23.0 · 25.0	2.0
55 · 26	25.0 · 27.0	2.0
55 · 28	27.0 · 29.0	2.0
55 · 30	29.0 · 30.0	2.0
55 · 1212	±11.0 · 13.0	1.0
55 · 1515	±14.0 · 16.0	1.0
55 · 1818	±17.0 · 19.0	1.0

Elantec Inc.
7718 CLAIREMONT MESA BOULEVARD
SAN DIEGO, CALIFORNIA 92111 / (714) 279-1414

DC POWER SUPPLY

MODEL 55-5





RESISTORS

R1,8,14	100	RL20
R2,4,9,16,17	1K	RL20
R3	10K	RL20
R5	910	RL20
R6,11,13	510	RL20
R7	.05	WW
R10	2.2K	RL20
R12	500	POT
R15	27	RL20

CAPACITORS

C1	500 MFD	15V
C2	9200 MFD	15V
C3	4.7 MFD	50V
C4	1000 mmfd	
C5	500 MFD	15V

SEMICONDUCTORS

U1	Regulator 723C
Q1	2N5296
Q2	2N3055
CR1,4	1N4002
CR2,3	VTA200/T (VARO)
CR5	1N752A (5.6V)
CR6	40654 (RCA)

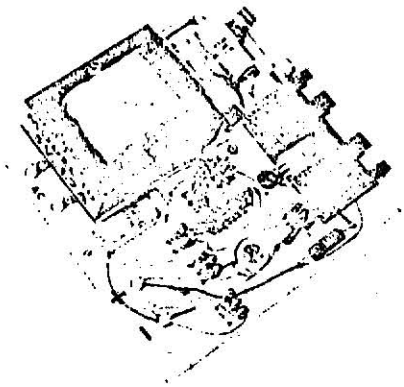
F1	Fuse AGC6
T1	Transformer 55T5

NOTE: F1, R15, R16, R17, CR5, and CR6 are on units with overvoltage option only.

MODEL 10 DC POWER SUPPLIES

SINGLE VOLTAGE $27
DUAL $35

Designed especially for IC's, logic circuits, and test equipment



Up to 10 watts any DC voltage 3 to 30

Immediate Delivery From Stock

Electrical Specifications:

INPUT: 105-125 VAC. 50-420 Hz

REGULATION: LINE: 0.005% or 2 mv MIN (10 VOLT CHANGE)
LOAD: 0.05% or 10 mv MIN (FULL LOAD CHANGE)

RIPPLE: LESS THAN 250 MICROVOLTS

IMPEDANCE: 100 Hz - 0.001 OHMS
1 KHz - 0.005 OHMS
10 KHz - 0.01 OHMS
100 KHz - 0.1 OHMS

RECOVERY TIME: 25 MICROSECONDS

OVERSHOOT: NONE ON TURN ON OR OFF

TEMPERATURE: OPERATING -20 TO +71° C
STORAGE -65 TO +85° C
COEFFICIENT 0.01%/°C MAX

CURRENT LIMITING: FIXED - FOLDBACK TYPE - AUTOMATIC RECOVERY

OUTPUT: FLOATING

SEMICONDUCTORS: SILICON

CAPACITORS: COMPUTER GRADE 10 YEAR LIFE

OVERVOLTAGE PROTECTION: OPTIONAL

WEIGHT: 1.2 LBS

*Model	Voltage	Amps
10-5	4.5-5.5	1.2
10-12	11-13	0.8
10-15	14-16	0.6
10-24	23-25	0.4
10-28	26-30	0.35
10-1212	±11-13	0.35
10-1515	± 14-16	0.35
10-1818	±17-19	0.35

ANY OUTPUT TO 30 VOLTS AVAILABLE

Quantity	Single Supplies	Single With OV*	Dual Supplies	Dual With OV
1 - 9	$27 ea.	$32 ea.	$35 ea.	$45 ea.
10 - 24	$24 ea.	$28 ea.	$32 ea.	$41 ea.

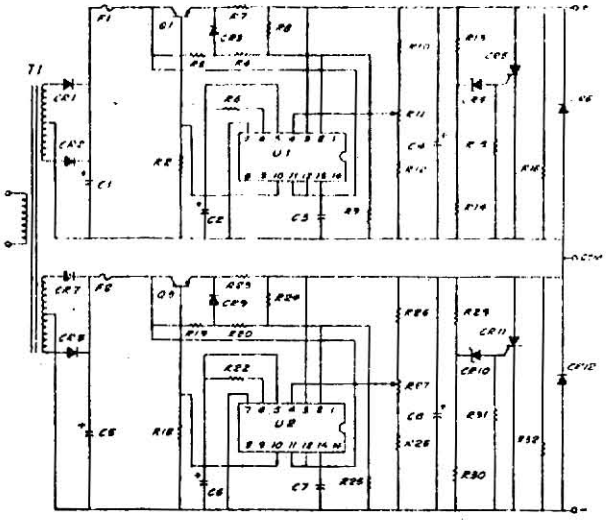
*FOR OVER VOLTAGE MODELS ADD -0 TO MODEL NUMBER

Low Cost and Reliable DC Power Supplies

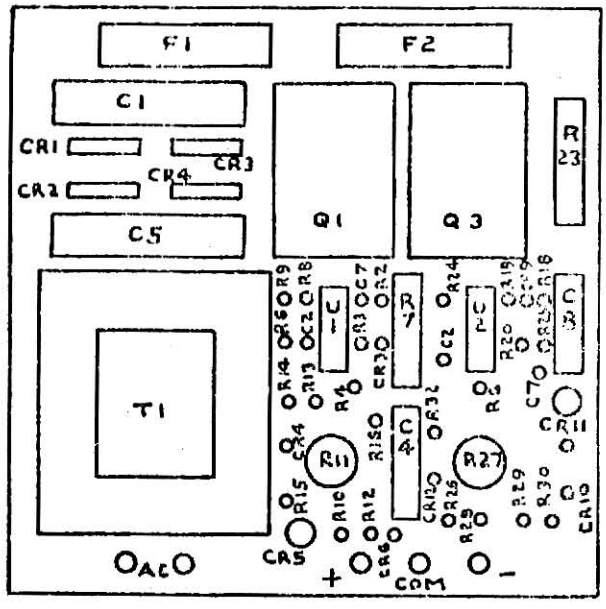
Electrostatics, Inc.
7718 CLAIREMONT MESA BOULEVARD
SAN DIEGO, CALIFORNIA 92111 / (714) 279-1414

DC POWER SUPPLY

MODEL 10-1515



SCHEMATIC

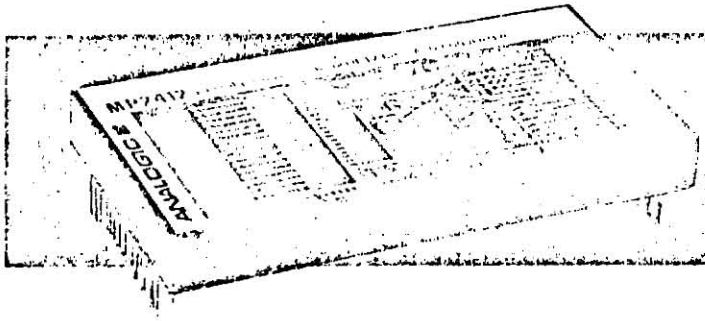


PC BOARD LAYOUT

PARTS LIST

C1,5	860 MFD	30V		R2,18	10K RL20
C2,6	4.7 MFD	10V		R3,19	750 RL20
C3,7	1000 mmfd	200V		R4,20	100 RL20
C4,8	47 MFD	25V		R6,22	910 RL20
CR1,2,3,6, 7,8,9,12		1N4002		R7,23	1.0 BWH
CR4,10		Zener 1N4742		R8,15,24,31	1K RL20
CR5,11		SCR 40654		R9,25	2.7K RL20
U1,2		Regulator 723		R10,26	680 RL20
T1		Transformer 10T1515		R11,27	500 POT
F1,2		Fuse AGC1		R12,14,28,30	820 RL20
				R13,29	220 RL20
				R16,32	910 RL20

NOTE: R13,14,15,29,30,31,CR4,5,10, & 11 are only on units with overvoltage protection.



MP2410/MP2412
economical, high speed 10 & 12-bit A/D CONVERTERS

GENERAL DESCRIPTION

Analogic's MP2410 and MP2412 are extremely low cost, high speed, highly accurate, stable, and highly reliable analog-to-digital converters. Housed in a small 4" x 2" x 0.4" MODUPAC™ these fast (40 microseconds for 12 bits) and highly reliable (250,000 hours MTBF) converters provide substantial space and cost economies in high speed-medium resolution digitizing systems. The high accuracy and differential linearity (0.012%) plus the high stability (differential linearity tempco is 5PPM/°C) of the MP2412 assure high performance in all general purpose applications.

PERFORMANCE ACHIEVEMENTS

The high digitizing rate of 25,000 conversions per second with an accuracy and differential linearity of 0.012% and the high stability of the MP2412 are economically achieved by extensive utilization of MSI and other advanced components. While producing a fast, accurate and stable converter, the broad use of MSI reduces the total parts count thus enhancing reliability. Reliability is further increased by employing the latest manufacturing and automatic testing procedures in the construction and checkout of this ADC. Implementing these and similar techniques assures that the MP2410 and the MP2412 provide highly reliable and economical analog-to-digital conversion.

The MP2412 is an extremely flexible system component useful in many digitization applications. The input full scale voltage range is pin selectable as is the output digital resolution and binary code. The serial data output allows A/D conversion at the analog source and provides single-line transmission of the digitized data to remote equipment. The accessible reference control permits rationetric digitization for use in tracking applications.

FEATURES

- Low Cost-MP2412: $75 (100's)
  ...MP2410: $65 (100's)
- High Thru-Put
  ...up to 50KHz
- High Accuracy and Linearity
  ...within 0.012%
- Low Parts Count
  ...only 46 components
- High Reliability
  ...250,000 hours MTBF

APPLICATIONS

- Instrumentation Systems
- Computer Controlled Industrial Processing
- Data Scanning Systems

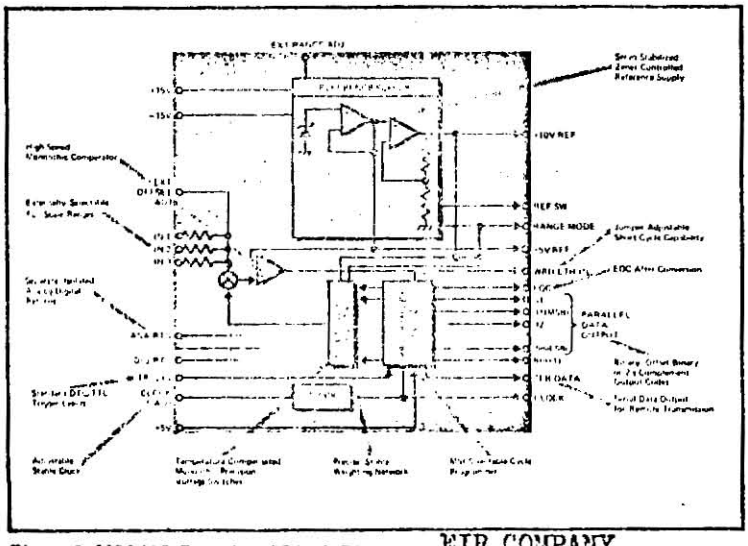


Figure 1. MP2412 Functional Block Diagram.

ANALOGIC®
... The Digitizers

Audubon Road ■ Wakefield, Massachusetts 01880
TWX (710) 348-0428 Tel. (617) 246-0300

EIR COMPANY
Suite 205, 6405 Metcalf
Shawnee Mission, Kansas 66202
913 - 362 - 0114

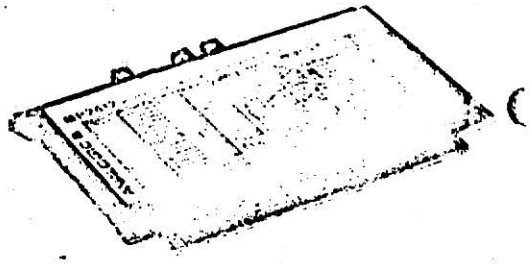
W. G. (Bill) Rieland

SPECIFICATIONS

ANALOG INPUT	
Input Voltage (Full Scale Range)	Pin selectable: −10V to +10V, 0V to +10V, −5V to +5V, or 0V to +5V (See Fig. 11)
Input Impedance	Depends on FSR. See Fig. 11
ACCURACY (@25°C)	
Resolution	Pin selectable: 2 to 12 bits (MP2412); 2 to 10 bits (MP2410)
*Absolute Accuracy	±0.012% FSR (MP2412); ±0.05% FSR (MP2410)
**Relative Accuracy	±0.012% FSR (MP2412); ±0.05% FSR (MP2410)
**Differential Linearity	±0.012% FSR (MP2412); ±0.05% FSR (MP2410)
Quantizing Error	±½ LSB
3σNoise (Includes Reference Noise)	0.01% FSR P-P referred to input
Monotonicity	Guaranteed
Missing Codes	None at optimum linearity. Refer to Fig. 8A.
STABILITY	
Tempco of Differential Linearity	<±6ppm/°C FSR
Tempco of Gain	<±25ppm/°C Reading
Tempco of Offset	<±20ppm/°C FSR
Power Supply Sensitivity	±0.0012%/% change in supply voltage
Repeatibility	Defined by Noise and Accuracy
CONVERSION TIME	
Total Conversion	*Adjustable: 24 to 48 μsec for 12 bits,* 20 to 40 μsec for 10 bits (See Figures 9 and 9A)
DIGITAL SIGNALS	
Parallel Output (See Timing Diagram, Fig. 3)	Binary: B1, B1 to B12. TTL compatible, 2 unit loads/line
Serial Output (See Timing Diagram, Fig. 3)	Negative pulses simultaneous with clock pulse for "0" bits
Output Coding	Pin selectable: Binary, Offset Binary, 2's complement, 1's complement; Available with external circuitry, see Fig. 10
Trigger Input	Standard TTL. See Timing Diagram
Trigger Input Transition	<200nsec (90% to 10%)
End of Conversion, EOC	"0" level transition, nominally 100nsec after LSB data pulse. TTL compatible, 9 loads *(See Timing Diagram)*
EOC Transition	<20nsec (10% to 90%)
Clock Output	TTL compatible (See Timing Diagram)
Clock Stability	±0.1%/°C
Clock Output Capacitive Load	30pF maximum allowable
Selectable Word Length	2 to 12 bits (MP2412); 2 to 10 bits (MP2410) (See page 3)
POWER SUPPLY	
+15V ±3%	25 mA
−15V ±3%	10 mA
+ 5V ±5%	200 mA
ENVIRONMENTAL, PHYSICAL, & RELIABILITY	
Maximum Input Without Damage	±15V
Warm-up Time to Stated Accuracy	<5 minutes
Operating Temperature	0°C to +70°C
Storage Temperature	−25°C to +85°C
Relative Humidity	5% to 95% non-condensing
Mechanical Configuration	Encapsulated plastic case†
Packaging MP24XX	2" x 4" x 0.4" Modupac (See Fig. 4)
Packaging AN24XX	MP24XX on plug-in P.C. card (See Fig. 12)

Analogic may upgrade these specifications at any time.
* Refer to CALIBRATION section and Figs. 5-8
**See Figure 9A
†For OEM quantities the standard metal case is available for use in severe noise environments

AN2412 (PC card mounted MP2412)



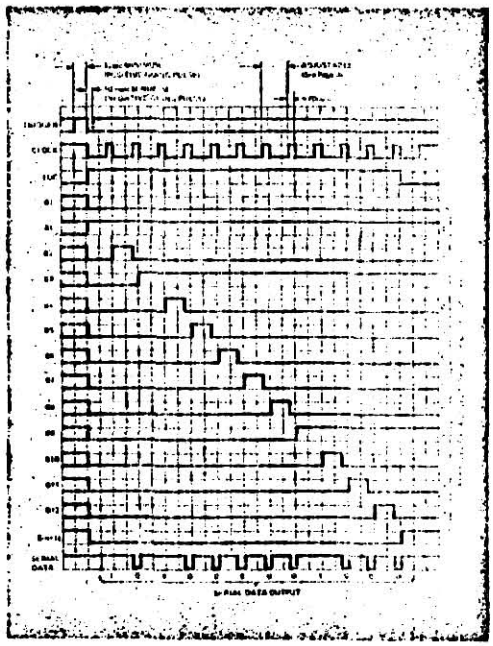


Figure 3. Timing Diagram for MP2412 showing nominal waveforms for 6.2695 volts input at 0 to +10V FSR.

Binary Output Coding*

The input full scale voltage range and the output digital code are pin selectable. The input voltage-to-output code transfer functions are shown below.

10 BIT RESOLUTION		12 BIT RESOLUTION	
Unipolar binary:		**Unipolar binary:**	
+ 9.990V	= 1 111 111 111	+ 9.9976V	= 111 111 111 111
0.000V	= 0 000 000 000	0.0000V	= 000 000 000 000
	B1.....B10		B1.....B12
Offset binary:		**Offset binary:**	
+ 9.980V	= 1 111 111 111	+ 9.9951V	= 111 111 111 111
0.000V	= 1 000 000 000	0.0000V	= 100 000 000 000
−10.000V	= 0 000 000 000	−10.0000V	= 000 000 000 000
	B1.....B10		B1.....B12
Two's complement:		**Two's complement:**	
+ 9.980V	= 0 111 111 111	+ 9.9951V	= 011 111 111 111
0.000V	= 0 000 000 000	0.0000V	= 000 000 000 000
−10.000V	= 1 000 000 000	−10.0000V	= 100 000 000 000
	B1, B2.....B10		$\overline{B1}$, B2.....B12

*10 volt units only. For 5 volt units divide input shown by 2.

Figure 2. Input/Output Coding Table.

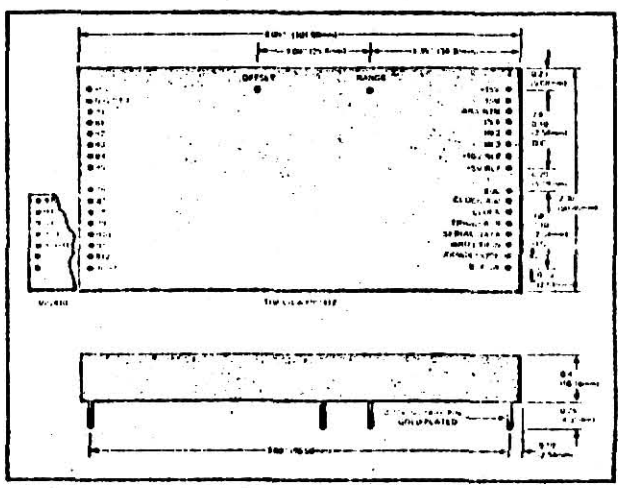


Figure 4. MP2412 Outline Configuration.

CALIBRATION AND OPERATION

Linearity and relative accuracy of the MP2410 and MP2412 is built in. Absolute accuracy is implemented by adding the external circuitry described in Figures 6 and 8 and calibrating the zero offset and full scale range.

Zero Offset Adjust

Apply the input voltage shown in the accompanying table and adjust the OFFSET potentiometer so that the LSB of the output codes listed in the table alternates equally between "1" and "0". OFFSET should be readjusted whenever the selected full scale range is changed.

F.S. Range	MP2410 or AN2410		MP2412 or AN2412	
	Input Voltage	Output Code ($B_1, B_2, \ldots B_{10}$)	Input Voltage	Output Code ($B_1, B_2, \ldots B_{12}$)
−10V to +10V	+0.0098	1 000 000 000/1	+0.0024	100 000 000 000/1
0V to +10V	+0.0049	0 000 000 000/1	+0.0012	000 000 000 000/1
− 5V to + 5V	+0.0049	1 000 000 000/1	+0.0012	000 000 000 000/1
0V to + 5V	+0.0024	0 000 000 000/1	+0.0006	000 000 000 000/1

Figure 5. Offset Calibration Chart

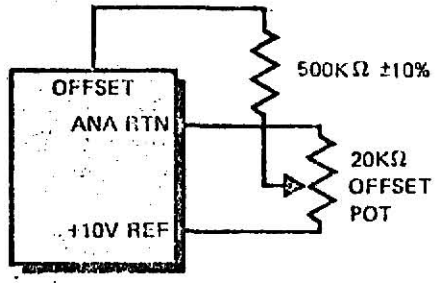


Figure 6. Connection for Offset Adjustment.

Range Adjust **Zero offset should be calibrated before adjusting RANGE.** Apply the input voltage as shown in the accompanying table. Adjust the RANGE potentiometer so that the LSB of the output code, 111...110/1(B_1, B_2, ...$B_{(n)}$), alternates equally between "1" and "0". RANGE should be readjusted whenever the selected full scale range is changed.

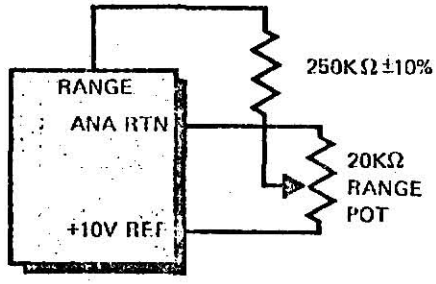


Figure 8. Connection for Range Adjustment.

F.S. Range	MP2410 or AN2410	MP2412 or AN2412
	Input Voltage	Input Voltage
−10V to +10V	+9.9706	+9.9927
0V to −10V	+9.9853	+9.9964
− 5V to + 5V	+4.9853	+4.9964
0V to + 5V	+4.9927	+4.9982

Figure 7. Range Calibration Chart

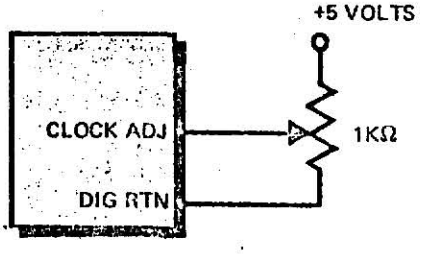


Figure 9. Connection for Clock Adjustment.

Conversion Speed Adjust

Conversion time may be set from 2.0μsec/bit to 4.0μsec/bit by adding the circuitry described in Fig. 9 and adjusting the clock frequency. An open CLOCK ADJ terminal results in a 2.5μsec/bit conversion time. Some deterioration in accuracy may occur at the higher clock speeds. (See Fig. 9A).

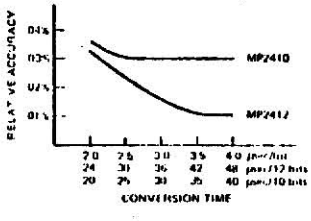


Figure 9A. Relationship of Relative Accuracy to Conversion Time.

Output Word Length Selection

The number of bits in the output word is pin selectable. To operate the ADC at its full capacity B(n+1) must be connected to WRD LTH IN. This connection is factory installed on the PC card for all AN versions ordered and must be removed when operating at less than full capacity. To operate the converter at less than its full digital output capacity WRD LTH IN must be connected only to the terminal identified as one bit more than the desired number of bits out.

EXAMPLE: When the ADC is operated as an 8-bit converter, connect WRD LTH IN to B9 only.

Ratiometric A/D Conversion

Ratiometric A/D conversion is available with the MP2410 and MP2412. Write for application note showing details.

One's Complement

One's complement output code may be obtained by connecting the converter as shown in Figure 10.

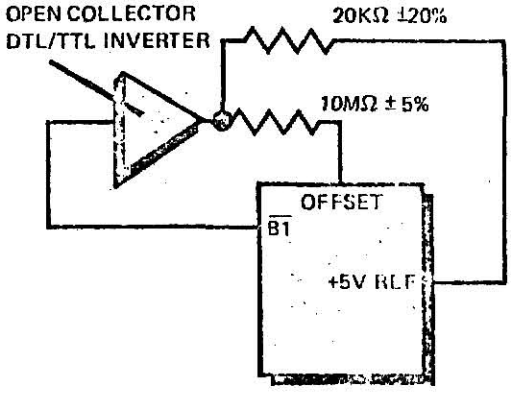


Figure 10. Connection for One's Complement.

Input Voltage Range Selection

The full scale input voltage range can be selected by making the connections according to the following tables.

MODUPAC MP2412 OR MP2410

RANGE	INPUT IMPEDANCE	IN 1	IN 2	IN 3	RANGE MODE
−10V to +10V	10,000Ω	TO +5V REF	TO INPUT	TO ANA RTN	TO REF SW
0V to +10V	5,000Ω	TO ANA RTN	TO INPUT	TO INPUT	TO ANA RTN
− 5V to + 5V	5,000Ω	TO +5V REF	TO INPUT	TO INPUT	TO REF SW
0V to + 5V	2,500Ω	TO INPUT	TO INPUT	TO INPUT	TO ANA RTN

P.C. CARD AN2412 OR MP2410

RANGE	INPUT IMPEDANCE	PIN 17	TERMINALS ON CARD	
−10V to +10V	10,000Ω	TO Pin V	E28 to E31,	E36 to E50
0V to +10V	5,000Ω	TO Pin 19	E28 to E29,	E33 to E34
− 5V to +5 V	5,000Ω	TO Pin V	E29 to E50,	E33 to E34
0V to + 5V	2,500Ω	TO Pin 19	E33 to E34,	E33 to E36

Figure 11. Range Selection Tables Showing the Jumper Connections Needed for FSR Required. Analog and digital ground must be connected so that the voltage between them does not exceed 300mV.

ORDERING INFORMATION

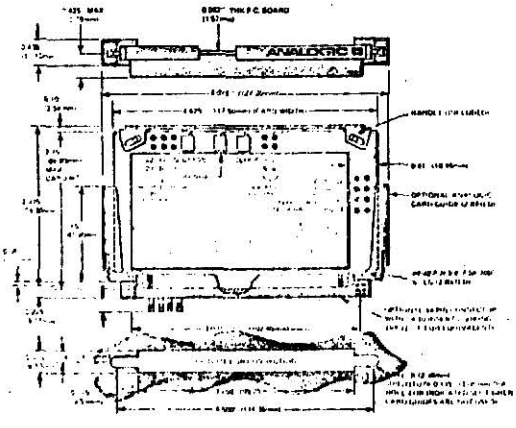
Simply specify

Configuration

For	*Enter*
12 Bit Modupac	MP2412
MP2412 on a PC card	AN2412*
10 Bit Modupac	MP2410
MP2410 on a PC card	AN2410*

* For OEM quantities or as part of a system order, FSR connections (See Fig.11) are made at the factory. The part number should be adjusted as follows: For 0 to +10V, add −1; −10V to +10V, add −2; −5V to +5V, add −3; 0V to +5V, add −4. For example a AN2412-2 is a 12 bit ADC with −10V to +10V FSR.

OUTLINE DRAWING



TERMINAL DESIGNATION

E 1	ANA RTN
E 2	ANA RTN
E 3	IN 2
E 5	CLOCK ADJ
E 6	+5V
E20	WRD LTH IN
E21	WRD LTH IN
E22	WRD LTH IN
E25	B(n+1)*
E26	B11*
E27	B9
E28	ANA RTN
E29	IN 1
E31	IN 3
E33	ANA INPUT
E34	IN 3
E36	IN 1
E50	+5V REF

PIN DESIGNATION

TRIGGER IN	A 1		EOC
	B 2		
WRD LTH IN	C 3		B (n+1)*
	D 4		
B2 OUT	E 5		B1 OUT
B4 OUT	F 6		B3 OUT
B12 OUT	H 7		B6 OUT
B5 OUT	J 8		B8 OUT
B7 OUT	K 9		
CLOCK	L 10		SERIAL DATA
+5V	M 11		+5V
DIG RTN	N 12		DIG RTN
*B11 OUT	P 13		B10 OUT
$\overline{B1}$ OUT	R 14		B9 OUT
SIG RTN	S 15		ANA RTN
INPUT	T 16		INPUT
	U 17		RANGE MODE
REF SW	V 18		
ANA RTN	W 19		ANA RTN
−15V	X 20		−15V
+15V	Y 21		+15V
+10V REF OUT	Z 22		RANGE ADJ

*For MP2412 only. For AN2410 pin P and terminal E26 are B(n+1); pins 3 and H and terminal E25 are at binary "0".

Figure 12. AN24XX Outline Drawing, Jumper Terminal and Connector Pin Diagram.

ANALOGIC

Audubon Road ■ Wakefield, Massachusetts 01880 ■ Tel. (617) 246-0300 ■ TWX (710) 348-0425

In Europe: Baslerstrasse 88 ■ CH-4123 Allschwil ■ Switzerland ■ Tel. (061) 39 87 40

Bulletin No. 7038-20831

ZELTEX

D-A CONVERTERS
8-10-12 BIT BINARY HIGH SPEED
MODEL ZD440, 441, 442

CONVERSION PRODUCTS □ OPERATIONAL AMPLIFIERS □ POWER SUPPLIES

FEATURES

- 0 – 70°C OPERATION
- TTL/DTL COMPATIBLE
- 2 µs SETTLING TIME
- FITS STANDARD DIP MATRICES
- ADJUSTABLE FSR AND ZERO OFFSET
- MODELS INTERCHANGEABLE PIN-FOR-PIN

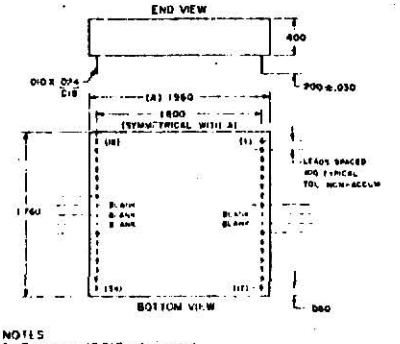
GENERAL DESCRIPTION

Models ZD440, 441 and 442 are fast settling digital-to-analog converters offering resolutions of 8-, 10-, or 12-bits binary and settling times as fast as 2 us.

Each converter, including its +10V reference, is completely self-contained in a small module. The converters are capable of being driven either from the internal reference, or from an external reference. When required, the internal +10V reference can be used to drive up to two additional ZELTEX 400 Series DAC's (if no external trim circuitry is connected to the reference). If external trimpots are used to adjust the full scale or offset, as shown in Fig. 1., the internal reference supply must be buffered. Full scale range selection is accomplished by jumpering pins, as shown in Table 1.

The leads are spaced to fit standard DIP pc boards such as AUGAT and CAMBION. In addition, the leads are coated with a special tin plating which meets the salt spray requirements of MIL-T-10727A.

OUTLINE DIMENSIONS



NOTES
1. Tolerance ±0.010 unless noted.
2. Leads "float" to accommodate error in connector location.
3. Case material: diallyl phthalate epoxy.
4. Leads: beryllium copper with special tin plating, meets the salt spray requirements of MIL-T-10727A.
5. Bottom surface double coated with epoxy – Dielectric insulation of 450 V-mil or greater.

PERFORMANCE SPECIFICATIONS

Typical @ 25°C and ±15V Power Supplies

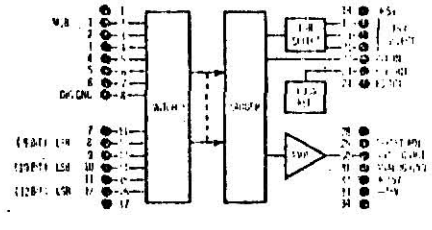
Model No.	ZD440	ZD441	ZD442
RESOLUTION	8 Bit	10 Bit	12 Bit
SETTLING TIME (to ½ LSB)			
0V to +10V	2 µs	5 µs	5 µs
−5V to +5 V	2 µs	5 µs	5 µs
−10V to +10V	5 µs	10 µs	10 µs
ACCURACY @ 25°C			
Scaling Error (% of Reading) Max.①	±0.1% (±0.005%/°C).	±0.1% (±0.005%/°C)	±0.05% (±0.002%/°C)
Zero Offset (% FSR) Max.① and ②	±0.2% (±0.002%/°C)	±0.05% (±0.002%/°C)	±0.05% (±0.002%/°C)
Linearity (% of FSR) Max.① and ②	±0.2% (±0.002%/°C)	±0.05% (±0.002%/°C)	±0.01% (±0.002%/°C)
Long Term Stability (% of FSR)⑦	±0.05%/10,000 Hr.		
INPUTS			
Data Coding	Modified 2's Complement Bipolar, Straight Binary Unipolar		
Data Configuration (TTL/DTL Compatible	Parallel, 1 Line/Bit		
Logic Levels	DTL/TTL Compatible, Positive True Logic		
Data Loading	1 TTL Load/Line		
External Reference Input	+10V @ 1.5 mA		
OUTPUTS			
Full Scale Range	User Selectable Via Wire Jumpers 0V to +10V, ±10V or ±5V		
Output Drive (Short Circuit Proof)	5 mA		
Output Capacitive Load	300 pF	300 pF	1000 pF
Output Impedance @ DC	0.1 ohm		
Output Noise	<1 mV RMS, 10 Hz to 300 kHz		
Internal Reference Output	+10V (±1%) @ 4 mA ±0.1% (No Load - Full Load)		
ENVIRONMENTAL			
Operating Temp.	0 to 70°C		
Storage Temp.	−25 to 85°C		
Relative Humidity	90% Non-Condensing		
POWER REQUIREMENTS	+5V(±5%) 50 ma ±15V @ 25 mA	+5V (±5%) 50 mA ±15V @ 25 mA	+5V (±5%) 50 mA ±15V @ 25 mA −15V @ 10 mA
Derated Performance	±11.5V to ±18V	±11.5V to ±18V	±11.5V to ±18V
PRICE (1-24)	$29	$39	$55

Prices and specifications subject to change without notice.

① Adjust to zero error with external trim potentiometer.

② FSR is defined as 10V for ±5V operation, 10V for 0 to +10V operation and 20V for ±10V operation.

MODELS 440, 441, 442–BLOCK DIAGRAM



OPERATION

Several external connections must be made for proper operation of each digital-to analog converter. Internal or external reference, and full scale voltage ranges are selected by jumpering pins as shown in Table 1.

Table 1. External Connections for DAC Operation

DESIRED OPERATION	CONNECTIONS
Internal Reference	Pin 22 to Pin 23
External Reference +10V (±10%), 1.5 mA	Connect to Pin 22
±10V FSR	Pin 21 to Pin 22
±5V FSR	Pin 20 to Pin 30 Pin 19 to Pin 22
0V to +10V FSR	Pin 20 to Pin 30

INTERNAL REFERENCE

The internal reference of each D/A converter can be used to drive two additional units. To use, connect pin 23 of first unit to pin 22 of each additional converter.

GROUNDING

Analog and Digital grounds on the ZD442 must be tied together somewhere within the system. On ZD440 and ZD441, the grounds are internally jumpered together.

OPTIONAL ADJUSTMENT

Each converter is ready to operate within given specifications without external adjustments. However, special full scale settings or fine adjustment of offset voltage can be made using the circuit shown below. The circuit provides a full scale adjustment range of ±10%, and an offset adjustment range of ±40 mV.

NOTE: When using external reference, adjust the full scale range by varying the external reference voltage.

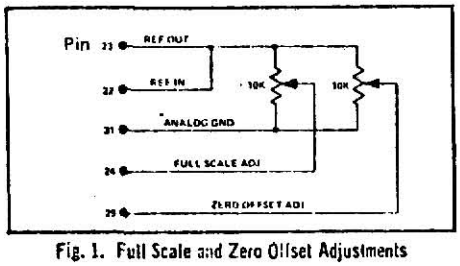


Fig. 1. Full Scale and Zero Offset Adjustments

INPUT CODING

Table 2. Offset Binary

ANALOG OUTPUT (BIPOLAR)	INPUT CODE MSB							LSB
	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-n}
F.S. – 1 LSB	1	1	1	1	1	1	1	1
+½ F.S.	1	1	0	0	0	0	0	0
0V + 1 LSB	1	0	0	0	0	0	0	1
0 Volts	1	0	0	0	0	0	0	0
0V – 1 LSB	0	1	1	1	1	1	1	1
–½ F.S.	0	1	0	0	0	0	0	0
–F.S. + 1 LSB	0	0	0	0	0	0	0	1
–F.S.	0	0	0	0	0	0	0	0

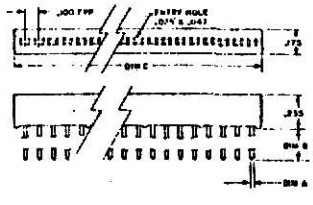
Table 3. Straight Binary

ANALOG OUTPUT (UNIPOLAR)	INPUT CODE MSB							LSB
	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-n}
F.S. – 1 LSB	1	1	1	1	1	1	1	1
+¾ F.S.	1	1	0	0	0	0	0	0
+½ F.S.	1	0	0	0	0	0	0	0
+¼ F.S.	0	1	0	0	0	0	0	0
0V + 1 LSB	0	0	0	0	0	0	0	1
0 Volts	0	0	0	0	0	0	0	0

Table 4. Binary Weights

MSB	2^{-1}	.5
2	2^{-2}	.25
3	2^{-3}	.125
4	2^{-4}	.0625
5	2^{-5}	.03125
6	2^{-6}	.015625
7	2^{-7}	.0078125
8	2^{-8}	.00390625
9	2^{-9}	.001953125
10	2^{-10}	.0009765625
11	2^{-11}	.00048828125
LSB	2^{-12}	.00024414062

MATING CONNECTOR DATA



PART NO. & TYPE	DIM A	DIM B	DIM C	SIZE	NO. REQ'D	UNIT PRICE
MC30 Axial Wire	0.115	0.715	1.250	31 PIN	2	$1.25
MC31 Solder Pin	0.05 x 0.25	0.160	1.250	31 PIN	2	$1.00

APPENDIX C

PARTS SUPPLIERS

Supplier	Parts bought
Amp Special Industries P. O. Box 844 Paoli PA 19301	binding posts, pin connectors
Analogic Audubon Road Wakefield MA 01880	A/D converter
manufacturer's sales outlet:	W. G. (Bill) Reinschmidt EIR Company Suite 205, 6405 Metcalf Shawnee Mission KS 66202
Burstein - Applebee 3199 Mercier Kansas City MO 64111	Vector perfboard, capacitors, miscellaneous
Cherry Electrical Products Corp. 3600 Sunset Avenue Waukegan IL 60085	lever switches
Dialight Corporation 60 Stewart Avenue Brooklyn NY 11237	light emitting diodes
Electrostatics, Inc. 7718 Clairemont Mesa Blvd. San Diego CA 92111	power supplies
Newark Electronics 500 North Pulaski Road Chicago IL 60624	potentiometers, IC's, Amphenol connectors, fuses, handles, miscellaneous
Olive Industrial Electronics 6662 Olive Boulevard St. Louis MO 63130	Scamby IC sockets, connectors, switches, wire, miscellaneous
Radio Shack 2609 Anderson Manhattan KS 66502	knobs, capacitors, diodes, toggle switches, screws, miscellaneous

PARTS SUPPLIERS (Continued)

Radio Supply Company P. O. Box 1220 115 Laura Wichita KS 67201	Zener diodes, miscellaneous
RGS Electronics 3650 Charles St., Suite K Santa Clara CA 95050	IC's
Stevenson Sign Service, Inc. 127 McCall Road Manhattan KS 66502	aluminum, plexiglass
Walter's Radio Supply, Inc. 3627-35 Main Street Kansas City MO 64111	relays, miscellaneous
Zeltex, Inc. 940 Detroit Avenue Concord CA 94518	D/A converter

manufacturer's sales outlet: Ron Harper
Technical Representatives, Inc.
Rt. 1, Box 301
Peculiar MO 64078

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In conclusion, thanks are due to the many electrical engineering faculty members not already mentioned, who were at one time or another consulted for their ideas and assistance.

THE DESIGN AND IMPLEMENTATION OF AN INTERFACE BETWEEN THE NOVA 1200 AND THREE PERIPHERALS: AN ANALOG-TO-DIGITAL CONVERTER, A DIGITAL-TO-ANALOG CONVERTER, AND AN INCREMENTAL TAPE TRANSPORT

by

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B.A., Lehigh University, 1970
B.S., University of Texas, 1973

AN ABSTRACT OF A MASTER'S THESIS

submitted in partial fulfillment of the

requirements for the degree

MASTER OF SCIENCE

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1974

ABSTRACT

This report concerns the design and implementation of a basic digital data acquisition system. The system is capable of digitizing a variety of analog signals, and involves the Nova 1200 computer in the Electrical Engineering Department of Kansas State University. The report is also intended to serve as a manual for operating this system.

Included are operating instructions for the analog-to-digital and digital-to-analog capabilities, along with an incremental digital tape recording capability, all three of which were interfaced to the Nova. A special chapter which deals with the general interfacing concepts pertaining to the Nova is also included.

In conclusion, several interesting applications of the above data acquisition facility are suggested along with ideas for extending the interfacing capabilities of the same.