A VERSATILE TIMING MARKER GENERATOR FOR A REAL-TIME ANALOG COMPUTER

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INTRODUCTION

When a general-purpose electronic analog computer is used to solve physical problems, voltage represent the problem's dependent variables. For the majority of cases the independent variable is time, and the purpose of a study is to determine how the physical quantities change with time. When a physical problem is thus simulated on an analog computer the solutions can be directly plotted on an X-Y recorder. Whenever the X-Y recorder plots the response curve on a graph sheet a prime consideration is calibration of the time axis.

In this paper a versatile timing marker generator is under discussion. There are many different ways leading to the construction of a timing circuit. The use of vacuum tubes through linear and non-linear wave shaping is not discussed here. We examine rather, a hybrid timing circuit employing two junction transistors and one unijunction transistor with the junction transistors forming a conventional flip-flop and the unijunction transistor serving as an oscillator and trigger. The special features of such a timing circuit are its excellent timing stability and a configuration not prone to "lock-up." Here "lock-up" implies a state mode of operation wherein oscillations do not occur.

The basic concept of oscillation in a unijunction transistor relaxation oscillator is due to its negative-resistance characteristic over a wide range of operation. Chapter one thus emphasizes the analysis of the principles of negative-resistance oscillation. In the later chapters we give a general introduction to unijunction transistors as well as the circuit design of a bistable multivibrator. In the fifth chapter we combine these two circuits

together to form a hybrid timing circuit. Finally, the solution of an ordinary second-order linear differential equation is illustrated by means of analog simulation and the timing marker is introduced on the time axis of X-Y recorder to provide our real-time computation.

RELAXATION OSCILLATORS

A relaxation oscillator is a nonlinear device generating nonsinusoidal waveforms. Multivibrators, blocking oscillators, pulse generators, saw-tooth generators and other special generators are classified as relaxation oscillators.

Classifications

Generally speaking, relaxation oscillators may be classified into three types:

(1) Gas tube relaxation oscillators (soft tube oscillators):
   A. Neon tube relaxation oscillator.
   B. Thyratron relaxation oscillator.

(2) Vacuum tube relaxation oscillators (hard tube oscillators):
   A. Multivibrator.
   B. Blocking oscillator.
   C. R-C coupled relaxation oscillator.
   D. Dynatron (negative-resistance) relaxation oscillator.

(3) Transistor relaxation oscillators:
   A. Junction transistor relaxation oscillator.

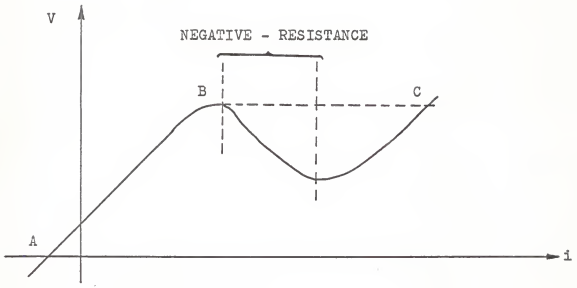
B. Unijunction transistor relaxation oscillator.

C. Tunnel diode relaxation oscillator.

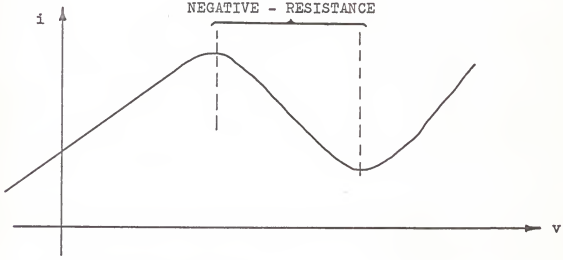
In this paper we are interested in the transistor circuits and a study of the negative-resistance oscillator will be considered in this chapter. From this point of view a better understanding of the operation of a unijunction transistor will be obtained.

Negative-Resistance Relaxation Oscillator

Two possible types of negative-resistance characteristic are shown in Fig. 2-1, one called current controlled in which the voltage is a unique function of the current but the current is multivalued function of the voltage; and the other called voltage controlled where the reverse is true. In the negative-resistance region the slope $\frac{\partial v}{\partial i}$ and $\frac{\partial i}{\partial v}$ respectively is negative. It is apparent from Fig. 2-1 that under certain conditions a negative-resistance device will act like a switch, i.e., change suddenly from a high to a low resistance, or vice versa. Let us assume that the applied voltage v is raised from point A towards B. At B the total d-c resistance of the device v/i is relatively high. As v is raised further, the current in the device suddenly jumps to point C, where the d-c resistance, v/i, is considerably smaller. Other such transitions are possible wherever the slope of the curves change sign.



(a) Current-controlled



(b) Voltage-controlled

Fig. 2-1. Negative-resistance characteristics.

The operation of most negative-resistance relaxation oscillators may be visualized by some modification of the model shown in Fig. 2-2. Energy is delivered at a certain rate characterized by a time t_1 from a power supply to a storage element which in simple cases may be a capacitance or inductance. The negative-resistance element may then be regarded as a switch which is activated by the amount of energy stored in the storage element (e.g. voltage across capacitor, current through inductor). As the switch closes, the stored energy is discharged into the load at a rate which is characterized by another time t_2. The total cycle of the relaxation oscillator is then given by the sum of the charge, storage, discharge and recovery times.

Let us consider the specific example of a current-controlled negative-resistance device with a characteristic as shown in Fig. 2-3 (a). If the capacitance C were absent from the circuit, the d-c operating point would adjust itself at point A in Fig. 2-3 (b), which is simply the operating point of intersection of the negative-resistance characteristic of the device and the $i_R = (v - V_o)/ R$ line of the resistance R. If the negative-resistance

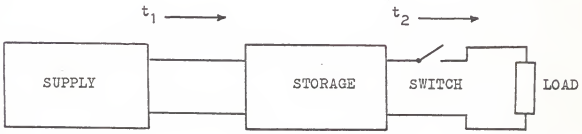
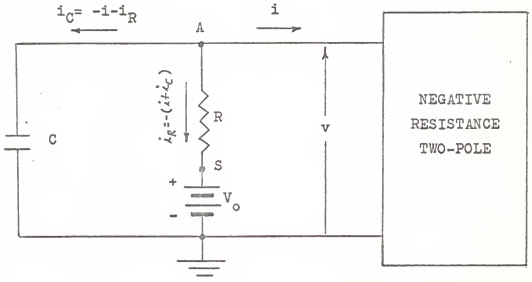


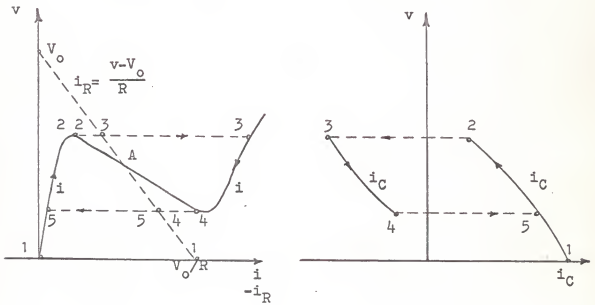
Fig. 2-2. Model for operation of negative-resistance relaxation oscillator.

device were absent from the circuit, the capacitance C would begin to charge to the full value of the d-c supply voltage V_o as soon as a switch at point S in the circuit is closed. The charging time constant would obviously be RC.

Now consider the entire circuit and assume that a switch at point S is open. We have $i = i_C = i_R = 0$ and $v = 0$. In the first moment after the switch is closed the system will be at point (1) in the plot of characteristics, Fig. 2-3 (b), i.e., the current through the resistor R is equal to $i_R = - V_o / R$ the largest part of which exists as charging current $i_C = -i - i_R$ into the capacitor C. As the capacitor C is being charged, the voltage across it, v, increases and the current through R decreases, as does the charging current itself. This continues until point (2) on the curve is reached. When the negative-resistance device presents a high resistance to the rest of the circuit in this region, the time constant for the system to go from point (1) to point (2) is given by RC. As the voltage v tries to increase further the negative-resistance two-pole goes from point (2) to point (3), i.e., suddenly changes from a high to a low resistance. For this to occur it is obvious that the i_R line must not intersect the device characteristic at any point between (1) and (2), since this would imply a fixed operating point. With the negative-resistance device at point (3) now presenting a low resistance, the voltage v across the capacitor is considerably higher than would correspond to the steady-state potential of point A if the capacitor were not present. It therefore begins to decrease, the capacitor discharges, which also manifests itself in the negative value of the charging current in the characteristics. The current i_R in R is still positive at point (3), but the current i, in the negative-resistance device for a voltage v across it, is so much higher that the charging current of the



(a)



(b)

Fig. 2-3. (a) Relaxation oscillator circuit utlizing negative-resistance two-pole.
(b) Negative-resistance characteristics of two-pole.

capacitor has to change sign to satisfy the node equation at point A. The capacitor thus discharges and the voltage v across the negative-resistance device decreases. This process will evidently continue as long as for a given voltage v the current in R is smaller than, but of the same sign, as the current in the device.

As point (4) is reached, the current through the device again becomes a single-valued function of the voltage. As the voltage tries to decrease further, the device jumps from point (4) to (5), i.e., changes suddenly from a low resistance to a high resistance. Under these conditions, however, the voltage v across the capacitor is smaller than would correspond to the steady-state potential of point A if the capacitor were not present. The capacitor therefore is being charged, the voltage across it increases, and the cycle starts again. For the system to reach point (4) it is important that the i_R line in the plot of characteristics should not intersect the i curve anywhere in the positive-resistance region between point (3) and (4). This consideration, together with earlier remarks, leads to the following condition for the values of R and V_o. For a negative-resistance relaxation oscillator to be free-running, the i_R line in the plot of characteristics must intersect the negative-resistance region. Otherwise the system has a stable condition in which it will lock itself.

UNIJUNCTION TRANSISTOR CIRCUITS

Introduction

A unijunction transistor sometimes may also be called a double-base diode which lends itself to calculation on a negative-resistance basis. It is a three-terminal semiconductor device which has electrical characteristics quite different from those of a conventional two-junction transistor. It exhibits a stable N-type negative-resistance characteristic between its emitter and base-one terminals when a positive bias is applied between its base-one and base-two terminals.

Most of the more important applications of the unijunction transistor make use of one or more of its four unique electrical characteristics:

(1) A stable firing voltage (V_p) which is a fixed fraction of the applied interbase voltage.

(2) A very low value of firing current (I_p).

(3) A negative-resistance characteristic which is uniform from unit to unit and stable with temperature and life.

(4) A high pulse current capability.

These important features make the unijunction transistor advantageous in oscillators, timing circuits, trigger circuits and bistable circuits where it can often perform the function of two conventional transistors.

Basic Theory of Operation

A cross-sectional diagram of the unijunction transistor is shown in

Fig. 3-1. Two ohmic contracts, called base-one (B_1) and base-two (B_2) are made at opposite ends of a small bar of N-type silicon material. A single rectifying contact, called the emitter (E), is made on the opposite side of the bar close to B_2. An interbase resistance, R_{BB}, of between 5 and 10 kilohms exists between B_1 and B_2. In normal circuit operation, B_1 is grounded and a positive bias voltage, V_{BB}, is applied at B_2. With no emitter current existing the silicon bar acts like a simple voltage divider (Fig. 3-2) and a certain fraction η of V_{BB} will appear at the emitter. The fraction η is termed the intrinsic stand-off ratio and is determined by the spacing between the emitter junction and the two base contacts.

If the applied emitter voltage, V_E, is less than ηV_{BB} the emitter junction will be reverse biased and only a small reverse leakage current I_{eo} will exist in the emitter circuit. If the applied emitter voltage exceeds ηV_{BB} by an amount equal to the forward voltage drop of the emitter diode, V_D, holes will be injected into the silicon bar. Because of the electric field within the silicon bar these holes will move towards B_1 and increase the conductivity of the bar in the region between emitter and base-one. This is obvious, since

$$\sigma = (u_p p + u_n n) \qquad (3\text{-}1)$$

where σ = conductivity in $(\text{ohm-cm})^{-1}$, or mho/cm

u_p, u_n = mobility for P and N type of charge carriers respectively.

p, n = hole and electron density respectively

In our case the silicon bar is doped N-type and the holes are the minority carriers, so the first term on the right of Eq. (3-1) may be neglected in the

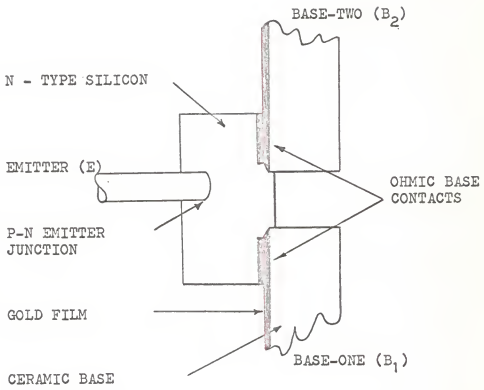


Fig. 3-1. Construction of unijunction transistor.

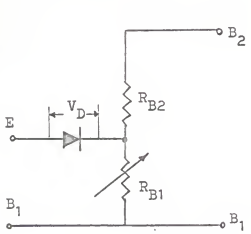


Fig. 3-2. Unijunction transistor representative circuit.

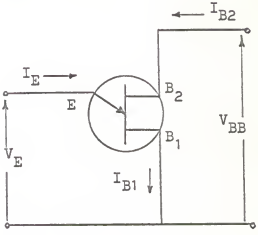


Fig. 3-3. Symbol for unijunction transistor.

absence of any injected carriers from the emitter. However, since the emitter junction is biased in the forward direction and holes are injected into the bar, there will be a region within the bar in which the conductivity will be greatly increased. This increase in conductivity will be due to the increase of the hole concentration, p, in the region where the injected holes appear, and to the corresponding increase in electron concentration, n, which occurs to maintain space charge neutrality.

As the emitter current I_E is increased the emitter voltage will decrease because of the increased conductivity so that a negative-resistance characteristic is observed between the emitter and the base-one terminals.

The essential features of the emitter characteristic curve are shown in Fig. 3-4. The two important points on the curve are the peak point and the valley point. At these two points the slope of the characteristic curve is zero. The region to the left of the peak point is called the cutoff region, where the emitter diode is reverse biased. The region between the peak and the valley points is called the negative-resistance region, here the conductivity modulation of the silicon bar between emitter and base-one is important. The region to the right of the valley point is called the saturation region. In the saturation region conduction between emitter and base-one is limited by the surface and bulk recombination of the holes and electrons.

Unijunction Transistor Relaxation Oscillator

The relaxation oscillator circuit employing a unijunction transistor is shown in Fig. 3-5. It is chiefly useful in timing circuits, pulse generators,

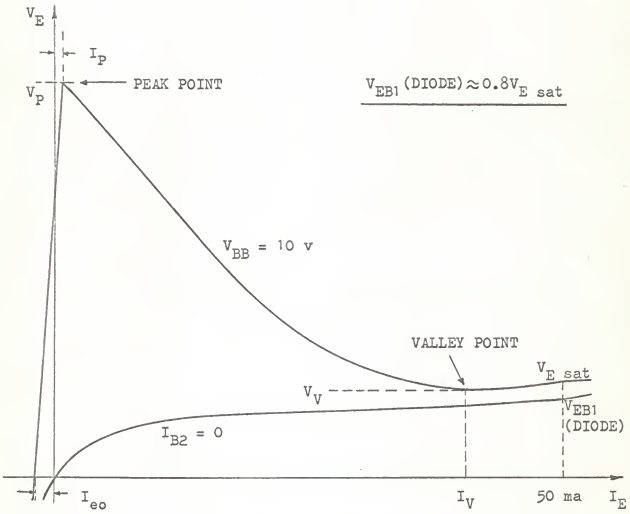


Fig. 3-4. Static emitter characteristic curve showing important parameters.

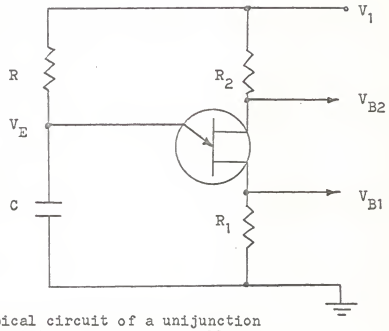


Fig. 3-5. Typical circuit of a unijunction transistor relaxation oscillator.

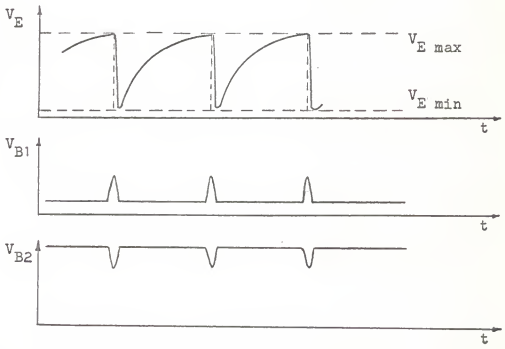


Fig. 3-6. Bases and emitter voltages.

trigger circuits or saw-tooth wave generators. At the beginning of an operating cycle the emitter is reverse-biased and hence non-conducting. As the capacitor C is charged through the resistor R the emitter voltage rises exponentially towards the supply voltage V_1. When the emitter voltage reaches the peak point voltage V_p the emitter becomes forward biased and the dynamic resistance between the emitter and base-one drops to a low value. The capacitor C then discharges through the emitter. When the emitter voltage reaches a value of about 2 volts the emitter ceases to conduct and the cycle is repeated. The period of oscillation T is given by

$$T = RC \ln. \frac{V_1 - V_{E\ min}}{V_1 - \eta V_{BB} - V_D} + 2t_f \qquad (3\text{-}2)$$

where t_f is the emitter voltage fall time, $t_f \cong (2 \div 5C) V_{E\ sat}$ in microseconds. $V_{E\ min}$ is the minimum emitter voltage and is relatively independent of bias voltage, temperature and capacitance if R_1 is zero. $V_{E\ min}$ is approximately equal to 0.5 $V_{E\ sat}$ and lies between 1.2 and 2.4 volts for most units.

In order to facilitate the verification of this formula, let us first remove both R_1 and R_2 from the circuit with the capacitor C initially uncharged. After switch SW is closed, the emitter will be reverse-biased to ηV_1 and the voltage across the capacitor will increase exponentially according to the equation:

$$V_C = V_1 (1 - e^{-t/RC}) = V_E \qquad (3\text{-}3)$$

This curve is shown as a dashed line in Fig. 3-8. The charging of the capacitor will continue only until the voltage across the capacitor reached

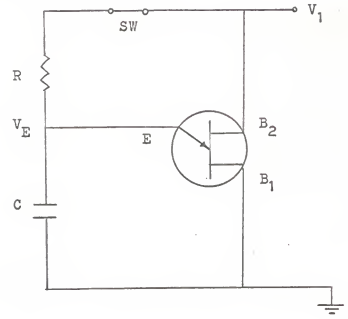


Fig. 3-7. A unijunction transistor relaxation oscillator.

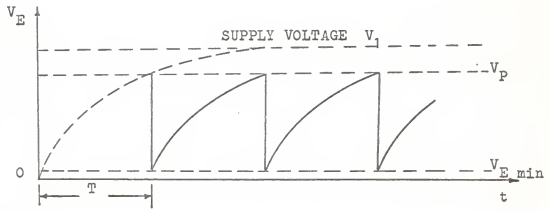


Fig. 3-8. The emitter waveform of a unijunction transistor relaxation oscillator.

ηV_1+V_D (i.e., V_p). At this time the emitter becomes forward biased and charge will leak off the capacitor very rapidly through the emitter-to-base-one junction. When the emitter voltage reaches the valley point value V_V the emitter ceases to conduct and the capacitor will again begin to charge through the local R-C circuit. Thus the entire process will repeat itself.

Now assume t is the time measured from the instant when the capacitor starts to charge then the capacitor voltage is given by:

$$V_E - V_{E\,min} = (V_1 - V_{E\,min})(1 - e^{-t/RC}) \qquad (3\text{-}4)$$

$$V_E = (V_1 - V_{E\,min})(1 - e^{-t/RC}) + V_{E\,min} \qquad (3\text{-}5)$$

This equation is consistent with the following facts. At t=0, V_E must equal the minimum emitter voltage $V_{E\,min}$. At t=T, V_E must equal the supply voltage V_1. The time constant is T=RC. Now from Eq. (3-5), put $V_E=V_p$ at t=T . Then

$$V_p - V_{E\,min} = (V_1 - V_{E\,min})(1 - e^{-T/RC}) \qquad (3\text{-}6)$$

$$\frac{V_p - V_{E\,min}}{V_1 - V_{E\,min}} = 1 - e^{-T/RC} \qquad (3\text{-}7)$$

$$\frac{V_p - V_{E\,min} - V_1 + V_{E\,min}}{V_1 - V_{E\,min}} = - e^{-T/RC} \qquad (3\text{-}8)$$

$$\frac{V_1 - V_p}{V_1 - V_{E\,min}} = e^{-T/RC} \qquad (3\text{-}9)$$

$$\ln. \frac{V_1 - V_P}{V_1 - V_{E\ min}} = - T/RC \qquad (3\text{-}10)$$

$$T = RC \ln. \frac{V_1 - V_{E\ min}}{V_1 - V_P}$$

$$= RC \ln. \frac{V_1 - V_{E\ min}}{V_1 - \gamma V_{BB} - V_D} \qquad (3\text{-}11)$$

Eq. (3-11) is identical to Eq. (3-2) provided the emitter fall time t_f is not included. The natural frequency of oscillation of the relaxation oscillator is

$$f = \frac{1}{T} = \frac{1}{RC \ln. \frac{V_1 - V_{E\ min}}{V_1 - \gamma V_{BB} - V_D}} \qquad (3\text{-}12)$$

Since

$$\frac{V_1 - V_{E\ min}}{V_1 - \gamma V_{BB} - V_D} = \frac{V_1(1 - V_{E\ min}/V_1)}{V_1(1 - \gamma V_{BB}/V_1 - V_D/V_1)}$$

$$= (1 - V_{E\ min}/V_1) \cdot \frac{1}{1 - \frac{\gamma V_{BB} + V_D}{V_1}}$$

$$= \frac{1 - V_{E\ min}/V_1}{1 - \gamma \frac{V_{BB} + V_D/\gamma}{V_1}} \qquad (3\text{-}13)$$

And

$$V_{E\ min} = 1.2 \quad 2.4 \text{ volts}$$

$$V_D = 0.7 \text{ volt}$$

$$\eta = 0.51 \quad 0.75$$

with lower R_1 and R_2 in series with base-one and base-two, the voltage drops across R_1 and R_2 are very small (since R_{BB} is nominally 4.7 up to 9.1 kilohms while R_1 and R_2 are generally below 150 and 470 ohms respectively).

By making the following approximations

$$\frac{V_{E\ min}}{V_1} \ll 1 \qquad (3\text{-}14)$$

$$\frac{V_{BB} + V_D/\eta}{V_1} \cong 1 \qquad (3\text{-}15)$$

Eq. (3-13) can be reduced to

$$\frac{V_1 - V_{E\ min}}{V_1 - \eta V_{BB} - V_D} \cong \frac{1}{1 - \eta} \qquad (3\text{-}16)$$

Hence Eq. (3-12) becomes

$$f = \frac{1}{T} \cong \frac{1}{RC \ln. \frac{1}{1 - \eta}} \qquad (3\text{-}17)$$

$$T \cong RC \ln. \frac{1}{1 - \eta} \qquad (3\text{-}18)$$

The typical value of η of various unijunction transistors range from 0.51 to 0.75. By properly choosing of it is expected to have $1/(1 - \eta) = 2.7183$, i.e., $\eta = 0.632$

Then

$$f \cong \frac{1}{RC} \qquad (3\text{-}19)$$

$$T \cong RC \qquad (3\text{-}20)$$

Oscillation Requirements

The unijunction transistor relaxation oscillator is noteworthy for its ability to operate over a wide range of circuit parameters and ambient temperature. However, there are several important conditions which must be satisfied if this circuit is to operate satisfactorily.

(1) The load line formed by the resistor R and the supply voltage V_1 must intersect the emitter characteristic curve to the right of the peak point. This condition ensures that the resistor R can supply sufficient current to the emitter to "fire" the transistor. This condition may be written

$$\frac{V_1 - V_P}{R} > I_P \qquad (3\text{-}21)$$

(2) The second condition which must be satisfied is that the load line formed by R and supply voltage V_1 must intersect the emitter characteristic to the left of the valley point, i.e.,

$$\frac{V_1 - V_V}{R} < I_V \qquad (3\text{-}22)$$

If this condition is not satisfied the load line will intersect the emitter characteristic curve in the saturation region and the transistor will not turn off after it fires on the first cycle.

(3) A final condition for the operation of the unijunction transistor relaxation oscillator concerns the allowable range of capacitance C. As C is increased the recovery time of the emitter voltage waveform increases. As the size of C is decreased below about 0.01 uf the amplitude of the emitter voltage waveform will decrease. This decreases the frequency stability of the circuit and also reduces the allowable range of R.

Design of Unijunction Transistor Oscillator

In this section we want to choose a proper set of R-C combinations to make the relaxation oscillator capable of generating pulses at specified frequencies which in turn will be transmitted to our bistable multivibrator as the triggering pulses. First let us refer to the static emitter characteristics of the 2N489A unijunction transistor shown in Fig. 3-9. The peak point voltage, V_p, and the valley point voltage, V_V, are found to be about 16 volts and 4 volts, respectively. The corresponding peak point

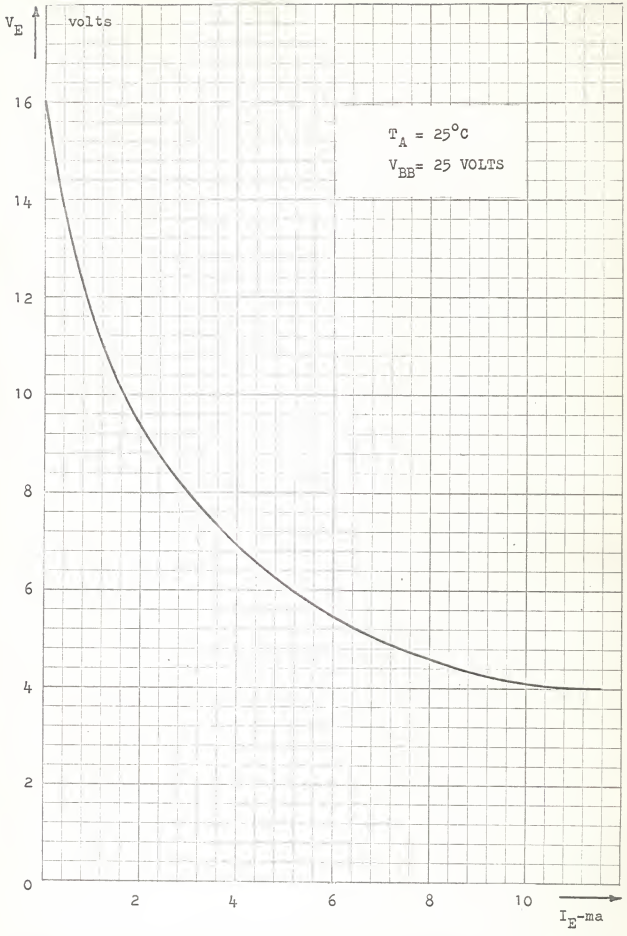


Fig. 3-9. Static emitter characteristics (2N489A).

emitter current, I_p, and the valley point emitter current, I_v, are around 10 microamperes and 10 miliamperes respectively. Thus in order to satisfy Eq. (3-20) and Eq.(3-21), a typical maximum value of I_p and a typical minimum value of I_v might be considered to be approximately 10 ua and 10 ma respectively. The allowable range of R would approach 1000 to 1. For a proper circuit design with the reasonable choice of supply voltage and suitable resistance in series with base-two for the temperature compensation purpose, the range of R might be from about 2 kilohms up to 2 megohms.

In order to fulfill the last condition for the operation of a unijunction transistor relaxation oscillator, the value of capacitance C will be limited to a value not below 0.01 uf. The upper range of C will be, to a certain extent, self-limited due to the large volume and higher cost.

Following shows a table with the entries of all different combinations of resistance and capacitance to obtain the required time markers. The corresponding frequencies and the periods are also listed in two separate columns:

R (ohms)	C (uf)	f (cps)	T (sec)
610 K	2	1	1
610 K	1	2	0.5
610 K	0.2	10	0.1
610 K	0.1	20	0.05
610 K	0.02	100	0.01
610 K	0.01	200	5 ms
122 K	0.01	1 K	1 ms
61 K	0.01	2 K	0.5 ms

The above resistance and capacitance are obtained on the basis of the following relation with the intrinsic stand-off ratio given as 0.56 and the frequency varying from 1 cps to 2 KC.

$$f = \frac{1}{RC \ln. \frac{1}{1-\eta}} = \frac{1.22}{RC} \qquad (3\text{-}23)$$

The errors arising in the calculation of R and C from the above formula will be considered tolerable. In the actual circuits all R's and C's will be individually adjusted such that the desired frequencies may be obtained. This can be done through the calibration on an oscilloscope.

Temperature Compensation

The peak point voltage V_p of the unijunction transistor determines the triggering voltage in the multivibrator and the frequency of the relaxation

oscillator. From the equivalent circuit of the unijunction transistor shown in Fig. 3-2

$$V_P = \eta V_{BB} + V_D \qquad (3\text{-}24)$$

The principal variation of V_p with temperature is due to the variation of V_D with temperature. This effect may be compensated for by means of a small resistor, R_2, in series with base-two as already shown in Fig. 3-5. As the ambient temperature increases the interbase resistance R_{BB} will increase and V_{BB} will also increase due to the voltage divider action of R_2, R_{BB} and R_1. If R_2 is chosen correctly the increase in interbase voltage will compensate for the decrease in V_D. The approximate value of R_2 is

$$R_2 \cong \frac{0.70\ R_{BB}}{\eta V_1} + \frac{(1 - \eta)\ R_1}{\eta} \qquad (3\text{-}25)$$

If R_2 satisfies this equation the peak point voltage will be given by

$$V_P \cong \eta V_1 \qquad (3\text{-}26)$$

Here η is a constant, relatively independent of interbase voltage V_{BB} and ambient temperature.

With a typical value of R_{BB} = 5.6 kilohms and η = 0.56 for the unijunction transistor 2N489A, Eq. (3-25) gives

$$R_2 = 398 \text{ ohms}$$

A resistor of 400 ohms will serve properly.

BISTABLE MULTIVIBRATOR

A bistable multivibrator is a circuit that has two stable states. It remains in one of these states until forced by an external trigger to change its state.

The circuit is normally designed so that during the switching interval it has regenerative loop gain. This means that the external trigger need only initiate the switching action; the circuit will carry the action through to completion. There are many methods for the design of a bistable multivibrator depending upon whether or not it is to be used in fast switching. The only reason for not saturating the on transistor is to avoid storage-time delay during switching of the bistable. In this paper the timing marker generator operated at a frequency range from 1 cps to 2 KC, in which case the storage-time delay is of minor importance in the transition from one state to the other. Thus only a saturated version of a bistable multivibrator will be discussed here.

Circuit Design

Consider the circuit shown in Fig. 4-1. The output voltage will swing approximately between V_1 and $V_1 R_E/(R_E+R_C)$. The back bias on the OFF transistor will be approximately

$$V_{EB} = \frac{R_1}{R_1 + R_2} \cdot \frac{R_E V_1}{R_E + R_C} \qquad (4\text{-}1)$$

Many of the diffused base germanium units and most silicon units have low

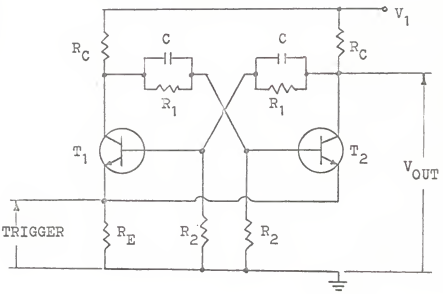


Fig. 4-1. Bistable multivibrator.

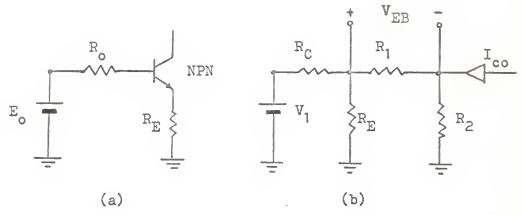


Fig. 4-2. (a) ON transistor (b) OFF transistor.

emitter-base back bias breakdown voltage (1 to 2 volts). Therefore either the back bias must be limited or the parallel combination of R_1 and R_2 must be large enough so that the current existing in the broken-down junction is limited to a safe value.

In addition to these considerations, the resistors must be chosen so that the transistor with the lowest β is saturated at the lowest possible temperature, and the transistor with the highest I_{co} is off at the highest possible temperature. These points are illustrated in Fig. 4-2. In part (a) we have made an equivalent circuit assuming that one transistor is completely off and the other is on. To insure saturation

$$E_o - I_B R_o = V_1 - I_C R_C \qquad (4\text{-}2)$$

$$I_C = \beta I_B \qquad (4\text{-}3)$$

where

$$R_o = (R_1 + R_C) \,//\, R_2 \qquad (4\text{-}4)$$

$$E_o = \frac{R_2 V_1}{R_1 + R_2 + R_C} \qquad (4\text{-}5)$$

When these equations are combined with the approximate I_C at the edge of saturation, the result is

$$(\beta + 1) R_E (R_1 + R_C) \leq (\beta - 1) R_C R_2 - R_1 R_2 \qquad (4\text{-}6)$$

Eq. (4-6) may be solved for any one resistor in terms of the minimum β and

the other resistors.

Note that V_1 has vanished, so that to a first approximation saturation is not a function of V_1. The equality leads to the just saturated condition.

In Fig. 4-2 (b) we determine the effect of I_{co} in turning on the normally off unit. If both junctions are back biased, then we know that if $\beta \gg 1$, $I_B \cong -I_{co}$. This is the output current of a NPN transistor; hence it tries to turn the transistor on. The minimum allowable back bias is subject to some argument since the I_C that exists for a given V_{EB} also increases with temperature.

If $V_{EB} = 0$ is taken as the limit, then

$$I_{co} R_2 \leqq R_E V_1 / (R_E + R_C) \qquad (4\text{-}7)$$

from which

$$R_2 \leqq \frac{R_E}{R_E + R_C} \cdot \frac{V_1}{I_{co}} \qquad (4\text{-}8)$$

If Eq. (4-6) is solved for R_2, we obtain

$$R_2 \geq \frac{(\quad + 1) R_E (R_1 + R_C)}{(\quad - 1) R_C - R_1} \qquad (4\text{-}9)$$

Which requires that

$$(\beta - 1) R_C > R_1 \qquad (4\text{-}10)$$

In our circuit design we choose $R_C = 2.2K$, $R_E = 135$ ohms and $R_1 = R_2 = 33$ kilohms which will satisfy both Eq. (4-9) and Eq. (4-10). There is

another feasible way to check the maximum temperature stability, the existance of sufficient base current to saturate the ON unit and to determine the transistor power dissipation.

A pair of NPN silicon audio-frequency transistors 2N334 are employed in our bistable circuit design. The maximum ratings and the electrical parameters referred to the G.E. Transistor Manual are shown in the following table:

2N334 TRANSISTOR CHARACTERISTICS

MAXIMUM RATINGS

$P_{C\ mw}(25^{o}C)$	BV_{CB}	$I_{C\ ma}$	$T_J\ ^{o}C$
150	45	25	200

ELECTRICAL PARAMETERS

MIN. $h_{fe}(\beta)$	$I_{C\ ma}$	MIN. $f_{hfb\ mc}$	MIN. $G_{e\ db}$	MAX. $I_{co\ ua}$	V_{CB}
18	1	8	13	2	30

where

P_C Average continuous collector power dissipation.

BV_{CB} DC breakdown voltage collector to base junction reverse biased, emitter open-circuited.

I_C RMS collector current

T_J Junction temperature.

$h_{fe}(\beta)$ Common emitter small-signal short-circuit forward current transfer ratio, output a-c short-circuited.

f_{hfb} Common base small-signal short-circuit forward current transfer ratio cut-off frequency.

G_e Common emitter small-signal power gain.

I_{co} DC collector current when collector junction is reverse biased and emitter is open-circuited.

V_{CB} DC collector to base voltage.

Checking Procedures

It is noted that the fastest way to design a saturating bistable multivibrator is to define the collector and emitter resistors by the current and voltage levels generally specified as load requirements. Then assume a tentative cross-coupling network. With all components specified, it is easy to calculate the on base current and the off base voltage.

Let us examine the circuit shown in Fig. 4-1. It can be analyzed as follows. Assume $V_{BE} = 0.3$ volt and $V_{CE} = 0.2$ volt when the transistor is on. Also assume that $V_{EB} = 0.2$ volt will maintain the off transistor reliably cut-off. The transistor specifications are used to validate the above assumptions.

(1) Check for the maximum temperature of stability:

$$V_E = \frac{R_E V_1}{R_C + R_E} = \frac{135}{2200 + 135}(25) = 1.446 \text{ volts}$$

$$V_{C\ on} = V_E + V_{CE\ on} = 1.446 + 0.2 = 1.646 \text{ volts}$$

Assuming no I_{co}, the base of the OFF transistor can be considered connected to a potential,

$$V'_B = V_{CE\ on} \frac{R_2}{R_1 + R_2} \quad \text{through a resistor } R'_B$$

$$R'_B = R_1 \,/\!/\, R_2 = 33K \,/\!/\, 33K = 16.5K$$

$$V'_B = 1.646 \frac{33}{33 + 33} = 0.823 \text{ volt}$$

The I_{co} of the OFF transistor will exist in R_B' reducing the base to emitter potential. If I_{co} is high enough, it can forward bias the emitter to base junction causing the OFF transistor to conduct. In our circuits, V_E = 1.446 volts and V_{EB} = 0.2 volt will maintain off conditions. Therefore, the base potential can rise from 0.823 volt (V_B') to 1.246 volts ($V_E - V_{EB}$ = 1.446 - 0.2 = 1.246 volt) without circuit malfunction. This potential is developed across R_B' by I_{co} = (1.246 - 0.823)/16.5K = 25.65 ua. A silicon transistor with I_{co} = 2 ua at 25°C (2N334) will not exceed 25.65 ua at higher ambient temperature.

(2) Check for sufficient base current to saturate the ON transistor:

$$V_{B\ on} = V_E + V_{BE\ on} = 1.446 + 0.3 = 1.746 \text{ volts}$$

The current in R_2 is,

$$I_2 = V_{B\ on} / R_2 = 1.746/33K = 0.0529 \text{ ma}$$

The current in R_C and R_1 in series is,

$$I_1 = \frac{V_1 - V_{B\ on}}{R_C + R_1} = \frac{25 - 1.746}{2.2K + 33K} = 0.6265 \text{ ma}$$

The available base current is,

$$I_B = I_1 - I_2 = 0.6265 - 0.0592 = 0.5736 \text{ ma}$$

The collector current is,

$$I_C = \frac{V_1 - V_{C\ on}}{R_C} = \frac{25 - 1.646}{2.2K} = 10.15 \text{ ma}$$

$I_C / I_B = 10.15 / 0.5736 = 17.7$

The transistor will be saturated if β at 10 ma is greater than 17.7. With the transistor 2N334, β equals 18 and the necessary restriction is met.

(3) Check transistor dissipation to determine the maximum junction temperature:

The dissipation in the ON transistor is

$$P_{on} = V_{BE\ on}\ I_B + V_{CE\ on}\ I_C$$

$$= 0.3 \times 0.5736 \times 10^{-3} + 0.2 \times 10.15 \times 10^{-3}$$

$$= 2.2218 \text{ mw}$$

The dissipation in the OFF transistor resulting from the maximum I_{co} is

$$P_{off} = V_1\ I_{co}$$

$$= 25 \times 25.65 \times 10^{-6} = 0.642 \text{ mw}$$

Generally the dissipation during the switching transient can be ignored at speeds justifying saturated circuitry. In both transistor the junction temperature is within $1^{\circ}C$ of the ambient temperature. It is interesting to note that the 2N334 transistor is a silicon high temperature transistor and can be operated at higher ambient temperature without introducing any parameter variations.

HYBRID TIMING MARKER GENERATOR

In the previous chapters we have studied the function of a junction transistor and a unijunction transistor both used as relaxation oscillators. In this chapter, a hybrid timing circuit is constructed by interconnecting those two separate circuits together. It will be seen that the unijunction transistor used in conjunction with conventional junction transistor to obtain a timing circuit is quite possible as well as very useful. The advantages of such circuits include:

(1) The output voltage at either collector of the junction transistor is very nearly an ideal rectangular waveform.

(2) The circuits are not prone to "lock-up" or non-oscillation.

(3) A single small timing capacitor C can be used.

(4) The circuits will tolerate large variations of transistor parameters as compared to conventional circuits.

(5) The timing stability is excellent.

Fig. 5-1 shows such a circuit. It is easily seen that the junction transistors form a conventional bistable multivibrator (flip-flop) with the unijunction transistor serving the timing and triggering functions. Each time the unijunction transistor fires the discharge current from the capacitor C develops a pulse across R_E which triggers the flip-flop from one state to the other.

A single fixed timing resistance R in Fig. 3-5 connecting directly to the source voltage gives a square-wave output. In the hybrid circuit, however, R has been divided into two parts, R_{T1} and R_{T2}, each of which is connected to one of the collectors of the junction circuit through a coupling

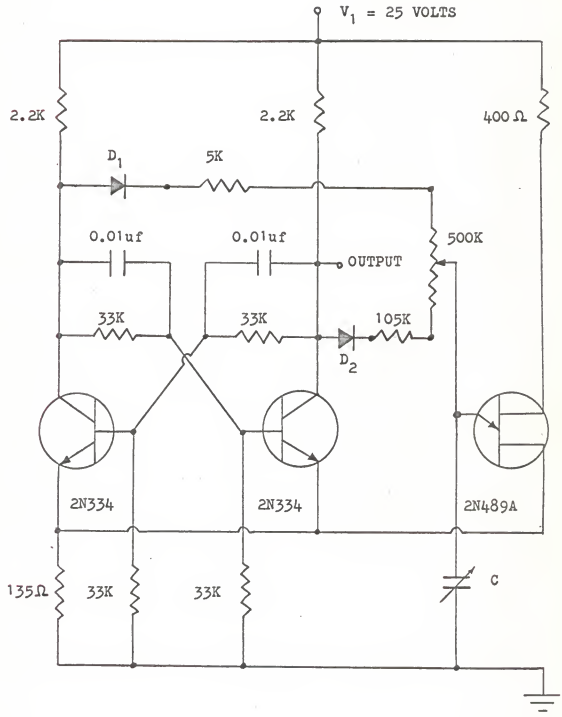
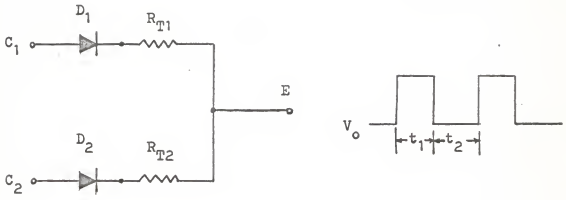
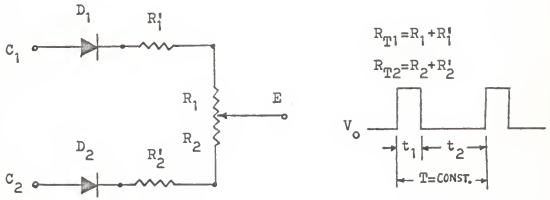


Fig. 5-1. Hybrid timing marker generator.



(a) Variable frequency



(b) Constant frequency

Fig. 5-2. Nonsymmetrical hybrid timing circuits.

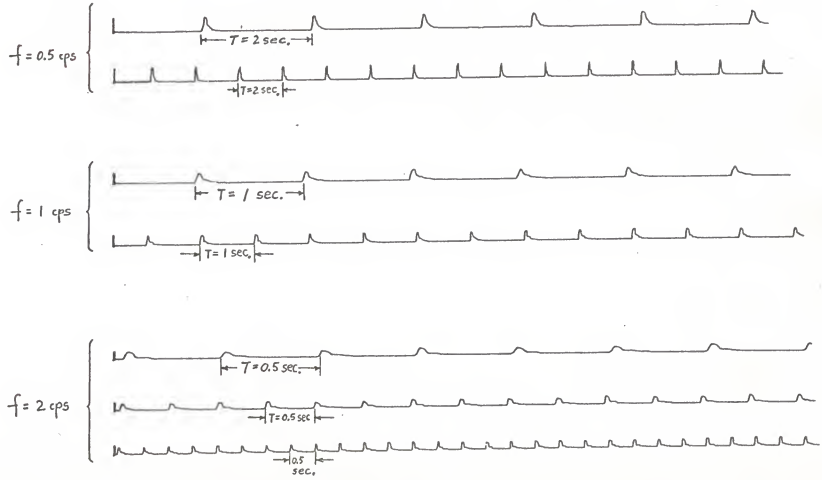


Fig. 5-4. Timing markers shown on X-Y recorder.

diode. Thus the timing capacitor C will be charged through the resistor R_{T1}, R_{T2} alternatively depending upon which collector of the junction transistor is high positive. The diodes will isolate the other resistor from the timing capacitor. The two parts of the period t_1 and t_2 can thus be set independently.

Here $$t_1 = R_{T1} C \qquad (5\text{-}1)$$

$$t_2 = R_{T2} C \qquad (5\text{-}2)$$

and $$T = t_1 + t_2 = (R_{T1} + R_{T2}) C \qquad (5\text{-}3)$$

With a timing circuit arranged as shown in Fig. 5-2 (b), it will yield a multivibrator which has a constant frequency but a variable duty cycle. This is particularly desirable in our case since a quite sharp pulse will cause significant difficulty in use on an X-Y recorder. A variable pulse duration is thus required to satisfy the frequency response limitation of the typical X-Y recorder.

APPLICATION OF TIMING MARKER ON ANALOG SIMULATION

In this chapter a second-order linear differential equation is solved through analog-computer simulation. An analog computer KEESAC-I installed at Kansas State University was used. The output response curve was plotted on an X-Y recorder with the horizontal sweep arbitrarily set to scale such that the response curve assumed its final steady-state value within tolerable

space of the graph sheet. The timing marker was hereafter added on the X-axis (time-axis) by connecting the output of the timing marker generator to the Y-input of the X-Y recorder with the horizontal sweep unchanged. The amplitude variations of the response curve were directly read from the digital voltmeter while the time scale was thus defined by the periods of the timing marker.

Consider the following differential equation:

$$\frac{d^2x(t)}{dt^2} + 2\xi w_n \frac{dx(t)}{dt} + w_n^2 x(t) = f(t) \qquad (6\text{-}1)$$

$$\ddot{x}(t) + 2\xi w_n \dot{x}(t) + w_n^2 x(t) = f(t) \qquad (6\text{-}2)$$

If $w_n = 1$, while ξ varies from 0.2, 0.4, 0.7 up to 1.0 and

$$\ddot{x}(0) = \dot{x}(0) = 0$$

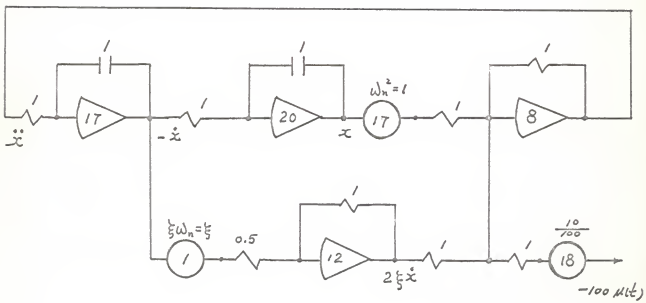
$$f(t) = 10\, u(t)$$

CONCLUSIONS

In this paper a versatile timing marker generator is presented and has been illustrated in the solution of a second-order linear differential equation through analog simulation approach. It is found in the whole procedure that this circuit is capable of operating only within some lower frequencies if an X-Y record is used to plot the time response curve.

The limitations would be due to the fact that the servo motor of an X-Y recorder is essentially a low-pass filter and the mechanical motion of the machine is limited to slowly varying functions.

If a string galvanometer type oscillograph is chosen as the plotting instrument, then the middle frequency range will be applicable. The higher operating frequencies are hence reserved for fast time computation which uses an oscilloscope as an output display device.



$$\ddot{x}(t) = 10\,u(t) - 2\xi\,\dot{x}(t) - x(t)$$

Fig. 6-1. Analog computer circuit diagram.

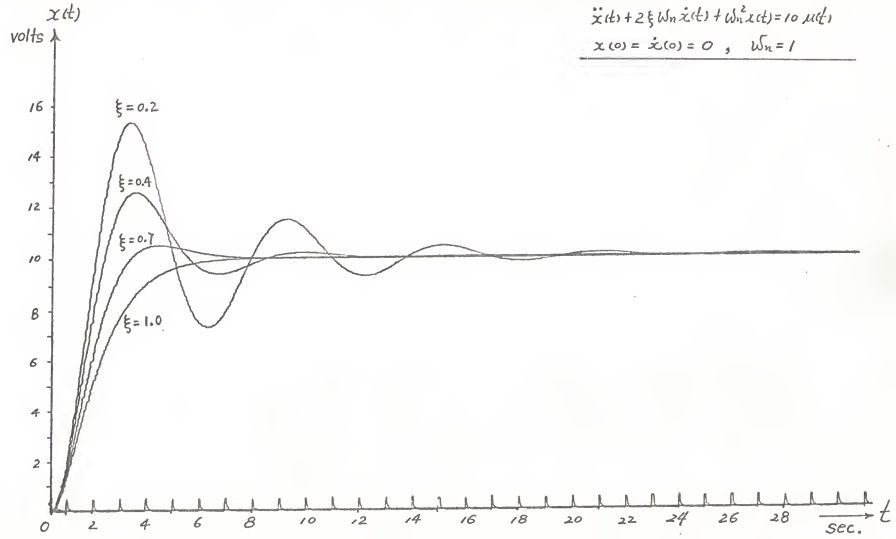


Fig. 6-2. Computer response curve.

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A VERSATILE TIMING MARKER GENERATOR FOR A REAL-TIME ANALOG COMPUTER

by

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Taipei, China

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When a physical problem is simulated on a general-purpose electronic analog computer, the solutions can be directly plotted on an X-Y recorder. Whenever the X-Y recorder plots the response curve on a graph sheet a prime consideration is how to calibrate the time axis.

In this paper a versatile timing marker generator is under study. There are many different ways leading to the construction of a timing circuit. The use of vacuum tubes through linear and non-linear wave shaping is not discussed here. We examine rather, a hybrid timing circuit employing two junction transistors and one unijunction transistor with the junction transistors forming a conventional flip-flop and the unijunction transistor serving as an oscillator and trigger.

The special features of such a timing circuit are its excellent timing stability and a configuration not prone to "lock-up." Included in this paper is a solution of a second-order linear differential equation obtained by means of analog simulation process and the timing marker is added on the time axis of the X-Y recorder to provide our real-time computation.