MICROWAVE PERFORMANCE OF THIN-FILM TECHNOLOGIES ON LTCC

by

ANDREW FUND

B.S., Kansas State University 2005

A THESIS

submitted in partial fulfillment of the requirements for the degree

MASTER OF SCIENCE

Department of Electrical Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2015

Approved by:

Major Professor
William B. Kuhn

Copyright

ANDREW D. FUND

2015

Notice: This manuscript has been authored using funds under the Honeywell Federal Manufacturing & Technologies under Contract No. DE-NA0000622 with the U.S. Department of Energy. The United States Government retains and the publisher, by accepting the article for publication, acknowledges that the United States Government retains a nonexclusive, paid-up, irrevocable, world-wide license to publish or reproduce the published form of this manuscript, or allow others to do so, for United States Government purposes.

Abstract

At RF frequencies and beyond, metallic circuit interconnects no longer behave as lumped-element wires; instead they exhibit distributed-element behavior and are classified as transmission lines. Power losses on transmission lines are of great concern to RF and microwave engineers and great care is taken to minimize power losses while still maintaining application-based robustness. The combination of low-temperature co-fire ceramics (LTCCs) and thin-film transmission line fabrication allows application-specific robustness and excellent microwave and millimeter wave performance to be achieved. LTCC technology provides a low-loss microwave substrate and allows for thin-film metal and insulator depositions to form precision transmission-line geometries and surface-applique capacitors.

In the field of thin-film metals however, concern over excess power losses at high frequencies has arisen due to the necessity of a high-resistance metallic adhesion layer which is required for the mechanical adhesion of the transmission lines to the LTCC substrate. This is especially worrisome in a microstrip configuration where the current density is concentrated at the substrate-metal interface; exactly where the high-loss metal is situated. This thesis shows that if the high-resistance adhesion layer is limited to a thickness which is a fraction of its skin depth, with more conductive metals layered above, then those excessive resistive losses can be avoided.

Issues with decreasing the total thickness of the thin-film layered metals are also investigated to achieve better interconnect line-and-space resolution, which is required for electronics operating at millimeter-wave bandwidths. Several test cases show that thinning of the metal layers has minimal impact on electrical performance. However, poor signal integrity is observed when the finished thickness of the metal stack up is reduced below 1μm. Further testing reveals that surface roughness leads to manufacturing issues when trying to produce thin-films with thicknesses in the sub-micron range.

Finally, a novel bypass and coupling capacitor topology is proposed and investigated. The capacitors are simple thin-film metal-insulator-metal constructions designed for use in a flip-chip mounting environment. Testing shows the capacitors exhibit a very low impedance through 20 GHz making them an ideal board-level bypass solution. This technology has the potential to replace all but the large bulk charge storage capacitors in electronic designs, increasing

performance and mechanical robustness, while simultaneously decreasing bill of material cost and PCB assembly times.

Table of Contents

List of Figures vii
List of Tables x
Acknowledgements xi
Dedication xii
Chapter 1 - Background and Introduction 1
1.1 Brief History of Microwave and Millimeter Wave Substrates 1
1.2 Summary of Substrates and Properties 5
1.3 LTCC and Metallization Patterning Techniques 7
1.3.1 Thick-film Patterning 7
1.3.2 Thin-film Patterning 8
1.4 Thesis Organization and Contributions 8
Chapter 2 - Thin-film Transmission Lines on LTCC 10
2.1 Adhesion Layer Losses in a Thin-film Microstrip Transmission Line 10
2.1.1 Estimation of Adhesion Layer Losses 12
2.1.1.1 Simulation of Losses 12
2.1.1.2 Analytic Modeling of Stacked-Metal Losses 14
2.1.2 Experimental Setup 20
2.1.3 Measurement Results 22
2.2 Losses Due to Thinning of Cu-layer 24
2.2.1 Estimation of Losses 25
2.2.1.1 Simulation of Losses 25
2.2.1.2 Analytic Modeling of Thinning Cu-layer Losses 26
2.2.2 Measured Results 27
2.2.3 Ultra-thin-film Investigation 28
2.2.3.1 Ultra-thin-film Estimation of Losses 29
2.2.3.2 Effects of Surface Roughness on Ultra-Thin-Films 31
2.2.3.3 Ultra-thin-film Measured Results 34
Chapter 3 - Thin-film Capacitors on LTCC 43
3.1 Novel Bypass and Coupling Capacitor Topologies 43

3.1.1 Low-Inductance Bypass Solution 44
3.1.2 Low-Inductance Coupling Capacitor Solution 45
3.2 Thin-film Capacitor Fabrication 46
3.3 Thin-film Capacitor Measured Results 48
3.3.1 Test Setup and Probing Location 48
3.3.2 Extracting Capacitor Parameters from S-parameter Measurements 52
3.3.3 Measured Results 53
3.3.4 Comparison with Traditional Ceramic SMD Capacitors 56
Chapter 4 - Conclusions 60
4.1 Thin-film Microstrip on LTCC 60
4.2 Effects of Thinning the Main Cu Layer 60
4.3 Thin-film Capacitors on LTCC 61
4.4 Future Directions 61
References 62
Appendix A - S-parameter Background 65

List of Figures

Figure 1.1 Typical laminate manufacturing process (figure from [7]) 2
Figure 1.2 Co-fired ceramic manufacturing process (figure from [12], reprinted with permission from Microwave Journal).. 3
Figure 1.3 High-frequency PCB material development (figure after [5]) 4
Figure 2.1 Cross-section of thin-film microstrip transmission line 10
Figure 2.2 Current distributions in a microstrip transmission line (figure from [26], copyright 1968 IEEE)... 11
Figure 2.3 Simulated losses from dielectric only for loss-tangents of 0.001 and 0.006.............. 13
Figure 2.4: Simulated losses with loss tangent set to zero for three different Cu metal thicknesses (0.5, 2 and 6 μm).. 13
Figure 2.5 Cumulative losses with and without 0.5 um surface-roughness effects..................... 14
Figure 2.6 Cross-sectional view of thin-film microstrip structure.. 15
Figure 2.7 Short segment of Ti/Cu layered microstrip with decaying longitudinal E-fields........ 15
Figure 2.8 Model of a short segment of transmission line composed of stacked Ti and Cu metals 17
Figure 2.9 Comparison of R_{eff} for attenuated and un-attenuated E-fields in Cu layer of Ti/Cu layered microstrip with t_{Ti} = 200 nm, t_{Cu} = 4 μm, l_{strip} = 1.3 inch, w_{strip} = 21.5 mil 19
Figure 2.10 Attenuation due to the conductors of Ti/Cu microstrip line of Figure 2.9 with varying Ti adhesion layer thicknesses.. 20
Figure 2.11 LTCC test panel, with visible thin-film test structures and resolution patterns........ 21
Figure 2.12 Test setup using 40 GHz HP8510 system and GGB model 40A ground-signal-ground probes... 22
Figure 2.13 Insertion loss (S21) of 1.3 inch long, 21.5mil wide microstrip line with varying Ti thickness... 23
Figure 2.14 Return loss (S11) of 1.3 inch long, 21.5mil wide microstrip line with varying Ti thickness... 24
Figure 2.15 Attenuation of a Cu microstrip line with varying Cu thicknesses............................ 26
Figure 2.16 Insertion loss (S21) of 1.3 inch long, 21.5mil wide microstrip line with varying Cu thickness... 27

Figure 2.17 Return loss (S11) of 1.3 inch long, 21.5mil wide microstrip line with varying Cu thickness ... 28
Figure 2.18 Thick and ultra-thin-film microstrip comparison on DuPont 951 with ... 30
Figure 2.19 Thick and ultra-thin-film microstrip comparison on DuPont 9K7 with ... 30
Figure 2.20 Surface roughness attenuation comparison for DuPont 951 and 9K7 substrates ... 32
Figure 2.21 Ultra-thin-film microstrip on DuPont 951 LTCC simulation with ... 33
Figure 2.22 Ultra-thin-film microstrip on DuPont 9K7 LTCC simulation with ... 33
Figure 2.23 Measured results of ultra-thin-film microstrips on DuPont 951 ... 34
Figure 2.24 Measured results of ultra-thin-film microstrips on DuPont 9K7 ... 35
Figure 2.25 Comparison of ultra-thin-film microstrip on DuPont 951 and 9K7 panels ... 36
Figure 2.26 Ultra-thin-film DC resistance comparison between DuPont 951 and 9K7 panels ... 37
Figure 2.27 SEM cross-section view of Panel 1 (951) ... 38
Figure 2.28 SEM cross-section view of Panel 2 (9K7) ... 38
Figure 2.29 Image showing layer thickness in Panel 1 (951) ... 39
Figure 2.30 Images showing layers and thicknesses in Panel 2 (9K7) ... 39
Figure 2.31 SEM visual surface roughness comparison, Panel 1 left (951), Panel 2 right (9K7) 40
Figure 2.32 AFM image of Panel 1 (951) ... 41
Figure 2.33 AFM image of Panel 2 (9K7) ... 41
Figure 2.34 Image of film discontinuity ... 42
Figure 2.35 Another thin-film discontinuity ... 42
Figure 3.1 Typical surface mount capacitor layout (side view) ... 43
Figure 3.2 Side-view of surface deposited thin-film capacitor under solder bumps ... 44
Figure 3.3 Surface deposited thin-film capacitor under solder bumps (top-view) ... 45
Figure 3.4 Schematic representation of thin-film coupling capacitor (top-view) ... 46
Figure 3.5 Thin-film capacitor test panel ... 47
Figure 3.6 Thin-film MIM capacitor showing three-terminal probing structure (from [21]) ... 47
Figure 3.7 Thin-film capacitor measurement setup ... 48
Figure 3.8 Probing locations ... 49
Figure 3.9 S_{11} results with lead in structures intact ... 50
Figure 3.10 S_{11} when probing the middle of the capacitor with the lead-in structures intact ... 51
Figure 3.11 Lead-in removal and probing location ... 51

Figure 3.12 S11 with lead-in structure removed 52
Figure 3.13 Impedance magnitude vs. frequency of 20x20mil thin film capacitor 54
Figure 3.14 Capacitance vs. frequency for 20x20mil thin film capacitor 54
Figure 3.15 Resistance (ESR) vs. frequency for 20x20mil thin film capacitor 55
Figure 3.16 Reactance magnitude vs. frequency for 20x20mil thin film capacitor 55
Figure 3.17 Image of ceramic capacitor used for performance comparison 56
Figure 3.18 Smith chart of ceramic capacitor showing the series SRF and parasitic inductance and ESR effects 57
Figure 3.19 Capacitance vs. frequency of 18pF, 0805 ceramic capacitor 57
Figure 3.20 Impedance magnitude vs. frequency of 0805 ceramic capacitor 58
Figure 3.21 ESR vs. frequency of 18pf, 0805 ceramic capacitor 58
Figure 3.22 Reactance magnitude vs. frequency of 18pF, 0805 ceramic capacitor 59
Figure A.1 2-port network with incident and reflected waves 65
Figure A.2 Lossless transmission line terminated in a load impedance Z_L (figure after [43]) 67

List of Tables

Table 1.1 Survey of microwave and millimeter wave substrate materials 6
Table 2.1 Thin-film recipes investigated with varying Ti thickness 22
Table 2.2 Thin-film recipes investigated with varying Cu thickness 27
Table 2.3 Thin-film recipes tested in ultra-thin-film experiment 29

Acknowledgements

A special thank you to Dr. Bill Kuhn for his guidance and patience throughout this "non-traditional" MSEE endeavor. Your insights and abilities to simplify complex engineering problems have been of tremendous help. I also greatly appreciate that you are a practical engineer that likes to build "real stuff" and work in the lab. Your common sense and good-natured humor did not go unappreciated especially when floundering in the uncertain waters of research. I would also like to thank the other members of my committee; Dr. Andrew Rys and Dr. Don Gruenbacher. I fully appreciate your support and guidance along the way.

Thank you to the traditional graduate students that made this older, non-traditional graduate student, feel at home after being away from school for several years. It was a huge relief not being alone while going through the coursework. It is truly amazing how much one can forget in a short five year span.

I would like to thank the sponsor of this research, Honeywell Federal Manufacturing and Technologies and also the collaborations with the University of Arkansas and the Missouri University of Science and Technology. These three organizations were invaluable in this large team-effort research endeavor.

Lastly, thank you to my family for encouraging me through both the BSEE and MSEE degrees. I certainly would not be in this position without your support.

Notice: Portions of Chapter 2 have been co-authored by Honeywell Federal Manufacturing & Technologies under contract No. DE-NA-0000622 with the U.S. Department of Energy. The United States Government retains and the publisher, by accepting the article for publication, acknowledges that the United States Government retains a non-exclusive, paid up, irrevocable, world-wide license to publish or reproduce the published form of this manuscript, or allow others to do so, for the United States Government purposes.

Dedication

This thesis is dedicated to my wife, Kimberly, for her unending support, patience and willingness to pick up and put down new roots. She has made many sacrifices in order for this endeavor to happen and I could not have succeeded without her.

Chapter 1 - Background and Introduction

1.1 Brief History of Microwave and Millimeter Wave Substrates

Electrical engineering revolves around the design and fabrication of electronic circuits and systems for various applications such as power generation and delivery, information storage and transfer, transportation, medicine, entertainment, and national defense to name a few. Electronic circuits are networks consisting of active and passive electronic devices interconnected by transmission lines. These networks manipulate electric energy in a predetermined fashion to obtain a desired transformation of the input signal. In order to deploy these electrical networks into the field, a planar, high-resistivity rigid substrate, also known as a printed wire board (PWB) or printed circuit board (PCB) is typically utilized to provide mechanical robustness and portability. Several factors impact the choice of a substrate including cost, application environment, ease of manufacturing, dielectric constant (Dk), thermal coefficient of expansion (TCE), thermal coefficient of dielectric constant (TCDk), loss tangent or dissipation factor (DF), number of layers, thermal conductivity, interconnect density, moisture absorption, re-workability, metal adhesion, conductor loss, solder mask, etc. [1][2][3]

At operational frequencies less than a few hundred MHz, PCB choice is not overly critical when it comes to signal integrity since transmission line effects are minimal. Hence cost, mechanical, and environmental characteristics will typically determine the material used. However at microwave and millimeter wave frequencies many factors need to be considered in the choice of a substrate. Substrates in this regime must support the transmission of signals with minimal loss and consistent performance while also meeting application requirements [4].

At microwave frequencies, traditional PCB laminates like copper-clad epoxy/woven glass (FR-4) suffer from high dielectric loss, and the lack of ability to tightly control the dielectric constant during manufacturing leads to poor control of transmission line impedance [5]. However, these resin-based laminates with added stiffening agents are still among the most widely adopted and cost effective PCB manufacturing process in existence today [6]. Figure 1.1 shows a diagram of the typical FR-4 resin-based laminate PCB manufacturing process. Many of the substrates in the proceeding text have been adapted for use in FR-4 manufacturing lines which has led to their widespread use and adoption.

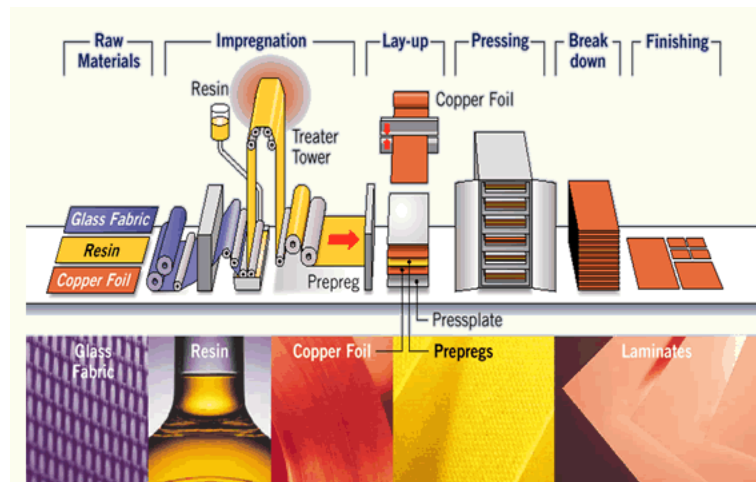

Figure 1.1 Typical laminate manufacturing process (figure from [7])

In the 1950's, the first resin based system for high frequency PCB use appeared and utilized polytetrafluoroethylene (PTFE, or Teflon®) reinforced with woven glass that addressed the above issues [5]. This technology allowed microwave designers to create circuits on a planar surface without the need for bulky waveguides. Further developments led to higher dielectric constants which allowed circuit miniaturization and increased density [5]. Pure or nearly-pure PTFE substrates offer the best electrical performance in the industry but PTFE is a 'soft' dielectric and typically requires special processing steps and suffers from dimensional and dielectric changes with temperature. This is especially problematic for microwave designs that are subjected to fluctuating temperatures and for multilayer boards where plated-through hole (PTH) alignment is critical [8].

After the Second World War, co-fired ceramics consisting of ceramic and glass powders mixed with a binding agent and solvent were being investigated to create more robust capacitors with higher self-resonant frequencies (SRF), lower equivalent series resistance (ESR) and better temperature stability[9]. During this time knowledge was gained in crystallography, phase transitions and the chemical and mechanical optimization of ceramic materials. Two leading technologies came out of this investigation; high-temperature co-fire ceramics (HTCC) and low-temperature co-fire ceramics (LTCC). However, due to the high firing temperatures, specialized equipment, high-resistivity metals used in fabrication, and cost, HTCCs were not widely adopted for use as PCBs. Nevertheless HTCCs have since been adapted for use in the ceramic capacitor and integrated circuit (IC) packaging industries due to their excellent mechanical stability,

matched TCE of metal and semiconductor substrates, thermal conductivity, ability to create hermetic seals, ability to support a large number of electrical feedthroughs in a small space, and have solderable/wire-bondable surfaces after metallization [10], [11].

LTCCs have seen more use in microwave PCB industry due to the availability of metals with much higher conductivities than those found in HTCCs, allowing for better insertion losses. Tunable Dk, good TCDk, and low DF have also contributed to their adoption by microwave designers. The lower firing temperatures of LTCC have also allowed high levels of system integration to be achieved through the use of embedded passive devices, three-dimensional structures and cavities for direct die attachment and wire bonding. Figure 1.2 shows a co-fire ceramic manufacturing process. This is the process used in the research covered in this thesis.

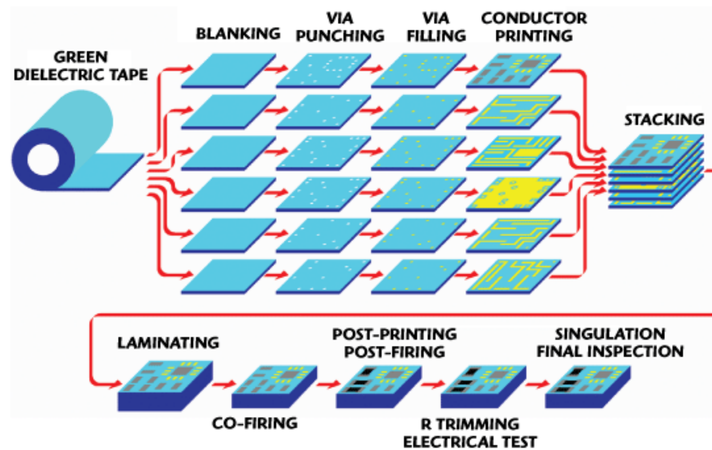

Figure 1.2 Co-fired ceramic manufacturing process (figure from [12], reprinted with permission from Microwave Journal)

Meanwhile, temperature-stable ceramic-filled PTFE composites started to appear in the early 1990's from manufacturers that addressed the thermal expansion issues plaguing the 'soft' dielectrics and allowed designers a new option for high-volume multi-layer PCB development. But due to the PTFE material, specialized processing steps were still required for creating PTHs. Specialized thermoplastic boding agents, typically with different dielectric constants, were also required for adhesion between layers of multi-layer PCBs [5]. Using thermoplastic bonding agents typically limits the number of layers that can be used due to thermal excursions in sequential lamination processes causing delamination of layers and PTH reliability [13]. However, this was still a major step forward for the microwave industry because many of the

PCB manufacturers in existence could adapt their FR-4 manufacturing lines to easily handle these new thermoplastic laminates. Thermoplastic substrates are heavily utilized for this reason and advancements in materials have led to non-PTFE-filled based substrates appearing and newer exotics such as liquid crystal polymers, cyanate esters, modified epoxies, etc.

In the mid-1990s, ceramic hydrocarbon thermoset polymer composites became available which fixed many of the issues associated with thermoplastic resins. Thermosets, when heated above a certain temperature undergo a phase change and when cooled become rigid bodies just like the thermoplastic resins. However, thermosets will not exhibit the same plasticity with repeated temperature cycling. This allows many of the traditional PCB manufacturing processes to be used without fear of delamination. Thermoset substrates combine low TCDk, a copper matched TCE, tunable and uniform Dk. When compared to co-fired ceramics, thermosets offer key fabrication advantages since they are available with copper cladding allowing the use of standard PCB subtractive processes which has led to their widespread use in the industry [14]. Figure 1.3 outlines high-frequency PCB material development relative to driving forces and shows that much of the early advancements were due to government and defense efforts and as technologies and markets have matured advances are now mainly commercially driven [5].

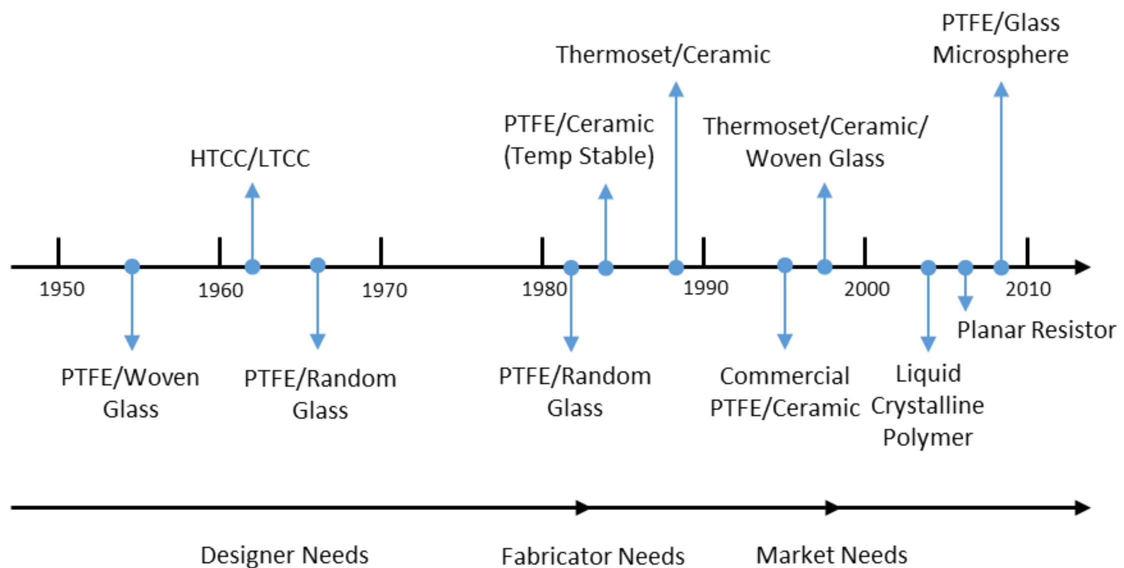

Figure 1.3 High-frequency PCB material development (figure after [5])

1.2 Summary of Substrates and Properties

Modern microwave and millimeter wave systems are continually demanding high performance substrates which continues to drive the materials industry. All of the technologies outlined above are still in use today and many derivatives can be found from a host of manufacturers. Improvements in manufacturing have allowed many of the previously cost prohibitive substrate materials to be used in high-volume manufacturing environments today [15]. In cost sensitive mixed-signal designs, several technologies may be used together such as a PTFE insert in a FR-4 board or a PTFE layer may be laminated to one side of a FR-4 board as an outer layer to achieve acceptable performance [16]. Co-fired ceramics may also be found as high-frequency modules soldered to more traditional substrates for cost-conscious designs that still have high frequency needs, or as PCBs themselves for their exceptional layer, environmental and packaging capabilities. It would be quite a large undertaking to outline all known microwave and millimeter wave substrate offerings in great detail so a more pragmatic approach is utilized. This list could go on indefinitely but in the end engineering always comes down to tradeoffs, and only after the careful consideration of design parameters, can an appropriate technology be chosen.

A sample of substrates from several industry leading manufacturers are provided in Table 1.1. The type of each substrate is presented to show that the materials discussed in section 1.1 are still produced in today's market, and to show that many companies manufacture a variety of substrates that meet the needs of many applications. Dielectric constant and loss tangent are also captured since these are typically of great concern to microwave designers and to demonstrate that many combinations are available to fit a host of needs. Manufacturing costs are shared as they are usually the discriminating factor when choosing a substrate material in the commercial world. For high performance systems where cost is not the primary driver, LTCC technologies offer high reliability, mechanical robustness, and excellent microwave performance. For this reason, this thesis focuses on LTCC technology. Lastly, a few key benefits of each PCB material system are shown to help illustrate where the materials might find use.

Table 1.1 Survey of microwave and millimeter wave substrate materials

Manufacturer	Model	Type	Dk	Df @ 10 GHZ	PCB Manufacturing Cost	Benefits
Various	FR-4 Laminates	Epoxy laminate with woven glass reinforcement	3.80 to 4.20	0.02	$	-Easy to manufacture -Low manufacturing and material cost
Rogers	RO3000 Series Laminates	Ceramic-filled PTFE laminates with available woven glass reinforcement to increase rigidity	3.00 to 10.20	0.0009 to 0.0027	$$$	-Consistent mechanical properties regardless of Dk -Good CTE allows for multilayer PCBs -Very stable Dk
Rogers	RO4000 Series Laminates	Reinforced hydrocarbon ceramic laminates	2.55 to 6.15	0.0027 to 0.0038	$$	-Can manufacture with traditional FR-4 processes -Good multilayer capability due to low TCE
Rogers	RT/duroid Laminates	Ceramic or glass filled PTFE laminates	2.20 to 10.20	0.0009 to 0.0027	$$$	-Designed for very precise microstrip and stripline applications -Dk is uniform from panel to panel and constant over a wide frequency range -High Dk can be used for circuit miniaturization
Rogers	TMM Laminates	Ceramic hydrocarbon thermoset polymer composite laminates	3.27 to 12.85	0.0019 to 0.0023	$$	-Can manufacture with traditional FR-4 processes -Thermoset material will not soften once set -Good multilayer capability due to low TCE -Laminates can be bonded directly to copper or brass plates for increased thermal capabilities -High Dk can be used for circuit miniaturization
Arlon	CLTE Series Laminates	Ceramic-filled PTFE laminates with woven glass reinforcement to increase rigidity	2.94 to 3.00	0.0012 to 0.0023	$$$	-Very good TCDk -Good TCE allows for multilayer boards -Tight thickness tolerances
Arlon	TC Series Laminates	Ceramic-filled PTFE laminates with woven glass reinforcement to increase rigidity	3.50 to 6.15	0.002	$$$	-very good thermal dissiapation characteristics ideal for high power applications -Smooth copper can be used to decrease roughness losses
Arlon	Low-Loss Thermoset Laminates	Fiberglass reinforced ceramic filled thermoset laminates	3.38 to 3.70	0.0025 to 0.0045	$$	-Can manufacture with traditional FR-4 processes -Thermoset material will not soften once set -Good multilayer capability due to low TCE
Arlon	IsoClad Series Laminates	Non-woven glass PTFE laminates	2.17 to 2.33	0.0013 to 0.0016	$$$	-non-woven materials can be used to create conformal/wrap-around antennas
Nelco	Mercurywave, N43X0 Laminates	Modified epoxy resin	3.50 to 3.80	0.0065 to 0.008	$$	-Can manufacture with traditional FR-4 processes -Good multilayer capability due to low TCE
Nelco	N8000 Series Laminates	Cyanate ester epoxy laminate	3.20 to 3.50	0.007	$$$	-Good for extremely harsh environments
Nelco	N9000 Series Laminates	PTFE laminate with woven glass reinforcement	2.08 to 4.50	0.0006 to 0.0055	$$$	-Low Dk good for very low loss antenna designs -Much better passive intermodulation performance compared to other PTFE substrates
Taconic	RF Series	Ceramic-filled PTFE laminates	2.97 to 10.00	0.0011 to 0.0038	$$$	-Smooth copper can be used to decrease roughness losses -High Dk can be used for circuit miniaturization -Low Dk good for very low loss antenna designs
Taconic	TL Series	Woven glass reinforced PTFE laminates	2.17 to 3.00	0.0009 to 0.0030	$$$	-Legacy low cost RF laminates
Dupont	Green Tape System	LTCC	7.10 to 7.80	0.001 to 0.006	$$$$	-Very low TCE allows for multilayer PCBs and direct IC attachment -Machinabililty allows 3-D structures to be realized -Metalization is wire-bondable for IC applications -High Dk allows for circuit miniaturization
Ferro	A6 Tape System	LTCC	5.90	0.002	$$$$	-Stable Dk through 110 GHz -Similar benefits to Dupont Green Tape System
Ferro	L8 Tape System	LTCC	7.30	0.002	$$$$	-Stable Dk through 40 GHz -Similar benefits to Dupont Green Tape System
Various	Alumina	99% Al_2O_3	9.00	0.0002	$$$$	-Machinabililty allows complex structures to be realized -Metalization is wire-bondable for IC applications -High Dk allows for circuit miniaturization -Good thermal conductivity allows for high power designs -Very low Df allows for low loss designs

1.3 LTCC and Metallization Patterning Techniques

Options for creating metallic interconnects on ceramic substrates are typically limited to thick-film and thin-film patterning techniques. Both methods are more costly and require special equipment for production, however, superior mechanical and electrical performance can be achieved when compared to traditional manufacturing methods.

1.3.1 Thick-film Patterning

Thick-film metallization is the most common type of metal patterning technique used in LTCC PCB manufacturing due to its simplicity and cost-effectiveness. It is an additive process in which metal-infused inks are printed onto ceramic substrates and then co-fired with the ceramic substrate. The metallized features can either be defined through masking techniques where the paste is pushed through a screen with defined openings or a uniform coating of paste can be etched after firing. In a multilayer PCB scenario, screen printing is most often utilized because etching of the inner layers is not possible after the firing process.

For microwave applications, line and space rules for traditional thick-film processes have reached 50 μm (~2 mils) in the literature [17]. Advances in thick-film fine-line printing have brought this number down to 30 μm (~1.2 mils) [18]. Edge resolutions and film thicknesses become increasingly important as the frequency of operation increases. But the accuracy of the film thickness and the resolution of the conductor edges are limited by the thick-film process itself.

Transmission line losses also become very important in microwave and millimeter wave applications. While thick-film materials, being relatively cheap and easy to produce, do well in X-band and lower applications, they suffer in applications where the operating frequency is at higher frequencies. The most notable culprit being the metal-infused inks. The inks are two-phase mixtures of ceramic glass and metals. Once fired, the film is relatively porous and prone to losses with conductivities sometimes as low as 10 percent of the conductivity of the bulk metal [19].

Several factors need to be considered when choosing a metallization [17] and no single thick-film metalized paste can meet all of these requirements. Thus for demanding microwave and millimeter wave applications, thin-film patterning techniques may be desirable.

1.3.2 Thin-film Patterning

Thin-film patterning techniques have traditionally been found in the integrated circuit industry but their use at the PCB level is becoming more widespread, especially in microwave and millimeter wave applications where tight manufacturing tolerances are required. Thin-film techniques involve depositing a thin layer of metal uniformly on a substrate and then photolithography etching processes are used to realize high-resolution structures. Due to the nature of the process, multiple metal films can be deposited sequentially with varying thicknesses before etching to produce a metallized structure that has many of the desirable features [17] outlined previously.

Metallization thickness and edge resolution can be tightly controlled in thin-film processes which is critical for low-loss transmission lines in high frequency applications. Line and space resolutions of 10 μm (~0.4 mils) on LTCC have been reported [18] which are necessary for commercially available MMICs [20]. Film quality is much greater than that of thick-film inks. The deposition process (evaporation, sputtering, etc.) produces metal films with a structure and quality similar to that of bulk metals and therefore do not suffer from the resistive losses seen in thick-film inks.

Structures other than transmission lines can be realized as well with thin-film technologies. Dielectric materials such as tantalum or aluminum oxide can be evaporated onto a thin-film metal electrode substrate to produce high-quality thin-film capacitors. High resistance materials can also be deposited to form surface-applique resistors.

Thick and thin-film technologies are often combined since thin-film patterning can only be used on the outer surfaces of a sintered LTCC substrate. Thus highly integrated microwave systems can be realized on a single substrate with non-critical metallization produced using thick-films and the tightly controlled tolerances of high frequency transmission lines produced using thin-films. This method is used for the fabricated structures in this thesis.

1.4 Thesis Organization and Contributions

This thesis is broken into four chapters with the first being a brief introduction and survey of microwave and millimeter wave PCB materials. Transmission line fabrication techniques on LTCC are also discussed. Chapter 2 explores the notion that adding a high-resistance (relative to Cu) adhesion layer to a thin-film microstrip transmission line could lead to poor microwave

performance. Reducing the thickness of metals in a thin-film stack-up to improve line and space resolution at the expense of microwave performance is also investigated. Chapter 3 looks at a thin-film capacitor solution that could lead to wide-band bypassing networks for use in flip-chip applications. Chapter 4 concludes this thesis and gives a brief overview of the work done and important findings. Suggestions for future work are also presented.

The work done in this thesis reveals that adding a lossy-adhesion layer for mechanical robustness in a thin-film transmission line on LTCC does not impact microwave performance if the adhesion layer thickness is a fraction of its skin depth at the maximum frequency of operation. Similar to the adhesion layer work, empirical evidence shows that thinning the metals in the thin-film stack-up used in this research can be done to a certain point without impacting the signal integrity of the transmission line. Further investigations show that surface roughness plays a critical role in thin-film fabrication and can cause serious electrical performance issues when the thickness of the film is pushed into the sub-micron range. The preceding results both contribute and enhance the body of knowledge for microwave engineers working with LTCC substrates and thin-film metallization.

The research done in this thesis pertaining to thin-film capacitors shows that this technology produces a broadband low-impedance bypass solution. Based upon the measured results, the coupling and bypass architectures presented may promote future technology adoption especially if it is capable of decreasing or eliminating the use of surface mount capacitors.

Chapter 2 - Thin-film Transmission Lines on LTCC

One of the main goals of this research is to understand the implications of adding high-resistance metal layers for mechanical adhesion purposes on LTCC substrates at microwave and millimeter wave frequencies. Based upon the available literature, one might conclude that adding a lossy adhesion layer could be detrimental to the microwave performance of the transmission line. However, as shown in this chapter, an adhesion layer is not a problem, provided its thickness is kept to a fraction of its skin depth.

Another investigation focuses on losses as the overall finished thickness is decreased in a thin-film recipe, namely thinning of the copper layer to reduce the z-dimension, which allows for finer line and space resolutions to be achieved in circuit board layouts. Based on lithography processes used in this research [21], the resolution achievable is a function of the overall metal thickness due to the amount of photoresist needed during the ion etching step of fabrication. To create finer line and space rules, less photoresist must be used which translates to a thinner metal film requirement. However, by going to a thinner stack-up the cross-sectional area of the conductors decrease which could lead to increased resistive losses. This is a critical hurdle as the electronics industry moves not only toward device miniaturization but also towards system miniaturization and higher frequencies of operation. This complex subject is addressed in section 2.2.

2.1 Adhesion Layer Losses in a Thin-film Microstrip Transmission Line

Copyright 2014 IEEE. Portions of section 2.1 are reprinted with permission from A. D. Fund, W. B. Kuhn, J. A. Wolf, R. J. Eatinger, K. U. Porter, M. D. Glover, and H. A. Mantooth, "Metal Layer Losses in Thin-Film Microstrip on LTCC," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 4, no. 12, pp. 1956–1962, Dec. 2014.

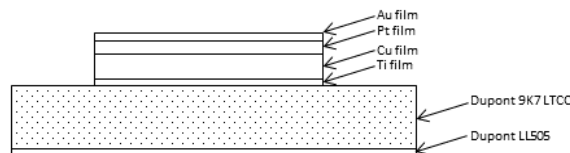

Figure 2.1 Cross-section of thin-film microstrip transmission line

Figure 2.1 shows a cross-sectional view of a stacked metal thin-film microstrip transmission line used in LTCC processes [21]. At the bottom of the stack is a thin layer of titanium metal which is used for mechanical adhesion of the thin film to the LTCC substrate. Unfortunately Ti is 25 times more resistive than the copper conductor above it and due to the nature of wave propagation and current distributions in planar microstrip transmission lines at microwave frequencies [22], concerns have arisen that the incorporation of a lossy adhesion layer could lead to excessive conductor losses accumulating along any appreciable length of transmission line [23] [19]. However, for mechanical robustness, adhesion layers are necessary when using thin-films on ceramic substrates [24] to ensure a strong chemical bond to the substrate. Titanium, chromium, and tantalum are well-known materials used frequently as adhesion layers on oxides and nitrides for other less adhesive films such as Cu [19] [25]. However, with conductivities much less than that of Cu, the concerns over including a lossy adhesion layer persist [23] due to the current distributions studied in [22] shown in Figure 2.2. If the adhesion layer carries a significant portion of the total current, then its higher resistance can be expected to produce power losses and degrade performance in microwave circuits.

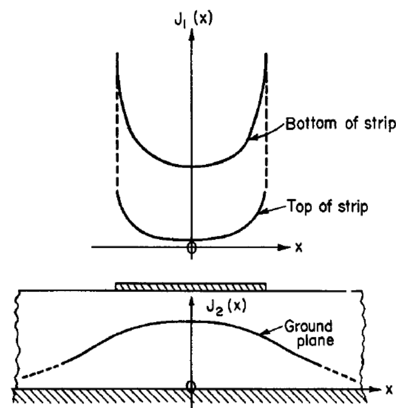

Figure 2.2 Current distributions in a microstrip transmission line (figure from [26], copyright 1968 IEEE)

In the case of printed circuit boards operating at GHz frequencies, it is known that electroless nickel/immersion gold (ENIG) surface finishes can create significant loss under certain conditions such as differential signaling where currents flow largely in the coated surfaces [27]. Hence, for microstrip on LTCC, where currents concentrate at the interface

between the metal conductor line and the substrate where the high-resistance adhesion layer resides, significant losses may also be expected.

A thin-film stack-up consisting of Ti/Cu/Pt/Au has been proposed to address the adhesion issue while providing good microwave performance. This stack-up provides for solder and wire bond connectivity and corrosion resistance [21] and is used as the basis for this research. In order to look at the effect a lossy adhesion layer has on microstrip line losses, several LTCC panels were fabricated with varying adhesion layer thicknesses, and loss characteristics were assessed for each case.

2.1.1 Estimation of Adhesion Layer Losses

For a microstrip line with a sufficiently thin dielectric layer, the dominant losses along the line result from the finite conductivity of the metals, surface roughness, and polarization losses within the substrate. It is quite difficult to separate these losses in measured results. However, computer-based simulators offer a way to explore the contributions of each loss mechanism mentioned above.

2.1.1.1 Simulation of Losses

Ideally a 3D electromagnetic simulator can model the full physics of the layered-metal, dielectric, and surface roughness problem. However, 3D simulation attempts with thin layered metals using two different commercial-grade simulators failed to produce reasonable results. The issues are still being investigated by the software developers at the time of this writing. To quantify some of the basic losses involved, a simpler 2.5D simulator was therefore employed. This allows assessment of the relative contribution of dielectric, metal, and roughness effects through the embedded closed-form modeling equations employed, but not the effects of layered metals.

To estimate the loss contribution from the dielectric only, the metal is set to infinite conductivity while the substrate loss is modeled with an appropriate loss-tangent entry. Conversely, to isolate metal losses, the substrate loss-tangent is set to zero and the metal conductivity set to a value representative of the Cu material used. Figure 2.3 and Figure 2.4 show the results using the Agilent ADS simulator configured to model a 10 mil wide, 1.3 inch long microstrip line on an 8.5 mil thick LTCC substrate with permittivity of 7.1.

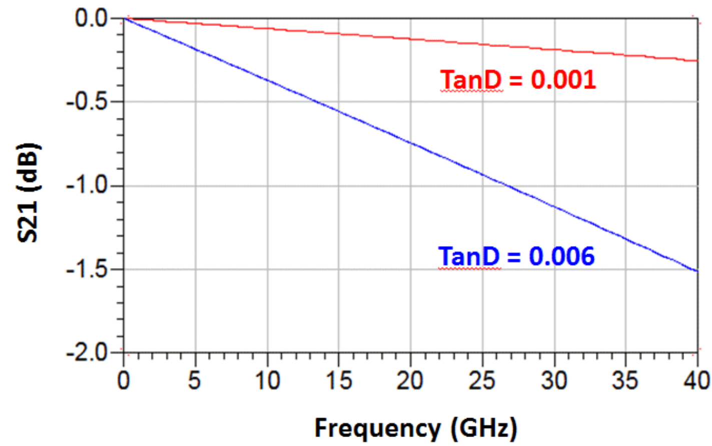

Figure 2.3 Simulated losses from dielectric only for loss-tangents of 0.001 and 0.006

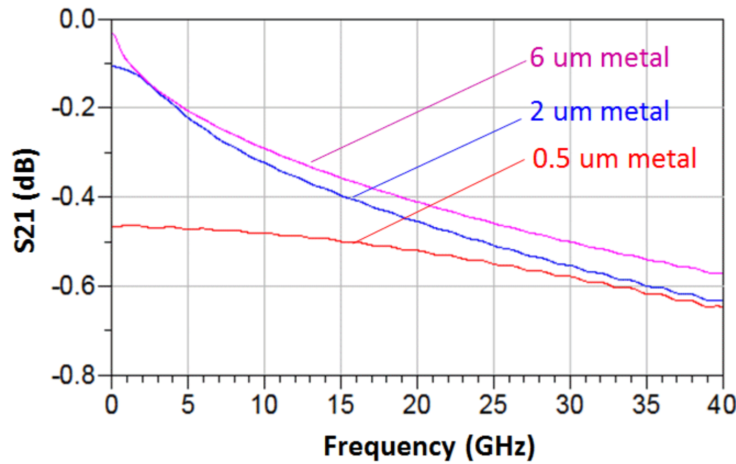

Figure 2.4: Simulated losses with loss tangent set to zero for three different Cu metal thicknesses (0.5, 2 and 6 µm)

For loss tangents in the 0.001 range (typical for microwave targeted LTCC), we see that dielectric losses and metal losses are comparable, but that metal losses play a more dominant role. This is especially true at low frequencies for thinner films. At higher frequencies metal-only loss is not a strong function of thickness, since all cases shown are at least one skin depth at about 20 GHz. (Thicker metal has a slight advantage at higher frequencies, since there is more surface area for current flow when the sidewalls of the line are accounted for.)

Surface roughness must also be considered in microwave transmission lines since it essentially lengthens the line within the thin layer in which the currents flow, further increasing the metal loss. The effect is illustrated in Figure 2.5 which shows the cumulative result of dielectric loss and metal loss with and without 0.5 µm of roughness. For both cases, the line is 10

mils wide and 1.3 inch long as before, and the loss tangent is 0.001. Cu metal with a thickness of 2 μm is used. Note that the effect of roughness increases with frequency since the active region of current flow is substantially thinner than the 2 μm bulk metal thickness at microwave frequencies, and this active region is mainly at the metal-substrate boundary where the roughness is present.

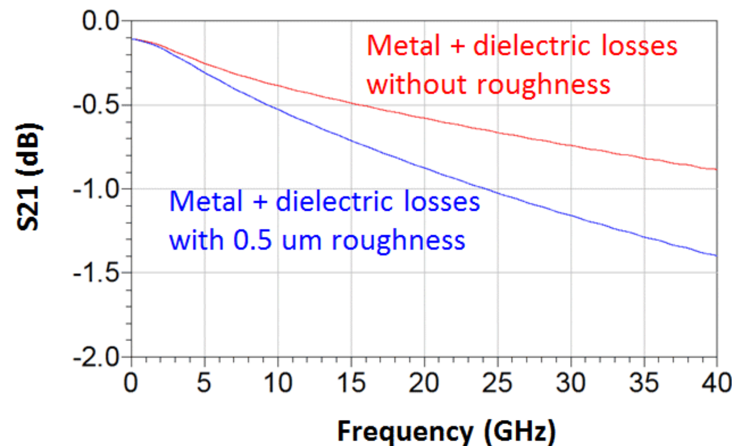

Figure 2.5 Cumulative losses with and without 0.5 um surface-roughness effects

Simulations such as these, while providing some ability to independently quantify metal and dielectric losses and possibly provide an assessment of layered metal effects if a 3D simulation can be successfully completed, provide limited insight into the physics behind the losses observed. Moreover, with limited opportunity to observe their solution methods, their ability to accurately quantify the effect of stacked metal systems remains open to question. With this in mind, a simple analytic model is proposed next to estimate those effects, and the analysis is then validated in the following section using measured results. To simplify the problem, the analysis is done under the constraint that the adhesion layer thickness is significantly less than its skin depth, and roughness is not modeled. Since skin depth of a higher resistivity material is comparatively large, these assumptions are reasonable for obtaining a rough order of magnitude estimate.

2.1.1.2 Analytic Modeling of Stacked-Metal Losses

Figure 2.6 shows a thin-film microstrip line looking in from one end. In this case, if a voltage is applied to this end, a strong vertical E-field results as shown. Currents in the line also

create a companion H-field, resulting in a quasi-TEM wave propagating longitudinally down the line.

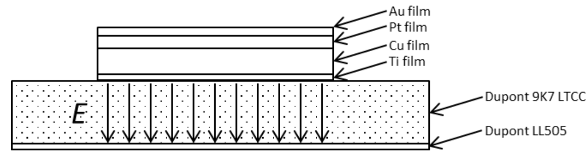

Figure 2.6 Cross-sectional view of thin-film microstrip structure

Figure 2.7 shows the same line rotated 90 degrees so that the longitudinal E-fields can be seen within the metals. Specifically the E-fields and resulting currents within the metals that make up the microstrip line are the quantities of interest. Note that for real, finite-conductivity metals, a small, but non-zero longitudinal E-field is required to support the RF currents that flow in the microstrip as the signal propagates down the line away from the source. These fields are exaggerated in Figure 2.7 to show the field-decay within the metals under study. To concentrate on the main problem at hand, the problem has been simplified by ignoring currents on the sides and top of the line, which are somewhat lower in amplitude due to the dielectric constant of air versus that of the substrate. Only the main fields and currents at the metal-substrate interface are studied here.

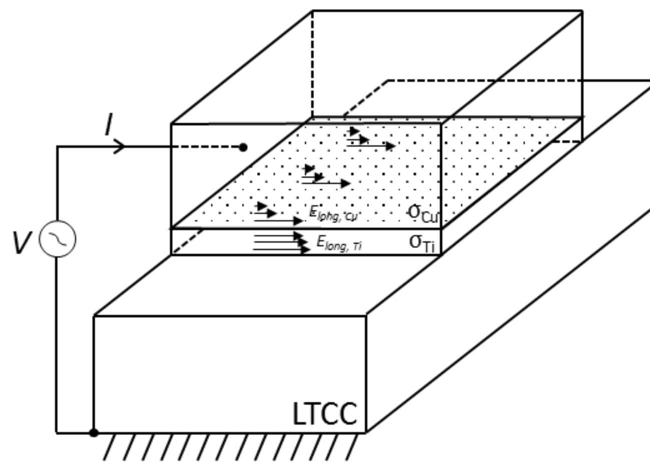

Figure 2.7 Short segment of Ti/Cu layered microstrip with decaying longitudinal E-fields

It is a well-known fact from electromagnetics that such electric fields within a good conductor decay exponentially resulting in shallow penetration depths from the surface, or in this

case from the substrate-metal interface. However, in a multi-layer thin-film configuration, the fields may not decay appreciably in the first layer if the thickness of the conductor is sufficiently less than its associated skin depth. For example, if the two-layer microstrip case of Figure 2.7 is considered, with t_{Ti} = 200 nm and t_{Cu} = 4 μm respectively, it can be shown that at 40 GHz, 88% of the longitudinal electric field will reach the Ti/Cu interface, and the field will then decay primarily within the Cu metal. This is illustrated in Figure 2.7 by the moderate shortening of E_{long} between the Ti-substrate and Ti-Cu boundaries and the rapid shortening within the Cu metal. Thus, the current distribution within the Ti layer will largely resemble that of a uniform DC scenario and the resistance of this layer can be approximated using the DC resistance formula.

$$R_{DC} = \frac{l}{\sigma A} \tag{2.1}$$

where σ is the conductivity of the metal, *l* is the length of the metal, and *A* is the cross-sectional area of the metal under consideration.

As the field enters the Cu layer it decays rapidly due to the higher conductivity of this metal, reducing the useful thickness of the Cu to approximately one skin depth, making the AC resistance higher than its DC resistance. Equation 2.2 gives the AC resistance of the conductor as

$$R_{AC} = \frac{l}{\sigma \delta w} \tag{2.2}$$

where *w* is width of the conductor, and *δ* is the skin depth of the conductor and is defined as

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}. \tag{2.3}$$

Since the field has already been attenuated slightly by the Ti layer, a small reduction in the amount of current flowing in the Cu layer will occur relative to what it would be if the Ti were not present. This reduction in current will result in a slight increase in the *effective* AC surface resistance of the Cu layer.

Referring to Figure 2.8 this behavior is further explained quantitatively. As a first-order approximation, the stacked configuration of Figure 2.6 can be viewed as the lumped-element current divider model shown in Figure 2.8 with the resistance of the Ti layer approximated as the bulk DC case and the resistance of the Cu layer being a modified form of its AC surface resistance.

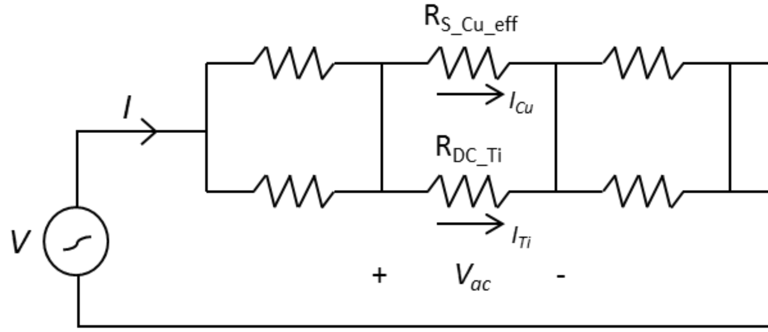

Figure 2.8 Model of a short segment of transmission line composed of stacked Ti and Cu metals

As previously stated, the E-field at the Ti/Cu interface is slightly attenuated due to the presence of the Ti adhesion layer, and can be modeled as

$$E_{Cu} = kE_{Ti} \tag{2.4}$$

where k is slightly less than unity and quantifies the attenuated E-field at the Ti/Cu interface. From electromagnetics, its value is found from

$$k \stackrel{\text{def}}{=} e^{-\frac{t_{Ti}}{\delta_{Ti}}} \tag{2.5}$$

where δ_{Ti} is the skin depth of titanium and t_{Ti} is the thickness of the titanium adhesion layer. According to Figure 2.8, the current in the each layer can be found through Ohm's law as

$$I_{Ti} = \frac{V_{ac}}{R_{DC_Ti}}, \tag{2.6}$$

and

$$I_{Cu} = \frac{kV_{ac}}{R_{S_Cu}} \tag{2.7}$$

with the modified EMF kV_{ac} seen across the Cu layer. The *effective* surface resistance in the Cu layer can now be defined as

$$R_{S_Cu_eff} \stackrel{\text{def}}{=} \frac{R_{S_Cu}}{k} \tag{2.8}$$

and the current in the Cu layer becomes

$$I_{Cu} = \frac{V_{ac}}{R_{S_Cu_eff}} . \tag{2.9}$$

Realizing these resistances are in parallel, they can be combined using the standard circuit formula to find the resulting total effective resistance of the Ti/Cu structure

$$R_{eff} = R_{DC_Ti} || R_{S_Cu_eff} = \frac{(R_{DC_Ti})(R_{S_Cu_eff})}{R_{DC_Ti} + R_{S_Cu_eff}} \tag{2.10}$$

which reduces to

$$R_{eff} = \frac{(R_{DC_Ti})(R_{S_Cu})}{kR_{DC_Ti} + R_{S_Cu}} . \tag{2.11}$$

This modified parallel resistance formula (per unit length) results in a net effective resistance slightly larger than the parallel combination of the DC resistance in the Ti layer and the un-modified AC surface resistance in the Cu layer. As previously explained, this is an expected result due to the attenuation of the electric field as it traverses the finite thickness of the adhesion layer.

Figure 2.9 shows a comparison between effective resistances of the layered strip for the attenuated and un-attenuated E-field cases using equations (2.5) and (2.8). For the case shown, with t_{Ti} = 200 nm, t_{Cu} = 4 µm, l_{strip} = 1.3 inch, the total effective resistance is not substantially increased with the Ti introduced. This is a direct result of the longitudinal E-field reaching the Cu metal without strong attenuation.

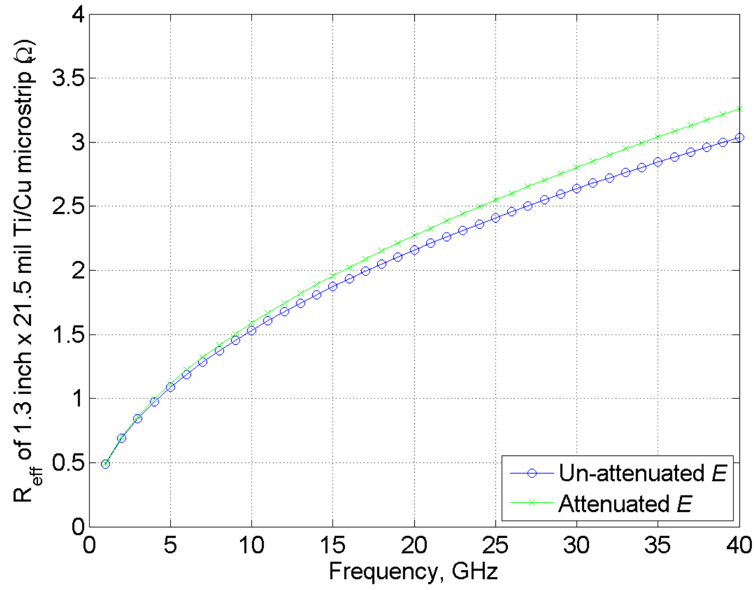

Figure 2.9 Comparison of R_{eff} for attenuated and un-attenuated E-fields in Cu layer of Ti/Cu layered microstrip with t_{Ti} = 200 nm, t_{Cu} = 4 μm, l_{strip} = 1.3 inch, w_{strip} = 21.5 mil

Figure 2.10 shows the corresponding incremental increases in attenuation of the Ti/Cu microstrip as the Ti layer is thickened. Here, the attenuation from the conductors in a low-loss scenario have been converted to dB using

$$\alpha_{cond} = 4.34 \left(\frac{R_L}{Z_0}\right) dB \tag{2.12}$$

where R_L is the resistance of the line [28]. Figure 2.10 shows this attenuation for the parameters of Figure 2.9 and reveals that the addition of the Ti adhesion layer provides minimal excess loss for the thicknesses and frequencies considered in this study. The measured results in Figures 2.13 and 2.14 confirm this result.

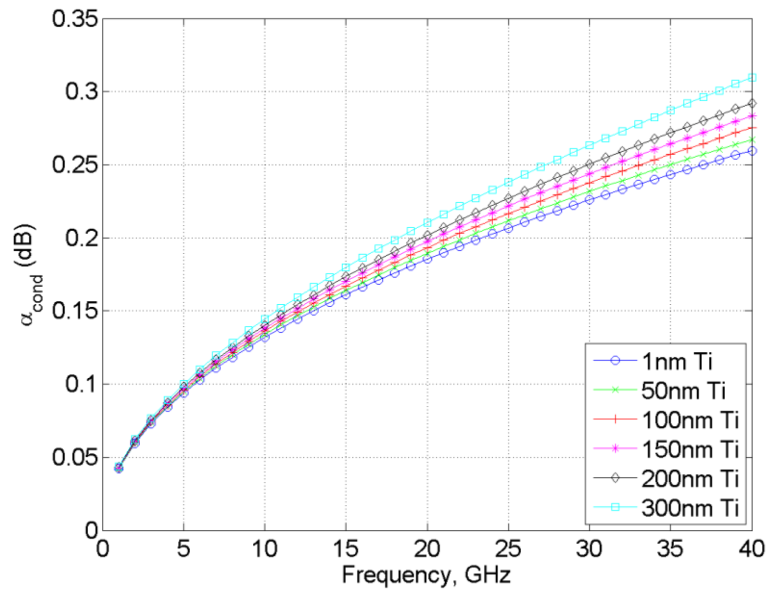

Figure 2.10 Attenuation due to the conductors of Ti/Cu microstrip line of Figure 2.9 with varying Ti adhesion layer thicknesses

2.1.2 Experimental Setup

Ultimately, experimental results, if carried out carefully, provide the most fidelity in assessing a complex issue such as the effect of metal layering in microstrip lines. This section describes the test setup used to assess losses based upon varying adhesion layer thicknesses. In this experiment, Ti/Cu/Pt/Au thin-films on low-loss DuPont 9K7 LTCC are investigated. A test panel is shown in Figure 2.11 and includes microstrip lines to directly measure transmission-line losses. The thickness of the Ti adhesion layer was varied through fabrication of multiple panels and the S-parameters of the microstrip lines were extracted using a HP8510 vector network analyzer (VNA) through 40 GHz.

The LTCC substrates were fabricated by partnering institutions using four 10 mil-thick sheets of DuPont 9K7 Green Tape^{TM} resulting in a fired thickness of 35 mils for mechanical stability. The microstrip lines are formed on the top surface, with a ground-plane two layers below. DuPont LL505 gold paste and thick-film techniques were used in ground plane construction while DuPont LL500 gold paste was used as via fill material in the ground-signal-ground probe sites at the ends of the lines. The surface deposited microstrip test structures were constructed using physical vapor deposition methods along with photolithography and ion-beam milling techniques. The thin-film metallurgical properties used in this research included a 200

nm-thick adhesion layer of Ti followed by a 4 μm-thick layer of Cu, a 2 μm-thick layer of Pt, and a 0.375μm-thick layer of Au for a total finished thickness of 6.575μm. Figure 2.6 shows the stacked structure of the fabricated microstrip lines. A 0.0215 x 1.3 inch microstrip was used to ensure that sufficient loss accumulated along the length of the line to allow even small variations in loss to be measureable with network analyzer equipment whose resolution and noise limits are in the 0.1 dB range.

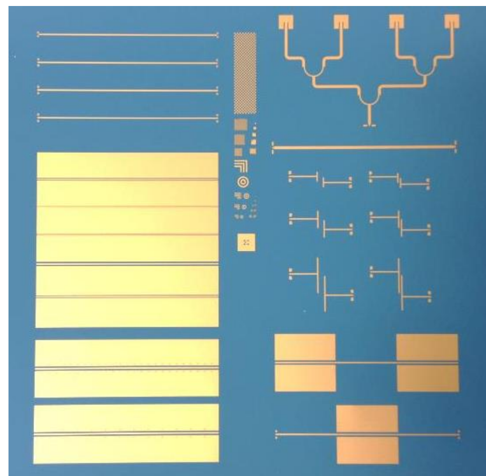

Figure 2.11 LTCC test panel, with visible thin-film test structures and resolution patterns

Performance measurements were carried out using a HP8510 VNA with a frequency span of 45 MHz to 40 GHz with 801 sample points. Probing of the microstrip line was performed with 500 micron GGB Industries ground-signal-ground (GSG) coplanar probes. GSG probes were used to facilitate simple DUT probing and for their ability to produce more accurate results at GHz frequencies due to their inherently lower ground inductance, fringing capacitances and ability to more tightly control the electromagnetic fields around the signal probe [29]. A standard two-port calibration was performed using a GGB GSG CS-9 alumina calibration substrate to remove the systematic errors and losses within the VNA, its associated cabling, and the GSG probes. Figure 2.12 shows images of the measurement setup and probed microstrip line.

Three panels were fabricated with the film thicknesses shown in Table 2.1. The Ti adhesion-layer thickness was varied while all other layer thicknesses were held constant.

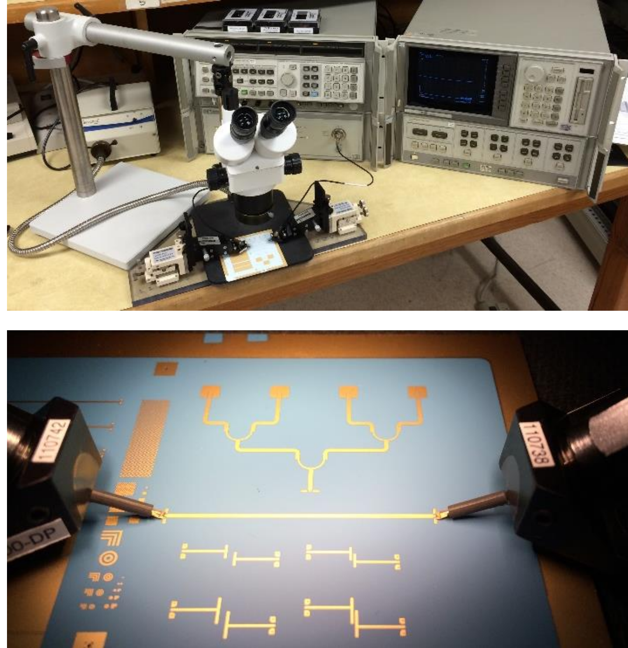

Figure 2.12 Test setup using 40 GHz HP8510 system and GGB model 40A ground-signal-ground probes

Table 2.1 Thin-film recipes investigated with varying Ti thickness

	Ti (μm)	Cu (μm)	Pt (μm)	Au (μm)
Panel 1	0.200	4.00	2.00	0.375
Panel 2	0.050	4.00	2.00	0.375
Panel 3	0.000	4.00	2.00	0.375

2.1.3 Measurement Results

Measured insertion loss and return loss for the three recipes is shown in Figures 2.13 and 2.14, respectively. Within the microwave region from 1 to 40 GHz, total losses vary from approximately 0.2 to 3 dB for the 1.3 inch length line. In contrast, variations across the three recipes are less than the total trace-noise of about 0.1 dB. Clearly, there is a negligible difference in insertion loss between the configurations tested as predicted in the results of Figure 2.10. The dip at 7 GHz is believed to be due to electromagnetic radiation loss, since measured return loss is less than ideal at this frequency as seen in Figure 2.14. At frequencies above 15 GHz through 40 GHz, the S21 response rolls off significantly. This roll off is believed to be due to the frequency-

dependent nature of the complex dielectric constant of the 9K7 LTCC [30], as well as limitations of the calibration using the available HP8510 system. Nevertheless, the relative losses with and without Ti layers is clearly less than 0.1 dB, which is consistent with the 0.04 dB loss increase predicted by the analysis of the previous sections. As a check on overall measurement accuracy, we note that comparison of the total loss with that reported in [31] is consistent when loss is adjusted for line-length differences in the two cases. This total loss effectively masks the small increase in metal loss from the adhesion layer – making the adhesion layer losses negligible in a practical sense at all frequencies.

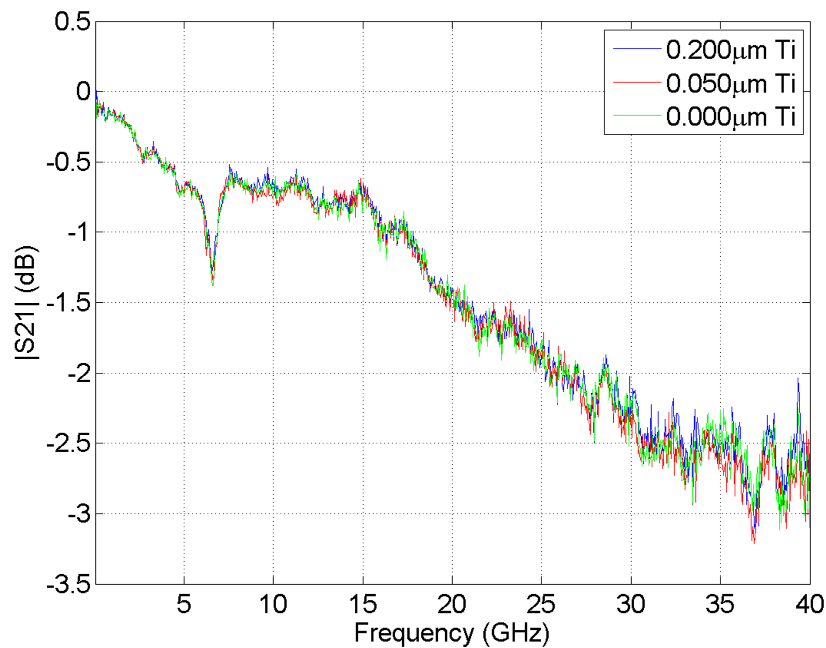

Figure 2.13 Insertion loss (S21) of 1.3 inch long, 21.5mil wide microstrip line with varying Ti thickness

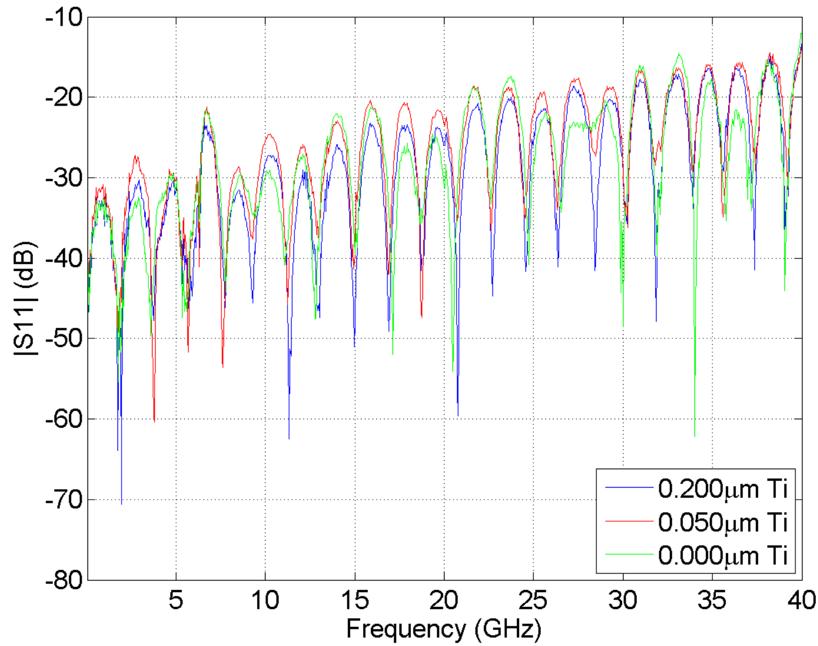

Figure 2.14 Return loss (S11) of 1.3 inch long, 21.5mil wide microstrip line with varying Ti thickness

2.2 Losses Due to Thinning of Cu-layer

As previously mentioned, shrinking of the overall height of thin-film stack-up is of interest to achieve improved line and space resolutions for the manufacturing process used in this research. The use of thinner metals allows less photoresist to be used in the ion etching step of fabrication reducing etch times and allowing for finer geometries to be obtained. This is a critical hurdle as the electronics industry moves not only toward device miniaturization but also towards system miniaturization and higher frequencies of operation. With the dimensions presented in [20], 1 mil line and space rules are quickly becoming required for systems to operate in the millimeter wave frequency band. However, thinning of the metals to improve line and space resolution may come at a cost of increased losses in the associated transmission lines.

With [21] as the reference recipe, the Ti layer is used for good mechanical adhesion to the LTCC substrate, the Cu layer is used for good RF conductivity, the Pt layer is used for solderability and as a barrier layer between the Cu and Au layers to prevent metal creep, and the Au layer is used for wire bondability. The results found in the previous section indicate that a majority of the current is carried in the Cu layer and if the skin depth of Cu is considered then

considerable thickness could be removed from the Cu layer while still maintaining acceptable microwave and millimeter wave performance.

In this work Cu layer thicknesses of 4 μm, 2 μm, 1 μm, and 0.45 μm are tested. Except for the 0.45 μm case, all other metal thicknesses are held constant and shown in Table 2.2. Details of the 0.45 μm case are explained in section 2.3.3.

2.2.1 Estimation of Losses

Much of the simulation and analytic modeling methods from section 2.1.1 can be utilized in this investigation. As previously discussed in section 2.1.1, a 3D EM simulator would ideally be used to predict the effects of thinning the Cu layer, but unfortunately the simulators available were unable to produce results that correlated well with the empirical results obtained. Therefore, Agilent's ADS 2.5D planar simulator will be utilized to investigate the losses in the microstrip transmission lines used in this research. The same analytical model found in section 2.1.1.2 can be used for this work as well. Sections 2.2.1.1 and 2.2.1.2 present an estimation of the losses one might expect when removing thickness in the Cu layer.

2.2.1.1 Simulation of Losses

Simulation data using Agilent's ADS simulator is shown in Figure 2.15. A microstrip line with a width of 21.5 mils, length of 1.3 inches was simulated on a DuPont 9K7 dielectric with a thickness of 17 mils and a loss tangent set to zero. The metal used in this simulation was Cu with a conductivity set to 5.96E7 S/m. The results follow those of Figure 2.4 and predict that at lower frequencies, there will be a larger impact on performance due to thicker skin depths. However, with a difference of roughly 0.08 dB between the 4 μm and 1 μm Cu thicknesses this should be of little practical concern. As the frequency approaches 7 GHz the losses between all three scenarios are nearly identical as the skin effect theory predicts. There is a slight separation at higher frequencies, but the difference is likely negligible in a real world setting.

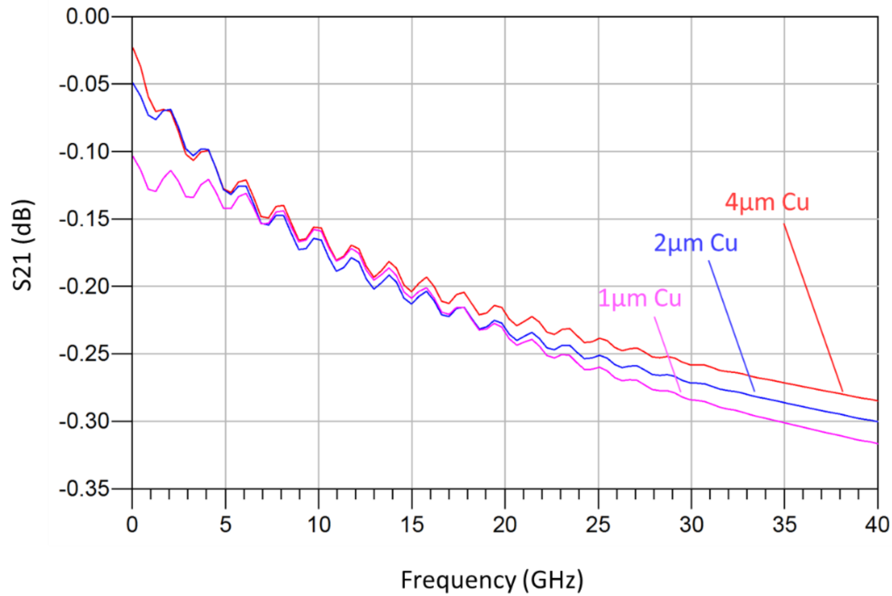

Figure 2.15 Attenuation of a Cu microstrip line with varying Cu thicknesses

2.2.1.2 Analytic Modeling of Thinning Cu-layer Losses

Following the approach outlined in 2.1.1, the same ideas can be employed to model the losses that arise when considerable thickness is removed for the Cu layer. The results mirror those found in Figures 2.9 and 2.10 for the 4 µm and 2 µm Cu cases since the skin depth of Cu is thinner than the deposited Cu thicknesses over the frequency range of interest. However, the 1 µm case will behave somewhat like the Ti adhesion layer issue explained in section 2.1 at frequencies lower than 7 GHz because the thickness of the Cu layer will be smaller than the skin depth of Cu. Therefore, some of the longitudinal E-field will penetrate into the less conductive Pt layer causing increased losses. As the frequency becomes greater than 7 GHz the 1 µm thickness becomes greater than the skin depth of Cu and has losses similar to 4 µm and 2 µm cases.

With the mathematical complexities of microstrip transmission lines in conjunction with multiple layers thinner than their skin depths', the problem quickly becomes quite difficult to model accurately with the methods of section 2.1.1. Hence, the electronic simulations in section 2.1.1 are used to provide a first order estimate of the microwave performance of the Cu layer variations.

2.2.2 Measured Results

The experimental setup detailed in section 2.1.2 is employed in this experiment as well. Measured insertion loss and return loss for the three recipes is shown in Figures 2.16 and 2.17, respectively. Metal recipes used in this experiment are shown in Table 2.2.

Table 2.2 Thin-film recipes investigated with varying Cu thickness

	Ti (μm)	Cu (μm)	Pt (μm)	Au (μm)
Panel 1	0.200	4.00	2.00	0.375
Panel 2	0.200	2.00	2.00	0.375
Panel 3	0.200	1.00	2.00	0.375

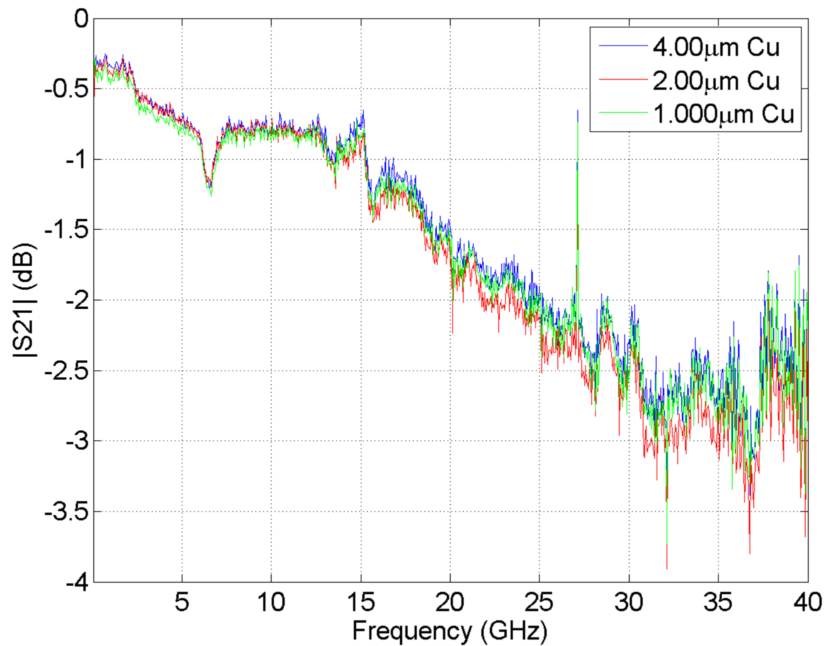

Figure 2.16 Insertion loss (S21) of 1.3 inch long, 21.5mil wide microstrip line with varying Cu thickness

As discussed in section 2.2.1 and shown in Figure 2.16, the reduction in Cu thickness has little effect on the microwave performance of the recipes tested. A slight separation of 0.1 dB of the 1 μm sample can be seen at frequencies lower than 10 GHz which is an expected result. Above 15 GHz there is little difference between the 4 μm and 1 μm panels. The fact that the 2

μm panel has slightly more loss than the 1 μm line likely indicates a slight probe placement variation due to the use of a manual probing system [29]. Many of the same conclusions found in section 2.1.3 hold true for this experiment as well such as the significant roll-off above 15 GHz, the radiation loss at 7 GHz, and the total loss being consistent with the results found in [31]. The results shown in Figures 2.16 and 2.17 confirm that thinning of the Cu layer to facilitate better line and space resolutions can be done without sacrificing microwave performance—to a certain point, which will be discussed in the following section.

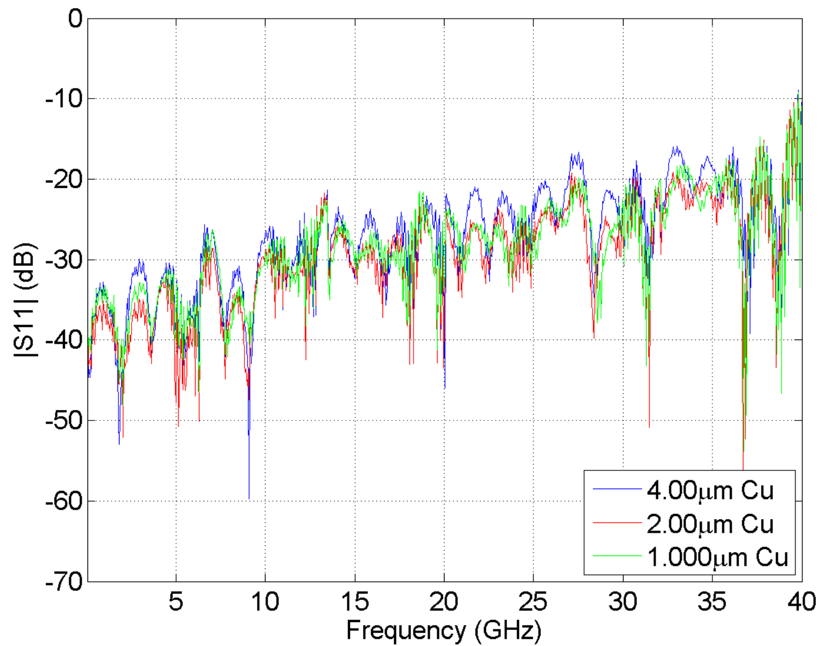

Figure 2.17 Return loss (S11) of 1.3 inch long, 21.5mil wide microstrip line with varying Cu thickness

2.2.3 Ultra-thin-film Investigation

In an effort to further push the line and space rule limits of the thin-film fabrication process used in this work, the thicknesses of all metal layers in the stack-up were decreased substantially. The trials investigated are given in Table 2.3 and the microstrip lines have a finished thickness of 0.65 μm.

Table 2.3 Thin-film recipes tested in ultra-thin-film experiment

	LTCC Type	Ti (μm)	Cu (μm)	Pt (μm)	Au (μm)
Panel 1	951	0.050	0.400	0.150	0.050
Panel 2	9K7	0.050	0.400	0.150	0.050
Panel 3	951	0.000	0.450	0.150	0.050
Panel 4	9K7	0.000	0.450	0.150	0.050

Both DuPont 951 and 9K7 LTCC materials were used in this investigation since their roughness profiles vary, with 951 having an RMS roughness of less than 0.34 μm and 9K7 with an RMS roughness of less than 0.52 μm respectively. In the case of microstrip lines, [32] shows that substrates with larger roughness features will exhibit greater resistance than a substrate with smaller features due to an effective increase in the path length the current must travel. This may be especially critical when considering metal films that will have a total thickness comparable to the surface roughness features of the substrate. Therefore, simulations were done to compare losses between thick and ultra-thin conductors and losses when smooth substrates and those with the 951 and 9K7 roughness profiles listed above are used with ultra-thin-films.

2.2.3.1 Ultra-thin-film Estimation of Losses

Figures 2.18 and 2.19 show the S21 results of the ADS simulations for the thick and ultra-thin-film microstrip on DuPont 951 and 9K7 respectively. The surface roughness was set to zero for these simulations to quantify the losses associated with metal thickness and substrate loss-tangent only. The results indicate that if the intended application is not extremely sensitive to transmission line losses then a small sacrifice in microwave performance could be made for an improvement in line and space resolution, especially if operating at high frequencies. The waviness of the 9K7 simulation starting around 20 GHz is caused by a slight characteristic impedance mismatch due to the original LTCC panel design being based on the DuPont 951 dielectric constant[1].

[1] 951 and 9K7 panels were fabricated using the same mask set, so a slight mismatch occurred on the 9K7 panels and is captured in the 9K7 simulations.

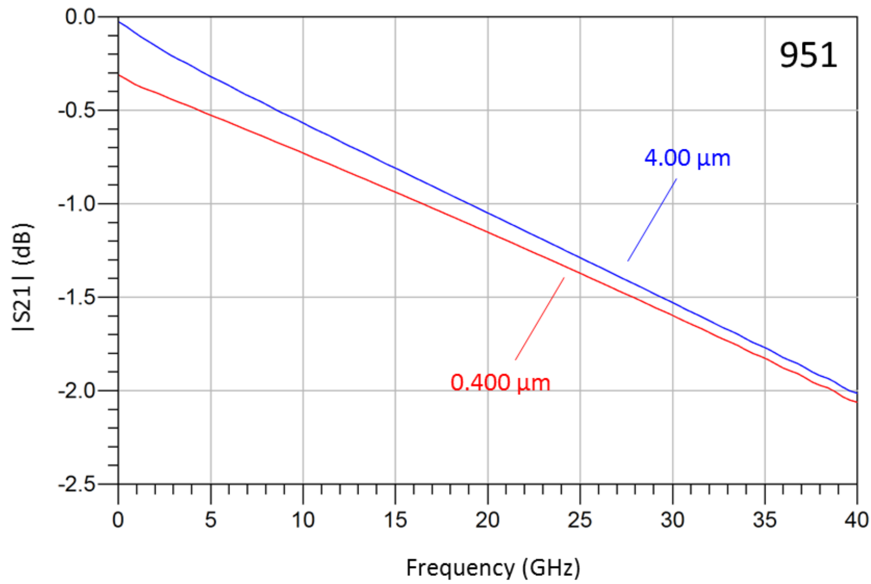

Figure 2.18 Thick and ultra-thin-film microstrip comparison on DuPont 951 with ***σ_{cond} = 5.96E7 S/m, t_{diel} = 17 mils, ε_r = 7.8, and tanδ = 0.006***

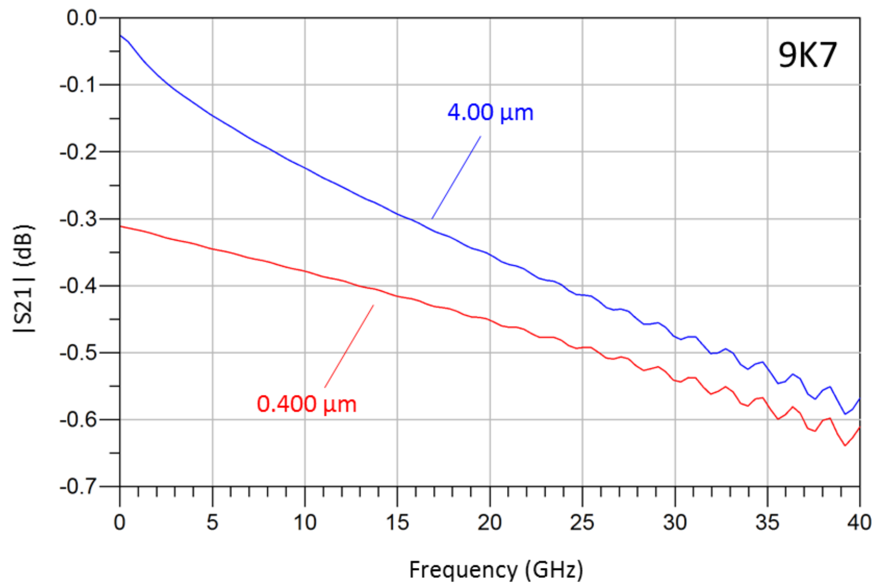

Figure 2.19 Thick and ultra-thin-film microstrip comparison on DuPont 9K7 with ***σ_{cond} = 5.96E7 S/m, t_{diel} = 17 mils, ε_r = 7.1, and tanδ = 0.001***

2.2.3.2 Effects of Surface Roughness on Ultra-Thin-Films

Before turning directly to a simulator to estimate the attenuation effects due to surface roughness, an empirically derived model for copper films in a microstrip configuration [33] was considered. Equation (2.13) includes an additional loss term to capture the added attenuation from a non-smooth surface,

$$\alpha_c' = \alpha_c \cdot K_{SR} \tag{2.13}$$

where α_c' is the total attenuation coefficient with surface roughness included, and K_{SR} is the additional loss due to surface roughness and is calculated as [33],

$$K_{SR} = 1 + \frac{2}{\pi}\arctan\left[1.4\left(\frac{\Delta}{\delta}\right)^2\right] \tag{2.14}$$

where Δ is the RMS surface roughness value and δ is the skin depth. Notice that at DC, the arctan quantity goes to zero and K_{SR} becomes one which implies a perfectly smooth surface. Plotting equation (2.13) in Figure 2.20 for a Cu conductor and using the respective roughness profiles of 951 and 9K7 shows that one could expect roughly 20% more loss due to surface roughness when using 9K7 substrates. However, this slight increase in attenuation may be of little importance to the designer since the 9K7 material will still exhibit better high-frequency performance than 951 due to its smaller loss tangent.

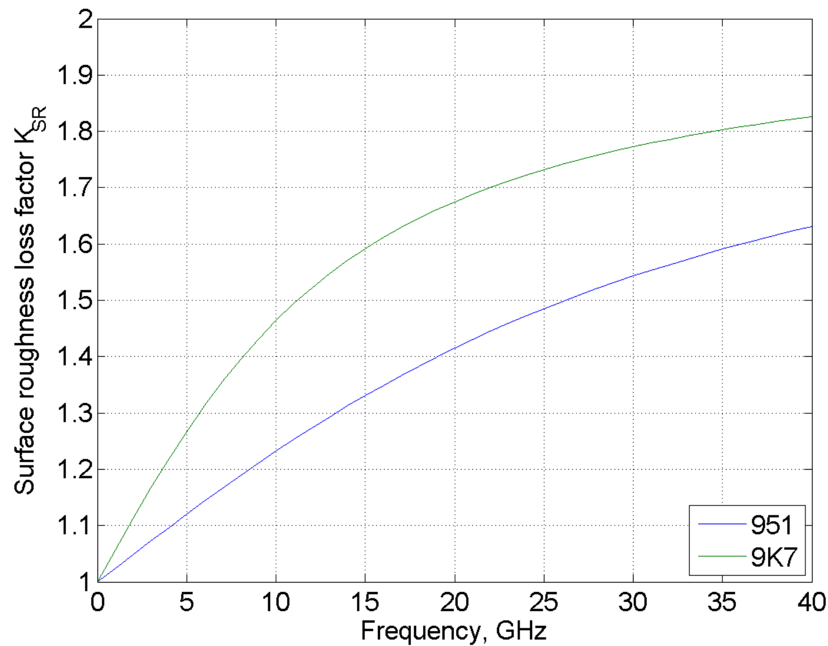

Figure 2.20 Surface roughness attenuation comparison for DuPont 951 and 9K7 substrates

Figures 2.21 and 2.22 show results of ADS simulations for the microstrip lines when the ultra-thin metals and surface roughness are both considered. The roughness of the substrates show increasing losses with frequency as expected. The simulations show a relatively rough substrate could be used with minimal added loss, as predicted by Figure 2.20, for the sake of good film adhesion as well as saving time and manufacturing costs by avoiding polishing steps to enhance substrate smoothness. However, as the measured results in section 2.2.3.3 will show, unexpected behaviors can arise with ultra-thin metals on LTCC substrates.

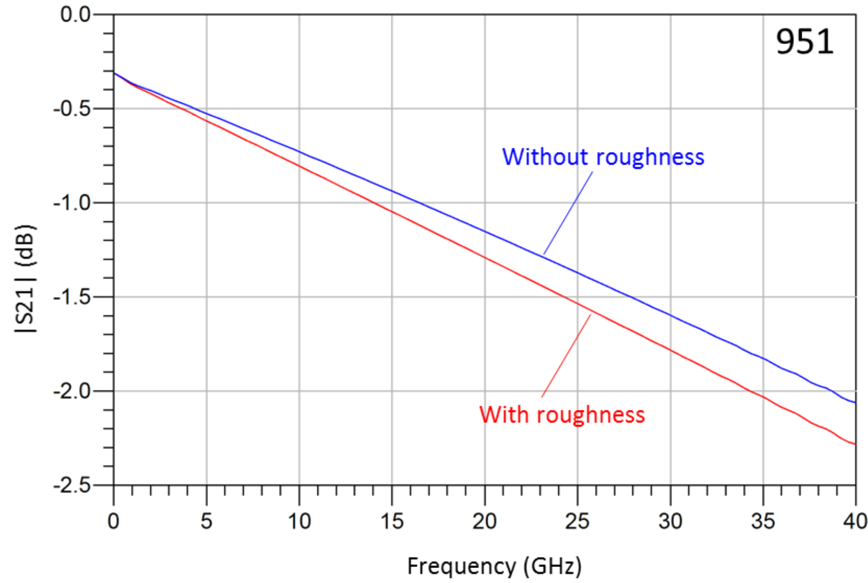

Figure 2.21 Ultra-thin-film microstrip on DuPont 951 LTCC simulation with ***t_{cond} = 0.400μm, σ_{cond} = 5.96E7 S/m, t_{diel} = 17 mils, ε_r = 7.8, and tanδ = 0.006, RMS roughness = 0 and 0.34μm***

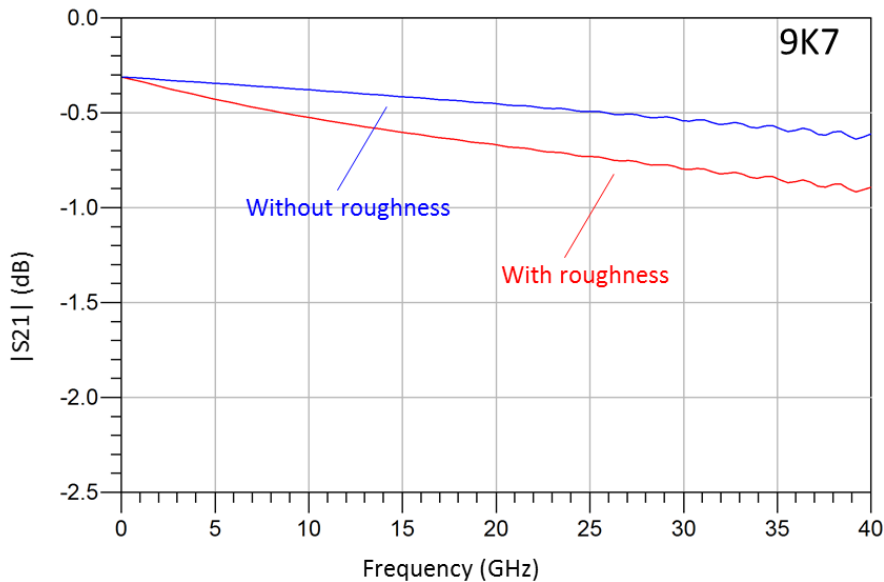

Figure 2.22 Ultra-thin-film microstrip on DuPont 9K7 LTCC simulation with ***t_{cond} = 0.400μm, σ_{cond} = 5.96E7 S/m, t_{diel} = 17 mils, ε_r = 7.1, and tanδ = 0.001, RMS roughness = 0 and 0.52μm***

2.2.3.3 Ultra-thin-film Measured Results

Measured results were obtained using the same VNA setup found in section 2.1.2. The thin-film recipes measured in this work are those shown previously in Table 2.3. Insertion loss comparisons between the 951 and 9K7 panes are shown in Figures 2.23 and 2.24. Comparing the simulated results to the measured results reveals some rather large differences. Focusing firstly on the 951 panels, the simulated losses below 3 GHz match the empirical results fairly well. Beyond this point, the measured results incur greater losses at a higher rate with increasing frequency. The overall behavior of the measured results correlates well with the simulated results other than the increased losses of the actual panels.

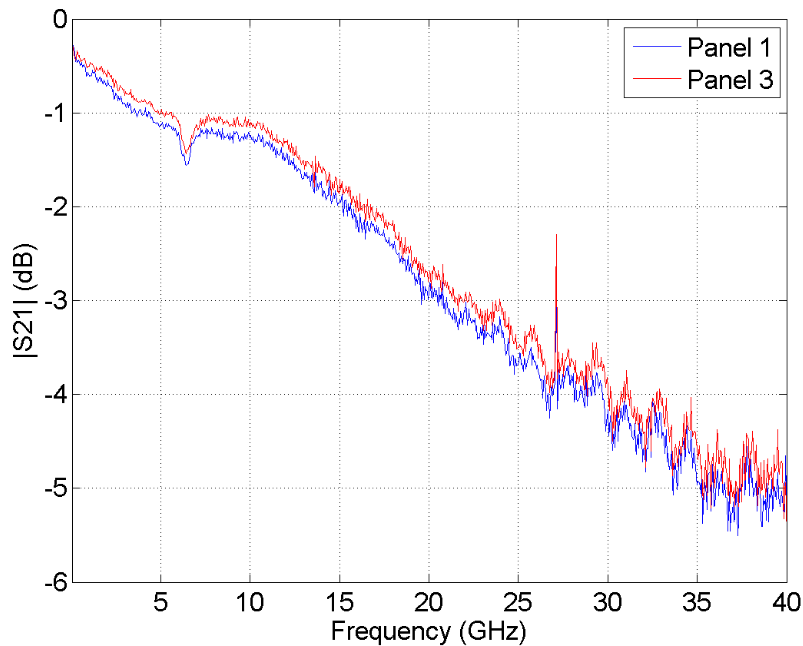

Figure 2.23 Measured results of ultra-thin-film microstrips on DuPont 951

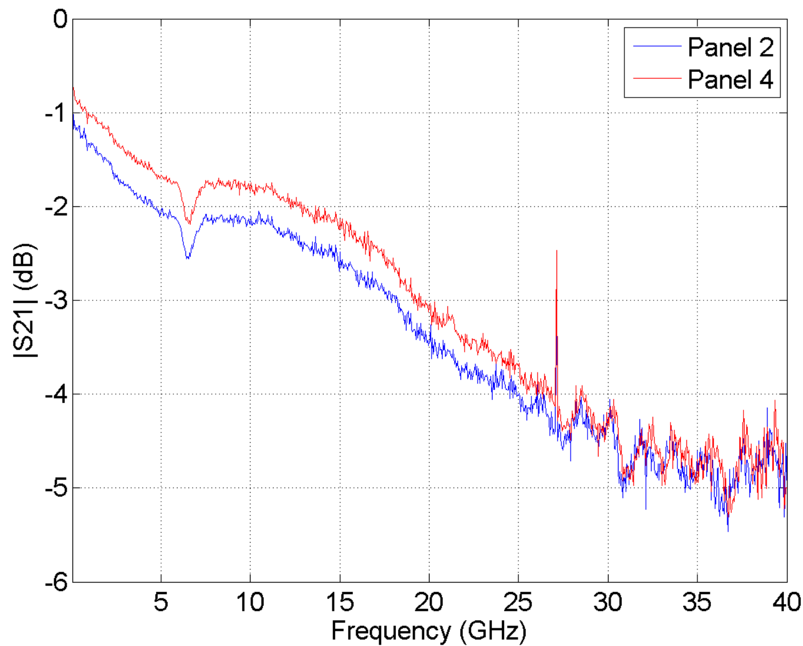

Figure 2.24 Measured results of ultra-thin-film microstrips on DuPont 9K7

Comparing the 9K7 panel results in Figure 2.24 to those of Figure 2.22 show a large difference in S21 performance. The measured results are nearly 4 dB lower at 40 GHz than the predicted values from the simulator. An interesting result is obtained if the measured results of the 951 and 9K7 panels are compared. Figure 2.25 shows this comparison. In theory, the performance of the 9K7 panels should be better than the 951 panels due to the lower loss tangent of the material. However, as Figure 2.25 shows, at frequencies less than 35 GHz the 951 material exhibits better S21 performance. The S21 performance difference is especially evident at frequencies less than 15 GHz with differences as much as 1 dB. This likely means that either the panels were fabricated incorrectly or that simulation models have issues when ultra-thin metal thicknesses are used. Attention was turned towards the first hypothesis since the problem even occurs at DC.

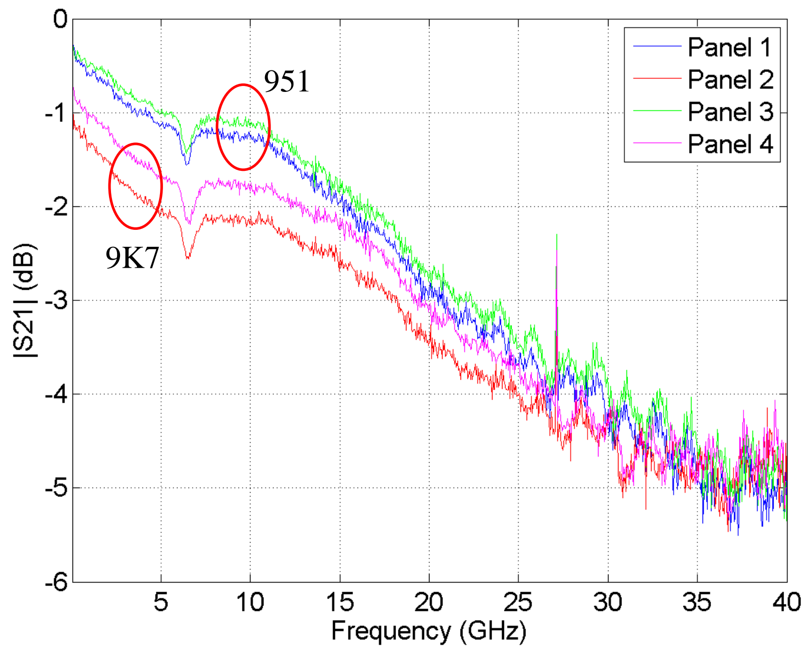

Figure 2.25 Comparison of ultra-thin-film microstrip on DuPont 951 and 9K7 panels

Initial investigations into this phenomenon started with simple DC measurements of the top conductor of the microstrip structures to verify the 9K7 panels did indeed have a higher resistance than the 951 panels. Figure 2.26 shows a measured DC resistance comparison between Panel 1 and Panel 2 from Table 2.3. Based on the empirical results of Figure 2.26, the resistance in the 9K7 panel is more than 3 times greater than that of the 951 panel which indicates a metal thickness issue or a mechanical integrity issue.

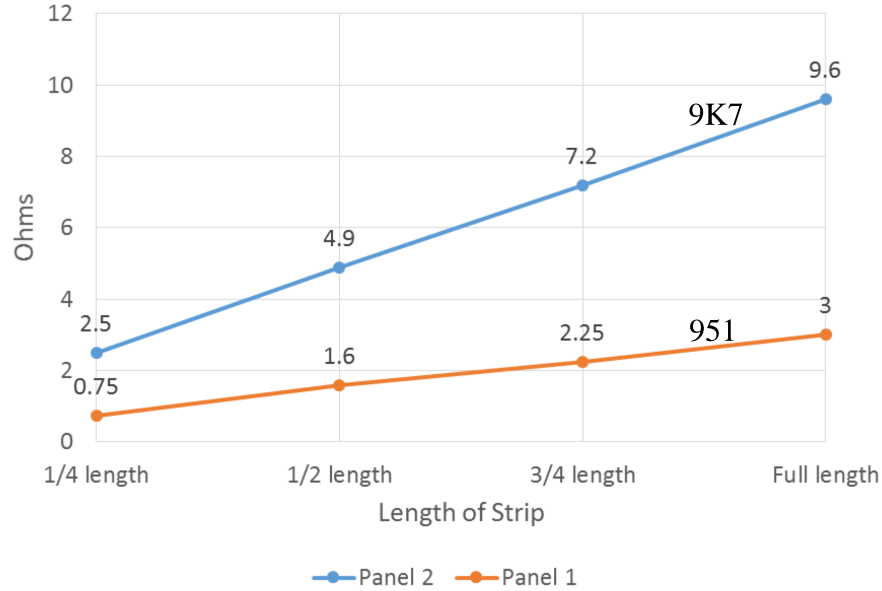

Figure 2.26 Ultra-thin-film DC resistance comparison between DuPont 951 and 9K7 panels

Referring to the structure of the microstrip line in Figure 2.6 and neglecting the ground plane, circuit theory suggests the structure of the top strip could be modeled as a simple current divider at DC. The resistance of each layer can be calculated using (2.1) and Table 2.3. The resistances can be combined using the parallel resistor formula to find the resistance of the full-length composite structure as

$$R_{strip} = R_{Ti}||R_{Cu}||R_{Pt}||R_{Au} = 2.2\Omega \tag{2.15}$$

which is relatively similar to the measured 951 panel (Panel 1, right side of Figure 2.26)) but nearly 4 times less than what the measurements show for the 9K7 panel (Panel 2, right side of Figure 2.26). In order to reach the reported Panel 2 resistance assuming all other layer thicknesses in the stack-up were correct, the Cu layer would need to have had a thickness roughly 1/10 of the reported 0.400 μm, or 40 nm. Other layers could be suspect as well, but the Cu layer is the most dominant material when considering the net resistance of the structure.

To assess actual layer thicknesses, the panels were examined by the University of Arkansas' HiDEC facility using a focused ion beam system for cross-sectioning Panel 1 and Panel 2 and a scanning electron microscope to view the cross-sectioned thin-films. Figures 2.27 and 2.28 show the cross-sectioned views for Panel 1 and Panel 2 respectively. Figures 2.27 and

2.28 show the thin-film to be intact but the surface of Panel 2 (9K7) appears to be much rougher than that of Panel 1 (951).

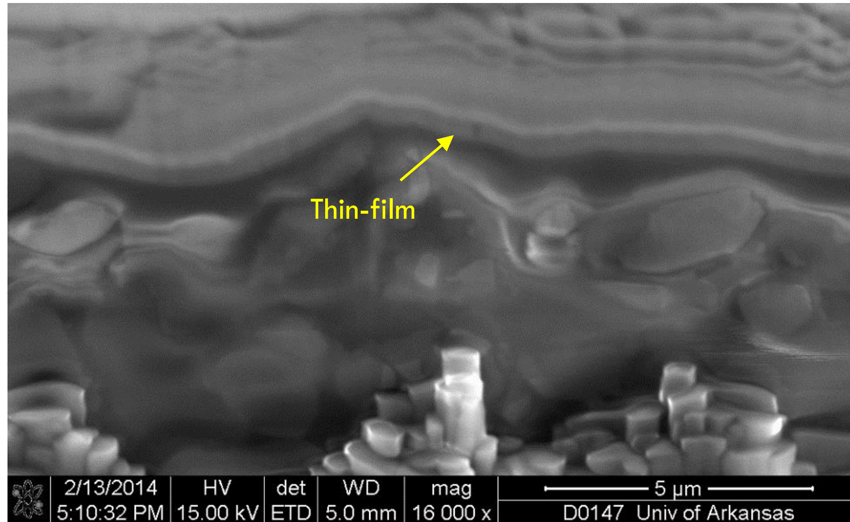

Figure 2.27 SEM cross-section view of Panel 1 (951)

(Photo courtesy of University of Arkansas High Density Electronics Center)

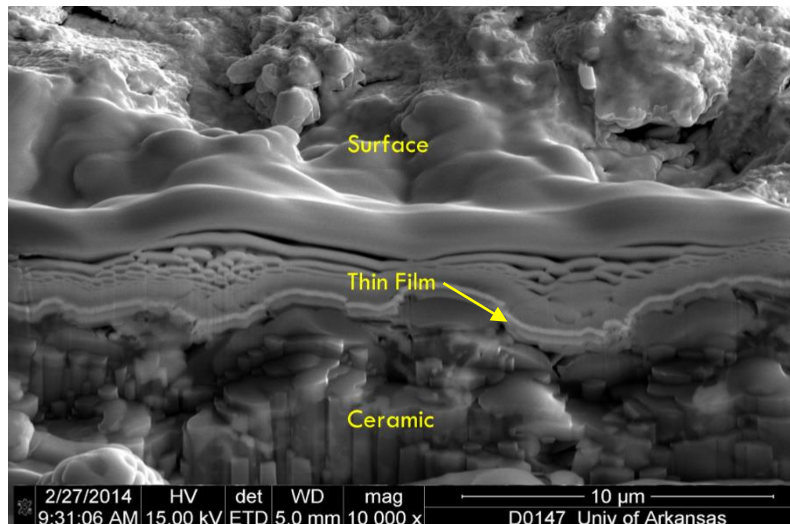

Figure 2.28 SEM cross-section view of Panel 2 (9K7)

(Photo courtesy of University of Arkansas High Density Electronics Center)

Figures 2.29 and 2.30 show the thin-film measured thicknesses of the cross-sectioned panels. In the areas tested, the reported thicknesses are consistent with the recipes shown in

Table 2.3. Based upon this evidence it seems that another factor is producing the higher resistance being seen on Panel 2 (9K7).

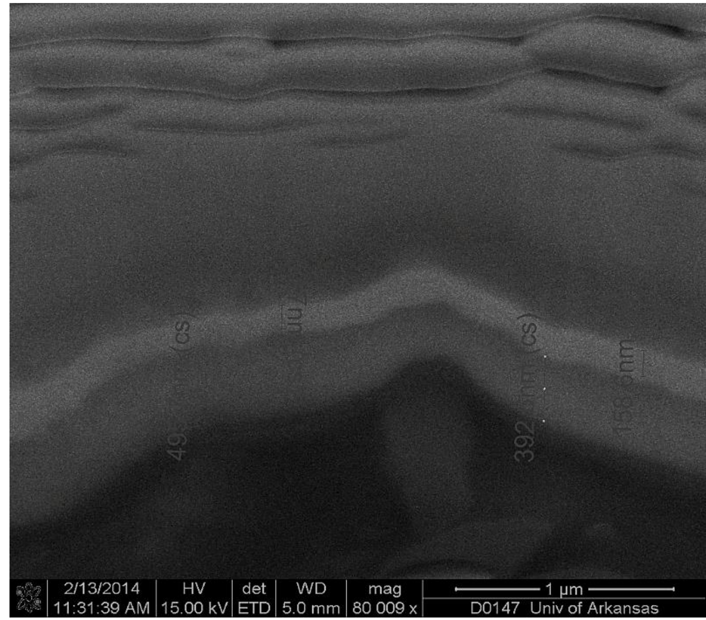

Figure 2.29 Image showing layer thickness in Panel 1 (951)

(Photo courtesy of University of Arkansas High Density Electronics Center)

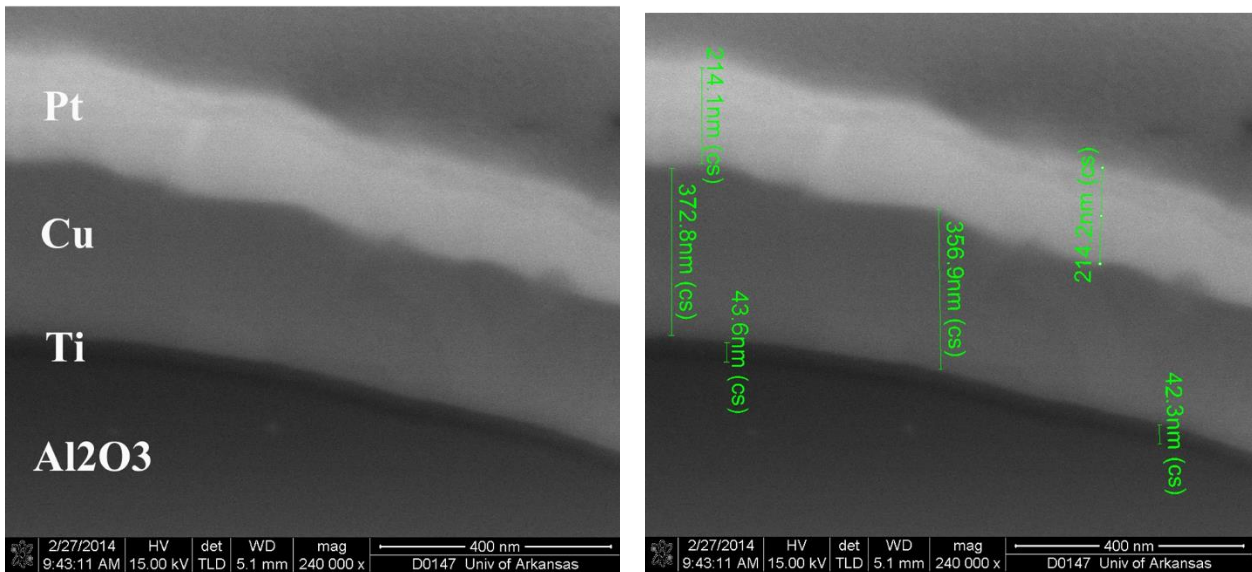

Figure 2.30 Images showing layers and thicknesses in Panel 2 (9K7)

(Photo courtesy of University of Arkansas High Density Electronics Center)

With the metal thicknesses confirmed, attention was shifted to the surface roughness of the two materials. With a reported roughness of almost 2X that of the 951 material, “shadowing” and breaks in the thin-film continuity of the 9K7 panel were suspect. A visual comparison of SEM surface images in Figure 2.31 reveal that the 9K7 panel is rougher as expected. The 951 panel has a more undulating surface with few sharp transitions between peaks and valleys in contrast to the sharp and jagged nature of the 9K7 surface which could lead to poor thin-film coating when using ultra-thin-films.

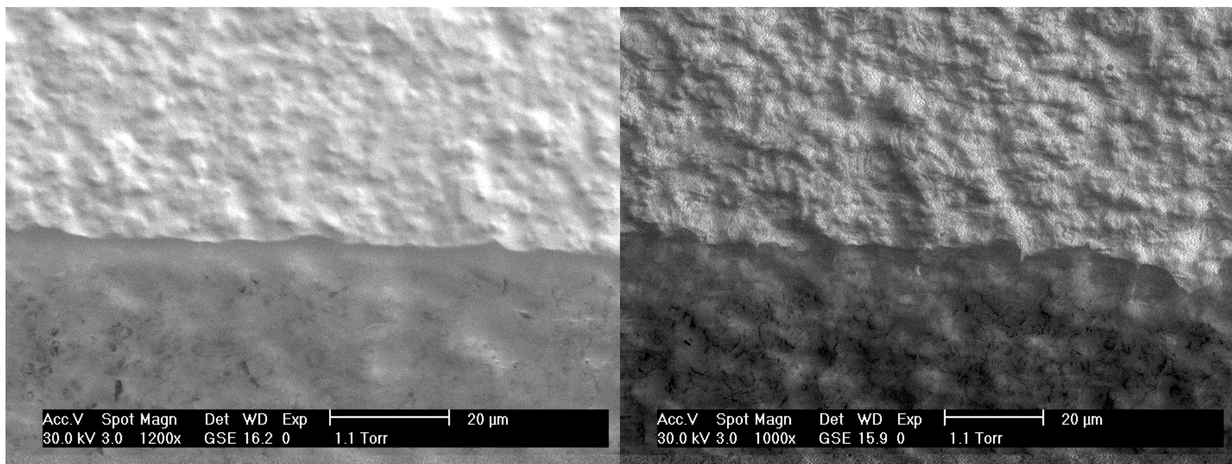

Figure 2.31 SEM visual surface roughness comparison, Panel 1 left (951), Panel 2 right (9K7)

(Photo courtesy of University of Arkansas High Density Electronics Center)

Atomic force microscopy (AFM) was used to empirically verify the visual observations discussed above. Figures 2.32 and 2.33 show the surface profiles over a length of 10 µm for Panel 1 and Panel 2 respectively. The undulating nature of Panel 1 comes through in Figure 2.32 with gradual transitions between colors representing the elevation of its surface features. The mountainous behavior of Panel 2 can clearly be seen in Figure 2.33. The jaggedness of the surface features are especially evident with the rate of change in the colors of the image. Of note is the closeness of the extreme elevation changes in Panel 2. The closeness of the peaks and valleys make for an extremely difficult environment to produce ultra-thin-films with consistent thickness and continuity. Figures 2.34 and 2.35 show the consequences of trying to deposit ultra-thin-films on 9K7. Holes and breaks in the film are clearly evident and lead to the poor performance shown in Figures 2.23 and 2.24. This evidence clearly shows that the robustness of using ultra-thin-films to achieve improved line and space resolution is poor at best. If one

desires to use ultra-thin-films then it is likely that surface smoothing treatments will need to be applied to 9K7 substrates.

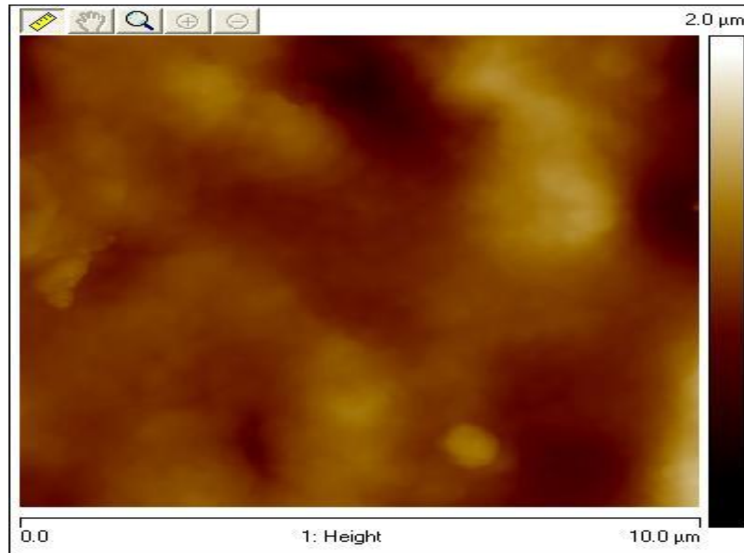

Figure 2.32 AFM image of Panel 1 (951)

(Photo courtesy of University of Arkansas High Density Electronics Center)

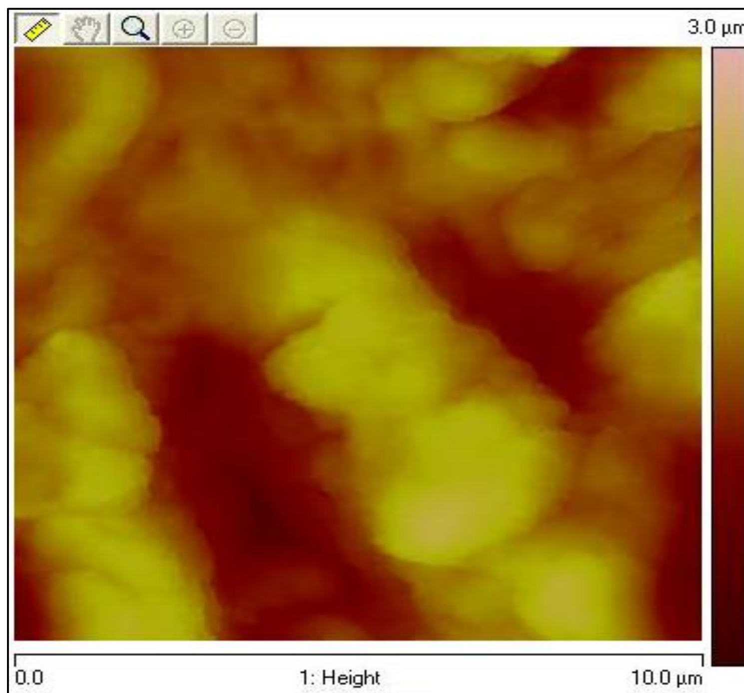

Figure 2.33 AFM image of Panel 2 (9K7)

(Photo courtesy of University of Arkansas High Density Electronics Center)

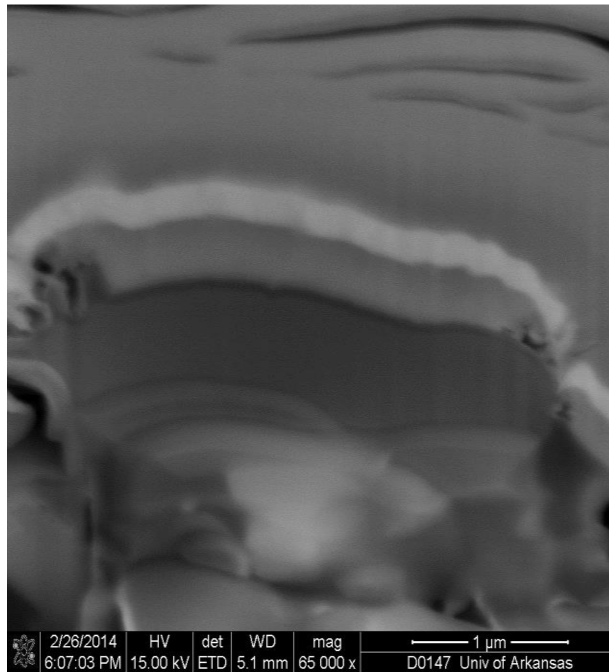

Figure 2.34 Image of film discontinuity

(Photo courtesy of University of Arkansas High Density Electronics Center)

Figure 2.35 Another thin-film discontinuity

(Photo courtesy of University of Arkansas High Density Electronics Center)

Chapter 3 - Thin-film Capacitors on LTCC

This chapter characterizes metal-insulator-metal (MIM) capacitors on LTCC for use at microwave and millimeter wave frequencies. The capacitors in this research were fabricated using thin-film techniques to address issues found with traditional surface-mount ceramic capacitors when operating at microwave and millimeter wave frequencies. The work done in the following sections represents a first step in developing novel bypass and coupling capacitors to minimize the parasitic inductance problem found in traditional PCB layout techniques in this frequency range.

3.1 Novel Bypass and Coupling Capacitor Topologies

Parasitic inductance plagues traditional passive surface mount devices (SMD) in the microwave and millimeter wave frequency regimes. This inductance dominates the device impedance at high frequencies and is a result of the physical length of the component coupled with the length of its interconnect. For example, even though the case size of an SMD capacitor may only be 40 by 20 mils, traditional layout and decoupling techniques still result in signal path lengths of multiple millimeters, yielding a net *inductive* impedance of >100 Ohms at 10 GHz.

To illustrate this problem, Figure 3.1 shows a traditional decoupling/bypass layout using a surface mount capacitor. If we ignore mutual inductance effects and use the well-known 25 nH/inch or 1nH/mm approximation for the self-partial inductance of a wire, we find loop inductances on the order of 5-10nH for a 0402 case size [28]. Even at 1 GHz, this results in the capacitor presenting an *inductive* impedance of 30Ω and this number only gets larger with increases in frequency. Minimizing such loop inductance is the key to decreasing the impedance of decoupling networks which allows for wide-band system operation.

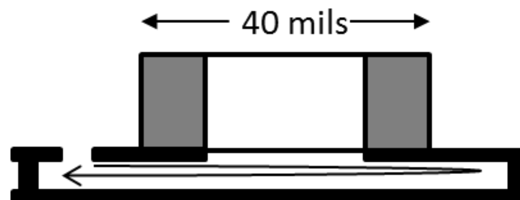

Figure 3.1 Typical surface mount capacitor layout (side view)

3.1.1 Low-Inductance Bypass Solution

Current solutions to lowering loop inductance include decreasing SMD case size, using beam-lead and metal-insulator-semiconductor (MIS) chip capacitors, integrating passive devices within a substrate [34] [35], die bonding to capacitive interposers [36], and on-chip capacitor integration [37]. However when interconnects, wire bonds, and vias are included in the loop of Figure 3.1, the inductance is still excessive. To address this problem a new topology is proposed here and in [38] to minimize inductance in bypass networks. The topology involves using surface deposited thin-film capacitors in conjunction with flip-chip bonding and co-planar waveguide ground-signal-ground structures as shown in Figures 3.2 and 3.3.

In this new configuration, the parasitic inductance is greatly minimized due to a much smaller current loop, which in-turn decreases the impedance of the decoupling network. For example, if it is assumed that the solder bump pitch of Figure 3.2 is 0.1 mm (4 mils) and the solder bump height is also 0.1 mm [39], then using the approximation from [28] yields an inductance of roughly 0.4 nH for each G-S loop. However, since a G-S-G configuration is used, the currents will split in half making the inductance of the network 0.2 nH. Comparing this to the SMD result above shows an 98% decrease in the inductance of the decoupling network which translates to a 98% decrease in the inductive impedance allowing the decoupling network to remain effective at up to 50 times higher frequencies.

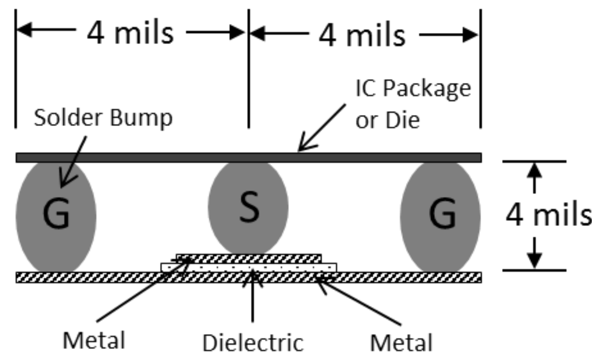

Figure 3.2 Side-view of surface deposited thin-film capacitor under solder bumps

Although not elaborated above, for this technology to work well, it is critical for the thin-film capacitor to have a thin dielectric (e.g. ≤ 1 μm) with a sufficiently high Dk to achieve the capacitances necessary for bypassing. For lower Dk materials a large layout area may be required which is addressed in section 4.3. With the 100 μm ball pitch considered above, a

square MIM capacitor such as in Figure 3.3 will yield a C value of only 9 pF if alumina is used as the dielectric, where typically 100 pF or more is needed. However with high Dk materials such as barium titanate , with a Dk reaching over 600, the resulting capacitance will be greater than 500pF.

3.1.2 Low-Inductance Coupling Capacitor Solution

Not only could thin-film technology be used for bypass capacitors, but it could also be used for coupling capacitors or any general use capacitor, virtually eliminating the need for surface mount capacitors when LTCC is used as the PCB material. Various dielectrics could be used to tailor desired performance parameters based upon application or to achieve a certain capacitance per unit area [40]. A schematic of an in-line thin-film capacitor is shown in Figure 3.4. Thin-film processing techniques allow surface-applique capacitors to be constructed on appropriate substrates, although dielectric breakdown and yield issues must be considered [40]. The conformal-coating nature of the thin-film process ensures complete and uniform coverage of the metals and dielectrics ensuring high-quality, robust capacitors that would perform especially well in high-G environments where SMD components often fail. The ruggedness of this technology could be especially beneficial for defense and space exploration applications.

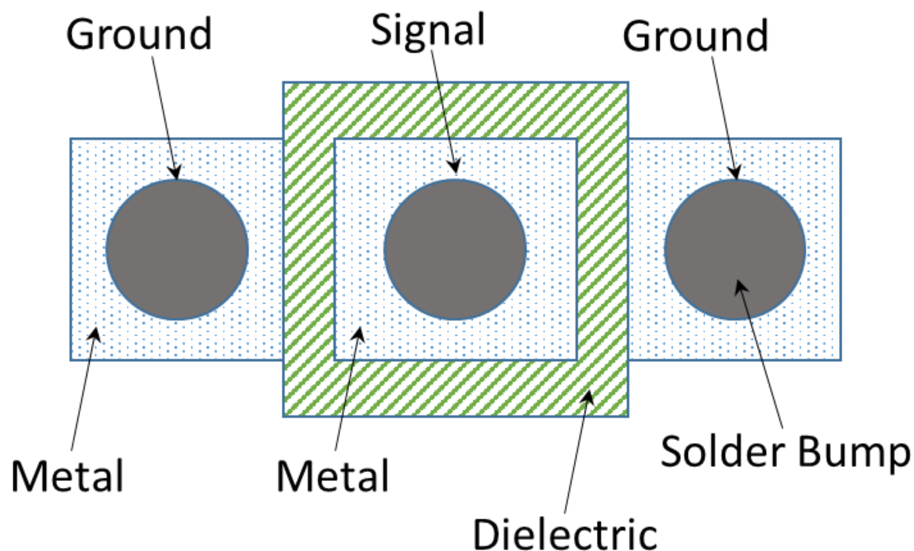

Figure 3.3 Surface deposited thin-film capacitor under solder bumps (top-view)

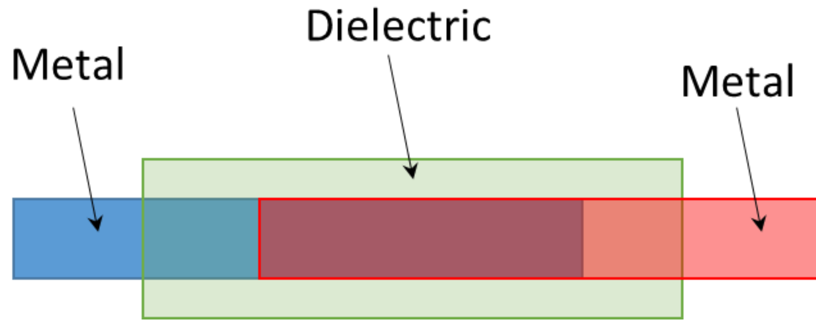

Figure 3.4 Schematic representation of thin-film coupling capacitor (top-view)

The following sections focus on capacitor fabrication and the RF performance achievable and the challenges involved in characterizing this unique low inductance technology.

3.2 Thin-film Capacitor Fabrication

The capacitors were constructed by Missouri Science and Technology University using layout geometries specified by Kansas State University. The fabricated capacitors are configured in a single layer metal-insulator-metal (MIM) design and constructed on DuPont 951 LTCC. The capacitors were sputter deposited through physical masks in three separate layers: a 500 nm thick bottom electrode, a 1000 nm thick Al2O3 dielectric layer, and a 500 nm thick top electrode. Sputter deposition was carried out at Missouri Science and Technology University with a Denton Discovery 18 system and electrode layers were deposited from 99.99% pure metallic targets at a power of 300 W using a DC power supply. The Al_2O_3 dielectric layer was deposited from a 99.9% pure ceramic target at a power of 200 W using an RF power supply. All depositions were carried out in an atmosphere of 99.999% pure Ar at a working pressure of 8 mTorr. No substrate heating was used during deposition. Figures 3.5 and 3.6 show examples of the panels and capacitors fabricated, including the three terminal ground-signal-ground probing structure.

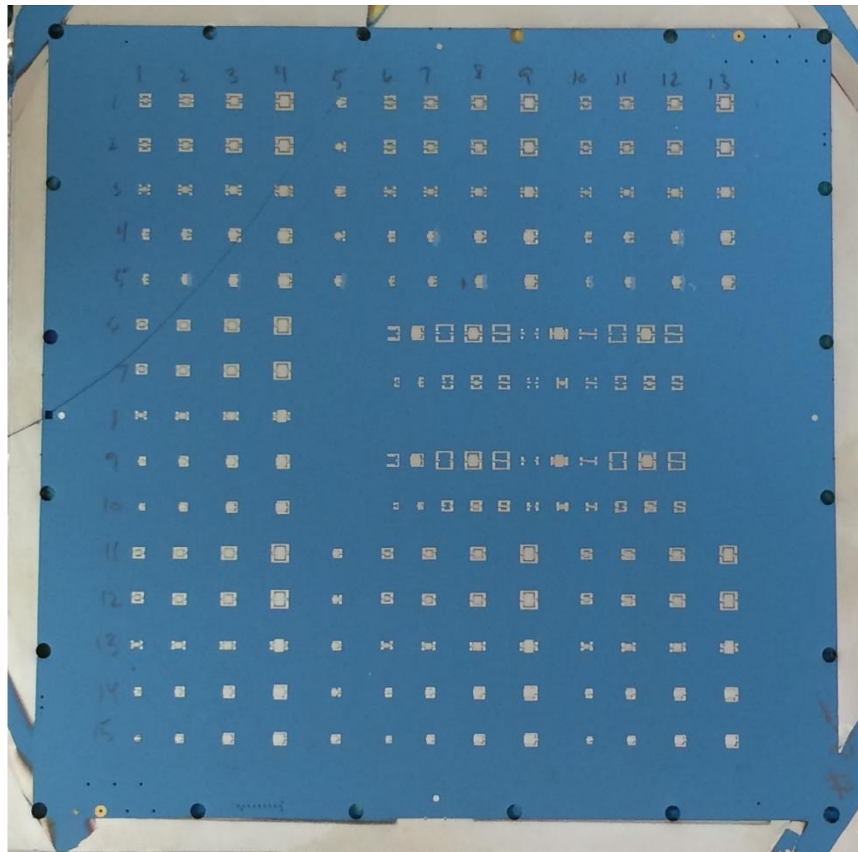

Figure 3.5 Thin-film capacitor test panel

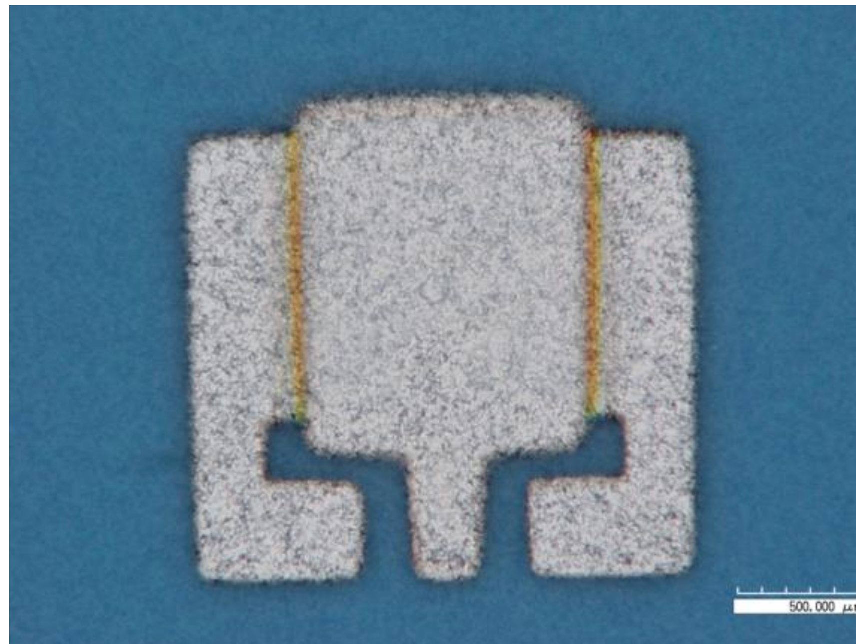

Figure 3.6 Thin-film MIM capacitor showing three-terminal probing structure (from [21])

3.3 Thin-film Capacitor Measured Results

3.3.1 Test Setup and Probing Location

Performance measurements were carried out at Kansas State University using an Agilent 8720ES VNA with a frequency span of 50 MHz to 20 GHz with 801 sample points. Probing of the capacitors was performed with 500 micron GGB Industries ground-signal-ground (GSG) coplanar probes. GSG probes were used to facilitate simple DUT probing and for their ability to produce more accurate results at GHz frequencies due to their inherently lower ground inductance, low fringing capacitances and ability to more tightly control the electromagnetic fields around the signal probe tip [29]. A standard one-port open-short-load (OSL) calibration was performed using a GGB CS-9 alumina calibration substrate to remove the systematic errors and losses within the VNA, its associated cabling, and the GSG probe. The test setup is shown in Figure 3.7. The probing locations of the thin film capacitors are shown in Figure 3.8.

Figure 3.7 Thin-film capacitor measurement setup

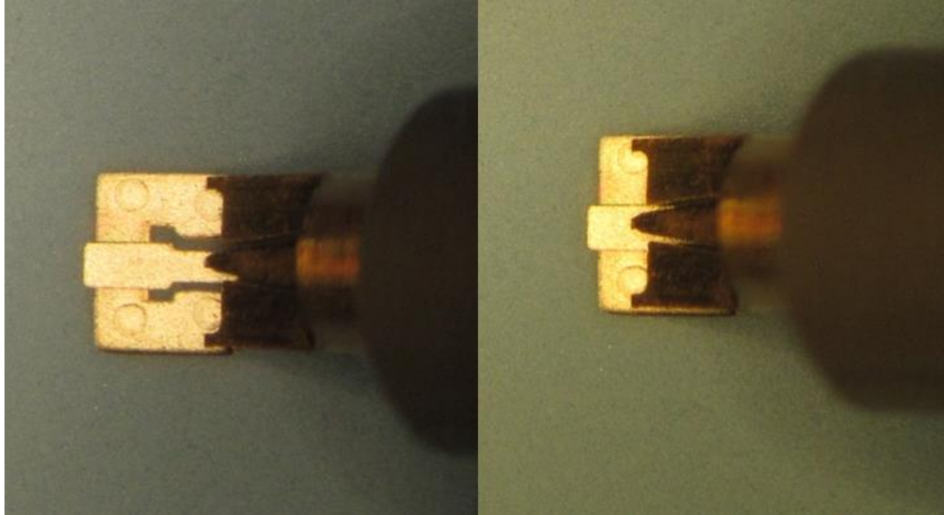

Figure 3.8 Probing locations

Initial measurements were taken at the terminals shown in the left image of Figure 3.8. Probing at this location suffers from inherent measurement error due to series lead-in inductance and associated resistive losses which must be accounted for with de-embedding structures. The series inductance dominates the impedance at higher frequencies and causes a low self-resonance frequency (SRF) as shown in the Smith chart of Figure 3.9. While this inductance can be de-embedded to an extent, the lead-in inductance is so large compared with the inductance of the thin-film capacitor that an alternative probing procedure needed to be considered. Greater effective series resistance (ESR) is also obtained when probing at this location which can also be seen in Figure 3.9 by the trace moving inward toward the center of the chart.

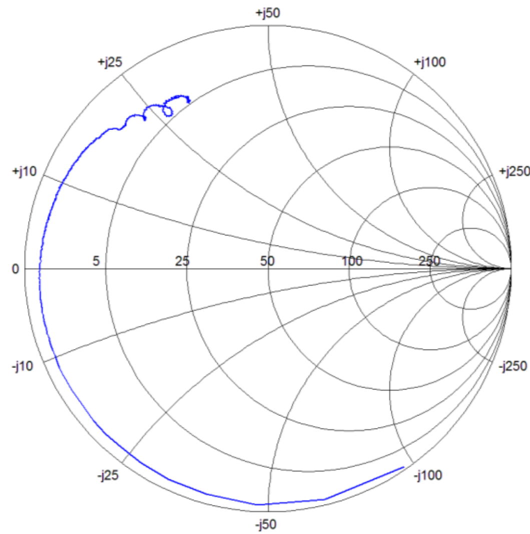

Figure 3.9 S_{11} results with lead in structures intact

The image on the right of Figure 3.8 shows the second probing location, and the measured results are shown in Figure 3.10. Initially this appeared to be a more valid probing location to represent the application of the capacitor in the flip-chip environment of Figure 3.2 and Figure 3.3. However, detailed investigation revealed that the folding back of the trace in Figure 3.10 was a result of the changing characteristic impedance of the probe due to the extra parasitic capacitance formed between the exposed metallic probe body and the top electrode of the capacitor extending beneath the probe [29]. Movement of the trace toward the center of the Smith chart above 10 GHz is a combination of substrate and radiation losses.

In order to maintain the characteristic impedance of the probing system, the lead-in structure was removed with a diamond scribe and the capacitor was probed on its edge. Figure 3.11 shows this modification in detail. Removal of metal below the GSG probe allows the characteristic impedance of the probe to remain constant to the calibration reference plane of the GSG probe tips. It can be seen in Figure 3.12 that the removal of the metal under the probe produces expected results showing nearly ideal capacitor behavior. With the measurement setup reporting valid results, attention can be turned to characterizing capacitor performance from S-parameter measurements.

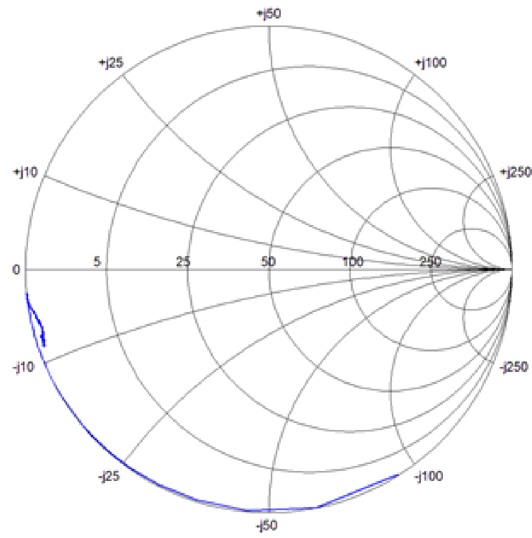

Figure 3.10 S_{11} when probing the middle of the capacitor with the lead-in structures intact

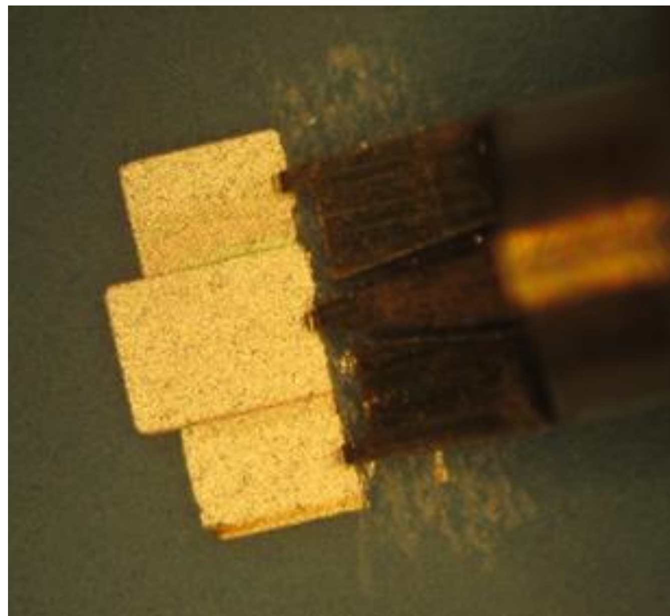

Figure 3.11 Lead-in removal and probing location

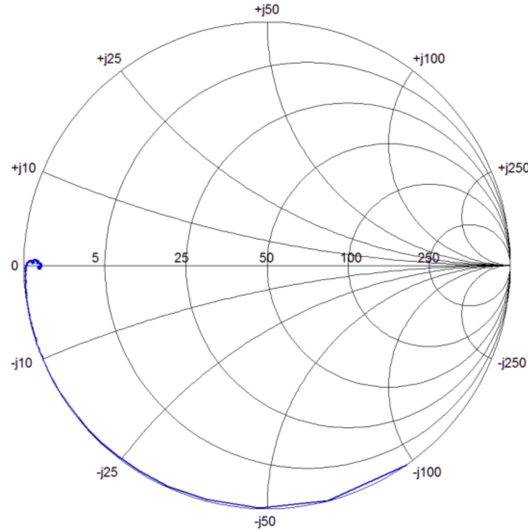

Figure 3.12 S11 with lead-in structure removed

3.3.2 Extracting Capacitor Parameters from S-parameter Measurements

With probing issues addressed the capacitors were characterized in terms of their resistive and reactive components. These parameters can be extracted from the measured S_{11} values and the corresponding impedance value. Background motivation on extracting capacitor parameters from S_{11} data can be found in Appendix A. Solving for the load impedance, Z_L from the measured S_{11} data, the following is obtained,

$$Z_L = Z_0 \frac{1+S_{11}}{1-S_{11}}, \tag{3.1}$$

and allows for the components of the load impedance to be found if the characteristic impedance of the transmission line is known along with the complex reflection coefficient. This is precisely the information a VNA measures, so if equation (3.1) can be manipulated further, then finding the impedance components of interest will be possible.

Recognizing that S_{11} data is complex and that the characteristic impedance of lossless transmission line is a purely real quantity, then equation (3.1) can be rewritten as

$$Z_L = R + jX = Z_0 \left[\frac{1+(\alpha+j\beta)}{1-(\alpha+j\beta)}\right], \tag{3.2}$$

where α and β are the real and imaginary components of the measured S_{11} data. Simplifying and solving equation (3.2) for the real and imaginary components will give the resistance and reactance of the device-under-test (DUT) as

$$\mathcal{R}\{Z_L\} = R = Z_0 \left[\frac{1-\alpha^2-\beta^2}{(\alpha-1)^2+\beta^2}\right] \tag{3.3}$$

$$\mathcal{I}\{Z_L\} = X = Z_0 \left[\frac{2\beta}{(\alpha-1)^2+\beta^2}\right]. \tag{3.4}$$

In the case of a capacitor, equation (3.3) can be viewed as its effective series resistance (ESR) and equation (3.4) can be inserted into equation (3.5) below and manipulated to extract the capacitance of the DUT.

$$X_C = \frac{1}{2\pi f C} \tag{3.5}$$

$$C = \frac{1}{2\pi f Z_0 \left[\frac{2\beta}{(\alpha-1)^2+\beta^2}\right]} \tag{3.6}$$

Therefore, by using a VNA, which sweeps across a specified frequency range and measures S_{11} data at each point in the sweep, the ESR and capacitance can be extracted.

3.3.3 Measured Results

A thin film capacitor with a plate size of 20x20 mil was measured with the setup shown and described in section 3.3.1. The result shown in Figure 3.13 confirms that a low-impedance bypass solution is obtainable with the proposed thin-film capacitors. The impedance drops rapidly through 4 GHz as expected and is a minimum near 8 GHz at the self-resonant frequency. The increase in impedance past 8 GHz is mainly due to ESR which can be seen in Figure 3.15.

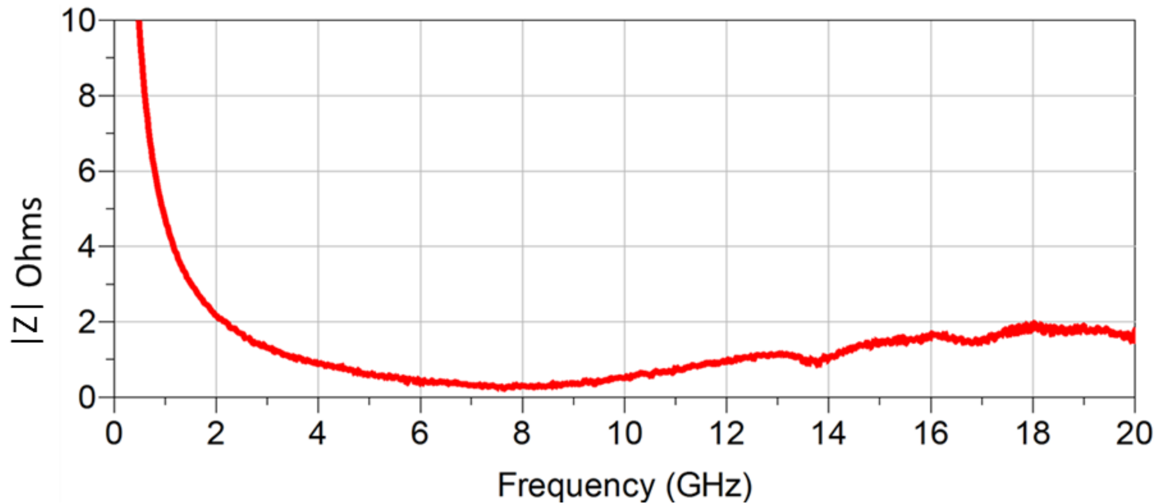

Figure 3.13 Impedance magnitude vs. frequency of 20x20mil thin film capacitor

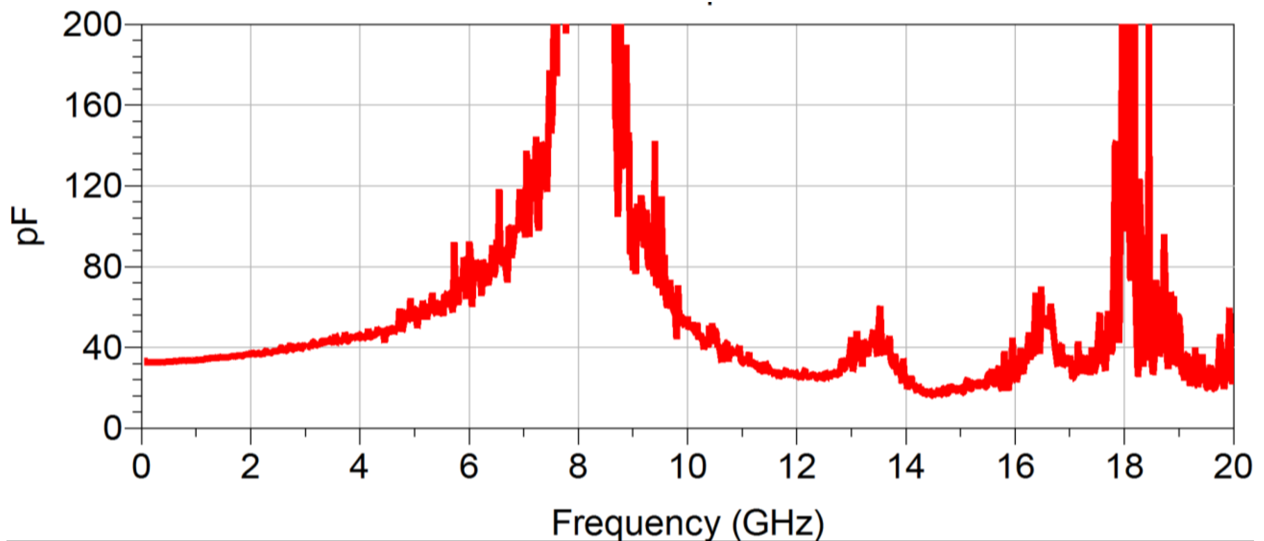

Figure 3.14 Capacitance vs. frequency for 20x20mil thin film capacitor

The measured capacitance of the thin film capacitor is shown in Figure 3.14. The capacitance remains fairly constant through 4 GHz before parasitic inductance causes a self-resonance characterized by the rapid rise occurring near 8 GHz. However, for many digital baseband and PCB decoupling applications, this provides a more than adequate bypass solution especially since the impedance of the capacitor remains relatively low through 20 GHz.

Figure 3.15 shows the extracted ESR of the thin-film capacitor is quite good through 10 GHz before it starts to increase due to dielectric losses within the capacitor itself and resistive losses in the electrodes due to the skin effect.

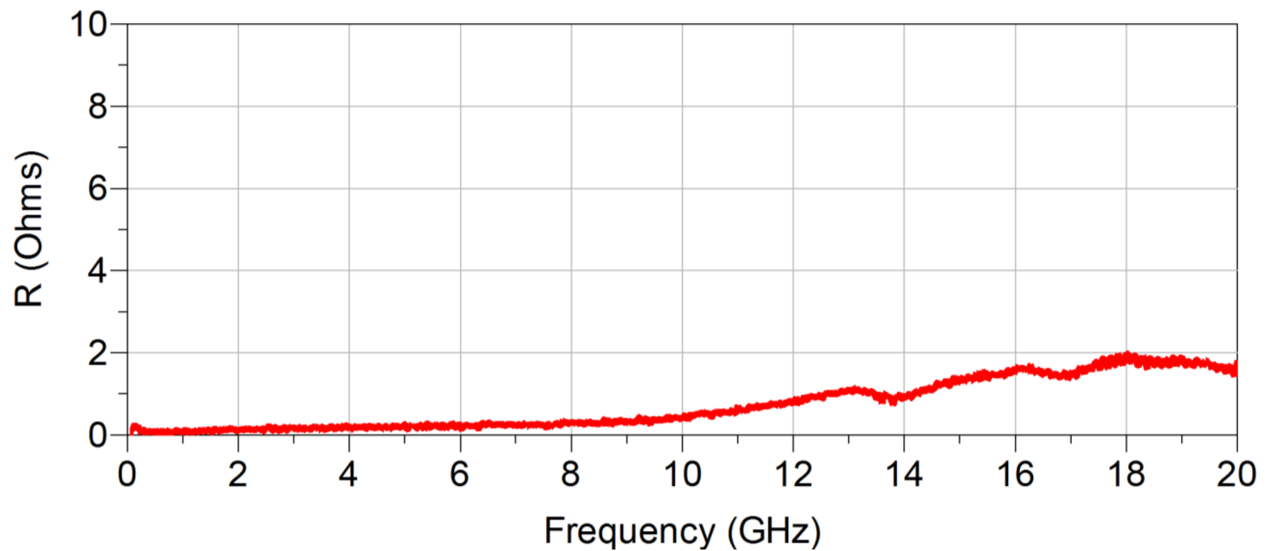

Figure 3.15 Resistance (ESR) vs. frequency for 20x20mil thin film capacitor

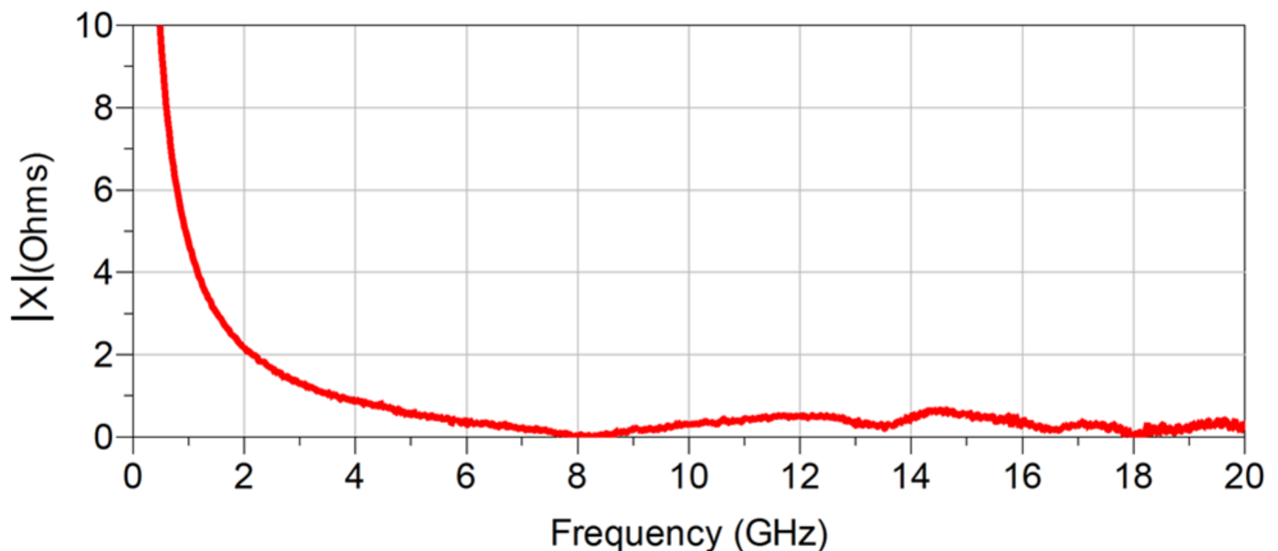

Figure 3.16 Reactance magnitude vs. frequency for 20x20mil thin film capacitor

Figure 3.16 shows the measured reactance of the capacitor under test. It is quite high at frequencies below 1 GHz which is expected due to its relatively low 35 pF value and remains quite low beyond 5 GHz. By plotting the resistance and reactance, the conclusion can be made that the slight increase in impedance above 8 GHz is mainly due to the ESR of the capacitor and not parasitic inductance. This may not necessarily be a bad characteristic as it can serve as a de-Q'ing mechanism to flatten the response of the decoupling network but can also cause undesired

losses in high frequency applications. Different electrode metals and dielectric materials could also be explored to develop capacitors that exhibit higher Q values for use in resonator circuits or to minimize power loss in millimeter wave applications.

3.3.4 Comparison with Traditional Ceramic SMD Capacitors

To verify the performance enhancements of thin film capacitors relative to a SMD device, an industry standard 18 pF, 0805 ceramic capacitor was measured on an FR-4 PCB as shown in Figure 3.17. The layout in Figure 3.17 should be considered optimal if one disregards the probing structure required by the 500 µm GSG probe. The large copper traces and lack of vias (no ground plane available) minimize inductive effects. The narrow center lead-in likely adds a small amount of series inductance and resistance but is actually quite similar to a typical bypass layout required by modern IC packages. The extra ground leg at the top of the image adds a small amount of parasitic capacitance pushing the first SRF to a slightly lower frequency and causing other resonances in the measurement frequency band. Nevertheless, the layout will still serve as a good comparison between the proposed thin-film capacitors and traditional ceramic capacitors.

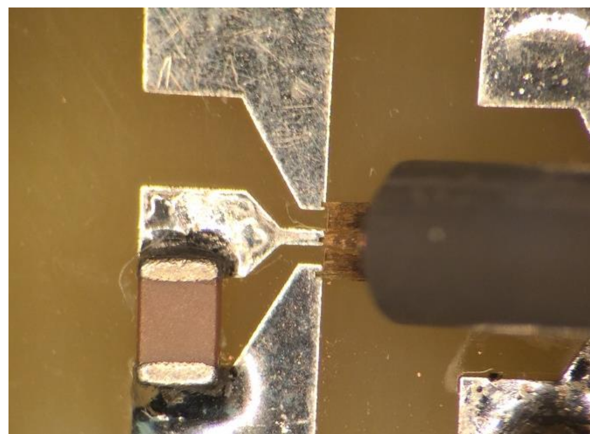

Figure 3.17 Image of ceramic capacitor used for performance comparison

The 50Ω Smith chart in Figure 3.18 shows the ceramic capacitor behaves as such through 800 MHz where it then passes through a series self-resonance. Beyond 800 MHz, the impedance rises sharply with frequency as the parasitic ESR and reactance of the device dominate the impedance which peaks at the first parallel resonant frequency near 5 GHz as shown in Figures

3.18, 3.19 and 3.20. At this point, the capacitor is essentially an inductor and is useless in bypass situations.

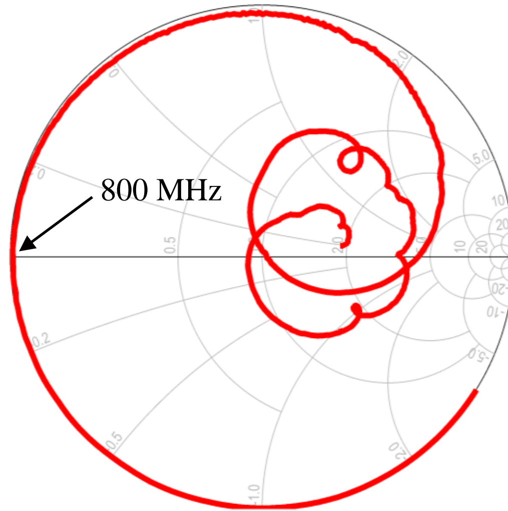

Figure 3.18 Smith chart of ceramic capacitor showing the series SRF and parasitic inductance and ESR effects

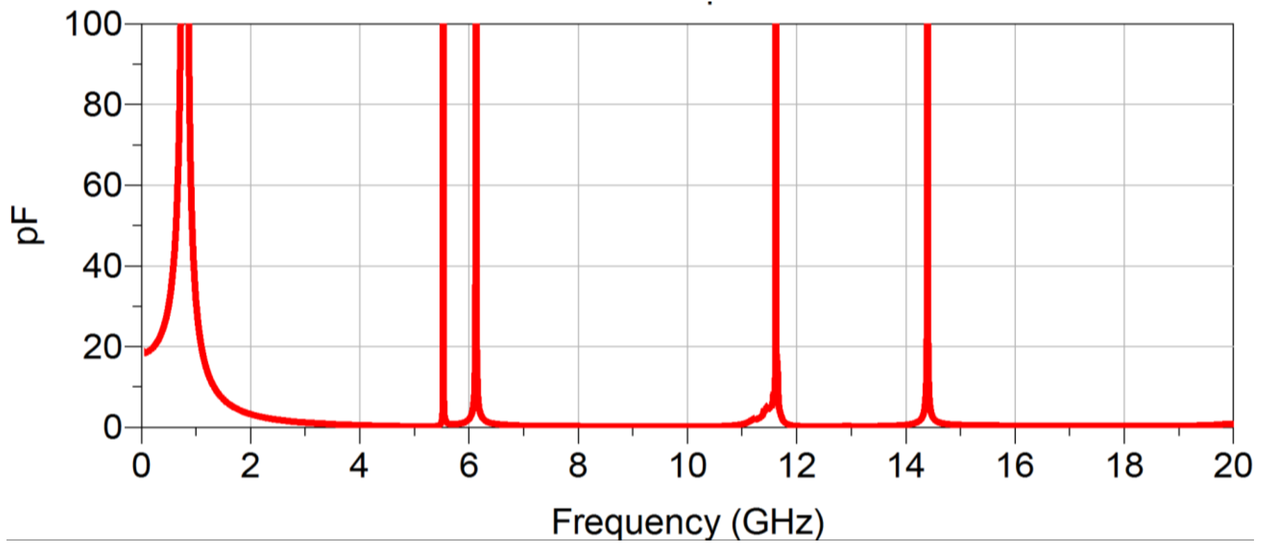

Figure 3.19 Capacitance vs. frequency of 18pF, 0805 ceramic capacitor

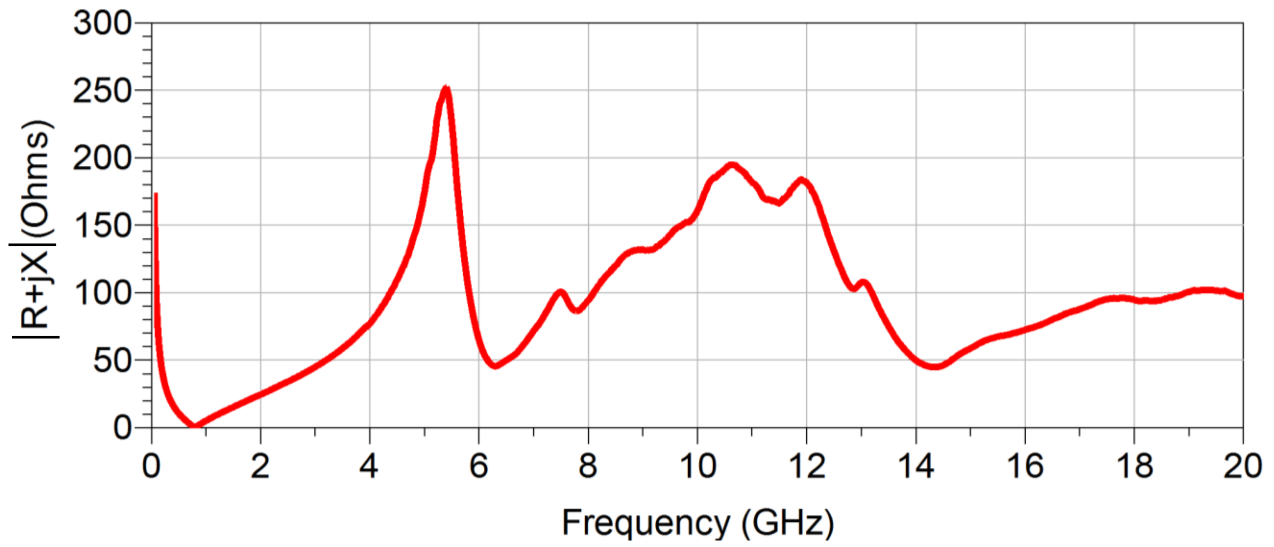

Figure 3.20 Impedance magnitude vs. frequency of 0805 ceramic capacitor

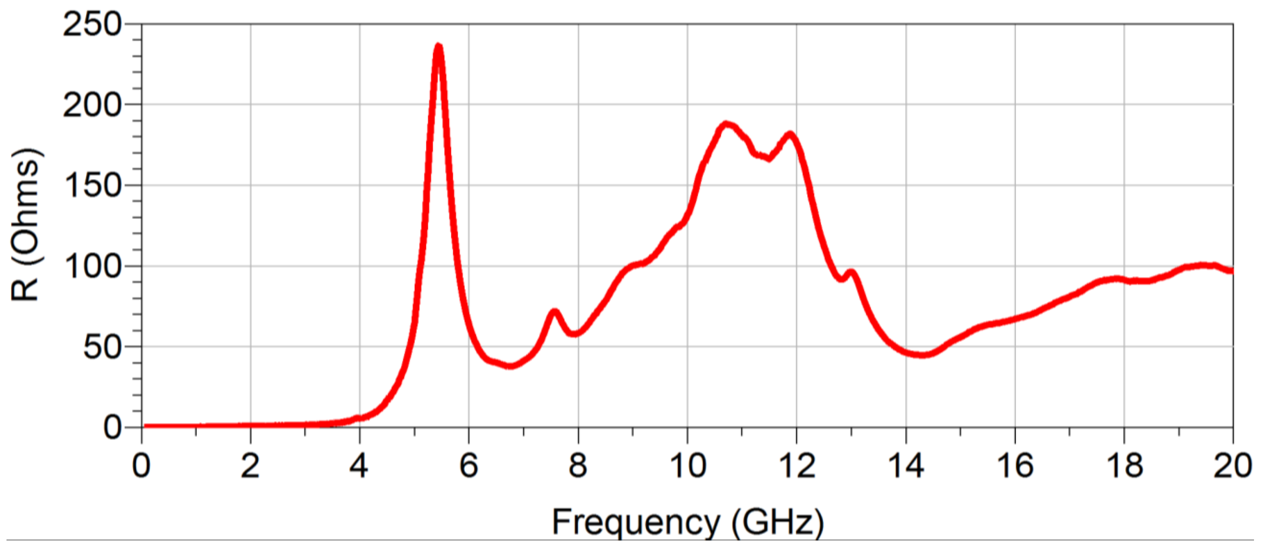

Figure 3.21 ESR vs. frequency of 18pf, 0805 ceramic capacitor

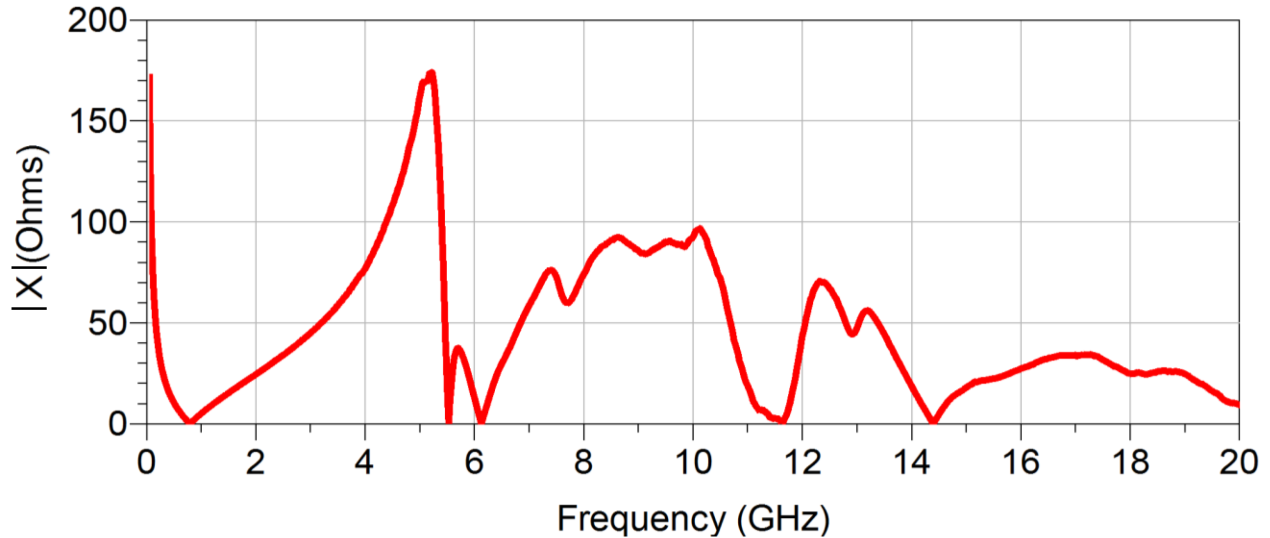

Figure 3.22 Reactance magnitude vs. frequency of 18pF, 0805 ceramic capacitor

Comparing the reactance of the conventional SMD capacitor in Figure 3.22 to the reactance of the thin-film capacitor in Figure 3.16 we see that the latter provides bypass performance improvements with a reactive impedance that is up to 100 times smaller. Compared to traditional surface mount capacitors, while not a complete broadband solution, thin film caps propose a very good local bypass for many board level decoupling needs and could limit the use of the more traditional paralleling capacitor method [41] saving both bill of material cost and layout space.

Chapter 4 - Conclusions

The goals of this research included understanding the basic history of RF/microwave substrates and investigating improved methods for transmission line construction on LTCC. Specifically we have focused on investigating how a lossy adhesion layer metal in a thin-film microstrip transmission line influences microwave power losses, how power loss is impacted when the thickness of Cu is decreased to achieve better line and space resolutions, and what applications might benefit from a new bypass and coupling capacitor topology using thin-film construction techniques.

4.1 Thin-film Microstrip on LTCC

Concerns and conflicting information found in the literature over the addition of a lossy-adhesion layer for mechanical robustness in the construction of transmission lines on LTCC was addressed. It was found that the addition of titanium at the substrate-to-metal interface in microstrip lines had minimal effect on signal losses through 40 GHz and could be included in a thin-film stack-up without worry. It should be noted that in order to minimize power losses, the adhesion layer metal should be much thinner than its skin depth at the maximum frequency of operation. This ensures the least amount of longitudinal E-field attenuation in the adhesion layer which maximizes current density in the more conductive layers above.

4.2 Effects of Thinning the Main Cu Layer

Worries over increased signal losses due to the thinning of the main conducting layer in a thin-film microstrip in favor of improved interconnect line-space resolution was investigated. A standard thin-film recipe with a Cu layer thickness of 4 µm was used as the reference for this work. LTCC panels with thin-film microstrip structures were fabricated using Cu thicknesses of 4, 2, 1 and 0.4 µm respectively while all other metal thicknesses within the stack-up were held constant (except in the extreme case of 0.4 µm). Measured results show that power losses from 6 through 40 GHz are essentially identical between the 4, 2 and 1 µm cases, which can be attributed to the skin effect limiting the penetration depth of the E-field into the main Cu layer. Thus one can safely remove considerable thickness from the Cu layer of the original recipe in favor of better line-space resolution. However, if the metal thicknesses are pushed to extreme

levels where finished metal thicknesses are in the sub-micron range, substrate surface roughness along with manufacturing defects can significantly degrade signal integrity.

4.3 Thin-film Capacitors on LTCC

A simple thin-film capacitor topology was investigated. Metal-insulator-metal capacitors were fabricated on LTCC panels and various parameters were characterized through 20 GHz. After initial investigations revealed the proper probing technique, it was found that the thin-film capacitors can perform quite well through at least 20 GHz in bypass scenarios. This can be explained through the proposed ground-signal-ground topology that keeps parasitic inductance to a minimum, which in turn acts to keep the impedance of the capacitor small. These capacitors would be ideally suited to a flip-chip environment where connections to the IC would be kept very short, minimizing inductance and creating a relatively broadband bypass solution.

4.4 Future Directions

Future work in the area of thin-film capacitors in particular shows promise. At the time of this writing, the capacitors were fabricated using an alumina dielectric which translates to a relatively small capacitance per unit-area. Applying such thin-film capacitors using small dielectric constants is possible; however, due to the dimensions needed to achieve the desired capacitance values, one needs to explore the transmission line properties of the resulting structure [38]. Experiments with higher Dk materials should be done to check the viability of creating large value capacitors suitable for use at lower frequencies and as "charge reservoirs" for heavy load scenarios. Developing thin-film processes for other PCB material types would also prove to be beneficial as it would allow the use of this technology in lower-cost scenarios and perhaps increase reliability and decrease bill of material cost and fabrication time. Ultimately, the ability to develop an electronic system without use of passive SMD components though a combination of thick and thin-film techniques is a worthy end goal, but simultaneously achieving higher performance will bring the most important benefits.

References

[1] J. Coonrod, “Ambiguous Influences Affecting Insertion Loss of Microwave Printed Circuit Boards [Application Notes],” *IEEE Microw. Mag.*, vol. 13, no. 5, pp. 66–75, Jul. 2012.

[2] J. Coonrod, “Understanding the variables of dielectric constant for PCB materials used at microwave frequencies,” in *Microwave Conference (EuMC), 2011 41st European*, 2011, pp. 938–944.

[3] J. Coonrod, “Circuit Materials and High-Frequency Losses,” *The PCB Magazine*, pp. 24–29, Feb-2012.

[4] J. Coonrod, “Understanding PCBs for High-Frequency Applications,” *Printed Circuit Design & Fab*, pp. 25–28, Oct-2011.

[5] A. Aguayo, “Advances in High-Frequency PCB Materials,” *Defense Tech Briefs*, vol. 4, no. 5, pp. 4–7, Oct-2010.

[6] I. Poole, “PCB Manufacturing Process.” [Online]. Available: http://www.radio-electronics.com/info/manufacture/manufacture/pcb/pcb-manufacturing-process.php. [Accessed: 30-Jan-2015].

[7] M. Tarr, “Basic Board Materials.” [Online]. Available: http://www.ami.ac.uk/courses/topics/0232_bbm/. [Accessed: 20-Feb-2014].

[8] J. Browne, “Picking Materials For Multilayer PCBs | Materials content from Microwaves & RF.” [Online]. Available: http://mwrf.com/materials/picking-materials-multilayer-pcbs. [Accessed: 20-Feb-2014].

[9] “Ceramic capacitor,” *Wikipedia, the free encyclopedia*. 01-Aug-2014.

[10] R. Sturdivant, “Millimeter-Wave Performance of Alumina High Temperature Cofired Ceramics IC Packages,” in *IMAPS*, San Diego, California, USA.

[11] “High and Low Temperature Cofired Multilayer Ceramics (HTCC and LTCC).” [Online]. Available: http://www.us.schott.com/epackaging/english/download/schott-htcc-ltcc-datasheet-2013-08-us.pdf.

[12] J.-P. Bertinet, E. Leleux, J.-P. Cazenave, J.-P. Ganne, M. Pate, and R. Lebourgeois, “Filtering Capacitors Embedded in LTCC Substrates for RF and Microwave Applications,” Nov-2007. [Online]. Available: http://www.microwavejournal.com/articles/print/5610-filtering-capacitors-embedded-in-ltcc-substrates-for-rf-and-microwave-applications. [Accessed: 20-Feb-2014].

[13] R. Trine, “Multilayer lamination methods for PTFE Based PCBs.” [Online]. Available: http://www.taconic-add.com/pdf/technicalarticles--multilayer_lamination_methods.pdf. [Accessed: 20-Feb-2014].

[14] “TMM® Laminates.” [Online]. Available: http://www.rogerscorp.com/acm/producttypes/8/TMM-Laminates.aspx. [Accessed: 17-Feb-2014].

[15] M. Huschka, “The Use of PTFE/Woven Glass Base Material in the PCB Industry,” 1998. [Online]. Available: http://www.taconic-add.com/pdf/technicalarticles--theuseofptfebasematerials.pdf.

[16] J. Coonrod, “Benefits of Mixed Dielectrics When Used for High-Frequency PCB Applications,” *High Frequency Electronics*, pp. 28–36, Nov-2012.

[17] S. Hildebrandt and K.-J. Wolter, “Thin film structuring on LTCC,” in *Electronics Technology, 2008. ISSE’08. 31st International Spring Seminar on*, 2008, pp. 526–530.

[18] J. Muller, R. Perrone, H. Thust, K.-H. Drue, C. Kutscher, R. Stephan, J. Trabert, M. Hein, D. Schwanke, and J. Pohlner, "Technology benchmarking of high resolution structures on LTCC for microwave circuits," in *Electronics Systemintegration Technology Conference, 2006. 1st*, 2006, vol. 1, pp. 111–117.
[19] H. Sobol, "Applications of integrated circuit technology to microwave frequencies," *Proc. IEEE*, vol. 59, no. 8, pp. 1200–1211, Aug. 1971.
[20] "1GG5-8045 110 GHz Double Balanced Mixer | Keysight (formerly Agilent Test and Measurement)." [Online]. Available: http://www.keysight.com/en/pd-1748561-pn-1GG5-8045/110-ghz-double-balanced-mixer?cc=US&lc=eng. [Accessed: 20-Aug-2014].
[21] J. A. Wolf and K. A. Peterson, "Thin Film on LTCC for Connectivity and Conductivity.," *J. Microelectron. Electron. Packag.*, vol. 8, no. 2, pp. 43–48, 2011.
[22] R. Faraji-Dana and Y. L. Chow, "The current distribution and AC resistance of a microstrip structure," *Microw. Theory Tech. IEEE Trans. On*, vol. 38, no. 9, pp. 1268–1277, 1990.
[23] E. J. Denlinger, "Losses of microstrip lines," *Microw. Theory Tech. IEEE Trans. On*, vol. 28, no. 6, pp. 513–522, 1980.
[24] Y.-H. Kim, "Adhesion of titanium thin film to oxide substrates," *J. Vac. Sci. Technol. Vac. Surf. Films*, vol. 5, no. 5, p. 2890, Sep. 1987.
[25] K. R. Williams and R. S. Muller, "Etch rates for micromachining processing," *Microelectromechanical Syst. J. Of*, vol. 5, no. 4, pp. 256–269, 1996.
[26] R. A. Pucel, D. J. Masse, and C. P. Hartwig, "Losses in microstrip," *Microw. Theory Tech. IEEE Trans. On*, vol. 16, no. 6, pp. 342–350, 1968.
[27] Xin Wu, D. Cullen, G. Brist, and O. M. Ramahi, "Surface Finish Effects on High-Speed Signal Degradation," *IEEE Trans. Adv. Packag.*, vol. 31, no. 1, pp. 182–189, Feb. 2008.
[28] E. Bogatin, *Signal integrity-- simplified*. Upper Saddle River, NJ: Prentice Hall, 2004.
[29] S. A. Wartenberg, *RF measurements of die and packages*. Boston: Artech House, 2002.
[30] B. Thrasher, D. Nair, J. Parisi, G. Oliver, and M. A. Smith, "Bulk and In-Circuit Dielectric Characterization of LTCC Tape Systems Through Millimeter Wave Frequency Range," presented at the IMAPS 2011, 2011.
[31] K. M. Nair, M. F. McCombs, K. E. Souders, J. M. Parisi, K.-I. Hang, D. M. Nair, and S. C. Beers, "Research Triangle Park, NC 27709," *Adv. Electroceramic Mater. II Ceram. Trans.*, vol. 106, p. 213, 2010.
[32] L. G. Maloratsky, "Reviewing the basics of microstrip," *Microw. RF*, vol. 39, pp. 79–88, 2000.
[33] T. Liang, S. Hall, H. Heck, and G. Brist, "A Practical Method for Modeling PCB Transmission Lines with Conductor Surface Roughness and Wideband Dielectric Properties," in *Microwave Symposium Digest, 2006. IEEE MTT-S International*, 2006, pp. 1780–1783.
[34] J. Müller and D. Josip, "Integrated capacitors using LTCC," *Proc. MicroTech2002 Manch. UK January*, 2002.
[35] I. Bord-Majek, P. Kertesz, J. Mazeau, D. Caban-Chastas, B. Levrier, L. Bechou, and Y. Ousten, "Operational Performances Demonstration of Polymer-Ceramic Embedded Capacitors for MMIC Applications," *Compon. Packag. Manuf. Technol. IEEE Trans. On*, vol. 1, no. 9, pp. 1473–1479, 2011.

[36] N. Kamehara, J. D. Baniecki, T. Shioga, K. Kurihara, and M. Mizukoshi, “Low inductance thin film capacitors for decoupling applications,” in *17th International Zurich Symposium on Electromagnetic Compatibility, 2006. EMC-Zurich 2006*, 2006, pp. 565–567.
[37] B. Dang, M. Shapiro, P. Andry, C. Tsang, E. Sprogis, S. Wright, M. Interrante, J. Griffith, V. Truong, L. Guerin, R. Liptak, D. Berger, and J. Knickerbocker, “Three-Dimensional Chip Stack With Integrated Decoupling Capacitors and Thru-Si Via Interconnects,” *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1461–1463, Dec. 2010.
[38] D. Iguchi and H. Umekawa, “A signal and power integrity oriented packaging for low cost and high performance systems,” in *2012 2nd IEEE CPMT Symposium Japan*, 2012, pp. 1–4.
[39] “Flip Chip Packaging Technology Solutions.” [Online]. Available: http://www.amkor.com/go/flip-chip-packaging. [Accessed: 03-Mar-2015].
[40] P. Jain and E. J. Rymaszewski, “Embedded thin film capacitors-theoretical limits,” *IEEE Trans. Adv. Packag.*, vol. 25, no. 3, pp. 454–458, Aug. 2002.
[41] T. Schmitz and M. Wong, “Choosing and Using Bypass Capacitors,” *Intersil Co*, 2011.
[42] T. H. Lee, *Planar microwave engineering: a practical guide to theory, measurement, and circuits*. Cambridge, [England] ; New York: Cambridge University Press, 2004.
[43] D. M. Pozar, *Microwave engineering*, 3rd ed. Hoboken, NJ: J. Wiley, 2005.

Appendix A - S-parameter Background

Capacitor performance information can be extracted from the scattering matrix measurements made by a network analyzer. The scattering or S-parameters are a network characterization technique popularized by Hewlett-Packard in the 1960's. It's especially useful at microwave frequencies since the technique only considers incident and reflected voltage waves on each respective port instead of trying to measure voltages and currents directly, which can be very difficult to perform at high frequencies due to non-zero length test fixtures perturbing the measurements [42].

The S-parameters captured by a VNA can be defined using a network like the one shown in Figure A.1. Since the S_{21} parameter is used extensively throughout this thesis, Figure A.1 has been modified from its conventional form [43] to assist the reader in understanding its definition. Specifically, the port 2 voltage directions are changed from the conventional directions to emphasize the flow of energy through the network. The matrix equation (A.1) mathematically defines the parameters for this 2-port network.

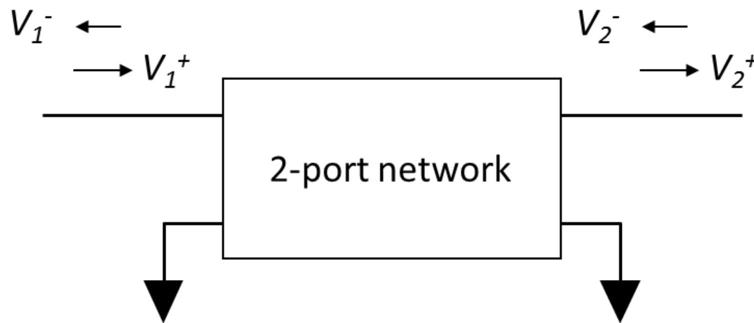

Figure A.1 2-port network with incident and reflected waves

$$\begin{bmatrix} V_1^- \\ V_2^+ \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^- \end{bmatrix} \tag{A.1}$$

This matrix yields the equations below that show how the incident and reflected waves are related.

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^- \quad (A.2)$$

$$V_2^+ = S_{21}V_1^+ + S_{22}V_2^- \quad (A.3)$$

The four S-parameters can be found by manipulating equations (A.2) and (A.3) along with the fact that a transmission line terminated in its characteristic impedance, Z_0 will not produce any reflected waves, resulting in the following relationships:

$$S_{11} = input\ port\ reflection = \frac{V_1^-}{V_1^+}\ while\ V_2^- = 0 \quad (A.4)$$

$$S_{12} = reverse\ gain = \frac{V_1^-}{V_2^-}\ while\ V_1^+ = 0 \quad (A.5)$$

$$S_{21} = forward\ gain = \frac{V_2^+}{V_1^+}\ while\ V_2^- = 0 \quad (A.6)$$

$$S_{22} = output\ port\ reflection = \frac{V_2^+}{V_2^-}\ while\ V_1^+ = 0 \quad (A.7)$$

As noted above, the S_{11} and S_{22} terms are equivalent to the voltage reflection coefficients at their respective ports and describe how much of an incident wave is reflected by an impedance discontinuity in the transmission line. Thus the port reflections can be defined in terms of their respective complex reflection coefficients. Equation (A.8) defines S_{11} in terms of this reflection coefficient:

$$S_{11} = |\Gamma|e^{j\phi} \quad (A.8)$$

where $|\Gamma|$ is the magnitude of the reflection coefficient and $e^{j\phi}$ provides its phase angle in gamma space. It is equation A.8 that allows impedance i.e., resistance and reactance to be extracted from VNA measurements.

In order to extract impedance from S_{11}, one must turn to transmission line theory, specifically the case of a terminated lossless transmission line. Figure A.2 shows an arbitrary lossless transmission line terminated in a load impedance Z_L which could be the input impedance of port 1 of Figure A.1. In this case, port 1 is at the coordinate x=0 and is being fed with a signal carried in from a transmission line

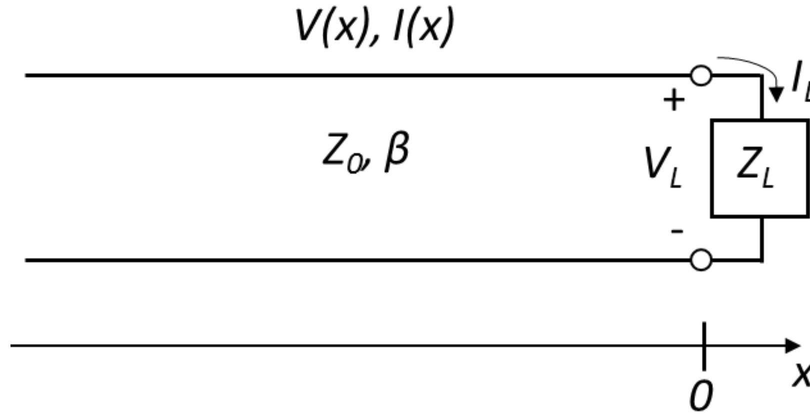

Figure A.2 Lossless transmission line terminated in a load impedance Z_L (figure after [43])

If it is assumed that a generator produces an incident voltage wave at some location x < 0, then $V^+(x)$ can be described by $V_o^+ e^{-j\beta x}$. If the transmission line is infinitely long, then one can use its characteristic impedance to find the voltage-to-current ratio for this incident wave. However, for a finite length of line, if the load impedance is not matched to the characteristic impedance, that is $Z_L \neq Z_0$, the current-to-voltage relationship must still equal Z_L at x = 0. Therefore, a reflected wave of appropriate amplitude will be produced to satisfy this ratio, which leads to the total voltage on the line being the sum of the incident and a reflected wave:

$$V(x) = V_o^+ e^{-j\beta x} + V_o^- e^{j\beta x} \tag{A.9}$$

where V_o^+, V_o^- are the phasor amplitudes of the incident and reflected voltage waves, and the complex exponentials $e^{\pm j\beta x}$ model the phase changes with x. Similarly, the current on the line can be written as,

$$I(x) = \frac{V_o^+}{Z_0} e^{-j\beta x} - \frac{V_o^-}{Z_0} e^{j\beta x}. \tag{A.10}$$

Note the minus sign being used to represent the reflected current wave since it travels in the opposite direction of the specified reference direction assumed for the total current into the load. According to Ohm's law, the total voltage and current at the load $x = 0$, are related through the load impedance Z_L, as

$$Z_L = \frac{V(0)}{I(0)} = \frac{V_o^+ + V_o^-}{V_o^+ - V_o^-} Z_0. \tag{A.11}$$

Solving for V_o^- gives the magnitude of the reflected wave as

$$V_o^- = \frac{Z_L - Z_0}{Z_L + Z_0} V_o^+. \tag{A.12}$$

Equation (A.13) shows that the ratio of the reflected wave to the incident wave is equivalent to the reflection coefficient found in (A.8) and the S_{11} parameter in (A.4) when port 2 is properly terminated,

$$S_{11} = \frac{V_o^-}{V_o^+} = \Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{A.13}$$

Now with (A.13), one can begin the process of extracting the capacitance and ESR from measured S_{11} results.