FABRICATION OF AN EXPERIMENTAL N-CHANNEL INSULATED-GATE FIELD EFFECT TRANSISTOR

by

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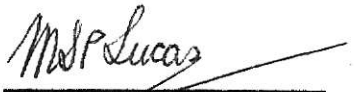

Major Professor

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CHAPTER 1

INTRODUCTION

The choice of fabricating an enhancement type insulated-gate field effect transistor rather than another type of field effect or bipolar transistor or diode was made in order to get the best possible device with the least possible effort. The effort required to fabricate an enhancement type IGFET was comparatively small because the source and drain diffusions were made simultaneously and no other diffusions were needed since a doped rather than an intrinsic wafer of silicon was used. The procedures necessary to successfully fabricate such a device are recorded in sufficient detail within this thesis that one wishing to duplicate this work could do so without trauma or undue mental strain. Improvement upon the transistor in question, should anyone accept the challenge, would be a long, arduous task because of the number of variable parameters involved, such as gate oxide thickness, the amount of charge trapped in the gate oxide, device geometry, surface preparation, diffusion profile and channel type.

The original device geometry was annular but after consultations with engineers at the Motorola semiconductor plant, Mesa, Arizona, semi-circular geometry was decided upon because it allowed half the transistor chip to be reserved for bonding pads. In the annular configuration it was difficult to provide for a drain bonding pad with the required minimum pad diameter of 5 mils (1 mil = 1/1000 inch) and at the same time allow for a source bonding pad of the same minimum diameter. The final dimensions are specified in Appendix 1. Once these dimensions were determined, the diffusion, ohmic contact, metalization and passivation patterns were prepared with rubylith, using conventional techniques, 500 times (linearly) final size. These patterns were sent to Motorola in Mesa, Arizona, where a set of four masks was prepared by

reducing the rubylith artwork 500 times and then, by step and repeat photography, a 100 X 100 matrix of said reduced patterns was produced with a center-to-center spacing between patterns of 20 mils on a $2\frac{1}{2}$ inch x $2\frac{1}{2}$ inch by 1/16 inch high resolution glass photographic plate. These masks were then used in the field effect transistor fabrication in the semiconductor lab, department of electrical engineering at Kansas State University. Appendix 2 discusses these masks in more detail.

The silicon wafers were purchased from Chisso Corp., Tokyo, Japan, for $1.40 each. A complete list of the mechanical and electrical properties of the wafers is given in Appendix 3.

Several visits were made to the Western Electric semiconductor plant, Lee's Summit, Missouri, to observe methods used in manufacturing active devices and to ask on-line supervisors questions which had arisen during the preparation for making IGFET's at KSU. Particular attention was paid to wafer cleaning as this process is necessary in all types of solid state device fabrication. Western Electric's cleaning practice was followed as closely as our equipment allowed because it had been proven by years of experience to be adequate for bipolar device production and therefore provided a good starting point for IGFET fabrication. This cleaning sequence is recorded in Appendix 4. Some of the supervisors at Western Electric explained that their cleaning schedule had been arrived at empirically and felt that one should not hesitate to make changes, particularly on such a small scale production. There are times, however, when one must not argue with success.

Appendix 5 contains a list of the equipment and materials used in the IGFET fabrication processes and includes a list of additional items that could have been used.

The most difficult phase of this research and definitely the most time

consuming was in researching books and journals and the subsequent organizing of the equipment to be used which took almost a full year. The actual fabrication process took four working days to complete the first wafer of transistors, which were all defective, four days for the second wafer which also contained no working devices and only one day for the third and successful attempt. Processing time per wafer could have been reduced by cleaning several wafers simultaneously, but this could also have been an easy way to ruin several wafers concurrently.

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CHAPTER 2

FROM FANCY TO FACT - A HISTORY

A complete historical review of the field effect transistor would have to go back at least to 1925 and perhaps even further. A series of three patents was issued to Julius Edgar Lilienfeld, professor of physics at the University of Leipzig, by the U. S. Patent Office for three devices which described in great detail methods for controlling or amplifying electric currents [1], [2], [3]. All three of these devices as proposed by Lilienfeld worked on the principle of modulating a current in a thin film with an electric field.

Figure 1 is a cross section view of Lilienfeld's first device, [1]. According to the inventor, two electrodes (2 and 3) of platinum, gold, silver or copper were to be deposited on a glass slide (1) which was first to be fractured along a line parallel to the two electrodes and an aluminum foil (5) placed in the fracture and trimmed flush with the top surface of the slide. A very thin film of copper sulfide (4) deposited over the top of the device, including the two electrodes and aluminum foil, formed an ohmic contact with the electrodes and a rectifying contact with the aluminum foil.

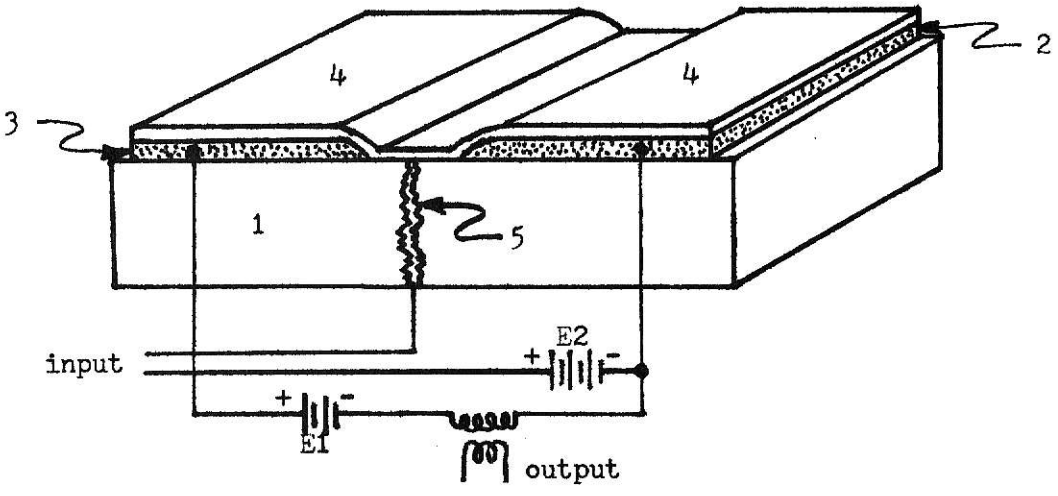

Fig. 1. Cross section view of Lilienfeld's first device.

In the inventor's own words, "The thickness of the (copper sulfide) film, moreover, is minute and of such a degree that the electrical conductivity therethru would be influenced by applying thereto an electrostatic force (at the copper sulfide-aluminum junction)." Potential E1 provides for current flow through the film from one electrode to the other and E2 is a bias potential which sets the operating point of the modulating input signal. As if to conceive such a device were not enough, Lilienfeld included in the patent a complete schematic diagram for a tuned r. f. receiver using four of his amplifying devices and no vacuum tubes.

Figure 2 is a cross section view of Lilienfeld's second device, [2]. The fabrication of this device started with a metal base (1) such as aluminum, magnesium, tantalum or tungsten upon which an insulating oxide (5) could easily be formed. A highly conductive film of metal (4) such as copper, lead or aluminum was then to be deposited upon the oxide. Further depositions of metallic conductors (2 and 3) were for contact to the outside world. It was due to the thinness of the conducting film along the vertex of the triangular notch (6) that "enables one to subject a conducting layer of extreme thinness

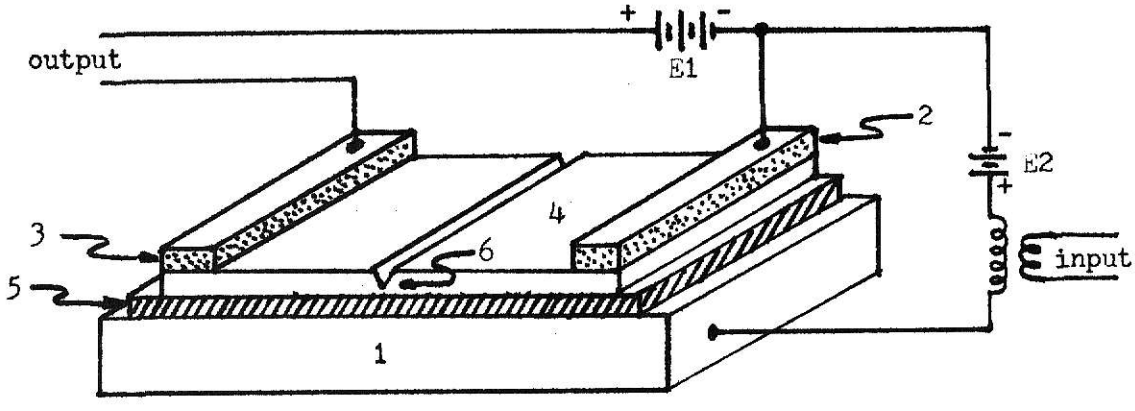

Fig. 2. Cross section view of Lilienfeld's second device.

(approaching molecular thickness) throughout its full volume to a very strong electrostatic field, for example in the provision of an amplifier device."

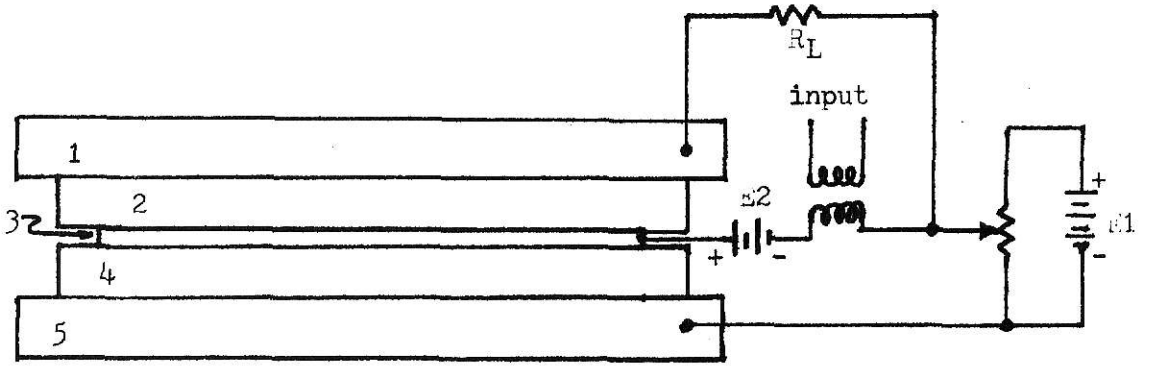

Fig. 3. Cross section view of Lilienfeld's third device.

Professor Lilienfeld's third device consisted of a layer of magnesium (3) sandwiched between two layers of copper sulfide (2) and (4). For good ohmic contact to the outside world, gold (1), (5) was to be deposited on the outer surfaces of the copper sulfide. The copper sulfide-magnesium junctions are rectifying, and therefore provide for a high resistance path for current driven by potential E1. Again as for the first two devices, potential E2 sets the operating point of the modulating signal. Lilienfeld claimed that the thickness of the magnesium layer should be about 2 angstroms. According to the inventor, "the amplifier may be operative also if the outer layers be constituted by the polarizable metal and the intermediate layer by a conducting polarizing compound. In such case, however, the bias of the intermediate layer should be negative, while in the previous case it was positive."

A comparison of the three amplifying devices of Lilienfeld with each other brings one to some rather astounding conclusions. The first device shown in fig. 1 is similar to the junction field effect transistor, the device in fig. 2 resembles quite closely the insulated-gate field effect transistor and most amazing of all is the resemblance of device number three to the modern bipolar

transistor, both npn and pnp! Lilienfeld claimed that such devices as described in his patents had several advantages over vacuum tubes: no filaments, lower circuit voltages, small size, long life, small manufacturing costs, and small input capacitance. Although the device in fig. 3 physically resembles a bipolar device, it is not. It is doubtful that Professor Lilienfeld was aware of minority carriers which play such an important role in today's bipolar transistor. But to discount the reasonability of the device on those grounds is to lack imagination. It seems probable that if Lilienfeld had devoted all his efforts to achieve a working amplifier he may eventually have invented the point contact transistor, particularly if he had been working for such a group as RCA or Bell Telephone. As it turned out, Professor Lilienfeld was an anachronism - a man twenty years before his time.

Several years before Lilienfeld began applying for his patents a discovery was made by Professor G. W. Pickard [4], which unfortunately didn't stir up the interest that it deserved. While experimenting with a cat's whisker crystal detector to which he had connected a 9 volt battery, the circuit began to oscillate. Since a short article appeared in an amateur radio publication, QST, it is hard to believe that dozens of hams did not duplicate Pickard's circuit and give rise to the beginnings of a serious investigation into the characteristics of semiconductors. The device which Pickard had stumbled onto would later be called the tunnel diode.

In 1938, Hilsch and Pohl built a triode with an alkali halide crystal [5], but its amplification was limited to frequencies less than 1 hz. It was after Hitler's War that an intense investigation of the properties of semiconductors at Bell Labs began which resulted in the discovery of a practical solid state amplifier [6]. Under the direction of W. Shockley at the Bell Labs in December of 1947 John Bardeen and Walter Brattain invented the transistor by

touching the surface of a block of germanium with two electrodes very closely spaced as in fig. 4 [6]. It was theorized that by applying a potential between the germanium and an electrode, a "point contact", an electric field of sufficient strength could affect the current flowing into an adjacent point contact in such a manner as to amplify signals corresponding to changes in the electric field. The point contact configuration amplified an input signal but it was later found that it was due to the emitter injecting plus charges or holes into the germanium. Bell Labs was awarded a patent for their transistor and in 1952 they began to license other companies to manufacture and sell them.

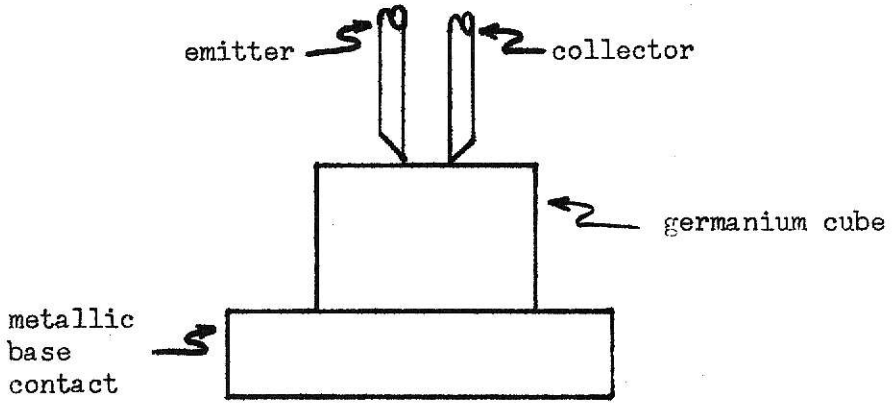

Fig. 4. Bell Lab's first transistor - the point contact transistor.

The race was on and transistor technology was and still is in a state of flux. First came the junction transistor, then zone refining, grown junction transistors, thermal diffusions, mesa transistors, silicon dioxide masking and planar transistors. The planar technique, developed by Jean Hoerni of Fairchild [7], consisted of growing an oxide on a silicon wafer, and selectively etching areas through the oxide where diffusions were desired. The oxide served as an impurity mask and a succession of two or three diffusions, each one in successively smaller surface area as in fig. 5, so that the emitter, base and collector are all accessible at the surface of the device; hence,

the name "planar".

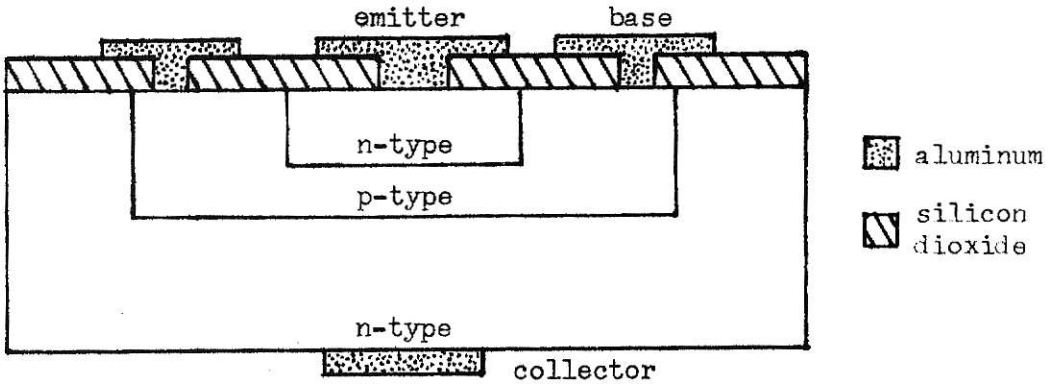

Fig. 5. Planar transistor.

The planar technique spurred the development of the insulated-gate field effect transistor, also called the MOS, or metal oxide semiconductor. This transistor is truly a field effect device. As opposed to the bipolar device, the IGFET depends only on majority carriers rather than both majority and minority carriers. The transistor fabricated at KSU while pursuing the research herein described resembles the semiconductor triode patented by M. Atalla [8] in 1962. The process begins with a lightly doped p-type silicon wafer and an oxide layer around 1000 angstroms thick applied to the surface of the silicon as in fig. 6(a). Using photo etching techniques, selected areas are etched through the oxide layer. When the wafer is heated in a diffusion furnace in the presence of n-type impurity atoms, the remaining oxide acts as a mask and does not allow the impurities to diffuse into the silicon except in the areas of bare silicon. (See fig. 6(b).) After the impurity diffusion has been successfully carried out the oxide mask is removed from the wafer and a new oxide layer is applied to the silicon. Again with photo etching techniques, areas are selectively etched through the oxide and aluminum is vacuum deposited over the entire wafer as in fig. 6(c). By selectively etching away specific portions of the aluminum and annealing the wafer at a temperature slightly below the silicon-aluminum eutectic temperature to insure a good alloy bond

between the aluminum and silicon the transistors are completed and ready for testing. As can be determined by inspection of fig. 6(d), aluminum conductors make ohmic contact with the two heavily n-doped regions which are called the source and drain and are electrically interchangeable. The aluminum deposit over the channel and insulated from it by the oxide layer is the gate electrode and, as can be seen, forms a capacitor with the channel being one capacitor plate, the aluminum over the oxide being the other.

The insulated-gate field effect transistor lends itself quite nicely to a hueristic or "hand waving" introduction to the principles upon which the device functions. A thorough description of the IGFET could certainly consume an entire text book. There are two types of IGFET's, the enhancement type and the depletion type. The n-channel enhancement type, shown in fig. 7,

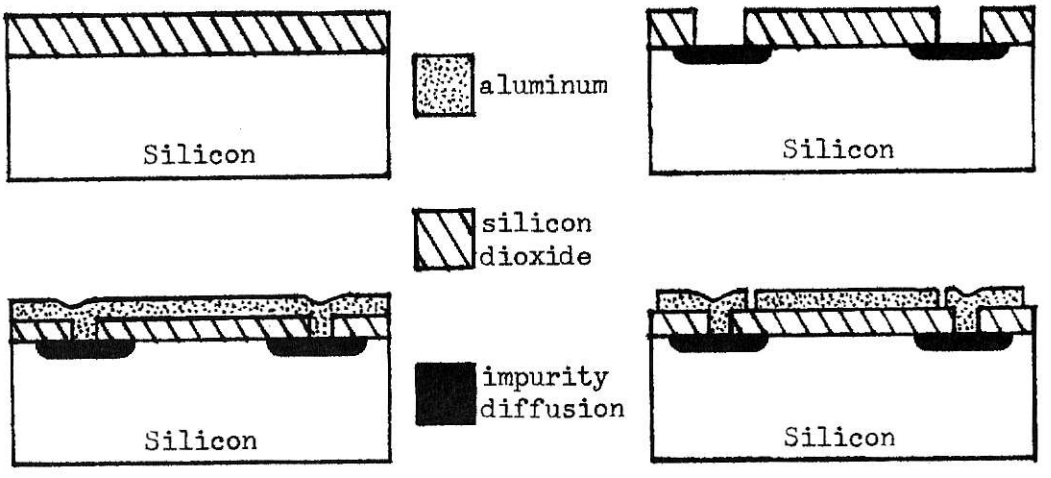

Fig. 6. The silicon wafer is first prepared by applying a thin layer of silicon dioxide over the surface (a). Windows are etched through the oxide and the diffusion is made (b). A thin layer of aluminum is deposited over the entire wafer (c). Specific areas of the aluminum are etched away to yield the finished IGFET (d).

consists of a source, drain, insulated gate and a p-type channel. The source and drain, being n-type, form a pn junction with the channel and therefore are equivalent to two diodes connected in series back-to-back, which constitutes a high resistance circuit. A potential applied between the source and drain contacts will therefore cause a very small current equal to the leakage current of the pn junction which is reverse biased. A positive potential applied to the gate electrode with respect to the substrate will attract electrons out of the source and drain diffusion regions which will migrate into the channel area and locate themselves at or very near the silicon-silicon dioxide interface. The surface of the silicon substrate will therefore become n-type which means that the source and drain now have a current path available between them. The more positive the gate is made the more electrons are attracted into the channel and therefore the smaller the resistance of the current path across the channel. This device is called an n-channel FET because the channel must become n-type in order for source-drain current to flow. It is referred to as an enhancement type device because in order to establish source-drain current the channel must be "enhanced" with majority carriers (in this case, electrons).

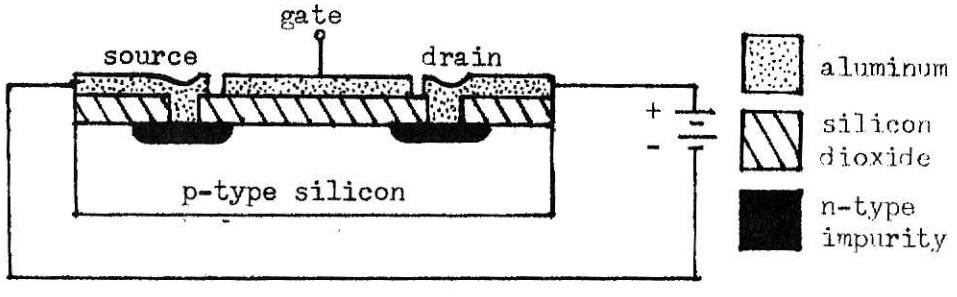

Fig. 7. Enhancement type n-channel IGFET cross section.

The n-channel depletion insulated-gate field effect transistor is identical to the enhancement type except that during the diffusion of the source and drain regions a small amount of impurities is allowed to diffuse into the

channel as in fig. 8. There does not exist a pn junction at the source-channel or drain-channel interface. Therefore a current path exists between the source and drain with zero gate bias. The application of a negative potential at the gate electrode with respect to the substrate will force some of the free electrons out of the channel thus increasing the channel resistance. A sufficiently large gate potential will completely deplete the channel of majority carriers (electrons for the n-channel device) and essentially no source-drain current will flow. Hence this device is called a depletion device.

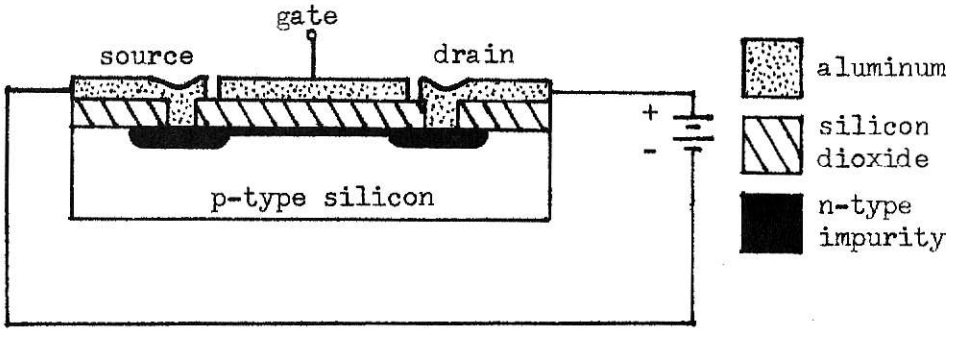

Fig. 8. Cross section of the depletion type n-channel IGFET.

Admittedly the above developments are intuitive but a more rigorous treatment of the IGFET is given in chapter V. At this point it may be more meaningful to review Lilienfeld's three devices and contrast them with the modern day insulated gate FET.

CHAPTER 3

EXPERIMENTAL TECHNIQUES

As Atalla suggests [9], surface cleaning is in reality surface doping and since the IGFET is a surface device whose characteristics depend upon surface states it is reasonable to expect that the surface treatment used in cleaning the silicon determines to a great extent the resultant device characteristics. The cleaning process should accomplish the following [9]: (a) remove surface imperfections (mechanical), (b) remove the weakly bound organic surface residues, (c) remove chemically bound organic substances, (d) remove metallic impurities, (e) provide in a controlled fashion a thin surface oxide. Particular care was taken to avoid contaminants which diffuse through silicon dioxide with relative ease, such as sodium. The cleaning process used for the KSU IGFET (Appendix 4) appears to suit these requirements as proposed by Atalla.

All possible sources of sodium contamination were avoided, such as glassware, tap water, perspiration, body grease and common laboratory chemicals such as sodium bicarbonate. The chemical hood where the bulk of the cleaning process took place was prepared by wiping it down with a sponge and a mild Alconox solution followed by a very thorough rinse. 100 ml. plastic beakers were used for all the cleaning liquids specified in the appendix, each filled to approximately the 40 ml. level. The sulfuric acid, the two mixed acids and the trichloroethylene were heated to 80 to 85° Centigrade by placing them in an electric frying pan filled with an inch or so of water and adjusted so that the water never quite reached the boiling point. Teflon tweezers were used at all possible times, the exceptions being in the trichloroethylene and when working around the hot quartz paddle in the furnace. The sodium bicarbonate kept on hand for acid spills was stored outside the hood. The rinse water

used for rinsing the wafer was double distilled water obtained from the physiology department and stored in a five-gallon teflon jug on top of the chemical hood. The elevated jug provided sufficient water pressure for the ion filter attached to the inside wall of the hood at shoulder level, the two being interconnected with a piece of tygon tubing. Plastic syringes were secured from student health and each syringe was dedicated to one specific substance. The wafer was transported, rinsed and stored in plastic petri dishes.

After cleaning the wafer as specified in the appendix, it was dried under a 275 watt sun lamp at eight inches for 15 minutes. The wafer was placed in the spinner and flooded with silicafilm using a syringe fitted with a millipore filter assembly and then spun at 3000 rpm for 30 seconds. The wafer was again flooded with silicafilm and spun as before and then inserted into the diffusion furnace at 950° C. for five minutes. After this brief heat treatment the wafer was again placed in the spinner, flooded with silicafilm and spun at 3000 rpm for 30 seconds. The wafer was then put into the diffusion furnace for 40 minutes at 950° C. which completed the diffusion mask oxide layer.

After removing the wafer from the furnace it was <u>immediately</u> taken to the spinner and the photoresist application begun. Using another syringe fitted with a micropore filter assembly, four drops of Shipley photoresist were applied and the wafer spun for 30 seconds at 3000 rpm followed by the application of four more drops and an identical spin program. The wafer was then laid eight inches below the sun lamp and dried for 15 minutes exercising care not to overheat the photoresist.

After baking the wafer it was exposed to mask 01, the "diffusion" mask, for two minutes to ultra violet light in the Western Electric vacuum hold

down alignment exposure jig. Development of the resist-coated wafer took 15 seconds in a 50% deionized water 50% Shipley developer solution, after which the wafer was rinsed two minutes in deionized water and then the resist pattern was hardened by baking it 15 minutes under the heat lamp. A particular area of the wafer was selected to be photographed at each stage throughout the fabrication process. This area was photographed at this time and appears in fig. 9. The olive colored area is photoresist and the blue silicon dioxide is visible through the open areas or windows in the resist. The wafer was submerged in a beaker of buffered hydroflouric acid and the beaker placed in an ultrasonic cleaner for six minutes which etched the bare oxide down to the silicon surface. Extreme care must always be exercised when using HF acid because of the absence of any immediately painful reaction with skin and its visual indistinguishability from water. The painful reaction with tissue comes several hours after exposure by which time most of the tissue damage is done; this damage is sometimes so severe that it requires surgery to remove damaged tissue and bone. After rinsing the wafer in deionized water, removing the photoresist with acetone and rinsing again for several minutes in deionized water, the wafer was dried under the heat lamp and inspected with a microscope.

Fig. 10 shows that the etching went well as demonstrated by the nice sharp lines and apparent lack of severe imperfections such as pin holes or pattern spreading. The tan areas are windows etched through the oxide to the silicon.

The bare silicon patterns in fig. 10 are the areas into which the impurities were about to be diffused. The wafer was placed in the spinner and flooded with phosphorsilicafilm, a phosphorous doped silicafilm, using again the syringe and filter assembly, followed by the same spin profile as previously used. The wafer was flooded again and spun again and then placed in the diffusion furnace at 950° C. for 30 minutes. While in the furnace

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EXPLANATION OF PLATE I

Fig. 9. The wafer prior to etching in buffered hydroflouric acid. The olive area is the photoresist and the blue is silicon dioxide unprotected by the resist which is to be etched away.

Fig. 10. Etched diffusion windows reveal the silicon beneath the blue oxide covering the remainder of the wafer.

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PLATE I

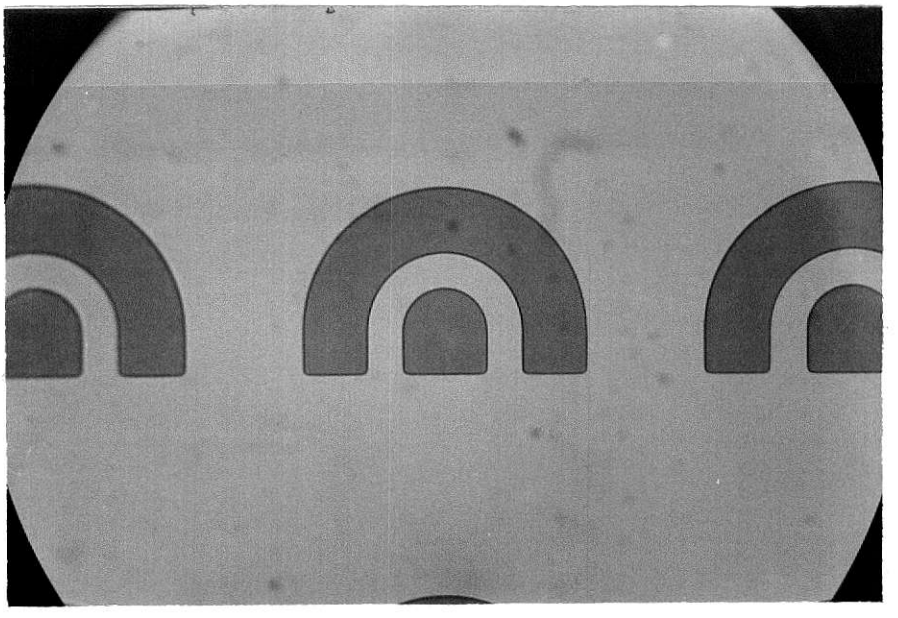

Fig. 9.

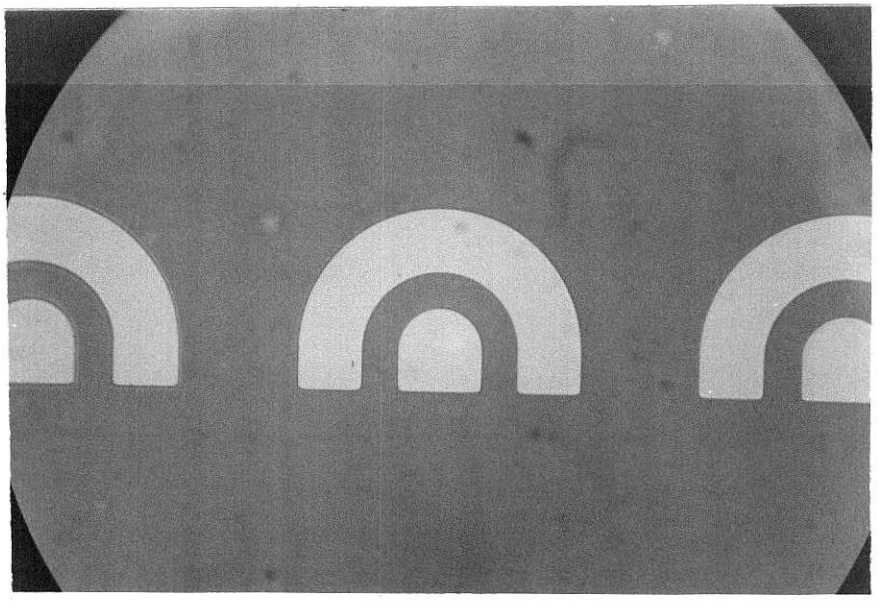

Fig. 10.

phosphorous atoms diffused into the wafer only at locations where the oxide had been etched away. In fig. 10 the semicircular, tan areas are locations into which phosphorous atoms diffused while in the furnace, the outer ring being the source diffusion, the inner semicircle being the drain diffusion, and the blue being the silicon dioxide mask. The oxide mask was then removed by etching for six minutes in buffered HF, rinsed several minutes in deionized water and dried under the heat lamp.

The wafer was placed in the spinner where five drops of silicafilm were applied with a plastic syringe with attached millipore filter assembly and spun at 3000 rpm for 30 seconds followed by five more drops of silicafilm and an identical spin. The wafer was then baked in the diffusion furnace for five minutes at 950° C. in order to harden the oxide coating just spun on. Five more drops of silicafilm and another spin followed the heat treatment and the wafer was put back into the furnace at the same temperature for 55 minutes.[1] The oxide just applied served as the gate dielectric, a permanent part of the transistor, whereas the first oxide was only temporary.

Immediately upon removing the wafer from the furnace photoresist was applied as described on page 14. After drying the resist coated wafer under the heat lamp for 15 minutes it was exposed to mask 02, the "ohmic contact" mask, using the same technique and equipment as previously used with the additional step of alignment required. That is, the pattern of this mask had to be precisely aligned with reference to the areas of the wafer previously diffused. Alignment marks on each mask allow for very accurate alignment and are described in Appendix 2 and illustrated in fig. 16. The wafer was developed,

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[1] In a private conversation with a representative of Emulsitone, Dr. Lee of the KSU Physics department was advised that the silicafilm coated wafer should be placed in the furnace at a very high temperature for a time well in excess of the times in the Emulsitone literature in order to "densify" the oxide and even at that it was doubtful if the resultant oxide would be suitable for MOS devices. Thirty to sixty minutes at 950° C. was arbitrarily chosen.

EXPLANATION OF PLATE II

Fig. 11. The photoresist pattern over the dielectric oxide. The tan areas are photoresist and the blue is the dielectric oxide. Note that the phosphorous diffused areas are visible.

Fig. 12. Windows etched through the oxide, blue, reveal the underlying silicon substrate, grey. Note that the previously phosphorous diffused areas are glassy in appearance.

PLATE II

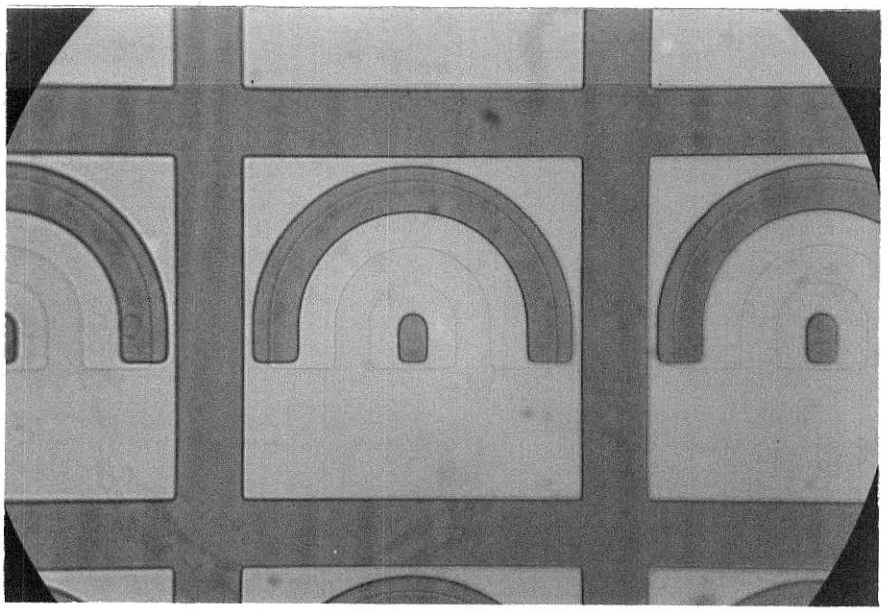

Fig. 11

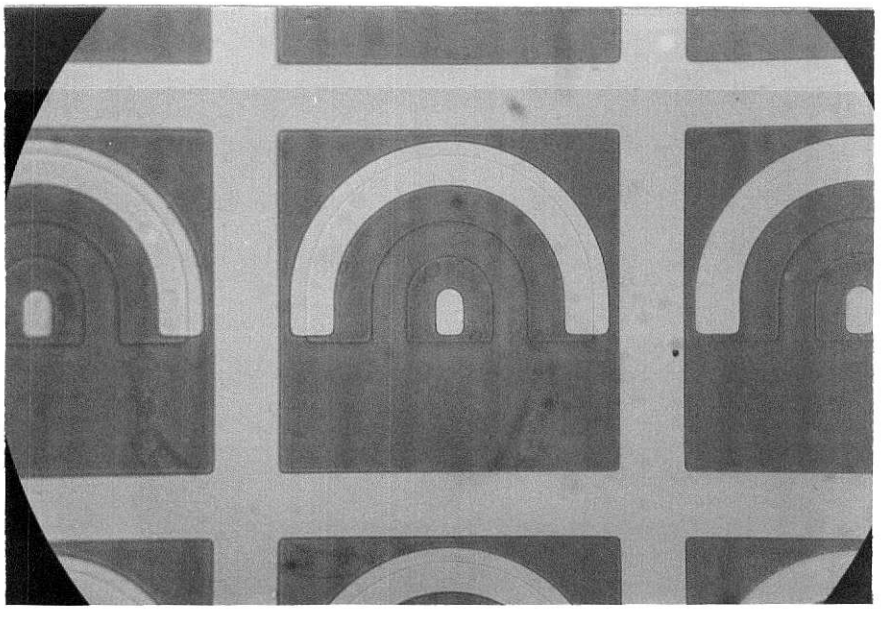

Fig. 12

rinsed and dried in the same manner as for the first pattern. As fig. 11 indicates, the exposure and development went well, with the tan portion being photoresist and the blue being oxide.

The wafer was placed in buffered HF and etched for six minutes in the ultrasonic cleaner, after which it was rinsed briefly, the resist removed with acetone, and rinsed for five more minutes in deionized water. At this point the wafer corresponded to fig. 6(b), and its photograph appears in fig. 12, the blue being oxide and the grey being silicon. Close inspection of figs. 11 and 12 reveals that the phosphorous doped areas are quite visible, a requirement for proper alignment of the second mask. In fig. 12 it can be seen that a small window was etched to the central region of the drain diffusion and the window etched down to the source diffusion extends beyond the diffusion onto the undiffused silicon. The subsequent evaporation of aluminum onto the wafer therefore, shorts the source to the substrate making the resultant transistor a three-terminal rather than a four-terminal device.[2] As a result, two transistors mounted on the same header have their sources connected together through the header itself, considerably restricting the available circuit wiring options.

Immediately after rinsing, the wafer was dried with the heat lamp and the specified area photographed under the microscope and then put into the vacuum system. The drying and photographing was done as rapidly as possible in order to keep oxidation of the exposed silicon to a minimum. The evaporation of aluminum onto the wafer was made when the pressure inside the bell jar reached 8×10^{-5} torr with the wafer heated to 250° C. by a small incandescent lamp placed about one half inch above the back of the wafer, and the temperature

2 The MOSFET is essentially a four-terminal device: source, drain, gate and substrate. Since in most circuit applications the source is usually, but not always, connected to the substrate, the decision was made to do the connecting right on the transistor die.

measured with a thermocouple placed about one quarter inch above the back of the wafer. Although this pressure was not as low as hoped for, the system had leveled off at this pressure, which from previous experience was barely sufficient. Aluminum films evaporated at too high pressure are characterized by dull and sometimes brown tinted films of aluminum. The aluminized wafer's photograph is in fig. 13 and the various surface features are visible through the aluminum, thus making the next alignment step possible. The aluminum thickness was measured as approximately 1200 angstroms with an interference microscope. A too thick film of aluminum renders the surface features of the wafer invisible, thus making alignment of the next mask impossible, whereas a too thin layer of aluminum fails to fill in the etched windows completely due to shadowing leading to a high percentage of device failure. The wafer at this juncture corresponded to fig. 6(c).

Photoresist was applied in the usual manner and the wafer dried as before under the heat lamp. The wafer was aligned under mask 03, the "metalization" mask, exposed, developed, rinsed and dried in the usual manner. Figure 14 shows the appearance of the same transistor die shown in the last five figures after photoresist development with the dark brown being resist-covered aluminum and the light brown being bare aluminum. The bare aluminum was etched away with aluminum etch[3] at 80° C. which took about three minutes. Rapid etching was hampered by the bubbles formed on the surface of the aluminum being etched. These bubbles clung tenaciously to the surface and the wafer had to be repeatedly removed from the etchant and the bubbles washed away under a stream of deionized water and then placed back into the etchant. When the bubbles stopped forming the etching was complete as confirmed by inspection

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3 Nine parts 48% orthophosphoric acid, one part 46% ammonium persulfate.

EXPLANATION OF PLATE III

Fig. 13. The aluminized wafer. the various surface features are visible under the thin metal film.

Fig. 14. The wafer ready for etching away the bare aluminum, light brown, and retaining the aluminum beneath the resist, dark brown.

PLATE III

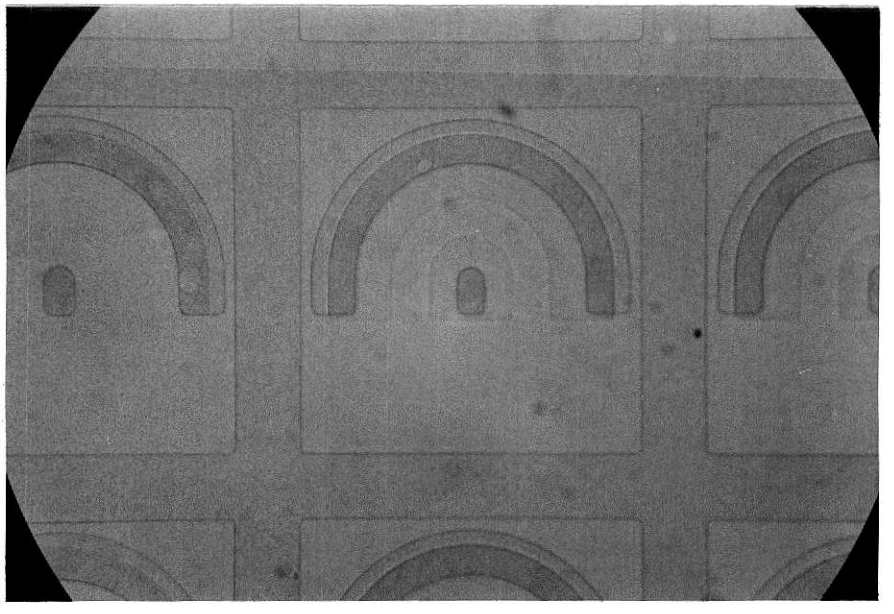

Fig. 13

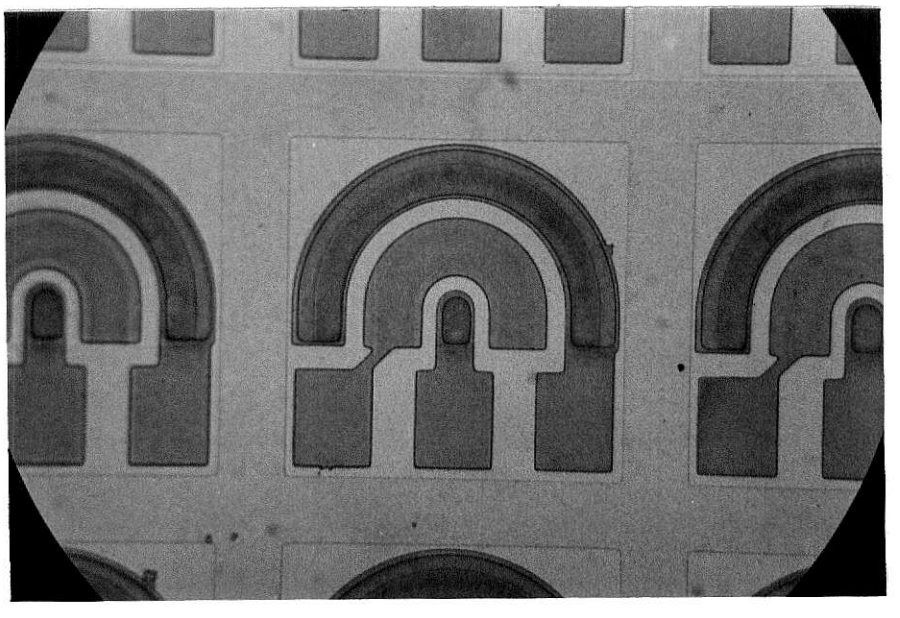

Fig. 14.

under the microscope. The photoresist was removed with acetone and the wafer rinsed in deionized water. The wafer was given a final cleaning by scrubbing it ultrasonically in a beaker of 80° C. trichloroethylene followed by a dip in methanol at room temperature and a five minute wash in running deionized water. The wafer was then dried under the heat lamp and photographed. Figure 15 is the finished transistor prior to alloying the aluminum/silicon ohmic contacts. The aluminum appears gold in color while the oxide is blue and the silicon is grey. Since silicon dioxide is amorphous, the oxide lying between transistors where the wafer would later be scribed and broken was etched away producing a "scribe grid".

The wafer was placed in the diffusion furnace at 550° C. for five minutes [10], [11] in order to insure that the aluminum and silicon form a good ohmic contact or alloy together. The transistors at this point were completed, corresponding to fig. 6(d), and were ready for testing.

The method just described required that the wafer be exposed to three different masks. Thus a means must be provided so that the last two masks can accurately be aligned over the pattern left on the wafer by the previous mask. For this reason each mask has on it a few alignment marks. A set of one of these marks is shown in fig. 16 as it appeared on the completed wafer. The alignment mark from the first mask is the grey, glassy pattern (phosphorous-doped silicon). The alignment mark from the second mask is the cluster of four blue oxide triangles oriented inside the first mark. The third alignment mark is the gold colored pattern positioned amongst the first two patterns. By aligning on one mark near the top of the wafer and another near the bottom of the wafer, one is assured of correct alignment throughout the entire mask. It can be readily seen that the second and third masks were shifted slightly to the left of the first.

EXPLANATION OF PLATE IV

Fig. 15. The completed transistor. The bonding pad on the right is the source, the center pad is the drain and the one on the left is the gate. The gate is a capacitor plate over the channel between the source and drain.

Fig. 16. A set of alignment marks on the completed wafer where the glassy, grey pattern is a diffused region, the blue pattern is oxide and the metallic pattern is aluminum.

PLATE IV

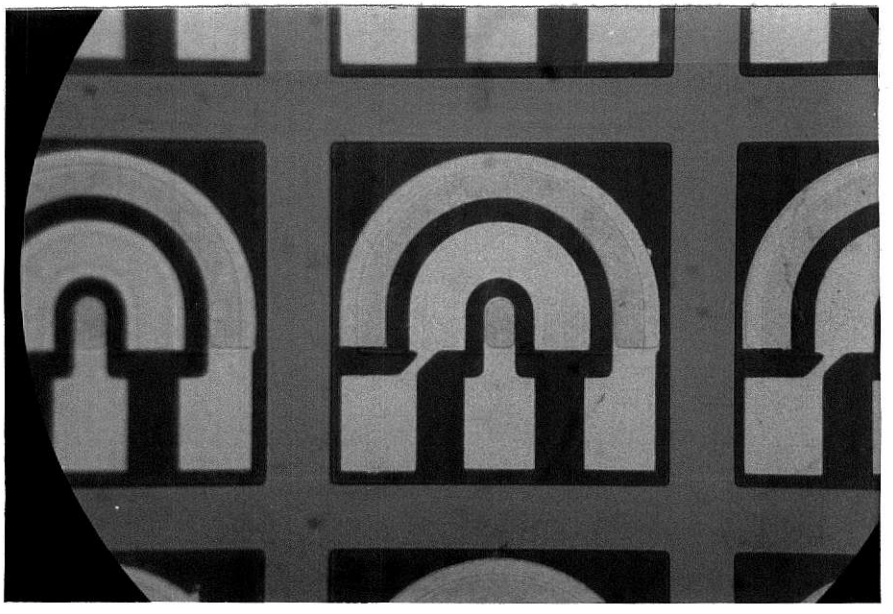

Fig. 15

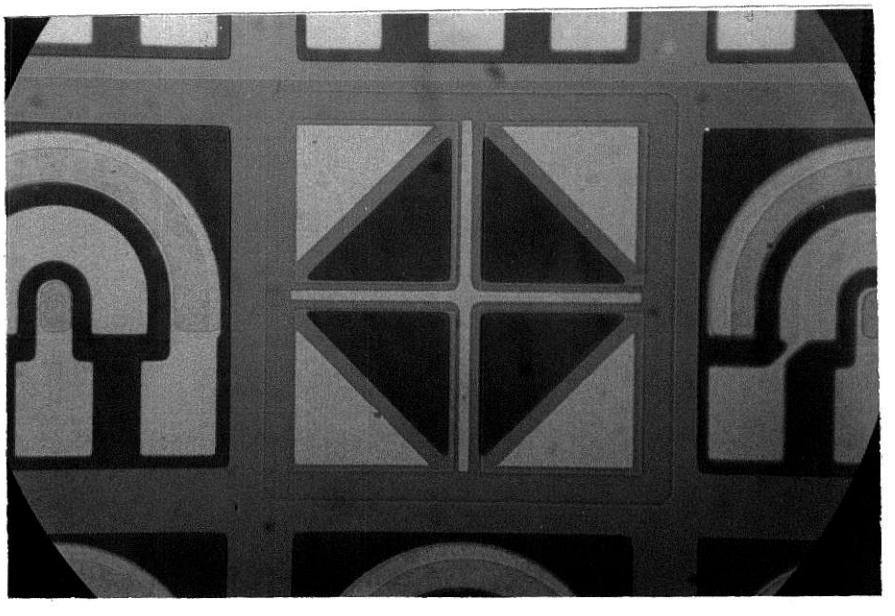

Fig. 16.

In order to test the transistors a three-point probe was constructed using three sewing needles, plexiglass and set screws which was then fitted onto the alignment jig. While observing under the microscope, the wafer could be positioned under the test probe by the jig's micromanipulator and the points gently

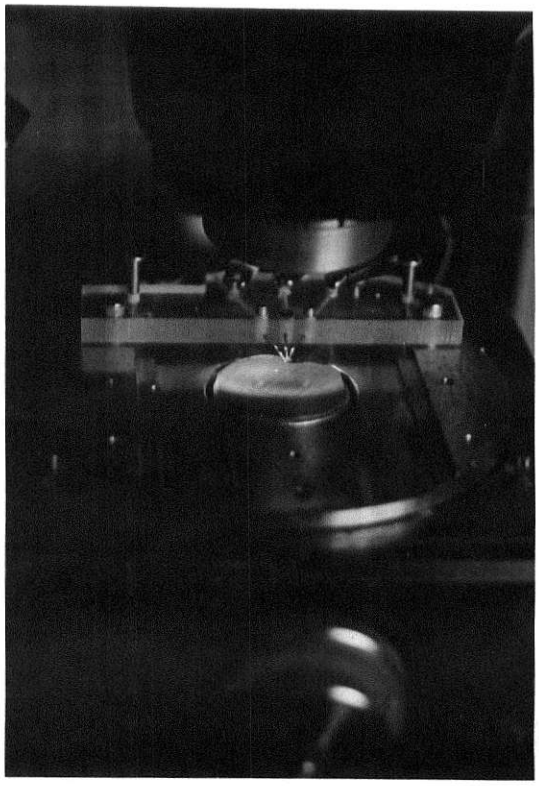

Fig. 17. The test probe mounted on the alignment jig.

dropped down onto the bonding pads. Ordinary hook-up wire connected the probe to a Tektronix 576 curve tracer. Figure 17 shows the test probe mounted on the alignment jig. The range of the alignment jig in the x- and y-directions was sufficient to test about one dozen transistors before having to reposition the wafer on the vacuum platform. Needless to say, this process was time consuming and, therefore, only about ten percent of the approximately 3000 transistors on the wafer were tested.

CHAPTER IV

EXPERIMENTAL RESULTS

Sample checks were made with the curve tracer at random points throughout the wafer and it was found that some areas exhibited better transistor curves on the average than others. In fact, some locales had no working devices at all. It was estimated that 60 to 70% of the transistors displayed some sort of transistor action on the curve tracer but perhaps only five to ten percent had characteristics similar to IGFET's available on the market today.

Figure 18 is typical for the majority of the working devices with a

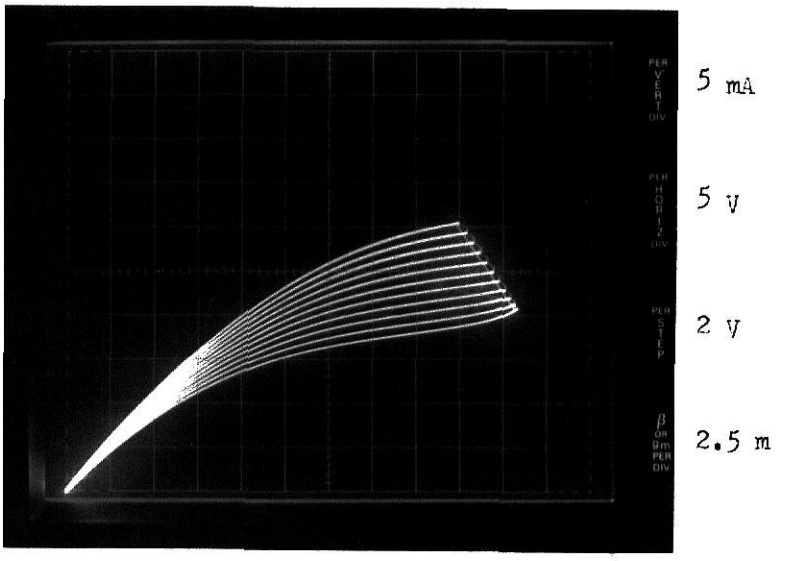

Fig. 18. A curve typical of most of the 60 to 70% of the working transistors.

transconductance of about 500 micromhos, a pinch off voltage which is not clearly defined and a source to drain current of 20 to 30 milliamperes at zero gate volts. The top curve in fig. 18 is the zero gate volts trace and the bottom trace is for a gate potential of -20 volts. As explained in Chapter II these are the characteristics of depletion FET's.

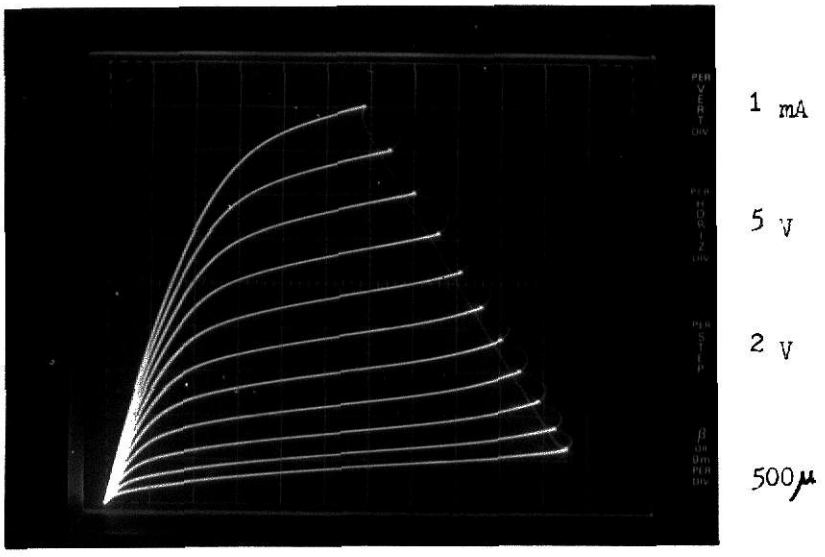

Fig. 19. The characteristic curves of one of the best transistors on the wafer, typical of about 5% of the transistors.

Figure 19 is the family of curves for one of the better transistors on the wafer, having a transconductance of 600 micromhos at zero gate volts and source-drain voltage of 30 volts. No transistors were found which had a higher transconductance than about 600 micromhos and it is doubtful that there were any.

Breakdown was observed on most transistors and would have been observable on all the working transistors except that occasionally the gate electrode would short to the channel while the transistor was being tested. Breakdown begins first on the trace with the greatest negative potential supplied to the gate. The most dramatic breakdown and the most unusual transistor found on the wafer is one whose family of curves appears in fig. 20. Notice that breakdown occurs first on the botton trace (gate volts equal -20 volts) and last on the top trace ($V_g = 0$).

An attempt was made to measure the gate threshold voltage with the curve

EXPLANATION OF PLATE V

Fig. 20. A rather unusual set of characteristic curves dramatically illustrating that breakdown occurs first on the maximum gate potential trace. In this instance $V_g = -20$ volts.

Fig. 21. Overlapping of the bottom traces indicates that there is a minimum source-drain current below which the device will not go.

PLATE V

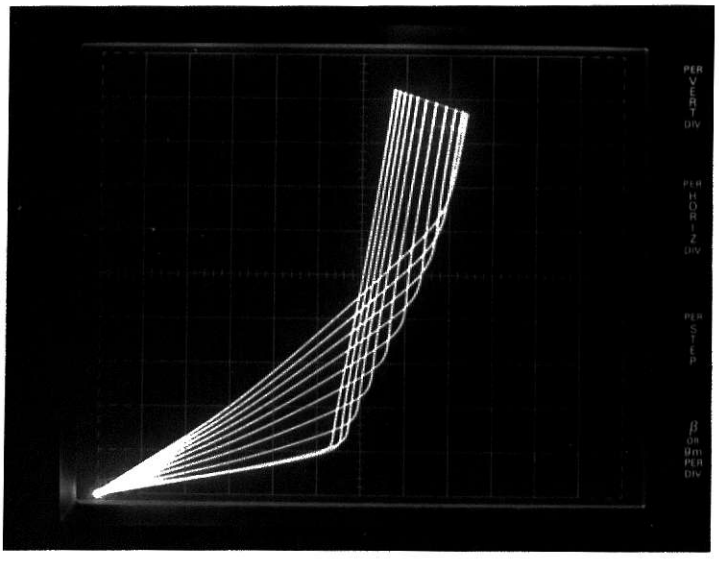

Fig. 20.

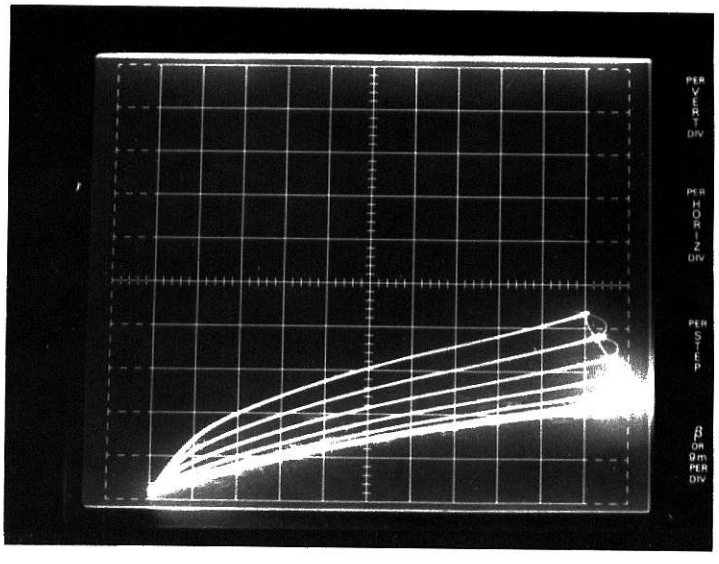

Fig. 21.

tracer but the drain current could not be reduced to zero as evidenced by fig. 21. The transconductance in fig. 21 at Vgs = -30 volts is approaching zero and zero transconductance has occurred just beyond Vgs = -30 volts indicated by the overlapping of the last four traces, Vgs = -32 to -40 volts.

Resistance measurements of 10^7 can be made with the curve tracer. By connecting the source and the drain of the transistor to the source input of the curve tracer and connecting the transistor gate to the drain input of the curve tracer an attempt was made to measure the gate resistance by taking the reciprocal of the slope of the trace. Since the slope was zero, the gate resistance was much greater than 10^7 ohms.

CHAPTER V

CONCLUSIONS

Since the surface of a semiconductor at the semiconductor-insulator interface is usually n-type [12], [13], n-channel enhancement IGFET's ordinarily require that the channel receive an additional p doping [10]. Therefore, it was not too suprising that the KSU IGFET's acted as depletion rather than enhancement devices. Furthermore, the positive charges which become trapped in the oxide during the oxide growth [13] or deposition process attract electrons (minority carriers in the p-type silicon) from the bulk silicon, which migrate to the surface of the semiconductor, increasing even more the number of electrons at the channel-oxide interface. Had the number of electrons at or near the surface of the channel of the transistor represented in fig. 19 been greater, the curves would all have shifted upward to yield a higher source-drain current for a given set of source-drain, source-gate voltages. The curves would shift as though a bias voltage were being applied to the gate.

The curves in fig. 19 would also have shifted if the oxide thickness were changed. A thinner oxide, the oxide charge being the same, would have caused the top trace, Vgs = 0, to shift upwards slightly because the charge density would have increased; more importantly, the transconductance would have increased [12] resulting in a spreading of the traces in fig. 19. A thinner oxide would also have reduced the gate-drain breakdown voltage; this means that a trade-off must be made between transconductance and gate breakdown voltage. Gate thicknesses of between 800 and 2,000 angstroms are typical [12], [14]. The gate dielectric thickness in the KSU IGFET's was approximately 1,000 angstroms as measured with an interference microscope. The diversity in device characteristics appears to have been caused by variations in surface inversions, (i.e., the minority carriers near the surface for some reason

outnumber the majority carriers) rather than in dielectric oxide thicknesses. The device in fig. 18 has a transconductance of about 500 micromhos, almost the same as the one in fig. 19, but for the same operating conditions the channel current is higher for the device in fig. 18 than the one in fig. 19. Since the transconductances were nearly the same throughout the wafer, the oxide thickness must have been fairly constant.

Avalanche breakdown, shown in fig. 20, occurs at the back biased substrate-drain pn junction and is dependent upon the gate-drain potential. The electric field in the depletion region surrounding the diffused drain adds to the gate-channel field in the drain-channel junction area [15]. The greater the negative gate potential the stronger the field in this drain-channel junction and a sufficiently strong field will cause avalanche breakdown. Thus breakdown takes place first at large negative gate voltages and last at more positive gate potentials in n-channel IGFET's as illustrated quite clearly in fig. 20. Successful electric field modulation of avalanche breakdown in FET's has been accomplished by some experimenters [12] and would provide for some useful research at KSU except that the reasons for one transistor to exhibit such an indestructible breakdown and not the others are not known, therefore making reproduction of that transistor difficult.

As previously mentioned, in none of the transistors could the channel current be completely cut off by application of a gate bias potential. Inspection of the device geometry in fig. 15, page 24, reveals the reason why. There is an unwanted channel between the source and drain not covered by the gate electrode. This channel is located between the source and drain bonding pads and has its origin in the surface inversion. This extraneous channel dominates the lower limit of drain current. It would be a wise precaution in depletion type FET's to have the gate completely isolate the source from the drain

physically, such as an annular configuration. Quite likely conduction in the channel beneath the gate metalization in the FET in fig. 21 was reduced to zero by the gate bias.

There are three modes of operation for the FET: (a) the variable resistance region, (b) the saturation region, and (c) the avalanche breakdown region.

FET operation in the saturation region is depicted in fig. 22. With a negative potential applied to the gate and a positive potential applied to the drain (both with respect to the source, remembering that the source is shorted to the substrate), the potential difference between the gate and channel is greater at the drain end than at the source end. If the difference is sufficient to deplete a portion of the channel of carriers, that portion of the channel is said to be pinched off. This condition corresponds to the bending of the characteristic curves from a large slope to a slope of nearly zero, and as can be seen in fig. 19, the pinch-off region is rather nebulous, particularly for the KSU FET's. Pinch-off is the boundary between the variable resistance and saturation regions of operation as shown in fig. 23. With an increase of drain potential, the depletion layer length in the channel will increase but not by an amount sufficient to decrease the length of the remainder of the

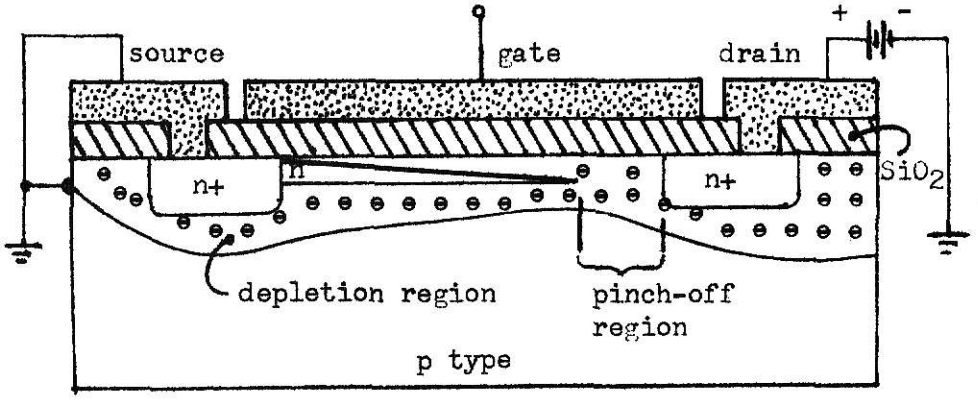

Fig. 22. Cross section view of the depletion IGFET beyond pinch-off.

channel substantially. The voltage across the non-depleted portion of the channel will remain fairly constant [12] and the remainder of the source-drain potential will appear across the depletion layer which is space-charge limited [15]. The drain current is, therefore, almost constant after pinch-off has

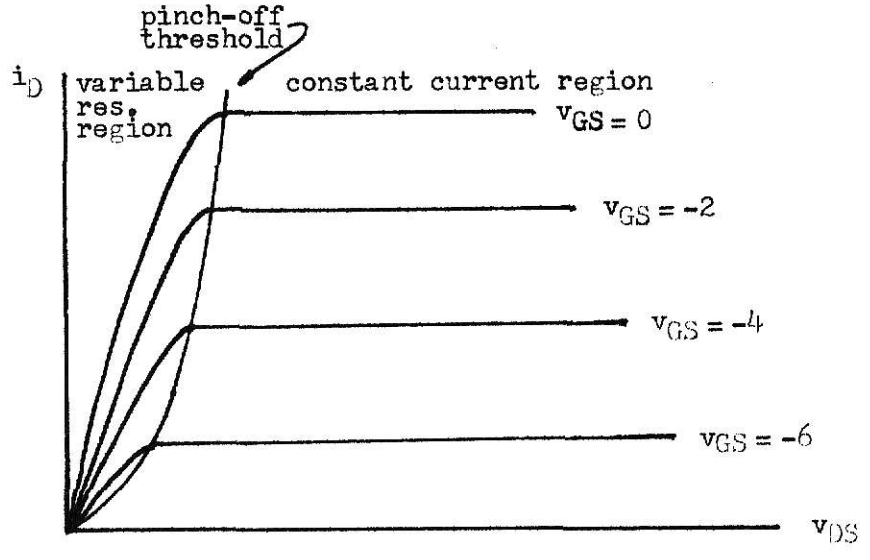

Fig. 23. Typical set of IGFET characteristic curves partitioned into two regions by the locus of the pinch-off voltage.

been obtained, provided that the drain potential is below the avalanche breakdown point.

In the variable resistance region of the characteristic curves, the channel current is essentially ohmic. Any circuit containing a variable resistance which varies as a circuit voltage is suited for an MOS transistor operating in this mode. Angelo [16] lists the drain current equations for the n-channel depletion IGFET as follows:

(a) for the variable resistance region: $i_D \approx K[2(v_{GS}-V_T)v_{DS}-v_{DS}^2]$ (1)

(b) for the saturation region: $i_D \approx K(v_{GS}-V_T)^2$ (2)

where $K = \mu\varepsilon W/2TL$,

μ = electron mobility in the channel,

ε = absolute permittivity of the gate dielectric,

W = channel width,

T = dielectric oxide thickness,

L = channel length between source and drain.

The threshold voltage, V_T, is the gate voltage just sufficient to cut off the drain current. The transconductance, g_m, is defined as the derivative of the drain current, i_D, with respect to the gate voltage, v_{GS}. Therefore:

$$g_m = di_D/dv_{GS} = 2K(v_{GS}-V_T) = \mu\varepsilon W(v_{GS}-V_T)/TL. \quad (3)$$

μ is determined by the type of semiconductor material being used and ε is dependent upon the oxide, and the control that can be exercised with these two parameters is limited. V_T can be controlled with the channel doping but accurate control is difficult, particularly for n-channel depletion devices with untreated channels [13]. Compared with commercially available MOS transistors the KSU transistors exhibited a rather low transconductance. Inspection of equation (3) indicates that the transconductance could have been improved with a better choice of device geometry. The channel length (source-drain separation) could have been reduced considerably and the channel width increased by using a spiral, comb or snake shape geometry rather than a simple semi-circle. Channel lengths of four or five microns are typical in current microwave MOSFET's [17] as compared with a 50 micron channel length in the KSU transistor. Once the transistors have been fabricated the transconductance could be increased by mounting more than one transistor on the same header and bonding them in parallel which would of course increase the input capacitance. Decreasing the gate oxide thickness would increase the transconductance, but as previously explained, there is a limit on minimum oxide thickness.

Since the KSU transistors turned out depletion rather than enhancement type the question arises as to whether the surface inversion was caused solely by surface contamination or partly by oxide charge. A very simple method of

determining the direct effects of any oxide charge on the device characteristics would be to remove all oxide from the transistor except where it serves as an insulator between the gate and channel. This could be done by etching the wafer in fig. 14 in HF after removing the aluminum with the aluminum etch. This would leave much of the device surface unprotected but would serve as a test to study the effects of the oxide charge. If a p-channel field effect transistor were to be made this kind of test would be even more useful because in p-type transistors inversions are due mainly to oxide charge. Removing all of the unnecessary oxide would remove the unwanted channel between the source and drain bonding pads.

Oxide charge can be removed during device fabrication by heating the wafer to a high temperature (circa 1000° C.) in a nitrogen atmosphere [20], or by exposing the oxide to ultraviolet radiation [21]. A KSU FET was selected and exposed to an ultraviolet lamp for four hours while connected to the curve tracer and the oxide charge was reduced somewhat as the volt-ampere curves all shifted down by approximately one half milliampere.

C-V curves (capacitance versus voltage) were recorded and the results appear in fig. 24. The gate electrode was used for one plate and the substrate was used for the other plate. Curves were taken at six different locations on the wafer and were similar except for shifts along the horizontal axis of two of the curves. The ratio C_{min}/C_{max} was the same for all six curves, 0.54, and from the work of Zaininger and Heiman [19] the impurity concentration N was sufficient to result in a channel resistivity of 0.6 ohm cm. Shifting along the horizontal axis is due to immobile charge in the oxide [13]. Several weeks after completing the KSU FET's equipment necessary to grow thermal oxides was acquired and capacitors were made with thermal oxide dielectrics and checked on the C-V analyzer. The thermal oxide curves were shifted very far from the

spin-on oxide curves along the abcissa with the valley of the curves lying at about 50 volts. Heating the oxide to 400° C. in a nitrogen atmosphere for one hour reduced the oxide charge so that the valley of the curve fell at 40 volts but this still was too great for MOS transistors. Annealing the wafer in the presence of a strong electric field would speed up the migration of charge out

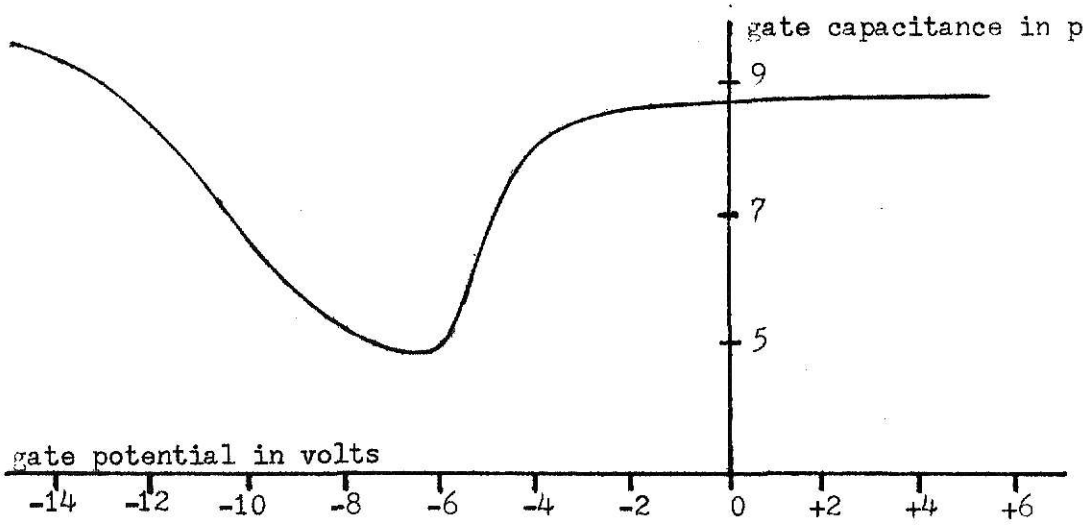

Fig. 24. C-V curve for a typical KSU FET.

of the oxide. Experiments with annealing would have to find an efficient method of reducing oxide charge in order to use thermally grown oxides as dielectrics in FET's. It is quite possible that the quartz flask used to boil the deionized water was not cleaned sufficiently or that the deionized water itself was contaminated. Since the trapped charge in the spin-on oxide was so much less than in the thermal oxide, perhaps it would be wiser to go ahead and utilize the spin-on oxide for further transistor fabrication and experiment with methods of reducing the charge in this oxide. Growing a thermal oxide however has a big advantage over a spin-on oxide in that the oxide-silicon interface recedes into the silicon as the oxide is growing resulting in a cleaner insulator-oxide interface.

The KSU transistors were developed with the intention of building the foundation of an integrated circuit capability. If the sources had not been

shorted to the substrate during production steps, several dies could have been bonded to the same header and the transistors interconnected in a fashion that would yield, in essence, an integrated circuit. Better quality transistors would be desirable for this scheme, i.e., higher transconductance, lower threshold or pinch-off voltage and passivation. Lower threshold voltages could be obtained by making p-channel devices in which surface accumulation rather than inversion would be present. Higher transconductance could be maintained by adherence to good geometrical design. Semiconductor manufacturers currently use silicon nitride as a passivation layer but phosphorsilicafilm would provide adequate passivation [18]. A fourth photographic mask was prepared for surface passivation, which allowed for the entire completed wafer to be coated with phosphorsilicafilm that could be selectively etched away from the bonding pads and scribe grid. The KSU FET's were not passivated because long term stability was not necessary.

Although threshold voltage is not easily controlled, MOS integrated circuits could be made and the threshold voltages adjusted by x-ray radiation techniques. Equipment exists on the Kansas State University campus for x-ray trimming of MOS transistors.

Many changes in technique were made when in the first and second wafers none of the transistors were found to be functional. Since silicon dioxide is not a diffusion barrier to sodium, sodium contamination can be quite troublesome, particularly in view of its relative abundance. To reduce the probability of sodium contamination, glassware was completely avoided on the third try, polypropylene beakers being used instead. Sodium bicarbonate, usually kept under the chemical hood for use on spilled acids, was removed from under the hood but kept nearby in case of a bad spill. Most acid spills encountered were of a small scale and use of bicarbonate was halted since immediate washing of

of the spill with water proved adequate. The practice of using metal tweezers was stopped when possible. Metal tweezers were used only in the trichloroethylene and for manipulating the wafer on the hot furnace paddle. The use of teflon tweezers not only helped reduce metal ion contamination but also reduced mechanical damage to the surface of the wafer. A supply of double distilled water was found in the Physiology Department which undoubtedly made a vast improvement in the chances for success, since the distilled water from the Mechanical Engineering still was stored in an open container and always had a large quantity of dirt floating on the surface. The ideal method would be the use of a quartz still for the second distillation and the washing of the wafers in a closed or recirculating water system plus the monitoring of the water conductivity as a measure of wafer purity.

The second wafer was off to a good start until it was dropped and landed face down on the floor. It was washed and the processing continued but the outcome was doomed. To further guarantee failure, three films of aluminum had to be deposited on the wafer since the first two were apparently evaporated at too high a pressure resulting in a dull film to which photoresist would not adhere properly.

The problem of finding a suitable point at which to stop processing and storing the wafer for a day or two was avoided by not stopping until the transistors were completed. A one hour diffusion allows ample time to break for dinner.

Alignment of the photographic mask over the wafer was impossible unless the light being used was directed down from above the mask. To obtain such lighting a piece of fibre optics was used with one end placed at the source of yellow light and the other located above the mask just out of the field of view. A fellow student made the clever observation that the binocular

microscope being used would yield parallel light simply by shining the light down one of the eyepieces. Indeed this worked but light alignment was touchy and a sturdy adaptor would have to be made for the eyepiece in order to hold the light source firmly in place.

The research efforts described in this thesis were successful because they culminated in many insulated-gate field effect transistors with characteristics good enough to be utilized in many circuits, such as choppers, high input impedance stages, low power amplifiers, etc. Judgement of this work must include consideration of the modest amount of equipment and money used. Although the insulated-gate field effect transistor is ten years old now, it is possible for other students to bring the solid state laboratory capabilities at KSU to the very forefront of semiconductor technology through diligent effort.

Shortly after the transistors were completed and while feeling quite elated a small speck on a piece of paper on my kitchen table was noticed to be flying around. It would fly for a time less than one second and cover a distance no more than an inch or two. After a five or ten second rest it would take off again. This beast was so small that he or she could not be seen while in flight. A magnifying glass similar to the removeable eyepiece found in most microscopes was placed over the mysterious creature trapping it in the magnifying glass assembly. By aiming the paper and glass toward the light the little animal could be observed while he walked around the surface of the paper. It was as though a math professor had used a housefly in one of his examples in which he let an area shrink to a point for this small speck looked exactly like an ordinary housefly, except that his body was so thin that he appeared to be made of cellophane. It occurred to me that this insect, which was capable of eating, walking, seeing, flying and even reproducing, would fit quite nicely on one of my transistor chips!

APPENDICES

APPENDIX 1

FINAL DIMENSIONS

The final transistor dimensions are given in figures 26 through 29 which are drawn 200 times the final dimensions. The rubylith patterns were cut 500 times final size and the least area was peeled. A standard 3 mil scribe grid was used on the ohmic contact and passivation masks which allows for the scribing to take place on the silicon surface rather than silicon dioxide. Each rubylith pattern was required to have two alignment marks, one on each side of the pattern. These marks are centered nine inches to the left and right of the vertical center of the pattern and centered horizontally as shown in fig. 25. To insure overlap in the step and repeat procedure, the scribe grids were extended 0.20 inches on the rubylith. The rubylith alignment marks did not appear on the finished photographic masks.

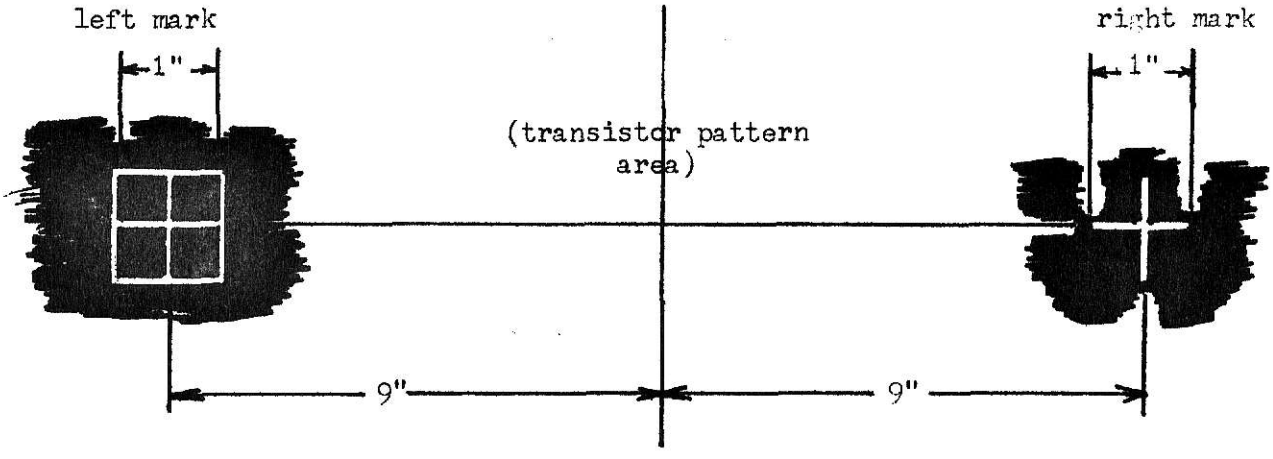

Fig. 25. Rubylith alignment marks. Alignment mark line widths = 40 mils.

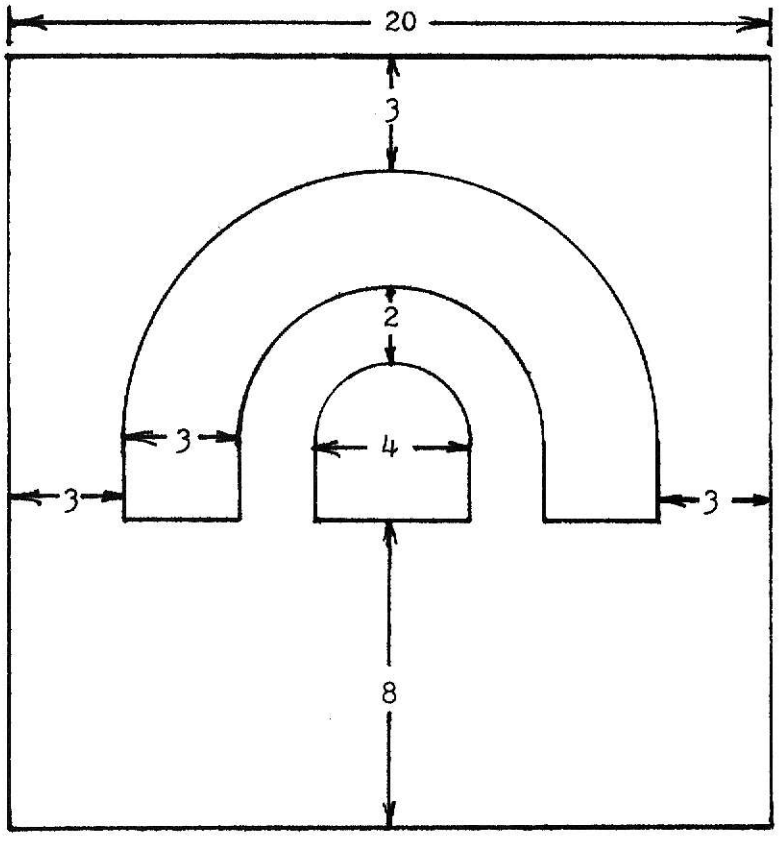

Fig. 26. Mask 01 - diffusion mask. Dimensions are in mils.

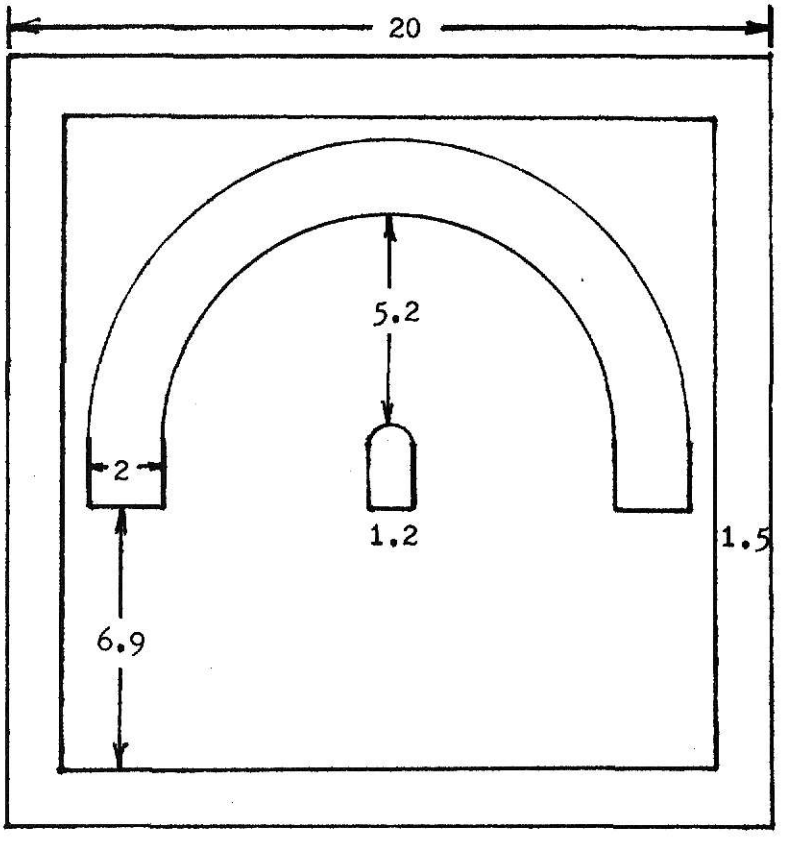

Fig. 27. Mask 02 - ohmic contact mask. Dimensions are in mils.

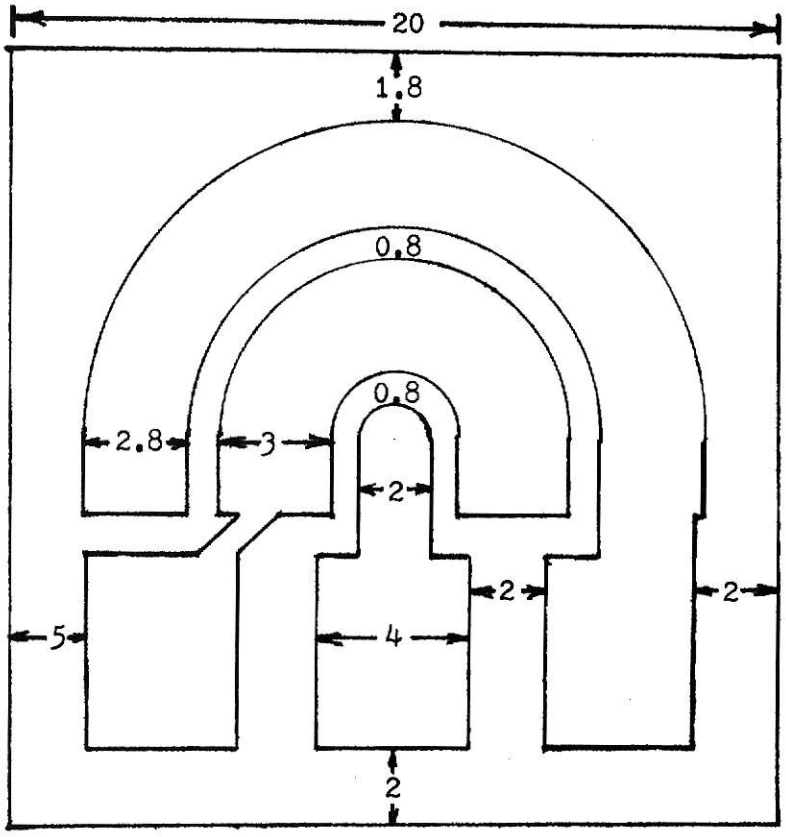

Fig. 28. Mask 03 - metalization mask. Dimensions are in mils.

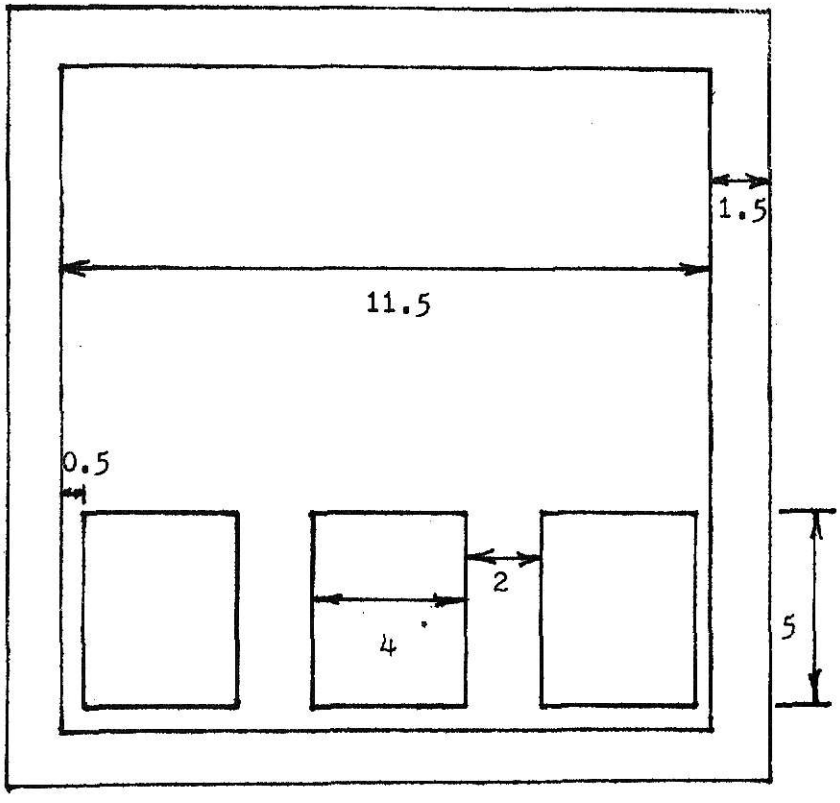

Fig. 29. Mask 04 - passivation mask. Dimensions are in mils.

APPENDIX 2

PHOTOGRAPHIC MASKS

The photographic masks were prepared by the Semiconductor Products Division of Motorola in Mesa, Arizona, using the rubylith patterns cut out at KSU on the coordinatograph. The transistor patterns were spaced 20 mils center-to-center and separated by a 3 mil scribe grid, and arranged in a 100 by 100 matrix. Within the matrix there were two alignment marks on each mask along the vertical center, two along the horizontal center and one at the intersection of the horizontal and vertical centers. The wafers used were considerably smaller than the wafers used by Motorola but large enough so that two alignment marks could be located upon the wafer, which proved sufficient since it only takes two points to describe a line. The alignment marks are illustrated quite vividly in fig. 16 on page 23. The mark corresponding to the first mask is the outer square divided into four quadrants by the cross and is glassy in appearance. The mark on the second mask consists of a blue diamond divided into four triangles. The third pattern's marks are the metallic pattern made up of four triangles positioned around the cross. These alignment marks are obviously the result of a lot of first hand experience on Motorola's part since alignment went without any difficulties. The exposure was done on a Kodak High Resolution plate measuring $2\frac{1}{2}$ by $2\frac{1}{2}$ by 1/16 inches. Since the alignment jig in the KSU lab was a gift from Western Electric, a special platform had to be milled in the Mechanical Engineering shops to adapt the jig for use of the Motorola masks.

APPENDIX 3

SILICON WAFER PROPERTIES

Polished silicon wafers were purchased from Chisso Corporation, 7-32 Chome Marunouchichiyoda-Ku, Tokyo, Japan, for $1.40 each. The certificate accompanying the wafers specified the following mechanical and electrical properties:

orientation - (1-1-1), off < 1°

lifetime - > 50 microseconds average

parallelism - < 12.7 microns across the slice

type - P

dopant - boron

resistivity - 40 to 70 ohm cm.

diameter - 28 to 31 mm.

thickness - 0.240 to 0.280 mm.

orientation of flat (reference edge) - (2-1-1) direction parallel to the (1-1-0) plane.

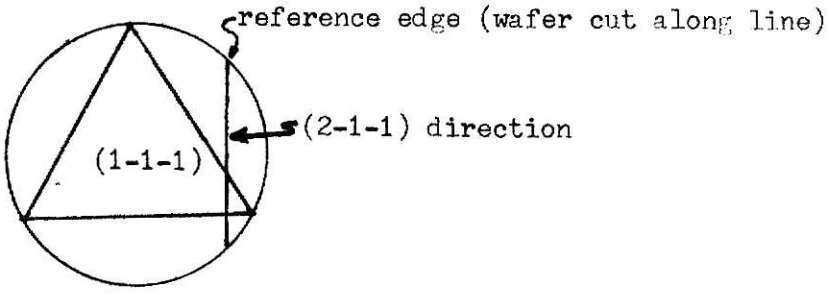

Fig. 30. Reference edge (flat) orientation.

APPENDIX 4

THE CLEANING SEQUENCE

The cleaning methods used at Western Electric in Lee's Summit, Missouri, were adapted for use in processing silicon wafers at KSU. The KSU procedure was mainly the same as Western Electric's except that the deionized water rinse at KSU was not recirculating and did not come from a quartz still. Where Western Electric would rinse a wafer until the water conductivity fell below 2.5 megohm cm., the KSU wafers were simply rinsed in a stream of deionized water for approximately five minutes.

Starting with polished wafers, Western Electric cleans their silicon as follows:

1. Degreasing cycle. The wafers are placed in hot trichloroethylene and cleaned ultrasonically for five minutes which removes organic contaminants, after which they are briefly rinsed in room temperature methanol, followed by a deionized water rinse.
2. Sulfuric acid cycle. The wafers are then put in hot concentrated sulfuric acid for 15 minutes. With the wafers still in the hot acid they are then ultrasonically cleaned for an additional ten minutes, followed by a deionized water rinse.
3. Mixed acid cycle. Equal parts of concentrated sulfuric and nitric acids are mixed and heated and the wafers placed therein. After 15 minutes in the hot mixed acid, the wafers are scrubbed ultrasonically for ten minutes in the same acid bath. The wafers are then rinsed thoroughly in deionized water. The acids remove metallic and inorganic contaminants.
4. Hydroflouric acid cycle. The wafers are then carefully submersed in 48% hydroflouric acid at room temperature for 60 seconds which removes mechanical damage from the silicon surface. The personal hazards in handling HF

are so severe that special hoods, lab coats and gloves must be used. After the HF etch the silicon is so clean that the surface will not wet which tends to make the water float in the following rinse in deionized water.

5. Mixed acid cycle. The wafers are put again into hot mixed acid for 15 minutes followed by an additional ten minute ultrasonic scrub in the same acid medium. The wafers are then given a final rinse in deionized water and dried in hot nitrogen. Visual inspection under a bright light will reveal any gross contaminants such as stains, streaks, or scratches.

Thirty seconds rather than sixty seconds was used for the etch time in HF for the KSU wafers for no other reason than it seems to work. Rather than drying the wafers in hot nitrogen, the KSU wafers were dried by placing them eight inches beneath a 275 watt sun lamp on the clean air bench for 15 minutes. For a time a product called Transene 100 was used to treat the wafers with as a final step prior to drying as it supposedly dries residue free, but some trouble was experienced in getting the silicafilm to adhere to the silicon after the Transene 100 treatment so this measure was eliminated as a precaution. Use of glassware was completely avoided in the cleaning process except that the deionized water came from a glass still. The hot mediums mentioned in the W. E. schedule are between 85 and 95° Celsius.

APPENDIX 5

EQUIPMENT AND SUPPLY REQUIREMENTS

The following is a list of equipment and supplies used in the fabrication of insulated-gate field effect transistors.

Clean-air bench: Edcraft Ind., Model CHL 846.

Diffusion furnace: Centigrade Systems, Inc., Model 10000, series AD, S.N. 316.

Chemical hood: suitable for use with HF.

Chemical hood: Hemco Co., suitable for use with sulfuric and nitric acids.

Filter ass'y.: Lab-line/Elga Hi-purity deionizer, catalog #28000.

Filter: Hi-purity deionizer cell, catalog #28010.

Spinner: Headway Research, Inc., Model EC 101-CB15, S.N. 20703.

Syringe: 3 ml hypodermic syringe, plastic.

Filter: Millipore #UHWP01300 for use with silicafilm.

Filter: Millipore #NRWP01300 for use with Shipley photoresist.

Filter Holder: Millipore, Swinney, catalog # XX30-012-00.

Microscope: Unitron, Model MMU, S.N. 34454, with interferometer.

Microscope: Bausch & Lomb, binocular, 0.7 - 3 power zoom.

Ultrasonic cleaner: Sears, Model 514-73150.

Beakers: 100 ml, polypropylene.

Quartz liner: Western Electric (donor), 2 5/8 inch O.D.

Quartz paddle: Western Electric (donor).

Vacuum pump: Duo-Seal.

Dopant: Emulsitone Co., Phosphorsilicafilm.

Oxide: Emulsitone Co., Silicafilm, spin on oxide.

Photoresist: Shipley, AZ-1350, positive resist.

Developer: Shipley, AZ-1350 developer.

Acid: Concentrated sulfuric, electronic grade.

Acid: Concentrated nitric, electronic grade.

Acid: 48% hydroflouric, electronic grade.

Acid: Buffer hydroflouric, electronic grade.

Solvent: Trichloroethylene, electronic grade.

Solvent: Methyl alcohol, electronic grade.

Rubylith: Ulano, 5DM.

Coordinatograph: Micromarker, Packman Research, LTD, England.

Masks: Complete set of photographic masks, courtesy Motorola.

Acid: Orthophosphoric.

Chemical: Ammonium persulfate crystals.

Vacuum system: Varian, VE-60 Evaporator.

Metal: Aluminum, 99.999%, A. D. Mackay, Inc.

Filament: Tungsten.

Solvent: Acetone, electronic grade.

Thermometer: -20 to 110° C.

Hot plate: Sunbeam teflon electric frying pan.

Alignment jig: Western Electric (donor), no model number, incl. u.v. source.

Lamp: Sears, sun lamp, 275 watt.

Tweezers: Teflon.

Tweezers: stainless steel.

Silicon: Chisso Corp., 28 mm. dia., 40 to 70 ohm cm.

Curve tracer: Tektronix, model 576.

Capacitance bridge: Bontoon Electronics, Model 71 AR, S.N. 1502.

Chart recorder: H. P. Moseley, 7004A X-Y recorder, S.N. 845-00580.

Power supply: Harrison Laboratories, Model 865B 0-40 volts, S.N. 4035.

Water: Double distilled, deionized, at least 10 gallons required.

Apparel: Gloves, safety goggles and coat suitable for use with HF.

Petri dishes: Plastic, used for storing and transporting wafers.

Many of the items listed above were obviously not indispensable. However, many items, in addition to those above, would have been used had they been available, and are listed below.

Camera: Step and repeat, preferably capable of 500:1 reduction.

Pump: Low capacity pump for use in a recirculating water supply.

Gauge: Beckman, Water Purity Controller, for measuring water conductivity.

Still: Quartz still, for making high purity distilled water.

Ultrasonic cleaner: Large capacity, capable of accepting a half gallon container.

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FABRICATION OF AN EXPERIMENTAL N-CHANNEL INSULATED-GATE FIELD EFFECT TRANSISTOR

by

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B. S., Kansas State University, 1969

AN ABSTRACT OF A MASTER'S THESIS

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A historical review of the events covering the period from 1920 to the present which led to the commercial production of field effect transistors is given. The techniques used in the successful fabrication of n-channel insulated-gate field effect transistors are recorded in sufficient detail that these experiments could easily be duplicated. These techniques include: device geometry; artwork preparation; wafer cleaning; impurity diffusion; spin-on oxide deposition; vacuum deposition of aluminum; photoresist application, exposure and development; and chemical etching. Color micro-photographs taken throughout the transistor processing are included. The reasons for the transistors exhibiting depletion rather than the intended enhancement type characteristics are discussed. Photographs of several characteristic curves as displayed by a curve tracer are shown. Suggestions are made concerning process changes which would result in enhancement type MOS transistors with improved characteristics. A complete list of equipment and supplies used to make the MOS transistors appears in the Appendix.