/GPIB INTERFACE FOR TESTING AND CONTROLLING LABORATORY PROJECTS/

by

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THIS BOOK CONTAINS NUMEROUS PAGES WITH DIAGRAMS THAT ARE CROOKED COMPARED TO THE REST OF THE INFORMATION ON THE PAGE.

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CHAPTER I

INTRODUCTION

The inclusion of a digital computer within an instrument or test system can result in major performance improvements. However, the provision of a suitable interface between the computer and the instrument which it is controlling is often a time consuming and difficult task. The IEEE 488 standard bus provides a convenient but complicated interface between a control computer and a test instrument but unless a special interface board is provided the set-up time for a new instrument is extremely long. This report discusses the design and construction of such an interface board. This board provides all of the necessary interfacing and control functions between the computer and the instrument being designed and thus enables the designer to concentrate on the instrument (Figure 1).

This interface board is flexible in that, a user can select both the mode of communication and address of the instrument as desired. The available modes include, off-line, talk only, listen only, talk/listen single address, and talk/listen extended address. An instrument can be assigned an address anywhere between zero and fifteen. Note that the extended addressing facility is utilized only for transmission of sixteen bit data. The selection of the mode and address is accomplished by setting the binary switches on the board. The board is equipped with LEDs to indicate its current (talk/listen) status. Programming the computer to perform the desired communication is very simple and uses instructions such as trigger, clear, write. The board has

latches and buffers at input and output for protection.

The next chapter includes a detailed description of the General Purpose Interface Bus (GPIB); it also outlines the handshaking procedure for data transfer. Chapter III gives circuit details, discusses the facilities provided on the board, and gives a functional description. The operating and programming instructions are provided in chapter IV. Chapter IV also contains test procedure for proper operation of the board. Conclusions and recommendations are discussed in the last chapter.

CHAPTER II

GENERAL PURPOSE INTERFACE BUS

This chapter deals with the detailed description of the General Purpose Interface Bus (GPIB), defined in the "IEEE Standard Interface for Programmable Instrumentation" (1). The standard includes mechanical, electrical, and functional specifications. The signals associated with this bus and the handshaking procedure are also elaborated in this chapter.

2.1 GPIB (IEEE 488 BUS)

GPIB is a bit parallel, byte serial party line bus structure organized to provide communication of digital data among a group of instruments and a system controller. These instruments function as talker/listener while the controller generates control instructions. Mechanically, the GPIB is a 16-wire interface that can connect as many as 15 instruments. Maximum cable length in the GPIB is 20 meters. All GPIB data and control signals are TTL-compatible and active low. The data transfer rate cannot exceed one megabyte/sec.

2.2 GPIB Control Lines

The GPIB has three control lines ($\overline{\text{DAV}}$, $\overline{\text{NRFD}}$, $\overline{\text{NDAC}}$), which operate in an interlocked handshake procedure to coordinate the asynchronous transfer of information on data lines.

$\overline{\text{DAV}}$: Data valid line is asserted true (low) by a talker after it places valid data on the $\overline{\text{DIO}}$ (data) lines. This assures the listener that the data on the bus is valid.

$\overline{\text{NRFD}}$: Not ready for data line, when asserted true (low),

indicates that not all instruments on GPIB are ready to receive data and goes high when all instruments are ready.

$\overline{\text{NDAC}}$: Not data accepted line is controlled by instruments receiving the data. This line is held true (low) until all receiving instruments capture the particular data byte.

2.3 GPIB Management Lines

Five lines are used for general interface management by the GPIB. These lines include $\overline{\text{ATN}}$, $\overline{\text{IFC}}$, $\overline{\text{EOI}}$, $\overline{\text{SRQ}}$, and $\overline{\text{REN}}$. Out of these $\overline{\text{ATN}}$, $\overline{\text{IFC}}$, and $\overline{\text{REN}}$ can be asserted only by the system controller.

$\overline{\text{ATN}}$: Attention line is asserted only by the controller during the addressing or command sequence. When forced low, all instruments must relinquish control of the interface line within 200 ns and interpret information on the data bus as command or address.

$\overline{\text{IFC}}$: It is interface clear line that transports a reset signal which can be initiated only by the controller. This is a provision for initializing the instrument.

$\overline{\text{REN}}$: It is Remote enable line that can only be asserted by the controller; when it is asserted (low), control of each instrument's function is tranferred from its front panel to programming instruction received via the interface bus.

$\overline{\text{SRQ}}$: Service request line is a type of interrupt line and can be asserted by an instrument needing service from the system controller.

$\overline{\text{EOI}}$: End or Identity line can be asserted by the system

controller or talker to notify the listener that the data byte currently on the $\overline{\text{DIO}}$ lines is the last one.

DATA BUS ($\overline{\text{DIO1}}$-$\overline{\text{DIO8}}$): All the data are transferred through these lines. Note that this transfer is governed by negative logic.

2.4 Interface Bus Concept

Instruments which communicate along the interface bus can be classified into three basic categories.

1. TALKERS- Instruments which send information on the bus when they have been addressed are termed talkers.
2. LISTENERS- Instruments which receive information sent on the bus when they have been addressed are called listeners.
3. CONTROLLERS- Instruments which can specify the talker and listener for an information transfer are designated controllers.

2.5 Handshake Procedure

Assuming that the address information is already transferred, the handshaking procedure can be explained by the following sequence of operations as illustrated in Figure 2.

The listener raises its $\overline{\text{NRFD}}$ implying that it is now ready for the data ①.

The talker then places the data on the bus and drops its $\overline{\text{DAV}}$ after allowing settling time ②.

Upon sensing $\overline{\text{DAV}}$ low the listener responds by lowering $\overline{\text{NRFD}}$ ③ and then raises $\overline{\text{NDAC}}$ ④ indicating that data have been accepted.

The talker senses $\overline{\text{NDAC}}$ high and raises $\overline{\text{DAV}}$ ⑤ indicating that

the data on the bus are no longer valid.

The listener detects $\overline{\text{DAV}}$ high and lowers $\overline{\text{NDAC}}$ ⑥ and raises $\overline{\text{NRFD}}$ ⑦ indicating that it is ready to receive the next data byte to be placed on GPIB.

An instrument is off-line unless it is specifically addressed by the system controller. The address sent by the system controller is compared with the address switched on the board. If the addresses match, GPIB controller goes active, and data transmission proceeds asynchronously at a rate determined by the speed of talker/listener. The talker and listener handshake logic is shown in Figure 3.

CHAPTER III

THE INTERFACE BOARD

This chapter includes a functional description, block schematic, and circuit details of the interface board. Furthermore, it describes facilities provided on this board.

3.1 Functional Description of the Interface Board

The block schematic for the interface board is shown in Figure 4. The interface board consists of a GPIB controller (Fairchild 96LS488), buffers, latches, switches, and some logic circuitry. The GPIB controller handles the bus protocol and handshaking between the system controller (HP9845B) and the board. The board can be set to operate in a desired communication mode and at a desired instrument address. An instrument can be assigned an address anywhere between zero and fifteen by setting four binary switches on the board. The details for mode and address setting are elaborated in the next chapter. The LEDs on the board indicate its current talk/listen status.

The board can operate in talk/listen single address, listen only, talk only, or listen/talk extended address modes. The extended address mode has been provided as an additional facility and can be utilized when 16-bit data need to be transferred. The GPIB controller (96LS488) interprets the data on lines $\overline{\text{DIO1}}$ through $\overline{\text{DIO8}}$ either as an address corresponding to an instrument or a command when $\overline{\text{ATN}}$ is low. For this interpretation, the $\overline{\text{DIO}}$ bits are decoded to determine if these data are a primary talk/listen address, a secondary address or a command

(Table1).The GPIB controller compares the primary address set by the switches on the board with the one sent by the system controller and goes active if and only if they match; otherwise the data which follow are ignored. The handshaking procedure is completed after the GPIB controller goes active. It then coordinates input/output with TTL logic using lines such as $\overline{\text{DRB}}$, RXST, $\overline{\text{TAD}}$.

If the extended address facility is used, then the select line 'ASEL' from the GPIB controller selects between the instrument primary and secondary addresses through a multiplexer. If the set primary address matches with the one sent by the system controller then the GPIB controller compares secondary addresses. In the present case secondary addresses always match. This is due to the fact that the secondary address on the board is latched in accordance with the secondary address sent by the system controller. If the single address mode is used, the multiplexer is replaced by an IC header so that primary address switches are connected directly to the GPIB controller. The reader is referred to the operating instructions furnished in the next chapter for further details. The secondary address is latched on 74LS377 when lines $\overline{\text{DAV}}$, $\overline{\text{ATN}}$, $\overline{\text{DIO6}}$, and $\overline{\text{DIO7}}$ are all low. Talk/listen single address mode is used to transfer 8-bit data. The extended address mode is used only when 16-bit data transfer is needed; this is accomplished by splitting the data into two 8-bit words and then sending them as lower and higher bytes. The data splitting is achieved by setting the least significant bit of the secondary address to zero and one for the

lower and higher bytes, respectively. In other words, when the secondary address is '00', the data byte is transferred to the lower byte latch, while the upper byte latching occurs when secondary address is '01'. Note that both the lower and higher bytes have the same primary address. When the single address mode is used, switch S1 (Figure 5) is set to 'ZERO' position and thus the data are transferred through the lower byte latch. In the extended address mode switch (S1) is set to the 'ONE' position. Inverting buffers are used for input and output because of the fact that the data on GPIB are active low.

The board is provided with an edge connector for connecting it to the system controller. The cable details are provided in Table 2. The sockets on the board provide connections for input to and output from the instrument (See Table 3).

3.2 Circuit Description

The circuit consists of the following major components (Figure5).

GPIB Controller (96LS488 - U1): The 96LS488 is a TTL LSI circuit containing all the logic necessary to interface talk, listen, and talk/listen type instruments and a system controller in accordance with IEEE-488 Standard for Programmable instrumentation (1). The 96LS488 has programming inputs (M0, M1, M2, M3) that determine whether it is to act as talker, listener, or both, single or dual address, high or low speed, according to the instrument requirements.

In this circuit, the schmitt-trigger buffer-inverter between

the CP and XTAL pins is used as a relaxation oscillator by connecting an external RC network to provide feedback.

The address inputs (A1-A5) are set high or low to assign an address to an instrument. Address input A5 is grounded to restrict the instrument addresses between 0 and 15. When programmed in the single address mode, the IC header is used to connect the binary switches directly to the address lines (A1-A4). In the extended address mode a 74LS157 (U3 in Figure 5) is used instead of the IC header and thus the primary or secondary address is selected through the MUX, which, in turn is controlled by 'ASEL' line. The IC header details are shown in Figure 6.

When a "WRITE" command along with an appropriate instrument address and data are sent by the system controller, the 96LS488 goes active if the addresses match as stated previously, and $\overline{\text{LAD}}$ goes low indicating that the board is in the listen mode (Table 4). The receiver strobe output (RXST) participates in the handshake to transfer a data byte to an instrument, when this instrument is addressed to listen. Thus the data are latched to the output latch only after RXST goes active. Then RXST is inverted and connected to RXRDY (receiver ready input), so that the 96LS488 receives the data bytes from the bus at a rate determined solely by the bus handshake. Timing diagrams for the listen address sequence are shown in Figure 7.

When a "READ" command with an appropriate instrument address is sent by the system controller, 96LS488 goes active if the addresses match as stated earlier. Furthermore, $\overline{\text{TAD}}$ goes low indicating that the board is in talk mode (Table 4). Thus, data

originating from the instrument are latched to the input latch after $\overline{TAD}$ goes low. Subsequently the 96LS488 drives $\overline{DRB}$ line low, thus, enabling external data bus driver to transfer the data to the bus. The transmit strobe output TXST is inverted and connected to TXRDY, therefore the data transfer rate is determined solely by the bus handshake (5). Timing diagrams for the talk address sequence are shown in Figure 8.

When a "CLEAR" command with an appropriate instrument address is sent by the system controller, the 96LS488 issues a negative pulse on $\overline{CLR}$ output and stays low until $\overline{ATN}$ goes high.

When a "TRIGGER" command is sent with an appropriate instrument address by the system controller, the 96LS488 issues a negative pulse on $\overline{TRIG}$ output and stays low until $\overline{ATN}$ goes high.

74LS240 (U5 and U6): These are tristate inverter buffers. Since the GPIB uses inverted data, the data are inverted before being read or written to the GPIB. One of these buffers is always enabled so that data from the system controller is always received from the bus, but the data from the instrument is transferred only when $\overline{DRB}$ goes active (low).

74LS377 (U11, U12, and U8): Two 74LS377's are used to latch data at the output when an instrument is addressed to listen. The switch S1 (Figure 5) is set to 'ZERO' position for the single address mode so that the data are latched on U12. For extended addressing, the switch (S1) is set to 'ONE' position and the higher and lower bytes of the sixteen bit data are latched on U11

and U12, respectively. The higher and lower byte transfer is done by using secondary addresses 00 and 01, respectively. The third 74LS377 (U8) is used to latch the secondary address and the S1 bit (Figure 5) is used to determine the higher or lower data byte. The address is latched when lines $\overline{ATN}$, $\overline{DAV}$, $\overline{DIO6}$, $\overline{DIO7}$ all go low simultaneously. A timing diagram for the secondary address sequence is shown in Figure 9.

74LS374 (U9 and U10): These are tristate latches and are used to read data from an instrument when the instrument is addressed to talk. The outputs of these latches are in high impedance state when they are not addressed to talk. When the single addressing is used the data are read from U10 (Figure 5). In the extended addressing mode, the data are read from U10 for lower byte and from U9 for higher byte; the lower or higher bytes are determined by the secondary addresses as 00 and 01, respectively. The data are latched when $\overline{TAD}$ goes active and is read on the bus when $\overline{DRB}$ goes active.

74LS157 / IC HEADER (U3): As explained earlier, in the single address mode, an IC header (Figure 6) is used instead of the multiplexer at U3, which connects the primary address switches directly to address lines A1 through A4.

In the extended address mode, a 74LS157 is used at U3. The line 'ASEL' from the 96LS488 selects between primary and secondary addresses. The primary address is selected when line 'ASEL' goes low while the secondary address is selected when line 'ASEL' goes high.

SOCKETS (T1, T2): The inputs and outputs are terminated on 16 pin IC sockets, T1 and T2. The connection details are given in Table 3. The details of connectors P and HP are also provided in Table 2.

List of components used on the board and the data sheet for 96LS488 have been furnished in APPENDICES A and B, respectively.

CHAPTER IV

OPERATING INSTRUCTIONS

This chapter provides operating instructions for the interface board, including mode and address settings and programming instructions. To begin the operation of the board, the first step is to connect the HP 98034A HPIB module to the system controller (HP 9845B). The bus card is then preset to select code 7. Note that the instructions in this chapter are written specifically for select code 7. Nevertheless, analogous instructions can be employed for other codes. In every instruction, the instrument address is always preceded by the select code, i.e., 7 in the present case. The standard HP connector is then hooked up to the interface board using a standard cable. Table 5 lists the available mode settings for the board.

For 8-bit data transfer in talk/listen single address mode, the following settings on the board are selected.

MODE SETTING:

M0	M1	M2	M3
H	H	L	L

Suppose that the instrument address is '03', then the following settings on the board are selected.

ADDRESS SETTING:

A4	A3	A2	A1
L	L	H	H

Next, the instrument (with address 03) input and output are connected to sockets (T2) and (T1), respectively (Figure 5). Note that pin # 16 of the socket (T2) is connected to the Most Significant bit of input data to the instrument. The other pins, 15 through 9 are connected in a descending order of the data bits. Similar connections are made for socket (T1). The switch (S1) is then set to 'ZERO' position and IC header is inserted at U3. At this stage, the board is ready to be programmed. A typical program is listed below (2). Note that the actions corresponding to the program instructions are also provided for reader convenience.

```
10  CLEAR 703           ! Clears instrument # 03
15  WRITEBIN 703;12     ! Writes '12' in binary to instrument # 03
20  TRIGGER 703         ! Triggers instrument # 03
25 V1=READBIN(703)      ! Reads data from instrument #03
                          into variable V1 in binary.
30  END
```

In the number 703, '7' refers to the select code and '03' to the instrument primary address.

For 16-bit data transfer in extended address mode, the following settings on the board are selected.

MODE SETTING:

M0	M1	M2	M3
H	H	H	H

Suppose that the instrument primary address is '02', then the

following settings on the board are selected.

ADDRESS SETTING:

A4	A3	A2	A1
L	L	H	L

The pins 1 through 8 of socket (T2) are connected to the instrument's higher input byte, while pins 9 through 16 are connected to its lower input byte. Pin # 8 of T2 is connected to the Most Significant bit of the higher input byte and other pins 7 through 1 are connected in a descending order of the data bits. Pin # 16 of T2 is connected to the Most Significant bit of the lower input byte and other pins 15 through 9 are connected in a descending order of the data bits.

The higher and lower output bytes are connected to pins 1 through 8 and 9 through 16 on the socket (T1), respectively. The switch (S1) is set to 'ONE' position and the IC header is replaced by a 74LS157 at U3. The lower input and output bytes are transferred using secondary address '00', while the higher input and output bytes use secondary address '01' for data transfer. Now the board is ready to be programmed. Programming instructions are similar to those of the single address feature. A typical program is shown below.

```
10 WRITEBIN 702.00;12    !Writes '12' in binary at lower byte
                           of instrument # 02.
15  WRITEBIN 702.01;10    ! Writes '10' in binary at higher byte
                           of instrument # 02.
```

```
20  V1=READBIN(702.00)    ! Reads lower byte from the instrument
                            # 02 into variable V1 in binary.
25  V2=READBIN(702.01)    ! Reads higher byte from the instrument
                            # 02 into variable V2 in binary.
30  END
```

In the number 702.00;12, the first digit '7' is the select code, '02' is the instrument primary address and '00' corresponds to its secondary address, '12' is the data to be written at the lower input byte to the instrument.

To ensure the proper functioning of the board, it is set in single address mode and at some desired address. The output of the board is connected to its own input. Data are then written on output latches and are read back from the input latch. The data written and read are then compared; matching of these data ensures proper functioning of the board.

CHAPTER V

CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

An interface board which allows a breadboarded instrument to readily communicate with a GPIB controller has been designed, built, and tested. The board can be programmed to operate in a desired communication mode and at a desired instrument address. The available communication modes include off-line, talk only, listen only, talk/listen single address, and talk/listen extended address. This board will enable testing and controlling a variety of laboratory instruments, especially students' circuits. It is simple and easy to operate.

RECOMMENDATIONS

In the present work certain features such as service request and status, have not been incorporated. These features can be added easily with some extra circuitry.

A "service request" can be sent by an instrument, at any time, to inform the system controller that it needs some type of interaction. The $\overline{\text{SRQ}}$ line on 96LS488 allows any instrument to interrupt the controller and request a service. The system controller can identify the interrupting instrument by conducting a serial poll or a parallel poll. In a serial poll, one byte of operational information about an individual instrument is obtained. While in the parallel poll, information about a group of instruments is obtained simultaneously. To do the serial poll, the system controller issues an unlisten command, a serial poll

enable command, and talk address of each instrument sequentially. Status strobe output (STST) from the 96LS488 can form part of the handshake logic used to pass a status byte from each instrument to the bus during the serial poll sequence. Similarly, the status ready input (STRDY) forms part of the handshake controlling the passing of a status byte to the bus during the serial poll sequence. Alternatively, the system controller can conduct a parallel poll by forcing both $\overline{EOI}$ and $\overline{ATN}$ lines low. Each Instrument responds by placing one status bit on a $\overline{DIO}$ line, where bit assignments have been previously made by the parallel poll enable command. Standard HP commands can be used to do the serial and parallel polls.

```
STATUS 703;V1              ! Do serial poll on instrument # 03.
```

This command will obtain the instrument status byte from instrument #03 and place the equivalent decimal value into variable V1.

```
PPOLL CONFIGURE 703;4      ! Respond on bit 4 (DIO4) with a '0'.
```

This command can be used for parallel polling. Instruments can be programmed remotely by the system controller to respond on a $\overline{DIO}$ line to a parallel poll, eg., in the above command instrument #03 shall respond on bit 4. The logic state of response (1 or 0) as well as the bit # (0-7) for the instrument can be programmed by a parallel poll configure statement.

Another feature that can be added is the Remote/Local facility. The 'REMOTE' statement can be used to enable instrument

on the bus to switch over to remote program control from its local front panel control. If any instrument is addressed by a remote statement, it switches to the remote control.

```
REMOTE 703          ! Instrument # 03 switched to remote control.
```

'LOCAL' statement can be used to return the specified instrument to local, front panel control.

```
LOCAL  703          ! Instrument # 03 returns to local front panel
                      control.
```

REFERENCES

1. IEEE document "IEEE Standard Interface for Programmable Instrumentation" IEEE Std. 488-1978.

2. HP 98034 Installation and Service (HP).

3. HP System 45B desktop Computer I/O ROM Programming.

4. Fisher Eugene and C.W.Jensen, "PET and the IEEE 488 Bus (GPIB)", Osborne/McGraw-Hill, Berkeley, 1980

5. Summers, Jonathan, "Microprocessor-GPIB interfacing with the 96LS488", Application note 351, Fairchild Camera and Instrument Corporation, May 1980.

APPENDIX A

COMPONENT LIST.

U1	96LS488	GPIB Controller
U2	74LS32	Two input OR gate
U3	74LS157	Quad two input multiplexer
U4	DIP Switches	Mode setting
U5, U6	74LS240	Octal inverter buffer (3-state)
U7	DIP Switches	Address setting
U8, U11, U12	74LS377	Octal D flip flop
U9, U10	74LS374	Octal D flip flop with 3-state
U13	74LS04	Hex Inverter
R1 - R8	1KΩ/1/4W	Resistor
R11, R12	1KΩ/1/4W	Resistor
R9, R10	330Ω/1/4W	Resistor
R13	150Ω/1/4 W	Resistor
R14	5.6KΩ/1/4W	Resistor
C1	150 pf	Capacitor
C2	3.3 µf	Capacitor
S1		Single pole double throw switch

FAIRCHILD
A Schlumberger Company

96LS488
General Purpose Interface Bus (GPIB) Circuit

Digital Integrated Circuits

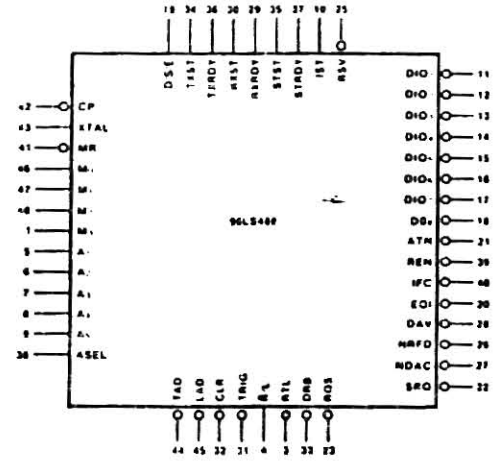
Description

The 96LS488 is a TTL LSI circuit containing all of the logic necessary to interface Talk, Listen and Talk/Listen type instruments and system components in accordance with the IEEE-488 standard for programmable instrumentation. All outputs that drive the IEEE-488 bus are guaranteed to sink 48 mA, and all bus inputs have Schmitt triggers and bus terminating networks. All pins that interface to the instrument logic are LSTTL compatible.

The 96LS488 has programming inputs that determine whether it is to be a talker, listener or both, single or dual address, high or low speed, etc., according to the instrument and system requirements. It operates with a minimum of external support logic and readily interfaces with most microprocessors. It operates from a single 5.0 V supply and a 10 MHz single phase clock and is capable of operating the bus handshake at the full 1 MHz data rate. It offers a variety of handshaking and status connections to the instrument logic for versatility and ease of design.

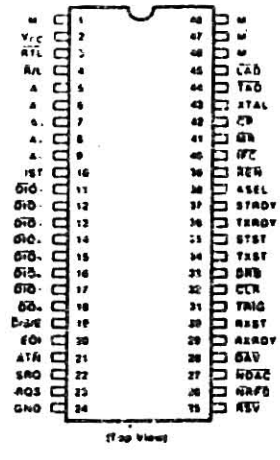
- SINGLE 5.0 V SUPPLY
- COMPLETE SOURCE AND ACCEPTOR HANDSHAKE LOGIC
- SAME OR SEPARATE TALK AND LISTEN ADDRESS
- SECONDARY ADDRESS CAPABILITY
- TALK ONLY OR LISTEN ONLY CAPABILITY
- SOURCE HANDSHAKE DELAY PROGRAMMABLE FOR LOW OR HIGH SPEED
- SERIAL POLL CAPABILITY
- PARALLEL POLL CAPABILITY
- SYNC TRIGGER AND DEVICE CLEAR OUTPUTS
- IMPLEMENTS REMOTE/LOCAL FUNCTION
- ON-CHIP CLOCK OSCILLATOR
- SERVICE REQUEST INTERRUPT FACILITY
- ALL BUS I/O SIGNALS COMPLY WITH THE IEEE-488 (1980) AND IEC-625-1 INPUT THRESHOLD, TERMINATION AND OUTPUT SPECIFICATIONS
- ALL INSTRUMENT INTERFACE SIGNALS ARE LSTTL COMPATIBLE
- GPIB PINS PRESENT NO ELECTRICAL LOAD WHEN DEVICE IS POWERED OFF

Logic Symbol



V_{CC} = Pin 2
GND = Pin 24

Connection Diagram
48-Pin DIP



(Top View)

Fairchild Camera and Instrument Corporation, Digital Division
333 Western Avenue, South Portland, Maine 04106
207/775-8700 TWX 710-221-1960

Input Loading/Fan-Out

Pin Names	Description	96LS (U.L.)** HIGH/LOW
A_1-A_5	Address Inputs	0.5/0.25
$\overline{ATN}$	Attention Input (Active LOW)	T*/1.4
$\overline{CP}$	Clock Input (Active Falling Edge)	0.5/0.25
$\overline{IFC}$	Interface Clear Input (Active LOW)	T*/1.4
IST	Instrument Status Input	0.5/0.25
$M_0 - M_3$	Mode Control Inputs	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.25
$\overline{REN}$	Remote Enable Input (Active LOW)	T*/1.4
$\overline{RSV}$	Request Service Input (Active LOW)	0.5/0.25
$\overline{RTL}$	Return to Local Input (Active LOW)	0.5/0.25
RXRDY	Receiver Ready Input (Active HIGH)	0.5/0.25
STRDY	Status Ready Input (Active HIGH)	0.5/0.25
TXRDY	Transmitter Ready Input (Active HIGH)	0.5/0.25
$\overline{DAV}$	Data Valid Input (Active LOW)	T*/1.4
	as Output (Active LOW)	130/30
$\overline{DIO_1}$-$\overline{DIO_7}$	Data Inputs	T*/1.4
	as Outputs (Active LOW)	T*/30
$\overline{DO_8}$	Data Output (Active LOW)	T*/30
$\overline{EOI}$	End or Identify Input (Active LOW)	T*/1.4
$\overline{NDAC}$	Not Data Accepted Input (Active LOW)	T*/1.4
	as Output (Active LOW)	T*/30
$\overline{NRFD}$	Not Ready for Data Input	T*/1.4
	as Output (Active LOW)	T*/30
ASEL	Address Select Output	10/5.0
$\overline{CLR}$	Device Clear Output (Active LOW)	10/5.0
$\overline{D/S/E}$	Data/Status Output (Active LOW)	10/5.0
	End-of-String Output (Active HIGH)	10/5.0
$\overline{DRB}$	Bus Drive Enable Output (Active LOW)	10/5.0
$\overline{LAD}$	Listen Address Status Output (Active LOW)	10/5.0
$\overline{ROS}$	Requested Service Status Output (Active LOW)	130/30
RXST	Receiver Strobe Output (Active HIGH)	10/5.0
$\overline{R/L}$	Remote/Local Output	10/5.0
$\overline{SRQ}$	Service Request Output (Active LOW)	T*/30
STST	Status Strobe Output (Active HIGH	10/5.0
$\overline{TAD}$	Talk Address Status Output (Active LOW)	10/5.0
TXST	Transmitter Strobe Output (Active HIGH)	10/5.0
$\overline{TRIG}$	Device Trigger Output (Active LOW)	10/5.0
XTAL	Crystal Output	10/5.0

*T = Resistive Termination per IEEE-488 Standard.

**Unit Load (U.L.) definitions
LOW State: 1.6 mA = 1 U.L.
HIGH State: 40 μA = 1 U.L.

$\overline{DIO8}$	$\overline{DIO7}$	$\overline{DIO6}$	$\overline{DIO5}$	$\overline{DIO4}$	$\overline{DIO3}$	$\overline{DIO2}$	$\overline{DIO1}$	
X	H	L	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$	PRIMARY LISTEN ADDRESS
X	H	L	L	L	L	L	L	UNLISTEN
X	L	H	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$	PRIMARY TALK ADDRESS
X	L	H	L	L	L	L	L	UNTALK
X	L	L	$\overline{S5}$	$\overline{S4}$	$\overline{S3}$	$\overline{S2}$	$\overline{S1}$	SECONDARY ADDRESS

COMMAND AND ADDRESS DECODING

TABLE 1

SIGNAL	CONNECTOR (P)	CONNECTOR (HP)
$\overline{\text{DIO1}}$	M	1
$\overline{\text{DIO2}}$	N	2
$\overline{\text{DIO3}}$	P	3
$\overline{\text{DIO4}}$	R	4
$\overline{\text{DIO5}}$	11	13
$\overline{\text{DIO6}}$	12	14
$\overline{\text{DIO7}}$	13	15
$\overline{\text{DIO8}}$	14	16
$\overline{\text{ATN}}$	Y	11
$\overline{\text{REN}}$	15	17
$\overline{\text{IFC}}$	W	9
$\overline{\text{EOI}}$	S	5
$\overline{\text{DAV}}$	T	6
$\overline{\text{NRFD}}$	U	7
$\overline{\text{NDAC}}$	V	8
$\overline{\text{SRQ}}$	X	10

CABLE DETAILS
TABLE 2

IC #	Pin #	Socket #	Pin #	
U9	3	T1	1	Connected to High Input Byte of Instrument
U9	4	T1	2	
U9	7	T1	3	
U9	8	T1	4	
U9	13	T1	5	
U9	14	T1	6	
U9	17	T1	7	
U9	18	T1	8	
U10	3	T1	9	Connected to Low Input Byte of Instrument
U10	4	T1	10	
U10	7	T1	11	
U10	8	T1	12	
U10	13	T1	13	
U10	14	T1	14	
U10	17	T1	15	
U10	18	T1	16	

INPUT AND OUTPUT CONNECTIONS

TABLE 3

IC #	Pin #	Socket #	Pin #	
U11	2	T2	1	Connected to High Output Byte of Instrument
U11	5	T2	2	
U11	6	T2	3	
U11	9	T2	4	
U11	12	T2	5	
U11	15	T2	6	
U11	16	T2	7	
U11	19	T2	8	
U12	2	T2	9	Connected to Low Output Byte of Instrument
U12	5	T2	10	
U12	6	T2	11	
U12	9	T2	12	
U12	12	T2	13	
U12	15	T2	14	
U12	16	T2	15	
U12	19	T2	16	

INPUT AND OUTPUT CONNECTIONS

TABLE 3 (Contd.)

$\overline{TAD}$	$\overline{LAD}$	$\overline{D/S/E}$	STATE
H	H	L	OFF LINE
H	L	L	ADDRESSED TO LISTEN(LADS)
L	H	L	ADDRESSED TO TALK(TADS)
L	H	H	SERIAL POLL MODE(SPM)
H	L	H	RECEIVING END MESSAGE(LACS)

STATUS CODES

TABLE 4

MODE INPUTS				OPERATING MODE	FUNCTION
M0	M1	M2	M3		
L	L	L	L	Off line	Device cannot take part in any GPIB operation
L	H	L	L	T	Talk only, single address mode
H	L	L	L	L	Listen only, single address mode
H	H	L	L	T/L	Talker/Listener Single address
H	H	H	H	TE/LE	Talker/Listener extended address

MODE SETTINGS

TABLE 5

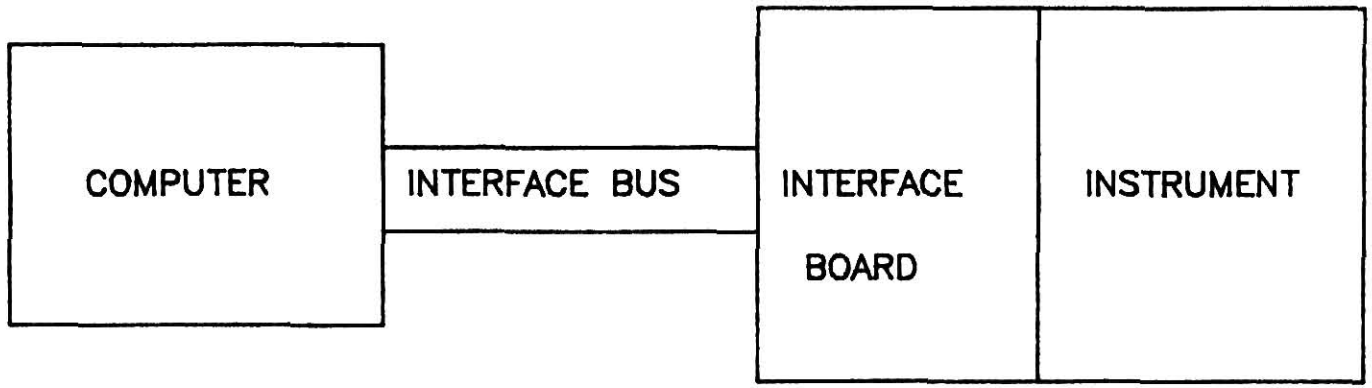


Figure 1. BLOCK DIAGRAM FOR INTERFACE SCHEME

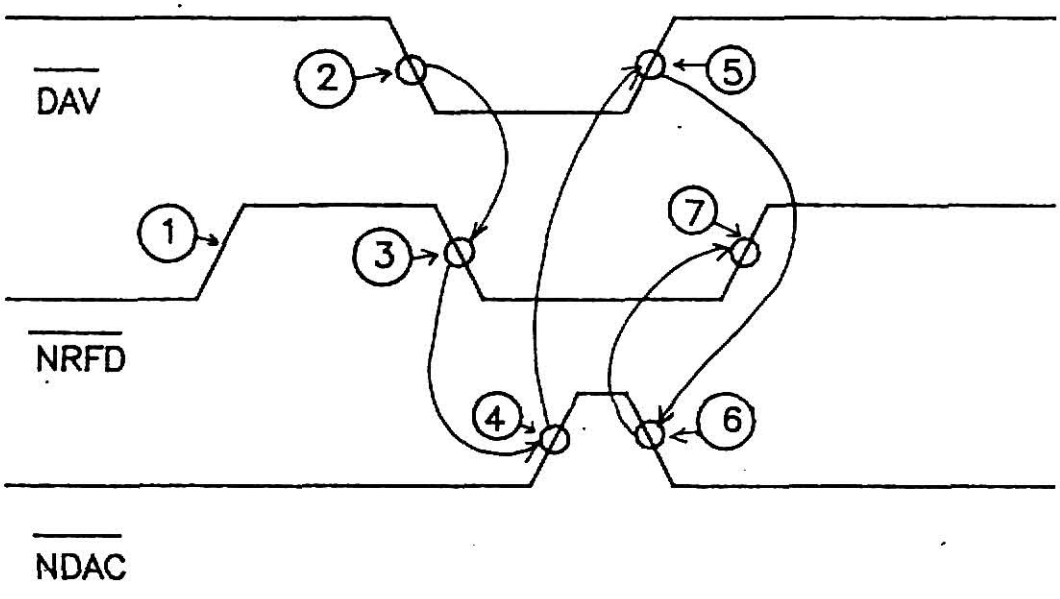


Figure 2. GPIB HANDSHAKE TIMING DIAGRAM

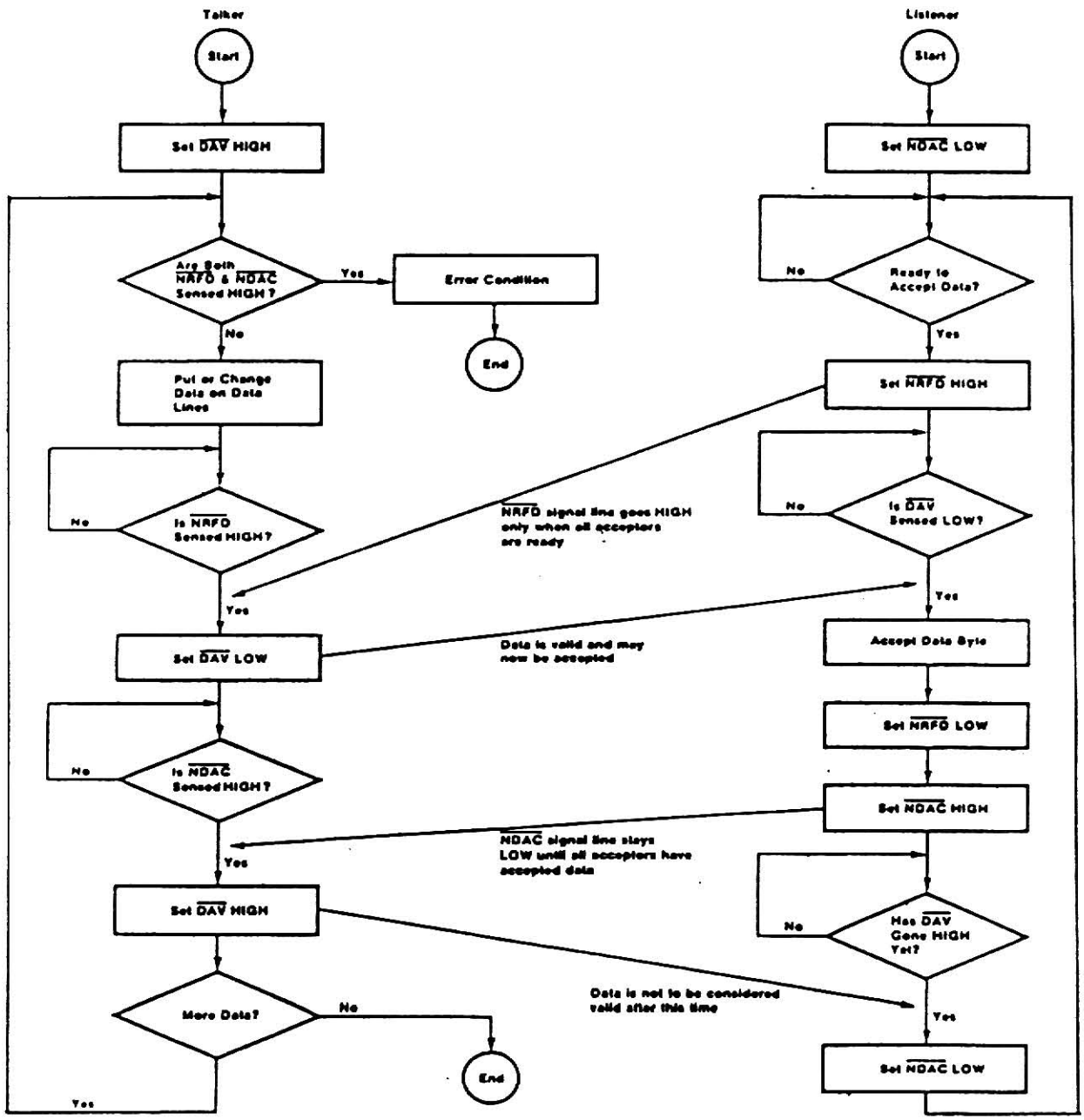


Figure 3. TALKER AND LISTENER HANDSHAKE LOGIC

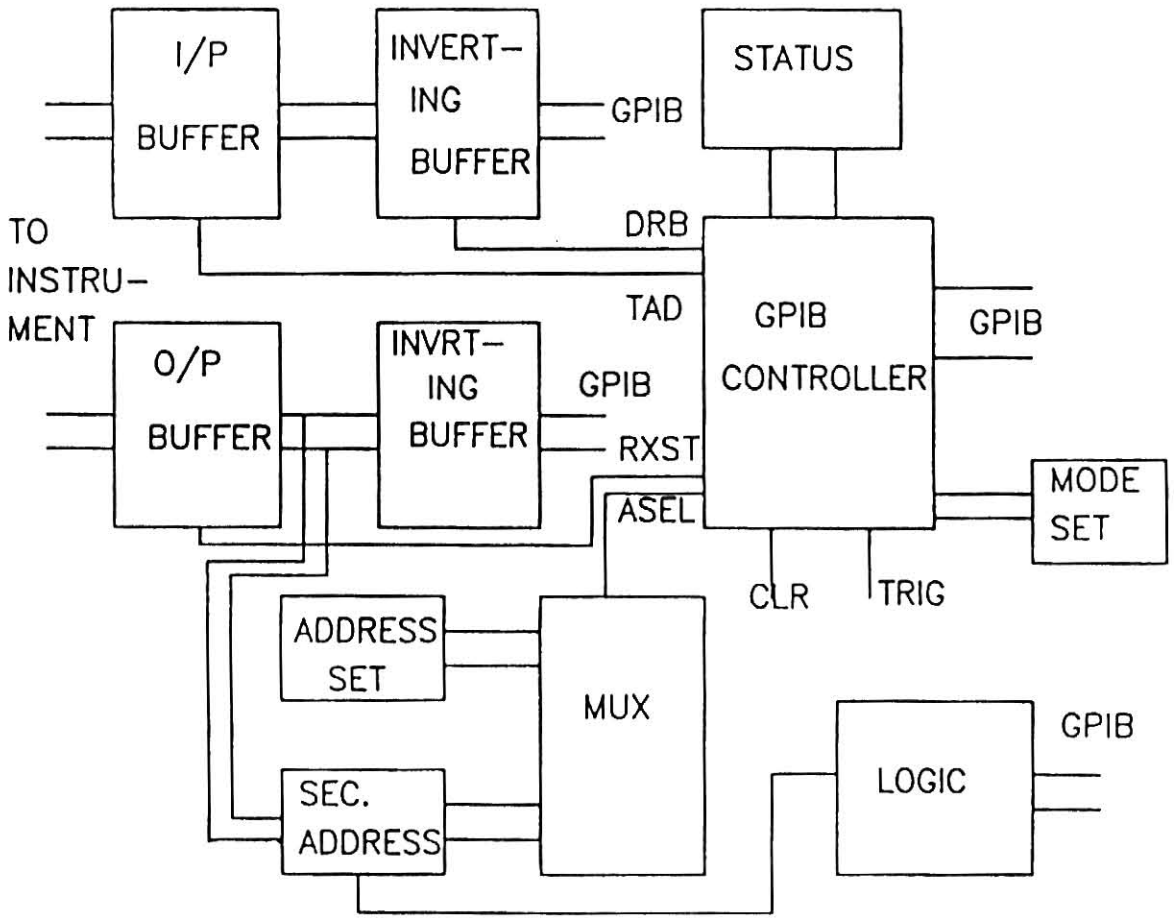


Figure 4 . BLOCK SCHEMATIC

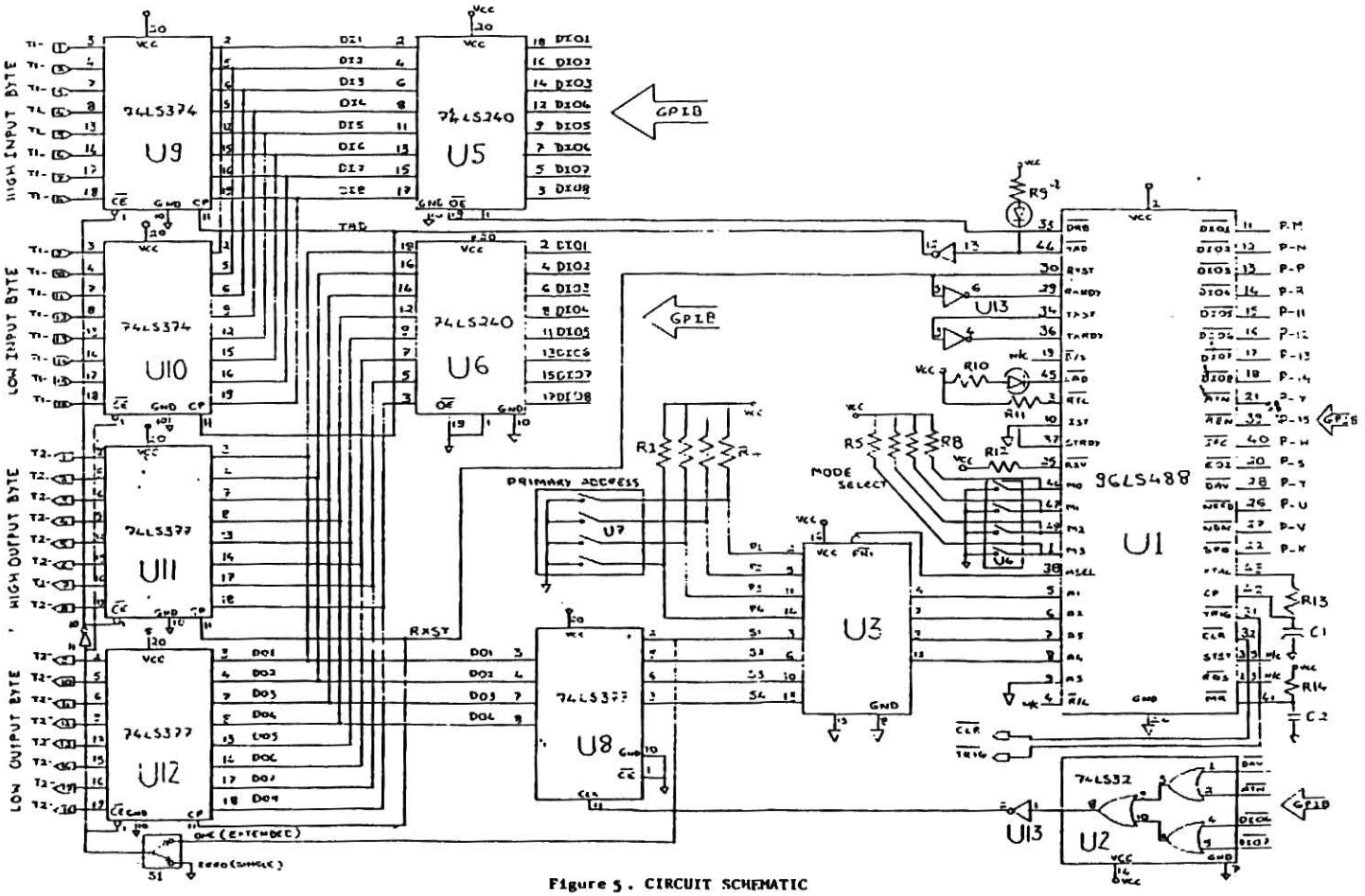


Figure 5. CIRCUIT SCHEMATIC

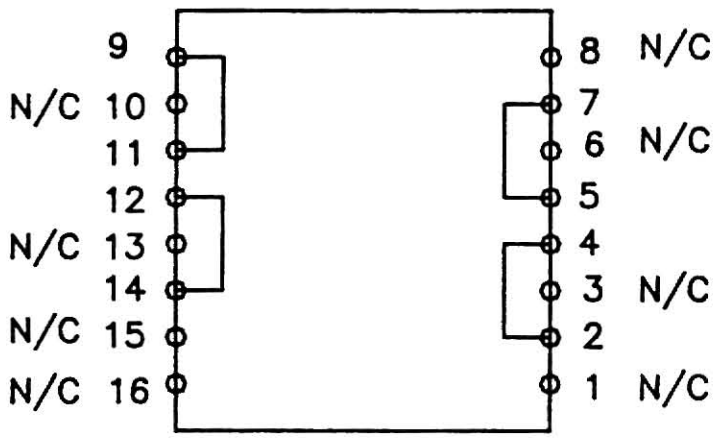
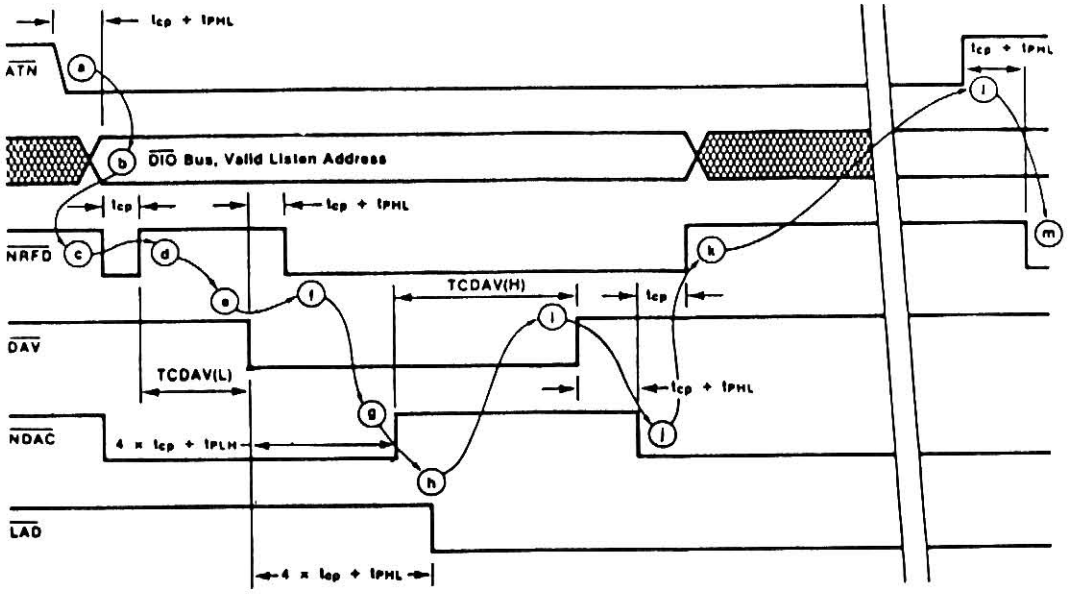


Figure 6. IC HEADER DETAILS



Note: ATN, DIO Bus & DAV driven by controller
NRFD, NDAC Driven by 96LS488

Figure 7. LISTEN ADDRESS SEQUENCE TIMING DIAGRAM

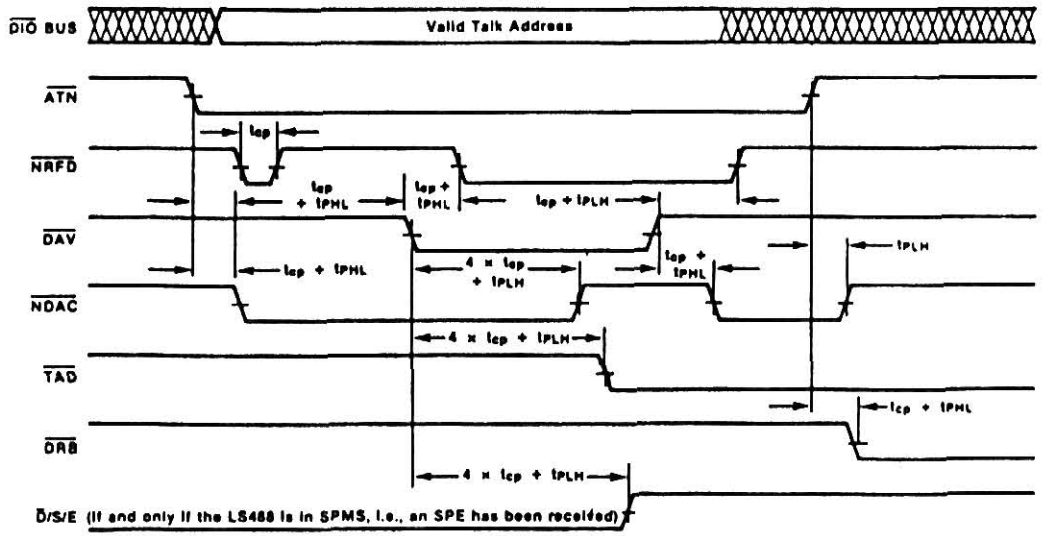


Figure 8. TALK ADDRESS SEQUENCE TIMING DIAGRAM

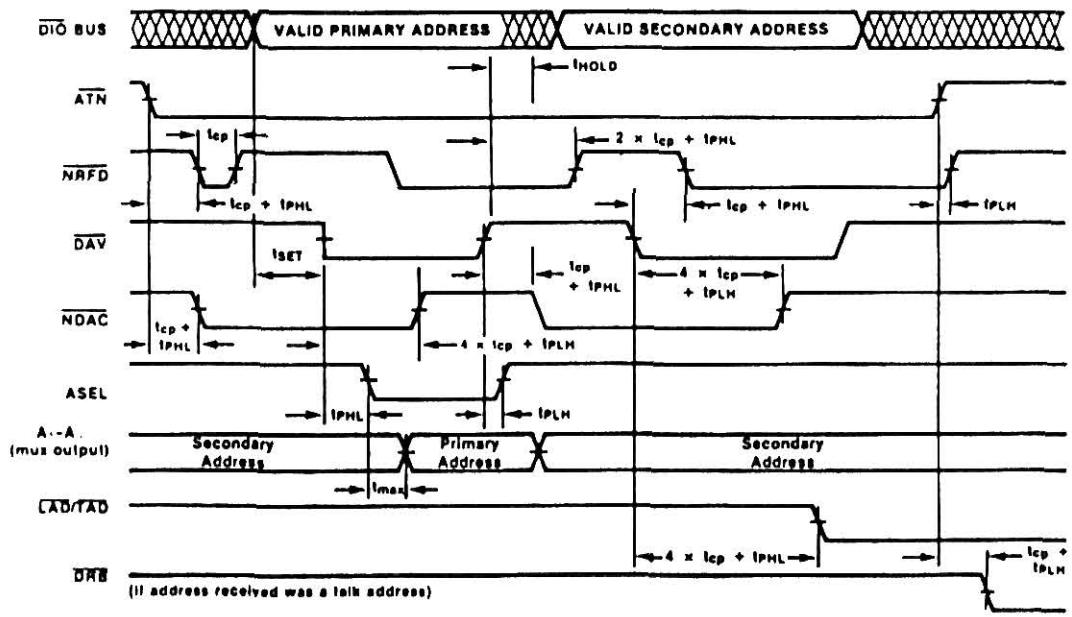


Figure 9. SECONDARY ADDRESS SEQUENCE TIMING DIAGRAM

GPIB INTERFACE FOR TESTING AND CONTROLLING LABORATORY PROJECTS

by

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B.E., College of Engineering, Pune, India, 1982

AN ABSTRACT OF A MASTER'S REPORT

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1986

ABSTRACT

A major performance improvement can be accomplished by including a digital computer within a system for testing and controlling an instrument. The inclusion demands a suitable interface between the computer and the instrument. This report discusses design and construction of an interface board that provides all the necessary interfacing and control functions between HP9845B and a variety of laboratory instruments.

The board can be programmed to operate in a desired communication mode and at a desired instrument address. The available communication modes include off-line, talk only, listen only, talk/listen single address, and talk/listen extended address. The board will enable us to test and control a variety of laboratory instruments, especially students' circuits. The board is simple to program and easy to operate.