SWITCHING CIRCUITS FOR A FERRITE CORE STORAGE

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INTRODUCTION

In the last decade the electronic computer industry has expanded at a rate comparable to the rapid development of radar during World War II. Even the laymen are acquainted with "mechanical brains" that predict election results far in advance of the final counting.

Some of these machines are probably the most complex pieces of equipment of any kind ever assembled which have to operate as a single centrally coordinated system.[1] They are, however, made up of familiar circuitry using familiar building blocks such as resistors, condensers, vacuum tubes, magnetic cores, and transistors.[2] The manner in which these familiar items are combined together to make up the completed electronic computer is the thing that is complex and unique to the computer.

Electronic computers are classified as analogue or digital computers. In the analogue computer the parameters are generally represented as voltages, while in the digital com-

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[1] W. Buchholz, "The Computer Issue," Proc. I.R.E., Oct. 1953, 41:1220.

[2] A. L. Samuel, "Computing Bit by Bit or Digital Computers Made Easy," Proc. I.R.E., Oct. 1953, 41:1223.

puter the parameters are represented by an ordered sequence of digits.

The information and discussion that follow in this thesis will apply to components of the digital computer. The functions or operations of a digital computer can be thought of in terms of three basic operations other than amplification, regeneration, and filtering.

The first operation of the basic three is switching. Switching can be thought of as changing the arrangement of information in space. It is merely connecting two things together such as a particular reading station to a counter or a storage position.

The second basic operation is storage or memory. Storage can be thought of as changing the time sequence of information. The storage retains information or holds it until it is needed for some operation, such as calculation or writing out.

The third basic operation is translation. Translation can be thought of as changing the value of information. An example of translation is a change in coding, such as changing from the binary system to the decimal system for read-out.

Leaving the operation of translation and concentrating on the operation of switching and storage, it is found that while the two are discussed as separate entities they are seldom separated from one another except for physical arrangement. Most switching devices will contain some form of information storage and likewise most memory devices will contain some

form of switching.[1] Ordinarily, the switching device feeding the storage will depend upon the type of storage used.

The present-day computer is limited in data handling capacity and speed. Capacity of data handled is dependent upon the storage devices in the computer, while the speed of operation is mostly dependent upon the switching associated with the storage. Most large capacity storage units in use today have slow switching devices associated with them and the use of a fast switching device seems to require a memory with a limited capacity.[2] There is a definite need for a storage of large capacity incorporating a fast switching mechanism. The primary purpose of the research conducted in preparation of this thesis was to survey and evaluate possible switching mechanisms for a relatively new memory device. A brief description of the most common memory devices along with their advantages and disadvantages will be helpful in showing the merits of the system chosen.

The delay-line memory is in common use at the present time. Basically, it is a delay element in a recirculation path or closed loop that circulates information until it is needed. The delay line can be an acoustic delay such as the mercury tank, magnetostrictive, and piezoelectric delay lines. These devices use transducers at the read-in and read-out ends, and

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[1] A. L. Samuel, "Computing Bit by Bit or Digital Computers Made Easy," Proc. I.R.E., Oct. 1953, 41:1228.

[2] Loc. cit.

therefore have a large attenuation during read-in and read-out. The attenuation in the medium, however, is very low. The delay line can also be an electric delay such as the distributed parameter and the lumped parameter delay lines. Neither type is as efficient space-wise as the acoustic delay lines and while their attenuation is negligible at the input and output, they have large signal attenuation in the line.[1] The disadvantages of delay-line memories are the awkward amount of access time and the amount of terminal equipment involved.[2] The access time is determined by the length of delay.

In the electrostatic type memory system the surface redistribution, holding beam, and selectron systems have good potentialities. The surface redistribution depends upon secondary emission from the screen of a cathode-ray tube. The secondary emission by itself, however, is not enough to give a binary type storage. Two patterns, such as a dot and a doughnut-type circle with the diameter of the hole equal to the diameter of the dot, are chosen to represent the "0" and "1" of the binary system. If the reading pattern is a circle and the stored pattern on the screen is a circle, it will remain a circle when it is read. The charge on the screen will change very little in this example. If the stored pattern is a dot, the reading pattern will change it to a circle. This change from one pattern to the other will change the charge on the

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[1] J. P. Eckert, "A Survey of Digital Computer Memory Systems," Proc. I.R.E., Oct. 1953, 41:1397.

[2] Loc. cit.

screen. The change can be read by placing a wire mesh close to the screen which will act as a condenser.[1]

The holding-beam system of electrostatic storage uses two levels of charge on the inside face of the tube rather than different patterns. In addition, it maintains these charges by spraying the face with a defocused beam of electrons from a separate holding gun. Generally, separate guns are used for reading and writing because the cathode of the reading gun is much more negative than the writing gun. A capacitor discharge type reading is again used. The magnitude of the discharge current is determined by the level of charge placed on the selected area during write-in. This system requires a rather expensive tube using three electron guns.

The selectron is a very complex type storage, particularly in its physical construction. Only a very general explanation will be attempted here. The selectron is made up of a number of cathodes with a storing eyelet for each cathode between the cathode and a fluorescent screen. Between the eyelets and the cathodes are horizontal and vertical selecting bars. These bars will isolate all the eyelets except the desired one by applying a negative pulse to the proper selecting bars. Between the eyelets and the fluorescent screen are a writing plate and a reading plate. The eyelets have a characteristic that they can be at either of two stable potentials. The writing plate determines which of the two levels will be stored in

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[1] J. P. Eckert, "A Survey of Digital Memory Systems," Proc. I.R.E., Oct. 1953, 41:1398.

the selected eyelet. One of these levels is near cathode potential. Electrons can pass through a .02-inch hole in the eyelet, only if the eyelet is at the more positive than cathode level. When the reading plate is pulsed positive, electrons that pass through a selected eyelet are accelerated to the fluorescent screen. Secondary emission occurs which is picked up on nearby output wires.[1]

The magnetic drum, a memory system widely used for digital computers, uses the same principle as tape recording for storage. The system consists of a cylindrical surface, with a coating of either powdered oxide or electroplated solid metal, rotating under read-write heads. The heads are in a row along the drum so that each head makes a "track" as the drum rotates under it. A track is the total number of cells (area of a single bit of information) under a single head. Each track holds information entirely separate from the other tracks.[2]

The most common method of putting information on the drum is called the "return to zero" method. In this system all the cells are put in the zero state by applying a negative pulse to the write winding of the head as the drum makes a complete revolution. The head may have three windings, one a read winding, one a write "0" winding, and one a write "1" winding, or the head may have only one winding with the associated circuitry separating the pulses. All the cells now are in the "0"

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[1] J. P. Eckert, "A Survey of Digital Computer Memory Systems," Proc. I.R.E., Oct. 1953, 41:1400.

[2] Ibid., p. 1401.

state, and any one of them may be changed to the "1" state if a pulse is sent through the write "1" winding at the instant the cell is under the head. This magnetizes the cell in the positive direction. On the read-out, the positive magnetized cell gives a positive voltage pulse at the output.

A memory system made up of magnetic cores was the system chosen for the research of this thesis. Basically, this system consists of small magnetic cores that remember in which direction they have been magnetized. The detailed explanation of the system will be given in a separate section.

A very promising system similar to the magnetic core memory is the ferroelectric cell. The cell is constructed by placing ferroelectric material between two plates. The ferroelectric material has a square hysteresis-like characteristic similar to the magnetic cores except the variables are D (electrostatic flux density) and E (electric field intensity), instead of B (magnetic flux density) and H (magnetic field intensity). Once the cell has been charged in one direction and the charging voltage reduced to zero, it maintains this charge until an opposite or negative voltage is impressed upon it. The cell then holds the negative charge resulting from the negative voltage. The construction of a working cell is similar to the magnetic cores. The ferroelectric material is placed between strips at right angles to each other. This forms a matrix of individual memory cells occurring at the intersections of the strips. Most of the advantages and disadvantages of the magnetic cell also apply to the ferroelectric

cell system.

A comparison of some important characteristics, such as destruction on read-out, destruction in case of power failure, destruction in event of drifts in the locating system, the resolution problem, and the time span of the memory, as given by Eckert, is shown in Fig. 1 in the Appendix.

CORE CHARACTERISTICS

As mentioned in the introduction, the fact that magnetic cores remember in which direction they have been magnetized is the basis of the magnetic core memory. The factor that enables the cores to remember is the residual magnetism that remains after the cores have been magnetized and the magnetizing current has returned to zero. Referring to Appendix Fig. 2, a core left at point B will be considered in the "0" state, and point E will be called the "1" state of core. A positive field strength or H_m applied to a core in the "1" state will move the core from point E to point A and then to point B as H_m goes to zero. If the core were in the "0" state, it would have moved from point B to point A and then back to point B for the same applied field strength. The first case would give a large change of flux, but the second case would give only a very small change of flux if the hysteresis loop were nearly square. The same results would be obtained if a negative H_m were applied to a core in the "0" state, and then the "1" state. This change of flux, going from one state to the other, is the

basis of using the cores in both memory and switching applications.

From the above discussion and Appendix Fig. 2, it can be seen that the squareness of the hysteresis loop is an important factor. If the loop were a perfect square, going from B to A or E to D would give no flux change. This would be ideal because the voltage induced from this small flux change is a non-switching or error voltage. To measure the squareness of the hysteresis loop, the squareness ratio ($R_s = B_d/B_m$) is used. B_d is the point of residual magnetism, or point B in Fig. 2, and B_m is the point of saturation or point A. R_s can be increased in many materials by operations that tend to align the directions of easy magnetization parallel to the applied field. Magnetic anneal, grain orientation, and application of stresses are used to increase R_s.

Another important factor to be considered in the use of magnetic cores in switching units and memory units is the time required to switch the cores from one state to another. The switching time is defined by Menyuk and Goodenough as, "The time required to change the induction in a core from its remanent value in one direction to a value corresponding to a driving field strength H_m greater than H_c in the opposite direction." H_c is the coercivity of the material. The time of switching is determined by the domain walls, that is, how fast the domain walls will move.

In order to understand domain walls, one goes back to the fact that the spinning electron has a magnetic moment. In fer-

romagnetic materials the atoms have their electrons oriented so that there is a resultant magnetic moment. In diamagnetic materials the magnetic moments of the electrons cancel each other in a single atom. In addition to this small magnetic moment from the atom, a ferromagnetic material has its atoms grouped together in small, irregular volumes called domains. These domains are randomly oriented in an unmagnetized material so that there will be no resultant magnetic moment. When a field is applied, those domains which have their magnetic moments more nearly in the direction of the applied field will grow at the expense of other domains. To allow this changing in size, the domain walls separating adjacent domains must move. Since the walls exhibit properties of mass and stiffness, they are subject to damping.

Menyuk and Goodenough[1] state that the time required to move the domain walls a distance "d" is $T = \beta_a / [2(H_m - H_o) \cdot I_s]$. H_m is the driving field, H_o is the threshold field strength at which the velocity is zero, I_s is the spontaneous magnetization, and β is the viscous-damping parameter. For normal memory applications $(H_m - H_o) \approx H_c$, where H_c is the coercive force. H_c is the demagnetizing force necessary to remove the residual magnetism B_r and return B to zero. As H_c is increased, the switching time T is decreased, but H_c is limited by power restrictions.

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[1] N. Menyuk and J. B. Goodenough, "Magnetic Materials for Digital-computer Components," Jour. of Applied Physics, Vol. 26, No. 1, Jan. 1955, p. 8-18.

The viscous-damping parameter is made up of β_e and β_r, where β_e results from the presence of eddy currents, and β_r results from the relaxation time. Relaxation time is the time required for the atomic spins to respond to an external force tending to change their direction. The effect of eddy currents can be reduced by the use of cores constructed by wrapping ceramic bobbins with thin metal tape (1/8-mil thickness has been used successfully), or by the use of cores formed by the molding of powdered materials (the ferrites used in this experiment are an example).

Reducing the distance between walls to reduce switching time can be accomplished by increasing the number of domains. It can be seen that the switching time can be varied by composition and method of preparation of magnetic cores.

CONSTRUCTION

The magnetic core memory was the first unit constructed. General Ceramic "S-1" cores with dimensions of .080 inch outside diameter, .050 inch inside diameter, and .025 inch thick, were used for the memory. Sixty-four cores were used to make an eight by eight unit, in which the cores were supported by the "x" and "y" read-write wires running through the cores. The wires were stretched between eight-position terminal strips mounted on a 4-inch square piece of Plexiglas. Since the read-out winding was to link all cores, the cores were staggered on the "x" and "y" read-write wires so that the axis of each core

was 90 degrees to the axis of the adjacent core. By staggering the cores, the error voltages induced in the read-out winding by the nonselected cores would cancel each other rather than add up to a very large voltage. A single wire was laced back and forth through every core, and it was then connected to two separate terminals for reading out of the cores. The wire used in the memory unit was size 34 lacquer-coated copper wire.

The final choice for the switching circuits was to have six cores feeding six of the eight "y" read-write wires, and two cores feeding two of the eight "x" read-write wires. The cores used were General Ceramic "S-1" with dimensions of .375 inch outside diameter, .187 inch inside diameter, and .125 inch thick. Each core had two 20-turn windings on the primary side and a one-turn winding on the secondary side. The primary and secondary windings supported the cores between terminal strips mounted on Plexiglas. The six cores and the two cores were mounted on separate pieces of Plexiglas.

The memory unit and the two switching units were all mounted on a piece of plywood. Connections were made between the output of the switch cores and the chosen read-write wires of the memory unit.

A three-ohm resistor was used in each connecting wire to reduce the L/R time constant of the circuit. A single-pole, double-throw switch was added in the connecting wire from the secondary of one of the "y" switching cores. This was necessary to show the output of the memory system with only half

the necessary excitation on the memory cores.

The method of selecting particular switching cores is shown by the schematic in Fig. 12 (Appendix), and will be explained later. From this schematic it can be seen that four separate current pulses are needed to supply A_y, A_x, B_y, and B_x. These current pulses must be square waves with amplitudes of about 350 ma. To obtain the desired pulses, it was decided to originate a pulse cycle by flipping a toggle switch. As shown in the circuit diagram in Fig. 11 (Appendix), the screen voltage is the voltage source to switch S_1. The voltage resulting from flipping switch S_1 is differentiated and fed to the grids of the nonconducting tubes in the multivibrators. These are one-shot multivibrators, and only one pulse will occur at the output from one flip of the switch. The output is base clipped, peak clipped, and amplified by two 6L6's in parallel to give the desired square-wave current pulse. Since each of the two multivibrators feeds two amplifiers, the result is the necessary four separate current pulses. Switch S_3 was added to prevent the A_y and A_x pulses during the restore cycle.

The units constructed are shown by the photographs in Plate I.

PRELIMINARY INVESTIGATION

One of the first unknowns that had to be determined was the number of ampere-turns required to saturate the switching cores. This value was calculated first and then checked by

EXPLANATION OF PLATE I

Fig. 1. Close-up of the switch and memory devices.

Fig. 2. Close-up of the current drivers.

Fig. 3. Over-all view of the experimental equipment.

PLATE I

Fig. 1.

Fig. 2.

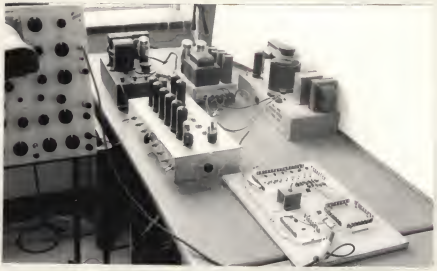

Fig. 3.

plotting a curve. Three 10-turn windings were wound on a core. A 20-kilocycle current of 10 milliamperes was applied to one winding, a varying direct current was applied to the second winding, and the third winding was used as an output winding. The output was fed to one oscilloscope for amplification and then to a second oscilloscope where the output was read as vertical deflection. Figure 3 in the Appendix shows a plot of deflection versus direct-current milliamperes for 10 ma and 20 ma of 20-kilocycle current. The graph shows that the steep portion of the hysteresis loop (the point where $H = H_c$) occurs at about 2.4 ampere-turns. This compares with the value of 2.67 obtained by calculation. The value of H_c given by General Ceramics was used in the calculations shown below.

$$H = \frac{NI}{2\pi R}$$

$$NI = (2\pi)(.1405)(3.03)$$

$$NI = 2.67$$

$R = .1405$ inch

1 oersted = 2.021 NI/inch

H_c = 1.5 oersted, or 3.03 NI/inch

The desired value of ampere-turns falls between the values that give $H = H_c$ and $H = 2H_c$, or 2.67 NI and 6.3 NI. From the graph, the slope of the curve indicates that 5 NI should give almost complete saturation; therefore, this was the value of ampere-turns chosen.

To obtain the large value of magnetizing force necessary to saturate the ferrites, a compromise between the number of

turns in the windings and the amount of current had to be made. Increasing the number of turns increases the interwinding capacitance as well as the inductance in the circuit. This can cause ringing effects, and will also increase the time constant of the circuit. In addition to the functional effects, as the number of turns increases the physical construction of the unit becomes more difficult. The size of the current is also limited if the compactness and complexity of the circuitry are concerned. A current of 250 ma in 20-turn windings was believed to be the best compromise.

After choosing the current and number of windings, the next step was to survey and evaluate the possible methods of switching. The various methods considered were combined into different categories. They were first grouped by the number of windings on the primary side. The output to the memory core was considered the secondary winding.

Two methods of switching were considered in the group with two windings on the primary. This is the least possible number of windings.

The first method requires two simultaneous pulses on a core before it will switch. This means that each winding must supply one-half the magnetizing force necessary to switch the core. In the discussion that follows, the number of turns will be considered constant and the current will vary. The current necessary for switching will be called I_m; therefore, in this case, each winding will carry $I_m/2$. It can be seen that the error voltage will be due to a value of $I_m/2$ in the

unselected switch cores, and will be rather large. The number of driving tubes required will be one for each vertical row of switch cores and one for each horizontal row of switch cores. Restoring the cores both initially and after switching would be rather complicated in this set-up.

The second method of switching with two windings uses the inhibit principle. All the cores in a row but one are biased with a $-I_m$ in the second winding. When I_m is put into the first winding, only the core not biased will switch. This scheme requires a full I_m of current in the windings, but gives a small error voltage since the two I_m's cancel in the non-selected cores. The same number of tubes is required as in the first method, but they must give twice as much current. Restoring is a simple matter. It can be accomplished by energizing only the inhibit windings.

Three methods of switching made up the group having three windings on the primary. The simplest of the three uses the third winding only to restore the cores. This is the same as the first method discussed in the two-winding group with a third winding added to restore the cores.

The second method considered is similar to the first except that currents of I_m are used in all three windings. The third winding is used as a bias winding and a restore winding. This winding can carry constant direct current so that all cores have a $-I_m$ bias in the quiescent state. To switch a core, both of the other two windings must be energized. One winding will cancel the effect of the bias winding, and the

second winding will switch the core. As the switching current pulses go to zero, the switch cores will be restored by the bias winding. This method has the advantage of smaller error voltages over the first method but requires tubes that carry twice as much current.

In the third method, the third winding is used to switch all cores properly set up by the first two windings. In this case each winding will be energized with $I_m/3$. The third winding will link all the cores, and any core that has its other two windings energized will be switched when the third winding is energized. This method has the disadvantages of large error voltages in the nonselected cores and does not have a simple method of restoring the cores. It has the advantages of smaller current requirements and more flexibility in timing of current pulses.

Another method of switching that cannot be grouped because the number of windings depends upon the number of cores, is called the commutator system.[1] This system is optimum as far as the number of tubes is concerned. The number of cores switched is equal to 2n where n is the number of stages of flip flops. Figure 4 (Appendix) shows the last six cores of the 16 cores that can be switched by four stages of flip flops. Each core has eight windings, (A, B, C, D, E, F, G, and H), with the polarity as shown. If tubes I, III, V, and VII are con-

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[1] J. Rajchman, "Static Magnetic Matrix Memory and Switching Circuits," RCA Review, June 1952, 13:183-201.

ducting, then core 16 is the only core that has four windings energized in the same direction with no windings opposing. If each winding carries $I_m/4$, then only core 16 will be switched. In this case the largest error voltage will be in cores 12, 14, and 15, and will be due to $I_m/4$ in two windings. An alternate to this method is to eliminate all the negative windings, so that each core will have only four windings. The current must again be $\frac{I_m}{4}$, and the error voltage will be $3/4\ I_m$. The error voltage is larger in this method.

From the evaluation of the various methods of switching, it was decided that the second method in the three-turn winding group had the most potentiality. Since only six "y" switching cores and two "x" switching cores were to be used, some modifications were made to this system. By arranging the six cores so that each of three drivers in the "y" direction fed two cores, and then biasing one of the two cores, when a pulse from a driver was received only one of the cores would switch. In this case the bias source can be a flip flop so that either set of three cores can be biased. Restoring can be accomplished by triggering one tube in the flip flop and then triggering the second. Only two sets of windings were needed on the primary. The purpose of this modification was to demonstrate the possibility of doubling the number of cores for the same number of driver tubes by adding a fourth winding that would isolate one-half of the cores. Each driver tube would feed twice as many cores.

In order to obtain some actual switching information prior

to complete construction of the memory system, two switch cores were wound separately and one memory core was driven by the two switch cores. Figure 5 (Appendix) shows the arrangement used.

It was first decided to use direct current in the bias winding and control it from a toggle switch. It was found that this method was not practical because even though the suddenly applied direct current restored the switching cores, it did not restore them fast enough to produce a large enough voltage to restore the memory core. It was decided that the bias winding should be energized with a current pulse at the same time and of the same amplitude as the driver current pulse. The bias pulse was made longer than the driver pulse to prevent switching after the bias pulse.

After setting up the additional pulse sources, readings were taken to plot the curves shown in Figs. 6, 7, 8, 9, and 10 (Appendix). The circuit in Fig. 5 shows the location of the different readings.

The curves shown in Fig. 6 are for the voltages taken at points A and B. Switch S was open, so that the voltages read were the primary voltages with an open secondary. The curves show that the switching time decreases with increasing current. Increasing the current is the same as increasing the $(H_m - H_o)$ term discussed under core characteristics. The peak voltage increases as the current increases. This is because the change of flux is increasing and the change of time is decreasing in the formula for induced voltage, as $e = \frac{d\phi}{dt}$.

Figure 7 shows the primary voltage taken at the same place

as Fig. 6 with the same conditions, except in Fig. 7 the cores were not switching. The voltage induced is due to the flux change going from B to A and then back to B on the hysteresis loop shown in Fig. 2.

The next set of curves shown in Fig. 8 were taken at points A and B with switch S closed. The resistors in the secondary were not yet added, and the secondary was practically short circuited. This increases the L/R time constant of the circuit, and, as shown by the curves, the cores are not completely switching. At this point it was suggested that resistance be added to the secondary circuit.

The conditions for the curves in Fig. 9 are the same as in Fig. 8 except that a one-ohm resistance was added in the secondary circuits. The curves show the results as expected, in that the switching time was reduced from 8 microseconds to 2.2 microseconds. The area under the curve is now the same as for the case with an open secondary. This means that the flux change is the same in both cases since complete switching is being achieved. The area under the curve in Fig. 8 is not as great, which indicates that there is insufficient time to allow a complete flux change.

Since the current is the important factor in switching the cores, the voltage drop across the one-ohm resistor was measured and the curves are shown in Fig. 10. Using the 383-ma current curve, it can be seen that the current to the small memory core is 2.2 amperes peak. By calculations, the current needed to overcome the coercive force is .6 ampere. Therefore

about one ampere would be a desirable current for driving the memory cores. Since this current is fed from two sources to the memory core, only .5 ampere is needed from each switch core and more resistance can be added to the one ohm in the secondary of the switch core. A value of three ohms was chosen for the final configuration.

DISCUSSION OF FINAL SWITCHING CIRCUIT

After completion of the preliminary investigation, circuit diagrams were made of the proposed system. The system was then constructed and the existing troubles were eliminated. Most of the troubles found were eliminated by proper grounding and by reduction of wire lengths where possible.

Figures 13 and 14 (Appendix) show the circuit diagrams of the one-shot multivibrator and current amplifier used to obtain the desired driving current. The complete over-all circuit for obtaining the current pulses is shown in Fig. 11 (Appendix). Most of this circuit was explained in the construction section.

The diagram in Fig. 12 (Appendix) shows the over-all wiring of the switch cores and the memory cores. For an explanation of the operation of the system, the condition will be considered in which switch cores Y_1 and X_1 will be switched. Switch S_2 is set to position one, switch S_3 is closed, and wafer switch S_4 is set to position two. The closing of switch S_1 originates a current pulse from all four amplifiers. Since

S_2 is at position one, amplifier A_y will send a current pulse through the windings of cores Y_1 and Y_2 of sufficient amplitude to switch the cores. At the same time, due to the setting of S_4, amplifier B_y sends a current pulse through a second winding of cores Y_2, Y_4, and Y_6. This current pulse is also of sufficient amplitude to switch the cores, but the windings are in the opposite direction to those energized by amplifier A_y. The resultant flux change in core Y_2 will be zero, the field strength in cores Y_4 and Y_6 will be in such a direction as to change the state of the cores from point E to point D on the hysteresis loop, and the field strength in core Y_1 will change the state of the core from point E to point A. As explained previously, this will cause a large voltage to be induced in the secondary of Y_1, a small voltage to be induced in the secondary of cores Y_4 and Y_6, and no voltage will be induced in the secondary of core Y_2. Amplifiers A_x and B_x will cause the same conditions in cores X_1 and X_2 with X_1 switching.

Since Y_1 and X_1 have been switched, current will flow in their secondary windings of half enough amplitude to switch the small memory cores. The core located at the intersection of the output wires of Y_1 and X_1 will receive sufficient ampere-turns to change its state from point E to point A on the hysteresis loop. All the other cores on the output wires of Y_1 and X_1 will receive only half enough ampere-turns, and their state will end up slightly above E. The switched cores will end up at point B on the loop, which is considered the "0" state of the cores.

To restore the switch cores, the cycle is again originated but S_3 is first opened and S_4 is changed to position three. This time only amplifiers B_y and B_x will be conducting, so current will flow in one winding of the cores Y_1, Y_2, Y_5, and X_1. This will change the state of all four cores to point D on the hysteresis loop and back to point E as the current goes to zero. The switch cores are now in the "1" state, ready for another cycle.

As the switch cores are returned to their "1" state, the voltage induced in their read-out windings is in the opposite direction to that induced when the cores were switched to the "0" state. The memory core at the intersection of their output windings will also be returned to its "1" state since the current flow through its windings is in the opposite direction.

The sequence of operation just considered is called the read cycle since the cores involved were returned to their "1" state. If the memory core were in the "1" state at the start of the cycle, a voltage would have been induced in the read-out winding as the memory core was switched to the "0" state, and a voltage of the opposite polarity would have been induced in read-out winding during the restore cycle to the "1" state. If the core had been in the "0" state at the start, only the voltage resulting from the restore cycle would be present in the read-out winding. It can be seen that the state of the memory core can be indicated by either reading the presence or not of the first induced voltage, or by combining the two voltages so that the resultant is zero in the first case but not

in the second case.

Although this experiment was not conducted to evaluate read-out principles, it is well to note that the sum method or integration type read-out method has the advantage that the error voltages from nonswitching memory cores will cancel out in this type read-out. These error voltages can be big in large matrixes.

The write cycle is the same as the read cycle, except that the switch cores are restored separately if it is desired to write a zero in the memory core. To write a "0" into a core, the same procedure is used as in the read cycle to put the memory core in the "0" state. To restore the switch cores in this case, two separate restore cycles are required. S_4 is set on position six for the first cycle and on position seven for the second restore cycle. This will restore core Y_1 on the first cycle and core X_1 on the second cycle. Since the output of one switch core by itself is not enough to switch a memory core, the core will be left in the "0" state as desired.

Figures 15, 16, and 17 (Appendix) show sketches of voltages observed at various locations in the final configuration. Since this was a single cycle system, the wave forms were not visible on the screen of the oscilloscope long enough to allow photographing.

Figure 15, parts (a) and (b), show the voltage across the 10.3-ohm resistors in the amplifier circuits. These are the current pulses in the primary windings of the switch cores. The current pulses from the B_x and B_y amplifiers are of a

longer duration for the reason explained previously. Parts (C) and (D) of Fig. 15 show the voltage across the primary of the switch cores during switching.

The current resulting from the switching and restoring of the switch cores is shown in parts (A) and (B) of Fig. 16. These are the voltage drops across a 3-ohm resistor in the secondary of switch core Y_1. It can be seen that a peak current of .6 ampere was obtained from each switch core. It can also be seen that the core was switching in 1.5 microseconds.

The output of a memory core is shown in parts (C) and (D) of Fig. 16. A peak voltage of around .3 volt was obtained on the switching cycle and about .2 volt on the restore cycle. The difference in peak voltage is probably due to difference in current pulses. The areas under the curves are about the same. These curves show a switching time of .3 microsecond.

Figure 17 shows the outputs from a memory core obtained during a write-read cycle. Curve (A) shows the output obtained by switching a memory core to the "0" state during the write cycle. Curves (B) and (C) show that a very small voltage is induced during the restore cycles of the switch cores. Curve (D) shows that the core was in the "0" state since no output voltage was obtained in the first half of the read cycle. Curve (E) shows the negative output voltage obtained as the memory core is restored to the "1" state during the last half of the read cycle.

CONCLUSION

With the use of ferrite cores in both the memory device and the switch device, a relatively simple memory system was built in which binary information was stored and read out. The simplicity of the system was shown by the fact that the system functioned by originating single current pulses from the closing of a toggle switch. This also showed that the function of the system was not dependent on time.

The time required for a complete cycle, however, is important in the consideration of an over-all computer system. The time required for switching the cores determines the speed at which the system can be operated. In this experiment, switching times of about two microseconds were obtained. This switching time shows the disadvantage of using the ferrite core as a switching device, rather than thin wraps of mo-permalloy on a bobbin. The switching time is inversely proportional to the driving current. The coercivity of ferrite is much greater than for mo-permalloy, and a greater driving field strength is needed to overcome this coercivity. For the same ampere-turns, the mo-permalloy will switch much faster and give a larger induced voltage in the secondary. A high coercivity is essential in the coincidence pulsing of the memory core because it determines how large the output from a single switch core can be without switching the memory core.

The large driving current requirement of the switch cores

presents a problem in driver tube design, particularly where compactness is a necessity. One method used to reduce the current requirement of the driver tube is to put a pulse transformer between the driver tube and the switch core. This will also reduce the windings on the primary of the switch core.

The ferrite cores used in this experiment as switching devices may also be incorporated in gating circuits preceding the switch cores. In addition, circuits have been designed that use the cores as counting devices and pulse generators.[1]

The results of the research on the switching circuits show how successfully magnetic cores will function in this application. The cores have indefinite life, are small in size, use little power, and are very reliable. Various switching circuits were considered and many more exist. This means that for any application there will probably be some type of switching circuit that will function satisfactorily.

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[1] S. S. Guterman and W. M. Carey, Jr., "A Transistor-Magnetic Core Circuit; A New Device Applied to Digital Computing," I.R.E. Convention Record, Part 4, 1955, p. 84-94.

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APPENDIX

	DESTRUCTION				
	READ OUT	POWER FAILURE	LOCATING SYSTEM DRIFT	RESOLUTION PROBLEM	LIMITED TIME EXISTENCE
DELAY LINE	YES	YES	YES	YES	YES
SURFACE RECIRCULATION	YES	YES	YES	YES	YES
HOLDING BEAM	NO	YES	YES	YES	NO
SELECTRON	NO	YES	NO	NO	NO
MAGNETIC DRUM	NO	NO	NO	YES	NO
FERROMAGNETIC CELL	YES	NO	NO	NO	NO
FERROELECTRIC CELL	YES	YES	NO	NO	NO

Fig. 1. Comparison of memory systems.

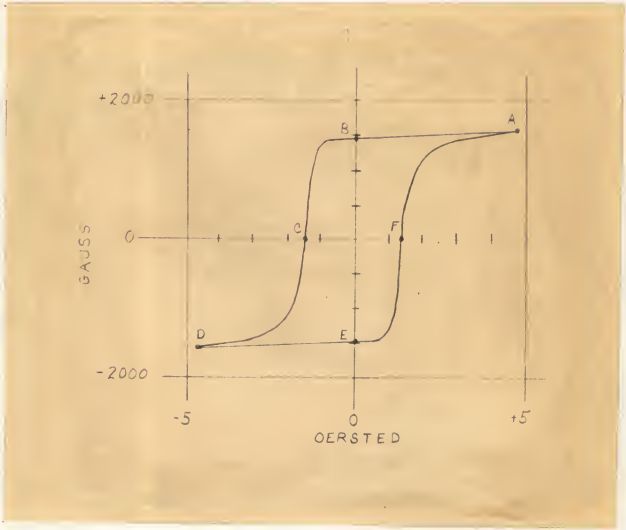

Fig. 2. Typical hysteresis loop.

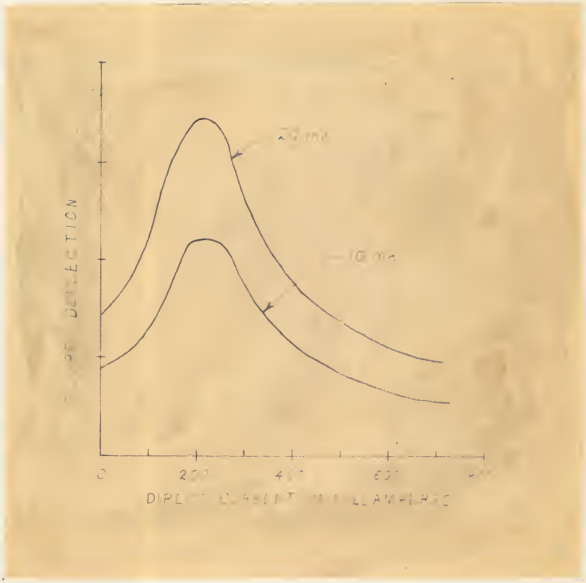

Fig. 3. Curves for determining saturation.

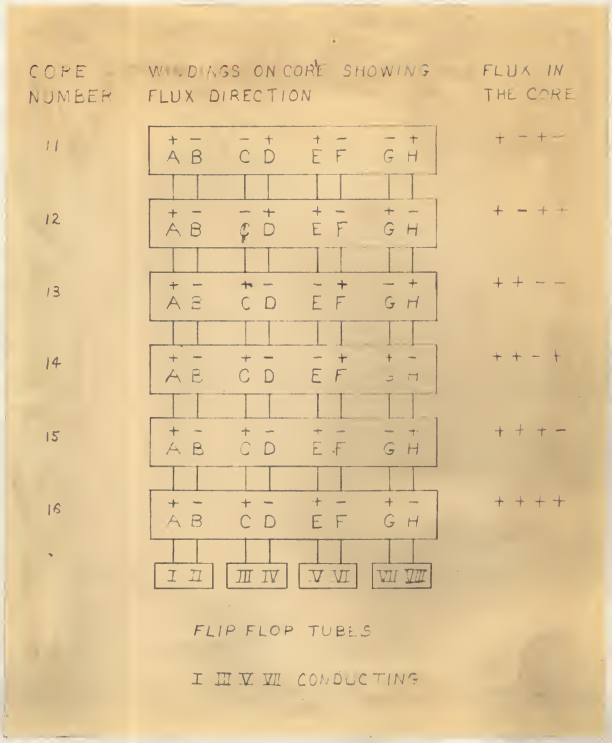

Fig. 4. Commutator winding.

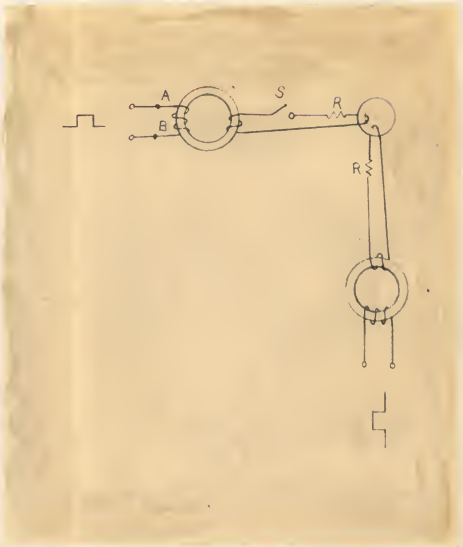

Fig. 5. Circuit to obtain preliminary data.

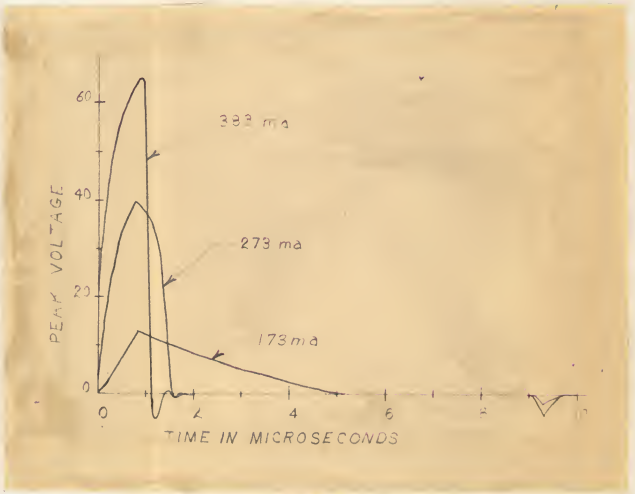

Fig. 6. Primary voltage with an open secondary.

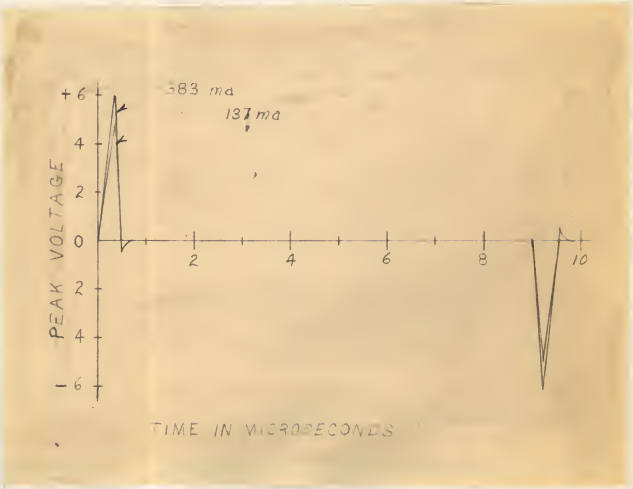

Fig. 7. Nonswitching primary voltage with an open secondary.

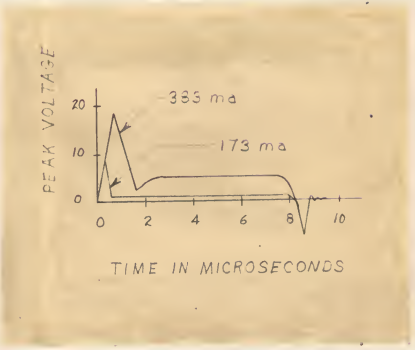

Fig. 8. Primary voltage with a memory core loading the secondary.

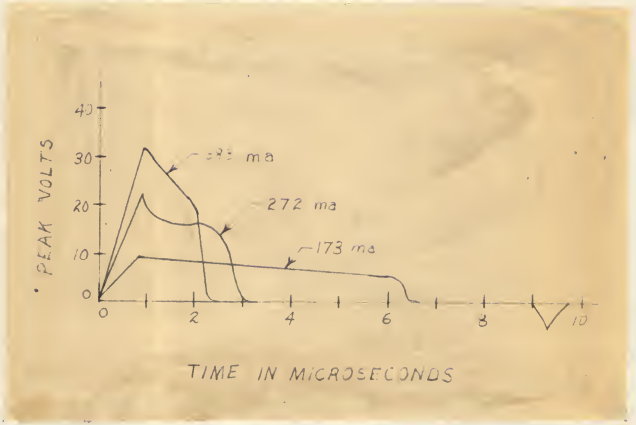

Fig. 9. Primary voltage with one ohm in the secondary.

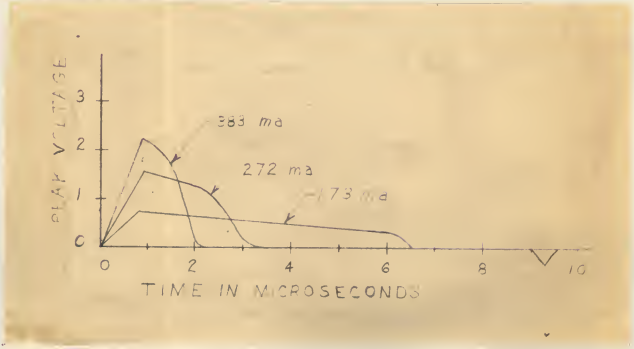

Fig. 10. Voltage across a one-ohm resistor in the secondary.

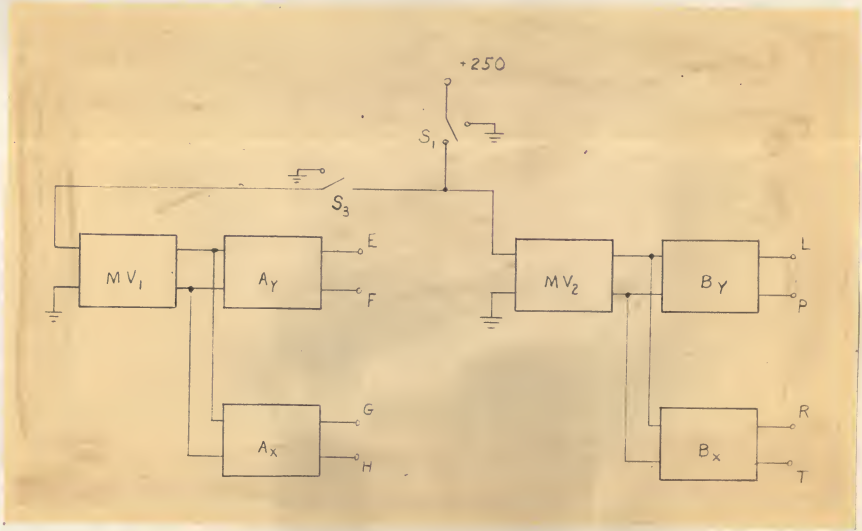

Fig. 11. Block diagram of drivers.

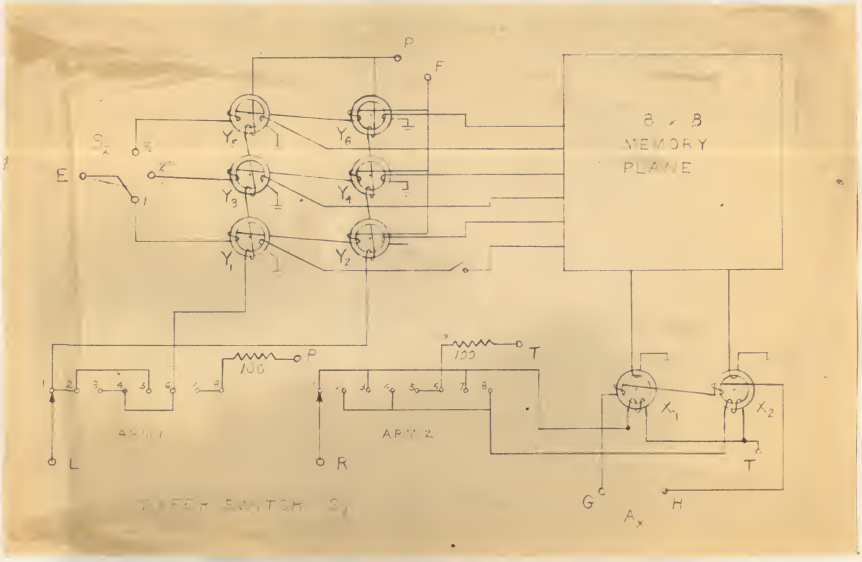

Fig. 12. Circuit diagram of switch cores.

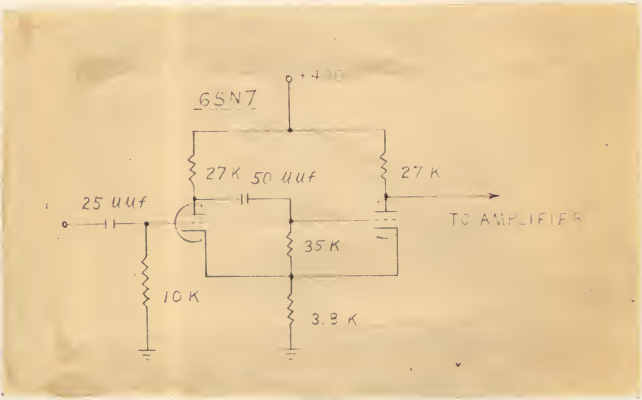

Fig. 13. Multivibrator.

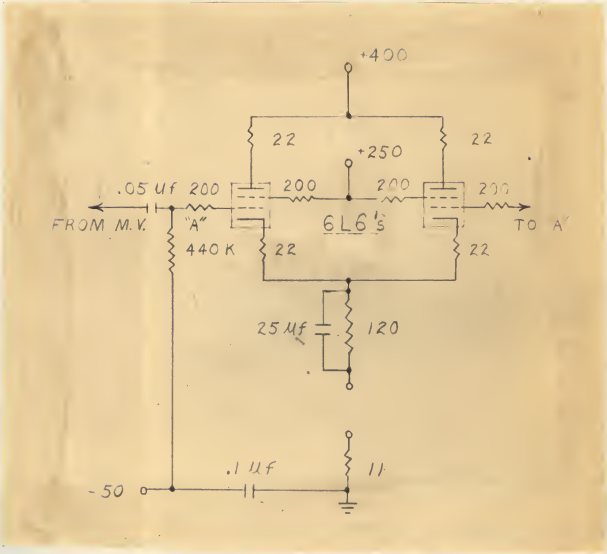

Fig. 14. Current amplifier.

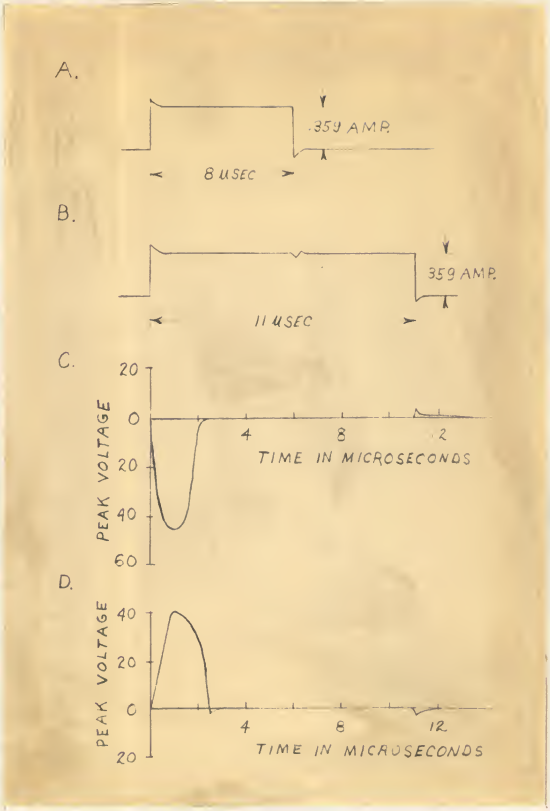

Fig. 15. (A) Current from amplifiers A_x and A_y. (B) Current from amplifiers B_x and B_y. (C) Voltage across the primary of a switch core during switching. (D) Voltage across the primary of a switch core during restoring.

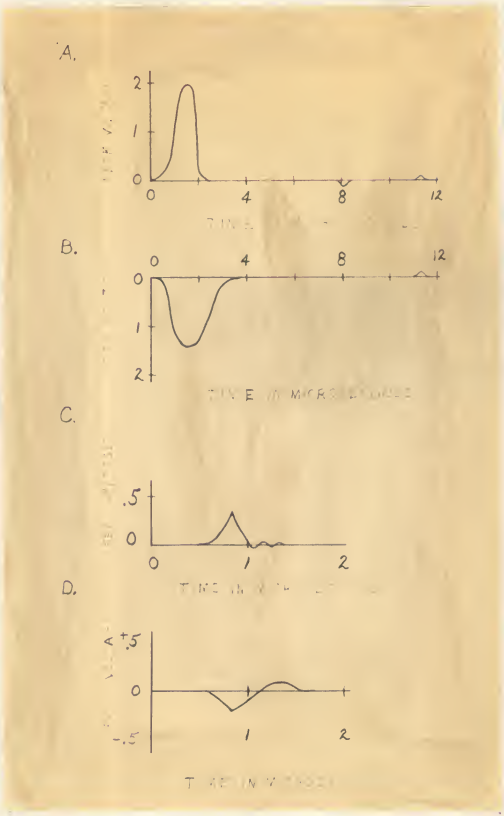

Fig. 16. (A) Voltage across a 3-ohm resistor in the secondary of a switch core during switching. (B) Voltage across a 3-ohm resistor in the secondary of a switch core during restoring. (C) Voltage in the memory read-out during switching. (D) Voltage in the memory read-out during restoring.

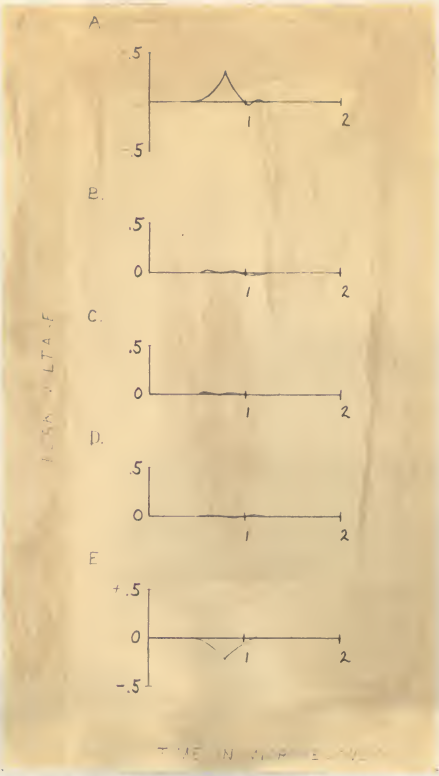

Fig. 17. (A) Voltage in the memory read-out during the switching of two switch cores simultaneously. (B) Voltage in the memory read-out during the restoring of one switch core. (C) Voltage in the memory read-out during the restoring of the second switch core. (D) Voltage in the memory read-out during the switching of the same two switch cores. (E) Voltage in the memory read-out during the restoring of the two switch cores simultaneously.

SWITCHING CIRCUITS FOR A FERRITE CORE STORAGE

by

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ABSTRACT OF
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OF AGRICULTURE AND APPLIED SCIENCE

1956

ABSTRACT

The purpose of the experiment was to survey several methods of using magnetic switch cores to drive a ferrite core memory matrix, construct the system that showed the most potential, and obtain experimental data for evaluation.

Since ferrite cores were available in the correct size for switch cores, it was decided to use them instead of cores made up of thin wraps of metal. After deciding upon the cores, it was necessary to do research on their characteristics. The magnetomotive force required to switch the cores was determined by the research.

In surveying the various methods of using the ferrite cores as switches, these factors were considered: the number of driver tubes required; the current required per winding; the size of unwanted voltages from nonselected cores; the complexity of the logic circuits needed to switch and restore the cores; and the complexity of core winding. The system chosen was a modification of a system that uses three primary windings per core with each winding supplying sufficient magnetomotive force to switch the core. One of the windings supplies a negative magnetomotive force for restoring the core and for canceling the effect of one of the other two windings. A core will switch only if the two positive windings are energized simultaneously.

A memory plane was constructed using 64 ferrite cores in

an 8 by 8 matrix. The driving sources were constructed next so that experimental data could be taken from two switch cores driving a single memory core. The amount of resistance needed to obtain the desired L/R time constant was determined from this setup. Sufficient information was obtained from the single core tests to complete the construction of the switching circuit.

The final circuit functioned satisfactorily for a binary storage system. The outputs of the selected memory cores were about 200 mv, while the outputs of the half-selected cores were estimated to be about 15 mv. The wave forms of voltages taken at various points in the final circuit showed that the memory cores were switching in less than one microsecond and the switch cores were switching in about two microseconds. The ferrite switch cores used in this experiment require a large driving current to obtain the switching time mentioned. An even larger drive current would be required to reduce this switching time. This is a disadvantage in using ferrite cores as switch cores.

The satisfactory results obtained in this experiment from the simple circuit used, the known reliability of magnetic devices, and the reasonable cost of magnetic cores are advantages that should give magnetic core switch devices an important part in future computer development.