

A grinding-based manufacturing method for silicon wafers: decomposition analysis of wafer surfaces

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Abstract

It is difficult for the lapping-based manufacturing method currently used to manufacture the majority of silicon wafers to meet the ever-increasing demand for flatter wafers at lower costs. A grinding-based manufacturing method for silicon wafers has been investigated. It has been demonstrated that the site flatness on the ground wafers (except for a few sites at the wafer center) could meet the stringent specifications for future silicon wafers. The generation mechanisms of the dimples and bumps in the central areas on ground wafers have also been studied. This paper reports another study on the grinding-based method, aiming to reduce the cost of chemical-mechanical polishing – the final material removal process in manufacturing of silicon wafers. Using design of experiments, investigations were carried out to understand the influences of grinding process variables on the peak-to-valley values of the polished wafer surfaces. It was found that the peak-to-valley values over the entire wafer surfaces did not show any relationship with grinding process variables. However, after analyzing the surface profiles by decomposing them into different frequencies, it was observed that there is a correlation between grinding process variables and certain surface feature components. Based on this finding, it is

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recommended to optimize the grinding process variables by minimizing the peak-to-valley values for each surface feature component, one at a time. This methodology has not been published for wafer grinding and is of practical use to the wafer industry.

Keywords: Grinding; Machining; Manufacturing; Polishing; Semiconductor material; Silicon wafer; Surface roughness.

1. Introduction

The impact of semiconductors on the economy and society is significant. The semiconductor industry generated the revenue of more than \$235 billion worldwide in 2005 [1]. A major factor for the huge growth has been the industry's ability to consistently increase product performance while decreasing the price [2]. Whether or not the semiconductor industry can maintain this ability in the future will largely depend on whether the wafer industry can supply wafers (more than 90% are silicon [3]) with increasingly better quality at reasonably low prices.

It is difficult for the lapping-based manufacturing method currently used to manufacture the majority of silicon wafers to meet the ever-increasing demand for flatter wafers at lower costs. A grinding-based manufacturing method for silicon wafers has been investigated and the results were published in three papers. The first paper [4] demonstrated that the site flatness on the ground wafers (except for a few sites at the wafer center) could meet the stringent specifications for future silicon wafers. The second and third papers [5,6] investigated the generation mechanisms of the dimples and bumps in the central areas on ground wafers, respectively, and provided solutions to eliminate or reduce them.

Chemical-mechanical polishing is the final material removal process in manufacturing of silicon wafers. It is slow, expensive, and detrimental to the environment. A lot of efforts have been exerted to reduce the polishing removal amount and much progress has been made. Nevertheless, further reduction in polishing removal is not only desirable but also necessary in order to further reduce the manufacturing cost of silicon wafers. However, it has become very difficult, if not impossible, to reduce polishing removal further from the current level due to the lack of understanding about the surface features on polishing feedstock wafers, the sources of each surface feature component of different frequency, and the responses of polishing to each surface feature component.

Previous studies [7-9] have shown that the curvature (or locus) of grinding marks (or grinding lines) and the line distance (the distance between adjacent lines) are determined by grinding process variables (wheel speed, chuck speed, and wheel diameter, etc.). Several mathematical models are available in the literature to predict the curvature [10-13] and line distance [11] of the grinding marks. Furthermore, experiments have shown that grinding process variables (such as wheel speed, chuck speed, and feedrate) also affect the effectiveness of polishing in removing the grinding marks [8]. However, no relationships have been established between the grinding process variables and the wafer surface quality (for example, wafer flatness and surface roughness) after polishing.

A literature search on the topic did not result in any reports about decomposition of the surface features on ground and polished wafers. Table 1 summarizes the results of the literature search. Numerous papers [7,9,11,14-54] reported studies on machined surfaces. In many of these studies [15,16,20,21,25-30,38-46,52], dimensional data on the machined surfaces were converted into the

frequency domain. However, only two papers reported decomposition of the surface features [15,52]. In only one paper [15], the decomposed surface features were correlated to the machining conditions for electrical discharge machining (EDM).

This paper presents an attempt to decompose the surface features on polished silicon wafers and to relate the individual feature components to the grinding process prior to polishing. The objective is to generate the necessary understanding and knowledge to further reduce the polishing removal, hence to lower the manufacturing cost of silicon wafers. The results will also be of value to wafer manufacturing of other materials such as gallium arsenide, germanium, sapphire, and silicon carbide. The methodology employed in this study can also be extended to improvement of surfaces machined by other processes.

2. Experimental conditions and results

2.1 Design of experiments

Single crystal silicon wafers having a diameter of 200 mm and the (100) planes as major surfaces were used. To block the possible effects of surface variations in the test wafers, all the test wafers (as sliced) were lapped with 7 μm aluminum oxide abrasive slurry and with same lapping removal (sufficiently large to remove the surface variations induced by slicing).

The grinding experiments were conducted at Strasbaugh Inc. (San Luis Obispo, CA) on a Model 7AF grinder. Fig. 1 illustrates the wafer grinding process. The grinding wheels are diamond cup wheels. The wafer is held on a porous ceramic chuck by means of vacuum. The rotation axis for the grinding wheel is offset by a distance of the wheel radius relative to the rotation axis for the wafer. During grinding, the grinding wheel and the wafer rotate about their own rotation axes simultaneously, and the wheel is fed towards the wafer along its axis.

The grinding wheels used were resin-bonded diamond wheels with a diameter of 280 mm. The grit size was mesh #320 for the coarse wheel and #2000 for the fine wheel. During grinding, deionized (purified) water was used to cool the grinding wheel and the wafer surface. The coolant was supplied to the inner side of the cup wheel, at a flow rate of 11.4 l min^{-1} (or, 3 gallon min^{-1}).

The process variables and their values for the coarse grinding are listed in Table 2. The intention was to study the effects of process variables in fine grinding. Therefore, the process variables for the coarse grinding were kept constant for all the grinding tests. For fine grinding, a 3^2 (two variables, three levels) full factorial design was employed to systematically change two process variables: feedrate and chuck speed. Table 3 shows the test matrix for fine grinding. The detailed description of factorial design can be found in many textbooks such as the one by Montgomery [55].

Under each grinding condition, five or more wafers were ground. However, only two wafers from each grinding condition were randomly chosen for double-side polishing. The reasons for not polishing all the ground wafers include the following. (a) The other ground wafers were saved for future studies based on the results of this study. (b) Polishing two wafers per test condition is less

costly than polishing all the test wafers. (c) The wafers ground under the same grinding condition exhibit virtually the same surface features. This practice of polishing only some of the ground wafers for each grinding condition has been used in several previous studies [4,8,56].

The identifications of the polished wafers are listed in Table 4. Wafers #1-9 were polished in one run and wafers #10-18 were polished in another run. About 5 μm thick of material was programmed to be polished off from each side of every wafer, using an identical polishing recipe. Note that these two sets of wafers were polished in two different runs on the same polisher. Although both runs used the same polishing recipe, some polishing variables were not identical, such as the condition of the polishing pad and the temperature of the polishing table. The differences in these variables resulted in a slight difference in the polishing removal amount. However, the difference in polishing removal amount would affect only the absolute peak-to-valley (PV) values on these wafers. It should not alter the relative comparison of the PV values on the wafers.

2.2 Measurements of wafer surfaces

A NanoMapper (ADE Phase Shift, Tucson, AZ), an automated surface mapping system, was used to inspect the polished wafers. It characterizes the wafer surfaces by providing whole wafer topography measurements, and measures surface height with sub-nanometer sensitivity. Further information on the NanoMapper technology can be found at the company's Web site (www.phase-shift.com).

2.3 Results of experiments

The peak-to-valley (PV) value for a wafer is the height difference of the highest point and the lowest point over the entire wafer surface. Note that no reference plane is necessary for such height difference. It was used in this study primarily because of the following fact. The wafer industry typically uses the maximum parameters instead of average parameters when describing the quality of a wafer. For example, wafer flatness is typically quantified by global flatness GBIR (TTV), the maximum deviation of the wafer surface from a reference plane over the entire wafer surface, or/and site flatness SFQR, the maximum deviation of the wafer surface from a reference plane over a site of certain size.

The PV values over the entire wafer surface for all the polished wafers (Wafers #1 to 18) are listed in Table 4. They were further processed, and the processed graphs will be presented and discussed later in the following section.

2.4 Necessity of decomposing the surface features

Fig. 2 plots the effects of feedrate and chuck speed (in fine grinding) on the PV values over the entire wafer surfaces. No consistent trends are observable on these graphs regarding to the effects of feedrate and chuck speed. In other words, no consistent trends can be observed on changes in the PV values as feedrate or chuck speed changes. For example, in Fig. 2(a), as the feedrate increases, the PV values increase for the wafers with the chuck speed of 0.28 rev s^{-1} , but decrease for the wafers with the chuck speed of 11.45 rev s^{-1} .

The above observation indicates that the feedrate and chuck speed in fine grinding are not the determining factors for the PV values over the entire wafer surfaces. Therefore, the PV values over the entire wafer surfaces (after grinding and polishing) cannot be used as the evaluation parameter to study the relationship between the grinding process variables (namely, feedrate and chuck speed) and the wafer surface quality.

The following section will show that, after decomposing the surface features into several components of different frequencies, consistent trends can be obtained for the effects of grinding process variables (namely, feedrate and chuck speed) on some feature components.

3. Decomposition methodology and preliminary results

3.1 Obtaining three circular profiles on each wafer surface

The first step to decompose the surface features on the test wafers was to obtain circular profiles along three circles on each wafer. As shown in Fig. 3, the three circles have the radii of 61.22 mm (R1), 72.79 mm (R2), and 83.22 mm (R3), respectively. As an example, Fig. 4 shows the circular profile for the circle of R3 on wafer #10. Note that both profiles in Fig. 4(a) (over the entire circle) and Fig. 4(b) (over 1/3 of the circle) are for the same profile. The profile shown in Fig. 4(b) is a zoomed view of the first 1/3 of that shown in Fig. 4(a).

The resolution of the data acquisition technique used in this study has 2,048 points for each circle (R1, R2, and R3). The distance between adjacent points is 0.188 mm for the circle of R1 and 0.255 mm for the circle of R3.

3.2 Transforming circular profiles to frequency domain using FFT

In order to gain an insight about the surface features, the circular profile data were transformed to the frequency domain using the Fast Fourier Transformation (FFT). Information on FFT can be found in many textbooks such as the one by Figliola and Beasley [57]. A commercial software, Matlab (MathWorks, Inc., Natick, MA, USA), was used to perform the FFT in this study. Fig. 5 shows the FFT graphs for some test wafers. Note that only the results on the circular profiles along the circles of R3 are presented in this paper in order to save the page space.

It can be observed that, for the wafers ground with the low chuck speed ($= 0.28 \text{ rev s}^{-1}$), there exists a high-frequency component in each of the three circular profiles. Furthermore, this surface feature component of high frequency (between 100 to 150 Hz), as marked in Fig. 5(a), is unique to the wafers ground with the low chuck speed. Wafers ground with higher chuck speeds do not have this high-frequency component, as shown in Fig. 5(b).

3.3 Filtering profile data to get high-frequency component

The next step was to filter the profile data to get the high-frequency component for every wafer ground with the low chuck speed ($= 0.28 \text{ rev s}^{-1}$). For the purpose of comparison, low-frequency

components were also obtained for these wafers. This filtering operation was performed by a program developed by the authors using Matlab.

The type of filtering used was the finite impulse response (FIR). The bandwidth was 1 KHz. The target frequency for the low-frequency component was the frequency window of [0, 150 Hz]. The target frequency for the high-frequency component was the frequency window of [150 Hz, 1000 Hz].

3.4 Effects of grinding process variables on high-frequency components

Fig. 6 shows the effects of feedrate (in fine grinding) on the PV values for the high-frequency surface feature component. A consistent trend can be observed between the two sets of wafers, and among the three circles (R1, R2, and R3). As the feedrate increases, the PV values increase.

As a contrast, Fig. 7 shows the effects of feedrate (in fine grinding) on the PV values for the low-frequency surface feature component. There are no consistent trends between the two sets of wafers, and among the three circles (R1, R2, and R3). Taking the example of wafers #1 - #3, as shown in Fig. 7(a), as the feedrate increases, the PV values increase for the circles of R1, but decrease for the circles of R3. Furthermore, as shown in Fig. 7(b), as the feedrate increases, the PV values decrease for the circles of R1 on wafers #10 - #12.

The above results indicate a promising approach to study the effects of grinding process variables on the wafer surface features after grinding and polishing. Consistent trends can be obtained only for the effects of the grinding process variables on the PV values of the high-frequency

component of the surface features. There are no consistent trends regarding their effects on the low-frequency component. Therefore, it is necessary to decompose the surface features of the ground and polished wafers, and optimize grinding process variables to minimize the PV values for each feature component, one at a time. After the PV values for every feature component are individually minimized, the optimum wafer surface will be obtained.

4. Conclusions

This paper reports an attempt to decompose the surface features of the silicon wafers (that have been ground and polished) into components of different frequencies, and to relate the individual feature components to the process variables in fine grinding. The major conclusions are:

- (1) Feedrate and chuck speed in the fine grinding process do not have determining effects on the peak-to-valley values over entire wafer surfaces.
- (2) After the circular profiles of the wafer surfaces are transformed into the frequency domain, there exists a high-frequency component unique to the wafers ground with the low chuck speed.
- (3) For this high-frequency component, there is a consistent relation between the peak-to-valley values and the feedrate. The peak-to-valley values increase as the feedrate increases.
- (4) For the low-frequency components, there are no consistent trends for the peak-to-valley values as the feedrate changes.

This study has illustrated that attempts to reduce the peak-to-valley values over entire wafer surfaces through optimizing grinding process variables (such as feedrate and chuck speed) would be fruitless. It has provided a promising approach to optimize the ground surfaces of polishing feedstock wafers. This approach involves decomposing the surface features into components of different frequencies and optimizing the grinding conditions to minimize the peak-to-valley values for each individual component, one at a time. The illustrated principle and methodology might be applicable to other machining processes and materials as well.

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