Electronic transport and low frequency noise in atomically thin graphene and hexagonal boron nitride two-dimensional heterostructure field effect transistors

by

Aroop K Behera

M.S., National Institute of Science Education and Research, India, 2018

AN ABSTRACT OF A DISSERTATION

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requirements for the degree

DOCTOR OF PHILOSOPHY

Department of Industrial and Manufacturing Systems Engineering
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KANSAS STATE UNIVERSITY
Manhattan, Kansas

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Abstract

Field Effect Transistors (FETs) form the basis for modern integrated circuits (ICs), that are the building blocks of every computing and communication device. The need for faster and energy efficient microprocessors has enabled continuous development of novel device architectures with the state-of-the art micro/nano-fabrication technologies, aiming for a transistor feature size of ≈3 nm and beyond. However, scaling down the device dimension below 3 nm brings added challenges due to various fundamental physical limits, thus demanding a paradigm shift in materials and device fabrication techniques. Two-dimensional (2D) atomically thin materials along with their heterostructures have shown exceptional electrical, optical, mechanical, thermal, and chemical properties that provide avenues to innovate newer and smaller devices with promise for delivering higher performance and energy efficiency. However, fundamental understanding of carrier transport in terms of their microscopic origin and their scattering mechanisms are necessary to elucidate the device physics of such 2D transistors. This dissertation work delves into the design and fabrication of 2D heterostructure graphene field effect transistor (2D-HGFET) devices, understanding their electrical transport properties by investigating various carrier scattering mechanisms, and characterize the fluctuations in the carrier transport by studying the electrical noise also called as *1/f* low-frequency noise. This dissertation work provides the first comprehensive study on the correlation between electrical transport and *1/f* noise in 2D-HGFET devices relating to graphene and hexagonal boron nitride materials. Both noise analysis and transport properties were used to estimate the trap energy levels in the devices.

The use of hexagonal boron nitride as the substrate and encapsulation material to a graphene conductive channel has been shown to produce high mobility transistors due to its similar crystal structure with minimal lattice mismatch, reduced impurities, lower interface trap states, and high difference in electrical conductivity. Furthermore, it has also

been demonstrated that one-dimensional electrical contacts (called "1D-edge contacts") to 2D-HGFETs provides high current injection with low contact resistances that are necessary for high performance devices. This dissertation employs 2D-HGFETs with 1D-edge contacts to study the electrical transport, *1/f* noise, and their correlation. Despite extensive transport measurements on heterostructure transistor devices, the coupling between atomic layers, particularly hBN and graphene, in terms of the phonon modes of hBN on electronic transport in graphene is in infancy. In this study, temperature dependent electrical transport and low frequency noise measurements were performed to understand the effect of phonon modes in hBN/graphene/hBN heterostructure and its conductance as 2D-HGFET device channel. The effect of LA phonons in graphene conductive channel is found to be the dominant carrier scattering mechanism at lower temperatures, whereas remote interfacial polar phonons in hBN dominate carrier scattering at elevated temperatures. Furthermore *1/f* noise in were modeled to the carrier-phonon scattering and the average density of trap states in hBN/graphene/hBN heterostructure systems were calculated from which the trap energy (both electronic and hole) were extracted. Finally, hBN/graphene/hBN heterostructure 2D-HGFETs fabricated using hBN crystals grown with isotopically pure Boron (i.e., ^{10}B and ^{11}B) and the systematic characterization of their transport and noise properties were also studied. 2D-HGFETs employing isotopically pure hBN show $\approx$ 3 to 4$\times$ reduction in remote interfacial phonon scattering compared to those using natural hBN substrates and encapsulation layers, leading to development of further ultra-high performance, ultra-low noise, and energy efficient graphene based 2D-HGFETs. The origin, impact, and engineering of the remote interfacial phonons on the electronic and noise characteristics constitute the most significant contribution of this dissertation and it provides further avenues for the investigation of engineered 2D heterostructures and their devices.

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List of Abbreviations

1D	One dimensional
2D material	Two Dimensional Material
CNP	Charge Neutrality Point
CVD	Chemical Vapor Deposition
DUT	Device Under Test
EBL	Electron Beam Lithography
EELS	Electron Energy Loss Spectroscopy
FET	Field Effect Transistor
finFET	fin Field Effect Transistor
GFET	Graphene Field Effect Transistor
hBN	hexagonal Boron Nitride
HEMT	High Electron Mobility Transistors
HFET	Heterostructure Field Effect Transistor
HGFET	Heterostructure Graphene Field Effect Transistor
HOPG	Highly Oriented Pyrolytic Graphite
LA	Longitudinal Acoustic
LAADF STEM	Low Angle Annular Dark Field STEM

LFN	Low Frequency Noise
LO	Longitudinal Optical
MOS	Metal Oxide Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NPGS	Nano Pattern Generation System
PC	Polycarbonate
PDMS	polydimethylsiloxane
PMMA	Poly methyl methacrylate
PPC	Poly-propelene carbonate
RF	Radio Frequency
RIE	Reactive Ion Etching
RIP	Remote Interfacial Phonon
SB-FET	Schottky Barrier Field Effect Transistor
SEM	Scanning Electron Microscope
SLG	Single Layer Graphene
SMU	Source Measurement Unit
SS	sub-threshold swing
STEM	Scanning Tunneling Electron Microscope
TA	Transverse Acoustic
TMD	Transition Metal Dichalcogenide

TO	Transverse Optical
VLSI	Very Large Scale Integration
VS2D	Vertically Stacked 2D Sheets
VSNS	Verically Stacked Nano Sheets

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Dedication

I dedicate this thesis in the memory of my father, Bijay Kumar Behera, who passed away in 2022. His words of wisdom, care and multiple sacrifices have made my career pursuit possible.

Chapter 1

Graphene and its Heterostructure with Hexagonal Boron Nitride

1.1 Motivation

Increasing demands for faster computing devices have been driving the semiconductor industry to manufacture smaller and energy-efficient logic units (CPUs) for current and future computing requirements. Since the invention of the first transistor in 1947, metal-oxide-semiconductor field-effect transistors (MOSFETs) have been the fundamental building blocks of CPUs. Moore's device dimension scaling and Denard's device power scaling have played pivotal role over the past decades to achieve a present-day MOSFET (called a fin-FET) of $\approxeq$ 3 nm feature size and subsequent ultra-scaled devices (e.g. vertically stacked nanosheet, VSNS, transistors) (see Fig. 1.1(a,b)).[1–3] This rapid reduction in the device dimensions has resulted in fundamental bottlenecks in the operational principles and fabrication of field-effect-transistors (FETs), such as quantum confinement, mechanical stability, parasitic resistance and capacitance, leakage currents, and short-channel-effects, thereby leading to device reliability issues (see Fig. 1.1(c)).[3;4] Therefore, a paradigm shift in achieving the next generation of materials and fabrication methodologies is necessary to develop the next generation of transistor devices.

A fascinating device architecture predicted to overcome the nodal size bottleneck of ≈ 3 nm is the vertically stacked 2D sheet (VS2D) structure, where 2D layers replace the Si-based conventional three-dimensional material in VSNS and behave as parallel transport channels (see Fig. 1.1(d)). These atomically thin nanosheets with their reduced quantum confinement, and better mechanical stability, promise to enable the future ≤ 1 nm nodal size FET architecture. Consequently, a plethora of 2D materials with different electronic properties have been explored. Recent discoveries have shown 2D nanosheets of semimetals, insulators, metals, semiconductors, superconductors, and magnetic nature such as graphene, hexagonal boron nitride (hBN), TaS_2, MoS_2, $NbSe_2$, to name a few, respectively, can now be used to fabricate 2D based heterostructure field effect transistors (HFETs) for different electronic applications.[5–11] More candidates are being added to the list of each of the mentioned categories, making them suitable for innovating novel 2D heterostructure field effect transistor devices (2D-HFETs). 2D transition metal dichalcogenides (TMDs) such as MoS_2 and WSe_2 show high ON/OFF ratios which makes them good candidates for logic applications but on the other hand display low electrical mobilities. Graphene however, shows ultra-high electrical mobility values ($\approx$ 140,000 cm^2/Vs at room temperature), making it 100 times faster than Si and 10 times faster than state of the art III-V semiconductors.[5;12] This property of ultrahigh electrical mobility makes graphene an appropriate material for future high electron mobility transistors (HEMTs) for radio frequency (RF) applications.[13–15] 2D insulators like hexagonal boron nitride (hBN) due to it's isomorphic crystal structure to graphene, atomically flat surface, and significantly reduced impurities is a good dielectric for the fabrication of 2D FETs. Morever, due to hBN's inert nature to the ambient environment, it can also be used as an encapsulating material to protect any reactive 2D nanosheets.[12]

The remainder of chapter 1 will introduce the electrical properties of graphene, specifically the electronic band structure and it's correlation to observed electrical properties. The chapter further delves into various GFET structures along with their importance for future RF transistors.

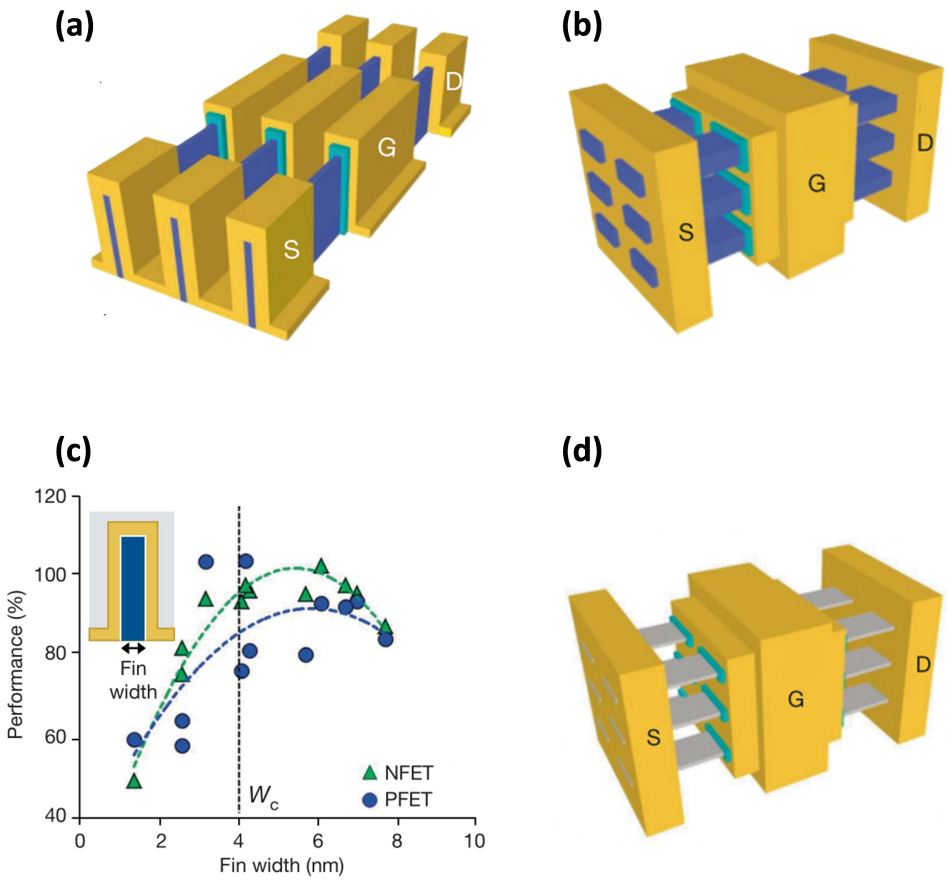


Figure 1.1: *Schematic diagram of finFET structure(a) and vertically stacked nanosheets(b). Performance of finFET as the function of fin width(c) and schematic diagram of vertically stacked 2D sheets (d). Wei Cao, Huiming Bu, Maud Vinet, Min Cao, Shinichi Takagi, Sungwoo Hwang, Tahir Ghani, and Kaustav Banerjee The future transistors, Nature, 620, 501-515, 2023, Reproduced with permission from Springer Nature*[3]*. X. He et al., Impact of aggressive fin width scaling on finfet device characteristics copyright IEEE 2017*[4]*.*

1.2 Graphene, its electronic band structure, and associated properties

All the descriptions made in this section and in this dissertation are related to a single atom thin graphene membrane unless otherwise specified. Graphene is a single layer of sp^2 hybridized carbon atoms that are arranged in a hexagonal honeycomb crystal structure (see Fig. 1.2(a)). This sp^2 hybridization in the graphene lattice creates strong σ bonds between the carbon atoms. These strong σ bonds in a single layer of graphene deliver exceptional

elastic properties which have been extensively studied through theoretical modeling and experiments.[16;17] Lee et al., in their study have used atomic force microscope nano-indentation to study the elastic properties of a suspended single layer of graphene.[18] Their study shows graphene has exceptional elastic stiffness of $\approx 340\pm50$ Nm^{-1}, which amounts to $\approx 1.0\pm0.1$ TPa. A simple comparison with the Young's modulus of silicon ($\approx$130 GPa) shows the extreme stiffness of a single layer of graphene by an order of magnitude.[19] Another similar study performed by Lee et al., shows the stiffness in a single layer of graphene through Raman spectroscopy which estimates the Young's modulus to be $\approx 2.4\pm0.4$ TPa.[20] 2D failure strength of 43 Nm^{-1} has also been measured by Lee et al., by nanoindentation measurements on a suspended graphene. A similar hypothetical thickness of steel shows 2D failure strength of 0.084-0.4 Nm^{-1}, which proves defect free graphene is 100$\times$ stronger than steel making it one of the strongest material. Furthermore, the unbonded delocalized electrons in the p_z orbitals in the lattice create interesting electrical properties. The electronic properties of a single layer of graphene can also be understood through electronic band formulation as follows: The carbon atoms in graphene can be visualized in a hexagonal lattice with two atoms per unit cell. The lattice vectors in graphene's unit cell are given by:

$$\begin{aligned} \vec{a_1} &= \frac{a}{2}(3, \sqrt{3}) \\ \vec{a_2} &= \frac{a}{2}(3, -\sqrt{3}) \end{aligned} \tag{1.1}$$

where a is the carbon-carbon bond distance $\approx$ 1.42 Å. The reciprocal lattice in graphene is also shaped in a hexagonal shape (see Fig. 1.2(b)) where the reciprocal lattice vectors are given by:

$$\begin{aligned} \vec{b_1} &= \frac{2\pi}{3a}(1, \sqrt{3}) \\ \vec{b_2} &= \frac{2\pi}{3a}(1, -\sqrt{3}) \end{aligned} \tag{1.2}$$

The first Brillouin zone and the corresponding high symmetry points for graphene in $\vec{k}$ space are shown in fig. 1.2(b). The vector $\vec{k}$ represents the wavevector associated with the electronic states in graphene where $\vec{k_x}$ and $\vec{k_y}$ represent the wavenumbers in $\vec{x}$ and $\vec{y}$ directions, respectively. The center of the Brillouin zone by convention is labeled as Γ corresponding to $\vec{k} = 0$ along with high symmetry **K** and **M** points on the edge of first Brillouin zone.

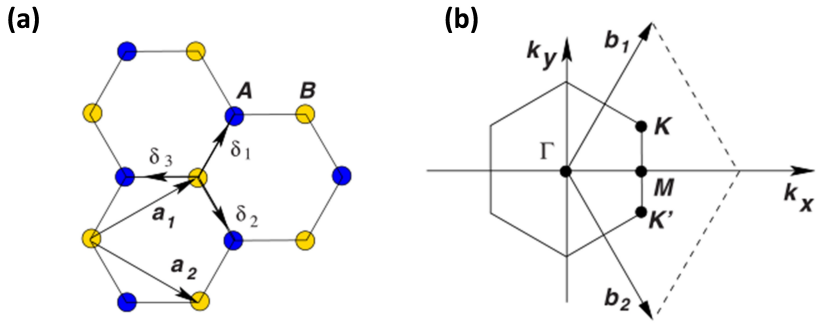


Figure 1.2: *Crystal structure of graphene(a) and the structure of graphene's first Brillouin zone (b). Reprinted figure with permission from [Castro Neto et al., Rev. Mod. Phys., 81, 109, 2009] Copyright (2009) by the American Physical Society*[21].

The electronic energy dispersion for graphene in the $\vec{k}$ space ($\vec{k} = (\vec{k_x}, \vec{k_y})$) is obtained by solving the tight-binding Hamiltonian for electrons that can hop between nearest and next-nearest atoms.[22] This energy dispersion follows as:

$$E_{\pm}(\vec{k}) = \pm t\sqrt{3 + f(\vec{k})} - t'f(\vec{k}) \tag{1.3}$$

$$f(\vec{k}) = 2cos(\sqrt{3}k_y a) + 4cos(\frac{\sqrt{3}}{2}k_y a)cos(\frac{3}{3}k_x a), \tag{1.4}$$

where the $\pm$ refers to the π^* and π bands corresponding to the conduction and valence bands, respectively (see Fig. 1.3). Fig. 1.3 shows the Dirac cones formed at **K** points in the first Brillouin zone, where the conduction band and valence band meet at a single point and exhibit linear dispersion in the vicinity of **K** points. This property of zero bandgap is the source of low ON-OFF ratios in graphene field effect transistors. Furthermore, the energy relations described in eq. 1.3 and eq. 1.4 near the **K** points resemble the energy of

ultrarelativistic particles that describe the electrons as massless Dirac fermions with Fermi velocity (v_F) close to the speed of light $\approx 10^6$ ms^{-1}. This massless nature of fermions in graphene renders ultra-high electrical mobility to the charge carriers hosted in the vicinity of **K** points. These interesting electrical properties of graphene can be further studied at an intricate level by fabricating graphene field effect transistors (GFETs) which will be introduced in section 1.3.

The relativistic nature of the Dirac fermions in a single layer of graphene also renders it interesting optical properties like discrete optical transparency that reduces with gradual increase in the number of atomically thin layers. A single and subsequent number of atomic layers of graphene absorb integer multiples of $\approx \pi\alpha = 2.3\%$ of the incident light, where $\alpha = e^2/\hbar c$ is the fine structure constant, $\hbar$ is the reduced Planck's constant, and c is the speed of light.[23] Nair et al., have performed optical transmittance measurements on samples with 1-5 layers of graphene and have found each layer absorbed 2.3% of incident light despite being atomically thick.[23] The absorption in a single layer is independent of the incident frequency and is a fundamental quantity described only by the fine structure constant.[23] Due to the above mentioned excellent mechanical stability, optical transparency, electrical, graphene is considered an interesting material for future electrical, thermal, and optical applications.

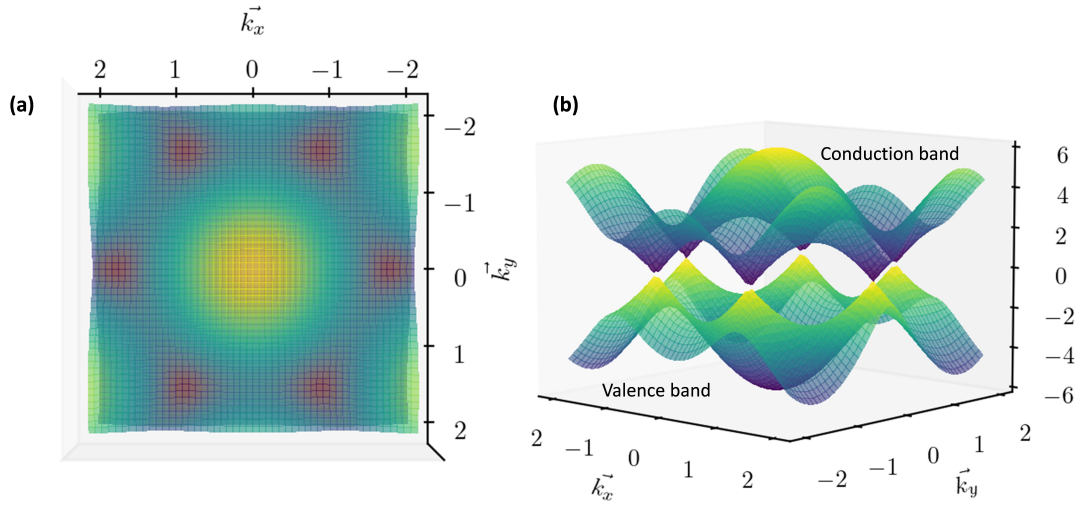


Figure 1.3: *(a) $E(\vec{k})$ in $\vec{b}$ space showing the six K points. (b) Energy plots showing the Dirac points for a single layer graphene.*

A single layer of graphene can be obtained by several different methods, each with its own advantages and disadvantages. Due to weak van der Waals interactions among graphene layers, a single layer of graphene can be mechanically exfoliated from graphite.[5] This method gives the best quality graphene with ultra-high mobility values, however the physical dimensions of a graphene flake obtained through this method are only a few micrometers. This renders micromechanical exfoliation unsuitable for large scale applications. Graphene can also be grown using chemical vapor deposition (CVD) and carbon segregation process on SiC substrates (epitaxially grown) in large wafer scale dimensions.[24–27] However, the electrical mobilities are lower in CVD and epitaxially grown graphene as compared to exfoliated graphene due to grain boundaries induced by growth procedures, rendering exfoliated graphene useful for fundamental investigations of graphene based materials and devices. Lastly, large area graphene can also be separated using chemical based exfoliation method, but has relatively poor quality and is not commonly used for high performance electronic device applications.[28] Table 1.1 below summarizes the mobility values in graphene devices where the graphene channel was obtained by different growth processes.

Table 1.1: *Graphene exfoliation processes*

Graphene Process	Mobility
Mechanical exfoliation	200 000 $cm^2/V.s$[5]
CVD grown	800–16 000 $cm^2/V.s$[24;25]
Epitaxially grown	1000–18 000 $cm^2/V.s$[26;27]

1.3 Graphene Field Effect Transistors

The physical structure and operations of a GFET can be traced back to a Schottky barrier field effect transistor (SB-FET) device, a modified view of a conventional MOSFET. A structural and operational schematic for a conventional MOSFET is shown in Fig. 1.4(a). A MOSFET is an electronic device with three terminals; the source (s), drain (d), and gate (g), where the source typically is parked at electrical ground, and the voltage bias and current amplitude between source-drain and source-gate terminal pairs are given by V_{ds}, I_{ds}, and

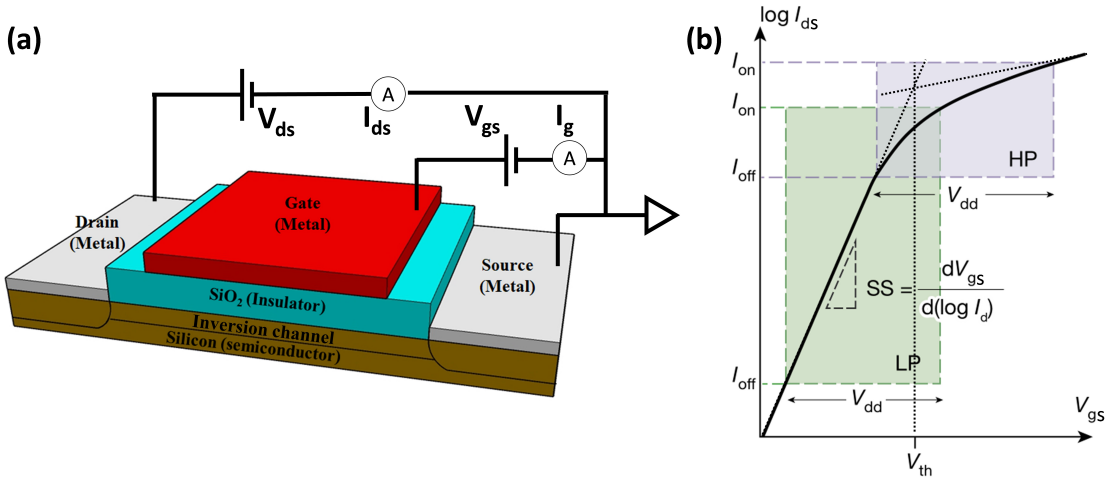


Figure 1.4: *(a) Schematic of a MOSFET. (b) log(I_d) vs V_{gs} plot showing current gate voltage relationship of an operational MOSFET. Cao et al., The future transistors, Nature, 620, 501-515, 2023, Reproduced with permission from Springer Nature*[3].

V_{gs}, I_g, respectively (see Fig. 1.4(a)). The source, drain and gate terminals are metallic in nature whereas the electrical channel is separated from the gate terminal by an insulating dielectric (eg., SiO_2) forming a metal-oxide-semiconductor (MOS) capacitor structure. The insulating dielectric is sometimes referred to as a gate oxide because oxides form a majority of the dielectric materials used in the MOSFETs. The above mentioned voltage biases are applied to control the flow of charge carriers between the source and drain in the electrical channel. Fig. 1.4(b) shows the behavior of measured drain current (I_{ds}) as a function of applied gate voltage (V_{gs}) for a MOSFET.[3] The device has two operating regimes, with high (near saturation) current and low current with a characteristic switching swing, with their respective OFF (I_{Off}) and ON (I_{ON}) current values. Another important parameter for a MOSFET operation is the magnitude of the gate voltage (V_{gs}) when the device turns ON and is designated as the threshold voltage (V_{th}). The rate at which the device turns ON is termed as the sub-threshold swing (SS) and is given by $SS = \frac{dV_{gs}}{d(logI_d)}$ (see Fig. 1.4(b)). It is indispensable to a MOSFET to possess faster switching capability (lower SS), which symbolizes the MOSFET can switch between OFF and ON states with less voltage, thus requiring a lower power of operation.

Fig. 1.5 (a–b) shows the schematics of GFETs with bottom and top gate geometries where

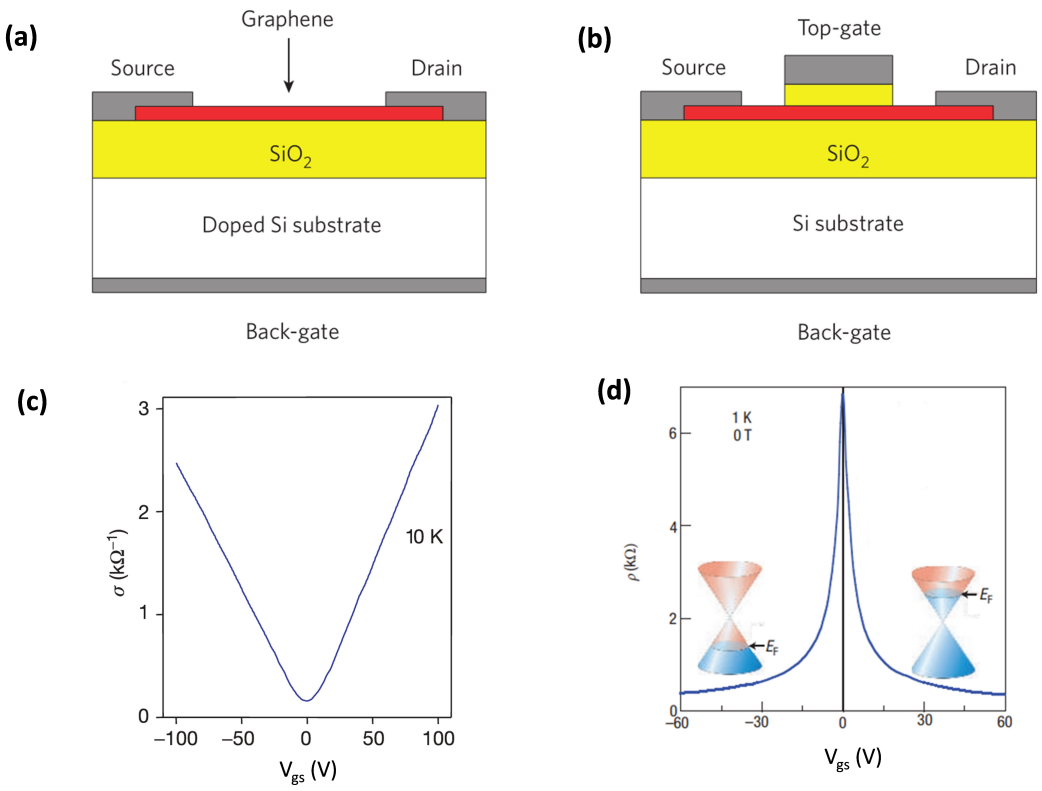


Figure 1.5: *(a-b) Schematic of bottom gated and top gated GFET. (c) conductivity (σ) vs V_{gs} plot of a typical GFET. (d) Resistivity (ρ) vs V_{gs} plot of a typical GFET. (a-b) Frank Schwierz, Graphene Transistors, Nature Nanotechnology, 5(7), 487-496 (2010), Reproduced with permission from Springer Nature*[29]*. (c) Novoselov et al., Two-dimensional gas of massless dirac fermions in graphene, Nature, 438(7065), 197-200 (2005), Reproduced with permission from Springer Nature*[5]*. (d) A.K. Geim and K. S. Novoselov, The rise of graphene, Nature Materials, 6(3), 183-191 (2007) Reproduced with permission from Springer Nature*[6]*.*

the metal gate terminal is below or above the graphene channel, respectively.[29] The effect of V_{gs} on a typical GFET's electrical conductivity and resistivity is shown in Fig. 1.5(c,d).[5] One may clearly notice that the electrical transport characteristics of a GFET are significantly different compared to conventional MOSFETs. This is attributed to graphene's linear band dispersion and semimetallic nature (Eq. 1.3). Upon the application of a positive (negative) V_{gs}, the Fermi energy level shifts up (down) making the graphene channel electron (hole) rich for electrical conduction (see Fig. 1.5(c,d)). This property of electrically tuning the Fermi level to populate either holes or electrons in the channel is termed as ambipolar

transport. Fig. 1.5(c,d) also shows a global conductance minima and resistance maxima at V_{gs}=0, called the Dirac point or the charge neutrality point (CNP) of a GFET. Graphene's finite conductivity at the Dirac point, compromises graphene's OFF current. However, due to its exceptionally high electrical mobility, a GFET is suitable for radio frequency (RF) applications (section 1.4).

1.4 High mobility transistors and their RF communication applications

RF transistors are used to amplify radio frequency signals. The amplification factor of an RF transistor, also known as small-signal current gain ($|h_{21}|$), describes the ratio of output signal to input signal. A typical behavior of $|h_{21}|$ is shown in Fig. 1.6 where the gain is typically highest at lower frequencies and varies as $1/f$ where f represents the signal frequency.[30] This $1/f$ behavior is due to parasitic capacitance and inductance in the RF transistor circuitry, which affect the impedance and phase of the input and output signals, reducing the efficiency of the amplification as frequency increases.[14] A red dashed line is shown in Fig. 1.6 displaying the $1/f$ behavior for current amplification.

The most widely used figure of merit for RF transistors is the cut-off frequency (f_t). Cutoff frequency is the value at which the small signal current gain ($|h_{21}|$) factor reduces to unity. Naturally, f_t represents the upper bound on the frequency at which an RF transistor can be operated. An equivalent circuit diagram for an RF transistor (see Fig. 1.7) details the various circuit components that determine f_t.[31] The cut-off frequency f_t is given by:[14;29;31]

$$f_t = \frac{g_m}{2\pi[(C_{gs}+C_{gd})(1+(R_d+R_s)g_{ds})+C_{gd}g_m(R_d+R_s)+C_{pg}]} \tag{1.5}$$

where g_m is the transconductance, C_{gs}, C_{gd}, and C_{pg} are the gate to source, gate to drain, and gate parasitic capacitance, respectively. R_s and R_d are the source and drain contact resistance and g_{ds} is the transistor channel conductance, respectively. Eq. 1.5 suggests that the cut-off frequency can be maximized by making g_m as large as possible and making all

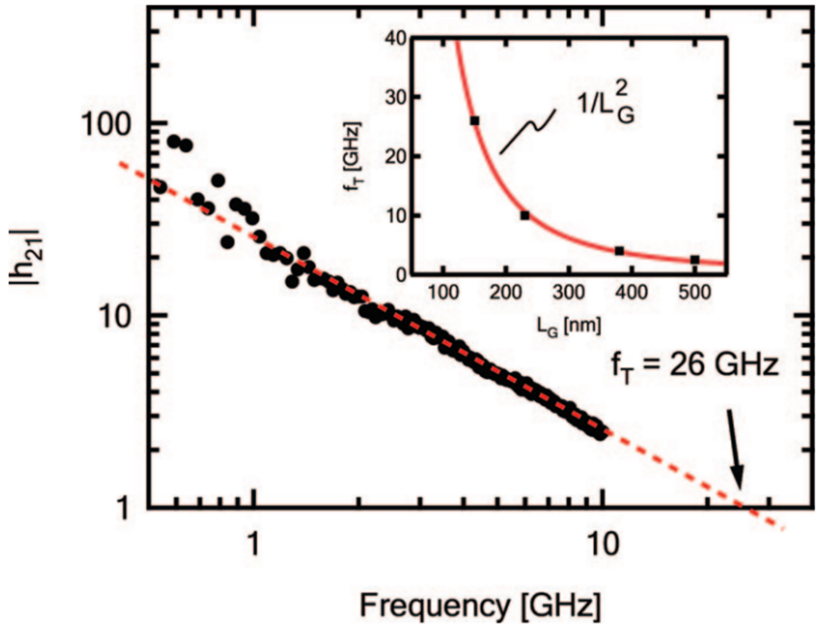


Figure 1.6: *Small current amplification of an RF transistor as a function of frequency. The inset shows* $\frac{1}{L_G^2}$ *scaling of cutoff frequency with gate length. Reprinted (adapted) with permission from Lin et al., Operation of graphene transistors at gigahertz frequencies, Nano Letters, 9(1), 422-426 (2009) Copyright 2009 American Chemical Society*[31].

the parasitic resistances and capacitances as small as possible. By first order approximation, $g_m \propto \frac{\mu}{L_G}$ where μ is electrical mobility and L_G is the gate thickness. In the diffusive regime, both $C_{gs}, C_{gd} \propto L_G$, which gives $f_t \propto \frac{1}{L_G^2}$. This $\frac{1}{L_G^2}$ scaling of the cut-off frequency is shown in the inset of Fig. 1.6. Therefore, an increased cut-off frequency in an RF transistor can be achieved by increasing the mobility and decreasing it's channel length. Graphene's ultra-high electron mobility makes it appropriate for future radio frequency transistors based current amplifiers.

However, the current gain of an RF transistor is not a smooth function of frequency. It exhibits fluctuations and variations that are caused by random noise sources within the transistor, such as thermal noise, shot noise, and flicker noise (see section 1.6). Flicker noise or $1/f$ noise is of higher interest for semiconductor devices because the level of noise is higher at low frequencies and decreases as the frequency of operation starts increasing. With RF transistors providing higher signal gain at lower frequencies, $1/f$ noise becomes a major bottleneck for efficient amplification of RF signal requiring fundamental understanding of

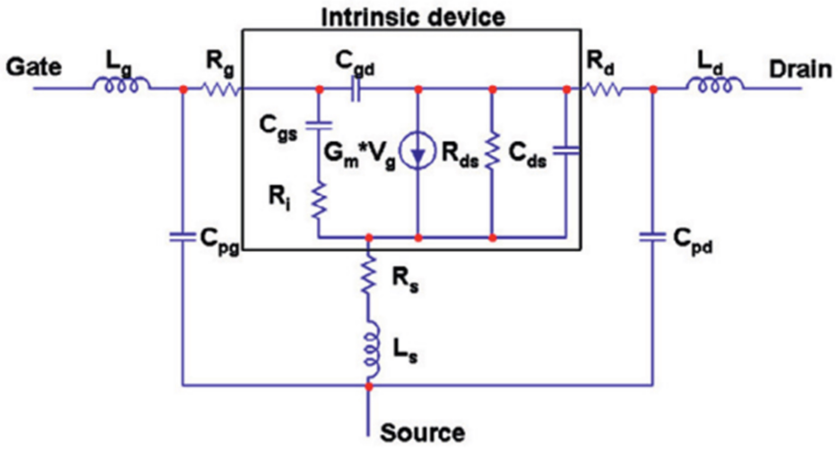


Figure 1.7: *Equivalent circuit diagram of an RF transistor. Reprinted from Graphene for radio frequency electronics, Lei Liao and Xiangfeng Duan, Materials Today, 15(7-8), 328-338 (2012) with permission from Elsevier*[14].

$1/f$ noise in GFET devices and their reduction for high performance application.

1.5 Ultra high mobility Heterostructure Graphene Field Effect Transistors (HGFETs)

The requirement for high mobility and low resistance materials for future RF devices entails a fundamental understanding of graphene's electronic properties and methodologies to fabricate the same. Electronic transport studies can be performed to understand the microscopic properties of graphene, governed by graphene's band dispersion (see section 1.2), and various scattering mechanisms of the charge carriers. Even though experimental techniques such as scanning probe microscopy exhibit little evidence of intrinsic structural defects,[32–34] the charge carriers in graphene nevertheless undergo scattering, caused by various external sources increasing channel resistivity. These scattering centers originate from charge impurities on top of the graphene surface and underlying substrate, interface traps,[35;36] and from lattice vibrations within the graphene channel and along the interface with the substrate.[37;38]

Multiple efforts have been made to reduce the effects of scattering to improve the perfor-

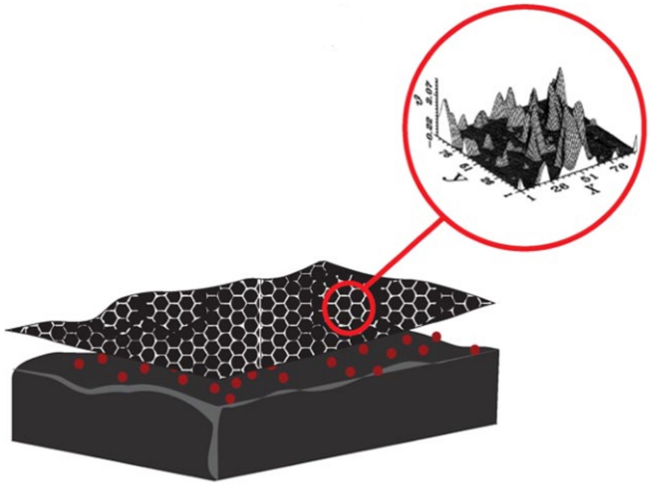


Figure 1.8: *Schematic of surface charge impurities at graphene/SiO_2 interface and the resulting Coulombic potential observed by charge carriers in graphene. Adam et al., A self-consistent theory for graphene transport, Proceedings of the National Academy of Sciences, 104(47), 18392-18397 (2007)*[39]

mance of graphene devices. Even though the effects of crystal vibrations can be reduced by decreasing the operating temperature, intrinsic defects and charge-impurity based scattering still have pronounced effects at low cryogenic temperatures. These effects can be minimized through different device fabrication schemes such as using defect-free, mechanically exfoliated graphene for the channel (see section 1.2) and employing them with atomically thin lattice matched hBN substrate. Due to graphene's high optical transparency in visible range, historically graphene has been exfoliated on to Si/SiO_2 substrates for its ease of identification. Although SiO_2 can be conveniently grown/deposited on Si wafers, it suffers from surface charge impurities, dangling bonds, and surface roughness that adversely affect the electronic transport properties in GFETs. Fig. 1.8 shows a schematic of surface charge impurities at graphene/SiO_2 interface. The presence of surface charge impurities at the interface leads to long-range Coulombic potentials in the channel which act as scattering centers for the charge carriers, effectively increasing the resistance of the GFETs.

Although the use of mechanically exfoliated graphene from high quality graphite sources typically produce low crystalline defects, extrinsic factors such as surface roughness from substrate materials can induce surface defects that hinder the electrical transport. The effects

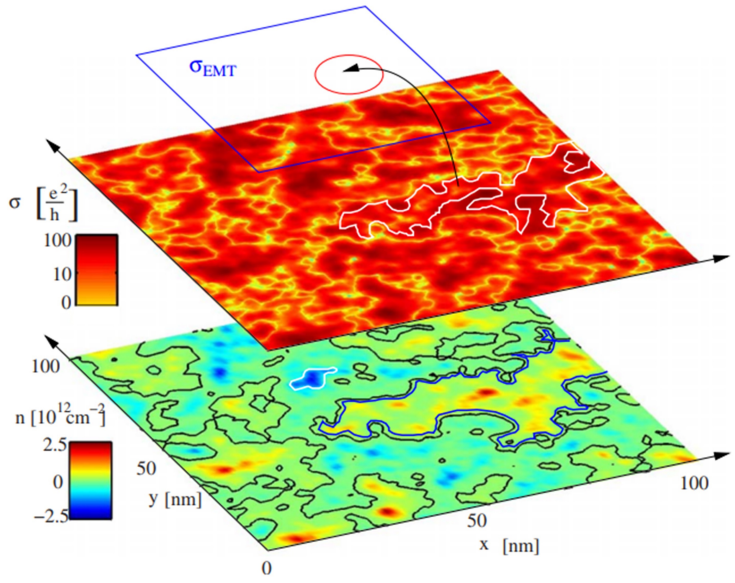


Figure 1.9: *Charge concentration (n) and conductivity (σ) profile of single layer graphene under the formation of electron-hole puddles. Reprinted figure with permission from [Enrico Rossi, S. Adam, and S. Das Sarma, Effective medium theory for disordered two-dimensional graphene, Physical Review B, 79(24), 245423, 2009] Copyright (2009) by the American Physical Society.*[40]

of interface charge impurities and surface roughness or corrugation become more profound at low carrier densities, where mobility values are expected to be high. The formation of electron-hole puddles in the channel gives rise to percolative transport paths, thereby increasing the channel resistance and decreasing mobility.[40–43] Fig. 1.9 shows the charge density (bottom panel) and electrical conductivity (upper panel) profile of a graphene sheet on an SiO_2 substrate with an interface charge density of 5×10^{11} cm^{-2} where electron-hole puddles affect the electrical conductivity.[40] Similarly, Fig. 1.10 shows the physical profile of a corrugated graphene sheet (a) and the corresponding electrical potential profile (b).[42] Similar to the long range Coulombic potential originating from charge impurities, the potential profile from rippled graphene also deters the flow of charge carriers.

Various device fabrication techniques have been developed to reduce substrate induced carrier scattering in order to increase the mobility of GFETs. Most notably, making suspended GFETs where the graphene is suspended above the substrate surface and encapsulat-

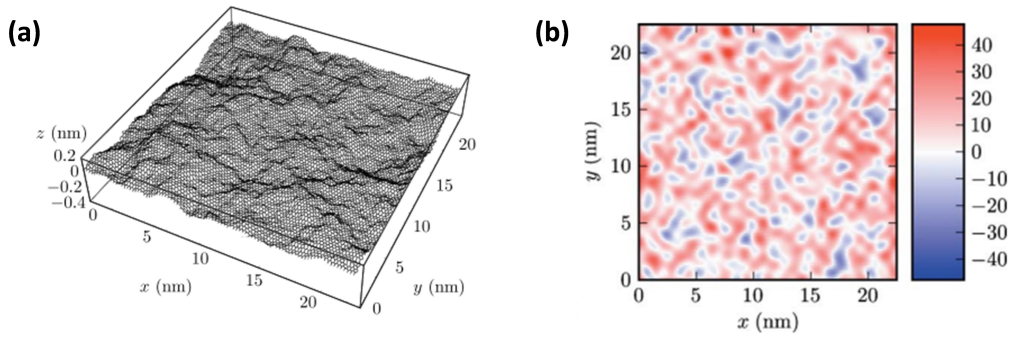


Figure 1.10: *Model showing the surface corrugation of graphene(a) and the effective electrical potential profile in graphene from the corrugation(b). Reprinted figures with permission from [Gibertini et al., Electron density distribution and screening in rippled graphene sheets, Physical Review B, 81(12), 125437, 2010] Copyright (2010) by the American Physical Society.*[42]

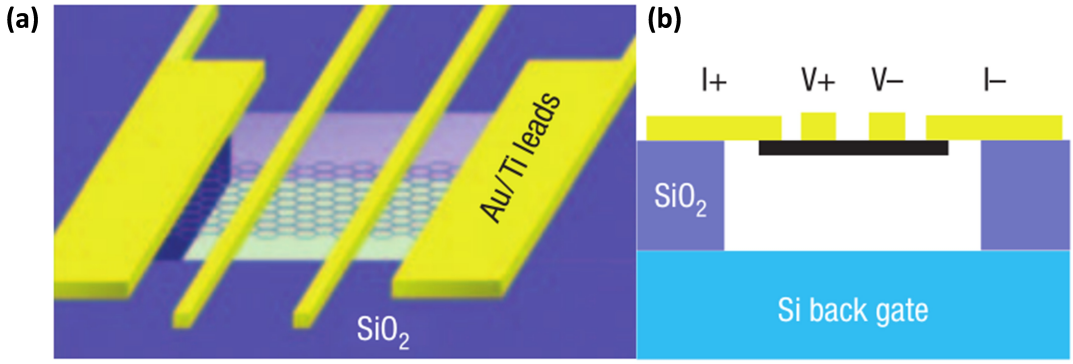


Figure 1.11: *Schematic of a suspended graphene FET as viewed from top(a) and side(b). Du et al., Approaching ballistic transport in suspended graphene, Nature Nanotechnology, 3(8), 491–495, 2008, Reproduced with permission from Springer Nature*[44]

ing the graphene channel within hBN have provided promising results. A suspended GFET is fabricated by selectively etching or removing the substrate underneath the graphene channel while being supported by the metal contacts at source and drain ends.[44;45] The schematics of a suspended GFET channel are shown in Fig. 1.11 in top-down and side view.[44] This leads to carrier transport with substantially reduced interfacial scattering, thereby resulting in very high electrical mobility. Du et al., in their study have shown carrier mobility values of $\approx$ 200,000 cm^2/V.s in suspended GFETS at 5K.[44] The study also shows that in suspended GFETS, carriers attain ballistic transport at low temperatures.

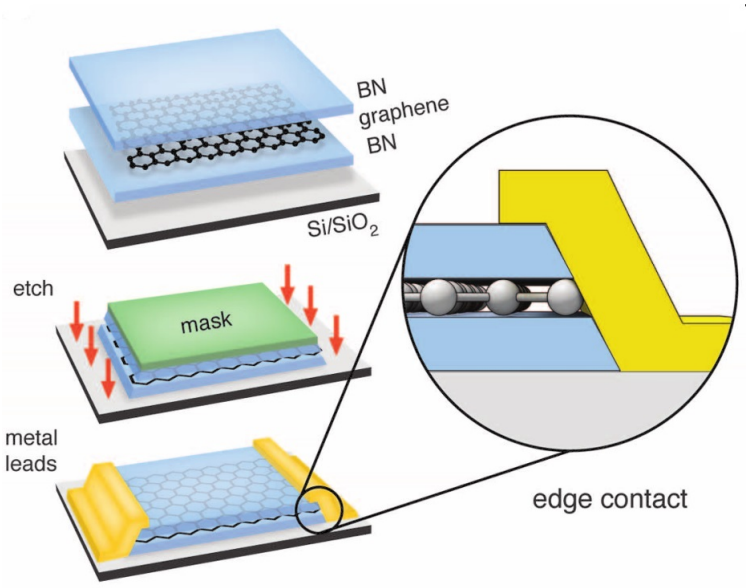


Figure 1.12: *Schematic of hBN/graphene/hBN heterostructure assembly procedure and HGFET fabrication process for creating 1D edge contacts. From [Wang et al., One-dimensional electrical contact to a two-dimensional material, Science, 342(6158), 614-617, 2013]. Reprinted with permission from AAAS*[12].

Although suspended GFETs show better device performance as compared to their non suspended counterparts, their fabrication is complex and involves wet etching the substrate that leads to surface corrugation which may reduce the device mobility (see Fig. 1.10). Moreover, suspended surface graphene, once fabricated is susceptible to impurities which lead to chronic device deterioration. On the other hand, Wang et al., have shown that the use of hexagonal boron nitride (hBN) both as a substrate and an encapsulating material enhances the room temperature device performance (see Fig. 1.12) in a heterostructure graphene field effect transistor (HGFET).[12] hBN, a material with two-dimensional atomically thin structure like graphene has consists of boron and nitrogen atoms in honeycomb lattice with minimal lattice mismatch with graphene. Encapsulating graphene between hBN warrants minimal surface corrugation and protection from any potential environmental adversaries. The surface charge impurities and dangling bonds that form long range Coulombic potentials (see Fig. 1.8) are also significantly lower in hBN which leads to enhanced device performance. The encapsulation of graphene facilitates the fabrication of a one-dimensional (1D) edge contact which results in lower contact resistance.[12] Fig. 1.12 shows the methodology for

fabricating a HGFET with 1D edge contact. Once, the hBN/graphene/hBN heterostructure is assembled, the contact region is etched out and only the edge of the graphene layer is exposed to form a 1D metal contact. The contact metal is then evaporated to make the metallic-electrical contact to graphene at the edge.

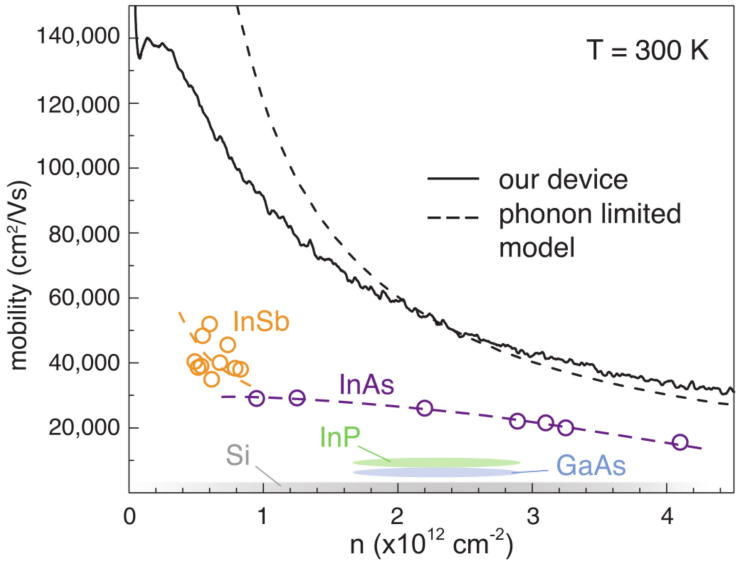


Figure 1.13: *Extracted carrier mobility as a function of carrier density in HGFET. For comparison mobility values of FETs fabricated using III-V semiconductors are also reported in the plot. From [Wang et al., One-dimensional electrical contact to a two-dimensional material, Science, 342(6158), 614-617, 2013]. Reprinted with permission from AAAS*[12].

Fig. 1.13 shows the room temperature electrical mobility of mechanically exfoliated HGFETs encapsulated in hBN with 1D edge contacts.[12] The device mobility in encapsulated HGFETs can reach up to 140,000 cm^2/Vs at room temperature for low charge carrier concentrations. The device also shows ballistic transport at low temperatures with a mean free path of 21 μm and device mobility of $\approx$1,000,000 $cm^2/V.s$. For comparison, the mobility values for Si and commonly used III-V semiconductors are also shown in the plot, emphasizing the superior performance of HGFETs for future high electron mobility transistors (HEMTs). Table 1.2 compares the mobility values obtained in mechanically exfoliated GFETs fabricated with a SiO_2 substrate and a suspended GFET.

Table 1.2: *Mobility values in mechanically exfoliated graphene*

Fabrication Process	Mobility (300K)	Mobility (10K)
Graphene on SiO_2	8,000 $cm^2/V.s$[5]	20,000 $cm^2/V.s$[46]
Suspended graphene	120,000 $cm^2/V.s$[45]	200,000 $cm^2/V.s$[44]
Graphene encapsulated by hBN	140,000 $cm^2/V.s$[12]	1,000,000 $cm^2/V.s$[12]

1.6 Electrical noise in semiconductors

As important is the electrical signal in a modern FET device, it is also indispensable to reduce the electrical noise in the same. Noise is ubiquitous and fundamental fluctuations of signal in a device and it is necessary to understand and contain. A fundamental understanding of electrical noise is necessary so it can be reduced while increasing the signal amplitude of the circuitry (enhanced signal-noise(S/N) ratio). Electrical noise also imparts key information on the device quality and performance. In electrical devices, noise sources can be separated into two larger categories, namely intrinsic and extrinsic sources. Extrinsic sources, as the name suggests, are electrical interference that originates from radio interference, background radiation, surrounding electronics, voltage/current sources, etc., which generally can be controlled through proper circuit layout. On the other hand, intrinsic noise sources stem from the semiconductor material and device structure which needs careful consideration.[47] Noise is characterized by power spectral density as a function of frequency which is represented as $S_x(f)$, where x can be either the voltage (V), current (I), or resistance (R) of the device. S_x in the frequency domain is calculated by a Fourier transform of current or voltage signal in the time domain. The different power spectral density values are related to one another by:[48]

$$\frac{S_I}{I^2} = \frac{S_V}{V^2} = \frac{S_R}{R^2} \tag{1.6}$$

where S_I, S_V, S_R are current, voltage and resistance noise spectral density and I, V, and R represent the drain current, drain to source voltage and the device resistance of the FET.

The different kinds of noise have different frequency dependencies. The most common, white noise and Johnson noise (thermal noise), are frequency independent.[49] The spectral density of Johnson noise in terms of the voltage and current are given by:[49]

$$S_v(f) = 4k_BTR \tag{1.7}$$

$$S_I(f) = \frac{4k_BT}{R} \tag{1.8}$$

where k_B, T, and R are the Boltzmann constant, absolute temperature, and resistance of the device, respectively. Due to the discrete nature of charge carriers, shot noise is generated when charge carriers randomly cross a potential barrier (PN junction, metal-semiconductor Schottky barrier, etc). This frequency independent noise spectra is given by:[50;51]

$$S_I = 2qI \tag{1.9}$$

where q is the electronic charge. Shot noise is generally observed in PN junction diodes and is very low in magnitude as compared to noise spectra typical in transistors.

The discrete nature of charge carriers also form the basis of frequency dependent noise in semiconductor devices. Consistent and random generation and recombination of electron-hole pairs in semiconductors from optical and thermal excitation, affect the charges moving in the channel. This noise, with its $1/f^2$ dependence, is generation-recombination (GR) noise and is given by:[52]

$$\frac{S_I}{I^2} = \frac{\tau}{1 + (2\pi f)^2\tau^2} \tag{1.10}$$

where τ is the average lifetime of generation-recombination events and f is the frequency.

Flicker noise, another frequency dependent noise, is the most common type in semiconductor devices due to multiple possible physical sources. $1/f$ noise also has the highest magnitude as compared to the previously discussed noise sources, thus making it the most studied noise type in semiconductor devices.[54–57] The general form of $1/f$ noise is given by:[57]

$$S_I \propto \frac{I^2}{f^\gamma} \tag{1.11}$$

where γ is generally constant and $\approxeq 1$ but interesting behavior can be observed in mi-

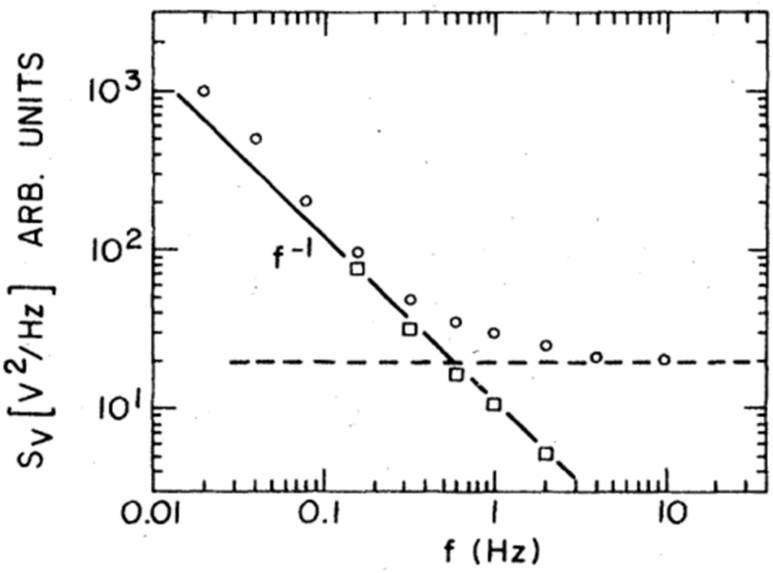


Figure 1.14: *The power spectral density of a carbon film as a function of frequency. The dashed line shows the background spectrum and the open circles shows the measured values. The open squares show the background corrected measurements (clearly showing* $1/f$ *behavior). Reprinted from [H. G. E. Beck and W. P. Spruit, 1/f noise in the variance of johnson noise, Journal of Applied Physics, 49(6), 3384–3385, 1978], with the permission of AIP Publishing*[53].

cro/nanoscale devices. Fig. 1.14 shows a typical $1/f$ noise power spectral density for a semiconducting device.[53] There are two accepted models that are used to explain the origin of flicker noise in traditional FET devices, namely McWhorter's number fluctuation model and Hooge's mobility fluctuation model.[59–61] The common physical explanation for $1/f$ noise in both the models is a combination of generation-recombination noise centers with a wide distribution of trapping time constants. By summing Eq. 1.10 over a wide distribution of time constants (τ), the characteristic $1/f$ envelope develops across the frequency span of interest. This phenomenon is shown in Fig. 1.15, where the red trace shows the envelope for a few generation-recombination time constants and the green curve shows the envelop for closely spaced distribution of time constants.[58] Note that the characteristic time constant (τ) in the individual traces need not be only the electron-hole generation recombination type. The interface states between the semiconducting channel and the gate oxide can also randomly trap and de-trap charge carriers with a wide distribution of characteristic time constants

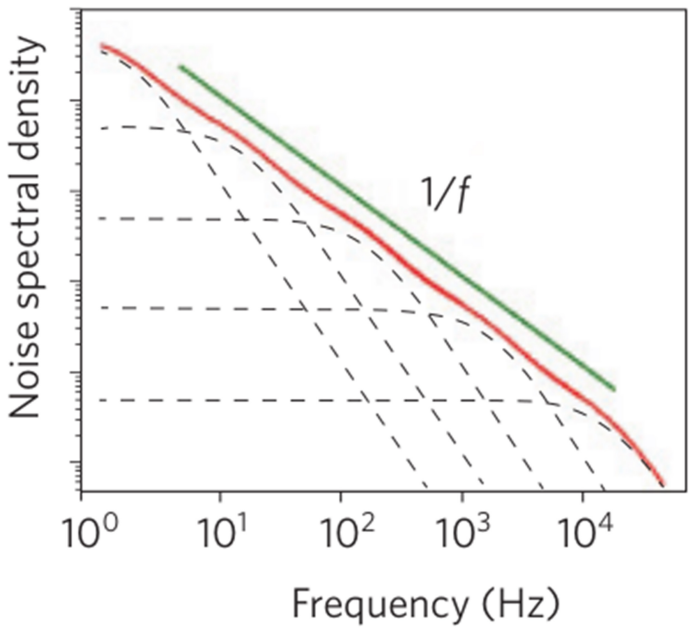


Figure 1.15: *Plot showing the power spectral density of a FET with multiple roll off generation-recombination profiles. The envelope shown in red and green lines form $1/f$ profile. Alexander A. Balandin, Low-frequency 1/f noise in graphene devices, Nature Nanotechnology, 8(8), 549–555, 2013, Reproduced with permission from Springer Nature*[58].

(τ_{trap}) as shown in McWhorter's number fluctuation theory.[59] This random trapping and de-trapping leads to fluctuations of charge carriers in the channel and $1/f$ noise. $1/f$ noise is not only attributed to number fluctuation, but also carrier mobility fluctuations as proposed by F.N. Hooge. Similar to trap states, multiple factors in the semiconducting channel can lead to wide distribution of fluctuating scattering centers with their own characteristic time constants (τ_{mob}). These fluctuating scattering centers affect the flow of carriers eventually leading to fluctuating carrier mobility and the characteristic $1/f$ noise.[60;61] The noise spectral density can be written according to Hooge's and McWhorter's model, respectively as:[59;60]

$$\frac{S_I f}{I^2} = \frac{\alpha_H}{N} \tag{1.12}$$

$$\frac{S_V}{V^2} = \frac{6.2e^2 k_B T}{AfC_g^2\kappa} D_{it} \left(\frac{g_m}{I}\right)^2 \tag{1.13}$$

where α_H is a dimensionless parameter called as the Hooge parameter and is the figure of

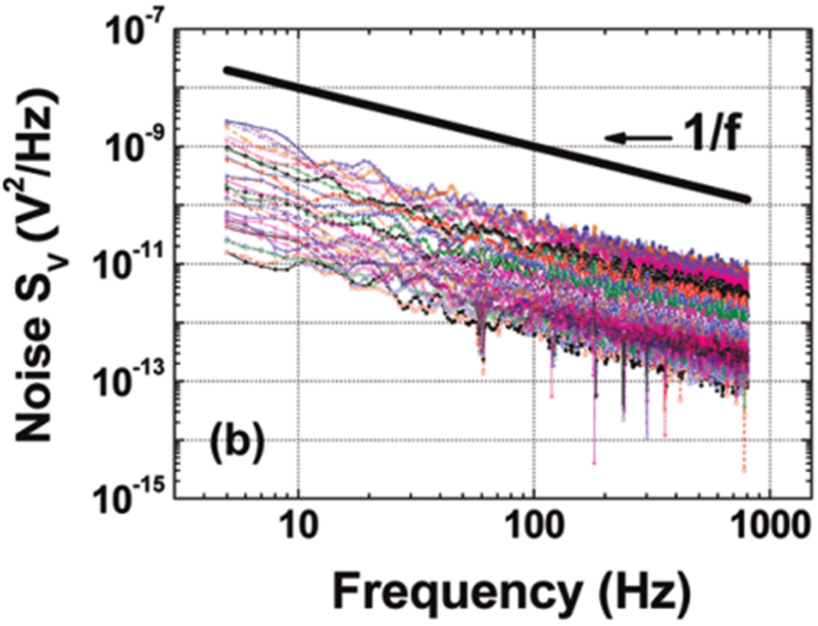


Figure 1.16: *Power spectral density of* $1/f$ *LFN measurements performed on a GFET at multiple gate volatges. Reprinted (adapted) with permission from Xu et al., Effect of spatial charge inhomogeneity on 1/f noise behavior in graphene, Nano Letters, 10(9), 3312–3317, 2010 Copyright 2010 American Chemical Society.*[62].

merit for device's noise, with lower values indicating less noisy devices. N is the total charge carriers present in the FET channel at a given temperature. In the McWhorter's model, A, C_g, κ,and D_{it} represent device area, gate capacitance per unit area, characteristic trap length ($\approx 10^9$ m^{-1}), and trap density respectively. g_m represents the transconductance of the device.

Although $1/f$ noise is an undesirable electronic phenomenon in semiconducting devices, it can be used as a spectroscopic tool, specifically at low frequencies to probe charge traps and carrier scattering centers in FETs. Multiple low frequency noise (LFN) studies on GFETs have probed the carrier physics in single and multilayer graphene layers.[64–68] Fig. 1.16 shows the power spectral density for a GFET at various operating gate voltages.[65] A reference line is also shown on the plot confirming the $1/f$ behavior of the noise spectral density at low frequency values. The noise levels for GFETs are commonly presented as noise amplitude

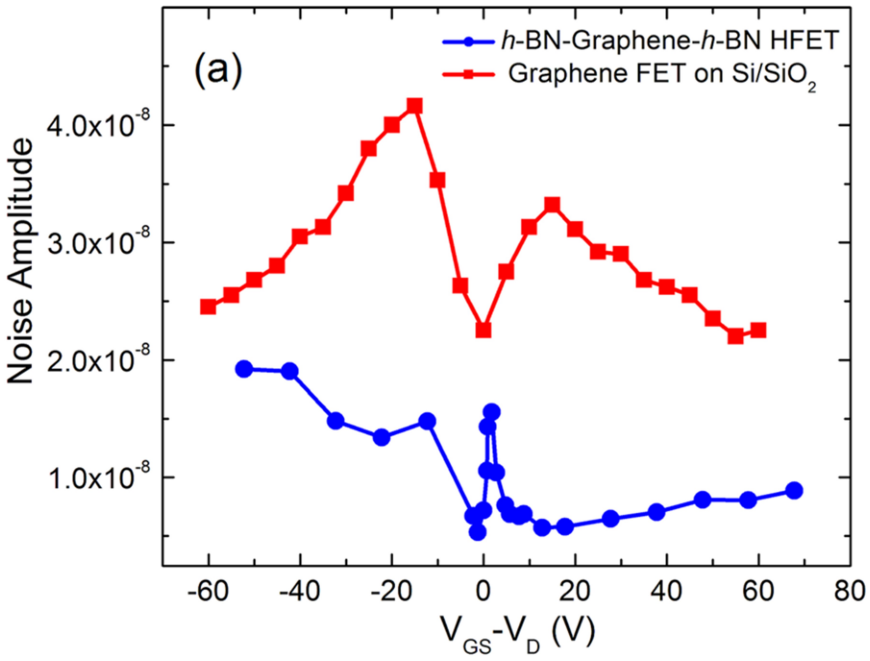


Figure 1.17: *Measured low frequency noise amplitude for GFET and hBN/graphene/hBN HGFET at different gate voltages. Reprinted from [F Stolyarov et al., Suppression of 1/f noise in near-ballistic hbn-graphene-hbn heterostructure field-effect transistors, Applied Physics Letters, 107(2), 2015], with the permission of AIP Publishing*[63].

(A), to comply with both the McWhorter's and Hooge's models and is given by:

$$A = \frac{S_I \times f}{I^2} \tag{1.14}$$

where f is the frequency, typically 100 Hz. The noise amplitude (A) calculated at a fixed frequency exhibits interesting gate voltage behavior, from which novel physical properties can be inferred. Fig. 1.17 shows the gate voltage dependence of the noise amplitude measured in GFETs and hBN/graphene/hBN HGFETs as a function of the applied overdrive voltage ($V_{GS} - V_D$).[63] Clearly, the noise amplitude in hBN/graphene/hBN HGFET devices are ≈ 2 times lower as compared to GFETs fabricated on Si/SiO_2 substrate further solidifying the importance of hBN as a substrate material for graphene devices. Moreover, Fig. 1.17 also shows the characteristic "M" shape (red) and "Λ" shape (blue) independently reported in multiple studies.[63;64;67;69;70]

Thus far, commercial finFET technology has evolved to 3-nm technology node and is expected to survive up to one more generation of 2-nm node. The challenges for finFET technology to continue scaling past 2-nm technology must address large parasitic capacitance, mechanically unstable fins due to large aspect ratios in their dimensions, limited fin width and small fin pitch, posing a major bottleneck that degrades device performance rapidly. The fundamental materialistic properties of 2D materials like graphene and hBN and their respective heterostructures mentioned earlier in this chapter promise future devices with nodal technology beyond 2 nm. The advantages imparted by 2D materials at the listed critical dimensions as compared to conventional three dimensional materials include significant mechanical strength at large aspect ratios, significantly higher density of states and carrier density for optimal device operation (ON-OFF ratios), and ultimate nodal size of one atomic width (<1nm). Hence, it is of utmost importance that elementary studies on 2D material heterostructures to understand the underlying physics governing the operation of electronic devices fabricated from these paradigm-shifting materials are performed for future device applications. In this dissertation we strategically study the mechanisms that govern the behavior of charge carriers (electrons and holes) in graphene with the special focus on hBN when used as the encapsulating material and as the polarizable dielectric for electrostatic gating. The objectives of this dissertation study include successful fabrication of 2D HGFETs with 1 dimensional edge contacts by using a plethora of nanofabrication techniques and analyzing the electrical transport and LFN behavior in the fabricated HGFETs by operating the devices at a series of cryogenic temperatures ranging from ≈10K up to 300K. Performing these experiments enables the study of temperature dependent scattering effects that limit charge transport in 2D HGFETs and temperature activated trap states at semiconductor/substrate interfaces that give rise to LFN.

The results of the experiments are assimilated in the chapters as follows. First the procedure used to assemble atomically thin 2D heterostructures and fabricate them into microelectronic devices with one-dimensional edge contacts is described (see Chapter 2). Next, the fundamentals of electrical transport and low frequency noise characterization in an HGFET to avoid of any contributions from electrical contacts are detailed (see Chapter 3). Chapter 4

and 5 shed light on charge carriers' (electrons and holes) interaction with defects and crystal vibrations in the graphene channel and at graphene/hBN interfaces. The temperature dependent impacts of these scattering effects and the charge traps at graphene/hBN interface on the measured low-frequency noise are then studied. Furthermore this dissertation also delves into the effect of electron-hole puddles on electrical transport and low frequency noise when HGFETs are operated close to the Dirac point (see Chapter 4). The use of isotopically pure hBN ($h^{10}BN$ and $h^{11}BN$) as the encapsulant in HGFETs were studied and the effect of boron isotope concentration on the measured cryogenic electrical transport and low frequency noise (see Chapter 5). Overall this dissertation provides a framework to fabricate high performance and low noise HGFETs with a mechanistic understanding of microscopic scattering phenomena involved within these devices.

Chapter 2

Design and Microfabrication of Heterostructure Field Effect Transistors

Due to the nanoscale physical dimension of HGFETs, the materials and process steps employed in the fabrication process play an enormous role in the device's performance. Furthermore, the physical stability including environmental stability, material composition, and process compatibility demand utmost care while selecting and developing 2D HGFETs. This chapter details the materials used and the process employed in the fabrication of HGFETs. All the fabrication processes were conducted in class 1000 cleanroom environment in the integration lab at Center for Integrated Nanotechnologies (CINT), Sandia National Laboratories, Albuquerque, New Mexico, USA.

2.1 Materials Used

2.1.1 Substrates

Commercial double-sided polished silicon wafers from Virginia semiconductors with <100> crystal orientation and a thickness of 400 μm were used as the substrate. A 275 nm thick layer of SiO_2 was thermally grown on both sides using a high temperature thermal treatment in dry O_2. Oxide thickness of 275 nm made it easy to identify a single layer of graphene under optical microscope after it gets transferred onto the substrate.[71;72] Moreover, SiO_2 traditionally acts as gate dielectric for GFETs with bottom gate configuration. The Si wafers were highly p-doped (boron doped) with a room temperature resistivity of 0.01-0.02 Ω-cm. The low resistivity of the wafer allows electrical contact for a global back gate (see Fig. 1.5 (a)) without requiring additional metallization. A low wafer resistivity (room temperature) is also needed to process meaningful measurements on HGFET devices studied at cryogenic temperatures.

2.1.2 Graphene

Single layers of graphene (SLG) were micromechanically exfoliated (see section 2.2) from highly oriented pyrolytic graphite (HOPG) crystals purchased from 2D Semiconductors. The use of HOPG allows exfoliation of large area SLG flakes onto the target substrate due to its crystal uniformity, absence of impurities, and low angle spread between each graphene layer.

2.1.3 Hexagonal Boron Nitride (hBN)

The hexagonal boron nitride (hBN) were obtained from two sources. In the first study, hBN samples obtained from the group led by T. Taniguchi and K. Watanabe in NIMS, Japan, were used for fabricating HGFETs for the electrical transport and LFN study (chapter 4). In the second study, the impact of boron isotope in hBN as the substrate and the encapsulant on the electrical transport and LFN was studied (chapter 5). These isotopic hBN samples

(crystals) were supplied by Prof. James Edgar's group at Kansas State University. The monoisotopic hBN used in this work come in three types, pertaining to the three isotopic concentrations of boron in hBN crystals. Boron has two isotopes with the atomic masses of ^{10}B and ^{11}B. Depending on the relative concentrations between the two isotopic variations, hBN crystals with varying crystal mass can be obtained. For this study, the three different hBN crystals were h^{10}B(99%)N, h^{11}B(99%)N and natural hBN which contains 80% ^{11}B and 20% ^{10}B. More information regarding the synthesis of isotopically pure hBN can be found in the study by Hoffman et al.[73] The electrical transport and LFN studies of the HGFETs with the above hBN types used as both the substrate and encapsulating material, are provided in chapter 5.

2.2 Fabrication of Graphene Heterostructure Field Effect Transistors

Two kinds of HGFETs were studied. The first type employed natural hBN as the substrate and encapsulant and the second type employed hBN with isotopically pure boron concentrations (both ^{10}B, ^{11}B, and natural boron mixing) as the substrate and encapsulant, respectively. The following subsections provide a detailed process flow for the fabrication of the two types of HGFETs. Typical process steps involve micromechanical exfoliation, heterostructure assembly, electron beam lithography, reactive ion etching, metal deposition, and ,metal liftoff, each of which is elaborated below.

2.2.1 Fabrication Process Flow

Backgated HGFET devices with natural hBN as the substrate and encapsulant with a single layer graphene (SLG) as the electrical channel were fabricated. The metal source and drain terminals were fabricated with a wedge shaped configuration, creating a one-dimensional (1D) edge contact architecture to the graphene channel following a complex series of lithography and etching methodologies.

Micromechanical exfoliation

Due to in-plane sp^2 bonding and out of plane van der Waal's interaction in both graphite and hBN crystals (and many other members of 2D crystal family), isolation of a few atomic layers to mono-atomic layers of graphene and hBN can be achieved through micromechanical exfoliation to obtain high quality atomically thin flakes. SLG and a few layers of hBN were obtained by mechanical exfoliation from bulk graphite and hBN crystals, respectively. Throughout this study micromechanical exfoliation method was chosen for HGFET fabrication due its suitability for high-performance electronic devices (see section 1.2 on page 3).

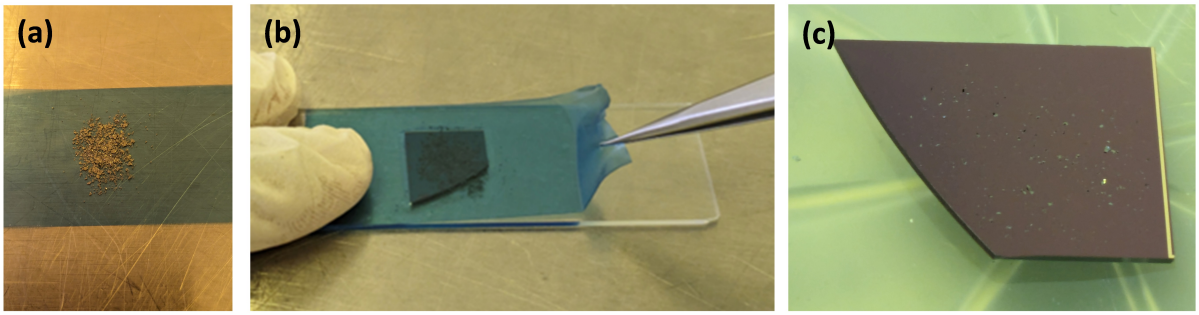


Figure 2.1: *(a) Graphite crystals on a blue SPV-224 tape after repeated exfoliation from one tape to another. (b) The tape containing the graphite crystals are attached and detached from Si/SiO_2 substrate placed on a glass slide. (c) An image of Si/SiO_2 substrate after the removal of the SPV-224 tape to realize ultrathin flakes on its surface.*

Fig. 2.1 illustrates the exfoliation process for obtaining graphene on a Si/SiO_2 substrate using blue SPV-224 Nitto tape commercially available by ProTapes. Initially, a few graphite crystals scraped from the HOPG crystal were placed on the blue tape. The tape along with the graphite crystals was then repeatedly attached and detached to separate clean regions on the tape to develop a circular region with thin graphite crystals as illustrated in Fig. 2.1(a). The tape was then adhered on to a clean Si/SiO_2 substrate (cleaned with acetone, isopropanol (IPA) and oxygen plasma at 2000W for 10 minutes), with the graphite side making contact with the wafer. Subsequently, the tape was slowly peeled off from the substrate (Fig. 2.1(b)). During this process, the strong van der Waals forces between the graphite crystals in contact with the SiO_2 surface cleaves graphene flakes of various thicknesses including SLG on the

substrate. Fig. 2.1(c) shows an image of a Si/SiO_2 substrate after the exfoliation is complete. A successful exfoliation process leads to at least one $10\mu m \times 10\mu m$ SLG flake on one wafer.

A similar procedure was performed to obtain few layers of hBN samples on a Si/SiO_2 substrate. A more detailed procedure on micromechanical exfoliation of graphene and hBN flakes can be found in Appendix A. The exfoliated flakes were then investigated under an optical microscope to search and identify single layer graphene (SLG) and few-layer hBN flakes for further processing in HGFET fabrication. Fig. 2.2 (a-b) shows representative images of a few layers of hBN and SLG (encircled), respectively used for HGFET fabrication.[74]

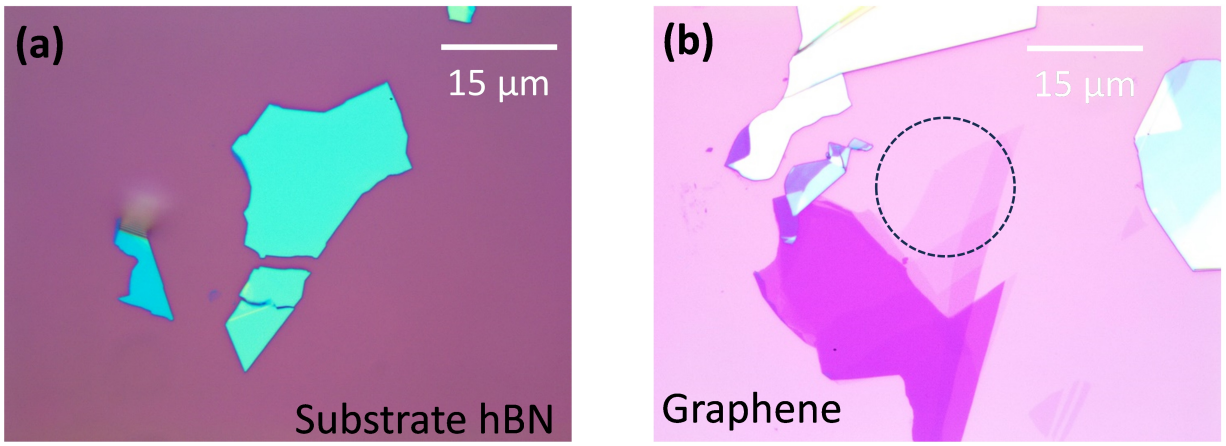


Figure 2.2: *(a) Micrograph of a few layer thick hBN flake on Si/SiO_2 wafer used as the substrate for heterostructure assembly. (b) Micrograph of a single layer graphene (encircled) surrounded by some few layer graphene and graphite on Si/SiO_2 wafer.*

As shown, the typical flake lateral size that are visibly uniform and thin are $\approx$10-20μm. Moreover, mechanical exfoliation results in a non-deterministic distribution of 2D flakes on the target substrate which make fabrication of 2D devices a challenging. Due to the small flake size, reliable navigation to the desired flake position on the substrates was achieved by fabricating alignment markers on the wafer which serve as microscopic landmarks. The best result was accomplished by capturing micrographs of target flakes along with the landmarks in the sample's vicinity. Fig. 2.3 shows an optical micrograph of an SLG exfoliated on a Si/SiO_2 wafer in the vicinity of alignment marks pre-fabricated on the wafer. The photolithography procedure for fabricating alignment markers on a 4" Si/SiO_2 wafer can be found in Appendix B.

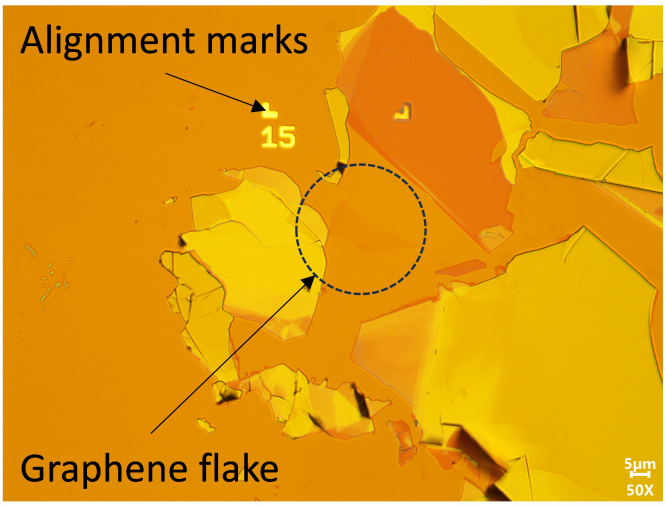


Figure 2.3: *Optical micrograph of a single layer graphene (encircled) in the vicinity of alignment markers.*

Heterostructure assembly

The atomically flat nature and the presence of lower surface charge impurities makes hBN an ideal substrate for 2D electrical channels. First, a heterostructure of SLG encapsulated between few layers of hBN was assembled. A schematic representation of a fully encapsulated hBN/graphene/hBN heterostructure is presented in Fig. 2.4. The process was achieved by lifting the exfoliated materials from their respective substrates and stacking them on top of one another (depending on the sequence) on a final Si/SiO_2 substrate on which the HGFET is desired to be integrated. The assembly procedure was performed using visco-elastic dry stamping method which employs a 2D material layer transfer system consisting of an optical microscope with long working distance lenses, X,Y,Z micro-manipulators, and a heated sample stage (see Fig. C.2).[75]

A visco-elastic dry stamping technique is a heterostructure assembly method for 2D materials where a polymer thin film is used to lift the requisite material from the exfoliated substrate and subsequently aligned and placed onto the target substrate using a different elastic polymer support. A schematic diagram for the visco-elastic stamping process used in this study is shown in Fig. 2.5. A polymer stack of polydimethylsiloxane (PDMS) and polycarbonate (PC) was used for the transfer process where the PDMS layer provided the

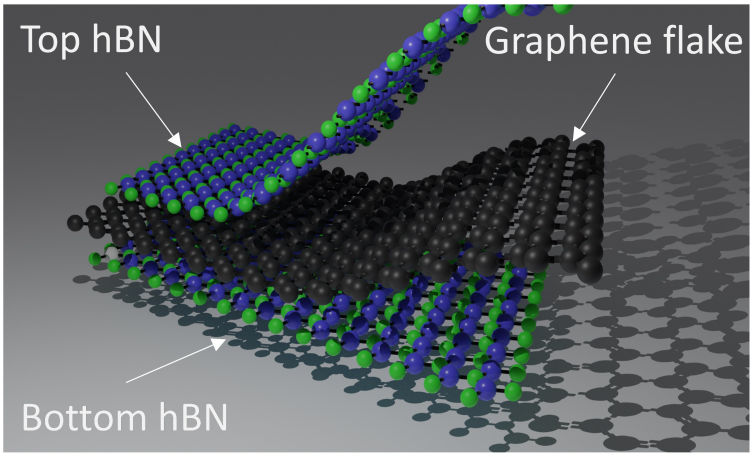


Figure 2.4: *A schematic representation of a 2D material stack for assembling a heterostructure of single layer graphene and hBN. Reprinted (adapted) with permission from Behera et al., Charge-inhomogeneity-mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. ACS Applied Nano Materials, 7(11), 12366–12375, 2024. Copyright 2024 American Chemical Society*[76].

elastic support, while PC provided the adhesive force to lift the required 2D material from SiO_2. The PDMS slab was obtained by cutting square shaped films from gelpak #4 storage boxes. 5% PC films were prepared by dissolving PC capsules in chloroform. The solution was then dropcasted onto a clean glass slide. A separate glass slide was used to smear the solution resulting in films of PC on the surface of the slides. After air drying for 5 minutes, square shaped pieces of PC were cut and were carefully placed on the PDMS film. By using a 2D layer transfer system (see Appendix C), the PDMS/PC polymer stack was used to pick up an hBN flake from a previously exfoliated Si/SiO_2 surface (see Fig. 2.5(a)). Next the PDMS/PC layer containing hBN (say top hBN) was aligned on to Si/SiO_2/graphene substrate to pickup graphene. The strong van der Waal's force between graphene and hBN allows graphene to leave the Si/SiO_2 surface and attach itself to the hBN on PDMS/PC film. Finally the stack was aligned onto another hBN (bottom hBN layer) on the Si/SiO_2 substrate to form the hBN/graphene/hBN stack suspended on the polymer stack as shown in Fig. 2.5 (b and c). The fully assembled heterostructure was then placed onto a separate clean substrate with alignment markers. By heating the stage to 200°C and lifting the polymer stack, the PDMS film detaches from the PC film, which leaves the heterostructure coated with PC only on the

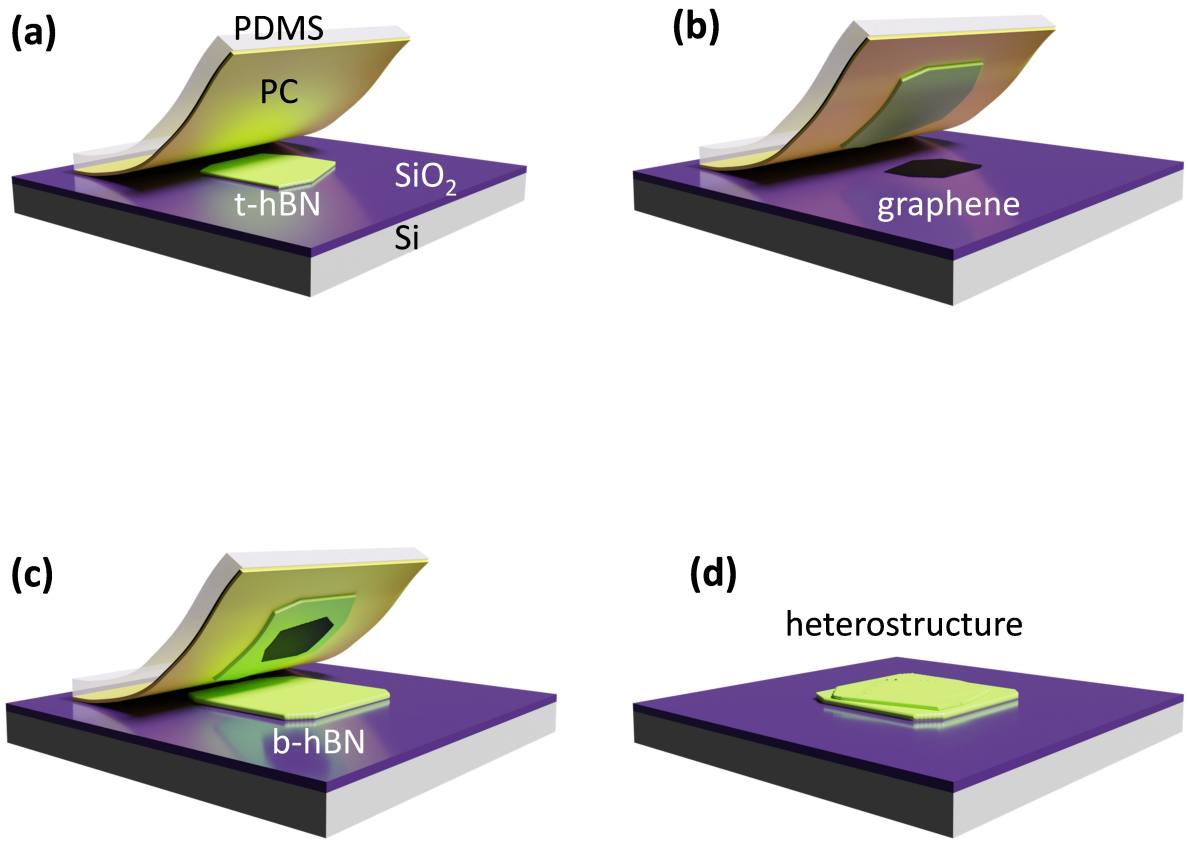


Figure 2.5: *The Process flow for assembling a 2D heterostructure (a) The polymer stack of PDMS/PC is brought in contact with top hBN to lift it from the surface of Si/SiO_2 substrate. (b) The top-hBN is aligned with the SLG and is picked up from the surface. (c) The top-hBN/graphene stack is aligned with bottom hBN to complete assembling the heterostructure(d).*

Si/SiO_2 substrate. The PC film was then dissolved in chloroform for 10 minutes to obtain the (hBN/graphene/hBN) heterostructure. The final assembled heterostructure, where the graphene layer is encapsulated within the hBN layers is shown in Fig. 2.5 (d).

A variety of different polymers have been studied to obtain high-quality heterostructures void of trapped impurities in between the 2D layers for studying their electrical properties.[77–80] Polycarbonate (PC) was used in this work as the transfer polymer due to its relatively lower melting point as compared to other polymers (eg., polypropelene carbonate (PPC)). The lower melting point in PC provided stacking of large area flakes while leaving minimal micro bubbles trapped between the consisting 2D layers. Fig. 2.6 shows a micro-

graph of an hBN/graphene/hBN heterostructure assembled using the visco-elastic stamping method discussed above.[74] One may also find microbubbles (encircled) in the fabricated heterostructure that are trapped at mechanical faults in the 2D stack. These microbubbles can be later eradicated by reactive ion etching discussed later in this chapter. It must be noted that one must not include a microbubble in the graphene electrical channel.

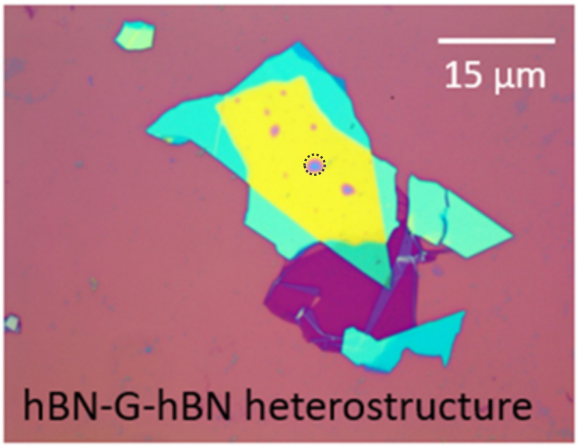


Figure 2.6: *Optical micrograph of an assembled hBN/graphene/hBN heterostructure on Si/SiO_2 (280 nm). Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

Electron beam lithography and Reactive Ion Etching

The hBN/graphene/hBN hetero-structures (as shown in Fig. 2.6) were then subjected to electron-beam lithography (EBL) and reactive ion etching (RIE) techniques to define the dimensions of the active channel of the HGFET. The etching was made in such a way to form a nano-wedge type structure for metallization of graphene to aid in creating an exposed edge while most of the graphene was encapsulated by hBN. This special graphene-metal contact is called as "1D contact". The process flow for etching a hetero-structure with defined channel length (l) and channel width (w) with 1D metal contact is shown in Fig. 2.7. The substrate containing the heterostructure was first spin-coated with Poly(methyl methacrylate) (PMMA 495K A3 and 950K A3) electron beam resist (positive) (see Fig. 2.7(a)), commercially available from Microchem. Electron beam patterning was performed on the substrates using an

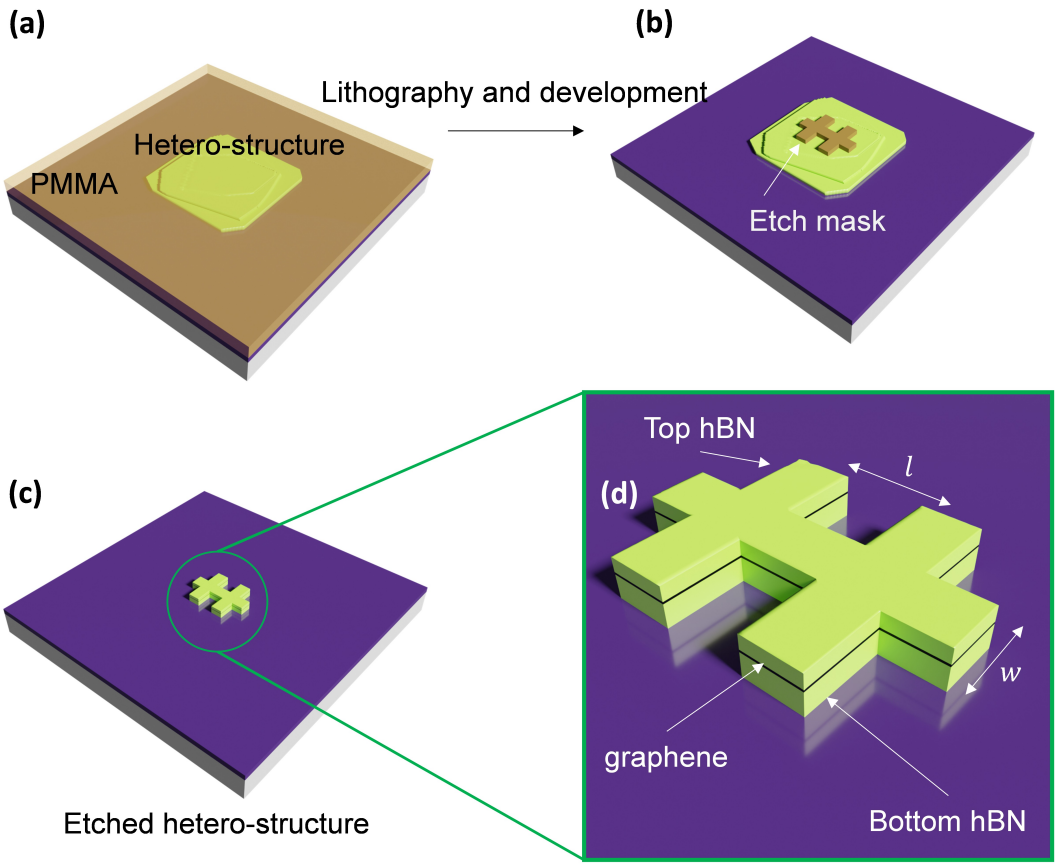


Figure 2.7: *Schematic of EBL and RIE process. (a) The wafer containing the hetrostructure is spin coated with PMMA. (b) Electron beam lithography and development is performed to form the PMMA etch mask. (c) Reactive ion etching removes the exposed region, followed by cleaning the etch mask with acetone.(d) A magnified schematic of the etched heterostructure showing device shape and dimensions* (l, w) *and exposed graphene edges.*

FEI Nova NanoSEM 450 scanning electron microscope (SEM) with Nano Pattern Generation System (NPGS) capability. The pre-patterned alignment markers on the substrate were used to steer the electron beam into the required position, and pattern the heterostructure. The samples were then developed in MIBK:IPA (1:3) solution to expose the regions irradiated with the electron beam, while the non-irradiated regions remained on the heterostructure as shown in Fig. 2.7(b). The presence of PMMA over the heterostructure protects the structure and is used as etch mask for the RIE process, while the regions not covered by PMMA are etched away.

Reactive Ion Etching (RIE) was performed on the samples containing the heterostruc-

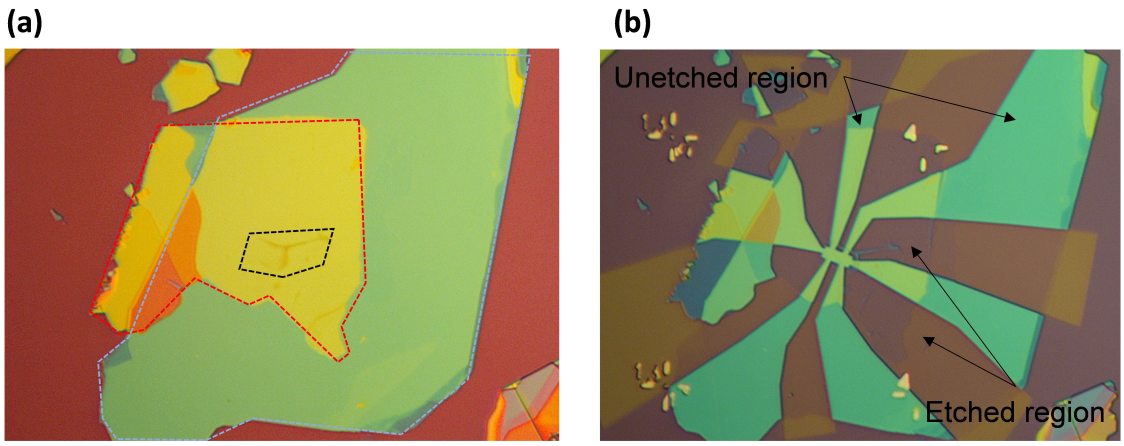


Figure 2.8: *(a) Optical micrograph of an assembled hBN/graphene/hBN heterostructure showing graphene (black dots), top hBN (red dots), and bottom hBN (blue dots). (b) Etched heterostructure after EBL, development, and RIE processes.*

tures using an Oxford Instruments PlasmaPro 80 RIE tool. Following the RIE step, the PMMA mask was removed from the substrate by soaking the sample in acetone for 6 hours. Fig. 2.7(c) shows a schematic of an etched hetero-structure on the substrate with a well defined shape after the removal of PMMA etch mask. Fig. 2.7(d) shows a magnified view clearly displaying the device dimensions (l, w) and the exposed graphene edges available for metal contact fabrication. The full detailed process flow for EBL and RIE (gas composition and plasma properties) can be found in Apendix D. Fig. 2.8 shows the micrographs of an SLG encapsulated within hBN (a) and micrograph of the heterostructure after the RIE process (b) clearly labeling the etched regions.

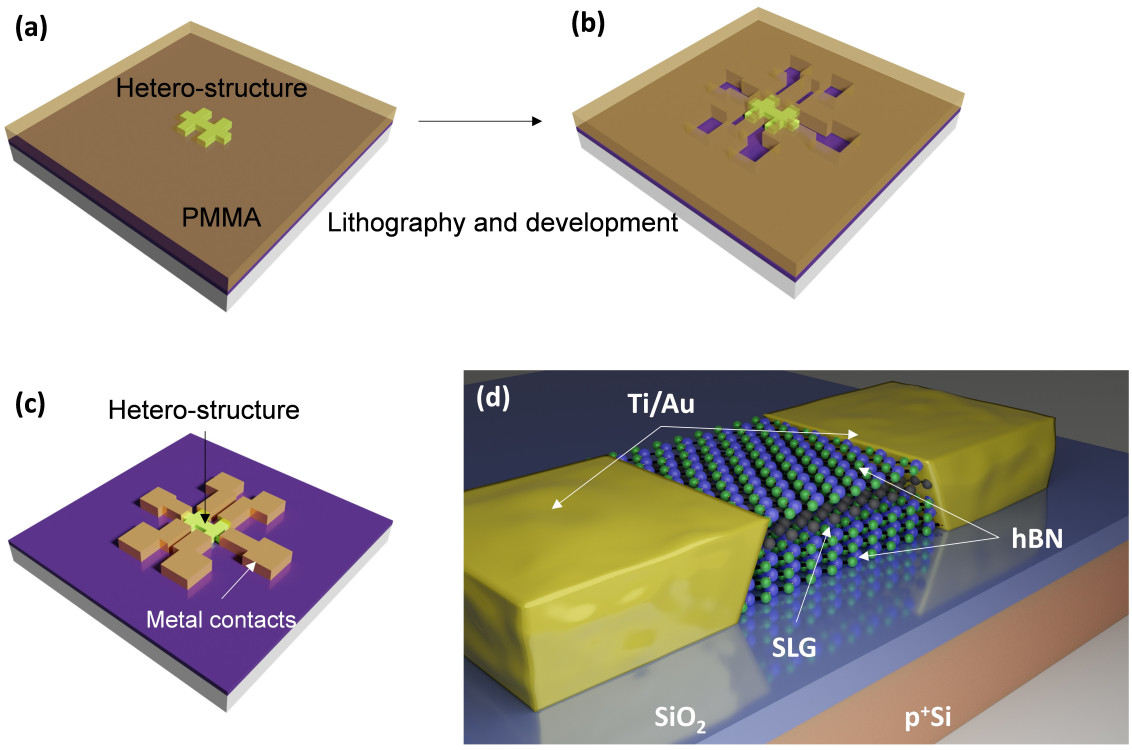


Figure 2.9: *Electron beam lithography and metallization process flow. (a) The wafer is spin coated with PMMA (b) followed by EBL and development to open areas intended for metal deposition. A second round of RIE is performed to open vias through top hBN and graphene followed by ellectron beam metal evaporation. (c) Schematic of a fabricated HGFET. (d) A high magnification of a schematic showing the edge contact to graphene layer in HGFETs.*

Electron Beam Lithography,metal deposition, and metal liftoff

A second set of EBL was performed on the etched heterostructures to fabricate metal contact electrodes to the graphene channel. Fig. 2.9 shows the process flow for fabrication of the electrical contacts and a schematic diagram of the HGFET device. The substrate containing the etched heterostructure is spin coated with PMMA (495K A3 and 950K A3) (see Fig. 2.9(a)), followed by exposure to electron beam lithography to pattern the contact regions. The exposed regions are then removed by using a developer solution (MIBK:IPA 1:3) to open up vias, as shown in Fig. 2.9(b). Note that during the first round of etching process, the regions intended for electrical contacts are not etched and are labeled as "Un-etched region" in Fig. 2.8(b). These unetched regions are then patterned using EBL for the second time and etched for making electrical contacts to the patterned graphene channel

encapsulated within hBN. By comparing the micrographs in Fig. 2.10 (a) and Fig. 2.8 (b), one may observe the etched vias with the top hBN and graphene removed after the second round of RIE process, exposing the edges of graphene available for one-dimensional (1D) metal contact fabrication.

Metal deposition and liftoff

Metal evaporation was performed by using an electron beam metal evaporator (TEMESCAL FC2000), where Ti/Au metal layers of 5nm/85nm thicknesses were deposited on the fabricated sample (see Appendix E for detailed metallization procedure). The samples were then soaked in acetone for 8-10 hours for metal liftoff, leaving behind the fabricated HGFET device. The schematic models of the fabricated HGFETs are shwon in Fig. 2.9(c) and (d) at high magnification, illustrating the material stacks and the source-channel-drain configuration. A micrograph of a fabricated HGFET is also shown in Fig. 2.10 (b). Finally, to complete the fabrication process of the HGFETs, the samples were annealed at 300°C in a H_2/Ar environment for 2 hours to reinforce the metal contact to the graphene channel and reduce any unwanted contact effects. This was performed in a vaccum chamber with a steady flow of H_2 (5%)/Ar(95%) gas flow at 2 sccm.

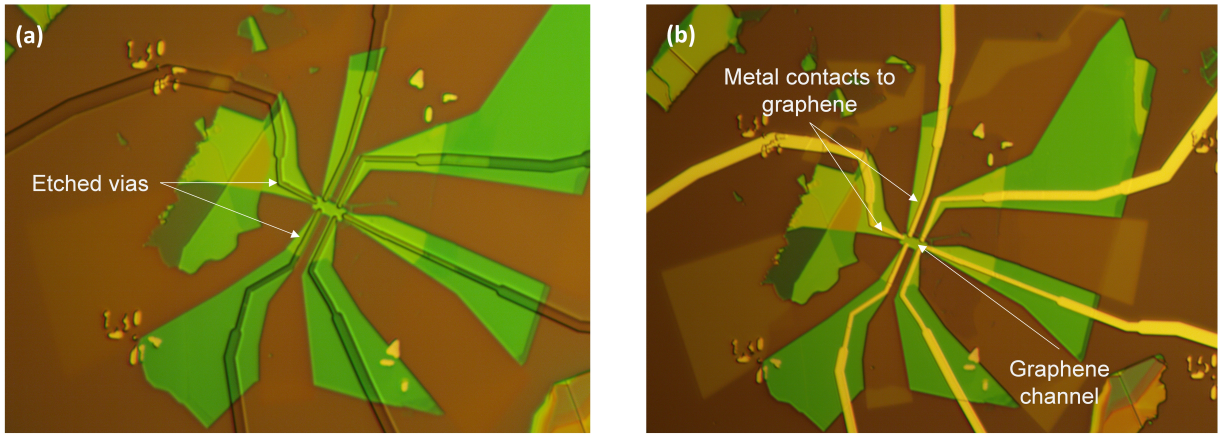


Figure 2.10: *(a) Optical micrograph of etched hetero-structure with vias intended for metal contacts to form 1D edge contact. (b) High magnification image of a HGFET showing the metal contact regions and the graphene channel.*

2.2.2 Fabrication of Graphene Heterostructure Field Effect Transistors Encapsulated in Monoisotopic hBN

Section 2.2 covered the process flow for fabrication of HGFETs encapsulated in hBN. Different boron isotopic purities of hBN were obtained from Edgar group at Kansas State University for fabricating three different classes of devices where a single layer of graphene was encapsulated between $h^{10}BN$, $h^{11}BN$, and naturally available hBN, respectively. To fabricate the devices, the isotopically pure hBN flakes were exfoliated separately onto respective cleaned substrates to avoid any cross-contamination. A similar blue tape method elucidated in section 2.2 was used for exfoliating the monoisotopic hBN as well as the graphite crystals to obtain SLGs. Each heterostructure was then assembled separately using the 2D transfer station through viscoelastic stamping method as explained earlier. Special care was taken to label the substrates containing the hBN flakes of various isotopic purities to prevent the isotopic mismatch of hBN below and above the SLG flakes. The samples were then subjected to electron beam lithography and reactive ion etching processes similar to steps shown in Fig. 2.7. The etched isotopic heterostructures were then subjected to subsequent electron beam lithography and reactive ion etching, similar to steps shown in Fig. 2.9, to expose the graphene contact region for metallization. Metal contacts were then fabricated by electron beam metal deposition followed by metal liftoff. Similar to HGFETs with natural hBN, devices with isotopic hBN were also annealed at high temperature (300°C) in H_2/Ar environment to improve the quality of metal contacts. The detailed material characteristics, electrical transport and LFN characterization for monoisotopic devices are assimilated in Chapter 5.

The 2D-HGFET devices fabricated by using the steps detailed in section 2.2 demonstrated $\approxeq$ 95% yield with high reliability.

Chapter 3

Electrical Measurements and Characterization Setup

Electrical transport measurements and low frequency noise (LFN) measurements are carried out extensively on the fabricated HGFET devices to study detailed insight on the charge carrier dynamics. This understanding of carrier dynamics provides crucial information about material quality, crystal vibrations, charge impurities, electrical band structure etc.

3.1 Electrical transport measurements

3.1.1 Three terminal measurements

A three terminal electrical transport measurement designed for HGFETs is similar to the conventional transistor measurements laid out in Fig. 1.4(a) in section 1.3. The circuitry for a device measurement is shown in Fig. 3.1 (a) where the device under test (DUT) is electrically connected to three terminals labeled as source, drain and gate. The drain and the gate terminals are used to apply voltage biases with respect to grounded source terminal and are termed as V_{ds} and V_{gs}, respectively. The corresponding current readouts recorded between the drain-source and gate-source terminals are labeled as I_{ds} and I_{gs}, respectively, as labeled in Fig. 3.1. The micrograph of an HGFET, illustrating the graphene channel,

source, drain, and the highly p-doped silicon as global back gate terminals is illustrated in Fig. 3.1(b).

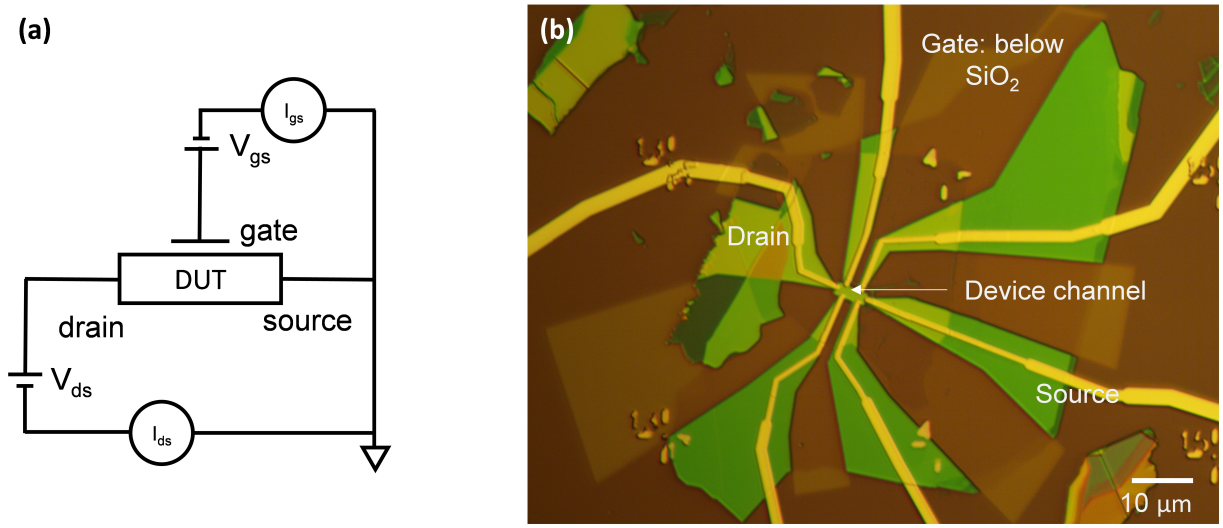


Figure 3.1: *(a) Circuit diagram for measuring the electrical transport in a FET in three terminal device. (b) A micro-graph of a fabricated device labeled with source, drain, and gate terminals. Metal terminals are fabricated to the channel for four-probe resistivity measurements (five terminal, including the gate).*

3.1.2 Five terminal measurements

With a given gate voltage, the resistance of two terminal (source and drain) device can be calculated by: $R_{DUT} = \frac{V_{ds}}{I_{ds}}$. It must be noted that the resistance calculated in this method represents the total resistance of the DUT, which may or may not be solely the resistance of the graphene channel. The resistor network of a DUT (a FET) is illustrated in Fig. 3.2 where the total resistance is the sum of channel resistance (R_{ch}) and the two contact resistances (R_c). Performing a three-terminal measurement to extract the channel resistance works well when $R_c << R_{ch}$. However, if $R_c \gtrsim R_{ch}$, the contacts become the dominant factor in the DUT's transport characteristics, effectively masking the channel's properties. In such cases, a five-terminal measurement is performed to accurately extract the transport properties of the FET's channel.

In a five terminal measurement, additional two leads are attached to the device to mea-

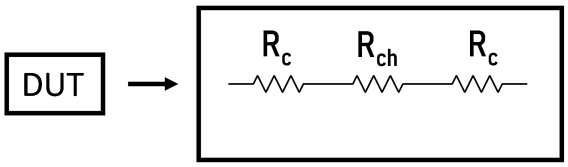


Figure 3.2: *The resistor network inside a DUT.*

sure the potential difference between two sections of the transistor's channel. The circuitry for five-terminal measurement scheme is shown in Fig. 3.3(a), illustrating the additional two leads connected through a voltmeter. The high load resistance of a voltmeter prevents any current from flowing through the sense lines, thereby aiding in an accurate potential difference measurement across the channel (V_{sense}). Fig. 3.3(b) shows the same HGFET shown in Fig. 3.1 with the sense terminals labeled as $sense_1$ and $sense_2$. The channel resistance is then calculated by: $R_{ch} = \frac{V_{sense}}{I_{ds}}$. The difference between the five-terminal resistance and three-terminal resistance can then be calculated to extract the resistance of the contacts (R_c). Both three terminal and five-terminal characterization techniques have been used to study the electrical transport in different HGFETs in this dissertation.

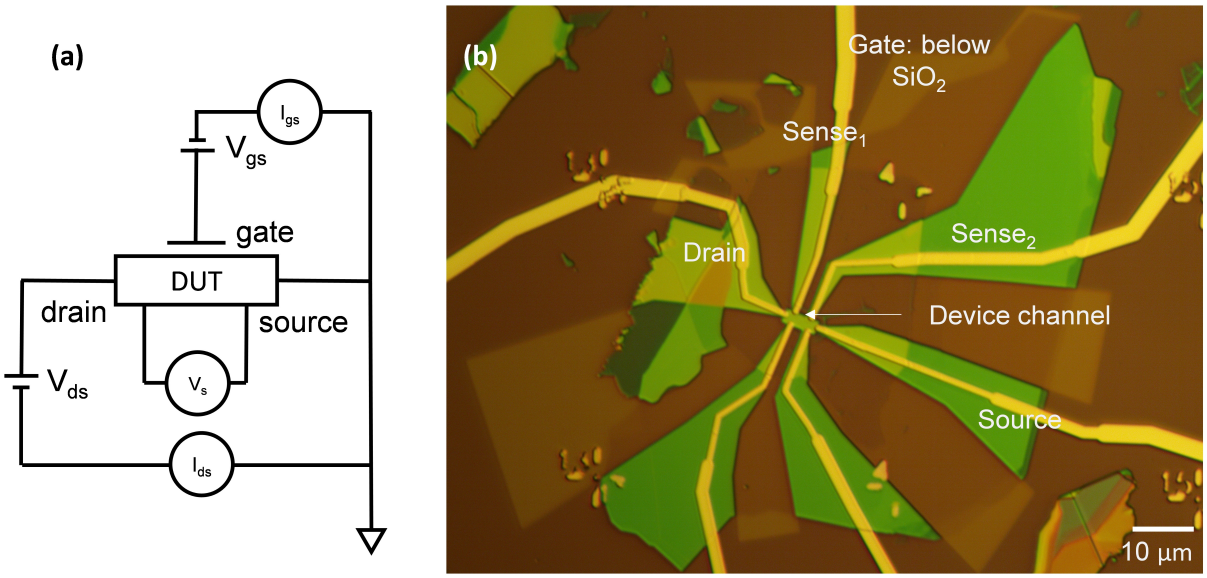


Figure 3.3: *(a) Circuit diagram for five terminal FET device (b) Optical micro-graph of a fabricated HGFET with the source, drain, gate and sense leads.*

3.2 Low frequency noise spectroscopy

Any signal (eg. I_{ds}, V_{sense}, etc.) across a DUT can be classified as an ideal signal if the recorded signal from the DUT at a fixed device configuration (fixed V_{ds} and fixed V_{gs}) is constant or time independent. However, in real world operations, any recorded electrical signal in a device is never constant. The true signal is overlaid with a time dependent signal fluctuation called as noise. The magnitude of these fluctuations generally depend on the source of these fluctuations and in some cases can be strong enough to mask the true signal. This phenomena of signal masking can be quantified by signal to noise ratio (S/N). Fig. 3.4 shows an illustration of an ideal signal (black) and a noisy signal (red) one would measure from an experiment. An extensive quantification of the recorded noise in the signal can be performed by using Fourier's theorem which states that any continuous function $f(t)$ can be expanded as an infinite weighted sum of sine and cosine functions. It can be seen from Fig. 3.4 that the recorded signal can be a non-periodic continuous signal in time. Performing Fourier transform on the recorded signal allows us to investigate frequency components in the recorded signal providing further insight into the origins of the recorded noise. This process can be facilitated by using a few electrical signal analyzers like a lock-in amplifier or a FFT spectrum analyzer with two separate methods of signal processing.

3.2.1 Lock-in Method

The lock-in method is a signal detection technique used to isolate components of the signal at a specific reference frequency and phase. This method is called phase-sensitive detection, where noise components away from the reference frequency are rejected and do not affect the measured signal. This method involves using an oscillating reference and applied signal, followed by signal mixing (mathematical product) that isolates the required signal at desired frequencies. In this method, a reference sinusoidal wave ($V_L sin(\omega_L t + \theta_{ref})$) is multiplied with the signal sinusoidal wave ($V_{sig} sin(\omega_r t + \theta_r)$), where V_L and V_{sig} are the amplitudes, ω_L and ω_r are angular frequencies, and θ_{ref} and θ_r are phases of reference and signal AC waveforms, respectively. The product results in two AC signal with sum and difference frequency of

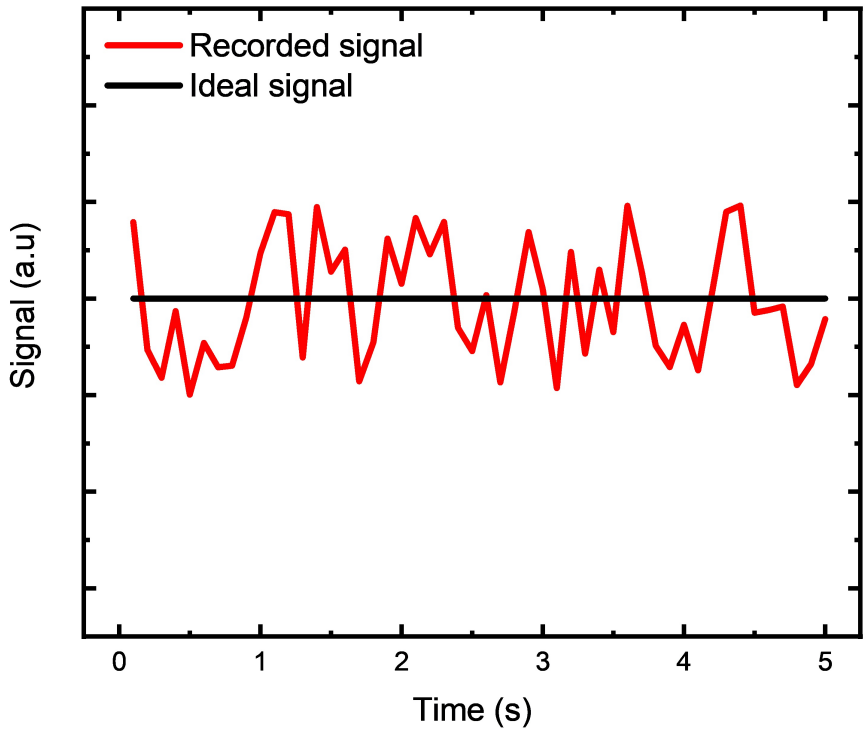


Figure 3.4: *Illustration of an ideal (black) and noisy rcorded signal (red).*

$(\omega_r + \omega_L)$ and $(\omega_r - \omega_L)$, respectively and are given as:

$$\begin{aligned} V_{out} &= V_{sig}V_L sin(\omega_r t + \theta_{sig})sin(\omega_L t + \theta_{ref}) \\ &= 1/2V_{sig}V_L cos([\omega_r - \omega_L]t + \theta_{sig} - \theta_{ref}) - \\ &\quad 1/2V_{sig}V_L cos([\omega_r + \omega_L]t + \theta_{sig} + \theta_{ref}) \end{aligned} \tag{3.1}$$

the angular frequency $\omega = 2\pi f$, where f represents the characteristic frequency. By setting the lockin reference frequency to the same value as the signal frequency ($\omega_L = \omega_r$), the difference in the signal becomes essentially a DC signal. The output signal is then passed through a low-pass filter to remove the sum component, resulting in the DC signal proportional to signal amplitude: $V_{out} = (1/2)V_{sig}V_L cos(\theta_{sig} - \theta_{ref})$. One can further set $\theta = \theta_{sig} - \theta_{ref}$=0 to obtain $\mathrm{V}_{out} \propto \mathrm{V}_{sig}$.

The noise in a signal can then be measured by extracting the standard deviation (root mean square of squared variations) of the output signal. Furthermore, the lockin amplifier

measures signals at frequency $f = f_r - f_L$. Normally, the f_r is set equal to f_L, while the response to the change in f_L is used to obtain the requisite noise spectrum.

3.2.2 FFT Spectrum Analyzer Method

In an FFT (Fast Fourier Transform) spectrum analyzer, a time-varying signal is transformed into its frequency domain by performing FFT operation on the recorded signal. The FFT analyzer digitizes the input signal at a very fast rate, where the input is generally a voltage signal from the DUT. The number of data points an FFT spectrum analyzer records must be 2^n, where n is an integer to satisfy FFT requirements[81]. Furthermore, Nyquist's theorem suggests that the sampling rate needs to be more than twice the highest frequency component of the signal to accurately represent the input signal.[82–85] For an example, if a signal is sampled for 2^5 times at 1000 Hz, accurate frequency data can be represented up to 500 Hz with a resolution of $\frac{1000}{1024} = 0.976$ Hz. To protect the feasibility (Nyquist's theorem) and to prevent long FFT calculations with large memory requirements, (which scales exponentially with recorded values), spectrum analyzers impose restrictions on the number of recorded data points. The spectrum analyzers used in this study (HP3588A and SR770) always take 1024 timed samples to yield a 400 point frequency spectra. Hence, the frequency span for the above measurement will be between 0Hz to $0.976 \times 400 = 390.4$ Hz.

Naturally, there are advantages and disadvantages to using either the lock-in method or the spectrum analyzer method for recording signals. In the above example, the resolution of the spectrum is restricted to 0.976 Hz which corresponds to the sampling rate, thus creating a limitation when searching for a frequency component at exactly 1 or 1.5 Hz. However, by using the lock-in method, the frequency resolution can be finely tuned by adjusting the lock-in reference frequency as needed. The spectrum analyzer, on the other hand, compensates the loss of resolution with it's high speed nature of spectrum acquisition. In the given example, it only takes $\cong$ 1s to obtain a spectrum with a frequency span of $\approx$ 400 Hz.

Power spectral density (PSD) quantifies the noise in a DUT. It can be calculated by normalizing the equivalent noise bandwidth from the measured variance (square of standard

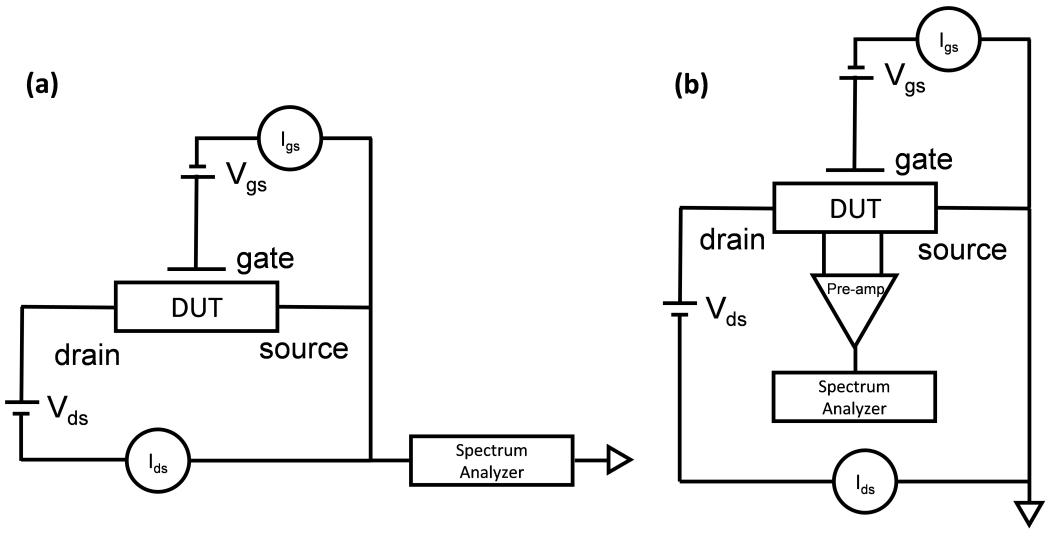


Figure 3.5: *Measurement circuitry for recording noise in (a) three terminal and (b)five terminal configuration.*

deviation) of the signal. Normalized PSD in a voltage signal can be quantified as:

$$PSD = \sqrt{\frac{V_{rms}^2}{linewidth}} \tag{3.2}$$

where V_{rms}^2 is the root mean square value of oscillations at the frequency of interest, contributing to the noise fluctuations. The normalization with the linewidth determines the density of signal fluctuation across different bandwidths (per Hertz). The equivalent noise bandwidth (linewidth) can be calculated in both lock-in and spectrum analyzer methods from the filter settings and sampling rate of the instruments, respectively. Power spectral density is generally represented by $V/\sqrt{Hz}$ for voltage noise spectra and $I/\sqrt{Hz}$ for current noise spectra.

3.2.3 Three-wire and Five-wire LFN Measurement

Similar to the electrical transport measurements, noise measurements on transistor devices can also be performed in two different schemes. The circuit diagrams for three and five terminal noise measurement techniques are shown in Fig. 3.5(a) and (b), respectively. One may notice the additional spectrum analyzer component in the circuit diagram as compared

to the transport measurement scheme depicted in Fig. 3.1 and 3.3. The noise recorded by the spectrum analyzer can originate from various noise sources, and can be broadly classified into extrinsic and intrinsic noise sources. Although the extrinsic sources (noise originating outside DUT) do not exhibit $1/f$ behavior, their magnitude may be larger than intrinsic noise sources in some cases, which may mask the intrinsic noise sources. The extrinsic sources can be mitigated through appropriate circuit design, radiation shielding, electrical grounding to name a few. The detailed measures taken to remove extrinsic sources in this study are covered in Appendix F.

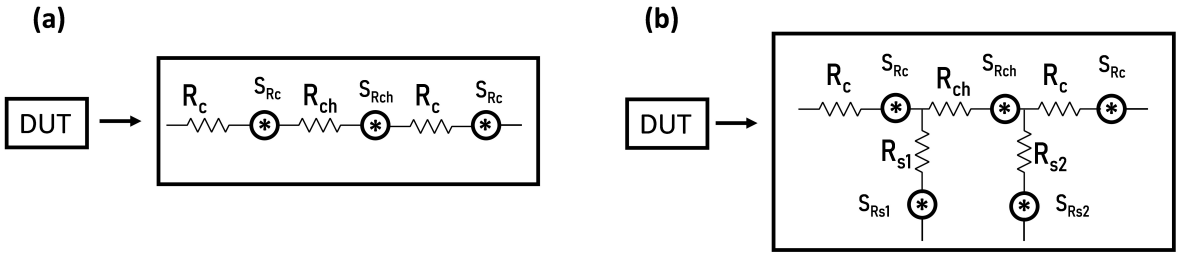


Figure 3.6: *Resistor and noise source network of a DUT in three terminal (a) and five terminal (b) configuration.*

The intrinsic noise sources originate from within the DUT and generally exhibit a $1/f$ nature where the DUT contains a semiconducting device which cannot be mitigated by any circuit design or radiation shielding. The $1/f$ nature of the noise spectrum can be recorded and analyzed to understand the sources of $1/f$ noise in the semiconductor device. It must be noted that special measures must be taken to accurately distinguish between the noise originating from contact electrodes and the noise from the channel in the DUT. Every resistor inside the DUT can be associated with a fluctuating voltage source with it's ideal resistance. Fig. 3.6(a) and (b) show the ideal resistors and noise network in a DUT for three terminal and five terminal geometries, respectively. For example, the contact resistances (R_C) and channel resistance (R_{ch}) in both three-terminal and five-terminal geometries have noise sources S_{RC} and S_{Rch} associated with them, contributing to the total noise measured by a spectrum analyzer. Even though the five terminal noise measurement technique removes the contribution of S_{Rc} in the measured spectrum, the contact resistances for the sense

leads (R_{s1} and R_{s2}) generate voltage fluctuations S_{Rs1} and S_{Rs2} that the spectrum analyzer identifies while recording the noise spectrum. All of the above factors make low frequency noise measurements in the DUT channel (S_{Rch} in R_{ch}) a challenging task, thereby requiring a sophisticated circuit analysis for HGFET device as shown in the following section.

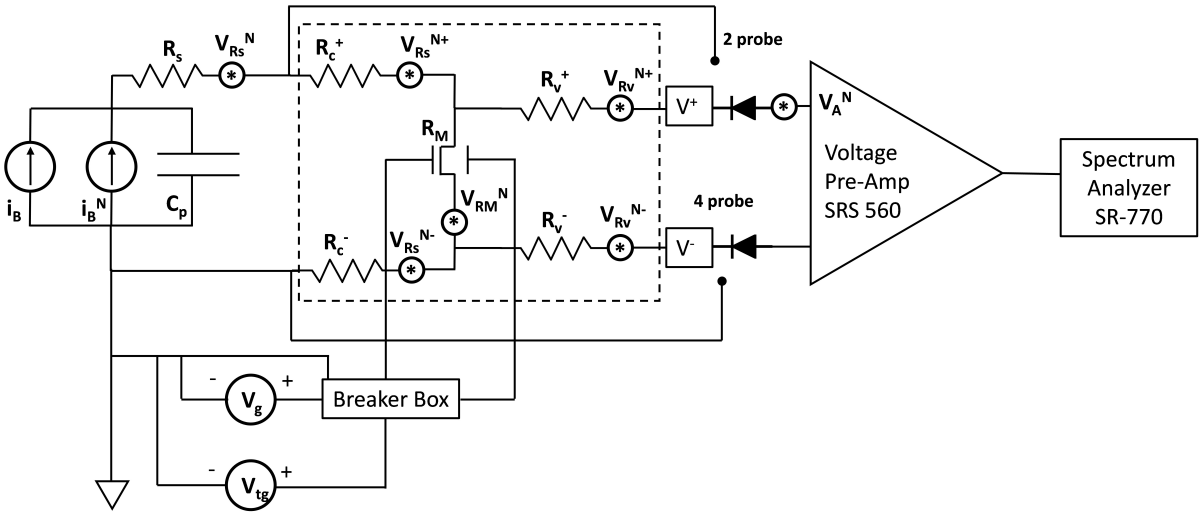


Figure 3.7: *Combined circuit arrangement for measuring three-terminal and five-terminal transport and low-frequency noise.*

3.2.4 True Channel Noise Extraction

The true channel noise in the HGFET device can be extracted by performing a Thevenin equivalent circuit analysis on the measured three-terminal and five-terminal noise spectrum of the DUT.[86] The noise spectrum and electrical transport in the HGFET were recorded in both three-terminal and five-terminal geometries. The circuitry used for this measurement is shown in Fig. 3.7. The fabricated HGFET is designated by the dashed box, with the constituent resistors and voltage noise sources from the channel and the contacts. The FET channel resistance, denoted by R_M, can be modulated by a back gate (V_g) and a top gate (V_{tg}) (if present), both provided by Keithley 2400 source measurement units (SMU), while the voltage noise in the channel is denoted by ${V_{RM}}^N$. The contact resistances in the DUT for the source-drain leads are given by ${R_C}^+$, ${R_C}^-$ and for the sense leads are given by ${R_V}^+$

and ${R_V}^-$, respectively. These resistors have associated voltage fluctuations, represented as ${V_{Rs}}^{N+}$, ${V_{Rs}}^{N-}$, and ${V_{Rv}}^{N+}$, ${V_{Rv}}^{N-}$, for source-drain and sense leads, respectively. In this measurement scheme three separate noise spectra acquisitions are performed: 5-terminal, 3-terminal, and zero-bias. The 5-terminal measurement corresponds to a measurement by sourcing a current through the main channel of the device followed by voltage noise reading between the sense leads. The 3-terminal measurement corresponds to sourcing a voltage bias across the DUT followed by the acquisition of noise in the drain current (I_{ds}). A zero-bias noise measurement is similar to a 5-terminal noise measurement, where the current source is set to 0A. The necessary current and voltage sources provided by a Keithley 2400 SMU also shows current fluctuation denoted by I_B and ${I_B}^N$, respectively. The source is fed through a low pass RC filter with capacitance C_p and resistance R_s. In the five-terminal measurement, the potential difference across the device channel is measured using a Stanford Research Systems SRS 560 voltage pre-amplifier in differential mode ($V^+ - V^-$), connected to the sense leads. The noise spectrum is then recorded using a Stanford Research System SRS770 network analyzer (spectrum analyzer). On the other hand, in the three-terminal geometry, the drain current across the complete DUT is converted into a voltage signal by using a DL1211 transimpedance amplifier. This voltage signal is then recorded using a DMM and a network analyzer. A zero bias noise spectrum is recorded by setting all the terminals (drain and gates) to zero or grounding all terminals.

The circuit shown in Fig 3.7 can be solved by assuming independent noise sources to extract the true device channel spectrum (S^{R_M}). In order to calculate S^{R_M}, five-terminal, three-terminal and zero bias noise spectrum were recorded. The contact resistances and sense lead resistances are simplified as : $R_C = {R_C}^+ + {R_C}^-$ and $R_V = {R_V}^+ + {R_V}^-$. The net Thevenin equivalent noise for the respective five-terminal (S_4), three-terminal (S_2), and zero bias (S_0) spectra can be written as[86]:

$$
\begin{aligned}
S_4 &= S^{R_V} + S^A + A\left(S^{R_S} + S^{R_C}\right) + BS^{R_M} \\
S_2 &= S^A + CS^{R_S} + D\left(S^{R_C} + S^{R_M}\right) \\
S_0 &= S^A + S_0^{R_M} + S^{R_V}
\end{aligned}
\tag{3.3}
$$

where S^A, S^{R_S}, S^{R_C}, and S^{R_V} are the spectral densities corresponding to the equivalent noise sources from amplifier (A), R_S, R_C, and R_V, respectively. The coefficients in Eq. 3.3 are voltage divider components given by[86]:

$$
\begin{aligned}
A &= \left|\frac{R_M}{Z_S + R_C + R_M}\right|^2 \\
B &= \left|\frac{Z_S + R_M}{Z_S + R_C + R_M}\right|^2 \\
C &= \left|\frac{R_C + R_M}{Z_S + R_C + R_M}\right|^2 \\
D &= \left|\frac{Z_S}{Z_S + R_C + R_M}\right|^2
\end{aligned}
\tag{3.4}
$$

where Z_S is the complex impedance of the RC filter given as $Z_S = R_S - \frac{j}{2\pi f C_p}$. By solving the set of linear equations in Eq. 3.3 and Eq. 3.4, the noise spectrum in the HGFET channel is calculated as:

$$
S^{R_M} = \frac{-K}{D(A-B)}\{DS_4 + A(C-D)S_{Rs} + S_A - AS_2 - DS_0\} \tag{3.5}
$$

where $K = 1 - \frac{1}{1+A-B}$. It must be noted that S^{R_M} must be a positive quantity thus from Eq. 3.5 the five terminal and three terminal spectrum must satisfy:

$$
AS_2 > DS_4 \tag{3.6}
$$

Furthermore, the low pass RC filter must have a cutoff frequency similar to the equivalent

noise bandwidth, that is:

$$\frac{1}{2\pi R_S C_p} \leq 0.5Hz \tag{3.7}$$

This study uses both three terminal and five terminal transport and noise measurements to understand the underlying carrier physics in HGFETs. More relevant details used for the measurements will be specified during the discussion of data in the following chapters.

Chapter 4

Electrical Transport and Low Frequency Noise in Graphene Heterostructure Field Effect Transistors

Declaration: The findings of this chapter are assimilated from our two publications: "Behera, Aroop K., et al. ACS Applied Electronic Materials 3(9), (2021): 4126-4134." [74] and "Behera, Aroop K., et al. ACS Applied Nano Materials 7(11) (2024):12366–12375." [76]

Two single layer HGFET devices with 1D edge contacts were fabricated using the heterostructure assembly and EBL techniques explained in chapter 2. For convenience, the devices were labeled as "SLG device 1" and "SLG device 2", respectively. The heterostructures consisted of a bottom hBN flake with thickness of $\approx$ 50 nm, an SLG channel, and a top encapsulated hBN of thickness $\approx$ 50 nm and 20 nm, respectively. A heavily doped (p-type) Si substrate (ρ = 0.01 Ω cm) was used as the global back gate to modulate the carrier concentration in the SLG channel. The channel lengths in the fabricated devices were 9 and 6 μm, respectively, with a channel width of 2 μm. A plethora of characterization techniques were used to deduce the properties of the materials used in the fabricated HGFET

systems. These techniques include scanning tunneling electron microscopy (STEM), Raman spectroscopy, electrical transport, and low frequency noise, the later two contributing the majority of our discussions in this chapter. This chapter discusses the results and conclusions of the above mentioned experiments in our HGFETs fabricated using natural hBN (obtained from NIST, Japan). Similar electronic characterization techniques were also used for HGFETs fabricated with hBN comprising of various isotopic purity (obtained from Prof. Edgar's group at Kansas State University) and the corresponding results will be discussed later in chapter 5.

4.1 Scanning transmission electron microscopy

To confirm the purity of the material stack in our hBN/Graphene/hBN heterostructure, the structure was analyzed using annular dark field scanning transmission electron microscope (STEM) combined with electron energy loss spectroscopy (EELS). Fig. 4.1 (a) shows cross-sectional low-angle annular dark field STEM (LAADF STEM) micrograph of the heterostructure clearly showing the material stack of SiO_2, bottom, and top hBN. The single layer of graphene is difficult to isolate in the image due to its single atomic width. The high magnification image shown in Fig. 4.1(b) confirms the van der Waals, layer by layer, atomic stacking of hBN with a clean interface among bottom hBN, graphene and top hBN.

Fig. 4.2 (a) shows the element mapping by using EELS where the red box outlines the active region. Individual element maps are shown in Fig. 4.2 (b) clearly indicating the presence of a layer of carbon between the top and bottom hBN indicating the presence of an SLG between the bottom and top hBN films.

4.2 Raman spectroscopy and Raman mapping

Raman spectroscopy was also performed on the heterostructures to confirm the presence of a single layer graphene and verify the quality of heterostructure. Point spectroscopic measurements and Raman mapping were conducted by using a WITec Raman spectrometer

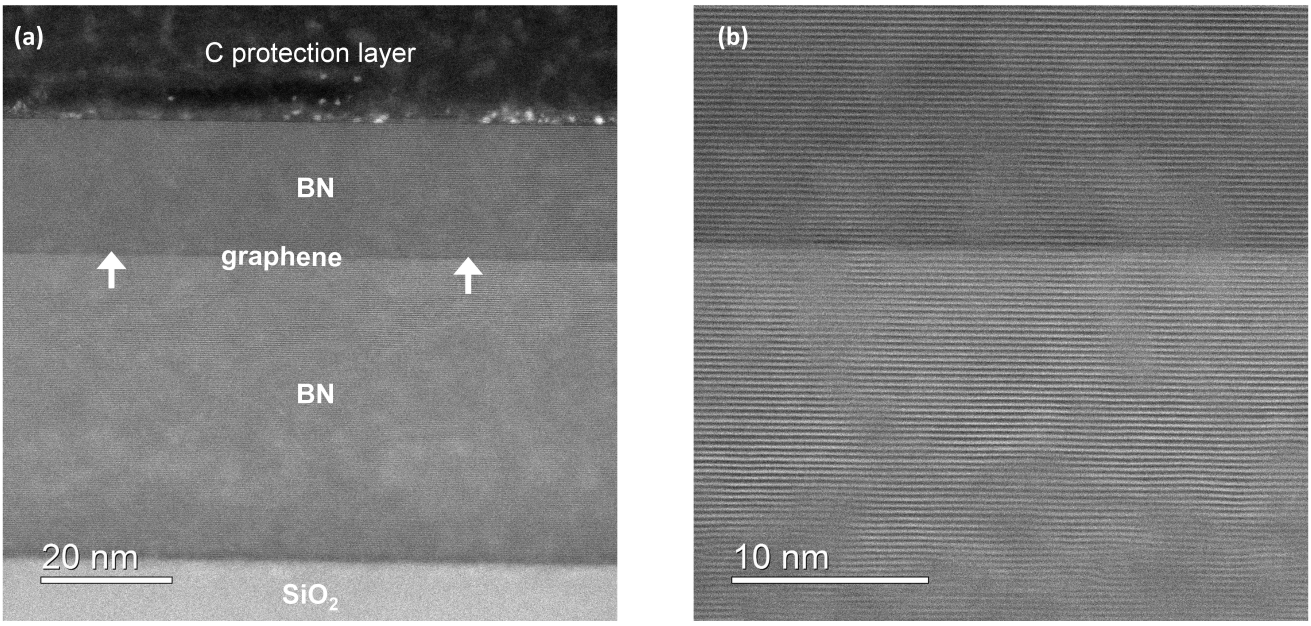


Figure 4.1: *(a) Low magnification STEM image of the hBN/graphene/hBN heterostructure. (b) Layer by layer stacking in 2D van-der Waals materials in the heterostructure. Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

where a 532 nm laser source was used with a 100× objective and 200μW power. Raman spectra were acquired using a 25s acquisition time per point, and maps were obtained using a 25 × 25 point grid with 200 nm step size.

Fig. 4.3 shows the Raman spectra and the Raman maps of fabricated devices. Fig. 4.3(a-b) shows point spectra acquired for the two HGFETs at two different channel positions. Fig. 4.3 (a) shows the characteristic Raman spectrum of a single layer of graphene with graphene's G and 2D vibration modes at ≈ 1580 cm^{-1} and 2700 cm^{-1}, respectively. The relative intensity of the vibration modes with $I_{2D} >> I_G$, further confirms the presence of a single layer of graphene in the two fabricated HGFETs, where I_{2D} and I_G are the intensity of the 2D and G bands, respectively. Fig. 4.3 (b) shows the the E_{2g} vibration mode of hBN used as the bottom and top encapsulation for the graphene channel at ≈ 1366 cm^{-1}. It can be seen that the intensity of the hBN E_{2g} peak is higher in device 1 as compared to device 2, which can be attributed to the presence of a relatively thick hBN as the top encapsulant

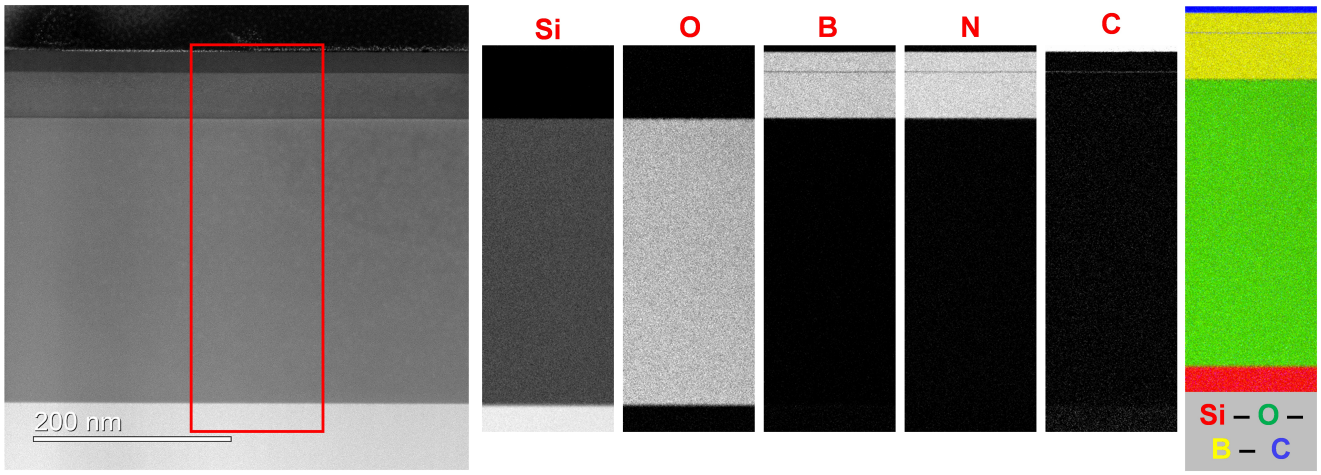


Figure 4.2: *EELS image of the hBN/graphene/hBN heterostructure. Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

in SLG device 1. The presence of a thicker hBN on the top allows a lower degree of laser interaction with graphene thereby reducing the intensity of the G and 2D peaks in SLG device 1 (see Fig. 4.3(a)). The electrical channel in the HGFETs were also be observed through Raman maps in a 5 μm $\times$ 5 μm region. The 2D and G vibration modes of the graphene layer present in the two devices are shown in Fig. 4.3 (c-f). The outlines of the devices are marked in green with the bright regions depicting the graphene channel whereas the dark regions either depicting absence of graphene or presence of metal contacts.

4.3 Overall device performance

Electrical transport measurements were performed by conducting standard transistor measurements on the fabricated HGFETs. Fig. 4.4 shows the electrical transport behavior recorded in SLG device 1. Fig. 4.4(a) shows the behavior of drain-source current (I_{ds}) as a function of drain-source voltage (V_{ds}) at different temperatures and applied gate voltages with an offset from the charge neutrality point (CNP) or gate overdrive voltage (V_g-V_{CNP}). The linear behavior of I_{ds} with V_{ds} (see Fig. 4.4(a)) confirms the presence of ohmic contacts

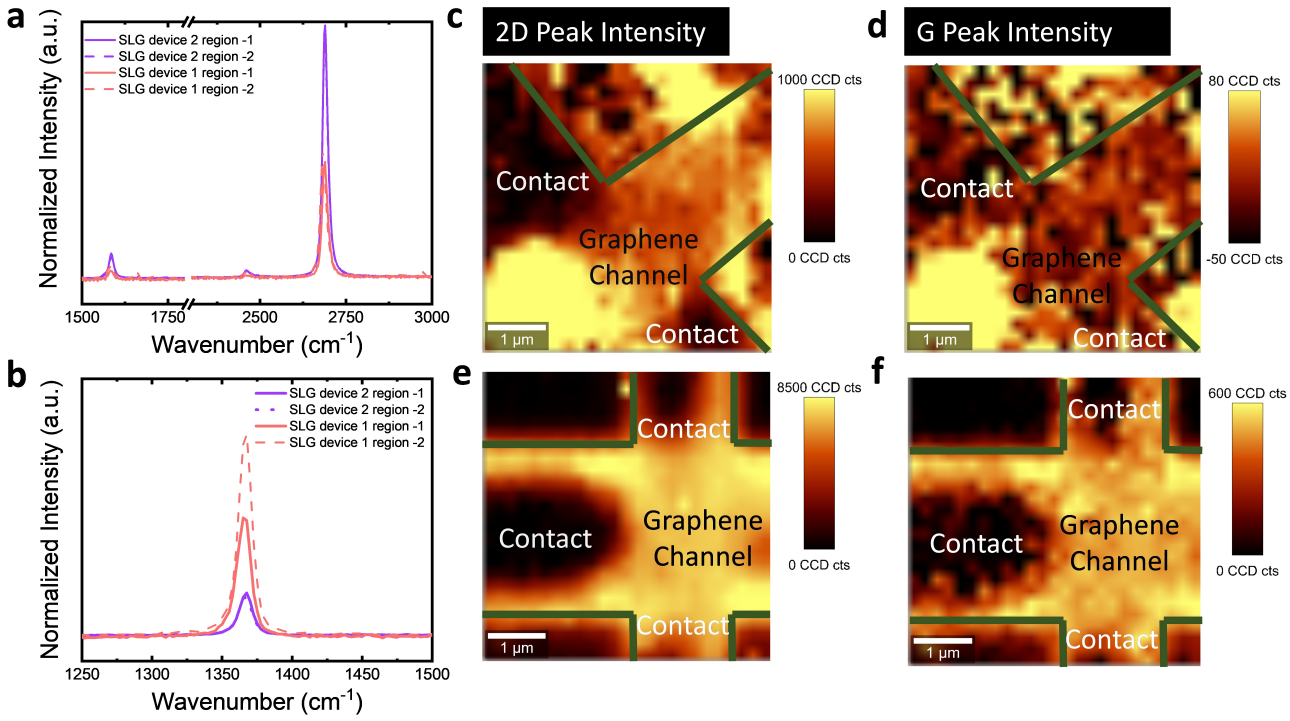


Figure 4.3: *(a)Raman spectrum of the heterostructure showing the graphene's G and 2D peaks in the heterostructure. (b) Raman spectroscopy showing the hBN E_{2g} peak. (c-f) Raman maps of G and 2D peaks in SLG device 1 and SLG device 2. Reprinted (adapted) with permission from Behera et al., Charge-inhomogeneity-mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. ACS Applied Nano Materials, 7(11), 12366–12375, 2024. Copyright 2024 American Chemical Society*[76].

between the contact metal (Ti/Au) and graphene. Higher current values are observed at high overdrive voltage suggesting gate dependent conductivity of the graphene device. Fig. 4.4(b) shows the measured I_{ds} as a function of applied overdrive gate voltages at a constant drain-source voltage bias (V_{ds}) of 5 mV at different operating temperatures. Fig. 4.4(b) further shows positive current values in both positive and negative overdrive gate voltages, confirming the ambipolar nature of graphene's electrical channel at all operating temperatures. The device shows two distinct behaviors at different overdrive voltages. From Fig. 4.4 (b) one can see the difference in the behavior of I_{ds} in the proximity of CNP and away from the CNP. This behavior can be seen more prominently by extracting the electrical resistivity of the single graphene layer as the function of overdrive gate voltage as shown in Fig. 4.5. The resistivity of the channel is maximum at the CNP and as the gate voltage increases (n-side)

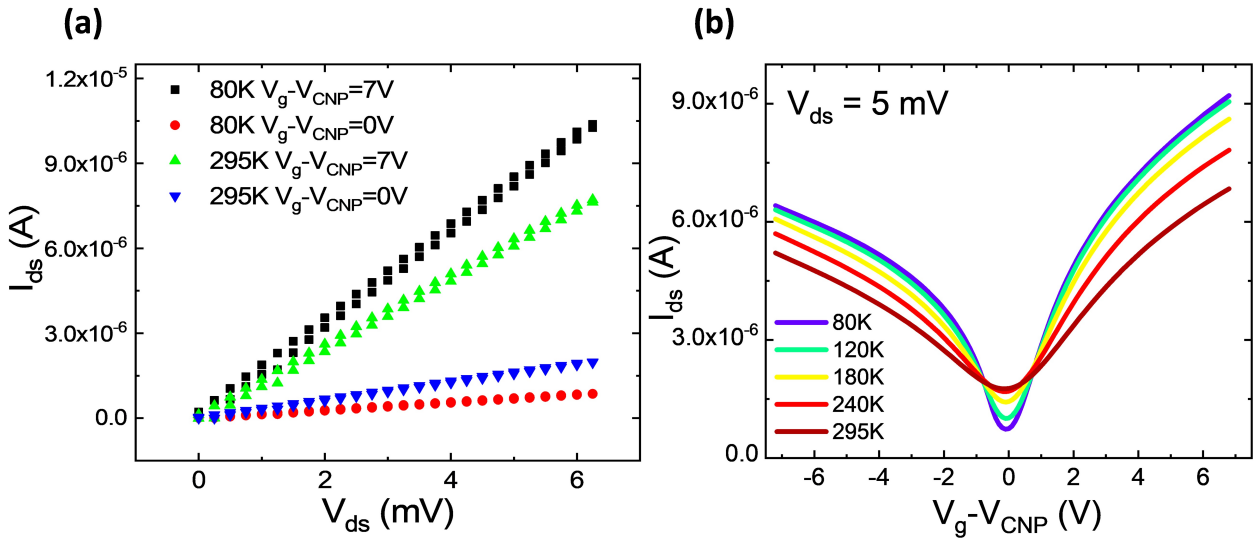


Figure 4.4: *(a) I_{ds} vs. V_{ds} plot for SLG 1 device at various gate voltages and operating temperatures. (b) I_{ds} vs. V_{gs} plots for SLG 1 device at different operating temperatures. Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

and decreases (p-side) the value of extracted resistivity reduces. Temperature dependency of the extracted resistivity shows that the highest resistivity value is obtained at the lowest operating temperature, which can be easily verified in Fig. 4.5. The temperature dependent resistivity of our HGFET qualitatively exhibits similar behavior to that reported for suspended graphene samples.[45] Approximately $|1.5V|$ beyond the CNP, the sample displays a metallic behavior where ρ increases with temperature, whereas an opposite trend (ρ reduces with increase in temperature) is observed at overdrive voltages close to the CNP (see Fig. 4.5).[74] This region close to the CNP is defined as charge residual region and is shaded in Fig. 4.5. In a highly carrier density-modulated system like graphene, it is important to define the region of interest for electrical transport and 1/f noise study. The following sections in this chapter delve into explaining the mechanisms that govern the electrical transport in graphene away from the charge residual region and within the charge residual region.

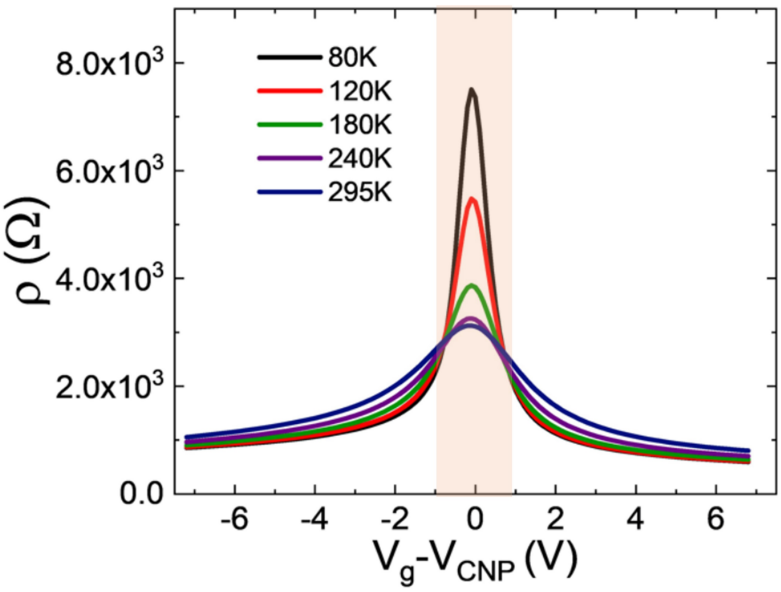


Figure 4.5: *Resistivity vs. V_g-V_{CNP} plot for the HGFET at different operating temperatures. Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

4.4 Electrical transport away from the charge residual region

In contrast to traditional FETs, which are typically probed in their ON state, here we explored the device operation away from the charge residual region. This region is achieved beyond a particular overdrive voltage (i.e., $|V_g - V_{CNP}| \geq V_{CNR}$, where V_{CNR} defines the boundary of charge residual region). In this regime, the channel's resistivity increases with the operating temperature (see Fig. 4.5). The behavior of channel conductivity ($\sigma = 1/\rho$) i.e., the transport of charge carriers away from the charge residual region is governed by diffusive transport where the charge carriers experience various scattering events that limit their electrical mobility. The conductivity of graphene away from the charge residual region

is a function of temperature (T) and gate voltage (V_g), given by:

$$\begin{aligned} \sigma(V_g) &\propto \frac{e^2}{h}\frac{n(V_g)}{n_i} \\ \sigma(T) &= \frac{g_s g_v e^2 E_F \tau}{4\pi\hbar^2} \end{aligned} \tag{4.1}$$

where e is the fundamental electronic charge, h is Planck's constant, n is carrier density, n_i is substrate charge impurity, $g_s = g_v = 2$ are the spin and valley degeneracy factors, E_F is the Fermi Energy, and τ is the scattering time given by:

$$\tau = \frac{\mu m^*}{e} \tag{4.2}$$

here, μ is the carrier mobility, and m^* is the effective carrier mass. The scattering time, τ defines the time taken by charge carriers between two successive collisions while traversing the graphene channel. As expected (from Eqn. 4.1), higher overdrive gate voltages increase the conductivity (or current) of the graphene channel as carrier density (n) in the channel increases (see Fig 4.4 (b)). The decrease in conductivity (or current) with increasing temperature can be explained by considering the factor τ, which plays a very important role in diffusive transport. These scattering events can originate from a plethora of mechanisms like charge impurities, crystallographic defects, carrier-carrier scattering, and crystal vibrations to name a few. The average carrier scattering (τ) can be written as a sum of constituent scattering mechanisms (τ_i) as:

$$\tau = \sum_{i=1}^{N} \tau_i \tag{4.3}$$

where N is the total number or types of scattering mechanisms.

By using Eq. 4.2 and 4.3, Matthiessen's rule can be obtained where the net effective mobility (μ_{eff}) can be written as:

$$\frac{1}{\mu_{eff}} = \sum_{i=1}^{N} \frac{1}{\mu_i} \tag{4.4}$$

where μ_i represents the mobility component from each corresponding scattering mechanism. The effective mobility in our device is represented by field effect mobility (μ_{FE}) where $\mu_{FE} \approxeq$

μ_{eff}. The field effect mobility in our HGFET were extracted by:

$$\mu_{FE} = \frac{g_m}{C_{ox} \times V_{ds}} \frac{L}{W} \tag{4.5}$$

where g_m is the transconductance, V_{ds} is the drain-source voltage (5.5 mV for these measurements), L is the channel length, W is the channel width, and C_{ox} is the oxide capacitance per unit area. The transconductance, g_m is calculated by (dI_{ds}/dV_g) and C_{ox} is given by (ϵ_{ox}/d_{ox}), where ϵ_{ox} is the dielectric constant of the gate dielectric and d_{ox} is the gate-dielectric thickness. It must be noted that in our back-gated devices, a thick layer of hBN exists between the SiO_2 and the graphene channel. Estimates show that by treating SiO_2 and the hBN as two series capacitors, the effective capacitance of the dielectric stack is set by SiO_2. For SiO_2, ϵ_{ox} is 3×10^{-11} F/m and with an oxide thickness ($\approxeq$ 300 nm), $C_{ox} = 1\times 10^{-4}$ F/m^2. Fig. 4.6 shows the extracted carrier mobility in the HGFET for applied gate voltages at different operating temperatures.[74] A mobility maxima of $\approxeq$ 60,000 cm$^2/Vs$ for electrons and $\approxeq$ 35,000 cm$^2/Vs$ for holes was obtained at room temperature (295 K) with a significant increase to $\approxeq$145,000 cm$^2/Vs$ 80 K for electrons and holes. Such high mobility values of charge carriers display the outstanding screening effects of the underlying hBN in reducing the effects of trapped charge impurities in SiO_2 substrate.

Similar to Fig. 4.5, different behaviors can also be observed in mobility within and away from the charge residual region. The charge residual region is bound by the blue and black dashed lines for 295K and 80K, respectively in Fig. 4.6. Away from the charge residual region as the gate voltage increases, the mobility values reduce. This temperature and gate voltage dependent behavior of electrical mobility can be understood from Eqn. 4.2 and 4.3. Lower temperatures lead to lower crystal vibrations thereby increasing the scattering time of carriers, which increases the carrier mobility. Moreover, as the gate voltage increases, the channel gets gradually saturated with increased number of charge carriers giving rise to lower scattering time among carriers resulting in lower carrier mobility.

When conducting temperature-dependent measurements, the total measured resistivity of the graphene channel can be separated into two components: temperature-independent

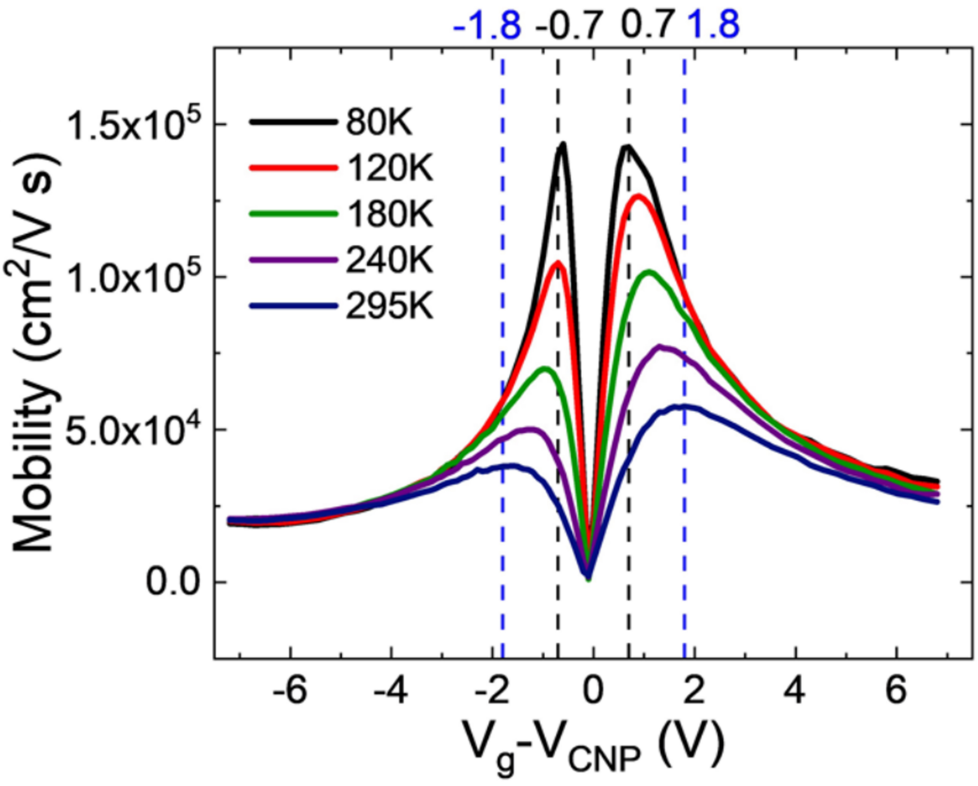


Figure 4.6: *Electrical mobility vs. V_g-V_{CNP} for the HGFET at different operating temperatures. Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

and temperature-dependent parts. Crucially, the temperature dependent components in the measured resistivity are generated from the charge carriers scattering from various crystal vibrations. Although, these crystal vibrations ideally freeze out at absolute zero temperature (0K), the finite operation temperature for the fabricated HGFETs, significantly impact carrier scattering and the measured electrical resistivity. The thermal energy associated with the crystal vibrations due to finite temperatures can be explained through characteristic quasiparticles known as phonons, which act as energy quanta for thermal energy or crystal vibrations. The scattering of charge carriers with crystal vibrations can now be seen as quasiparticle scattering between electrons and phonons that modulate the momentum of electrons in motion within the graphene channel or the graphene 2D electron gas. This phenomena is called as electron-phonon interaction (electron-phonon coupling) or electron-

phonon scattering.

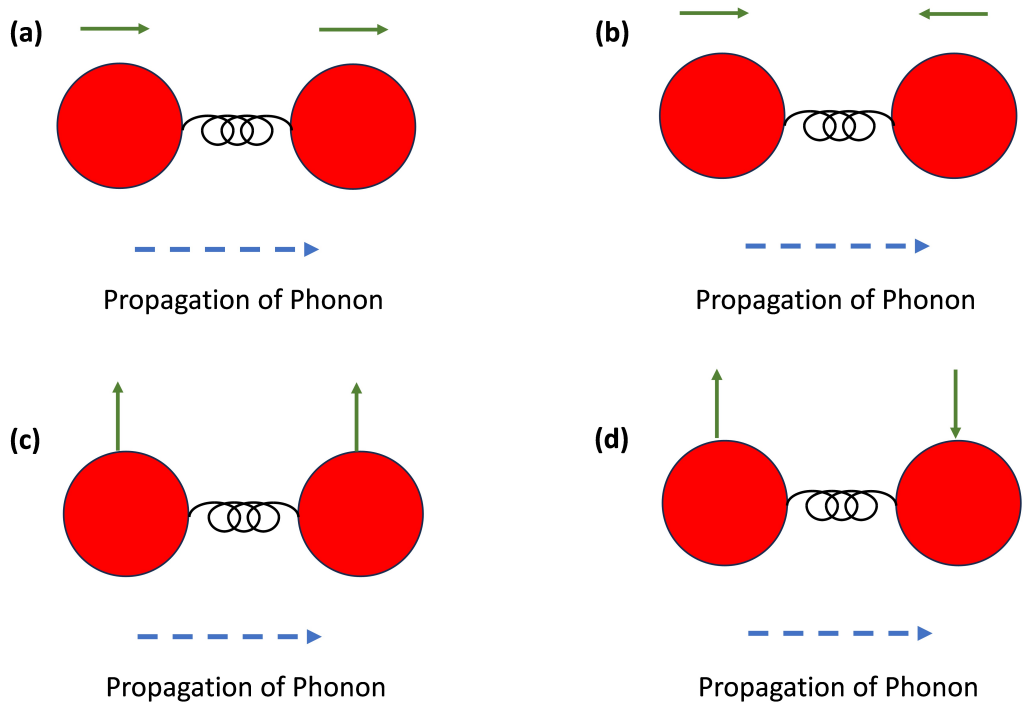


Figure 4.7: *(a)Longitudinal acoustic (LA) mode (b) Longitudinal optical (LO) mode (c) Transverse acoustic (TA) mode (d) Transverse optical (TO) mode.*

The phonons inside a crystal originate from different modes depending on the direction and the characteristic frequency of atomic vibrations. These modes can be classified into as either acoustic or with optical energy with longitudinal or transverse direction. Fig. 4.7 shows an illustration of different vibration modes for a diatomic molecule with the bond between the atoms approximated as a spring. Fig. 4.7(a,b) shows the atoms oscillating in the direction parallel to the propagation direction of the phonons. These are classified as longitudinal phonons. On the other hand, Fig. 4.7 (c,d) shows transverse modes where the atoms oscillate perpendicular to the direction of propagation. Furthermore, Fig 4.7 (a,c) shows acoustic modes where both atoms oscillate in phase whereas (b,d) shows optical modes where atoms oscillate out of phase. Generally optical modes have higher energy associated with them as compared to acoustic modes and do not interact with charge carrier transport within the material. In summary, the modes in Fig. 4.7 (a-d) can be classified as longitudinal acoustic (LA), transverse acoustic (TA), longitudinal optical (LO), and transverse optical (TO)

modes, respectively. The electrical charge carriers can interact (energetically favorable) with any modes available to experience scattering which leads to lower conductivity and electrical mobility. Performing temperature dependent electrical transport measurements on the fabricated HGFETs allows probing of the above crystal vibrations that affect the carrier transport in the graphene channel. The following subsections discuss the different temperature dependent carrier scattering and their impacts on channel resistivity (conductivity).

The net measured resistivity in the graphene channel can be written as[46]:

$$\rho = \rho_0 + \rho_{LA} + \rho_{RIP} \tag{4.6}$$

where ρ_0 is a gate voltage dependent term which accounts for temperature independent effects like short range carrier-carrier scattering, carrier-defect scattering, contacts, and long-range unscreened coulombic potentials etc. ρ_{LA} denotes the resistivity contribution from carrier-LA phonons, where the LA phonons are present in the graphene channel. The other temperature dependent resistivity contribution (ρ_{RIP}) arises from remote interfacial phonons (RIP). These RIPs are surface polar phonon modes present in hBN, which encapsulate the graphene channel. The details of LA scattering and RIP scattering are covered in following sections.

4.4.1 Longitudinal acoustic scattering

Longitudinal acoustic scattering occurs when an electron (Bloch state) with wave vector **k** interacts elastically with a LA phonon in the graphene channel with wave vector **q** and transitions into a Bloch state with wave vector **k+q**. Often scattering from longitudinal acoustic phonons is described by coupling to a single effective phonon mode where the characteristic scattering time (τ_{LA}) and resistivity (ρ_{LA}) are given by[37;46]:

$$\begin{aligned} \frac{1}{\tau_{LA}} &= \frac{1}{\hbar^3}\frac{D^2 k_B T}{4\rho_m v_f^2 v_{ph}^2} \\ \rho_{LA} &= \frac{\pi D^2 k_B T}{4e^2\hbar\rho_m v_f^2 v_{ph}^2} \end{aligned} \tag{4.7}$$

where D is the acoustic deformation potential, $\rho_m = 7.6 \times 10^{-8}$ g/cm^3 is graphene's mass density, $v_{ph} = 2 \times 10^4$ m/s is the velocity of sound or phonon propagation velocity in graphene, $v_f = 1 \times 10^6$ m/s is Fermi velocity of electrons, and $\hbar$ and k_B are reduced Planck's constant and Boltzmann's constant, respectively. The deformation potential (D) mentioned above refers to the change in energy of a band per unit strain. Due to lattice distortions from LA phonons, the graphene channel experiences strain that introduces a slowly varying potential in the graphene channel which scatters the mobile charge carriers. Hence, the electron-phonon interaction consisting LA phonons can be seen as electrons interacting with a potential generated from the LA phonons in the graphene channel.

Apart from LA modes, graphene channel also hosts phonons in TA, LO and TO modes. However, the scattering contribution from electron's coupling to TA mode is $\approxeq 10\times$ lower as compared to LA mode, hence TA scattering can be safely ignored while considering resistivity contributions with LA scattering dominating over TA scattering.[37] The optical modes on the other hand have very high energy, making coupling with charge carriers energetically unfavorable.[46]

4.4.2 Remote interfacial phonon scattering

The dielectric substrate used to support or encapsulate graphene, host surface polar phonon modes that couple with the charge carriers in the channel. These polar modes effectively produce fluctuating electric fields or potential profiles that scatter mobile charge carriers in the graphene channel. The characteristic frequency for a surface polar mode (ω_s) originating from a bulk transverse optical mode (ω_{TO}) is given by[38;87;88]:

$$\omega_s = \omega_{TO}\left(\frac{1+\epsilon_s}{1+\epsilon_\infty}\right)^{1/2} \tag{4.8}$$

where ϵ_s is the dielectric constant of the dielectric at surface phonon frequency($\epsilon(\omega) = \epsilon(\omega_s)$), and ϵ_∞ is dynamic dielectric constant at high frequencies. The Hamiltonian describing the coupling of electrons in graphene and the field induced by a surface mode of the dielectric is given by:

$$H_{e-ph} = \sum_{\vec{q}} M_{\vec{q}} \rho_{\vec{q}} (b^{\dagger}_{\vec{q}} + b_{-\vec{q}}) \tag{4.9}$$

where, $b^{\dagger}_{\vec{q}}$ and $b_{-\vec{q}}$ are creation and annihilation operators for surface phonons with momentum $\vec{q}$, and $\rho_{\vec{q}}$ is the charge distribution density in the momentum space. $M_{\vec{q}}$ in Eq. 4.9 is an interaction element which underlines the strength of interaction between the electrons and surface phonons and is defined by:

$$M_{\vec{q}} = \sqrt{g} \frac{e^{-qz}}{\sqrt{q}} \tag{4.10}$$

where g is a dimensionless coupling parameter and z is the distance between the substrate and the graphene layer which is typically ≈ 4 nm. The dimensionless parameter g introduced in Eqn. 4.10 plays an important role in the scattering as it determines the strength of scattering. The parameter g can be expanded as:

$$g = 2\pi\beta \frac{\hbar\omega_s}{\hbar v_F/a} \frac{e^2}{\hbar v_F} \tag{4.11}$$

where, a is the C-C bond distance $= 1.42$ $\mathring{A}$ and β is a proportionality factor that depends on the frequency dependent dielectric constant: $\beta = \frac{\epsilon_s - \epsilon_\infty}{(\epsilon_s+1)(\epsilon_\infty+1)}$. The other factor that affects the scattering of electrons is the number of surface phonons available that actually couple with the electrons. We denote this number as $n_B(T)$ which can be expanded by Bose-Einstein distribution to quantify the number of available phonons at a steady state temperature (T) and frequency (ω_s) as: $n_B(T) = \frac{1}{e^{\hbar\omega_s/k_B T}-1}$. Therefore, the net scattering of electrons which give rise to a temperature dependent resistivity contribution from surface polar modes (remote interfacial phonons) is given by:

$$\rho_{RIP} \propto g n_B(T) \tag{4.12}$$

which can be further expanded using the factors g and n_B, and can be written as:

$$\rho_{RIP} \propto \frac{\beta\omega_s}{e^{\frac{\hbar\omega_s}{k_BT}} - 1} \tag{4.13}$$

The complete expression for RIP contribution is given as:

$$\rho_{RIP} = BV_g^{-\alpha} \sum_{\omega_s i} \left(\frac{\beta_i\omega_{si}}{e^{\frac{\hbar\omega_{si}}{k_BT}} - 1}\right) \tag{4.14}$$

where the sum runs over all available surface modes and their corresponding coupling parameter β. The parameters B and α are fitting parameters where the value of $\alpha \approxeq 1$. A previous study with graphene on SiO_2 has shown the contribution for the remote modes in SiO_2 to have the functional form[38;46]:

$$\rho_{RIP} = BV_g^{-\alpha}\left(\frac{1}{e^{\frac{59meV}{k_BT}} - 1} + \frac{6.5}{e^{\frac{155meV}{k_BT}} - 1}\right) \tag{4.15}$$

where 59meV and 155 meV are characteristic surface modes in SiO_2 and the ratio of their corresponding $\beta_i\omega_{si}$ (numerators) is $1 : 6.5$, respectively. A separate theoretical study performed for hBN substrates show that the RIP contribution for graphene encapsulated within hBN[89]:

$$\rho_{RIP} \propto \frac{\beta_s\omega_s}{sinh[\frac{\hbar\omega_s}{k_BT}]} \tag{4.16}$$

where β_s and $\hbar\omega_s$ =101.6 meV are coupling parameter and surface phonon mode in hBN, respectively.[89;90]

4.4.3 Scattering in HGFET devices

By using equations 4.6,4.7, and 4.16, the temperature dependent resistivity in our HGFETs can be modeled as[74]:

$$\begin{aligned} \rho &= \rho_0 + \rho_{LA} + \rho_{RIP} \\ \rho &= \rho_0 + \frac{\pi D^2 k_B T}{4e^2 \hbar \rho_m v_f^2 v_{ph}^2} + \frac{B}{sinh[\frac{\hbar\omega_s}{k_B T}]} \end{aligned} \tag{4.17}$$

where $B \propto V_g^{-\alpha}\beta_s\omega_s$ is a gate voltage dependent fitting parameter.

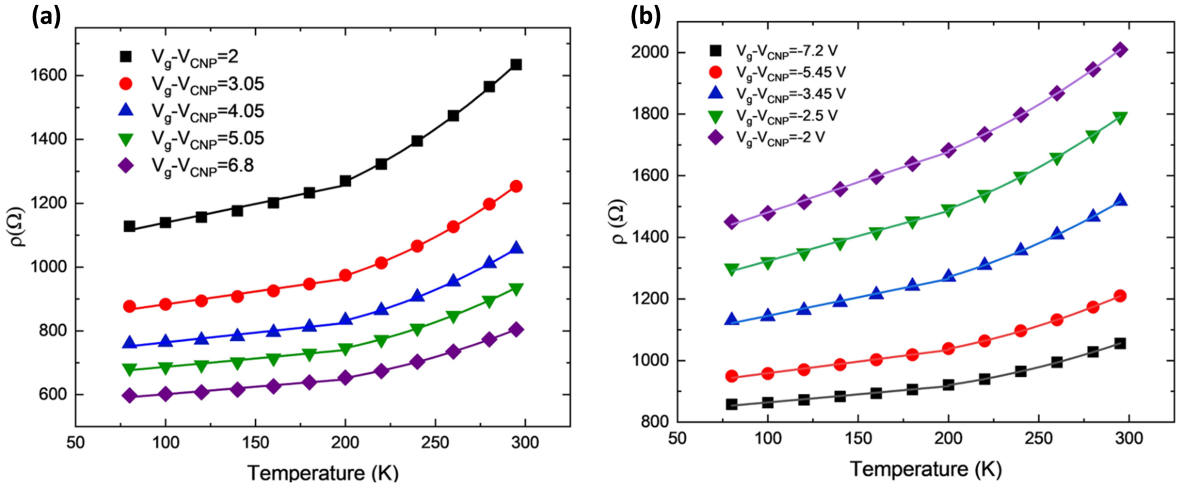


Figure 4.8: *Resistivity as a function of operating temperature at different overdrive voltages for (a) electron transport and hole transport (b). Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

Fig. 4.8 shows the channel resistivity of our HGFET as a function of operating temperature at different gate voltages for n-type transport(a) and p-type transport (b). At a fixed temperature, the standard gate voltage dependent behavior can be observed in the plots shown in Fig. 4.8, where the resistivity increases as gate voltage is modulated away from the charge residual region. The increase in resistivity at fixed gate voltages as function of temperature have been fitted according to Eqn. 4.17 and the fits plotted as solid lines in Fig. 4.8(a,b). These fits confirm the presence of LA (Eqn. 4.7) and RIP scattering (4.16) in

our HGFET systems.

Careful observation of all the temperature dependent resistivity curves shown in Fig. 4.8 reveal two different behaviors for our device. A linear dependence of resistivity to temperature can be observed below 200K, whereas a quasi-linear behavior in resistivity is observed above 200K. To explain the above observation, the resistivity contributions from LA scattering and RIP scattering alone respectively were obtained from the fits in Fig. 4.8 were analyzed. Fig. 4.9 shows the resistivity contribution from LA scattering (ρ_{LA}) and RIP scattering (rho_{RIP}) at a fixed gate voltage ($V_g - V_{CNP} = 3.55V$). One can observe that below 200K, ρ_{RIP} reduces sharply and vanishes below $\cong$ 150K. In this low temperature regime between 80K and 200K, LA scattering (ρ_{LA}) dominates over ρ_{RIP} giving rise to the linear dependence on temperature (see Eqn. 4.7). On the other hand, at operating temperatures $>$ 200 K, we can observe that ρ_{RIP} significantly dominates over ρ_{LA}. Due to the combined resistivity contribution from LA and RIP scattering at elevated temperatures, a quasi-linear resistivity behavior is observed at operating temperatures $>$ 200K.

The above result of RIP scattering dominating over LA scattering at higher temperatures provides an important insight on future graphene based heterostructure devices for wider use. It can be seen that at higher temperatures (device operating temperatures $\approx$ 350-400K) the contribution of RIP scattering will supersede LA scattering due to the exponential nature of RIP scattering as compared to linear rise in LA scattering case. The higher resistivity pose added hindrance towards creating low resistance and high mobility devices meant to operate at elevated temperatures.

4.5 Low frequency *1/f* noise away from the charge residual region

Next, low frequency *1/f* noise measurements were taken for the fabricated HGFET in a series of gate voltages. Fig. 4.10(a) shows the normalized current noise spectral density for the HGFET as a function of frequency over the operating temperatures for a specific gate

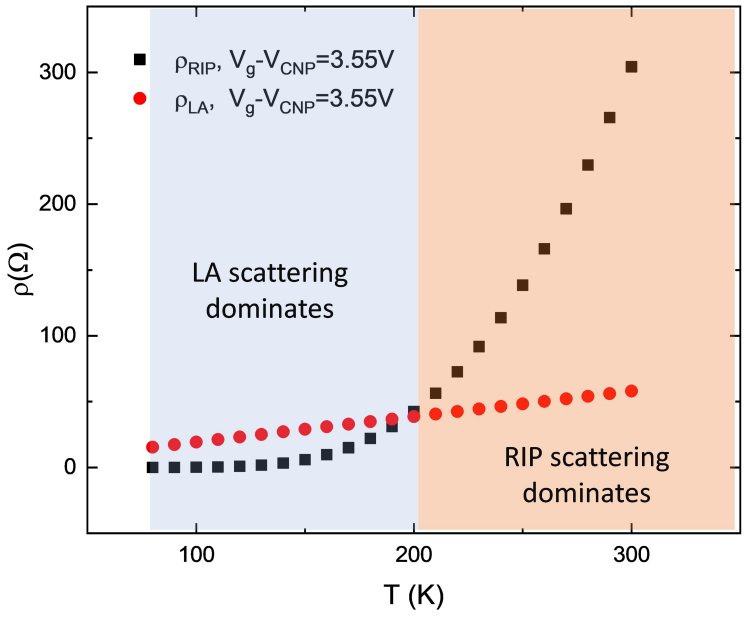


Figure 4.9: *Contribution of LA and RIP scattering as a function of temperature. Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

voltage of (V_g-V_{CNP}) of 6.8 V. The device exhibits *1/f* noise behavior referenced from the ideal *1/f* solid black line. Previous reports regarding low frequency noise in HGFETs have shown an order of magnitude reduction in noise due to the screening of charge impurities in SiO_2 and significantly lower trap states accessible to charge carriers in the graphene channel (see Fig. 1.17).[63;91] However, the relations between scattering and noise sources in high-performance 2D HGFETs are still not well studied. To understand the LFN and its microscopic origin, we use the temperature dependent resistivity data in the ON regime in section 4.4 and correlate the observed low frequency noise to electron-phonon (e-ph) scattering and the density of trap states in hBN.

In order to understand how the above scattering events lead to the measured noise in HGFETs, LFN measurements were performed by monitoring the normalized current noise spectral density from 2 Hz to 1.25 kHz (see Fig. 4.10(a)). Fig. 4.10 (b) shows the exponent factor γ from Eqn. 1.11 where the measured value of γ lies between 0.8 and 1.1 for most

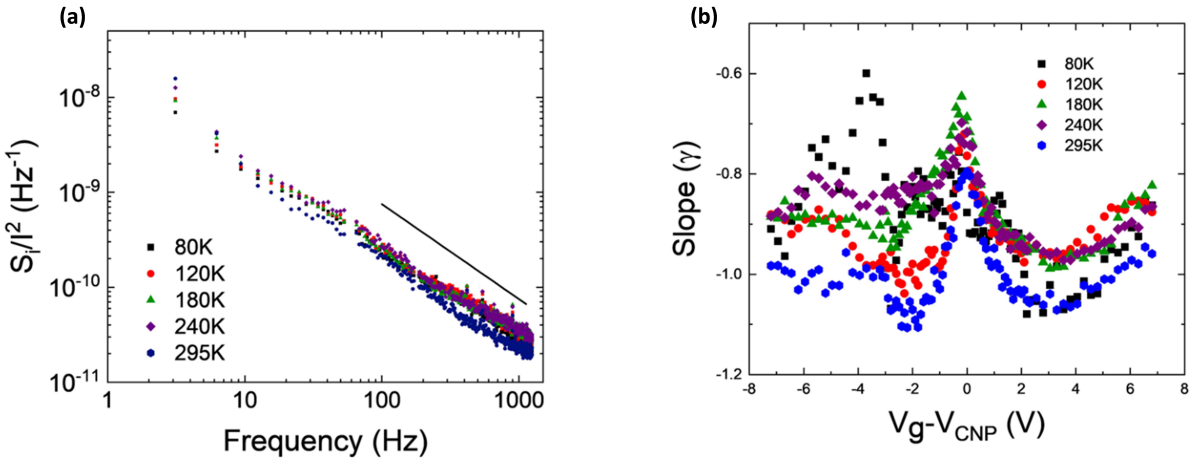


Figure 4.10: *Current normalized noise spectral density as a function of frequency at different operating temperatures (a). A reference 1/f line is also shown in (a). The exponent component (γ) plotted as a function of different overdrive voltages at different operating temperatures (b). Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

of the temperature values. Hooge's relation (see Eqn. 1.12) can be used for quantifying the noise in the HGFET as $S_I/I^2 = \alpha_H\ /(N \times f^{\gamma})$ when the device is operated in the regime where, $|V_g - V_{CNP}| \geq V_{CNR}$. The average noise amplitude over all the measured frequencies can then be written as:

$$A = \frac{\alpha_H}{N} = \frac{1}{N'} \sum_{i=1}^{N'} f_i^{\gamma} (S_I/I^2)_i \tag{4.18}$$

where both A (noise amplitude) and α_H (Hooge paramater) are dimensionless quantities that are characteristics of the electronic noise in the device. Fig. 4.11(a,b) shows the obtained α_H as a function of μ_{FE} at frequency $(f) = 100$ Hz at multiple operating temperatures. The values of α_H were obtained between 2.41×10^{-5} and 5.67×10^{-4} for holes and between 5×10^{-5} and 1.4×10^{-3} for electrons, respectively, which represent very small values of α_H in graphene devices for future practical applications. The power law dependence of Hooge parameter on the mobility can be visualized as a linear behavior in a log-log plot.

The extracted Hooge parameter can also be influenced by the density of trap states (DOTS) present in the surrounding hBN. Since our analysis is performed at $|V_g - V_{CNP}| >$

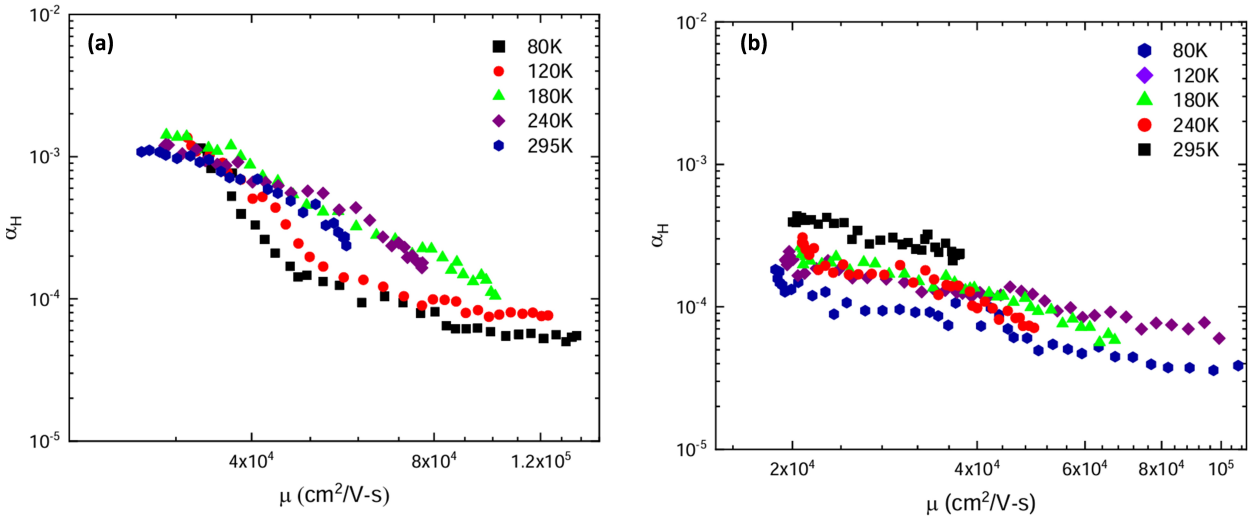


Figure 4.11: *Hooge parameter as a function of carrier mobility at different operating temperatures for electron transport (a) and hole transport (b). Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

V_{CNR}, where mobility and trap states are dependent on temperature, the Hooge parameter can be written as:

$$\alpha_H = f(\mu(V_g, T), D_{trap}(\epsilon, T)) \tag{4.19}$$

where $D_{trap}(\epsilon, T)$ is the distribution of trap states in energy (ϵ) and temperature (T).[92] The average noise amplitude then becomes:

$$A = \frac{1}{N} \times f(\mu(V_g, T), D_{trap}(\epsilon, T)) \tag{4.20}$$

This functional dependence of α_H on V_g and T is deeply connected to crystal lattice, interfaces between atomic layers, crystal defects as well as interface and trap states and thus makes the noise amplitude fundamentally complex to characterize. However, under certain conditions such as at high V_g where μ does not have a temperature dependence, α_H can be decoupled into temperature independent and temperature dependent terms. In a more general case such as ours, at the onset of the ON state of the device ($|V_g - V_{CNP}| \geq V_{CNR}$), the net

effective mobility can be written using the Matthiessen's rule as:

$$\mu_{eff} = \left[\frac{1}{\mu_{SRS}} + \frac{1}{\mu_{LRS}} + \frac{1}{\mu_{LA}} + \frac{1}{\mu_{RIP}} \right]^{-1} \tag{4.21}$$

where $\mu_{SRS}, \mu_{LRS}, \mu_{LA}$ and μ_{RIP} are individual mobility contributions for short range scattering, long range scattering, longitudinal acoustic phonon modes and remote interfacial phonon modes in the channel, respectively. Therefore the net Noise amplitude can then be written as:

$$A = \frac{1}{N} \times f(\mu_{eff}(V_g, T), D_{trap}(\epsilon, T)) \tag{4.22}$$

The shape of noise amplitude (A) vs $V_g - V_{CNP}$ depends on the interplay between above four mentioned scattering mechanisms (Eqn. 4.21 and section 4.4). Fig. 4.12(a-e) shows the measured values of normalized current noise spectrum as functions of $V_g - V_{CNP}$ for selected operating temperatures. Our edge contacted device presented here demonstrates lower level of noise due to lower contact resistance as compared to a surface contacted device, leading to a higher transfer length and a uniform current injection from 1D contacts to the channel without current crowding.[93;94]

The carriers experience resistances from three types of scattering i.e., short- and long-range scattering (for convenience, we group these two types into one, called residual scattering), longitudinal acoustic (LA) phonon scattering, and remote interfacial phonon (RIP) scattering where we consider each scattering mechanism to be a different source of noise in the graphene channel. For simplicity, we consider different temperature ranges and relative strengths of these scatterers therein to decouple the contribution of each scattering event towards the net noise amplitude. From fig. 4.9, it was established that at operating temperatures below 200K only residual scattering and LA scattering contribute towards measured resistance, whereas above 200K, residual, LA, and RIP scattering contribute towards the net resistivity with LA contribution being much smaller as compared to the RIP contribution. Note that the residual scattering is independent of temperature and is responsible for the highest noise resistance among the three at any given temperature. A two-scatterer problem

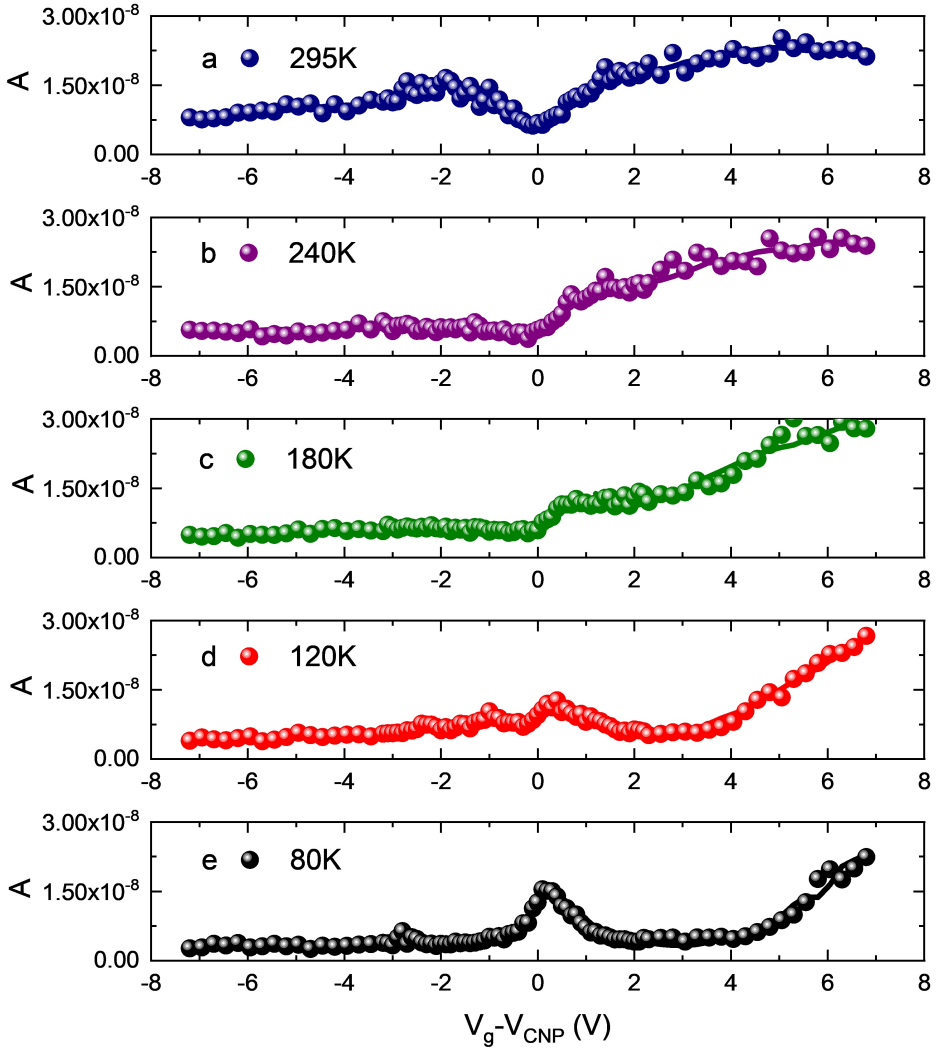


Figure 4.12: *Noise amplitude (A) as a function of overdrive voltages (V_g-V_{CNP}) at different operating temperatures. Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

(both in T $<$ 200 K and in T $>$ 200 K) with two separate noise sources with resistances R_1 and R_2 provides the total noise amplitude in the HGFET as follows:

$$A = \frac{S_I \times f}{I^2} = \frac{S_{R_{Tot}} \times f}{R_{Tot}} = \frac{(S_{R_1} + S_{R_2}) \times f}{(R_1 + R_2)^2} \tag{4.23}$$

where $S_{R_{Tot}}$ is the total noise spectral density, S_{R_1} and S_{R_2} are the respective noise spec-

tral density from two scatterers, R_{Tot} is the total resistance and R_1 and R_2 are individual resistances from the two scatterers.

By using the two scatterer problem (eqn. 4.23 and eqn. 4.6), the rate of change of noise amplitude A with the temperature T in the temperature regime between 80 K and 200 K, can be approximated by:[74]

$$\frac{dA}{dT} = \frac{f}{\rho_\circ^2}\frac{dS_{\rho_{LA}}}{dT} \tag{4.24}$$

where, $f = 100\ Hz$, $\rho_\circ$ is the residual resistance at low temperature (T independent) and $S_{\rho_{LA}}$ is the noise spectral density contribution from longitudinal acoustic phonon contributions only. Similarly, in the temperature regime between 200 K and 295 K, the rate of change of noise amplitude is given by:[74]

$$\frac{dA}{dT} = \frac{f}{\rho_\circ^2 T^2}\frac{dS_{\rho_{RIP}}}{dT} \tag{4.25}$$

By using eqn. 4.24 and 4.25, the behavior of noise amplitude observed in fig. 4.12 can be explained. As T decreases from 295 K to 200 K for electrons (see Fig. 4.12), the factor $(\frac{f}{\rho_\circ^2 T^2})$ increases rapidly (as T^2 decreases rapidly). On the other hand, the factor $\frac{dS_{\rho_{RIP}}}{dT}$ decreases rapidly due to thermal freezing of RIP phonons. Therefore, the noise amplitude A, remains fairly unchanged largely from 295 K to 200 K for electrons. A decrease in the magnitude of A in the same temperature range for holes, on the other hand, can be attributed to their higher residual resistivity $(\rho_\circ)$ compared to the electrons leading to a smaller increasing pre-factor $(\frac{f}{\rho_\circ^2 T^2})$. In temperature regime between 200 K and 80 K, where LA scattering dominates over RIP scattering, as the temperature decreases $(\frac{f}{\rho_\circ^2})$ remains constant and $(\frac{dS_{\rho_{LA}}}{dT})$ decreases (eqn. 4.24), leading to a decrease in noise amplitude, A. An absence of notable decrease in A between 200 K and 80 K might be due to higher $\rho_\circ$ value in the hole branch. The temperature dependent nature of these competing scattering mechanisms confirm the presence of higher level of noise at elevated temperatures and the gradual decrease in noise amplitude with the reduction in operating temperatures.

The thermally activated trap states at the channel-hBN interface and their collective activation energies were calculated by considering the Hooge parameter (or the noise amplitude) at large gate voltages where the mobility and the DOTS dependence on Hooge parameter

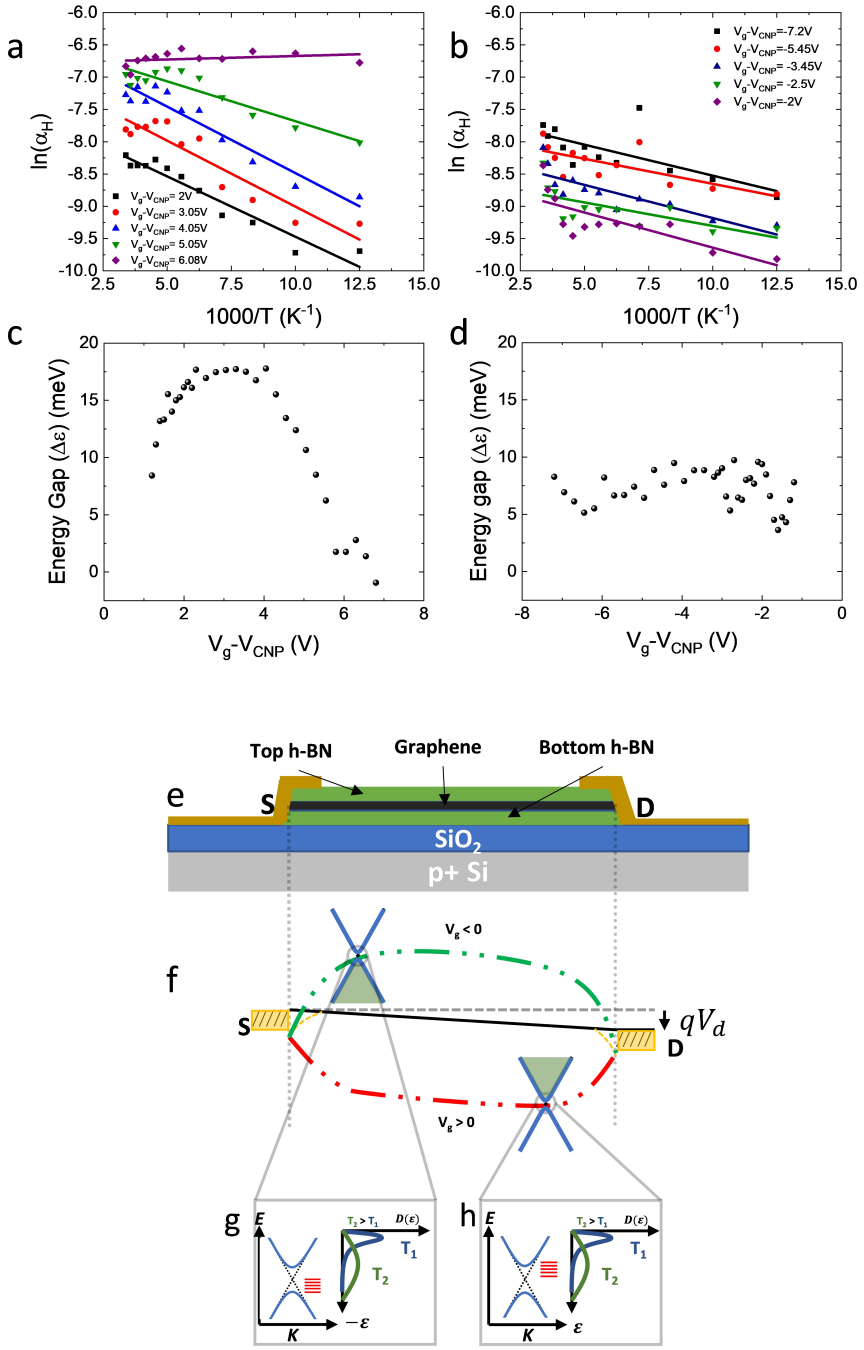


Figure 4.13: *(a,b) Arrhenius plots for Hooge parameter at different operating overdrive voltages. (c,d) Obtained energy levels of DOTS for electron and hole transport (e) Schematic diagram of the fabricated device. (f) Electrical band diagram showing the operation of the device along with the distribution of DOTS at at two different temperatures. Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

could be decoupled:

$$\alpha_H = f\big(\mu(V_g)\big) \times D_{trap}(\epsilon, T) \tag{4.26}$$

If $\Delta\epsilon$ is the collective activation energies of distribution of trap states at the interface between graphene and the encapsulating hBN, one can rewrite the Hooge parameter in terms of temperature dependence at a fixed V_g using the thermal emission model as follows[95]:

$$\alpha_H = Ae^{-\Delta\epsilon/k_BT} \tag{4.27}$$

Fig. 4.13(a, b) show Arrhenius plots of $ln(\alpha_H)$ vs. $1/T$ for various overdrive voltages for electrons and holes, respectively. The different slopes in the Arrhenius plots obtained at multiple gate voltages correspond to activation energies of trap states ($\Delta\epsilon$). Fig. 4.13(c,d) shows the extracted activation energies vs. $(V_g - V_{CNP})$ for electrons and holes, respectively showing the presence of traps within 20 meV below the conduction band edge for electrons and within 10 meV above the valence band edge for holes. The obtained values are reasonable, given a recent prediction of band gap opening of $\approx 120\ meV$ between the valence and conduction bands in hBN/graphene/hBN heterostructures.[96] The obtained trap levels in our devices show slightly higher activation energies as compared to a few studies performed on traps in SiO_2.[97;98] The above studies show the trap levels in SiO_2 lie between the energy levels of 2-20 meV. Moreover, the presence of charge impurities and dangling bonds on the surface of SiO_2 creates larger density of trap sites as compared to hBN's van der waals surface. These phenomena lead to a lower level of electrical noise in graphene devices encapsulated in hBN as compared to graphene devices fabricated on SiO_2. Based on the above analysis, a schematic band diagram of the HGFET working device with S/D edge–contacts is shown on in Fig. 4.13 (e and f). Fig. 4.13 (g and h) shows the schematic band diagram, distribution of shallow trap states within the energy gap, and the density of trap states with their temperature dependence near the valence band edge and conduction band edge, respectively.

4.6 Electrical transport within the charge residual region

The mechanisms that govern the electrical transport and noise in the graphene differ starkly from the topics discussed in section 4.4 and 4.5 when operated in the vicinity of the charge neutrality point (CNP) or the Dirac point. In order to understand these mechanisms in the two hBN/graphene/hBN HGFETs, electrical transport and LFN measurements were performed. Owing to the similarity of the two devices, one expects their qualitative LFN behavior to resemble each other. However, following our previously modeled LFN analysis in transistor's ON state (see section 4.5), the measured current normalized spectral density, behave differently at CNP as shown in Fig. 4.14.[74;76] Furthermore Device 1 also shows an inverse trend in the measured noise spectral density at 80 K as compared to 295 K. This variation in LFN is widely reported in the literature, however, a unified understanding of the mechanism of the LFN at the Dirac point (characterized by a charge residual region) is yet to be made.[66;67;70;99] The goal of this chapter is to establish such an LFN theory to demonstrate the noise resemblance of the two analogous devices shown here.

Fig. 4.15 shows the transport measurement results from device 2 (the measurement results with similar trends from device 1 have been shown earlier (see section 4.5) and will further be discussed in this chapter as needed). Fig. 4.15(a) shows the measured resistivity (ρ) as a function of applied gate voltage with an offset from the charge neutrality point (V_g-V_{CNP}) for a 2D HGFET. The highest resistivity appears at the Dirac point, which also corresponds to the lowest conductivity. The resistivity then gradually decreases as the gate voltage increases to positive and negative values, confirming electron and hole type of conduction, respectively.

Fig. 4.15(b) shows the extracted mobility (as per Eqn. 4.5) for device 2, plotted as a function of V_g-V_{CNP}. Mobility values of $\approx$ 70,000 cm^2/(Vs) were obtained at 295 K and $\approx$ 160,000 cm^2/(Vs) at 80 K. The mobility peaks for both electrons and holes are clearly observed at respective sides of the Dirac point with a sharp decrease in their values as the

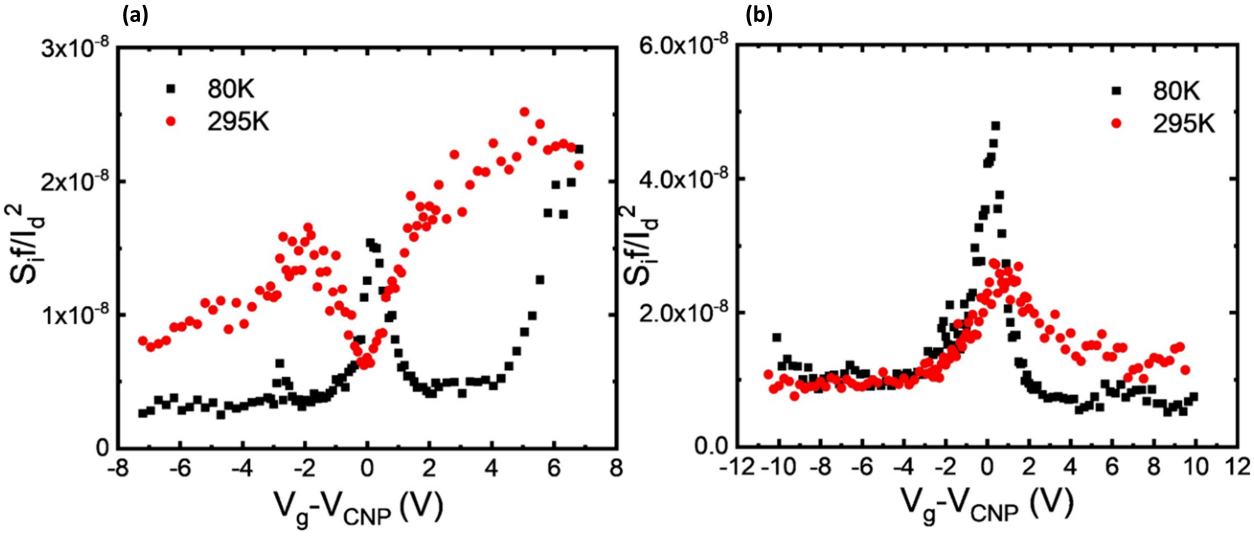


Figure 4.14: *Current normalized current noise spectral density for SLG device 1 and SLG device 2 at 295K and 80K. Reprinted (adapted) with permission from Behera et al., Charge-inhomogeneity-mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. ACS Applied Nano Materials, 7(11), 12366–12375, 2024. Copyright 2024 American Chemical Society*[76].

absolute value of the overdrive voltage increases. The orange and black dashed lines in Fig 4.15 (b) are the reference overdrive voltages for mobility maxima obtained from the device at 295 and 80 K, respectively. The corresponding peak voltages for the device were 0.9 and 1.4 V at 80 and 295 K, respectively. The regime for defining the charge residual region can be quantitatively defined as the V_g - V_{CNP} values bound by the dashed lines for a given temperature on either side of the Dirac point. It is important to note here that the width of the charge residual region is a function of temperature, where the width increases as temperature increases.

Unlike a standard semiconducting channel where the carrier concentration is a direct function of overdrive gate voltage, in graphene's charge residual region, the average channel carrier density is a constant value irrespective of gate bias, bound by the charge density (n^*) induced by the voltage at mobility maxima. The value of n^* increases as the width of the residual region increases with temperature. It is in this residual region that the spatial charge profile of the graphene channel becomes inhomogeneous with puddles of electrons and holes, and the channel conductivity is governed by percolative transport.[100] Percolative transport is

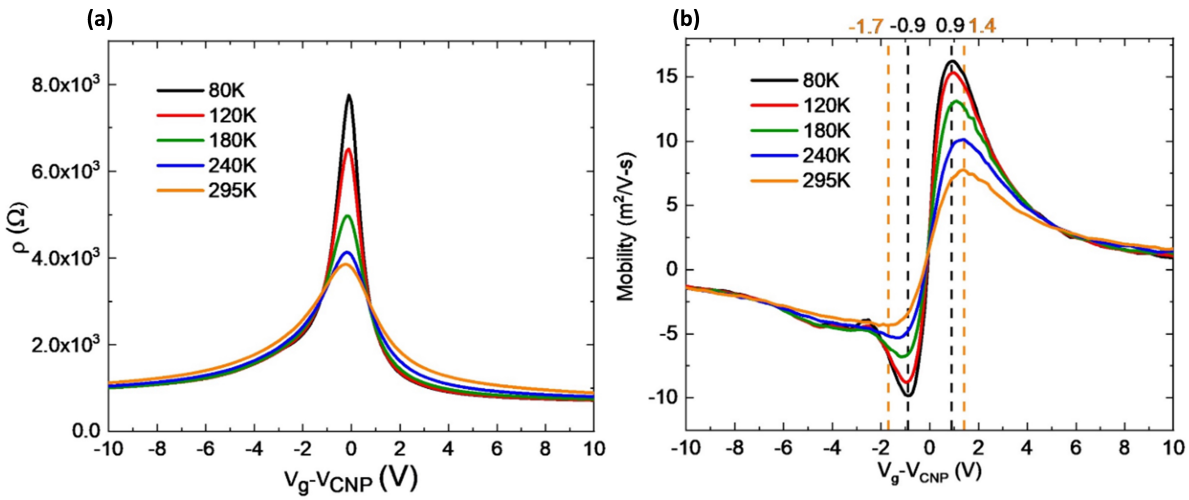


Figure 4.15: *Resistivity as a function of overdrive voltages at different operating temperature for SLG 2 device (a). Extracted mobility as a function of gate overdrive voltage (V_g-V_{CNP}) at different operating temperatures (b). Reprinted (adapted) with permission from Behera et al., Charge-inhomogeneity-mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. ACS Applied Nano Materials, 7(11), 12366–12375, 2024. Copyright 2024 American Chemical Society*[76].

a type of transport where the charge carriers traverse the length of the electronic channel by forming a continuous conductive path around the non-conducting puddles. The origin of the electron-hole puddles in the graphene channel has been attributed to the Coulomb potentials that arise from the charge impurities in the underlying substrate and to spatial corrugation of the channel from ripples and bending.[39;101] Although hBN provides an atomically flat surface for graphene to prevent folding, it has been shown that electron-hole puddles still exist in the graphene channel when hBN is used as a dielectric substrate due to charge impurities in hBN, although significantly lower as compared to thermally grown SiO_2[102;103]

To confirm the existence of electron-hole puddles in our channel, the extracted conductivity ($\sigma = 1/\rho$) is plotted as a function of operating temperatures. Fig. 4.16(a) shows the conductivity of SLG device 2 at different gate voltages within the charge residual region. Fig. 4.16(b), on the other hand, shows the device conductivity at a few gate voltages away from the charge residual region. One can clearly observe the opposite conductivity trends with the operating temperature in the residual and the saturated region. This discrepancy in the conductivity within the charge residual region as compared to the saturated region,

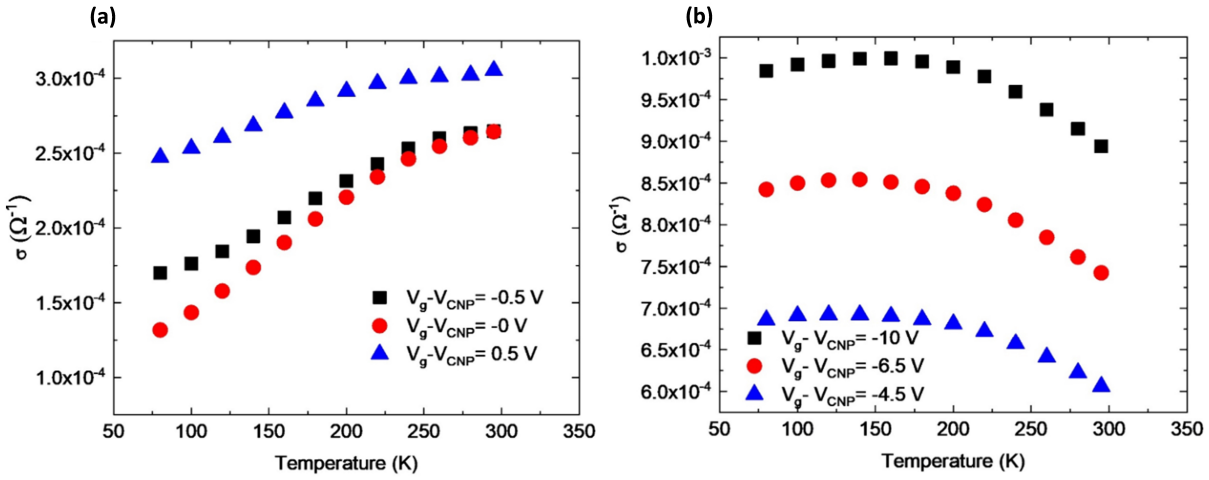


Figure 4.16: *Extracted conductivity vs. operating temperature near (a) and away from Dirac point (b). Reprinted (adapted) with permission from Behera et al., Charge-inhomogeneity-mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. ACS Applied Nano Materials, 7(11), 12366–12375, 2024. Copyright 2024 American Chemical Society*[76].

has been attributed to the presence of electron-hole puddles,[39;100] where the conductivity is described as:

$$\begin{aligned} \sigma(V_g) &\approxeq C\frac{e^2}{h}\frac{n(V_g)}{n_i} \quad for \quad n > n^* \\ \sigma(T) &\approxeq C\frac{e^2}{h}\frac{n^*(T)}{n_i} \quad for \quad n < n^* \end{aligned} \tag{4.28}$$

where e is the fundamental electronic charge, h is Planck's constant, n is the carrier density related to gate voltage as $n = C_{ox}V_g/e$, n^* is the residual carrier density (root-mean-square charge carrier density) in the percolation region considering the electron-hole puddle region induced by the substrate charge impurities of density n_i , C is a dimensionless parameter describing the strength of scattering, and T is the operating temperature.

The increase in conductivity with temperature for a fixed gate voltage (Fig. 4.16(a)) in the residual region can be explained with the increasing value of n^* as the temperature rises, confirming the existence of puddles in the 2D-HGFET. The extracted values of n^* as a function of temperature in our HGFETs are shown in Fig. 4.17. The increasing value of

n^* at elevated temperatures means that at higher temperatures carriers within puddles gain enough thermal energy to escape into the conducting percolation region to participate in the electrical conduction. Fig. 4.18(a) shows the schematic diagram of long-range Coulombic potential induced in the channel by the charge impurities (n_i) present in the substrate. This Coulombic potential gives rise to e-h puddles and a percolation region in the graphene channel, a qualitative schematic of which is provided in Fig. 4.18(b).

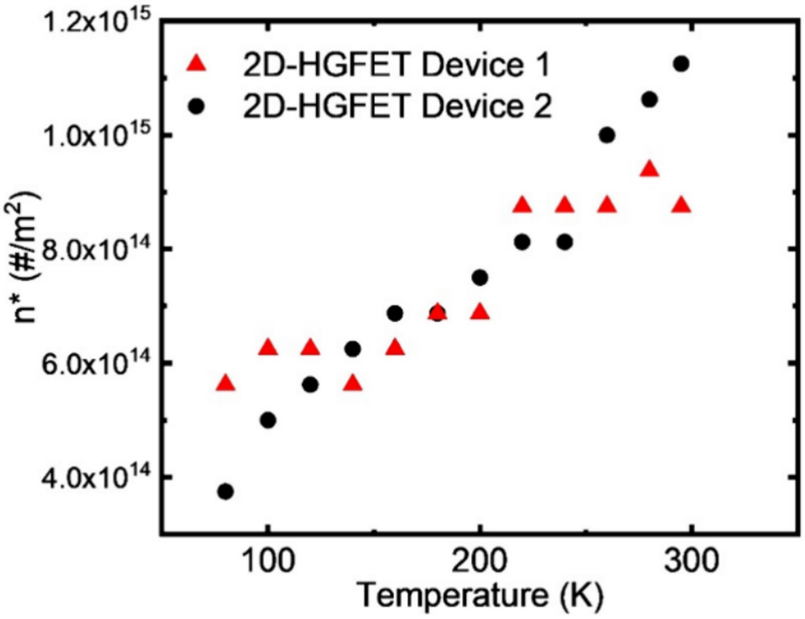


Figure 4.17: *Extracted n* value as a function of temperature for SLG device 1 and SLG device 2. Reprinted (adapted) with permission from Behera et al., Charge-inhomogeneity-mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. ACS Applied Nano Materials, 7(11), 12366–12375, 2024. Copyright 2024 American Chemical Society*[76].

To understand the role of e-h puddles on electrical noise in HGFETs with 1-D contacts, specifically within the charge residual region of the two devices (devices 1 and 2, whose normalized noise current densities based on purely electronic diffusive transport look widely different, as shown in Fig. 4.14(a,b)), we measured LFN by recording the normalized power spectral density in the devices in a frequency range from 2 Hz to 1.25 kHz. The average channel noise amplitude (A) normalized by area over all measured frequencies can be written as shown in Eqn. 4.18. In this section, we only analyze the noise results in the charge residual

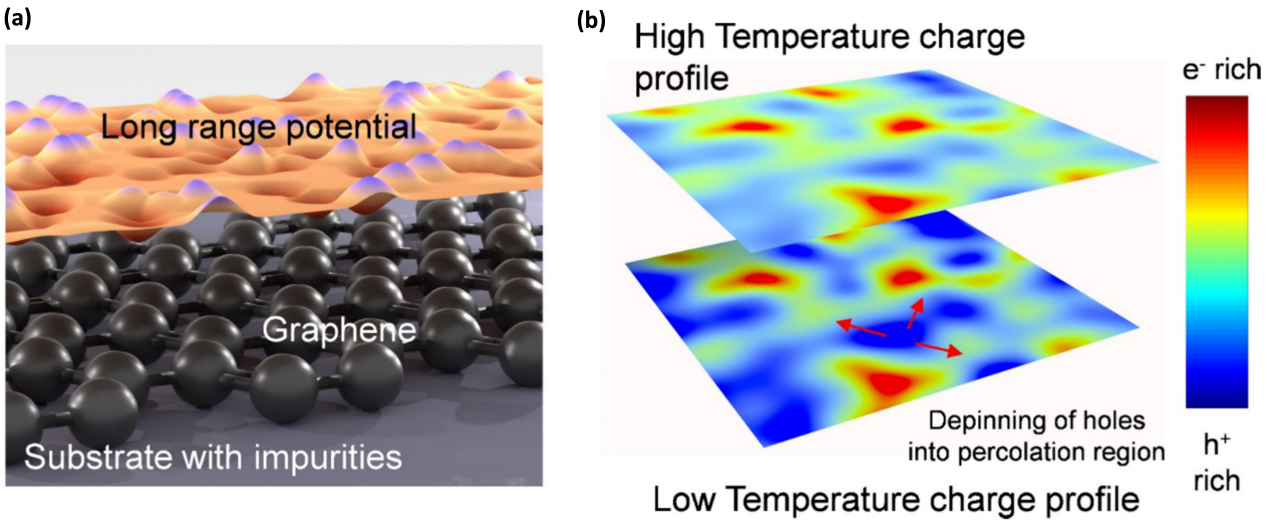


Figure 4.18: *Solid model showing the graphene sheet on a substrate with impurities that give rise to long range potentials (a). Model showing the e-h puddle profile at low and high operating temperatures (b). Reprinted (adapted) with permission from Behera et al., Charge-inhomogeneity-mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. ACS Applied Nano Materials, 7(11), 12366–12375, 2024. Copyright 2024 American Chemical Society*[76].

region in both of our devices.

Historically, e-h puddles on substrates have been classified into two types, namely Type-I and Type-II, which are attributed to a small size with a relatively high carrier concentration and a large size with a relatively lower carrier concentration, respectively.[40] While previous studies on noise arising from e-h puddles on GFETs fabricated on SiO_2 dielectrics used the mobility fluctuation model to explain the V shape trend near the Dirac point and attributed it to the gradual increase and decrease in the size of Type-II puddles (with applied gate bias),[62] however, Hooge's mobility fluctuation model is only valid for homogeneous electrical channels with a single type of charge carriers with a constant carrier concentration in the channel.[60;61;104] On the contrary in our case, the spatial charge profile in the graphene channel is inhomogeneous. Therefore, using McWhorter's number fluctuation model within the charge neutrality region is more appropriate.[105]

Since in a MOS device, the change in gate oxide's charge density is equivalent to flat band voltage fluctuations, by using McWhorter's carrier number fluctuation model (encompassing,

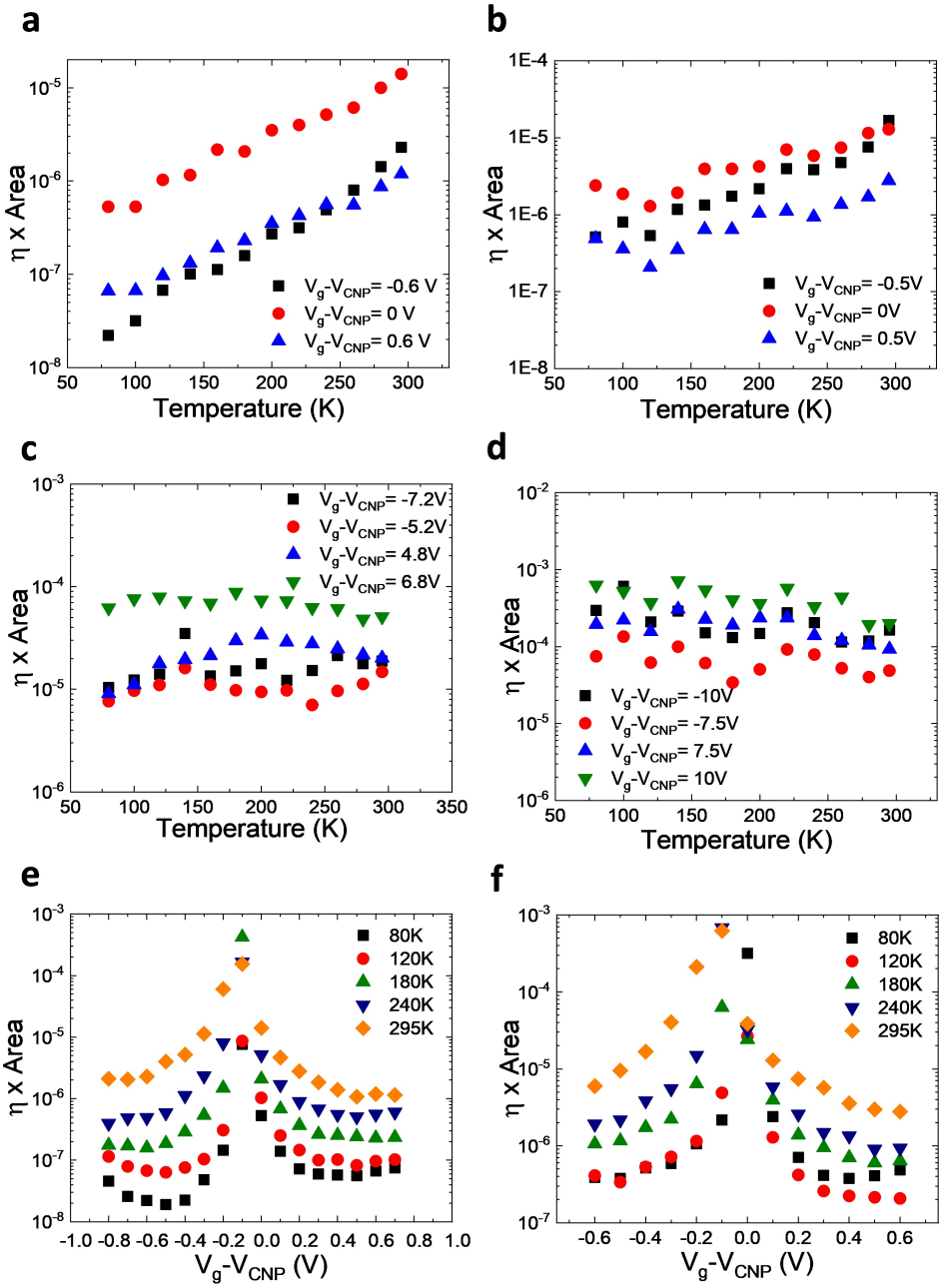


Figure 4.19: *(a,b) Area normalized η within the charge residual region for SLG 1 and SLG-2 device, respectively. (c,d) Area normalized η away from charge residual region for SLG-1 and SL-2 devices, respectively. (e,f) Area normalized η as a function of overdrive voltage within the charge residual region operated at different temperatures for SLG-1 and SLG-2 device. Reprinted (adapted) with permission from Behera et al., Charge-inhomogeneity-mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. ACS Applied Nano Materials, 7(11), 12366–12375, 2024. Copyright 2024 American Chemical Society*[76].

in our case, the dynamic charge trapping and detrapping from hBN surface to the percolative network channel via the e-h puddles), the measured current noise spectrum in our 2D-HGFETs can be described as[106]:

$$\frac{S_I(f)}{I_d^2} = \frac{g_m^2}{I_d^2} S_{V_{fb}} \tag{4.29}$$

where $S_{V_{fb}}$ is the flat band voltage spectral density associated with charge fluctuations at the interface between the channel and the dielectric. $S_{V_{fb}}$ has been shown to be equal to the equivalent input gate voltage spectral density S_{V_g}, where $S_{V_{fb}}$ is given as[69;106;107]:

$$S_{V_{fb}} = \frac{6.2e^2 k_B T}{AfC_{ox}^2 k} D_{it} \tag{4.30}$$

where k_B, T, A, k, and D_{it} are Boltzmann's constant, absolute temperature, channel area, inverse of decay scale in trap states $\approx 10^9$ m^{-1}, and trap density of hBN, respectively. To better elucidate the dynamic trapping of charge carriers from the charge inhomogeneous graphene channel, we define a parameter η from our measured current noise spectrum, defined as:

$$\eta = \frac{S_I(f)}{I_d^2} \times \frac{I_d^2}{g_m^2} \times f \tag{4.31}$$

where f is the selected frequency for analysis, which was set to 100 Hz. The physical significance of η could be understood as the rate of trapping and detrapping of charge carriers between the percolation region in the channel and the interface trap states in the dielectrics. This factor η quantifies our net device noise that will be further investigated in the rest of the chapter.

Fig. 4.19 (a,b) shows the behavior of η normalized by device area as a function of temperature for different overdrive voltages in the charge residual region for the two devices. On the other hand, Fig. 4.19 (c,d) shows the normalized η as a function of temperature for the same devices at overdrive voltages away from the charge residual region. The temperature dependence of η in the charge residual region corresponds to the trapping and detrapping of carriers in the percolation region. The temperature independence of the flat band fluctuation away from the charge residual region, on the other hand, indicates that the noise primarily

arises from dynamic scattering mechanisms via mobility fluctuations.[74]

Upon fitting the normalized η to eqn. 4.30 the trap densities D_{it} at CNP for the two devices were obtained to be 1.54×10^{16} and 1.91×10^{16} eV^{-1} cm^{-3} , respectively, which are in good agreement with a previous study.[69] Fig. 4.19(e,f) shows the normalized η as a function of applied gate voltage in the charge residual region for the two devices at various temperatures. A decreasing normalized η at both sides of the CNP at constant temperature is observed at different gate voltages within the charge residual region, indicating the progressive inaccessibility of relatively deeper trap states with increasing gate bias. On the other hand, the increase in the overall noise (η) with increase in operating temperatures (either in Fig. 4.19(e,f) or in Fig. 4.19(a,b)) is due to the thermally activated trapping and detrapping mechanism of charge carriers from or to the percolation region. Furthermore, we can also relate the noise behavior in the temperature to n^*. Since from Fig. 4.17 we obtained that n^* increases with temperature, we can safely conclude that the noise arising from the trapping and detrapping mechanism in the percolation region increases with n^* and vice versa. This means at higher temperatures, carriers in puddles with enough thermal energy escape into the conducting percolation region (Type-II), thereby increasing the number of available carriers to undergo trapping and detrapping and leading to higher measured electrical noise. This observed phenomenon has been termed as pinning and depinning of e-h puddles (see Fig. 4.18(b)). Thus, we conclude that lower flat band fluctuation noise at lower temperatures can be attributed to pinned puddles and higher noise at higher temperatures can be attributed to unpinned puddles.

Finally, the discrepancies in the noise spectral density in the charge residual region (between similar FET devices) as shown in Fig. 4.14 can be interpreted consistently as shown in Fig. 4.19(e,f) with a noise model based on flat band fluctuations (McWorter charge fluctuation model) involving e-h puddles and percolation transport in high performance 2D HGFETs. In order to justify the consistency between Fig. 4.14 and Fig. 4.19, we discuss a correlated noise model as follows. The normalized current spectral density according to the charge carrier trapping model with correlated mobility fluctuations (number and mobility

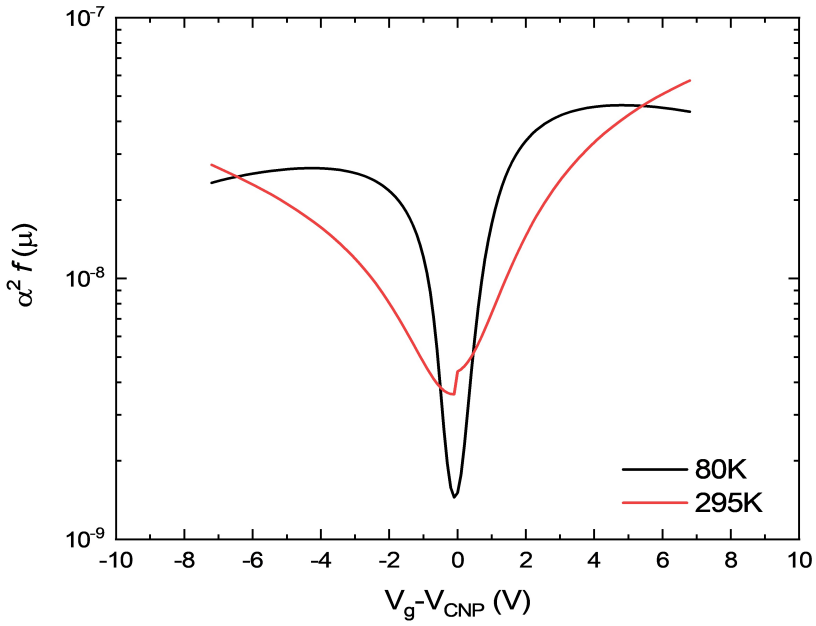


Figure 4.20: *Behavior of $\alpha^2 f(\mu)$ vs gate overdrive voltage (V_g-V_{CNP}) at 80K and 295K. Reprinted (adapted) with permission from Behera et al., Charge-inhomogeneity-mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. ACS Applied Nano Materials, 7(11), 12366–12375, 2024. Copyright 2024 American Chemical Society*[76].

fluctuations) studied bt Ghibaudo et al. is given by:[106]

$$\frac{S_I}{I_d^2} = \left(1 \pm \alpha\mu(r) C_{ox} \frac{I_d}{g_m}\right)^2 \frac{g_m^2}{I_d^2} S_{V_{fb}} \tag{4.32}$$

where α is a correlation term, when finite, suggests a significant effect of mobility fluctuations on the measured current spectral density. On the other hand, when $\alpha = 0$, there is no mobility fluctuation on the measured current spectral density and in this case, the above equation can be simplified as:

$$\frac{S_I}{I_d^2} = \frac{g_m^2}{I_d^2} S_{V_{fb}} + \alpha^2 f(\mu) S_{V_{fb}} \tag{4.33}$$

Now one can see when $\alpha = 0$, eqn. 4.33 essentially becomes eqn. 4.29; that is, a true McWhorter's number fluctuation model dictates the measured noise (number fluctuations only). However, when $\alpha \neq 0$, which is typically on the order of 10^4, there exist correlated

mobility fluctuations (number and mobility fluctuations). The plot for $\alpha^2 f(\mu)$ for $\alpha = 10^4$ s/C is shown in fig. 4.20 in similar V_g - V_{CNP} values which exhibits a "V" shape at both 80 and 295 K. From the plot, one can expect a "V" shape in the measured noise spectra when $\alpha \neq 0$: i.e., when there is contribution from mobility fluctuations. On the other hand, when $\alpha = 0$, the origin of noise can be explained by flat band fluctuations only as explained in detail in Fig. 4.19 (e,f) which leads to "Λ" shape.

Therefore the observed difference in the noise spectral density (V and Λ shape) shown in Fig. 4.14 can be understood from the competing contributions from number (Λ shape) and mobility (V shape) fluctuations in SLG device 1. At 295K, the carriers within the percolation region which participate in electrical conduction possess high thermal energy. This higher energy makes deeper level charge traps accessible resulting in higher degree of mobility fluctuations ($\alpha \neq 0$), thereby showing the characteristic "V" shape in noise power spectral density. On the other hand, at 80 K, the deep level trap states are not accessible by the charge carriers in the channel due to less thermal activation and thereby do not create a significant effect in mobility fluctuations ($\alpha = 0$). This gives the characteristic "Λ" shape to the measured current power spectral density. SLG device 2, shows a "Λ" shape at both low and high temperatures, suggesting significantly less trapping and detrapping of carriers from the deep trap levels with reduced or no mobility fluctuation contribution to measured noise spectra. In summary, the difference observed in different behaviors can be explained by relative contributions between the number fluctuation model and a hybrid number-mobility fluctuation model (dictated by whether $\alpha = 0$ or $\alpha \neq 0$, respectively). The effect of the number fluctuation model only leads to a "Λ" shape, as shown in Fig. 4.14(b), whereas a hybrid contribution shows a "V" shape as shown in Fig. 4.14(a).

Chapter 5

Graphene Field Effect Transistors Encapsulated in Isotopically pure Hexagonal Boron Nitride

In Chapter 4, we delved into the effects of various scattering mechanisms on charge carrier transport in graphene FETs and their impact on low-frequency noise measurements. Notably, from Fig. 4.9, remote interfacial phonon (RIP) scattering has $\approxeq 6\times$ greater influence compared to longitudinal acoustic (LA) scattering in the channel when a HGFET is operated at 300K. This resistivity contribution from RIP forms the largest temperature dependent resistivity contribution at room and higher operating temperatures. Furthermore, a comparison of RIP scattering in HGFETs fabricated with SiO_2 and hBN substrates (as shown in Fig. 5.1(a)) shows significantly lower RIP scattering in graphene FETs fabricated on hBN substrates as compared to SiO_2. This highlights hBN's superior nature as a substrate for 2D field-effect transistors as it not only shields the charge impurities from SiO_2 but also exhibits significantly lower remote phonon coupling at elevated temperatures.

RIP scattering originates from surface polar phonons present in the encapsulating hBN or the substrate for the graphene channel (see section 4.4.2). Since RIP scattering is the major contributor towards electrical resistivity at elevated temperatures, achieving low resistance

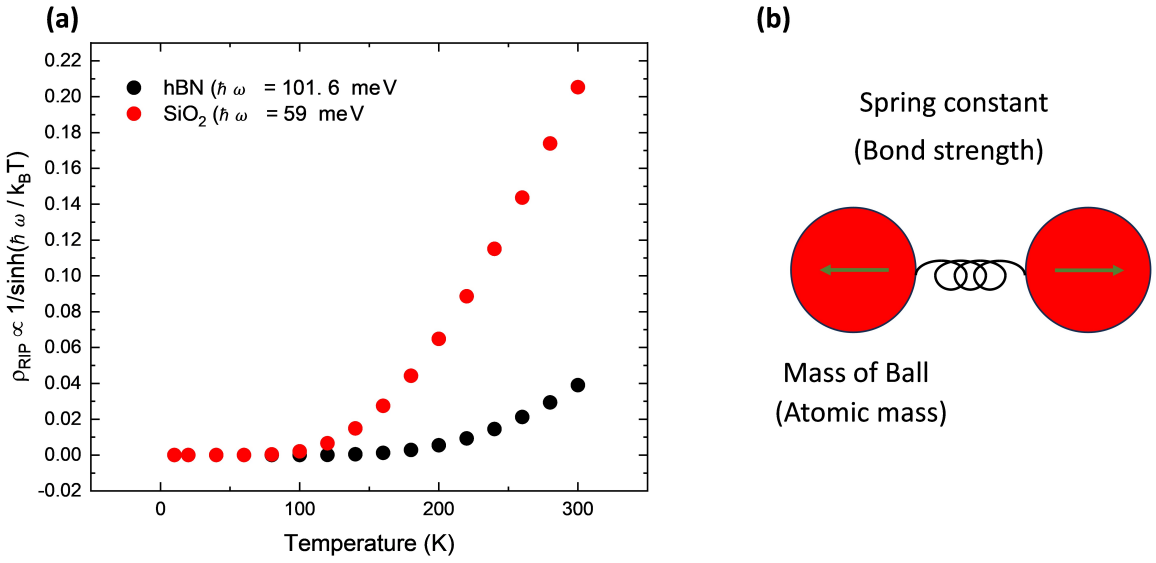


Figure 5.1: *(a)Comparison of RIP scattering at the interface of graphene and hBN vs. SiO_2. (b) Spring-ball model for a diatomic molecule. The green arrows illustrate the direction of motion of atoms (LO mode). Reprinted (adapted) with permission from Behera et al., High-performance and ultralow-noise two dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9), 4126–4134, September 2021. Copyright 2021 American Chemical Society*[74].

and high mobility devices at typical device operating temperatures (300K-400K) necessitates engineering the RIP scattering process. For HGFETs fabricated on hBN substrates and encapsulating the graphene channel by hBN, RIP scattering experienced by the charge carriers can be engineered by altering the surface phonon modes present in the surrounding hBN. A simplistic picture of a phonon mode in a diatomic molecule can be understood through a ball and spring model where the energy of the mode depends on the direction of oscillation, force constant of the spring (bond strength), and the mass of the balls (mass of the atoms) (see Fig. 4.7 and 5.1(b)). Thus, a vibration mode in a crystal can be altered by either changing the bonding strength or the masses of the constituting atoms. In hBN, this can be achieved by modifying the isotopic mass of constituting atoms. ^{10}B and ^{11}B are two isotopes of boron where the later has an extra neutron in the nuclei and thus a larger atomic mass. This difference in the atomic mass has a profound effect on the vibration modes (phonons) present in h^{10}BN and h^{11}BN crystals. For example, isotopically pure hBN (hBN with only either ^{10}B or ^{11}B) have higher thermal conductivity as compared to natural hBN (composed of 20%

^{10}B and 80% ^{11}B) because of reduced phonon scattering from isotope induced atomic mixing and higher phonon lifetimes at the interface of conducting media like graphene[108–110]. A recent work on isotopically rich hBN using first principle calculations shows a shift in phonon dispersion between h^{10}BN and h^{11}BN[111]. Thus it is indispensable to understand the effect of these isotopic order and disorder in device conductivity and mobility when semiconducting channels are fabricated with isotopically pure hBN as the substrate and as an encapsulant.

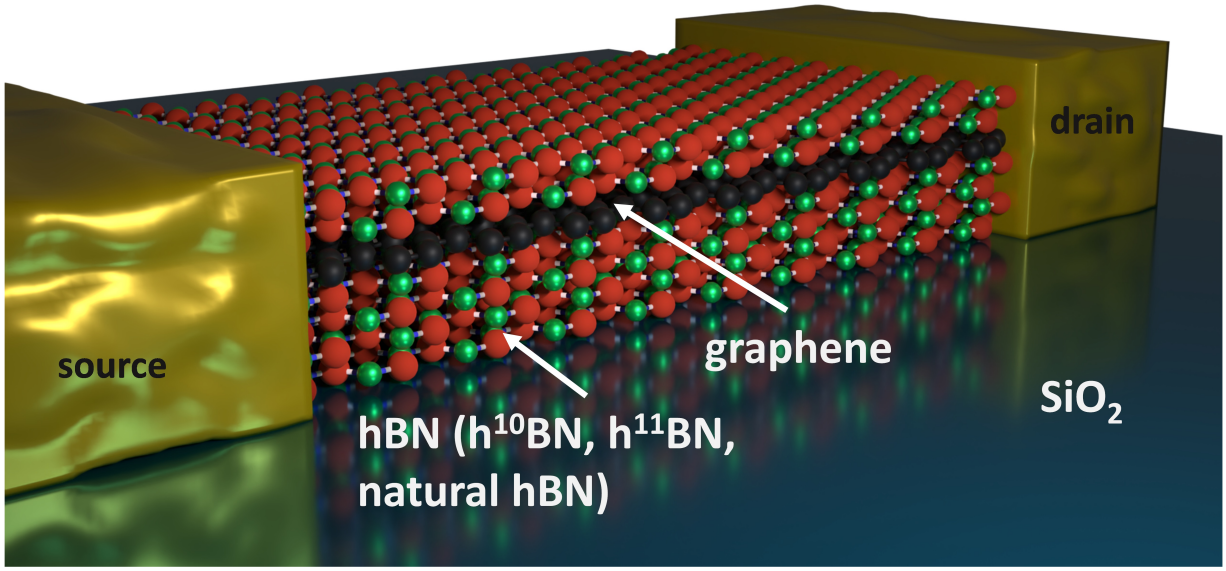


Figure 5.2: *A solid model showing different material stack for graphene encapsulated in isotopically pure and natural hBN.*

In this chapter, the effect of isotopic mixing of boron isotopes in hBN is studied by employing them as both the substrate and the encapsulation layer in HGFETs with ^{10}B enriched, ^{11}B enriched, and natural hBN and studying their electrical transport and LFN measurements. Temperature dependent transport measurements allows the probing of RIP scattering emerging from the difference in boron atomic masses and lattice vibration. This difference in RIP scattering stems from the the surface polar phonon modes present in various hBN crystals. Moreover, temperature dependent LFN measurements were performed to extract the Hooge parameters in these devices to compare the noise levels in HGFETs fabricated with hBN containing various boron isotope concentrations.

5.1 Device fabrication

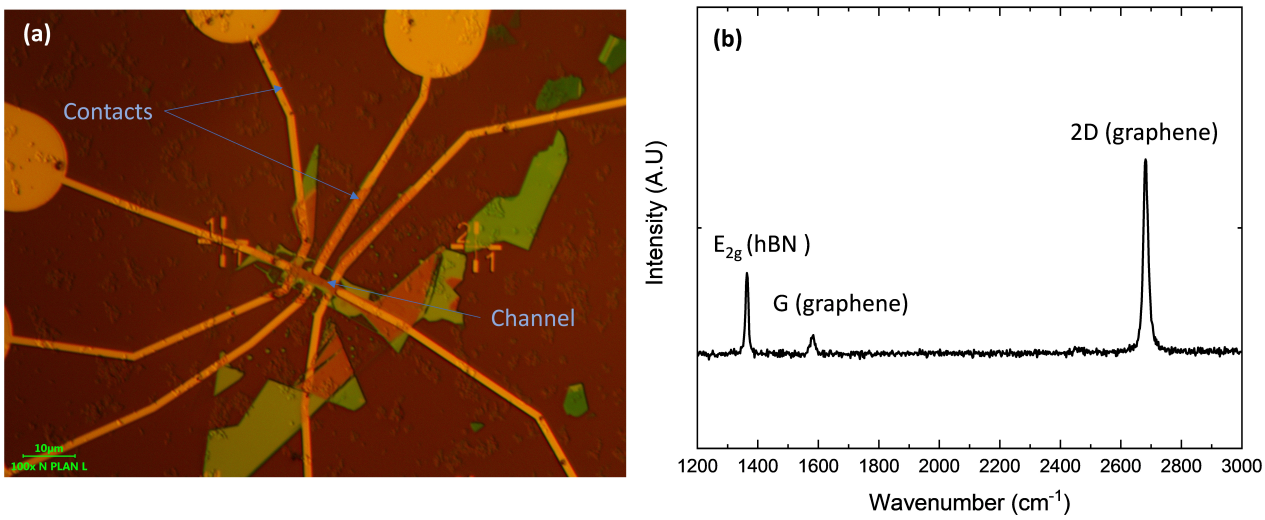


Figure 5.3: *(a) Optical micrograph of a fabricated HGFET showing the metal contacts and the electrical channel. (b) Raman spectrum of the heterostructure channel showing the E_{2g} peak of hBN, G peak of graphene, and 2D peak of graphene.*

HGFETs with a material stack of h^{x}BN/graphene/h^{x}BN were fabricated, where 'x' corresponds to hBN with different boron isotope concentrations. The isotopic compositions of the hBN included ^{10}B and ^{11}B enriched, and natural boron (20% ^{10}B and 80% ^{11}B). The hBN van der Waals layers, used as the bottom substrate and top encapsulation, had a thickness of approximately 30 nm, with a single layer of graphene encapsulated between them. The heterostructures were assembled using the dry visco-elastic stamping method as described in chapter 2. The assembled heterostructures were subsequently fabricated into HGFET devices by employing electron beam lithography and reactive ion etching methodologies. Metal contacts (1D edge contact with Ti(5 nm)/Au (80 nm)) were then deposited onto the graphene channel (as detailed in sections 2.2.1 and 2.2.2) to form the electrical connections to the graphene channel. The fabricated devices were then annealed at 300°C in H_2 (5%) in Ar environment for 2 hours to enhance the metal -semiconductor contact properties.

Fig. 5.3(a) displays an optical microscope image of a fabricated HGFET, illustrating the electrical channel and the metal contacts on a Si/SiO_2 substrate. To confirm the presence of a single layer of graphene and the encapsulation by appropriate isotopically pure hBN in

the heterostructures assembled for HGFET fabrication, Raman spectroscopy measurements were performed with a WiTEC Raman spectrometer with a laser power of 200μW at 100× magnification and a set wavelength of 532 nm. Fig. 5.3(b) shows the Raman spectrum of an example hBN/graphene/hBN channel, highlighting the E_{2g} peak of natural hBN, and the G, and 2D peaks of graphene. Notably, the intensity of the G band is significantly lower than the 2D band ($I_G < I_{2D}$) confirming the presence of a single layer of graphene within the hBN/graphene/hBN heterostructure. Additional microscope images and Raman spectra of the HGFETs for $h^{10}BN$ and $h^{11}BN$ encapsulated devices can be found in Appendix G.

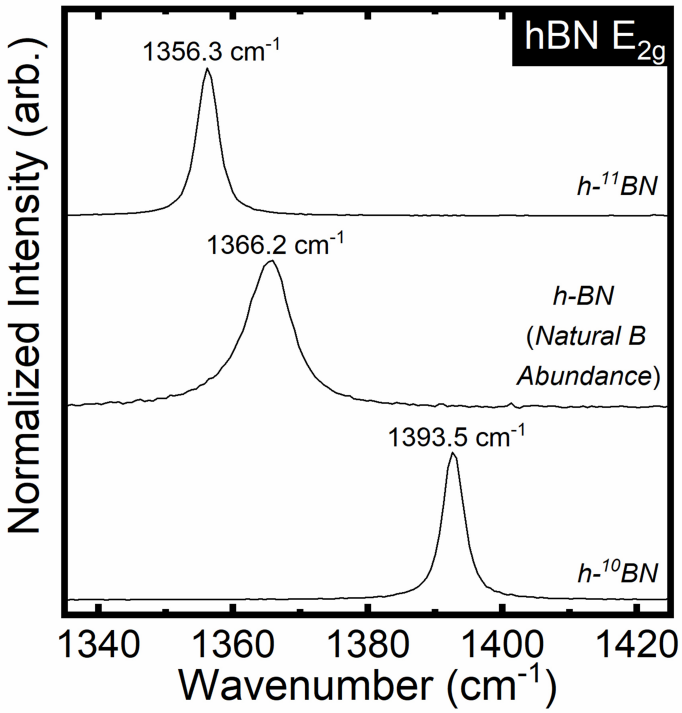


Figure 5.4: *Normalized E_{2g} Raman band of $h^{10}BN$, $h^{11}BN$, and natural hBN taken at similar optical measurement parameters.*

High resolution Raman spectroscopy was performed on hBN enriched with ^{10}B and ^{11}B isotope, and with the natural boron isotope concentration. Fig. 5.4 shows the spectra of $h^{11}BN$ (top), natural hBN (middle), and $h^{10}BN$ (bottom) samples. Fig. 5.4 further shows that as the concentration of ^{11}B increases the Raman peak shifts to a lower energy (red shift) with the $h^{11}BN$ E_{2g} peak at 1356.3 cm^{-1}, $h^{10}BN$ at 1393.5 cm^{-1}, and natural hBN at an intermediary location of 1366.2 cm^{-1}. This shift in Raman line positions in the hBN samples

with different boron isotopic concentration can be attributed to the energy of the vibrating lattice where the frequency or energy of vibration can be approximated as[108]:

$$E \propto \omega \propto \sqrt{\frac{k}{m}} \tag{5.1}$$

where k is the spring constant or the bonding strength, and m is the reduced mass. From Eqn. 5.1 one can deduce that as the reduced mass, m decreases, the vibrational energy of the crystal increases as confirmed by the shift of Raman line positions shown in Fig. 5.4. Our Raman spectra for isotopically pure hBN are also consistent with previous studies.[108;109] A separate theoretical study using first principle calculations also confirms the shifts in energy levels for Raman active optical phonon modes in $h^{11}BN$ and $h^{10}BN$ reaffirming the line shifts seen in Fig. 5.4.[111] The Raman active E_{2g} modes were analyzed by fitting to Lorentzian function to obtain the peak position and the full width at half maximum (FWHM) for the three types of hBN samples. The FWHM values for $h^{10}BN$ and $h^{11}BN$ were 6.7 cm^{-1} and 6.9 cm^{-1}, respectively with a significant increase to 9.4 cm^{-1} in the natural hBN type. This wider FWHM in natural hBN has been attributed to quartic anharmonic decay (4-phonon scattering effect) as compared to cubic anharmonic decay (3-phonon scattering effect) in isotopically pure hBN.[112]

5.2 Electrical Transport

Three and five terminal electrical transport measurements were performed on the fabricated set of devices at operating temperatures between 10K and 300K in a dry helium cooled cryostat. The temperature dependent electrical transport measurements are necessary to probe the interaction of charge carriers and phonons in the heterostructure (see sections 3.1). Fig. 5.5 shows the I_{ds} (drain current) vs V_{ds} (drain voltage) plots for HGFETs with natural hBN (a), $h^{10}BN$ (b), and $h^{11}BN$ (c) layers measured at an operating temperature of 10K for different gate voltages. The plots in Fig. 5.5 illustrate the linear dependence of I_{ds} with V_{ds} thus confirming the contacts between the metal and the semiconducting channel

were Ohmic. The current alsochanged with the overdrive gate voltages (V_G-V_{CNP}) which illustrate gate dependence of channel conductivity in all the three samples.

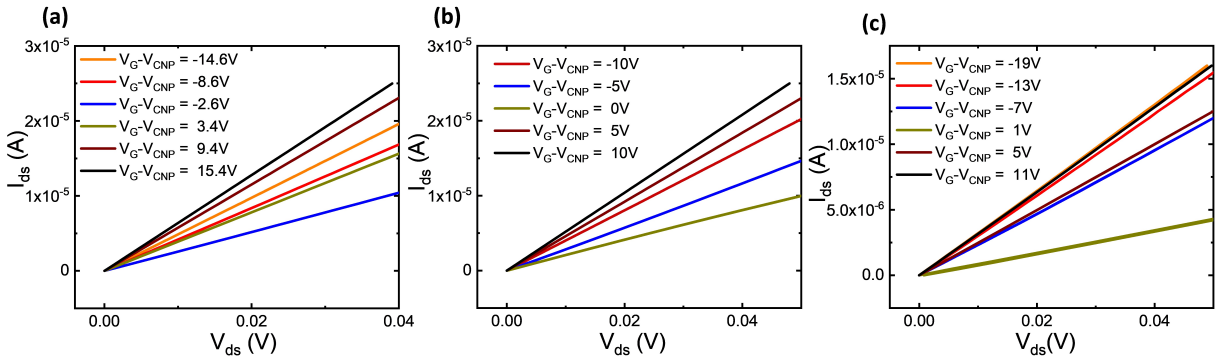


Figure 5.5: *I_{ds} vs. V_{ds} plots for HGFETs encapsulated in natural hBN (a), $h^{10}BN$ (b), and $h^{11}BN$ (c).*

Fig. 5.6 shows the gate dependent cryogenic transport behavior in the three devices at various operating temperatures. Fig. 5.6 (a–c) displays the five-terminal and 3-terminal resistance measured at different gate voltages corrected by charge neutrality point (CNP) in semi–log plots at multiple operating temperatures where ρ is resistivity and t is the film thickness. The 3–terminal resistances (dashed lines) are roughly an order of magnitude higher than the measured 5–terminal resistance values (solid lines) due to the added contact resistance. The 5–terminal resistances are in the range of 100Ω –1000Ω when operated away from the charge residual regime (non shaded region in Fig. 5.6a-c). Diffusive transport characteristics are observed in this regime as the electrical resistivity reduces with temperature (see section 4.4). However, the trend is opposite within the charge residual region (shaded region around CNP in Fig 5.6) where the electrical resistance increases as the temperature decreases. This behavior is due to the presence of electron–hole puddles in the graphene channel (see section 4.6). To understand the effect of surface phonons in isotopically pure and natural hBN, temperature dependent analysis of the data were conducted away from the charge residual region where the electrical channel has a homogenous charge profile of either electrons or holes.

Field effect mobility values (μ_{FE}) for the three devices were calculated by using Eqn. 4.5. However, to accurately calculate the field effect mobility in our devices where a constant

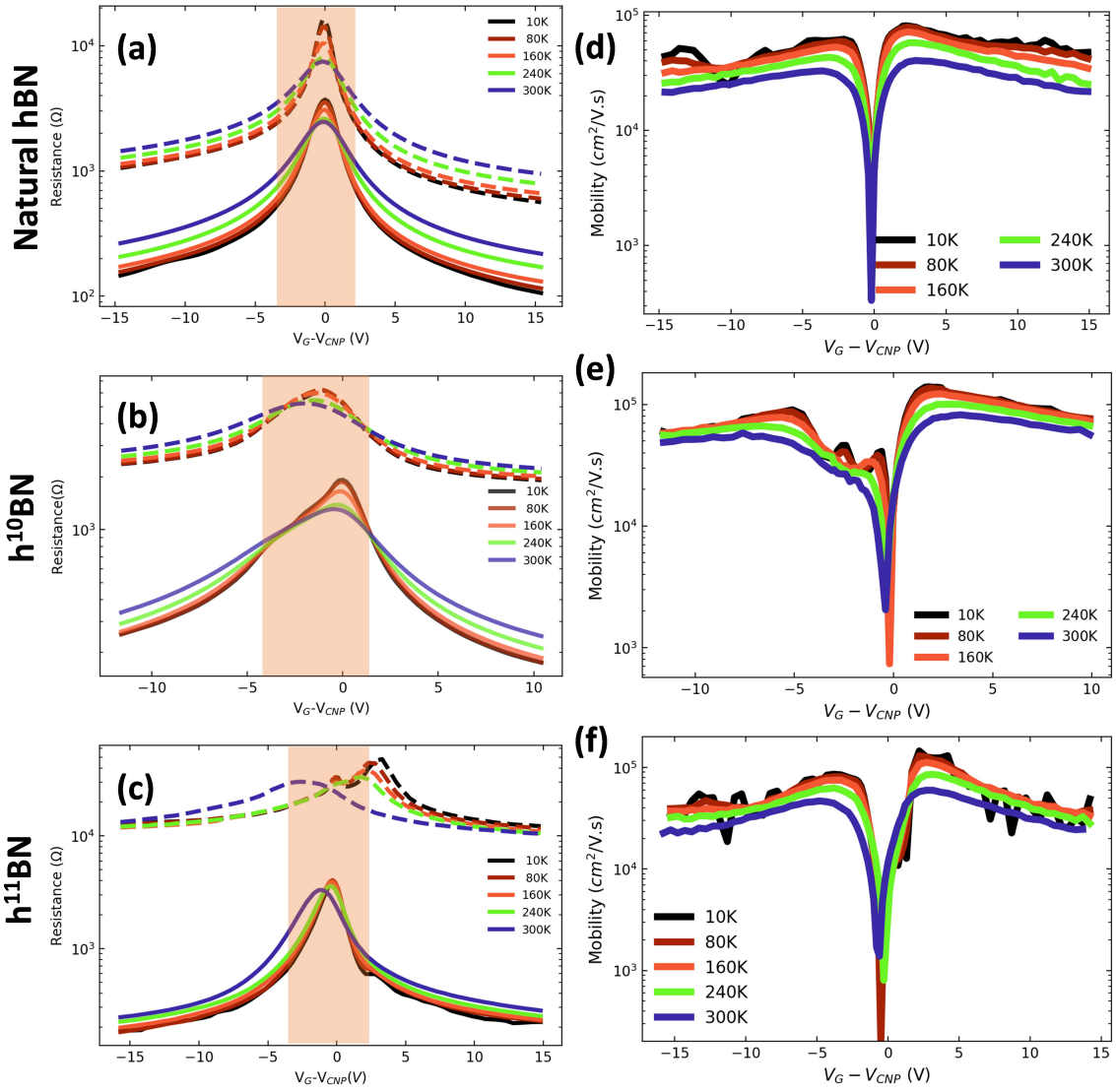


Figure 5.6: *Three-terminal (dashed) and five-terminal (solid) resistance of the HGFETs encapsulated and fabricated with natural hBN (a), $h^{10}BN$ (b), and $h^{11}BN$ (c) as substrates. Extracted five-terminal field effect mobility in the HGFETs fabricated using natural hBN (d), $h^{10}BN$ (e), and $h^{11}BN$ (f) as the substrate and encapsulating material.*

current was sourced (in case of five-terminal measurements), the field effect mobility was calculated by:

$$\mu_{FE} = \frac{\frac{d1/R}{dV_g}}{C_{ox}} \frac{L}{W} \tag{5.2}$$

where R is the five-terminal resistance of the device, L and W are the length and width of the graphene channel, respectively. C_{ox} is the gate capacitance per unit area given by

(ϵ_{ox}/d_{ox}) where ϵ_{ox} is the dielectric constant of hBN and d_{ox} is the dielectric thickness. The net dielectric capacitance is set by SiO_2 when an hBN layer is placed between the SiO_2 and graphene. For an SiO_2 dielectric of thickness $d_{ox} = 300$ nm and $\epsilon_{ox} = 3 \times 10^{-11}$ F/m, C_{ox} is 1×10^{-4} F/m^2 [113].

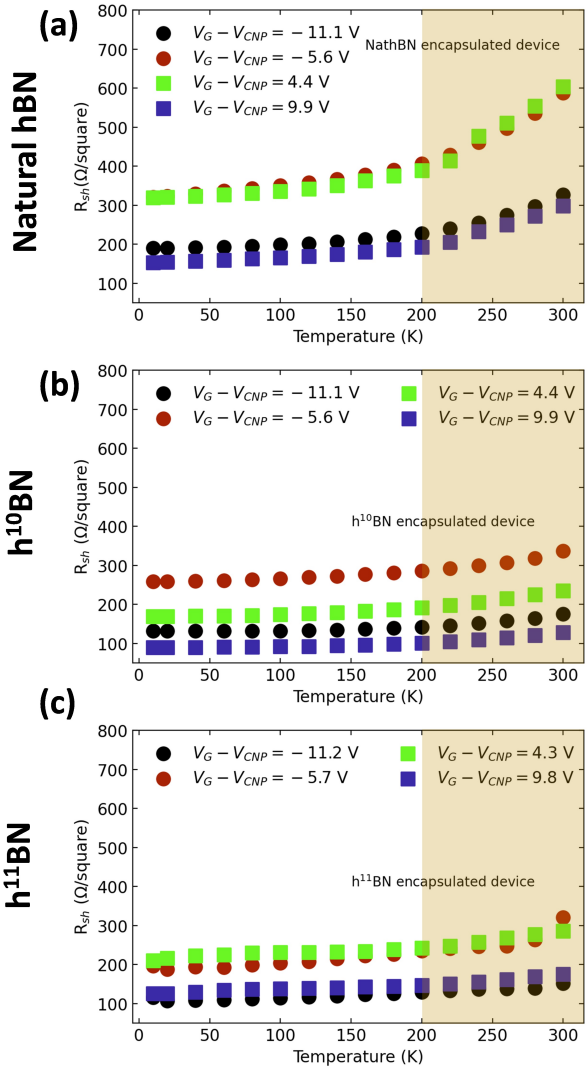


Figure 5.7: *Sheet resistance plotted as a function of operating temperature for various gate overdrive voltages for HGFETs encapsulated within natural hBN (a), $h^{10}BN$ (b), and $h^{11}BN$ (c).*

Fig. 5.6 (d–f) shows the extracted field effect mobilities for the three HGFETs as a function of applied overdrive gate voltages at multiple operating temperatures. In the saturation region (away from charge residual region) the mobility increases as the operating temperature

is reduced validating diffusive transport in the graphene channels (see Eqn. 4.1). Peak mobility values in natural hBN, h^{10}BN, and h^{11}BN encapsulated devices are $\approx$ 100,000 $cm^2/V.s$ at 10 K. The mobility peak values drop to $\approx$ 40,000 $cm^2/V.s$, $\approx$ 80,000 $cm^2/V.s$, and $\approx$ 60,000 $cm^2/V.s$ at 300K, for natural hBN, h^{10}BN, and h^{11}BN encapsulated devices respectively. This lowered mobility values at higher operating temperatures (as seen in Fig. 5.6) can be attributed to electrons or charge carriers experiencing scattering from different thermally activated sources including phonons. This dissertation focuses on the interaction of charge carriers and thermally activated phonons. These phonons are present within the electrical channel and at channel/substrate interfaces. In this chapter, the effects of electron-phonon coupling on the electrical transport is further studied, with a particular emphasis on electron-surface polar phonon coupling in graphene/hBN heterostructure with different boron isotopic concentrations. The measurements on HGFETS devices were conducted from cryogenic to room temperatures. These temperature dependent electrical transport measurements allow us to study the physical properties of phonons that scatter electrons.

In section 4.4, we saw that the net resistivity (or conductance) of graphene is strongly affected by different scattering events experienced by the charge carriers in the channel. These scattering mechanisms are broadly categorized as short- and long-range scattering effects from lattice centers, defects, electron-phonon coupling, etc. to name a few[36;37]. Moreover, the underlying substrate also induce long range potentials like Coulombic potentials from trapped charges and electron-phonon coupling from surface phonons.[38;87–89;114]

To understand the role of different boron isotope concentrations in hBN on the transport in graphene, graphene's sheet resistance (R_{sh}) was calculated from the five-terminal electrical transport measurements in the three types of samples. The sheet resistance (R_{sh}) can be calculated from the resistance as:

$$R_{sh} = \frac{\rho}{t} = \frac{R \times W}{L} \tag{5.3}$$

where ρ, t, R, W, and L are the resistivity, thickness, resistance, width, and the length of the electrical channel, respectively. Fig. 5.7(a-c) shows the sheet resistance of the graphene

channel in HGFETs encapsulated by natural hBN, $h^{10}BN$, and $h^{11}BN$, respectively. Just like electrical resistivity, graphene's sheet resistance can be further written as (see section 4.4.3):

$$\begin{aligned} R_{sh} &= (R_0 + R_{LA} + R_{RIP}) \times \frac{W}{L} \\ \rho/t &= \big(\rho_0 + \rho_{LA} + \rho_{RIP}\big)/t \end{aligned} \tag{5.4}$$

where ρ_0 is the residual resistivity due to defects, imperfections, carrier-carrier scattering, carrier-lattice scattering etc. ρ_{LA} is the resistivity from the electron-phonon coupling from longitudinal acoustic phonons in graphene and ρ_{RIP} represents the resistivity arising from electron-phonon coupling with surface polar modes in the substrate and encapsulating hBN. We are particularly interested in studying and analyzing ρ_{RIP} in the devices to differentiate the effects of surface modes in the three different types of hBN.

Analyzing the temperature dependent scattering, RIP scattering dominates over LA scattering at higher temperatures ($> 180K$) (see Fig. 4.9). This temperature regime where RIP dominates over LA scattering is shaded in Fig. 5.7 for reference. The sheet resistance (and resistivity) of the graphene channel has several key differences in the RIP regime when encapsulated with natural hBN as compared to isotopically pure hBN films. Firstly, the R_{sh} rises at a higher rate with temperature in the RIP regime for HGFETs fabricated with natural hBN as compared to HGFETs encapsulated with isotopically pure hBN. Secondly, the rate of rise of R_{sh} is higher at gate voltages closer to charge neutrality point or the Dirac point (V_{CNP}) in all three types of devices as compared to gate voltages farther away from V_{CNP}. These differences seen in Fig. 5.7 suggest different levels RIP scattering from the surface polar phonons present in natural hBN as compared to isotopically pure hBN counterparts.

To quantify the effect of RIP scattering in the devices, the extracted sheet resistance (R_{sh} or ρ/t) in the three devices were fitted to the resistance model (Eqn. 4.17 and 5.4) as:

$$R_{sh} = \left[R_0 + \frac{\pi D^2 k_B T}{4e^2 \hbar \rho_m v_f^2 v_{ph}^2} + B\left(\frac{1}{e^{101.6\ meV/k_BT} - 1} + \frac{1}{e^{195.7\ meV/k_BT} - 1}\right)\right] \times \frac{W}{L} \tag{5.5}$$

where $B \propto V_g^{-\alpha}$ is a gate voltage dependent fitting parameter and α is typically $\approxeq 1$. The other fitting parameters in Eqn. 5.5 are R_0 and D which represent the residual sheet resistance and the deformation potential from LA phonons, respectively. The two exponential terms in Eqn. 5.5 represent the two surface polar modes for hBN that couple to the charge carriers to create RIP scattering in the electrical channel. The fitting parameter B (which is proportional to $V_g^{-\alpha}$) qualitatively represents the fraction of carriers actively interacting with the available surface phonons. A higher value of B suggests a higher ratio of phonons to carriers resulting in higher scattering, whereas a lower value of B suggests a lower ratio of available phonons to carriers resulting in lower scattering.

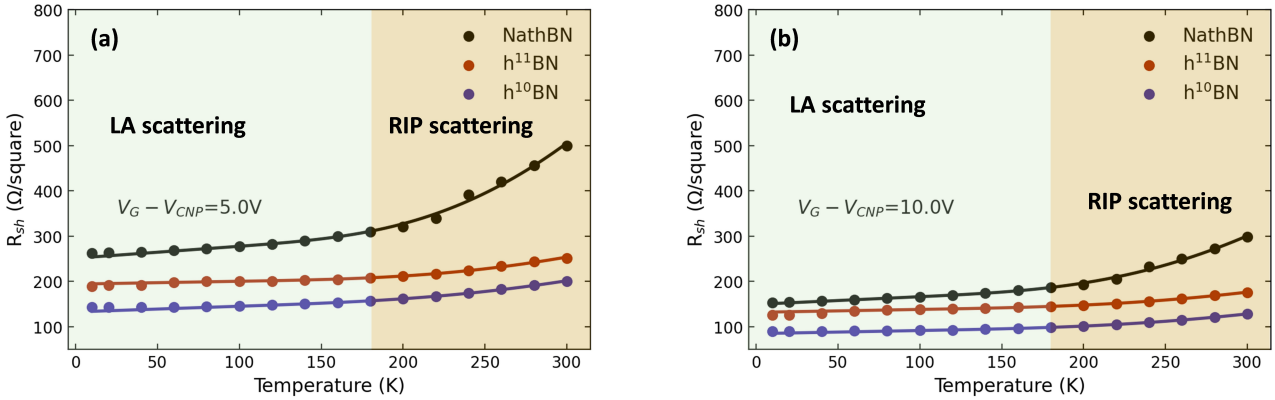


Figure 5.8: *Sheet resistance for HGFETs encapsulated in natural hBN, $h^{10}BN$, and $h^{11}BN$ as a function of operating temperature at overdrive gate voltages of 5V (a) and 10V (b). RIP scattering region is marked with increasing R_{sh} value for visual representation.*

Fig. 5.8(a,b) shows the sheet resistance of the graphene channels in three different heterostructures at gate overdrive voltages of 5V and 10V, respectively. Clearly the exponential rise of sheet resistance at elevated temperatures is significantly higher in graphene FETs encapsulated in natural hBN and at gate voltages closer to the charge neutrality point. This nonlinear behavior of R_{sh} with respect to operating temperature is shaded as RIP scattering regime while the linear regime is shaded as the LA scattering regime in Fig. 5.8 (note that the LA vs. RIP region demarcation is for visual representation only). The solid lines in Fig. 5.8 show the sheet resistance or ρ/t values fitted to Eqn. 5.5 confirming a good fit to the temperature dependent resistance model. The resistivity data from all the three devices were fitted

and the RIP scattering contributions from each of the device are shown in Fig. 5.9 (a,b) at gate overdrive voltages of 5V and 10V, respectively. The figure clearly shows that the electrical resistance originating from RIP scattering (which depends on surface polar phonons) is absent at lower temperatures and starts growing exponentially at $\approxeq$ 150K. Furthermore, RIP scattering component in natural hBN is $\approx$ 3 to 4$\times$ higher as compared to isotopically pure counterparts. In all hBN types, the RIP scattering is smaller at higher overdrive voltage, for eg. 10V compared to 5V (Fig. 5.9(b)). Although the difference in contribution of RIP scattering in $h^{10}BN$ and $h^{11}BN$ encapsulated graphene FETs is small, $h^{10}BN$ encapsulation has a slightly lower contribution, suggesting $h^{10}BN$ encapsulation of graphene yields the best device with least RIP scattering at elevated operating temperatures.

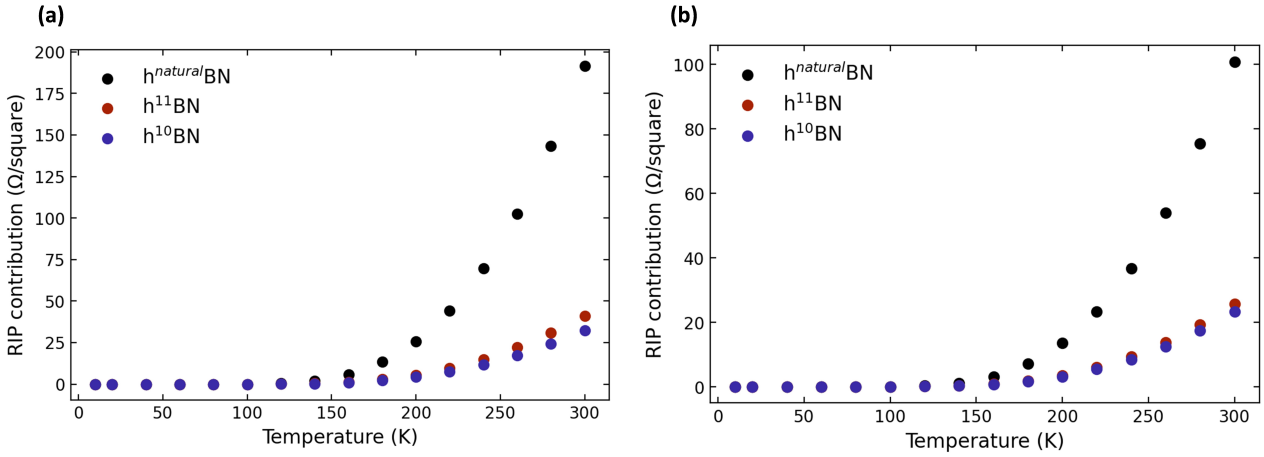


Figure 5.9: *Extracted RIP contribution from natural hBN, $h^{10}BN$, and $h^{11}BN$ at gate overdrive voltages of 5V (a) and 10V (b).*

The reduced RIP scattering at higher gate voltages for a given HGFET and at a given temperature (Fig. 5.9(a-b)) can be explained by the reduced fraction of charge carrier scattering as explained earlier (fitting parameter $B \propto V_g^{-\alpha}$). The temperature dependent RIP scattering is an interplay between phonons present in hBN statistically described by Bose-Einstein distribution (controlled by temperature) and the charge carriers in the graphene channel statistically described by Fermi-Dirac distribution (controlled by gate voltage).

5.2.1 Explanation of RIP contribution to resistivity for different HGFETs

As the reduced mass of natural hBN lies between the reduced mass of $h^{10}BN$ and $h^{11}BN$, one might naively expect the RIP contribution from natural hBN to lie between the isotopically pure counterparts (see Eq. 5.1). However, we observed a significant deviation in natural hBN's RIP contribution in Fig. 5.9 at a constant gate overdrive voltage. In this section, we formulate a deeper understanding to explain the systematic variation in RIP for various HGFETs by shedding light on the role of fitting parameter B in Eq. 5.5. As mentioned before, the parameter B quantifies the fraction of charge carriers experiencing scattering to the total number of charge carriers present (conducting) in the channel. The large difference in RIP contribution between natural hBN and isotopically pure hBN is observed for the first time in this study and constitutes one of the main findings of this dissertation. The presence of a larger number of low energy surface polar phonons in natural hBN that scatter the conducting electrons in the graphene channel as compared to isotopically pure hBN counterparts inspires future theoretical calculations. Phenomenologically, this observation can be explained through a phonon band broadening theory[115;116].

An isotopic mass mixing of ^{10}B and ^{11}B in natural hBN (typically $\approx$ 80% ^{11}B and 20% ^{10}B) leads to broadening of the phonon dispersion compared to individual isotopically pure hBN[115;116], thereby distributing available phonon energies in a wider available energy range at fixed phonon momenta. Bose-Einstein statistics governs the population of phonons $n(E)$ at a given temperature, T and with energy (E) as:

$$n(E) = \frac{1}{e^{E/k_BT} - 1} \tag{5.6}$$

The broadening of the phonon bands can be quantified by adding an energy perturbation (Δ) in Eq. 5.6 and can be written as:

$$n(E) = \frac{1}{e^{E \pm \Delta/k_BT} - 1} \tag{5.7}$$

which leads to an increased number of phonons in a broadened state by a factor of $\kappa = \frac{E^2}{E^2-|\Delta|^2}$. Naturally, the larger magnitude of broadening (Δ), leads to higher number of phonons in natural hBN. The effects of phonon broadening like higher phonon decay in natural hBN have been previously studied[110;112;115–117]. These higher number of low energy surface phonons lead to higher RIP scattering of channel electrons in the HGFETs using natural hBN as the substrate and encapsulating material as compared to isotopically pure hBN.

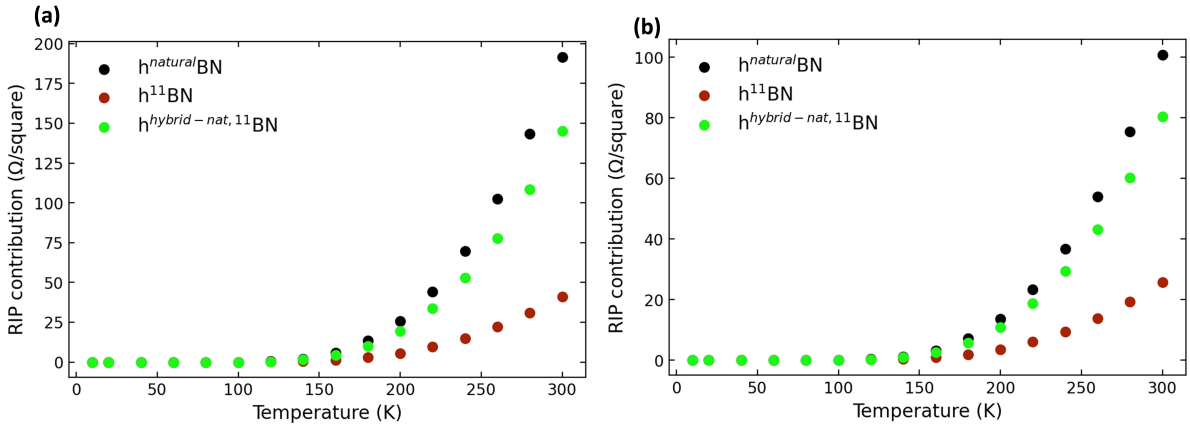


Figure 5.10: *Extracted RIP contribution from natural hBN, hybrid-hBN, and $h^{11}BN$ at gate overdrive voltages of 5V (a) and 10V (b).*

To further strengthen this understanding, an HGFET device was fabricated with natural hBN as the substrate to the SLG channel and $h^{11}BN$ as top encapsulation) called as a hybrid HGFET. Cryogenic transport was measured and the resistivity contribution to RIP scattering was extracted. Fig. 5.10 (a,b) compares RIP scattering of HGFETs with natural hBN, $h^{11}BN$, and hybrid hBN operated at V_G-V_{CNP} of 5V and 10V, respectively. The RIP contribution of the hybrid HGFET is close to that of natural hBN with $h^{11}BN$ showing more than 4 $\times$ lower RIP contribution. This demonstrates that even though the presence of $h^{11}BN$ provides a lower number of low energy phonons in the system, natural hBN on the other side acts as the scattering bottleneck by providing greater number of low energy polar phonons to the graphene channel leading to more RIP scattering. This agrees with the phonon broadening phenomena explained above.

To conclude, using isotopically pure hBN in HGFETs leads to a 3 to 4 $\times$ reduction of

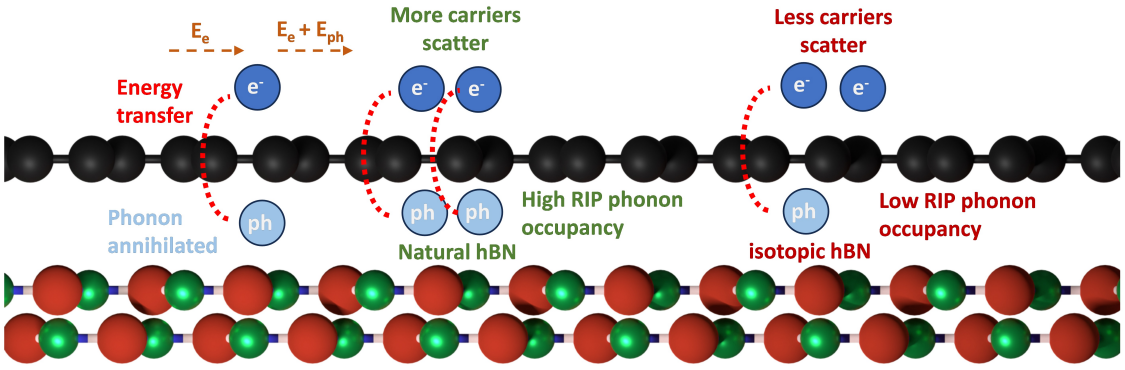


Figure 5.11: *A schematic model showing the origin of large RIP scattering in graphene channel encapsulated by natural hBN as compared to isotopically pure hBN.*

RIP scattering at room temperature, significantly enhancing the energy efficiency of the engineered HGFET devices in addition to their high performance (ultra high mobility) and ultra-low noise performances. The presence of natural hBN in the vicinity of graphene is the limiting factor that generates higher *RIP* scattering in HGFETs, and thus restricts device performances at elevated temperatures (>200K). Fig. 5.11 shows a phenomenological model of electrons (in the graphene channel) and *RIP* phonons (in hBN) scattering in both natural and isotopic hBN. Fig. 5.11 shows two cases when graphene is encapsulated by natural and isotopically pure hBN. The presence of more RIP phonons in natural hBN leads to greater degree of coupling between surface modes to electrons in the graphene channel. Fig. 5.11 further shows the reduction of RIP coupling when isotopically pure hBN films are used. This reduction in phonon coupling is due to lower number of surface phonons.

5.3 Low frequency noise

Next, the low frequency noise (LFN) were measured in the fabricated HGFETs using $h^{10}BN$, $h^{11}BN$, and natural hBN films as the substrate and as the encapsulant. Noise measurements were performed in both three-terminal and five-terminal device configuration to extract the true channel noise in their channels[86]. Current noise spectral density (S_I) and voltage noise spectral density (S_V) were measured in all the devices at a frequency range of 0.4 Hz to

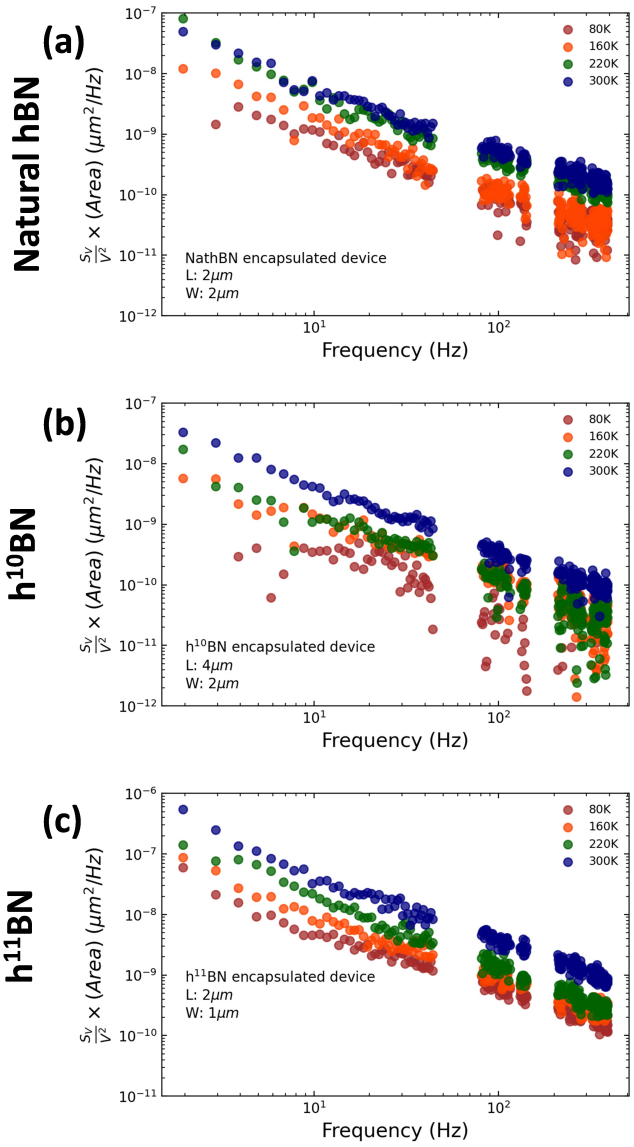


Figure 5.12: *Extracted voltage noise spectral density normalized by area and voltage as a function of frequency for various temperatures in HGFETS with natural hBN (a), $h^{10}BN$ (b), and $h^{11}BN$ (c).*

490 Hz to record the three-terminal and five-terminal noise, respectively. The circuitry used for these measurements was shown in Fig. 3.7 in section 3.2.4. Note that the electrical resistance measurements, where a standard combination of three-terminal and five-terminal measurements is used to get rid of contact resistance, will not be sufficient to determine the true channel noise.The channel noise was extracted by a Thevenin equivalent noise analysis as detailed in section 3.2.4 in the HGFET devices. The channel noise can be represented by:

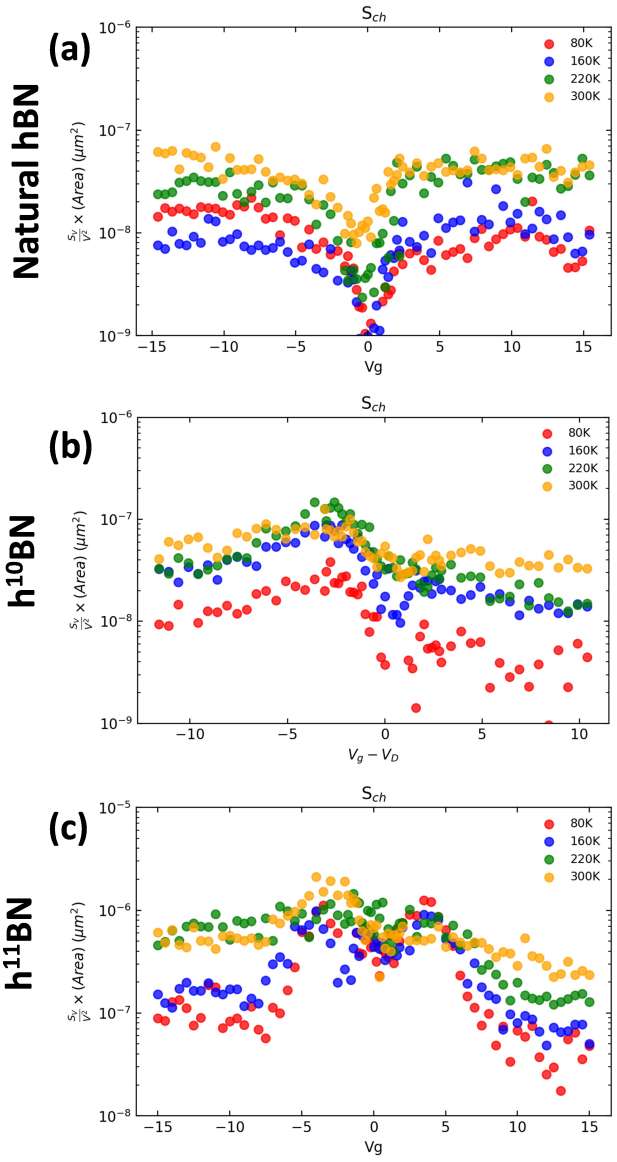


Figure 5.13: *Area and frequency normalized voltage noise spectral density in the graphene channel as a function of gate overdrive voltage for various temperatures in HGFETs with natural hBN(a), $h^{10}BN$(b), and $h^{11}BN$(c).*

$$\frac{S_V}{V^2} = \frac{S_I}{I^2} = \frac{S_R}{R^2} \tag{5.8}$$

where S_V, S_I, and S_R are measured or extracted voltage, current and resistance noise spectral density, respectively. Fig. 5.12 shows voltage channel noise (or the noise amplitude)

normalized with the device area, given for the three devices by:

$$A = \frac{S_V \times Area}{V^2} \tag{5.9}$$

where V is the voltage drop across the channel under consideration operated at different temperatures. All the spectra displayed in Fig. 5.12 are obtained at gate overdrive voltage (V_G-V_{CNP}) of 9.9V showing the inverse scaling of noise amplitude with respect to frequency ($1/f$ behavior). The normalized noise amplitude shows reasonable scaling with temperature where the noise levels increase with increasing temperature. This suggests thermally activated traps leading to higher noise according to the Hooge's noise model[60].

The noise amplitude for both electron and hole transport can be visualized with respect to the applied gate overdrive voltage (V_G-V_{CNP}) by setting a fixed frequency and normalizing the noise amplitude by frequency, as shown in Fig. 5.13. It further shows the obtained area and frequency normalized noise spectra for the three HGFET devices as a function of V_G-V_{CNP} at various operating temperatures and at a set frequency of 30 Hz. The rise in overall noise levels with the increase in device operating temperature is evident in Fig. 5.13 further confirming the thermally activated interface traps present in all three types of devices contributing towards the electrical channel noise.

The net noise in the devices can be quantified by using Hooge's relation to calculate the Hooge paramater (α_H). Hooge's parameter for the three devices were calculated by:

$$\frac{S_V}{V^2} \times f = \frac{\alpha_H}{n \times Area} \tag{5.10}$$

where n is the charge density in the graphene channel. Hooge's parameter is a net noise figure of merit in the device. Fig. 5.14 (a-c) shows the extracted Hooge parameter with respect to obtained carrier mobility for the three HGFETs at 80K, 200K, and 300K, respectively for the graphene channels encapsulated by $h^{10}BN$(black), $h^{11}BN$ (green), natural hBN (red), and hybrid hBN (natural and $h^{11}BN$) (blue). The Hooge parameters are between 10^{-5} and 10^{-2} at 80 K and between 10^{-5} and 10^{-1} at 300K showing ultra-low levels of low frequency noise

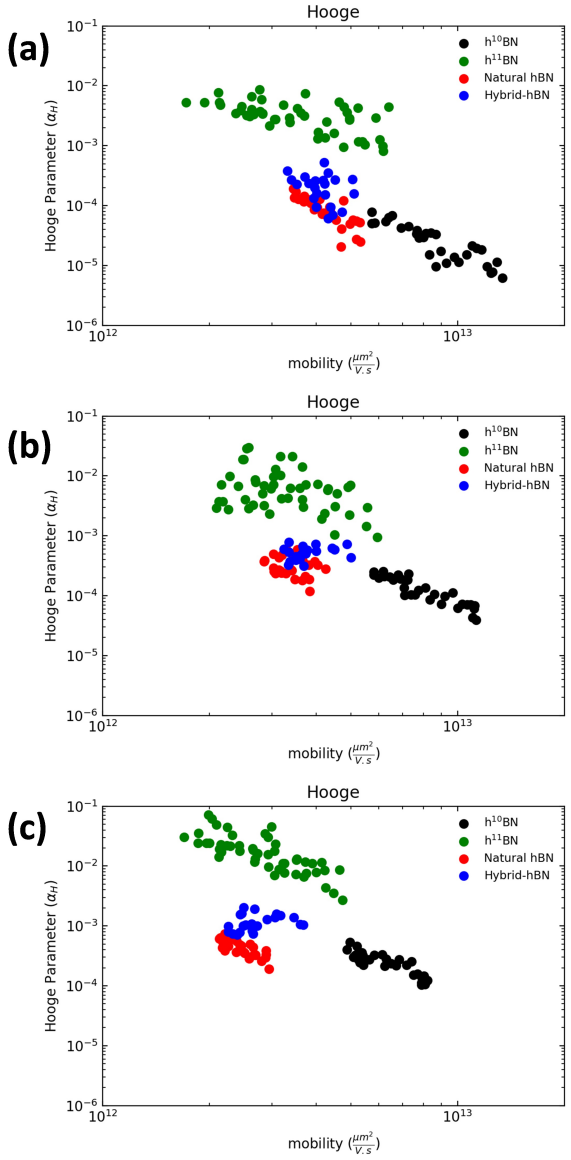


Figure 5.14: *Extracted Hooge parameter as a function of carrier mobility in HGFET devices using natural hBN, $h^{10}BN$, and $h^{11}BN$ at operating temperatures of 80K(a), 200K(b), and 300K(c).*

in the fabricated HGFETs. Furthermore, the inverse power dependence of Hooge parameter with respect to extracted mobility indicates mobility fluctuations originating from thermally activated charge traps for the studied devices[60;67;74]. Fig. 5.14 also illustrates that the α_H values obtained for $h^{11}BN$ encapsulated devices are roughly an order of magnitude higher as compared to $h^{10}BN$ and natural hBN encapsulated devices. This observation suggests the presence of higher density of traps in $h^{11}BN$ crystals as compared to $h^{10}BN$ crystals. This

allows future avenues for defect studies in transistor devices using engineered hBN crystals.

Chapter 6

Conclusions and Future Work

The work presented in this dissertation studied the fundamental mechanisms that govern the electrical transport and low frequency noise in graphene heterostructure field effect transistors fabricated using hexagonal boron nitride as the substrate and encapsulating material with 1-dimensional edge contacts. Natural hBN and hBN with boron isotopically purity with ^{10}B and ^{11}B were used to encapsulate a single layer of graphene and study the device transport and noise characteristics. The electrical transport in the graphene channel in HGFET devices behave differently within the charge residual region and away from the charge residual region. Away from the charge residual region, the charge carriers (electrons and holes) undergo diffusive transport where they experience scattering from crystallographic defects, charge defects, crystal vibrations, surface phonons etc.

Temperature dependent electrical transport measurements were used to demonstrate that the charge carriers in the graphene channel encapsulated by hBN experience scattering from longitudinal acoustic phonons and remote interfacial phonons at higher operating temperatures. Temperature dependent electrical resistivity further confirmed that LA scattering increases linearly with temperature, whereas RIP scattering increases exponentially as a function of temperature above ≋150K. These temperature dependent carrier scattering show that RIP scattering dominates over LA scattering by $\approx 6\times$ at room temperature with RIP scattering expected to dominate heavily at elevated temperatures. At lower temperatures

however, ($\leq$150K) LA scattering dominates over RIP scattering. We also showed that the surface phonons responsible for RIP scattering in hBN result in $\approx 2\times$ lower RIP scattering at elevated operating temperatures. This further demonstrates that not only hBN has atomically smooth surface but also, is a better dielectric for high mobility graphene FETs as compared to SiO_2. Low frequency noise measurement was used to characterize the trap states in the fabricated HGFETs. Hooge parameter, an electrical noise figure of merit was extracted on the fabricated HGFETs by performing $1/f$ low frequency noise measurements. The obtained Hooge parameter values lied between 10^{-5} and 10^{-2} showing ultra low levels of noise. The obtained Hooge parameter values were then used to extract the collective trap levels by using thermal emission model and the energy levels for the interfacial traps were extracted to be between 5-20 meV.

Electrical transport and low frequency noise measurements were also performed within the charge residual region for the HGFETs and a percolative transport model in the graphene channel was developed where the spatial charge profile was shown to form puddles of electrons and holes. Low frequency noise measurements show that the origin of the noise in this percolation transport regime can be explained through a correlated mobility and number fluctuation model. We show that the measured noise shows a "Λ" shape as a function of gate voltage due to number fluctuations only in contrast to the mobility fluctuation model away from he charge residual region. These number fluctuations can take place from either the charge traps to the channel or from the-non conducting puddles to the percolative channel, due to thermal activation, respectively. On the other hand, "V" shape is observed due to competing mobility and number fluctuations of charge carriers in the graphene channel.

The second part of the study dealt with understanding the electrical transport and low frequency noise in HGFETs with various mixtures of boron isotopes, namely $h^{10}BN$, $h^{11}BN$, and natural hBN (hBN with $\approx$ 80% ^{11}B and 20% ^{10}B). Temperature dependent electrical transport measurements and further analysis were performed on the fabricated devices from room temperature down to cryogenic temperatures in the diffusive transport regime. Further analysis of sheet resistance values in the fabricated devices showed different levels of phonon induced scattering at higher temperatures (LA scattering and RIP scattering).

Most notably, we observed greater degree of RIP scattering in devices encapsulated with natural hBN as compared with isotopically pure hBN. We explain this behavior as the result of phonon band broadening due to isotopic mixing of boron isotopes in natural hBN. The broadened band allows population of higher number of low energy surface phonons that directly result in greater degree of carrier scattering and limits carrier mobility and increases the channel resistance at high temperatures. The origin, impact, and engineering of RIP phonons in HGFETs are demonstrated for the first time in graphene devices. The findings of this study suggests the superior use of isotopically pure hBN as substrate and encapsulating material for room temperature high mobility graphene FETs. Low frequency $1/f$ noise characterizations were also performed on the fabricated HGFETs to extract the Hooge parameter in the devices. The extracted Hooge parameters show power law dependence with field effect mobility confirming mobility fluctations in the channel. We extract Hooge parameter values between 10^{-5} and 10^{-1} for all the devices confirming ultra-low noise in the HGFETs. We observed the lowest noise in HGFETs encapsulated in $h^{10}BN$, followed by natural hBN, while the devices encapsulated by $h^{11}BN$ showed the highest noise or Hooge parameter values.

The full understanding of heterostructure field effect transistors in 2D materials has further future potential. Future work towards high performance and low noise 2D HGFETs may have the following interests:

1. Contact resistance to HGFETs: The electrical transport measurements performed in this dissertation uses five-terminal measurement geometry to circumnavigate the problems posed by large contact resistances formed at the metal-2D semiconductor interface. This large contact resistance can mask the true 2D material channel properties when measurements are performed in a standard (industry preferred) three-terminal measurements. A future direction in 2D HGFET fabrication is, significant reduction of the contact resistance, at least to the level of channel resistance by using novel fabrication geometry, architecture and by using low work function metals as the contact materials.

2. Further isotopic effects: The above work was focused on understanding the effect of modulation of phonons present in the surrounding hBN on the charge carriers in graphene. A similar modulation can also be performed by altering the atomic mass of carbon atoms that form the single layer of graphene. A comparative transport study may be performed by using ^{12}C and ^{13}C based graphene which may have an effect on LA scattering. In contrast to effects on device resistivity at higher temperatures from RIP scattering as discussed in this dissertation, isotopic effects of carbon atoms in the conducting medium of graphene might have profound effects at low cryogenic operating temperatures.

3. Electrical transport in Moire patterned graphene/hBN heterostructures (Twistronics): Studies performed on twisted bilayer graphene have shown promising electronic properties like superconductivity. These observations arise from augmented band structures from Moire lattices formed by relative alignment of bands in the consisting layers of graphene. Due to crystallographic matching between hBN and graphene, similar twisted structures can be formed by relative twisting of the graphene layer as compared to hBN. These twisted heterostructures have potential for novel and exciting electronic and optoelectronic studies due to the presence of satellite Dirac points in the vicinity of the primary Dirac point or charge neutrality point.

4. Integration of graphene and hybrid CMOS devices: Current semiconductor manufacturing industry is highly integrated around using Si or other conventional three dimensional semiconductors. In order to fully leverage/utilize the potential of the properties of 2D materials, a seamless incorporation of 2D materials into the existing 3D semiconductor fabrication industry is indispensable. This requires future large-scale integration of 2D-3D hybrid devices that will act as the missing link between the promises of 2D materials and very large scale integration (VLSI) into commercial large scale device fabrication.

These are just a few ideas for future research directed towards understanding 2D HGFET devices involving novel physics that may lead to a fuller understanding of carrier transport

for a greater goal of integrating 2D materials into nanoscale electronics.

Bibliography

[1] John Shalf. The future of computing beyond moore's law. *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences*, 378(2166): 20190061, January 2020. ISSN 1471-2962. doi: 10.1098/rsta.2019.0061.

[2] R.R. Schaller. Moore's law: past, present and future. *IEEE Spectrum*, 34(6):52–59, June 1997. ISSN 0018-9235. doi: 10.1109/6.591665.

[3] Wei Cao, Huiming Bu, Maud Vinet, Min Cao, Shinichi Takagi, Sungwoo Hwang, Tahir Ghani, and Kaustav Banerjee. The future transistors. *Nature*, 620(7974):501–515, August 2023. ISSN 1476-4687. doi: 10.1038/s41586-023-06145-x.

[4] X. He, J. Fronheiser, P. Zhao, Z. Hu, S. Uppal, X. Wu, Y. Hu, R. Sporer, L. Qin, R. Krishnan, E. M. Bazizi, R. Carter, K. Tabakman, A. K. Jha, H. Yu, O. Hu, D. Choi, J. G. Lee, S. B. Samavedam, and D. K. Sohn. Impact of aggressive fin width scaling on finfet device characteristics. In *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE, December 2017. doi: 10.1109/iedm.2017.8268427.

[5] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, and A. A. Firsov. Two-dimensional gas of massless dirac fermions in graphene. *Nature*, 438(7065):197–200, November 2005. ISSN 1476-4687. doi: 10.1038/nature04233.

[6] A. K. Geim and K. S. Novoselov. The rise of graphene. *Nature Materials*, 6(3):183–191, March 2007. ISSN 1476-4660. doi: 10.1038/nmat1849.

[7] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis. Single-layer mos2 transistors. *Nature Nanotechnology*, 6(3):147–150, January 2011. ISSN 1748-3395. doi: 10.1038/nnano.2010.279.

[8] Mohammed S El-Bana, Daniel Wolverson, Saverio Russo, Geetha Balakrishnan, Don Mck Paul, and Simon J Bending. Superconductivity in two-dimensional nbse2field effect transistors. *Superconductor Science and Technology*, 26(12):125020, November 2013. ISSN 1361-6668. doi: 10.1088/0953-2048/26/12/125020.

[9] Xiaoxiang Xi, Liang Zhao, Zefang Wang, Helmuth Berger, László Forró, Jie Shan, and Kin Fai Mak. Strongly enhanced charge-density-wave order in monolayer nbse2. *Nature Nanotechnology*, 10(9):765–769, July 2015. ISSN 1748-3395. doi: 10.1038/nnano.2015.143.

[10] Theresia Knobloch, Yury Yu. Illarionov, Fabian Ducry, Christian Schleich, Stefan Wachter, Kenji Watanabe, Takashi Taniguchi, Thomas Mueller, Michael Waltl, Mario Lanza, Mikhail I. Vexler, Mathieu Luisier, and Tibor Grasser. The performance limits of hexagonal boron nitride as an insulator for scaled cmos devices based on two-dimensional materials. *Nature Electronics*, 4(2):98–108, February 2021. ISSN 2520-1131. doi: 10.1038/s41928-020-00529-x.

[11] Yury Yu Illarionov, Gerhard Rzepa, Michael Waltl, Theresia Knobloch, Alexander Grill, Marco M Furchi, Thomas Mueller, and Tibor Grasser. The role of charge trapping in mos 2 /sio 2 and mos 2 /hbn field-effect transistors. *2D Materials*, 3(3):035004, July 2016. ISSN 2053-1583. doi: 10.1088/2053-1583/3/3/035004.

[12] L. Wang, I. Meric, P. Y. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L. M. Campos, D. A. Muller, J. Guo, P. Kim, J. Hone, K. L. Shepard, and C. R. Dean. One-dimensional electrical contact to a two-dimensional material. *Science*, 342(6158):614–617, November 2013. ISSN 1095-9203. doi: 10.1126/science.1244358.

[13] Damon B. Farmer, Alberto Valdes-Garcia, Christos Dimitrakopoulos, and Phaedon Avouris. Impact of gate resistance in graphene radio frequency transistors. *Applied Physics Letters*, 101(14), October 2012. ISSN 1077-3118. doi: 10.1063/1.4757422.

[14] Lei Liao and Xiangfeng Duan. Graphene for radio frequency electronics. *Materials*

Today, 15(7–8):328–338, July 2012. ISSN 1369-7021. doi: 10.1016/s1369-7021(12)70138-4.

[15] Ivo Colmiais, Vitor Silva, Jérôme Borme, Pedro Alpuim, and Paulo M. Mendes. Towards rf graphene devices: A review. *FlatChem*, 35:100409, September 2022. ISSN 2452-2627. doi: 10.1016/j.flatc.2022.100409.

[16] Xiaoding Wei, Benjamin Fragneaud, Chris A. Marianetti, and Jeffrey W. Kysar. Nonlinear elastic behavior of graphene:ab initiocalculations to continuum description. *Physical Review B*, 80(20):205407, November 2009. ISSN 1550-235X. doi: 10.1103/physrevb.80.205407.

[17] Fang Liu, Pingbing Ming, and Ju Li. Ab initiocalculation of ideal strength and phonon instability of graphene under tension. *Physical Review B*, 76(6):064120, August 2007. ISSN 1550-235X. doi: 10.1103/physrevb.76.064120.

[18] Changgu Lee, Xiaoding Wei, Jeffrey W. Kysar, and James Hone. Measurement of the elastic properties and intrinsic strength of monolayer graphene. *Science*, 321(5887):385–388, July 2008. ISSN 1095-9203. doi: 10.1126/science.1157996.

[19] Euan J. Boyd and Deepak Uttamchandani. Measurement of the anisotropy of young's modulus in single-crystal silicon. *Journal of Microelectromechanical Systems*, 21(1):243–249, February 2012. ISSN 1941-0158. doi: 10.1109/jmems.2011.2174415.

[20] Jae-Ung Lee, Duhee Yoon, and Hyeonsik Cheong. Estimation of young's modulus of graphene by raman spectroscopy. *Nano Letters*, 12(9):4444–4448, August 2012. ISSN 1530-6992. doi: 10.1021/nl301073q.

[21] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim. The electronic properties of graphene. *Reviews of Modern Physics*, 81(1):109–162, January 2009. ISSN 1539-0756. doi: 10.1103/revmodphys.81.109.

[22] P. R. Wallace. The band theory of graphite. *Physical Review*, 71(9):622–634, May 1947. ISSN 0031-899X. doi: 10.1103/physrev.71.622.

[23] R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber, N. M. R. Peres, and A. K. Geim. Fine structure constant defines visual transparency of graphene. *Science*, 320(5881):1308–1308, June 2008. ISSN 1095-9203. doi: 10.1126/science.1156965.

[24] Sukang Bae, Hyeongkeun Kim, Youngbin Lee, Xiangfan Xu, Jae-Sung Park, Yi Zheng, Jayakumar Balakrishnan, Tian Lei, Hye Ri Kim, Young Il Song, Young-Jin Kim, Kwang S. Kim, Barbaros Özyilmaz, Jong-Hyun Ahn, Byung Hee Hong, and Sumio Iijima. Roll-to-roll production of 30-inch graphene films for transparent electrodes. *Nature Nanotechnology*, 5(8):574–578, June 2010. ISSN 1748-3395. doi: 10.1038/nnano.2010.132.

[25] Keun Soo Kim, Yue Zhao, Houk Jang, Sang Yoon Lee, Jong Min Kim, Kwang S. Kim, Jong-Hyun Ahn, Philip Kim, Jae-Young Choi, and Byung Hee Hong. Large-scale pattern growth of graphene films for stretchable transparent electrodes. *Nature*, 457 (7230):706–710, January 2009. ISSN 1476-4687. doi: 10.1038/nature07719.

[26] Suk Hyun Kang, Sungwook Mhin, Hyuksu Han, Kang Min Kim, Jacob L. Jones, Jeong Ho Ryu, Ju Seop Kang, Shin Hee Kim, and Kwang Bo Shim. Ultrafast method for selective design of graphene quantum dots with highly efficient blue emission. *Scientific Reports*, 6(1), December 2016. ISSN 2045-2322. doi: 10.1038/srep38423.

[27] Jakub Kedzierski, Pei-Lan Hsu, Paul Healey, Peter W. Wyatt, Craig L. Keast, Mike Sprinkle, Claire Berger, and Walt A. de Heer. Epitaxial graphene transistors on sic substrates. *IEEE Transactions on Electron Devices*, 55(8):2078–2085, August 2008. ISSN 1557-9646. doi: 10.1109/ted.2008.926593.

[28] Xiaolin Li, Guangyu Zhang, Xuedong Bai, Xiaoming Sun, Xinran Wang, Enge Wang, and Hongjie Dai. Highly conducting graphene sheets and langmuir–blodgett films. *Nature Nanotechnology*, 3(9):538–542, August 2008. ISSN 1748-3395. doi: 10.1038/nnano.2008.210.

[29] Frank Schwierz. Graphene transistors. *Nature Nanotechnology*, 5(7):487–496, May 2010. ISSN 1748-3395. doi: 10.1038/nnano.2010.89.

[30] Yanqing Wu, Yu-ming Lin, Ageeth A. Bol, Keith A. Jenkins, Fengnian Xia, Damon B. Farmer, Yu Zhu, and Phaedon Avouris. High-frequency, scaled graphene transistors on diamond-like carbon. *Nature*, 472(7341):74–78, April 2011. ISSN 1476-4687. doi: 10.1038/nature09979.

[31] Yu-Ming Lin, Keith A. Jenkins, Alberto Valdes-Garcia, Joshua P. Small, Damon B. Farmer, and Phaedon Avouris. Operation of graphene transistors at gigahertz frequencies. *Nano Letters*, 9(1):422–426, January 2009. ISSN 1530-6992. doi: 10.1021/nl803316h.

[32] Masa Ishigami, J. H. Chen, W. G. Cullen, M. S. Fuhrer, and E. D. Williams. Atomic structure of graphene on sio2. *Nano Letters*, 7(6):1643–1648, May 2007. ISSN 1530-6992. doi: 10.1021/nl070613a.

[33] Elena Stolyarova, Kwang Taeg Rim, Sunmin Ryu, Janina Maultzsch, Philip Kim, Louis E. Brus, Tony F. Heinz, Mark S. Hybertsen, and George W. Flynn. High-resolution scanning tunneling microscopy imaging of mesoscopic graphene sheets on an insulating surface. *Proceedings of the National Academy of Sciences*, 104(22):9209–9212, May 2007. ISSN 1091-6490. doi: 10.1073/pnas.0703337104.

[34] Katsuhiro Takahashi, Kazuki Yamada, Hiroki Kato, Hiroki Hibino, and Yoshikazu Homma. In situ scanning electron microscopy of graphene growth on polycrystalline ni substrate. *Surface Science*, 606(7–8):728–732, April 2012. ISSN 0039-6028. doi: 10.1016/j.susc.2011.12.009.

[35] E. H. Hwang, S. Adam, and S. Das Sarma. Carrier transport in two-dimensional graphene layers. *Physical Review Letters*, 98(18):186806, May 2007. ISSN 1079-7114. doi: 10.1103/physrevlett.98.186806.

[36] J.-H. Chen, C. Jang, S. Adam, M. S. Fuhrer, E. D. Williams, and M. Ishigami. Charged-impurity scattering in graphene. *Nature Physics*, 4(5):377–381, April 2008. ISSN 1745-2481. doi: 10.1038/nphys935.

[37] Kristen Kaasbjerg, Kristian S. Thygesen, and Karsten W. Jacobsen. Unraveling the acoustic electron-phonon interaction in graphene. *Physical Review B*, 85(16):165440, April 2012. ISSN 1550-235X. doi: 10.1103/physrevb.85.165440.

[38] S. Fratini and F. Guinea. Substrate-limited electron dynamics in graphene. *Physical Review B*, 77(19):195415, May 2008. ISSN 1550-235X. doi: 10.1103/physrevb.77.195415.

[39] Shaffique Adam, E. H. Hwang, V. M. Galitski, and S. Das Sarma. A self-consistent theory for graphene transport. *Proceedings of the National Academy of Sciences*, 104 (47):18392–18397, November 2007. ISSN 1091-6490. doi: 10.1073/pnas.0704772104.

[40] Enrico Rossi, S. Adam, and S. Das Sarma. Effective medium theory for disordered two-dimensional graphene. *Physical Review B*, 79(24):245423, June 2009. ISSN 1550-235X. doi: 10.1103/physrevb.79.245423.

[41] J. Martin, N. Akerman, G. Ulbricht, T. Lohmann, J. H. Smet, K. von Klitzing, and A. Yacoby. Observation of electron–hole puddles in graphene using a scanning single-electron transistor. *Nature Physics*, 4(2):144–148, November 2007. ISSN 1745-2481. doi: 10.1038/nphys781.

[42] Marco Gibertini, Andrea Tomadin, Marco Polini, A. Fasolino, and M. I. Katsnelson. Electron density distribution and screening in rippled graphene sheets. *Physical Review B*, 81(12):125437, March 2010. ISSN 1550-235X. doi: 10.1103/physrevb.81.125437.

[43] P. Partovi-Azar, N. Nafari, and M. Reza Rahimi Tabar. Interplay between geometrical structure and electronic properties in rippled free-standing graphene. *Physical Review B*, 83(16):165434, April 2011. ISSN 1550-235X. doi: 10.1103/physrevb.83.165434.

[44] Xu Du, Ivan Skachko, Anthony Barker, and Eva Y. Andrei. Approaching ballistic transport in suspended graphene. *Nature Nanotechnology*, 3(8):491–495, July 2008. ISSN 1748-3395. doi: 10.1038/nnano.2008.199.

[45] K. I. Bolotin, K. J. Sikes, J. Hone, H. L. Stormer, and P. Kim. Temperature-dependent transport in suspended graphene. *Physical Review Letters*, 101(9):096802, August 2008. ISSN 1079-7114. doi: 10.1103/physrevlett.101.096802.

[46] Jian-Hao Chen, Chaun Jang, Shudong Xiao, Masa Ishigami, and Michael S. Fuhrer. Intrinsic and extrinsic performance limits of graphene devices on sio2. *Nature Nanotechnology*, 3(4):206–209, March 2008. ISSN 1748-3395. doi: 10.1038/nnano.2008.58.

[47] A. Van Der Ziel and E.R. Chenette. *Noise in Solid State Devices*, pages 313–383. Elsevier, 1978. doi: 10.1016/s0065-2539(08)60414-x.

[48] A. van der Ziel. Unified presentation of 1/f noise in electron devices: fundamental 1/f noise sources. *Proceedings of the IEEE*, 76(3):233–258, March 1988. ISSN 0018-9219. doi: 10.1109/5.4401.

[49] J. B. Johnson. Thermal agitation of electricity in conductors. *Physical Review*, 32(1): 97–109, July 1928. ISSN 0031-899X. doi: 10.1103/physrev.32.97.

[50] A. Der Ziel. Theory of shot noise in junction diodes and junction transistors. *Proceedings of the IRE*, 43(11):1639–1646, 1955. ISSN 0096-8390. doi: 10.1109/jrproc.1955.277990.

[51] G.W. Neudeck. High frequency shot noise in schottky barrier diodes. *Solid-State Electronics*, 13(9):1249–1256, September 1970. ISSN 0038-1101. doi: 10.1016/0038-1101(70)90022-5.

[52] L.D. Yau and Chih-Tang Sah. Theory and experiments of low-frequency generation-recombination noise in mos transistors. *IEEE Transactions on Electron Devices*, 16 (2):170–177, February 1969. ISSN 0018-9383. doi: 10.1109/t-ed.1969.16586.

[53] H. G. E. Beck and W. P. Spruit. 1/f noise in the variance of johnson noise. *Journal of Applied Physics*, 49(6):3384–3385, June 1978. ISSN 1089-7550. doi: 10.1063/1.325240.

[54] A. van der Ziel. Flicker noise in semiconductors: Not a true bulk effect. *Applied Physics Letters*, 33(10):883–884, November 1978. ISSN 1077-3118. doi: 10.1063/1.90201.

[55] K.K. Hung, P.K. Ko, C. Hu, and Y.C. Cheng. A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors. *IEEE Transactions on Electron Devices*, 37(3):654–665, March 1990. ISSN 0018-9383. doi: 10.1109/16.47770.

[56] P. Dutta and P. M. Horn. Low-frequency fluctuations in solids: 1/f noise. *Reviews of Modern Physics*, 53(3):497–516, July 1981. ISSN 0034-6861. doi: 10.1103/revmodphys.53.497.

[57] A. Van Der Ziel. *Flicker Noise in Electronic Devices*, pages 225–297. Elsevier, 1979. ISBN 9780120146499. doi: 10.1016/s0065-2539(08)60768-4.

[58] Alexander A. Balandin. Low-frequency 1/f noise in graphene devices. *Nature Nanotechnology*, 8(8):549–555, August 2013. ISSN 1748-3395. doi: 10.1038/nnano.2013.144.

[59] R. H. Kingston, editor. *Semiconductor Surface Physics*. University of Pennsylvania Press, Philadelphia, Pa., 2016. ISBN 9781512803051.

[60] F.N. Hooge. 1/f noise is no surface effect. *Physics Letters A*, 29(3):139–140, April 1969. ISSN 0375-9601. doi: 10.1016/0375-9601(69)90076-0.

[61] F N Hooge, T G M Kleinpenning, and L K J Vandamme. Experimental studies on 1/f noise. *Reports on Progress in Physics*, 44(5):479–532, May 1981. ISSN 1361-6633. doi: 10.1088/0034-4885/44/5/001.

[62] Guangyu Xu, Carlos M. Torres, Yuegang Zhang, Fei Liu, Emil B. Song, Minsheng Wang, Yi Zhou, Caifu Zeng, and Kang L. Wang. Effect of spatial charge inhomogeneity on 1/f noise behavior in graphene. *Nano Letters*, 10(9):3312–3317, August 2010. ISSN 1530-6992. doi: 10.1021/nl100985z.

[63] Maxim A. Stolyarov, Guanxiong Liu, Sergey L. Rumyantsev, Michael Shur, and Alexander A. Balandin. Suppression of 1/f noise in near-ballistic h-bn-graphene-h-bn heterostructure field-effect transistors. *Applied Physics Letters*, 107(2), July 2015. ISSN 1077-3118. doi: 10.1063/1.4926872.

[64] Yu-Ming Lin and Phaedon Avouris. Strong suppression of electrical noise in bilayer graphene nanodevices. *Nano Letters*, 8(8):2119–2125, February 2008. ISSN 1530-6992. doi: 10.1021/nl080241l.

[65] Qinghui Shao, Guanxiong Liu, D. Teweldebrhan, A.A. Balandin, S. Rumyantsev, M.S. Shur, and Dong Yan. Flicker noise in bilayer graphene transistors. *IEEE Electron Device Letters*, 30(3):288–290, March 2009. ISSN 1558-0563. doi: 10.1109/led.2008.2011929.

[66] Atindra Nath Pal, Subhamoy Ghatak, Vidya Kochat, E. S. Sneha, Arjun Sampathkumar, Srinivasan Raghavan, and Arindam Ghosh. Microscopic mechanism of 1/f noise in graphene: Role of energy band dispersion. *ACS Nano*, 5(3):2075–2081, February 2011. ISSN 1936-086X. doi: 10.1021/nn103273n.

[67] Yan Zhang, Emilio E. Mendez, and Xu Du. Mobility-dependent low-frequency noise in graphene field-effect transistors. *ACS Nano*, 5(10):8124–8130, September 2011. ISSN 1936-086X. doi: 10.1021/nn202749z.

[68] Guanxiong Liu, Sergey Rumyantsev, Michael S. Shur, and Alexander A. Balandin. Origin of 1/f noise in graphene multilayers: Surface vs. volume. *Applied Physics Letters*, 102(9):093111, March 2013. ISSN 1077-3118. doi: 10.1063/1.4794843.

[69] Saloni Kakkar, Paritosh Karnatak, Md. Ali Aamir, Kenji Watanabe, Takashi Taniguchi, and Arindam Ghosh. Optimal architecture for ultralow noise graphene transistors at room temperature. *Nanoscale*, 12(34):17762–17768, 2020. ISSN 2040-3372. doi: 10.1039/d0nr03448g.

[70] Chandan Kumar, Manabendra Kuiri, Jeil Jung, Tanmoy Das, and Anindya Das. Tunability of 1/f noise at multiple dirac cones in hbn encapsulated graphene devices. *Nano Letters*, 16(2):1042–1049, January 2016. ISSN 1530-6992. doi: 10.1021/acs.nanolett.5b04116.

[71] Yuan Huang, Eli Sutter, Norman N. Shi, Jiabao Zheng, Tianzhong Yang, Dirk Englund, Hong-Jun Gao, and Peter Sutter. Reliable exfoliation of large-area high-quality flakes of graphene and other two-dimensional materials. *ACS Nano*, 9(11):10612–10620, September 2015. ISSN 1936-086X. doi: 10.1021/acsnano.5b04258.

[72] P. Blake, E. W. Hill, A. H. Castro Neto, K. S. Novoselov, D. Jiang, R. Yang, T. J. Booth, and A. K. Geim. Making graphene visible. *Applied Physics Letters*, 91(6), August 2007. ISSN 1077-3118. doi: 10.1063/1.2768624.

[73] T.B. Hoffman, B. Clubine, Y. Zhang, K. Snow, and J.H. Edgar. Optimization of ni–cr flux growth for hexagonal boron nitride single crystals. *Journal of Crystal Growth*, 393:114–118, May 2014. ISSN 0022-0248. doi: 10.1016/j.jcrysgro.2013.09.030.

[74] Aroop K. Behera, Charles Thomas Harris, Douglas V. Pete, Collin J. Delker, Per Erik Vullum, Marta B. Muniz, Ozhan Koybasi, Takashi Taniguchi, Kenji Watanabe, Branson D. Belle, and Suprem R. Das. High-performance and ultralow-noise two-dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. *ACS Applied Electronic Materials*, 3(9):4126–4134, September 2021. ISSN 2637-6113. doi: 10.1021/acsaelm.1c00595.

[75] Andres Castellanos-Gomez, Michele Buscema, Rianda Molenaar, Vibhor Singh, Laurens Janssen, Herre S J van der Zant, and Gary A Steele. Deterministic transfer of two-dimensional materials by all-dry viscoelastic stamping. *2D Materials*, 1(1):011002, April 2014. ISSN 2053-1583. doi: 10.1088/2053-1583/1/1/011002.

[76] Aroop K. Behera, C. Thomas Harris, Douglas V. Pete, Christopher M. Smyth, Marta B. Muniz, Ozhan Koybasi, Takashi Taniguchi, Kenji Watanabe, Branson D.

Belle, and Suprem R. Das. Charge-inhomogeneity-mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. *ACS Applied Nano Materials*, 7(11):12366–12375, May 2024. ISSN 2574-0970. doi: 10.1021/acsanm.4c00367.

[77] C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard, and J. Hone. Boron nitride substrates for high-quality graphene electronics. *Nature Nanotechnology*, 5(10):722–726, August 2010. ISSN 1748-3395. doi: 10.1038/nnano.2010.172.

[78] Kei Kinoshita, Rai Moriya, Momoko Onodera, Yusai Wakafuji, Satoru Masubuchi, Kenji Watanabe, Takashi Taniguchi, and Tomoki Machida. Dry release transfer of graphene and few-layer h-bn by utilizing thermoplasticity of polypropylene carbonate. *npj 2D Materials and Applications*, 3(1), May 2019. ISSN 2397-7132. doi: 10.1038/s41699-019-0104-8.

[79] D. G. Purdie, N. M. Pugno, T. Taniguchi, K. Watanabe, A. C. Ferrari, and A. Lombardo. Cleaning interfaces in layered materials heterostructures. *Nature Communications*, 9(1), December 2018. ISSN 2041-1723. doi: 10.1038/s41467-018-07558-3.

[80] Filippo Pizzocchero, Lene Gammelgaard, Bjarke S. Jessen, José M. Caridad, Lei Wang, James Hone, Peter Bøggild, and Timothy J. Booth. The hot pick-up technique for batch assembly of van der waals heterostructures. *Nature Communications*, 7(1), June 2016. ISSN 2041-1723. doi: 10.1038/ncomms11894.

[81] George B. Arfken, Hans-Jurgen Weber, and Frank E. Harris, editors. *Mathematical methods for physicists*. Academic, Oxford, 7. ed. edition, 2013. ISBN 9780123846549. Previous ed.: Amsterdam; London: Elsevier Academic, 2005. - Includes bibliographical references and index. - Description based on print version record.

[82] H. Nyquist. Certain topics in telegraph transmission theory. *Proceedings of the IEEE*, 90(2):280–305, 2002. ISSN 0018-9219. doi: 10.1109/5.989875.

[83] W. R. Bennett. Time division multiplex systems. *Bell System Technical Journal*, 20 (2):199–221, April 1941. ISSN 0005-8580. doi: 10.1002/j.1538-7305.1941.tb03601.x.

[84] C.E. Shannon. Communication in the presence of noise. *Proceedings of the IEEE*, 86 (2):447–457, February 1998. ISSN 1558-2256. doi: 10.1109/jproc.1998.659497.

[85] Robert J. Marks. *Introduction to Shannon Sampling and Interpolation Theory*. Springer New York, 1991. ISBN 9781461397083. doi: 10.1007/978-1-4613-9708-3.

[86] C. Barone, A. Galdi, S. Pagano, O. Quaranta, L. Méchin, J.-M. Routoure, and P. Perna. Experimental technique for reducing contact and background noise in voltage spectral density measurements. *Review of Scientific Instruments*, 78(9), September 2007. ISSN 1089-7623. doi: 10.1063/1.2786271.

[87] S. Q. Wang and G. D. Mahan. Electron scattering from surface excitations. *Physical Review B*, 6(12):4517–4524, December 1972. ISSN 0556-2805. doi: 10.1103/physrevb.6.4517.

[88] K. Hess and P. Vogl. Remote polar phonon scattering in silicon inversion layers. *Solid State Communications*, 30(12):797–799, June 1979. ISSN 0038-1098. doi: 10.1016/0038-1098(79)90051-6.

[89] Jürgen Schiefele, Fernando Sols, and Francisco Guinea. Temperature dependence of the conductivity of graphene on boron nitride. *Physical Review B*, 85(19):195420, May 2012. ISSN 1550-235X. doi: 10.1103/physrevb.85.195420.

[90] J. Serrano, A. Bosak, R. Arenal, M. Krisch, K. Watanabe, T. Taniguchi, H. Kanda, A. Rubio, and L. Wirtz. Vibrational properties of hexagonal boron nitride: Inelastic x-ray scattering andab initiocalculations. *Physical Review Letters*, 98(9):095503, March 2007. ISSN 1079-7114. doi: 10.1103/physrevlett.98.095503.

[91] Morteza Kayyalha and Yong P. Chen. Observation of reduced 1/f noise in graphene field effect transistors on boron nitride substrates. *Applied Physics Letters*, 107(11), September 2015. ISSN 1077-3118. doi: 10.1063/1.4930992.

[92] P. Dutta, P. Dimon, and P. M. Horn. Energy scales for noise processes in metals. *Physical Review Letters*, 43(9):646–649, August 1979. ISSN 0031-9007. doi: 10.1103/physrevlett.43.646.

[93] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi. Contact resistivity and current flow path at metal/graphene contact. *Applied Physics Letters*, 97(14), October 2010. ISSN 1077-3118. doi: 10.1063/1.3491804.

[94] Paritosh Karnatak, T. Phanindra Sai, Srijit Goswami, Subhamoy Ghatak, Sanjeev Kaushal, and Arindam Ghosh. Current crowding mediated large contact noise in graphene field-effect transistors. *Nature Communications*, 7(1), December 2016. ISSN 2041-1723. doi: 10.1038/ncomms13703.

[95] Youngseo Park, Hyoung Won Baac, Junseok Heo, and Geonwook Yoo. Thermally activated trap charges responsible for hysteresis in multilayer mos2 field-effect transistors. *Applied Physics Letters*, 108(8), February 2016. ISSN 1077-3118. doi: 10.1063/1.4942406.

[96] Ruge Quhe, Jiaxin Zheng, Guangfu Luo, Qihang Liu, Rui Qin, Jing Zhou, Dapeng Yu, Shigeru Nagase, Wai-Ning Mei, Zhengxiang Gao, and Jing Lu. Tunable and sizable band gap of single-layer graphene sandwiched between hexagonal boron nitride. *NPG Asia Materials*, 4(2):e6–e6, February 2012. ISSN 1884-4057. doi: 10.1038/am.2012.10.

[97] Manabu Itsumi. Electron trapping in thin films of thermal sio2 at temperatures between 30 and 300 k. *Journal of Applied Physics*, 54(4):1930–1936, April 1983. ISSN 1089-7550. doi: 10.1063/1.332247.

[98] V. S. Lysenko, T. K. Sytenko, V. I. Zimenko, I. P. Tyagulskii, and O. V. Snitko. Energy spectra of shallow traps in si-sio2 structures implanted with boron ions at various implantation energies. *Physica Status Solidi (a)*, 59(1):115–119, May 1980. ISSN 1521-396X. doi: 10.1002/pssa.2210590116.

[99] S Rumyantsev, G Liu, W Stillman, M Shur, and A A Balandin. Electrical and noise characteristics of graphene field-effect transistors: ambient effects, noise sources and physical mechanisms. *Journal of Physics: Condensed Matter*, 22(39):395302, September 2010. ISSN 1361-648X. doi: 10.1088/0953-8984/22/39/395302.

[100] Y.-W. Tan, Y. Zhang, K. Bolotin, Y. Zhao, S. Adam, E. H. Hwang, S. Das Sarma, H. L. Stormer, and P. Kim. Measurement of scattering rate and minimum conductivity in graphene. *Physical Review Letters*, 99(24):246803, December 2007. ISSN 1079-7114. doi: 10.1103/physrevlett.99.246803.

[101] Marco Gibertini, Andrea Tomadin, Francisco Guinea, Mikhail I. Katsnelson, and Marco Polini. Electron-hole puddles in the absence of charged impurities. *Physical Review B*, 85(20):201405, May 2012. ISSN 1550-235X. doi: 10.1103/physrevb.85.201405.

[102] Matthew Yankowitz, Jiamin Xue, and B J LeRoy. Graphene on hexagonal boron nitride. *Journal of Physics: Condensed Matter*, 26(30):303201, July 2014. ISSN 1361-648X. doi: 10.1088/0953-8984/26/30/303201.

[103] Jiamin Xue, Javier Sanchez-Yamagishi, Danny Bulmash, Philippe Jacquod, Aparna Deshpande, K. Watanabe, T. Taniguchi, Pablo Jarillo-Herrero, and Brian J. LeRoy. Scanning tunnelling microscopy and spectroscopy of ultra-flat graphene on hexagonal boron nitride. *Nature Materials*, 10(4):282–285, February 2011. ISSN 1476-4660. doi: 10.1038/nmat2968.

[104] L. K. J. Vandamme. How useful is hooge's empirical relation. In *2013 22nd International Conference on Noise and Fluctuations (ICNF)*. IEEE, June 2013. doi: 10.1109/icnf.2013.6578875.

[105] E. Burstein, A. L. McWhorter, P. H. Miller, D. T. Stevenson, and P. B. Weisz. *Semiconductor Surface Physics*. University of Pennsylvania Press, 1957. ISBN 9780812271133. URL http://www.jstor.org/stable/j.ctv512sg7.

[106] G. Ghibaudo, O. Roux, Ch. Nguyen-Duc, F. Balestra, and J. Brini. Improved analysis of low frequency noise in field-effect mos transistors. *Physica Status Solidi (a)*, 124(2): 571–581, April 1991. ISSN 1521-396X. doi: 10.1002/pssa.2211240225.

[107] Subhamoy Ghatak, Sumanta Mukherjee, Manish Jain, D. D. Sarma, and Arindam Ghosh. Microscopic origin of low frequency noise in mos2 field-effect transistors. *APL Materials*, 2(9), September 2014. ISSN 2166-532X. doi: 10.1063/1.4895955.

[108] T. Q. P. Vuong, S. Liu, A. Van der Lee, R. Cuscó, L. Artús, T. Michel, P. Valvin, J. H. Edgar, G. Cassabois, and B. Gil. Isotope engineering of van der waals interactions in hexagonal boron nitride. *Nature Materials*, 17(2):152–158, December 2017. ISSN 1476-4660. doi: 10.1038/nmat5048.

[109] Mingze He, Lucas Lindsay, Thomas E. Beechem, Thomas Folland, Joseph Matson, Kenji Watanabe, Andrey Zavalin, Akira Ueda, Warren. E. Collins, Takashi Taniguchi, and Joshua D. Caldwell. Phonon engineering of boron nitride via isotopic enrichment. *Journal of Materials Research*, 36(21):4394–4403, November 2021. ISSN 2044-5326. doi: 10.1557/s43578-021-00426-9.

[110] Alexandra Brasington, Song Liu, Takashi Taniguchi, Kenji Watanabe, James H. Edgar, Brian J. LeRoy, and Arvinder Sandhu. Phonon lifetimes in boron-isotope-enriched graphene- hexagonal boron nitride devices. *physica status solidi (RRL) – Rapid Research Letters*, 16(6), March 2022. ISSN 1862-6270. doi: 10.1002/pssr.202200030.

[111] Paul Zeiger, Jordan Hachtel, Dominik Legut, Eli Janzen, Juri Barthel, James H. Edgar, Leslie J. Allen, and Ján Rusz. Control of the phonon band gap with isotopes in hexagonal boron nitride, 2023.

[112] Ramon Cuscó, Luis Artús, James H. Edgar, Song Liu, Guillaume Cassabois, and Bernard Gil. Isotopic effects on phonon anharmonicity in layered van der waals crystals: Isotopically pure hexagonal boron nitride. *Physical Review B*, 97(15):155435, April 2018. ISSN 2469-9969. doi: 10.1103/physrevb.97.155435.

[113] Akash Laturia, Maarten L. Van de Put, and William G. Vandenberghe. Dielectric properties of hexagonal boron nitride and transition metal dichalcogenides: from monolayer to bulk. *npj 2D Materials and Applications*, 2(1), March 2018. ISSN 2397-7132. doi: 10.1038/s41699-018-0050-x.

[114] Massimo V. Fischetti, Deborah A. Neumayer, and Eduard A. Cartier. Effective electron mobility in si inversion layers in metal–oxide–semiconductor systems with a high-k insulator: The role of remote phonon scattering. *Journal of Applied Physics*, 90(9): 4587–4608, November 2001. ISSN 1089-7550. doi: 10.1063/1.1405826.

[115] Eran Bouchbinder and Edan Lerner. Universal disorder-induced broadening of phonon bands: from disordered lattices to glasses. *New Journal of Physics*, 20(7):073022, July 2018. ISSN 1367-2630. doi: 10.1088/1367-2630/aacef4.

[116] Fritz Körmann, Yuji Ikeda, Blazej Grabowski, and Marcel H. F. Sluiter. Phonon broadening in high entropy alloys. *npj Computational Materials*, 3(1), September 2017. ISSN 2057-3960. doi: 10.1038/s41524-017-0037-8.

[117] Ramon Cuscó, Bernard Gil, Guillaume Cassabois, and Luis Artús. Temperature dependence of raman-active phonons and anharmonic interactions in layered hexagonal bn. *Physical Review B*, 94(15):155435, October 2016. ISSN 2469-9969. doi: 10.1103/physrevb.94.155435.

Appendix A

Recipe for micromechanichal exfoliation

The wafers are first cleaned with high pressure (≈50psi) acetone spray to physically remove any organic residues from the surface. An O_2 plasma treatment of 2000W is followed for 10 minutes to remove any remaining organic traces. A blue SPV-224 Nitto tape is used instead of commercially available 3M scotch tape in the exfoliation process due to significantly lower organics on the sticky side of the tape. The process begins by placing a bulk crystal of graphite or hBN on the tape as shown in Fig. 2.1 (a). The crystal is then attached and detached to the opposite end of the tape to create a distribution of graphite on the tape as shown in Fig. 2.1(b). This distribution of graphite flakes are then attached to the clean wafer and placed on a hot plate at 110°C for 2 minutes as shown in Fig. 2.1(c). The wafer along with the tape is then taken out of the hot plate and the tape is then slowly peeled off from the surface of the wafer (Fig. 2.1(d)). The wafer is then inspected under an optical microscope to identify single layers graphene or few layers of hBN as shown in Fig. 2.1(e,f).

Appendix B

Recipe for Photolithography

The above mentioned alignment marks on the wafer of choice were fabricated by using photolithography processes. This process can be performed either before on clean wafer or once samples have been exfoliated onto target substrate. In this study, we choose to fabricate the alignment marks on substrates before exfoliation to reduce exposing the target sample to undesired polymers and organic solvents. During these processes, the wafers were spin coated with AZ5214E photoresist commerially available from MICROCHEM and heated on a hotplate at 110°C for 90 seconds. A maskless aligner (HEIDELBERG MLA150) was used to expose the wafer to a 405nm laser (165 mJ/cm^2 exposure) and developed in AZ400K 1:4 developer to pattern the alignment marks into the photoresist. Two thin metal layers of titanium (5nm) and gold (50nm) were deposited on the wafer by using a electron-beam metal evaporator (TEMESCAL FC2000) . Finally the wafer is plaed in acetone solution for 3 hours to perform the liftoff process where the remaining AZ5214E is removed from the wafer leaving the alignment marks made of Ti/Au layers behind. Due to the high throughput of MLA150, the photolithography process was performd on 4" wafers and later diced using a dicing saw into 12.5mm $\times$ 12.5mm pieces for further processing.

Appendix C

Heterostructure assembly procedure

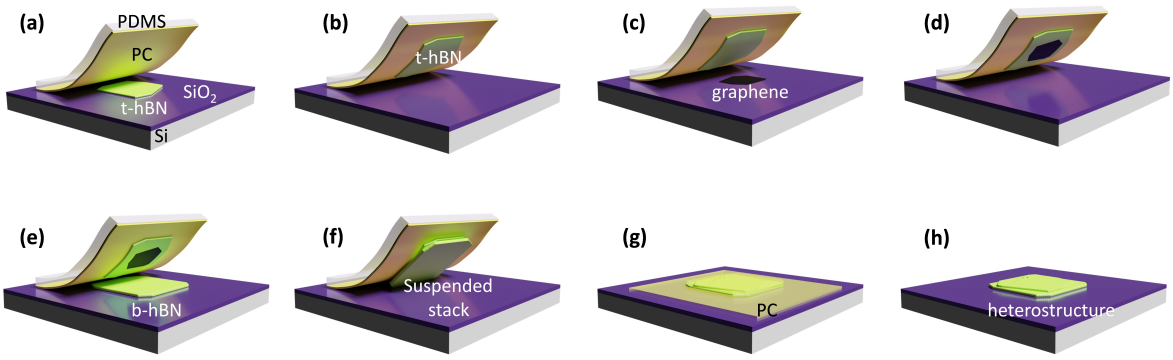


Figure C.1: *Schematic of the process flow for assembling an hBN/graphene/hBN heterostructure. (a) The PC/PDMS polymer stack is brought in contact to the encapsulating top hBN (t-hBN). (b) The polymer stack is lifted to detach the t-hBN from the wafer surface. (c) The t-hBN on polymer is aligned and attached to the required graphene flake on it's respective wafer. (d) The t-hBN/graphene stack is lifted from the wafer surface. (e) The t-hBN/graphene are aligned and attached to bottom hBN (b-hBN) and (f) The total heterostructure is lifted. (g) The hetero-structure is attached to a clean wafer and the PC is melted at 200° C onto the surface of the wafer. (h) PC is dissolved away to complete hetero-structure assembly on the wafer.*

The required 2D material flakes are exfoliated on separate Si/SiO_2 substrates as per mechanical exfoliation technique. The objective of heterostruccture assembly is to lift the target 2D flake from the substrate without creating any mechanical defect in the structure followed by aligning and placing the flake on another pre-identified 2D flake or target substrate. The end product in the procedure is to assemble a 2D heterostructure where graphene is encap-

sulated within two few layers of hBN flakes. The detailed process flow for assembling the 2D materials is given in Fig. C.1. First, a 5% solution of Polycarbonate (PC) in chloroform is prepared by stirring PC palettes in chloroform for 8 hours. A few drops of the solution is then placed on a clean glass slide and a separate glass slide is used to smear the solution on the surface of the slide. A square shaped piece of PC is cut out from the slide and placed on a PDMS film (GELPAK 4) of a similar shape. The PDMS/PC film is attached to a fresh glass slide and is loaded onto the slide holder in the 2D material transfer stage. A picture of the the transfer station is shown on Fig. C.2 with important components labeled.

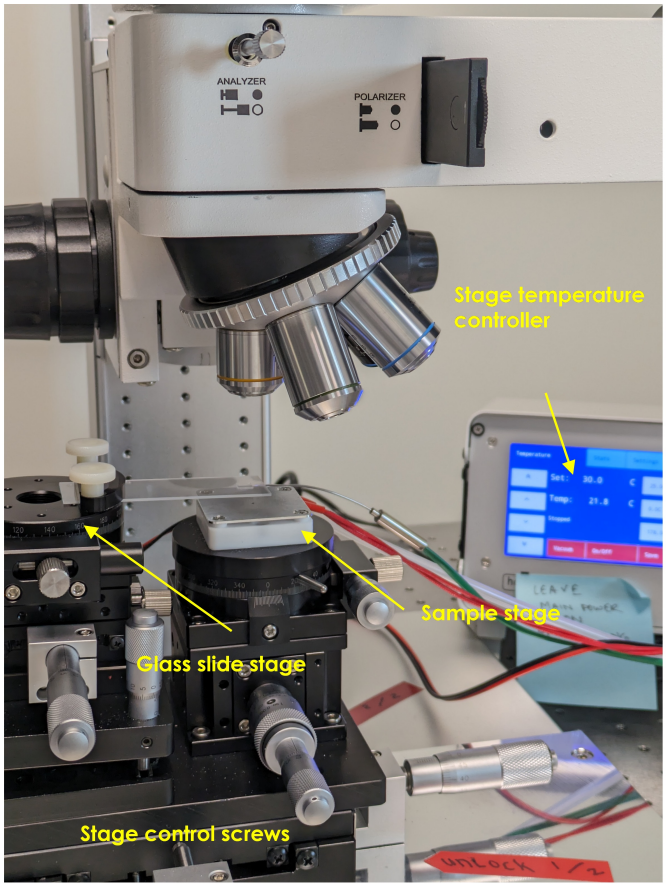


Figure C.2: *2D material transfer station with long working distance objective lenses.*

The substrate containing the top hBN flake is placed on the sample stage. By using the long working distance objectives in the microscope and the micrometer screws the PC/PDMS polymer stack is aligned to the target flake. The stage is then raised using the micrometer screws to bring the flake into contact with PC (see Fig. C.1(a)). The temperature of the

stage is then raised to 50°C and the sample stage is lowered. This makes hBN stick to PC and is removed from the Si/SiO_2 substrate (see Fig. C.1(b)). A similar 2D material lifting technique is repeated for picking graphene and the bottom hBN subsequently as shown in Fig. C.1 (c-f). This lifting technique uses the strong van der Waal's interaction between the 2D materials to lift the requisite 2D materials on top of one another to make the 2D stack suspended using PC as the adhesive polymer (see Fig. C.1(f)). The sample stage is then replaced with a fresh substrate with alignment markers and raised for the hetero-structure suspended with PDMS/PC to make contact with the substrate. The temperature of the stage is then increased to 200°C to melt the PC onto the substrate. ow by lowering the sample stage, PDMS is lifted away while the heterostructure with PC are left behind on the substrate (see Fig. C.1(g)). Finally the sample is soaked in Chloroform for 1 hour to dissolve the PC layer, completing the heterostructure assembly of the required 2D materials (see Fig. C.1(h)).

Appendix D

Electron beam lithography and reactive ion etching process

The samples were first spin coated at 3000 rpm for 30 seconds with PMMA 495K A3 followed by placing the sample on a hotplate set to 150°C for 5 minutes. The sample was the brought to room temp temperature and another layer of PMMA 950K A3 was spin coated at 3000 rpm. The sample was placed on a hotplate for 5 minutes at 150C. Electron beam lithography was used to pattern the sample at an electron beam dosage of 400 μC/cm^2. The sample was then developed in MIBK:IPA 1:4 for 60 seconds followed by a soaking in isopropanol (IPA) for another 60 seconds. The sample was inspected under an optical microscope to identify the developed region intended for etching.

A capacitively coupled plasma etcher or reactive ion etching (RIE) tool (OXFORD INSTRUMENTS PlasmaPro80) was used to etch the developed region. The gas composition used for the etching of the heterostructure was CHF_3 at 80 sccm, O_2 at 12.5 sccm, and CF_4 at 40 sccm. The plasma power was set to 130W. The etch rate determined for the process was 30 nm/minute. Depending the total thickness of the heterostructure, the plasma process was run between 1-2 minutes. The samples were then investigated under an optical microscope to confirm the removal of heterostructure in the developed region. If the heterostructure is not etched completely the process is repeated again to etch the material.

Appendix E

Metallization

The metal deposition step on the samples were performed by using a TEMESCAL FC2000 electron beam metal evaporator. The samples were loaded into the vacuum chamber and the chamber was pumped to high vaccum (5E-7 Torr) to reduce any impurities in the chamber to affect the metal deposition. In an ideal condition we want only gold to be used as the metal contact. However gold (Au) has poor adhesive strength when evaporated on a SiO_2 surface. If performed, the deposited gold can be easily peeled off by using a pair of tweezers or simply blown away by mouth. In order to avoid any harm to the fabricated contacts, generally a thin layer of adhesive metals like chromium or titanium are used to form an adhesive layer between SiO_2 and the contact metal. For our devices a 5 nm thick titanium was deposited at a rate of 0.5 Å/s which formed the adhesive layer. Without breaking the vacuum, an 85 nm thick gold layer was deposited at a rate of 1 Å/s to form the contact metal. It is important that the vacuum is not broken after deposition of titanium layer. This is because titanium is a very reactive metal, if exposed to atmosphere, titanium oxidizes rapidly to form TiO_2 thereby losing it's metallic properties. Therefore, even though titanium is a highly adhesive metal, can't be solely used as the contact metal and needs to be capped with an inert metal like Au.

Appendix F

Methods to reduce circuit and extrinsic noise

Extrinsic noise originating from circuitry and electro-magnetic radiations can hamper the noise and electrical signals being measured using the assembled apparatus.

1. Ground loops: Special attention must be taken to address multiple ground points in the electrical transport and low frequency noise. Multiple ground points in the circuit can lead to a potential difference between the grounding points. This small potential difference can lead to a small current flow or may act as antenna that can interfere with the measurements. This can be prevented by good circuit design.

2. Low pass RC filters: The low frequency noise measurements performed in this study are DC measurements where the DC signals were supplied through Keithley 2400 sourcemeters. Although they do a good job at sourcing the required potential and current values, however are very noisy in nature. This can be taken care of by inserting a low pass RC filter between the DUT and the sourcemeter to cut off any spurious noise from the sourcemeters. The cutoff filters used in this study had 3dB cutoffs at 0.3 Hz. Alternatively, a function generator can also be used in DC mode which has a noise output simmilar to that of a sourcemeter with a low pass filter.

3. Radiation shielding: The measured low frequency noise from the circuitry can be affected by nearby electromagnetic radiations. This can be prevented by electrically shielding the DUT and using twisted pairs as connecting wires to minimize electromagnetic flux through looped wires that interfere with the measured LFN.

4. Careful consideration of noise figures and electronic noise limits in all the electronics, (eg. sourcemeters, amplifiers, DMMs, spectrum analayzers etc.) must be made to operate the apparatus in the lowest noise configuration if possible. It must also be made sure that the noise measured from the DUT is higher than the noise floor of the entire apparatus.

Appendix G

Microscope images for graphene HFETs encapsulated within isotopically pure hBN

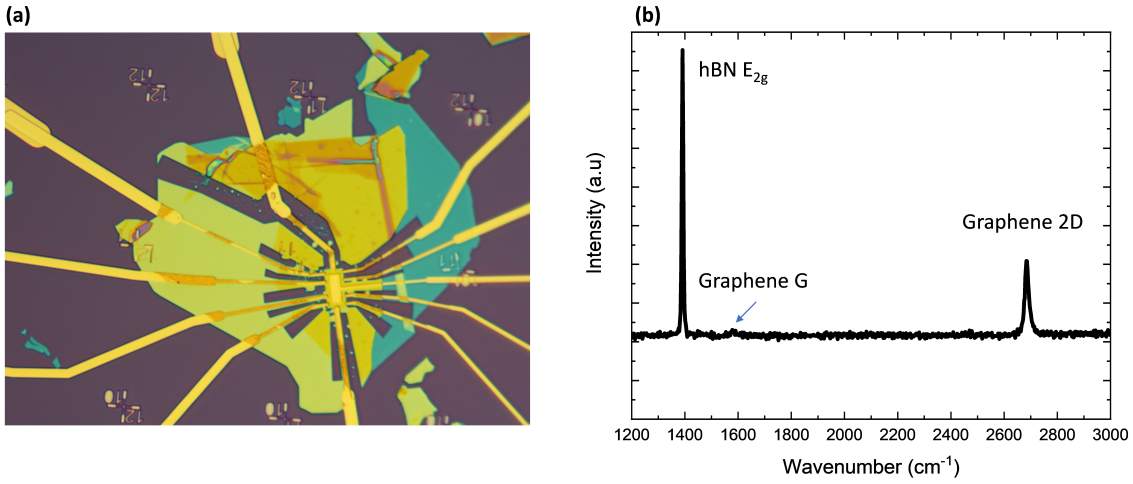


Figure G.1: *(a) Microscope image of the graphene HFET fabricated by encapsulation of graphene within $h^{10}BN$. (b) Raman spectrum of the assembled heterostructure displaying the hBN E_{2g}, graphene G and 2D bands.*

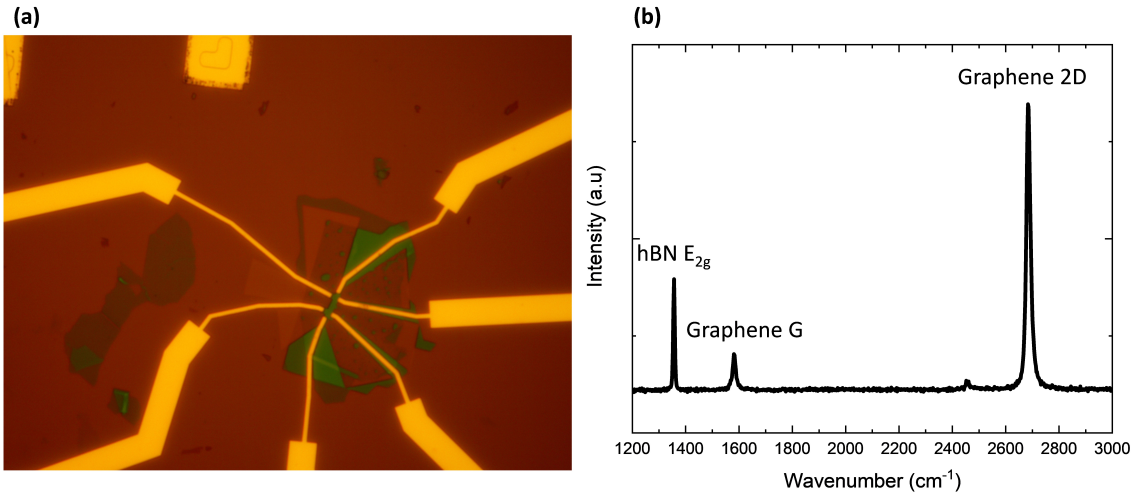


Figure G.2: *(a) Microscope image of the graphene HFET fabricated by encapsulation of graphene within h*[11]*BN. (b) Raman spectrum of the assembled heterostructure displaying the hBN* E_{2g}*, graphene G and 2D bands.*

Appendix H

Representative error analysis of I_{ds} vs V_g-V_{CNP} of 2D-HGFET device

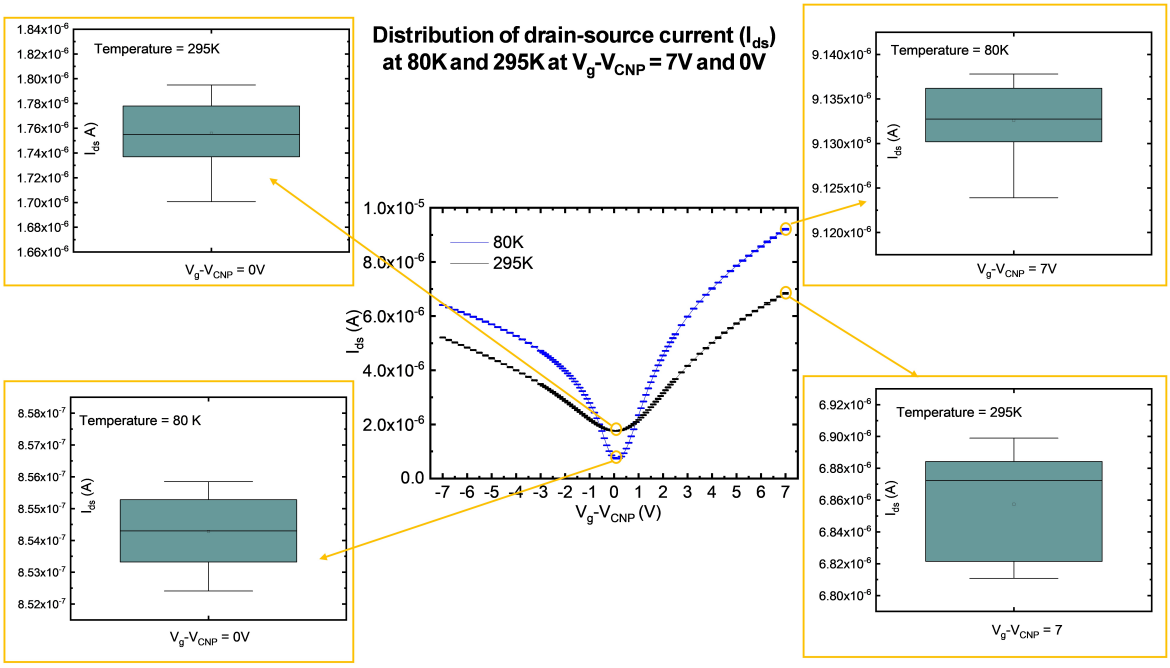


Figure H.1: *Error in measured I_{ds} in 2D-HGFET device at multiple gate overdrive voltages and temperatures.*

Appendix I

List of publications and presentations

I.1 Publications related to dissertation

1. Aroop K. Behera, Charles Thomas Harris, Douglas V. Pete, Collin J. Delker, Per Erik Vullum, Marta B. Muniz, Ozhan Koybasi, Takashi Taniguchi, Kenji Watanabe, Branson D. Belle, and Suprem R. Das. High-performance and ultralow-noise two-dimensional heterostructure field-effect transistors with one-dimensional electrical contacts. ACS Applied Electronic Materials, 3(9):4126–4134, September 2021. ISSN 2637-6113. doi: 10.1021/acsaelm.1c00595.

2. Aroop K. Behera, C. Thomas Harris, Douglas V. Pete, Christopher M. Smyth, Marta B. Muniz, Ozhan Koybasi, Takashi Taniguchi, Kenji Watanabe, Branson D. Belle, and Suprem R. Das. Charge inhomogeneity mediated low-frequency noise in one-dimensional edge-contacted graphene heterostructure field effect transistors. ACS Applied Nano Materials, 7(11):12366–12375, May 2024. ISSN 2574-0970. doi: 10.1021/acsanm.4c00367.

I.2 Additional publications

1. Aroop K. Behera, S. Chowdhury and Suprem R. Das. Magnetic skyrmions in atomic thin CrI_3 monolayer. Applied Physics Letters, 114: 232402, June 2019, ISSN 1077-3118. doi: 10.1063/1.5096782

I.3 KSURF (Kansas State University Research Foundation) disclosure and patent application

1. Suprem R. Das, Aroop K. Behera, James H. Edgar, C. Thomas Harris "Atomically Thin Two-dimensional Heterostructure Graphene Field Effect Transistors with Isotopically Pure and Natural Hexagonal Boron Nitride and One-dimensional Metal Contact Electrodes for Ultra-low Noise and High Mobility Applications". KSURF Disclosure (Notified on September 09, 2024)

I.4 Presentations related to dissertation

1. Aroop K. Behera, T M Lu, C. Thomas Harris, and Suprem R. Das, "Spin and Valley Hall Effects in MoS_2", CINT annual user meeting, Sandia National Laboratories, Santa Fe, NM, September, 2023

2. Aroop K. Behera, Ayaz Ali, C. Thomas Harris, Douglas V. Pete, Eli Janzen, Ozhan Koybasi, James H. Edgar, Branson D. Belle, and Suprem R. Das, "Graphene Heterostructure Field Effect Transistors encapsulated by Isotopically Pure Hexagonal Boron Nitride", MRS fall meeting 2022, Boston, MA, November, 2022

3. Aroop K. Behera, C. Thomas Harris, Douglas V. Pete, Collin J. Delker, Per Erik Vullum, Marta B. Muniz, Ozhan Koybasi, Takashi Taniguchi, Kenji Watanabe, Branson D. Belle, and Suprem R. Das, "Charge Inhomogeneity Mediated Low-Frequency Noise

in Encapsulated Graphene Field Effect Transistors", APS march meeting, Chicago, IL, March, 2022

4. Aroop K. Behera, C. Thomas Harris, Douglas V. Pete, Collin J. Delker, Per Erik Vullum, Marta B. Muniz, Ozhan Koybasi, Takashi Taniguchi, Kenji Watanabe, Branson D. Belle, and Suprem R. Das, "Transport and Noise Studies in One-Dimensional contacts to Two-Dimensional Heterostructure Graphene Devices", CINT annual user meeting, virtual, September, 2021

5. Aroop K. Behera, Sugata Chowdhury, and Suprem R. Das, "Skyrmions in Monolayer van der Waals 2D Magnets", APS march meeting, Boston, MA, March, 2019