A 10MHZ FLASH ANALOG-TO-DIGITAL CONVERTER SYSTEM FOR DIGITAL OSCILLOSCOPE AND SIGNAL PROCESSING APPLICATIONS

by

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ABSTRACT

The development of a 10MHz Flash Analog-to-Digital Converter system for digital oscilloscope and signal processing applications was investigated. The timing for the alternating method such that the digital word is stored consecutively in an alternate fashion in two slow (cheap) memories was simulated on the HP9845B computer. Then the circuit was built in the wire-wrap form. Two type of tests one static, the other dynamic were performed on the system to evaluate its performance. A second order low-pass active filter was used to reduce any noise coming into the system from the function generator. Test results indicated the alternating method worked as expected. Also, from the test results it was found out that at higher sampling frequencies system noise level increases and therefore degrading the performance of the FADC system.

CHAPTER-1

INTRODUCTION

The purpose of this thesis is to describe the development of a dual channel Flash Analog-to-Digital Converter (FADC) module with a maximum sampling rate of 10MHz. the FADC will be used in the instrumentation laboratory for Digital Oscilloscope and Signal Processing applications. Conventional instruments are normally in large boxes, are rack-mounted or consist of individual P.C. boards plugged into a motherboard . For example the Hewlett-Packard 6940B Multiprogrammer houses several hardware modules such as an Analog-to-Digital Converter, Voltage to Frequency Converter and a Voltage Controlled Oscillator apart from the relay cards and power supply unit. However, the cost of this system is in the $50,000 range.

The idea of developing an inexpensive system to perform the functions mentioned above, and also capable of connection to any personal computer via a single RS-232-C link, is an interesting one. Such an inexpensive system is referred to as a personal instrument. A personal instrument is any electronic measurement device that depends on a personal computer for control or data display. The personal instrument is an assortment of plug-in modules that link with a personal computer over an RS-232-C bus. The FADC module is one of such modules that is used as a 10MHz digital oscilloscope. Such a system with a variety of plug-in modules costs around $5000.

For test purposes the FADC module was built in the wirewrap form and interfaced to the Hewlett-Packard 9845B microcomputer via a 16-bit HPI/O interface bus. The block diagram for this Flash ADC module is shown in Fig 1.

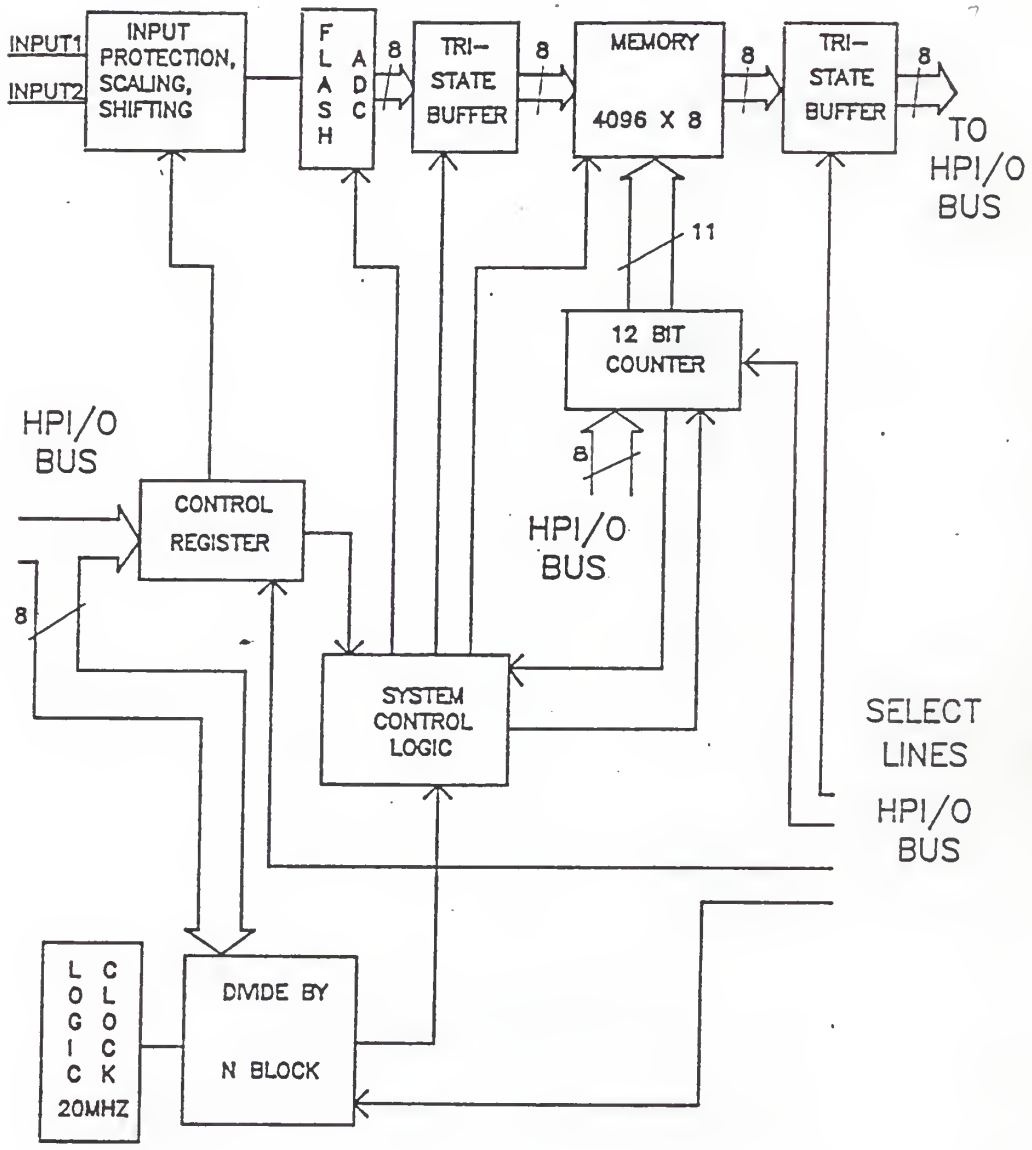


Fig. 1

BLOCK DIAGRAM FOR FLASH ADC MODULE

Analog input depending on the type of operation (single or dual channel) is fed into the front-end, where is conditioned, amplified, and shifted to the required level. Then, the analog signal is sampled by an 8-bit FADC at a fixed sampling frequency between 78KHz and 10MHz , and the resulting digital data is stored in 4096 byte of memory. The system control logic performs the Direct Memory Access (DMA) during the write mode. A 12-bit counter is clocked by the DMA controller which provides the 11-bit address lines to the memory. The upper HPI/O lines form the select lines to different components on the board. On command from the personal computer, data are read into a data file at a slower speed. Furthermore, through the use of computer processing and control, such functions as, Spectral Analysis, Signal Averaging, and Digital Filtering could be performed on the stored data, and the result could be displayed on the screen.

The advantage of such module is the ability to sample analog signals at sampling rates of up to 10MHz. Also, the cost($180) of such a module is much less than a similar one presently available in the market($800).

CHAPTER-2

THE FLASH ANALOG-TO-DIGITAL CONVERTER

2.1 CONVENTIONAL ANALOG-TO-DIGITAL CONVERSION

Analog-to-digital converters or ADCs are used to convert analog input data, usually voltages, into an equivalent digital form (a coded set of ONE/ZERO levels). Analog-to-digital conversion in its basic conceptual form is a two-step process: quantizing and coding. Quantization is the process of transforming an analog signal into a set of discrete output states. Coding is the process of assigning a digital code word to each of the output states. The non-linear transfer function shown in Fig. 2 is that of an ideal ADC with 8 output states.

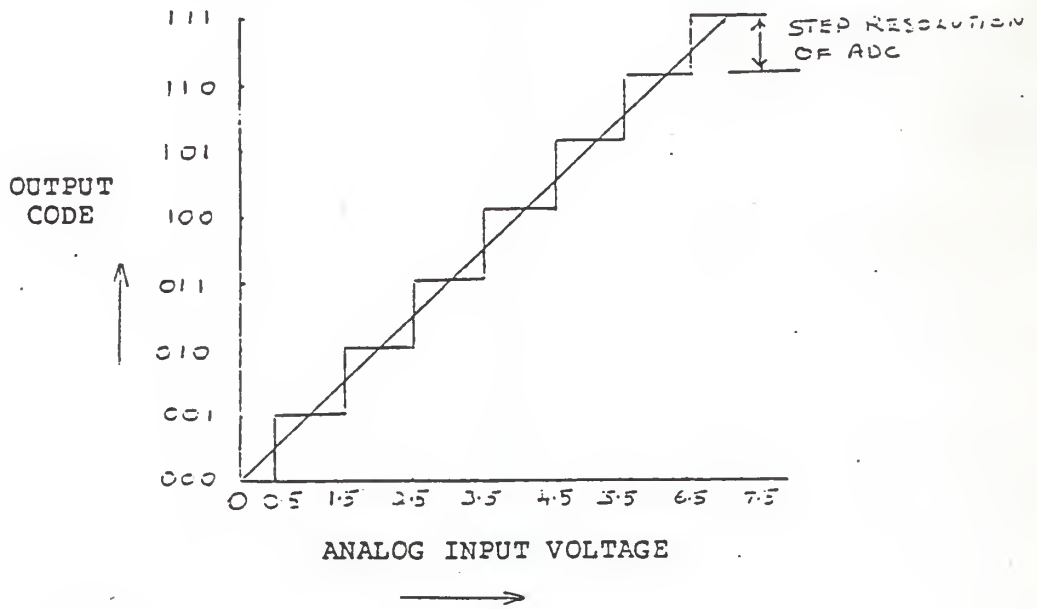


Fig. 2

TRANSFER FUNCTION OF A 3-BIT ADC

2.2 FLASH ANALOG TO DIGITAL CONVERTER

An analog-to-digital converter requires a small, but significant, amount of time to perform the quantizing and coding operations. Therefore, a sample and hold circuit is often used to perform the necessary function of holding the ADC input voltage fixed during quantization and coding. A sample and hold is simply an analog voltage-memory device in which an input voltage is acquired and then stored on a high quality capacitor.

Parallel, or Flash, encoding is the fastest method of converting analog information into digital form. Hence, FADCs do not require sample and hold circuits. A FADC is a very specialized analog-to-digital converter where the input analog voltage is simultaneously applied in parallel to a group of comparators . The analog input signal is applied in parallel to one of the inputs of each comparator while the other input obtains a precise reference voltage from a tap on a resistor network. Each reference voltage differs from the next by one least significant bit. Those with thresholds below the signal voltage turn on, while the others stay off. The outputs of all the comparators are applied to the decoding logic which yields the parallel output code. However, the number of bits could be increased for better resolution by connecting ADCs in tandem. For an 8 bit converter the number of comparators needed are 2**8-1=255 comparators. The block diagram for an 8 bit Flash ADC is shown in Fig. 3.

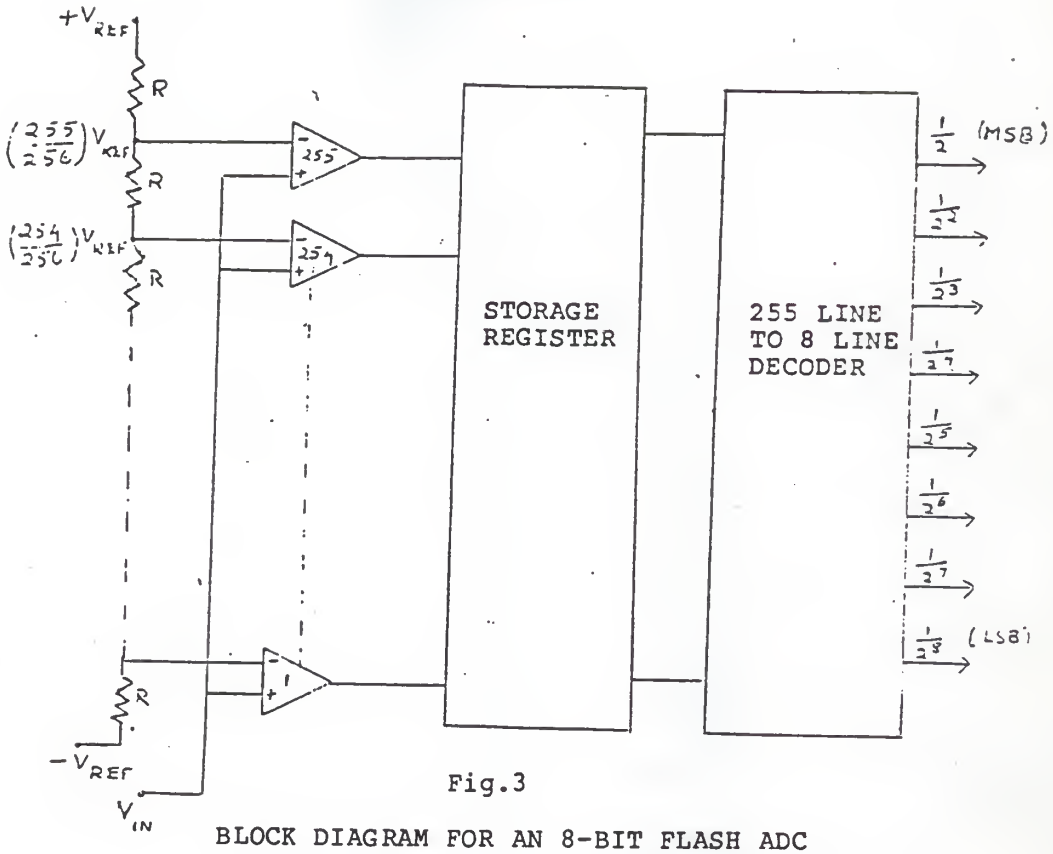


Fig.3

BLOCK DIAGRAM FOR AN 8-BIT FLASH ADC

The FADC used in this design is the TRW TDC1007, which is an 8 bit bipolar Flash ADC with a reference input voltage of 0.0 to -2.0 volts. Therefore, the analog input signal has to be in this range to prevent damage to Flash ADC. The digital word corresponding to an analog input signal is available at the output after two clock cycles. The voltage resolution that can be achieved with an 8 bit FADC using a 0.0 to -2.0 volts reference voltage, is (2.0/256)=7.84 mV and the quantization error is 3.9 mV.

Although the FADC can sample at a maximum sampling rate of 20MHz, due to unavailability of analog components that can handle such a bandwidth, it was decided to limit the maximum sampling rate at 10MHz. The conversion process is initiated by the CONV(CLOCK) signal to the ADC.

2.3 THE NEED FOR A FAST DATA ACQUISITION SYSTEM

With continued efforts in the high-frequency regions, the decreasing cost of converting data at 8-bit resolution has extended the use of digital techniques to a broad range of applications. FADCs are now used in video broadcasting and recording equipment, speedy oscilloscopes and waveform digitizers.

The FADC used in this study is the TRW TDC1007; an 8-bit, 20MHz converter. Presently, the TDC1007 is the only available 20MHz, 8-bit FADC from TRW . RCA manufactures another 8-bit FADC the RCA 41051 which has control similar to TDC1007. However, the present design was based on the TRW Flash because of its availability and superior specification sheets (documentation).

The design of the FADC module centers around the requirements for the FADC. The following are the considerations taken into account:

1) To digitize an analog signal at a maximum sampling rate of 10MHz.

2) To condition and shift the analog input signal within the reference voltage (0.0V to -2.0V).

3) To automatically set the range of the FADC with respect to the amplitude of the input signal, and to sample the signal at a frequency, specified by the user.

To sample at 10MHz, Direct Memory Access (DMA) control is required such that the digital word can be stored at such high speed in the on board RAMs. The DMA controller cicuitry provides the correct timing signals for the write(WE), the chip select(CS), and the address latch enables.

CHAPTER-3

ANALOG SECTION

3.1 ANALOG FRONT END

The purpose of the analog front end is to provide the scaling and input protection necessary to supply the FADC with valid analog input signals.

A schematic diagram of the analog front end is shown in Fig. 4; it consists of the following:

A. Attenuation and channel selection

B. Amplifier

C. Voltage Reference

D. Transistor Buffer

E. Input Protection

The following sections discuss in detail each of the above sections.

A. Attenuation and Channel Selection

The front end consists of two channels which allow conditioning of peak voltages of +40mV, +400mV, or +4V at 5MHz bandwidth. The channels are selected by closing S1 (channel A) or S2 (channel B). This is accomplished by applying a logic "0" in control bit 2 for channel A or a logic "1" for channel B. Switches S3, S4, and S5 provide attenuations of 1, 10, and 100 respectively. S3, S4, and S5 are controlled by bits 4,5, and 6 of the control register. All switches are open when a logic "1" is supplied and closed for logic "0". S1 through S5 are the ADG201 CMOS SPST high bandwidth switches which can handle voltages up to

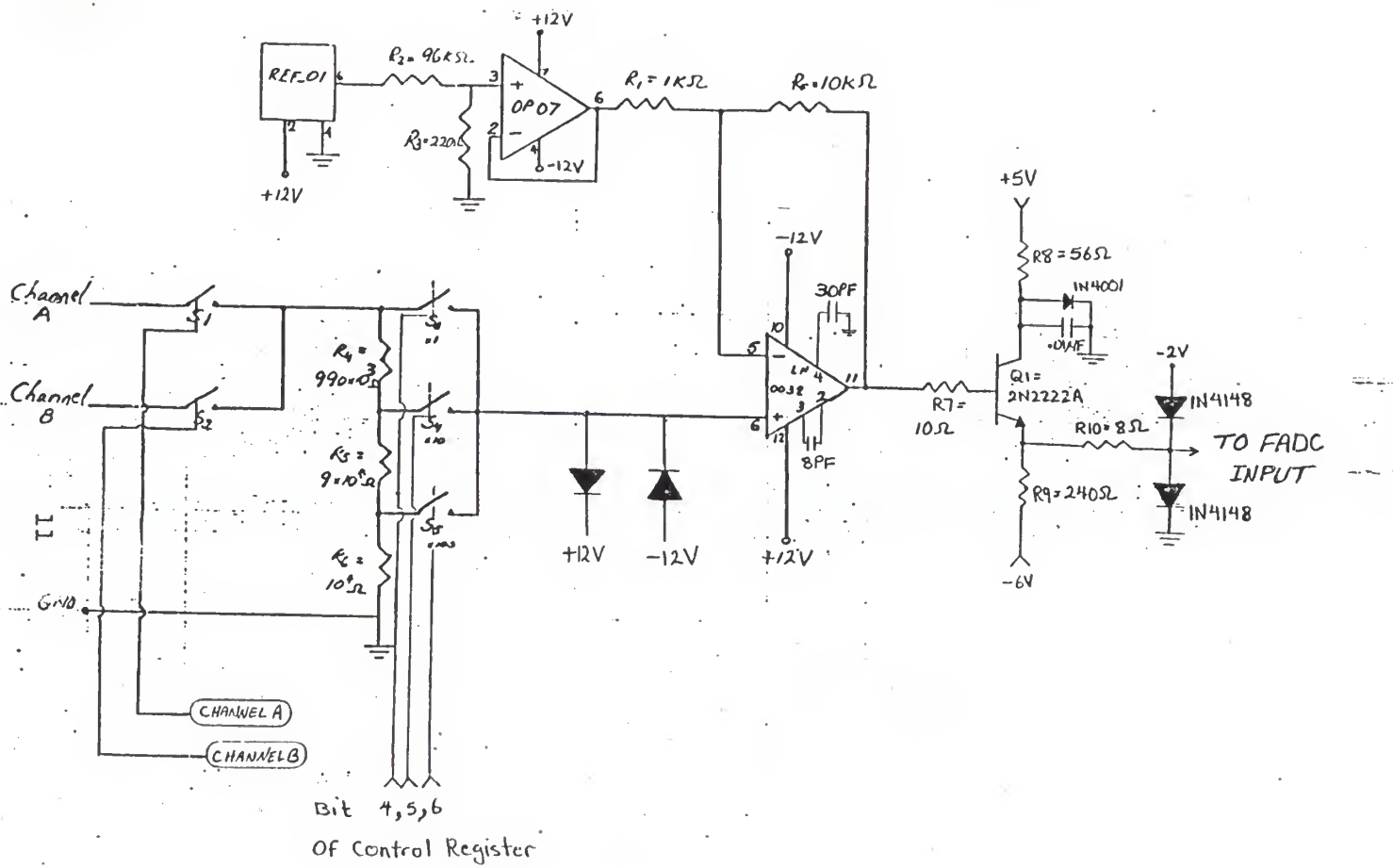


Fig. 4

Schematic Diagram of the Analog Front End

+37 V. Table 1 in Appendix A shows the various range settings available.

B. Amplifier

As the input signal is attenuated it is fed to the non-inverting input of the LH0032 ultra high speed amplifier. The input signal is amplified by the operational amplifier so that the amplifier output is between -2.0V and 0.0V. This is within the allowable analog input range of the FADC. Appendix B demonstrates the calculations for the resistors R1, R2, R3, and Rf.

The analog front end was built and tested by feeding sine-wave from the Hewlett-Packard 3325A Synthesizer/Function Generator. After running several tests by varying the input frequency and realizing that the cut-off frequency for the LH0032 according to the specifications for a gain of 32.2 (this is the calculated value) was 1MHz, it was decided to decrease the gain to increase the cut-off frequency to around 4MHz. Therefore a gain of 10 was chosen to achieve this. Accordingly the other resistor values had to be changed to do the required level shifting.

C. Voltage Reference

The REF_01 voltage reference (and associated circuitry) supplies 52mV to the non-inverting amplifier configuration to yield the necessary level shifting of the amplifiers output. A voltage divider is used to drop the +10 V output of the voltage reference to the required 52mV level. An AD OP_07 ultra low offset operational amplifier is used in conjunction with REF_01

to supply the necessary isolation for the voltage network R2 and R3.

D. Transistor Buffer

As the input signal to TDC1007 varies, the comparator input transistors change from active to cut-off, causing the net input resistance and capacitance to change. To prevent this action from degrading the integrity or accuracy of the output data, the output from the operational amplifier is followed with an NPN transistor buffer (2N2222A).

Test results indicated that by connecting the output from the operational amplifier directly to TDC 1007 input, input signals are distorted at frequencies greater than 200KHz. However, by adding the transistor buffer the input signal remained undistorted up to frequency of 4MHz.

E. Input Protection

To protect the input to the TDC 1007 as well as the LH0032 operational amplifier, the 1N4148 ultra high speed switching diodes are used to do the required protection by clamping the input signal, whenever the input voltage exceeds the allowable input levels.

3.2 REFERENCE VOLTAGE FOR TDC 1007

The TDC 1007 converts analog signals in the range Vrb < Vin < Vrt into digital form. Vrt (the voltage applied to the pin at the top of the reference resistor chain), and Vrb (the voltage applied to the pin at the bottom of the reference resistor chain) should be between 0.0V and -2.0V, with difference between them being less than 2.0V. In order to ensure optimum operation of TDC 1007, these points should be driven by low-impedance sources capable of providing the necessary reference resistor chain current.

The reference voltage circuitry shown in Fig. 5 is built to provide -2.0 volts at the bottom of the resistor chain. To meet the requirements, Vrb is driven with a PNP transistor-buffered operational amplifier. The transistor sinks the current flowing through the reference chain and keeps the driving impedance at the bottom end of the resistor chain low.

There are three power supply voltages (+5V, +12V, and -12V) available to the FADC module. TDC1007 operates from two supply voltages, +5.0V and -6.0V. The LM337 is a 3-terminal adjustable regulator used to provide -6.0V to the TDC1007 and other components on the board (see Fig. 6).

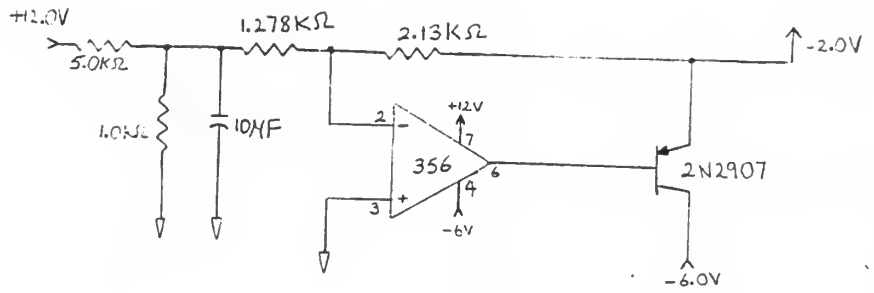


Fig. 5

Voltage Reference Circuitry

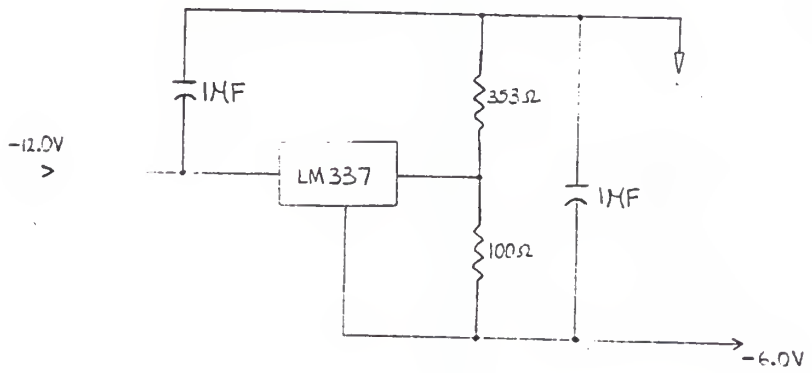


Fig. 6

LM337 3-Terminal Voltage Reference Configuration

CHAPTER-4

DIGITAL SECTION

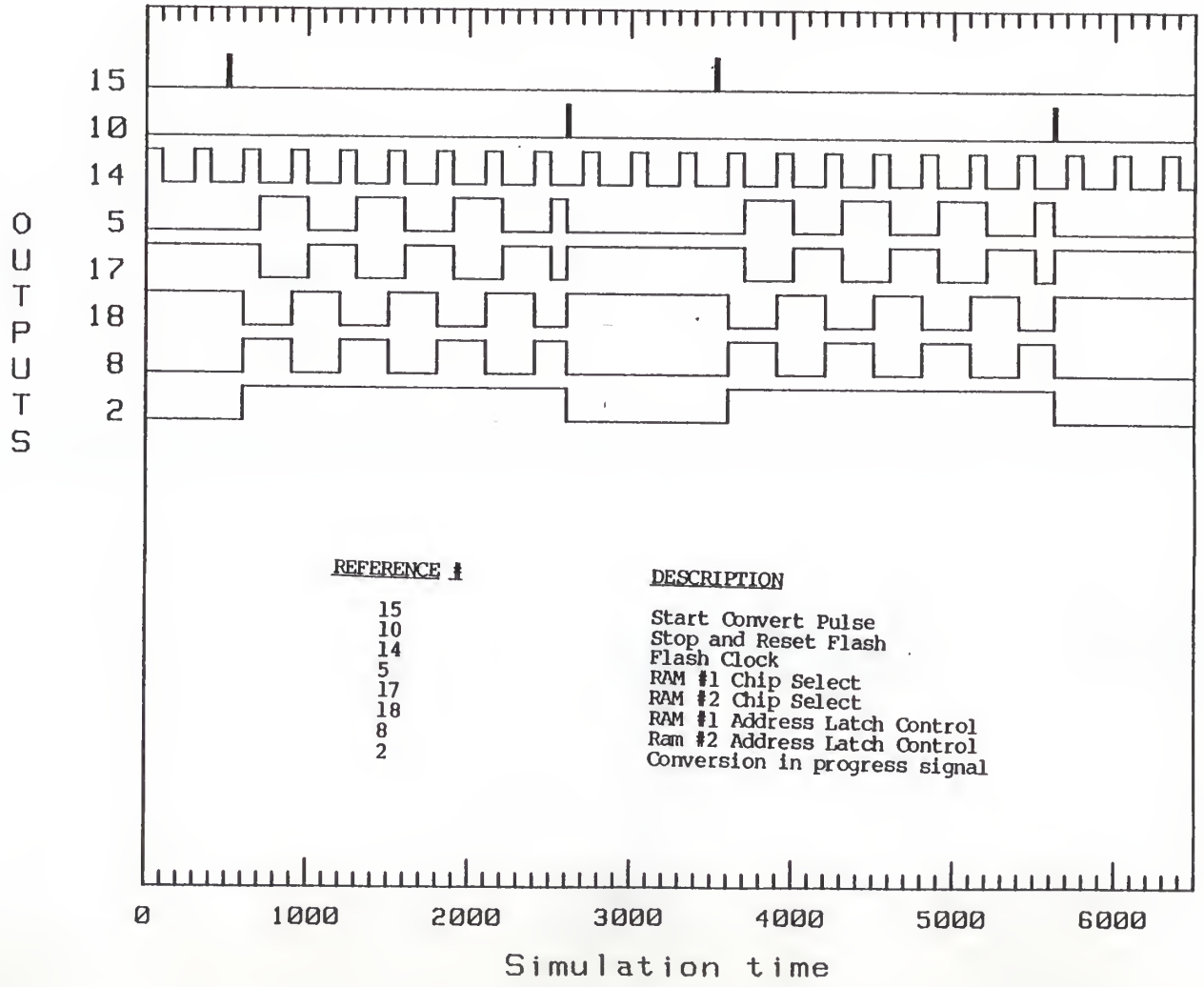
4.1 DIRECT MEMORY ACCESS CONTROLLER

The Direct Memory Access (DMA) controller is designed to control the FADC and memory elements at speeds (+10MHz) greater than those possible through the host microprocessor. This method is used widely in systems where the I/O device speed is much higher than the processor speed. For instance, the microcomputer executes instructions in 1 sec whereas the TDC1007 FADC has data available in 2 clock cycles (i.e. 200ns). Under program control data acquisition, the microcomputer would read only one out of 5 samples, thus defeating the purpose of using a FADC. Based on these considerations the DMA controller is used. The DMA controller is used only to write data from the FADC to memory. However, during the read mode, a select line (single step signal) from the microcomputer is used to read data at a slower speed from the on-board memory to a data file.

The DMA controller timing is based on the FADC clock so that the timing signals would appear the same (in a relative fashion) for any desired sampling rate.

For a sampling frequency of 10MHz (worst case), the required memory write pulse time is 50ns. Due to the unavailability of such memory, an alternating method is used to write data into two slower memories (HM6116LP2) and still accomplish the high speed data storage. In this manner, in one clock cycle data is written in the first memory and during the next clock cycle data

FIG. 7 DMA CONTROLLER TIMING DIAGRAM



is written into the second memory.

Fig. 7 is the timing diagram for the DMA controller simulated using the Digital Simulation package on the HP9845B. The numbers corresponding to each wave form are indicated in circles on the schematic diagram of Fig. 8.

Referring to the timing diagram and schematic of Fig. 8, the DMA is accomplished by four flip-flops, U1 and U2 (74LS74). The start convert pulse (reference # 15) to the DMA controller initiates the conversion and data storage process. To start the conversion process, a logic transition from a "0" to a "1" must be made through the control register bit 0 (U15).

Flip-flop #1 (FF #1) of U1 latches the start convert signal to FF #2 of U1. FF #2 is used to synchronize the system (i.e. to wait for a rising edge of the Flash clock before the conversion process starts). U2 consists of two flip-flops. FF #1 of U2 provide the chip select and write enable signals to RAM #2 and the inverse of this signal selects RAM #1 (reference numbers 17 and 5). FF #2 of U2 generates the address latch control for RAM #1 and its inverse for RAM #2 (reference numbers 8 and 18). From the timing diagram it can be noted that FF #1 operates on the falling edge of Flash clock, where as FF #2 operates on the rising edge.

Addresses to the memories are generated using three 4-bit binary counters cascaded together (U6, U7, and U8). The load input is controlled by a select line Sn+5 (n can be any number) from the microprocessor. As the desired number of conversions is

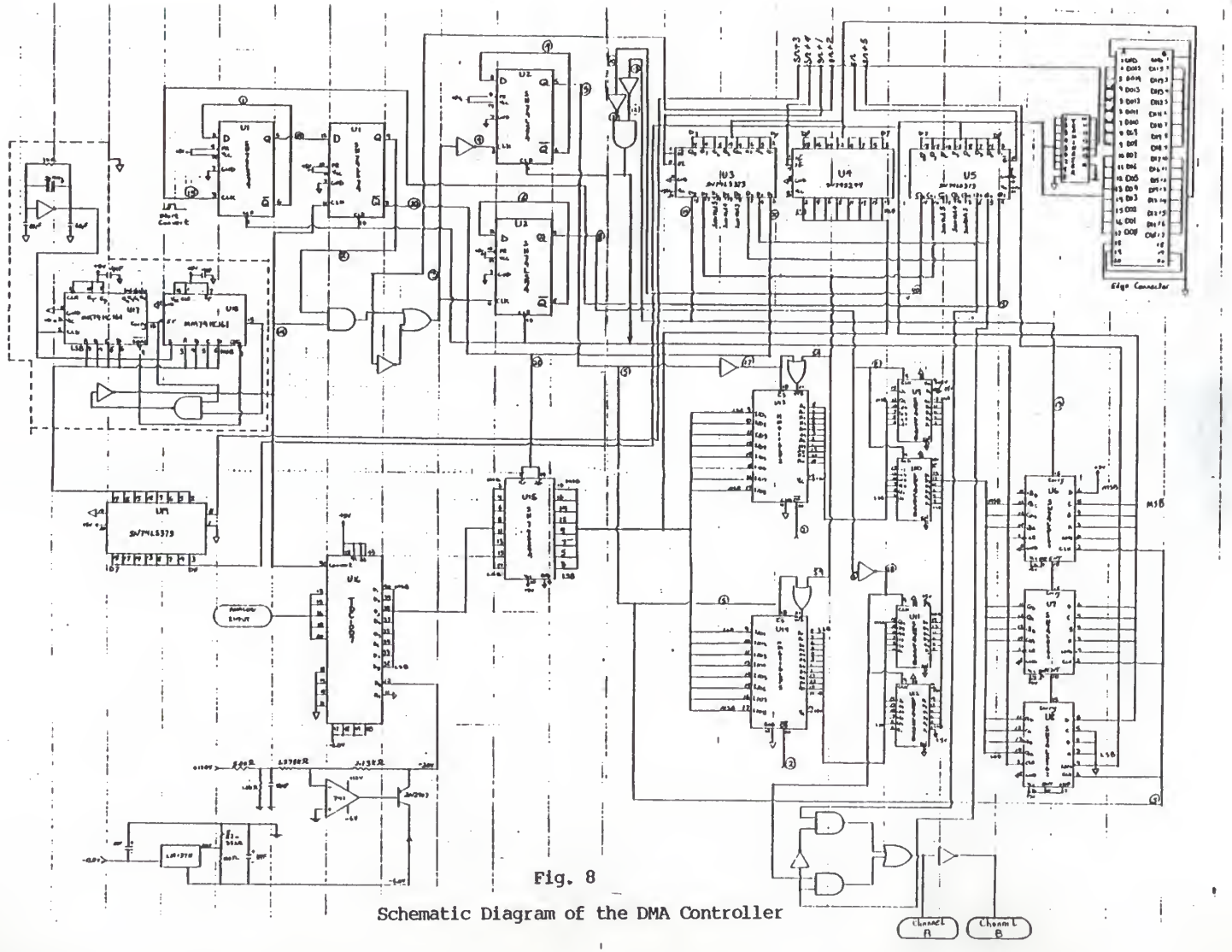


Fig. 8

Schematic Diagram of the DMA Controller

put on the data bus, a transition from a logic "1" to a logic "0" on the load pin, loads the number of A/D conversions into the registers of the 74LS161s. The clock to these counters is supplied by FF #1 of U2 (reference #5). On the rising edge of the clock the counters count up. The first stage of this three stage counter counts up to 15 (binary 1111) and outputs a pulse at the ripple carry output, which enables the second counter. The same process takes place for the second and third stages.

As the counters count up to all ones, the third stage puts out a pulse. This pulse is gated to the clear inputs of the DMA controller flip-flops, which in turn causes the conversion process to stop and reset the system (i.e. the desired number of A/D conversions has ended). Notice that there are eleven address lines necessary to address the RAMs. Therefore, the bottom 11 lines of the address counter lines are connected to the RAM address lines through the 74LS378 latches. To provide 11-bit address values from an 8-bit data value, the bottom three input pins of 74LS161s are tied low, whereas the MSB is tied high.

Table 4.2 depicts the 8-bit counter values and the number of A/D conversions made.

Table 4.2 COUNTER VALUES vs. A/D CONVERSIONS

COUNTER VALUE	A/D CONVERSIONS
0	4094 conversions
1	4078 conversions
2	4062 conversions
.	.
.	.
252	62 conversions
253	46 conversions
254	30 conversions
255	14 conversions

For a dual memory operation the number of A/D conversions based upon the 8-bit counter value is:

A/D Conversions =2[(255-counter value)*8+7]

In the above equation 2 is the two memory operation, 255 is the 2**8(i.e. from 0-255) maximum counter value, 7 is the number of memory spaces filled with the three LSBs of the counter tied low, and 8 is the LSB of the counter value.

Four 74LS378s (U9, U10, U11, and U12), latch the addresses from the counters to the RAMs alternately. Address latching is required to hold valid RAM addresses while the counters are incremented for the next valid address. U9 and U10 provide the 11-bit address lines for RAM #1 which are clocked from FF #2 of U2, while latches U11 and U12 provide address lines for RAM #2 clocked by the inverse signal of FF #2.

The data lines from the RAMs are connected to the internal data bus of the FADC module. The internal data bus is separated from the HPI/O bus through U4's tri-state buffers (74LS244). The control for U4 is through select line Sn+4. During read mode, select line Sn+4 is made low so that the internal data bus is connected to the HPI/O bus. Thus, during write mode U15 tri-state buffers are enabled (i.e. by signal reference #2 in table 4.1) to connect the FADC outputs to the internal data bus. Tri-state U15 is necessary so that the FADC outputs do not interfere with the data transfer from DMA memory to HP9845B during read mode. The write enable pin from the memories are controlled through control register bit 6. Control register bit 6 supplies a logic "0" for the write mode and a logic "1" for the read mode. The output enable pin (OE) is controlled by signal from reference #2 of table 4.1. This pin is high during write mode and low otherwise.

The FADC used is a TRW TDC1007 (U16) 20MHz, 8-bit converter. The TDC1007 has three major functional sections: a comparator array, encoding logic, and output data latches. The input voltage is compared with 255 separate reference voltage points tapped from the reference resistor chain. The analog input to the TDC1007 is sampled 10ns after the rising edge of the CONV(CLOCK) signal. This delay time is the sampling time offset. The output data is encoded from the 255 comparators on the falling edge of the CONV signal. The encoded result is transferred to the output latches on the next rising edge of the CONV signal. Two control inputs are provided on the TDC1007 for changing the format of the the output data. When NMINV is tied low, the most significant bit

of the output data is inverted, while tying NLINV low, the seven least significant bits of the output data are inverted. By using these controls, the output data format can be binary, two's complement, or inverted two's complement. However, for test purposes, binary format is chosen (i.e. by connecting NMINV and NLINV high). The TDC1007 does not have overrange or underrange outputs. Software is written to accomplish detection for overrange and underrange cases (see SOFTWARE DESCRIPTION).

Two 74LS373 (U3 and U5) latches are used as control and status registers. Control register U5 is selected through select line Sn, while the status register U3 is selected by select line Sn+1. Table 4.3 shows the bit configuration for the registers.

Table 4.3 BIT CONFIGURATION FOR CONTROL AND STATUS REG.

BIT #	CONTROL REG.	STATUS REG.
0	Start Convert	End of Conversion
1	2-Channel	2-Channel
2	Channel Selection	Channel Selection
3	Switch 3	Switch 3
4	Switch 4	Switch 4
5	Switch 5	Switch 5
6	Read/Write	Read/Write
7	Reset	Reset

4.2 DMA CLOCK

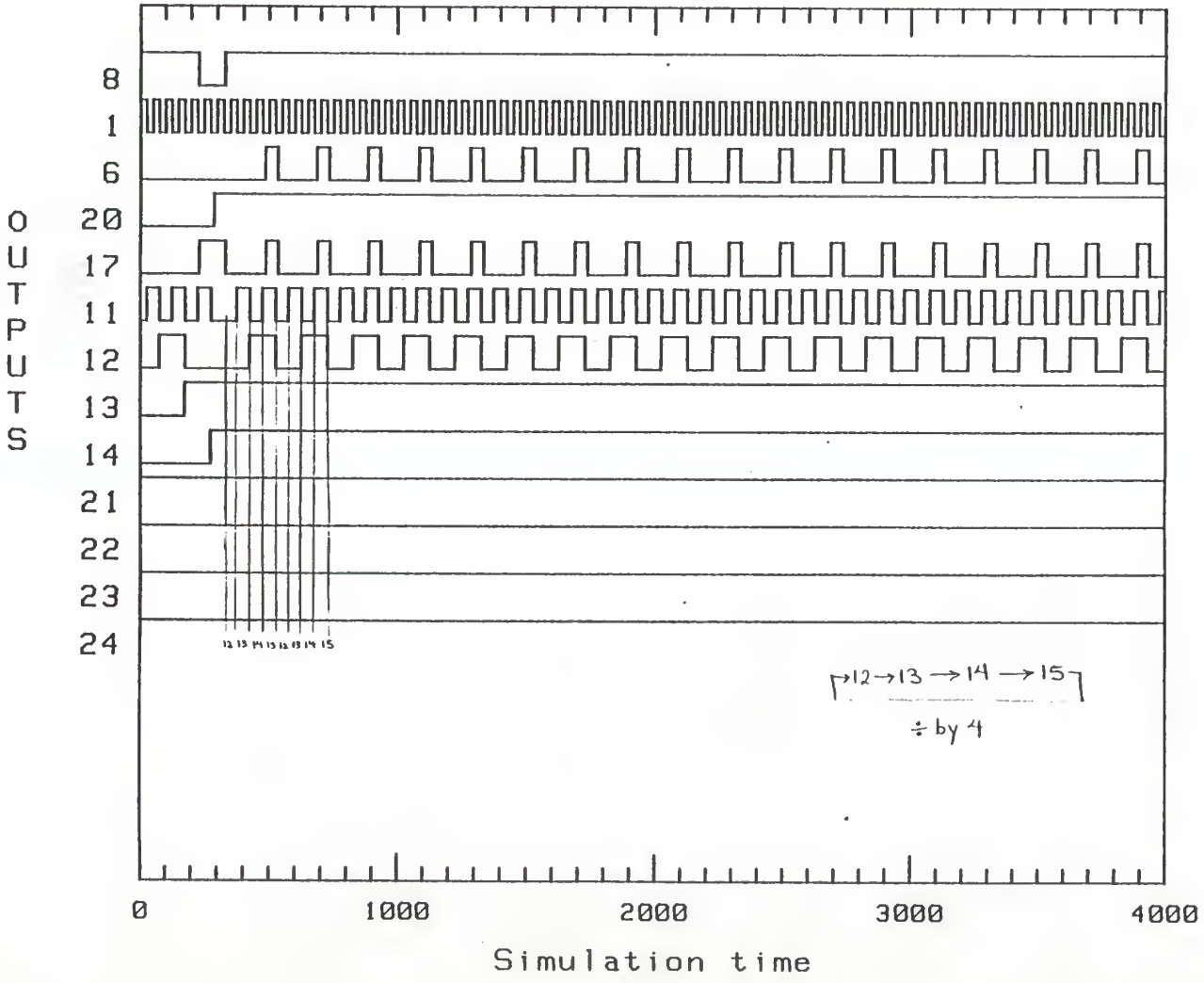
The DMA clock is generated by a 20MHz crystal and associated circuitry. An 8-bit programmable divider consisting of two 4-bit counters (74HC161s) U17 and U18 cascaded together are used to divide the fixed frequency of 20MHz by an integer, ranging from 0 to 254. This range of division gives the user the ability to sample analog signals from 78.7KHz up to 10MHz.

Shown in Fig. 9 is a simulation of an 8-bitprogrammable divider. This figure shows timing diagrams for a divide by 4 example. Table 4.4 is a listing of signals in Fig. 9.

Table 4.4 TIMING DIAGRAM REFERENCE DESCRIPTION

REFERENCE #	DESCRIPTION
8	Load Enable
1	20MHz Clock Input
6	Ripple Carry O/P from 1st Stage
20	Ripple Carry O/P from 2nd Stage
17	Flash Clock
11	QA from 1st Stage
12	QB from 1st Stage
13	QC from 1st Stage
14	QD from 1st Stage
21	QA from 2nd Stage
22	QB from 2nd Stage
23	QC from 2nd Stage
24	QD from 2nd Stage

FIG. 9 DIVIDE BY FOUR TIMING DIAGRAM



The first stage counts to all ones and outputs a pulse which in turn enables the second stage. The ripple carry outputs from the two stages are fed to the input of a NAND gate, and the output is connected to the load pins of the counters. Each time the output from the NAND gate goes low the counters load the input value. This way the counters are used as a divider.

An 8-bit latch 74HC373 (U19) is used to latch the desired input to the counters from the data bus. The latch is enabled by addressing select line Sn+3. Once the processor writes the desired count value to the latches, that count value will be used throughout the data collection period. Table 4.5 lists the valid counter values and the corresponding sampling rates.

Table 4.5 COUNTER VALUE vs. SAMPLING FREQUENCY

COUNTER VALUE	SAMPLING FREQUENCY
254	10MHz
253	6.66MHz
252	5MHz
.	.
.	.
2	79.36KHz
1	79.0KHz
0	78.7KHz

As shown in table 4.5, the sampling frequency based upon the 8-bit counter value is:

SAMPLING FREQUENCY=[20MHz/(256-COUNTER VALUE)] for

COUNTER VALUE < 255

CHAPTER-5

SYSTEM INTERFACING

5.1 INTERFACE DESCRIPTION

The FADC module is interfaced to the HP9845B microcomputer via the 16-bit HPI/O bus (98032A). The HP98032A I/O interface is a general purpose interface which provides 16-bit data exchange between the HP desktop computer and a peripheral (in this case the FADC module). The HP98032A has an interface card which can be configured for different data formats such as positive or negative logic, word or byte mode, etc. Table E.1 is the jumper configuration for the interface card. The cross(X) signs in front of the jumper numbers indicate the jumper connections for this design. Each of the data input lines(16) on the interface are connected to input latches. A resistive divider is connected to each of the input lines, these dividers hold the voltage at TTL level. But, each output line from the interface is driven by an open-collector circuit. Hence, a 14-line terminator (220/330) resistor network was put at the output driver lines to drive TTL components on the board.

The FADC module is controlled and monitored from the computer through a control register, a status register, and six select lines. The control register is write only, and is used to configure the FADC mode. The status register is read only and is used to monitor the status of the FADC module. The registers are written to or read from via the HPI/O bus. They are placed on the data bus by the correct selection of the select lines. The 8-bit control lines are connected to the lower 8 HPI/O lines, and the

select lines are tied to the upper 6 lines. The status and data lines from the FADC module are connected to the lower 8 lines of the HPI/O, and the 8 upper lines of the HPI/O lines are tied low. Table 5.1 is a description of the select lines from the HP9845B.

TABLE 5.1 SELECT LINE DESCRIPTION

SELECT LINE	DESCRIPTION
Sn	latches control word
Sn+1	outputs status word to HPI/O
Sn+2	Toggled to step through Flash memory address when reading from Flash memory
Sn+3	loads clock divisor into Flash clock divider
Sn+4	Flash memory is read when low
Sn+5	latches beginning address into Flash address counter

5.2 CONTROL ALGORITHM

The following are the algorithms necessary to control the FADC module.

A. Specifying the sequence to load the Flash clock divider

B. Writing to control register

C. Reading from the status register

D. Specifying the sequence to load the number of A/D conversions

E. Reading data from Flash memory

The following sections describe the above in detail.

A. The sequence to load the Flash clock divisor

1) Read the status register.

2) If the Flash is tri-stated (i.e. bit D0=1), continue, else abort attempt(data is being written in memory).

3) Write desired divide by value to clock divider latch by placing the word on the data bus and toggling select line Sn+3.

4) The FADC is now operating at the desired sampling freq.

B. The sequence used to write to the control register

1) The status register is read by setting Sn+1 low and checking Flash tri-state bit(D0).

2) If the Flash tri-state bit(D0) is high then the control register can be written to(this assumes that the control register will not be changed while taking data).

3) The control word is written to the control register by by placing the word on the data bus and toggling select line Sn.

4) With Sn high, the new control word has been loaded into the control register.

C. The sequence used to read from the status register

1) Select line Sn+1 is set high.

2) Status word is read from the data bus.

3) Sn+1 is set low.

D. The sequence for loading number of A/D conversions

1) Read Flash status register, check for conversion in progress(D0). If conversion in progress, abort attempt, else continue.

2) Write the desired number to the address counters by placing the number on the data bus and toggling select line Sn+5.

3) The new conversion value is now loaded into the address counter.

E. The sequence to read data from Flash on-board memory

1) Read the status register and check for Flash tri-state (if D0=1 continue, else abort attempt).

2) Load the control register with 40 hex. This sets the memory for read mode.

3) Load the beginning Flash memory address(this is the same value used when loading the number of A/D conversions).

4) Set select line Sn+4 high. This connects the Flash data bus to the HPI/O bus.

5) Toggle Sn+2 and read data into an array.

6) Check for EOC(end of conversion) high signal (status register bit D7).

7) Repeat steps 5 thru 6 until EOC goes high.

CHAPTER-6

ANALYSIS OF RESULTS

Two type of tests were used to evaluate the FADC system. First, static testing was performed with the system under test having a DC input voltage. The second kind of testing was dynamic and the FADC was exercised with a sinusoidal input. These two tests should give good characterization of the FADC performance.

The Static Testing

The static testing was done by applying a dc voltage between 0.0V and -2.0V to the analog input. The results from the static testing should indicate if there are any missing codes from the FADC as well as the level of noise in the system.

Two different dc signals one at -1.2V and the other -.58V were applied to the input which were digitized at sampling rates of 2.5MHz and 39KHz respectively. Fig. 10 shows the dc level as a function of time plot. Also, the fast Fourier transform (FFT) was performed on the data to see the magnitude as a function of frequency response. Fig. 11.a. is the FFT plot for the -1.2V dc sampled at 2.5MHz and Fig. 11.b. is the plot for the -.58V dc sampled at 39KHz. From the FFT plots one can note that with the decrease of sampling rate the noise level has decreased by about 5dB.

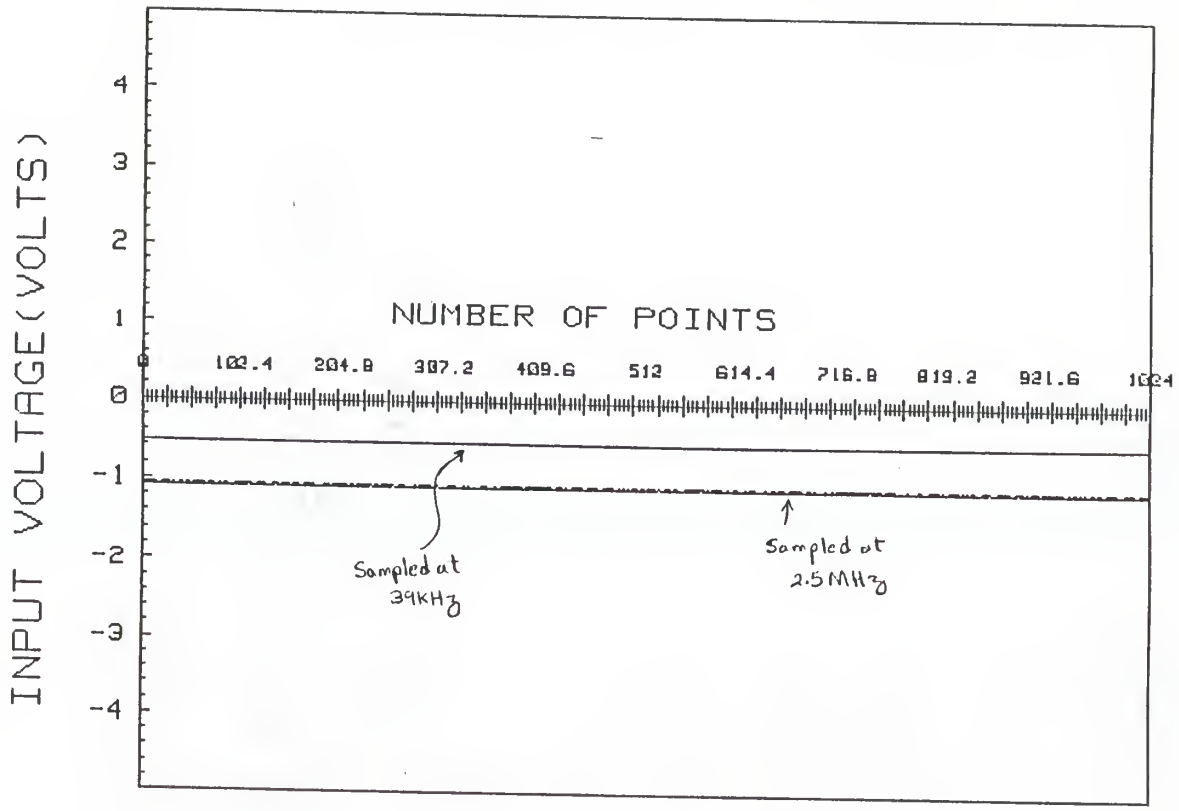
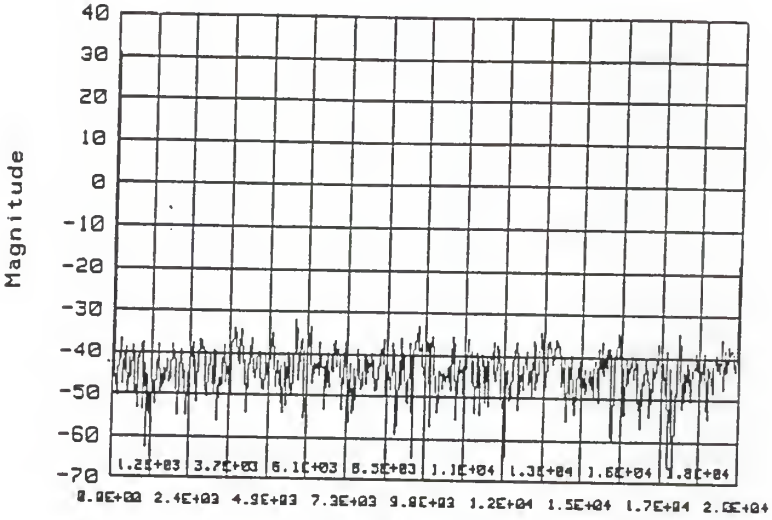


Fig. 10

DC Signal Level as a Function of Time

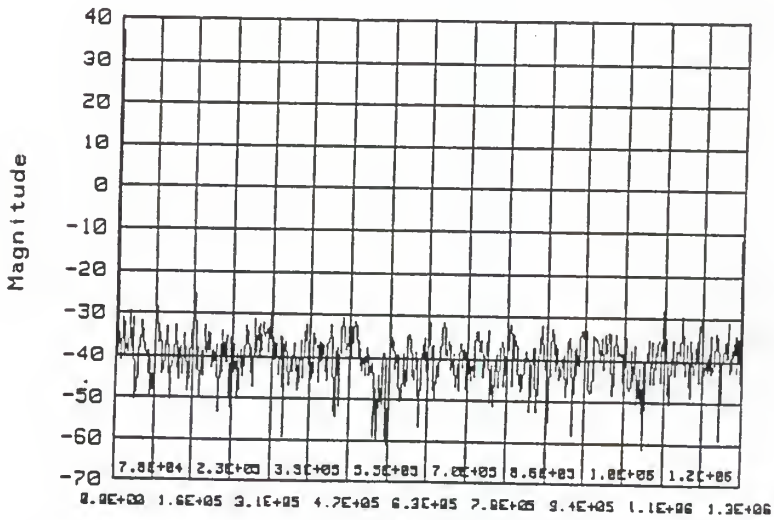
Fig. 11.b. FFT Plot for -.58V DC signal



Magnitude as a Function of Frequency

f= 0 , Sampling Frequency= 39000 , 1024 points

Fig. 11.a. FFT Plot for -1.2V DC signal



Magnitude as a Function of Frequency

f= 0 , Sampling Frequency= 2500000 , 1024 points

The Dynamic Testing

The dynamic testing was performed to see if the FADC system performed well in the dynamic range. Under static test conditions ADCs tend to behave ideally, but when faced with transients, most ADCs introduce error. Under dynamic operating conditions, a converter's transfer function can change dramatically. This change is due to the transfer function's direct dependence on how fast the converter's components can react to a change of state. For an 8 bit FADC the dynamic range is calculated to be 48dB. In general the dynamic range for any ADC can be found from 6.02ndB, where n is the resolution, in this case n=8.

For the dynamic testing a full scale sinusoidal waveform was applied to the input and sampled at different sampling frequencies. Fig. 12 shows the real-time plot of a 40KHz sinewave sampled at 2.5MHz and fig. 13 corresponds to the FFT plot. As shown in this plot the highest harmonic component measures 37dB below the full scale. A second order active filter with a cut off frequency of 45KHz was then placed at the input of the system to reduce any harmonic distortion from the function generator. Fig. 14 depicts the FFT plot of the same sinewave (40KHz) with the filter. From this plot it can be noticed that the highest harmonic component is now about 48dB below the fundamental. Since the harmonic distortion is about 48dB below the fundamental amplitude, the error caused by integral nonlinearity can be concluded to be 1 bit. In both plots the peak at about 1.21MHz represents the beat between 40KHz input and the 2.5MHz sampling

frequency aliased into the baseband.

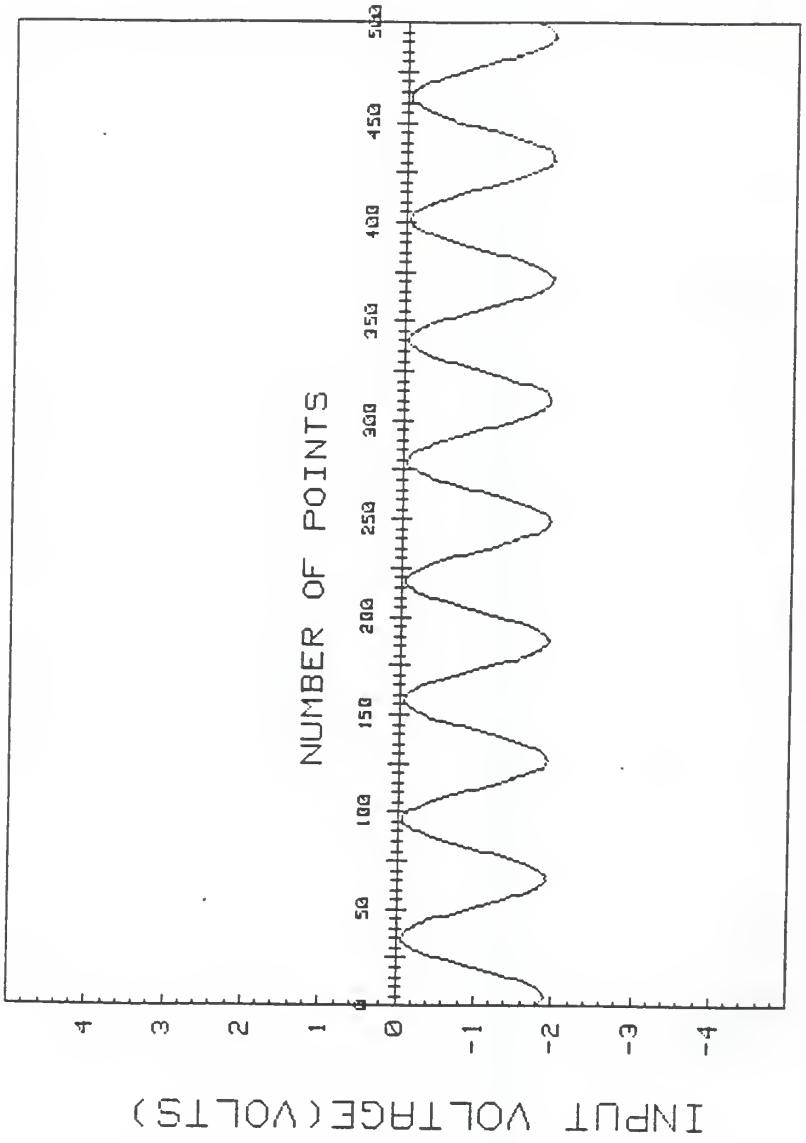


Fig. 12.
Voltage as a Function of Time

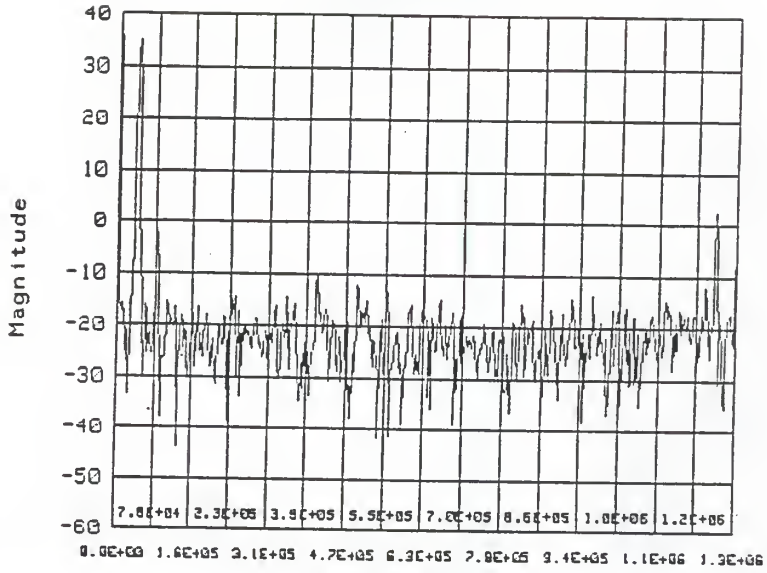


Fig. 13 FFT Plot for the 40KHz Sinewave

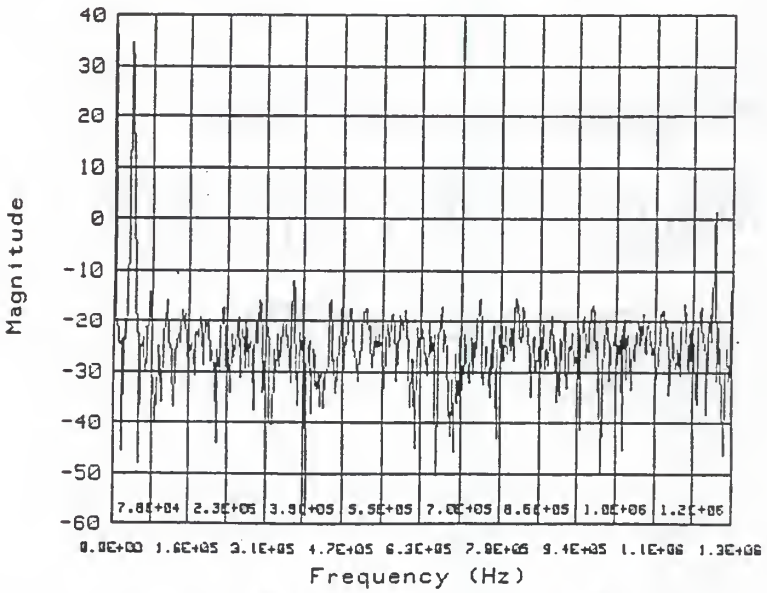


Fig. 14 FFT Plot for the 40KHz sinewave with Filter

CHAPTER-7

CONCLUSIONS

The results from the research into the performance of the FADC system with the use of an alternating method was satisfactory. However, there exist noise problems in the system mainly related to the 20MHz crystal. Also, the wirewrap section of the board (digital section) had enhanced the noise problems. It is the recommendation of the author that the FADC system be built on a PC layout as well as using CMOS digital components where ever necessary. In addition it is recommended to build the analog section on a separate board from the digital section such that the noise from the 20MHz crystal does not distort the analog input signal. Finally, shielding the clock circuitry as well as decoupling all the power supply pins on both the analog and digital sections would even more improve the performance of the system.

APPENDIX A

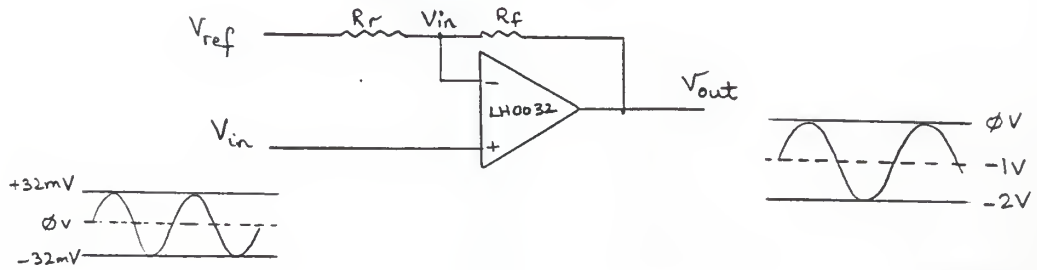
SWITCTH SETTING TABLE

Table A.1. Voltage Measurement and Switch Setting

SWITCH	VOLTAGE	40mV	400mV	4V
S1	Channel A			
S2	Channel B			
S3	V/1 attenuation	X		
S4	V/10 attenuation		X	
S5	V/100 attenuation			X

APPENDIX B

Vref and Gain Calculations



Vout should be between 0V and -2V (i.e. input to FADC).

For a 0V input (Vin=0) the output voltage should be -1V (Vout=-1)

KCL:

$$(Vin-Vref)/Rr + (Vin-Vout)/Rf = 0$$

$$Vin(1/Rr+1/Rf) - Vref(1/Rf) - Vout(1/Rf) = 0$$

Step #1: let Vin=0V and Vout=-1V, Vref=?

$$(0-Vref)/Rr + (0+1)/Rf = 0$$

$$1/Rf = Vref/Rr \qquad Vref = Rr/Rf$$

Step #2: let Vin=32mV and Vout=0V, Vref= Rr/Rf

$$32mV(Rr+Rf/RrxRf) - Rr/Rf(1/Rf) - 0 = 0$$

$$32mV(1+Rf/Rr) - Rr/Rf = 0 \quad \ldots\ldots\ldots\ldots \quad 1$$

Step #3: let Vin=-32mV and Vout=-2v, Vref= Rr/Rf

$$-32mV(Rr+Rf/RrxRf) - Rr/Rf(1/Rf) + 2(1/Rf) = 0$$

$$-32mV(1+Rf/Rr) - Rr/Rf + 2 = 0 \quad \ldots\ldots\ldots\ldots \quad 2$$

from 1 and 2 we get,

$$64mV(1+Rf/Rr) - 2 = 0$$

$$32mV(1+Rf/Rr) = 1$$

$$Rf/Rr = 30.25$$

and Vref= 1/30.25= 33.1mV

APPENDIX C

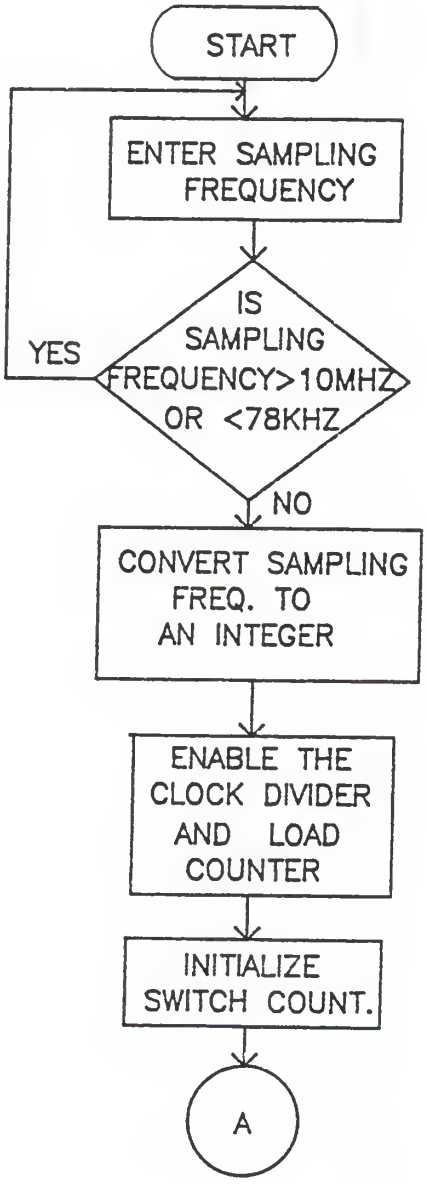
FLOW CHART AND PROGRAM DESCRIPTION

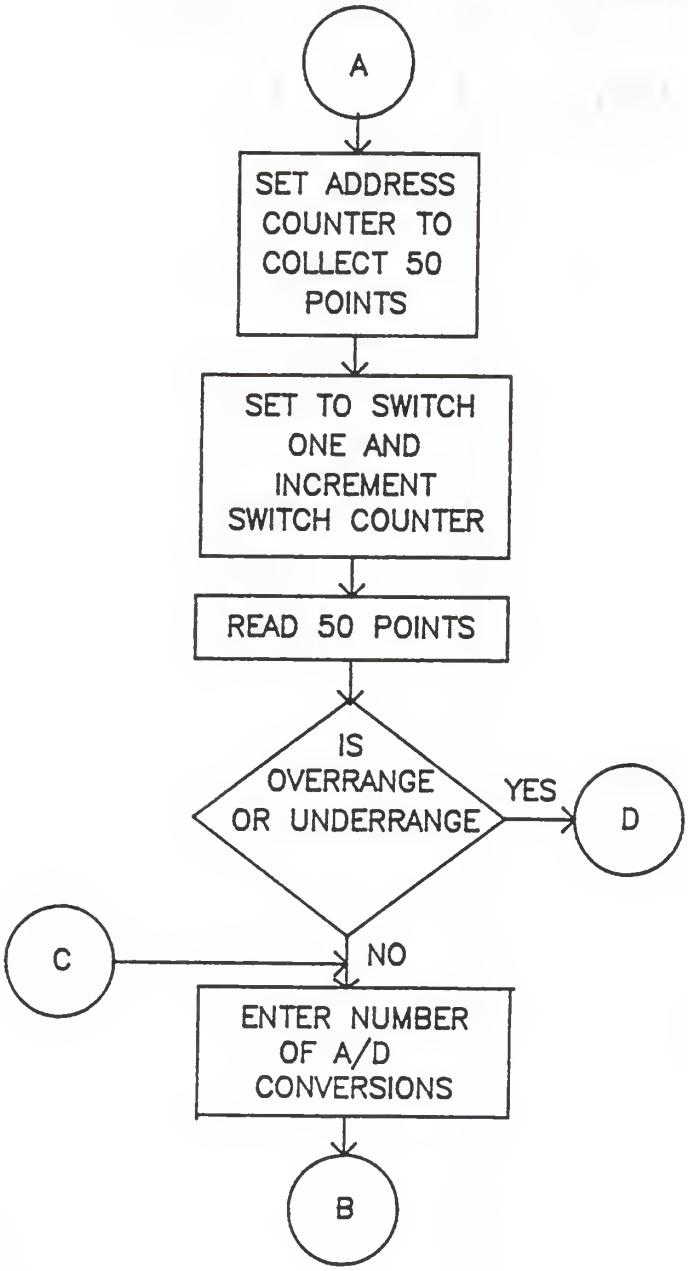
The monitor program for the FADC module starts by requesting a sampling frequency between 10MHz and 78KHz. As the user enters the valid sampling frequency, the corresponding integer value is then latched into the clock divider registers.

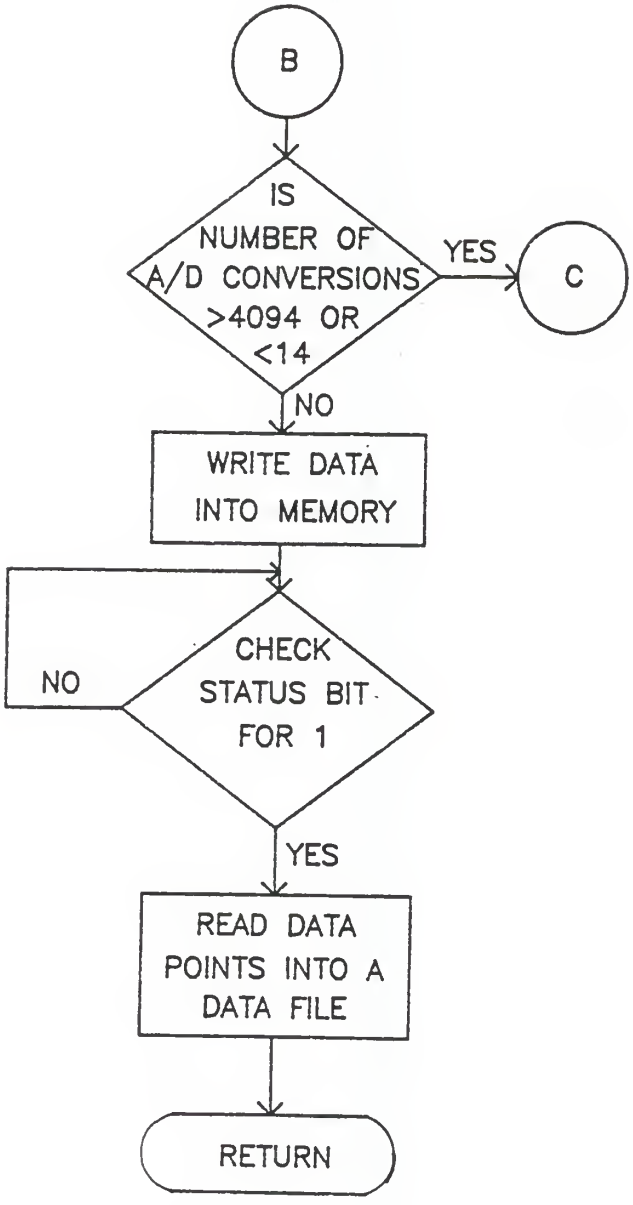
The monitor program is initialized to read 50 data points and check for the underrange and overrange cases. Switches 3, 4, and 5 are then set to provide proper attenuation of the input signal. TableA.1. in Appendix A shows the switch setting arrangement. After the switches are set for proper attenuation, the program waits for the user to enter the desired number of A/D conversions. After the number of A/D conversions has been entered data is then written into the memories (by DMA controller).

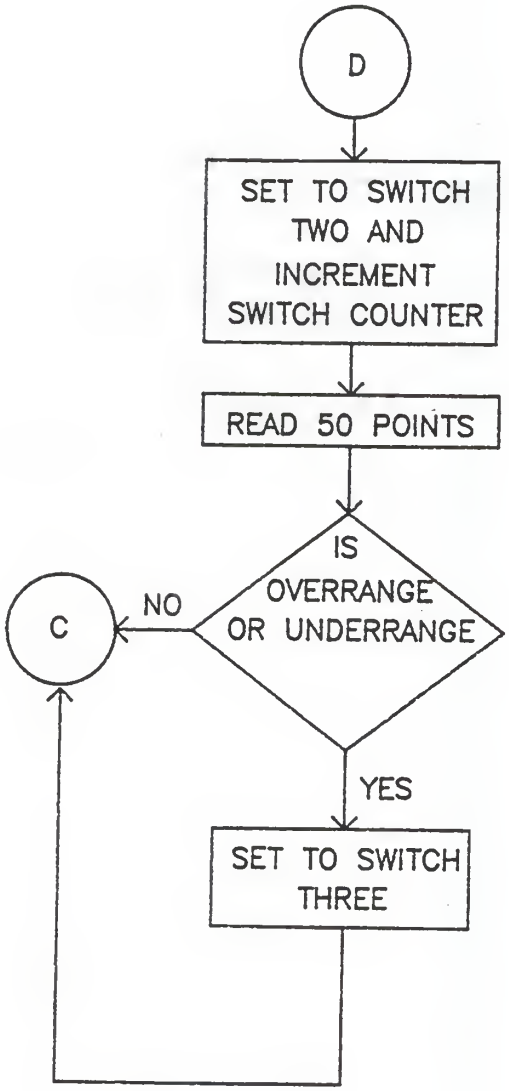
Then the status register bit 0 (D0) is checked for the end of conversion (EOC) signal. With EOC going high, the number of A/D conversions is loaded into the address counter registers(the same number for storing the number of A/D conversions). Thus, the stored data is then read from the on-board memories into a data file through the HP I/O bus.

COLLECT–DATA ROUTINE




A
SET ADDRESS COUNTER TO COLLECT 50 POINTS
SET TO SWITCH ONE AND INCREMENT SWITCH COUNTER
READ 50 POINTS
IS OVERRANGE OR UNDERRANGE
YES
D
C
NO
ENTER NUMBER OF A/D CONVERSIONS
B


B
IS NUMBER OF A/D CONVERSIONS >4094 OR <14
YES
C
NO
WRITE DATA INTO MEMORY
CHECK STATUS BIT FOR 1
NO
YES
READ DATA POINTS INTO A DATA FILE
RETURN


D
SET TO SWITCH TWO AND INCREMENT SWITCH COUNTER
READ 50 POINTS
IS OVERRANGE OR UNDERRANGE
NO
C
YES
SET TO SWITCH THREE

APPENDIX E

HP I/O Jumper Configuration

Jumper	Function, when installed
X 1	Sets bit 3 in the status register, changes the input data lines to positive true logic.
X 2	Sets bit 2 in the status register, changes the output data lines to positive true logic.
3	Complements the logic sense of PCTL; high = control set and low = control clear.
4	Complements the logic sense of PFLG; high = ready and low = busy.
5	Complements the logic sense of PSTS; high = not OK and low = OK.
6	Changes the handshake from full to pulse.
7	Allows the calculator to activate the DMA (Direct Memory Access) mode of operation.
8	Clocks the high input byte when PFLG goes busy from ready.
• 9	Clocks the high input byte when PFLG goes ready from busy.
X A	Clocks the high input byte at the time the calculator reads the register.
X B	Selects the words input mode.
C	Clocks the low input byte at the time the calculator reads the register.
• D	Clocks the low input byte when PFLG goes ready from busy.
X E	Clocks the low input byte when PFLG goes busy from ready.
X F	Selects the words output mode.

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A 10MHZ FLASH ANALOG-TO-DIGITAL CONVERTER SYSTEM FOR DIGITAL OSCILLOSCOPE AND SIGNAL PROCESSING APPLICATIONS

by

FARNAD SAJJADIAN

B.S., Kansas State University, 1983

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KANSAS STATE UNIVERSITY

Manhattan, Kansas

1985