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A SOFTWARE SIMULATOR TO HOST
THE DATA GENERAL NOVA ON THE IBM 360

by

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INTRODUCTION

A simulator allows programs written for one computer to be run on another. So does an emulator. Because of this there has been some confusion about the difference. As a matter of fact some people use the terms interchangeably. Compounding this confusion, simulation also refers to an entirely different concept, mathematical modelling.¹

The difference between the two is primarily the difference between the hardware and the software. An emulator can be implemented in two ways, by building an external hardware interface between the program input device and the computer or by changing the computer itself through microprogramming.

A simulator is a program written for the purpose of making the existing software and hardware compatible. Its advantage lies in the fact that no additional hardware needs to be built. So the computer requires no change that would alter its basic architecture, providing an additional measure of flexibility.

Software simulation of one computer on another can result in great gain with little effort. While the pitfalls of simulation are many, it is still the closest thing to a legal 'something-for-nothing' available to the computer user. It offers an opportunity of getting the available powers of one machine on another.

The purpose of this project was to provide a simulator which could be used to host the Data General Nova on an IBM 360. As described in the Systems Reference Manual For The Nova (2), the Nova computers are general purpose computer systems with a 16 bit word length. The machine is organized around four accumulators, two of which can be used as index registers. This accumulator/index register organization provides great efficiency and ease in

programming. The central processor performs a program by executing instructions retrieved from consecutive memory locations as counted by the 15 bit program counter PC. At the end of each instruction PC is incremented by 1 so that the next instruction is normally taken from the next consecutive location. Sequential program flow is altered by changing the contents of PC, either by incrementing it an extra time in a test skip instruction or by replacing its contents with the value specified by a Jump instruction. The other internal registers of importance to the programmer are four 16 bit accumulators, AC0 to AC3. Data can be moved in either direction between any memory location and any accumulator. Any instruction that references memory may address AC2 or AC3 as an index register. Instructions that move data to and from memory or the peripherals address a single accumulator as a source or destination of data while addressing a memory location or an I/O device. But the arithmetic and logical instructions do not reference memory; they simply address two accumulators, either or both of which may supply operands, and one of which may receive the result. Since an arithmetic or logical instruction does not contain a memory address, there are many bits that can be used for functions other than specifying the basic operation and the operands: the same instruction that adds or subtracts can also shift the result or swap its halves, test the result and/or carry for skip, and specify whether or not the result shall actually be retained.

Each instruction that addresses a memory location contains information to determine the effective address, which is the actual address used to fetch or store the operand or alter the program flow. The instruction specifies an 8-bit displacement which can directly address any location in four groups of 256 locations each. The displacement can be an absolute address, i.e. it may

be used simply to address a location in page zero, the first 256 locations in the memory. But it can also be taken as a signed number that is used to compute an absolute address by adding it to a 15-bit base address supplied by an index register. The instruction can select AC2 or AC3 as the index register; either of these accumulators can thus be used as an ordinary index register to vary the address computed from a constant displacement, or as a base register for a set of different displacements. The program can also select PC as a index register, so any instruction can address 256 words in its own vicinity (relative addressing). The computed absolute (15 bit) address can be the effective address. However, the instruction can use it as an indirect address, i.e. it can specify a location to be used to retrieve another address. Bits 1-15 of the word read from an indirectly addressed location can be the effective address or they can be another indirect address.

The program can make use of an automatic indexing feature by indirectly addressing any memory location from 20_8 to 37_8 . Whenever one of these locations is specified by an indirect address, the processor retrieves its contents, increments or decrements the word retrieved, writes the altered word back into the memory, and uses the altered word as the new address, direct or indirect. If the word is taken from locations 20_8 to 27_8 , it is incremented by 1; if taken from locations 30_8 to 37_8 , it is decremented by 1.

In the early stages of this project it was attempted to translate the Nova Object Codes (NOC) into IBM 360 Assembly Language, but it was found that simulation in this way will put some unnecessary restrictions on Nova Assembly Language programmers. For example, in such a case it would be virtually impossible to code Nova Assembly Language instructions to modify other instructions of the same program.

These restrictions provided an impetus to design some software to simulate the Nova Central Processor, instead of the NCC, on the 360.

This report describes the operation and scope of a software package which effectively simulates the operation of the Nova Central Processor on the IBM 360, except for I/O operations. The software package consists of a single PL/I program, which, when invoked, behaves as a Nova Central Processor and effectively simulates the execution of the NCC.

As Nova hardware processor is being simulated on the 360 software, it is not unexpected that the execution time of the NCC is considerably increased.

DESIGN OF THE SIMULATOR

The simulator basically consists of a variable size software-simulated Nova core and a software processor. The simulator reads in the core size in words -- each Nova word is 16 bits long -- and allocates appropriate 360 storage in units of 16 bits. Next it reads in the address of the memory starting from which the program is to be loaded, and the memory address at which the execution of the program is to begin. After this initialization phase the object code of the Nova program is read into the simulated memory and the execution is started as soon as the whole object module has been loaded. From the specified location it fetches one 16 bit instruction and interprets it in terms of the desired Nova operation and available System 360 facilities. The desired operation is then performed using 360 PL/1 instructions. The next instruction is then fetched, normally from the next consecutive software-simulated Nova word unless the immediately preceding operation itself dictates the location of the word from which the execution is to be resumed.

The simulation is terminated whenever any of the following conditions is met:

1. A HALT instruction is encountered.
2. An unidentifiable instruction is encountered.
3. The size of the object module exceeds the specified core-size.

At the termination of simulation the amount of core used by the object module, all the accumulators, the SHIFTER and the CARRY are printed out. If the termination occurs due to one of the first two conditions, the current value of the program counter is also printed out to show the last executed instruction.

NOVA OBJECT CODE

The following is a description of the structure of NOC, as given in the Nova manual (2,3).

There are four basic formats for instruction words. In all but the arithmetic and logical instructions, bit 0 is off. If bits 1 and 2 are also off, bits 3 and 4 specify the function, jump or modify memory, and the rest of the word supplies information for the calculation of effective address. Bits 8 to 15 are the displacement, bits 6 and 7 specify the index register if any, and bit 5 indicates indirection of address.

0	0	0	FUNCTION	TYPE	INDEX	DISPLACEMENT		
0	2	3	4	5	6	7	8	15

Jump and Modify Memory Instructions

If bits 1 and 2 of the instruction word are different, they specify a Move Data function. Bits 3 and 4, in this case, address an accumulator, the rest of the word is as above.

0	FUNCTION		ACCUMULATOR		TYPE	INDEX		DISPLACEMENT	
0	1	2	3	4	5	6	7	8	15

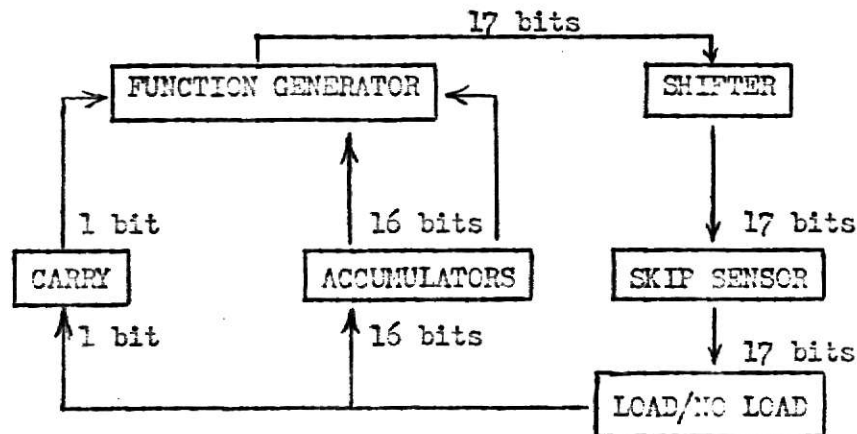
Move Data Instructions

If bit 0 of the instruction word is one, bits 5 to 7 specify an arithmetic or logical function. The structure of an arithmetic or logical instruction word is shown below.

1	AC Source		AC destination		FUNCTION			SHIFT		CARRY		LOAD	SKIP
0	1	2	3	4	5	6	7	8	9	10	11	12	13 15

Arithmetic and Logical Instructions

Each instruction in this class specifies one or two accumulators to supply operands to the function generator, which performs the function specified and produces a carry bit, whose value depends upon a base value specified by the instruction, the function performed and the result obtained. The base value may be derived from the carry flag or the instruction may specify an independent value.



Organization Of Arithmetic Unit

The 17-bit output of the function generator, comprising the carry bit and the 16-bit function result, then goes to the shifter. Here the 17-bit result can be rotated one place right or left, or the two 8-bit halves of the 16-bit function result can be swapped without affecting the carry bit. The 17-bit shifter output can then be tested for skip; the skip sensor can test whether the carry bit or the rest of the 17-bit word is or is not equal to zero. The 17-bit shifted word can be loaded into **CARRY** and one of the accumulators selected by the instruction. However, loading is not necessary; an instruction can perform a complicated arithmetic and shifting operation and test the result for skip without affecting **CARRY** or any accumulator.

The carry flag can be used in conjunction with the sign of the result to

detect overflow in operations on signed numbers, but its primary use is as a carry out of the most significant bit in operations on unsigned numbers, such as the lower order parts in multiple precision arithmetic. For unsigned numbers a carry is produced if addition or incrementing increases the number beyond $[2^{16}-1]$. In subtraction, the condition is the same if, instead of subtracting, the complement of the subtrahend is added and one is added to the result (subtraction is performed by adding the two's complement). In terms of the original operands, the subtraction $(A-B)$ produces a carry if A is greater than, or equal to B.

SIMULATION OF THE NOVA OBJECT CODE

1. Memory Reference Instructions:

The basic logic of the simulation of memory reference instructions consists of two basic steps, the calculation of the effective memory address and the simulation of the basic operation as specified by the object code.

The calculation of simulated address is taken care by an internal procedure called ADRSR.

The ADRSR fetches bits 9 to 16 of the NOC and converts them into a binary integer called M, by appending 8 binary zeros at the left end of M. Now if the NOC specifies absolute addressing, M is saved in a field called ADDR5. As in the other two types of addressing viz, relative and indexed, the displacement is signed, the ADRSR checks bit 9 of the displacement field to see if the displacement is negative. If so, the 8 zeros in the left half of M are replaced by 8 binary ones, in order to make the integer representation negative (2's complement notation).

If the object code specifies relative addressing, this binary integer is added to the contents of the simulated program-counter and placed in ADDR5. If the address is indexed, the bits representing the index register are picked up from the NOC and are used as a subscript to point to one of the four simulated accumulators. The contents of this accumulator are converted to a binary integer by using the UNSPEC function, and then added to M. The sum is then placed in ADDR5.

Bit 6 of the object code is now checked to see if the effective address is direct or indirect. If it is an indirect address the following procedure is followed:

The rightmost 15 bits of the simulated core location, pointed to by the

contents of ADDRS, are picked up and converted into a binary integer called M, appending a zero in the high order bit of M by using the UNSPEC function. If the core location from which the 15 bits have been fetched lies between 16_{10} to 23_{10} of the simulated core, M is increased by one and the rightmost 15 bits of the updated contents are stored back into the location from which they were fetched; otherwise if the address of the simulated core location lies between 24_{10} to 31_{10} , the contents of M are decreased by one and the rightmost 15 bits of the updated contents are stored back into the location from which they were fetched. Bit 1 of this location is now fetched and if it is a one, indicating an indirect addressing, bits 2 to 15 are again converted back to a binary number by appending 8 zeros at the high order position. This number is stored in ADDRS and the cycle is repeated until such contents are fetched whose bit one is nonzero, which indicates a direct address. As soon as a direct address is found out it is stored into ADDRS. The internal procedure now checks whether the address lies within the bounds of the object module and if not, a message is printed out just as a warning and no other action is taken. It should be noted that this last operation does not represent an equivalent operation of the Nova processor. The Nova processor does not perform any such checking. It simply uses the computed address as the effective address.

At this point the internal procedure returns the control back to the main procedure, with the effective address in the field called ADDRS.

Once the simulated address has been computed only the basic operation of the NOC remains to be simulated. The following is the description of the basic operation of different memory reference instructions:

MOVE DATA INSTRUCTIONS: If the bits 1 to 3 of the NOC are 001 then the

transfer of data from memory to a register is specified, otherwise if these bits are 010 the transfer of data is the other way around, that is, from one of the registers to memory. In these two cases bits 3 and 4 of the NCC are fetched from the NCC and converted to a binary number which is used as a subscript to point to the appropriate simulated accumulator, the contents of ADDRS are used as a subscript to point to the appropriate locations in the simulated Nova-memory. The transfer of data operation is simulated by PL/1 assignment statement.

JMP & JSR INSTRUCTIONS: These instructions specify that a branch is to be made to the effective address, that is, from the memory location pointed to by the contents of ADDRS. The JMP instruction is simulated by simply replacing the contents of PC by the effective address. JSR is slightly different in that before a branch is made return address is saved in accumulator 3. This operation is simulated by:

- Increasing the program counter (PC) by 1.
- Storing the bit representation of the PC in simulated accumulator 3.
- Replacing the contents of PC by those of ADDRS.

After any of these branch instructions has been simulated, the next instruction to be simulated is fetched from the core location pointed to by the PC.

Modify Memory Instructions: If bits 4 and 5 of the NCC are 10 or 11, it specifies Increment and Skip if Zero (ISZ) or Decrement and Skip if Zero (DSZ) instructions, respectively. Both of these instructions are simulated by:

- Fetching 16 bits from the simulated core location, pointed to by the contents of ADDRS.

- Converting these 16 bits to a binary number by using the UNSPEC function.
- Depending on bits 4 and 5 of the NOC, incrementing or decrementing this binary number by one.
- Storing the bit representation of the updated binary number back into the core location from where it was originally fetched.
- Incrementing the simulated PC by 1, if the resulting binary number was zero.

The last operation causes the skipping of the next instruction in the immediately following execution cycle.

2. Arithmetic and Logic Instructions:

As described earlier, each of these instructions specifies one or two accumulators to supply operands to the function generator, which performs the function specified by the instruction. The shifter is simulated as a 17-bit field. The four accumulators are simulated by an array of four elements each of which is 16 bits.

After simulating the basic function of the instruction, the result is stored in rightmost 16 bits of SHIFTER. In Nova, the function generator produces the carry bit whose value depends upon three quantities:

1. Base value specified by the instruction.
2. The function performed.
3. The result obtained.

The carry bit is simulated by the first of the 17 bits of the SHIFTER. In the Nova the base value of the carry may be derived from the carry flag. The carry flag is simulated as a 1-bit field, called CARRY.

In the Nova the 16-bit result and a 1-bit carry are then moved to the SHIFTER. The simulation of the SHIFTER was explained previously. In the Nova environment, the 17-bit result in the SHIFTER can be rotated one place right or left, or the two 8-bit halves of the 16-bit function result can be swapped without affecting the carry bit. As the first two operations deal with the individual bits, they are simulated by using the SUBSTR function. The swapping operation is simulated by using an 8-bit intermediate work area called STOROE3.

In the Nova, after the shifting operation has been performed, the skip sensor can test whether the carry bit or the other 16 bits are, or are not, equal to zero. This operation is simulated by converting the rightmost 16 bits of SHIFTER into a binary number and then comparing this number with zero.

Finally, the appropriate bit of the instruction is tested to find out whether the result of the operation is to be loaded into the destination accumulator (ACD) or not. Loading is simulated by a PL/1 assignment statement.

Simulation of Base Value of Carry Bit: The base value of the carry bit is simulated as follows:

- If bits 11 & 12 of the NOC are 00, the CARRY is unchanged.
- If bits 11 & 12 of the NOC are 01, the CARRY is equal to '0'B.
- If bits 11 & 12 of the NOC are 10, the CARRY is equal to '1'B.
- If bits 11 & 12 of the NOC are 11, the CARRY is equal to -CARRY.

Simulation of Left Rotation: This operation is simulated by:

- Storing the first bit of SHIFTER in a 1-bit field called STORE.
- Moving bits 2 to 17 into bit positions 1 to 16.
- Storing the bit in STORE into the 17th bit of SHIFTER.

Simulation of Right Rotation: This operation is simulated by:

- Storing the 17th bit of SHIFTER into a one bit field called STORE.
- Moving bits 1 to 16 into bit positions 2 to 17.
- Storing the bit in STORE in the first bit position of SHIFTER.

Simulation of Swapping: This operation is simulated by:

- Storing 2nd to 9th bits of SHIFTER in a 8-bit field called STORE3.
- Moving 10th to 17th bits of SHIFTER to 2nd to 9th bits of SHIFTER.
- Moving the 8 bits in STORE3 to the 8-bit right hand side subfield of SHIFTER.

Simulation of Loading: This operation is simulated by:

- Moving 2nd to 16th bits of SHIFTER to the Kth element of the array of registers simulating the Nova accumulators; where K is a binary number which is constructed by fetching bits 4 & 5 of the NOC (indicator of destination accumulator), and converting them into a binary number by using the UNSPEC function.
- Copying the first bit of SHIFTER into the one bit field called CARRY.

Simulation of Skipping: This operation is simulated by adding 1 to the simulated PC.

This operation causes the simulator to skip one instruction in the next execution cycle. The following text explains the simulation of various options of the Skip operation.

a) Skip on Zero Carry (SZC):

The first bit of SHIFTER is compared with a zero bit. If the comparison is equal, the skip operation is simulated.

b) Skip on Nonzero Carry (SNZ):

The first bit of SHIFTER is compared with a zero bit. If the comparison is unequal, the skip operation is simulated.

c) Skip on Zero Result (SZR):

Bits 2 to 16 of SHIFTER are converted to a binary number by UNSPEC function. This number is then compared with zero and if it is equal, the skip operation is performed.

d) Skip on Nonzero Result (SNR):

Bits 2 to 16 of SHIFTER are converted to a binary number by the UNSPEC function. This number is then compared with zero, and if it is unequal, the skip operation is performed.

e) Skip if Either Carry or Result is Zero (SEZ):

Both the comparisons of SZC and SZR are performed and if either of them shows an equal result, the skip operation is performed.

f) Skip if Both Carry and Result are Nonzero (SEN):

Both the comparisons of SZC and SZR are performed and if neither of them shows an unequal result the skip operation is performed.

g) Always Skip (SKP):

No checking is done and the PC is incremented by 1 under all the circumstances.

Simulation of the Basic Arithmetic & Logic Operations: The following text illustrates the simulation of the basic arithmetic and logic functions as specified by the NOC.

As these instructions refer to accumulators, bits 2-3 and 4-5 specify source and destination accumulators, respectively. As soon as any of these instructions is encountered these bits are picked up and converted to two binary numbers, J and K. These numbers are used as a pointer to locate the

corresponding simulated accumulators. J points to the source accumulator while K points to the destination accumulator.

a) Complement instruction (CCM):

Using the logical NOT function of PL/1, the 16 bits of Jth simulated accumulator, $\overline{\text{REG}(J)}$, are logically complemented and stored in bits 2-17 of SHIFTER.

b) Negate instruction (NEG):

Using the logical NOT function of PL/1, the 16 bits of REG(J) are logically complemented. Logical complement is then converted to a binary number and 1 is added to this number in order to get the 2's complement of the original value of REG(J). Bit representation of this 2's complement is then stored in bits 2-17 of SHIFTER. Now, if bits 2-16 are all off, bit 1 is replaced by the complement of CARRY, otherwise it is replaced by CARRY.

c) Move instruction (MOV):

The 16 bits of REG(J) are stored in bits 2-17 of SHIFTER. Bit 1 of SHIFTER is then replaced by CARRY.

d) Increment instruction (INC):

The 16 bits of REG(J) are converted to a binary number. 1 is then added to this binary number and the resultant value is stored in bits 2-17 of SHIFTER, using the UNSPEC function. Now, if all the 16 bits of REG(J) were zeros, bit 1 of SHIFTER is replaced by the complement of CARRY, otherwise it is replaced by CARRY.

e) Add Complement instruction (ADC):

The 16 bits of REG(J) are logically complemented by using the logical NOT function. This complement is then converted to a binary number M, using the UNSPEC function. The 16 bits of REG(K) are now converted to another binary

number called N. M and N are now added together and the sum is stored in bits 2-17 of SHIFTER.

If REG(J) is greater than REG(K), bit 1 of SHIFTER is replaced by the complement of CARRY, otherwise it is replaced by CARRY.

f) Subtract instruction (SUB):

The simulation of this operation is performed as follows:

- REG(J) is logically complemented by using the PL/1 logical NOT function.
- This complement is then converted into a binary number, M, by using the UNSPEC function.
- 1 is added to M to get 2's complement of the original value of REG(J).
- REG(K) is then converted to another binary number, called N, by using the UNSPEC function.
- M and N are added together and the sum is placed in bits 2-17 of SHIFTER, by using the UNSPEC function.
- If original value of REG(J) was not less than that of the original value of REG(K), bit 1 of SHIFTER is replaced by the complement of CARRY; otherwise it is replaced by CARRY.

g) Add instruction (ADD):

Basic operation of this instruction is simulated as follows:

- The 16 bits of REG(J) are converted to a binary number, M, by using the UNSPEC function.
- The 16 bits of REG(K) are converted to another binary number, N, using the UNSPEC function.
- The sum of M and N is placed in bits 2-17 of SHIFTER.

- If the sum is greater than 2^{16} , bit 1 of SHIFTER is replaced by the complement of CARRY; otherwise it is replaced by CARRY.

h) Logical AND instruction (AND):

This operation is simulated by storing the logical AND of REG(J) and REG(K) in bits 2-17 of SHIFTER by using the PL/1 AND operator.

TESTING AND DEBUGGING OF THE SIMULATOR

This simulator has been thoroughly tested for most of the possible errors. The following method was adopted in investigating whether the simulator simulated the Nova properly:

1. The simulator was broken up into different parts depending upon the types of instructions it simulates:
 - a) Move Data Instructions part.
 - b) Modify Memory & Jump instructions part.
 - c) Arithmetic & Logic Instructions part.
2. The calculation of memory addresses in memory reference instructions was applicable to a number of instructions, therefore it was also done in a separate module, although it was always tested along with the memory reference instructions.
3. Each of these modules was tested for most of the cases first independently of each other and then as one big module.
4. Finally, the modules for different types of instructions were merged into one module. In other words, the simulator now consists of three entities, arithmetic/logic simulation, memory reference simulation and effective address calculation simulation.

The sample programs which were tested on this simulator are included in Appendix II.

Since this simulator does not print the output, we tested the programs by executing the Nova Object Code on the simulator and on the Nova and then dumping out the simulated core and checking manually whether the result were the same as produced by Nova or not.

FUTURE MODIFICATIONS

This simulator is capable of simulating only execution of Nova Object Code, excluding I/O instructions. It does not simulate the hardware of the Nova completely. For example, it cannot simulate interrupts or the manual manipulation of the memory during the execution of a program.

The simulation of Nova I/O can be very easily incorporated in this simulator. The other two operations, however, are very difficult to simulate. The reason is that interrupts and manual manipulation are both time dependent features.

The main problem in the simulation of Nova I/O on the 360 is the interaction of the 360 I/O operations of one program with such operations of another concurrently running program. In the 360 environment, especially when using a high level language like PL/I, I/O operations are handled by the operating system; while in the Nova individual programs are responsible for their own I/O. Consequently, the logic of Nova I/O is very detailed since each and every thing is to be taken care of by the problem program. One individual step of this logic is meaningless if seen after separating it from other steps. Our simulator is not capable of decoding the logic of a Nova program. It simply reads one instruction and executes it. If it were possible to decide that the instruction being executed is a part of the I/O logic, the whole set of such instructions could be bypassed, and the control transferred to the appropriate 360 I/O routine.

Another problem is the difference in the internal and external representation of characters in the Nova and the 360. The internal representation of characters is entirely different in the two machines. Hence, whenever any I/O would be simulated a translation operation would have to be performed,

and this would somewhat affect the total execution time of a Nova program on the simulator.

One possible scheme of incorporating Nova I/O in this simulator would be to perform manual editing of the Nova listing and assigning special codes to those instructions which are a part of the I/O logic. The simulator would then be able to recognize these instructions and would be able to bypass them until it finds an explicit I/O instruction, at which point it can use the standard I/O routines of the 360. It should, however, be noted that this scheme would be practically useless in situations where the execution of a program would modify any of these marked instructions.

As of now, during the simulation of the execution of a Nova program whenever the simulator encounters an I/O instruction, it calls a procedure called I_O_ROUTINE. This procedure simply bypasses the simulation of the execution of this instruction and prints out a message:

'I/O INSTRUCTION BYPASSED AT LOCATION xxxx'

If, at any time, a routine is available which can simulate the Nova I/O, it can easily be appended to this simulator. It should, however, be noted that the simulation of Nova I/O is not easy, since detailed consideration must be given to the timing problems.

USING THE SIMULATOR

As described earlier, the main input to the simulator is the Nova Object Code. However, before reading in the Nova Object Code, the simulator looks to find out the following four initialization factors:

1. Core size of the Nova machine for which the original program was written.
2. Memory address at which the loading of the program is to begin.
3. Memory Address at which the execution of the program is to begin.
(This is to take care of such programs in which constants have been defined before the first executable code.)
4. Page zero location where the load address of this program is to be saved, i.e. the Restart Address.

These pieces of information should be presented in the input stream before the actual Nova Object Code, in the form of numeric constants in exactly the same sequence as they are listed above.

IMPORTANT: All four of these items should be in DECIMAL and NOT in OCTAL.

The main input of the simulator is the NCC in Binary Coded Octal. For example, the Nova source code:

ADD 1,2

is equivalent to:

133000₈

When coded in binary, each digit is represented by three bits except the first digit which is either a binary one or a binary zero. Hence, when this object code is to be used as input to the simulator, it should be coded as:

'1011011000000000'B

The simulator accepts input by a 'GET LIST' statement, and therefore, the

only format requirement for the input is that two binary coded NCCs should be separated by at least one blank, if there is more than one NCC on a single card, and each of them should be enclosed in quotation marks and followed by the alphabetic B. Consequently, a maximum of four NCCs can be accommodated in a single card.

After all the NCCs have been placed in the input stream, the last NCC should be followed by a non bit-string constant. This will raise a `CONVERSION` condition, which will be recognized by the simulator as the end of the Nova program. This is in anticipation for the situation when the simulator will be able to perform I/O also, at which stage the input to the Nova program will also have to be present in the input stream of the simulator.

It should be noted that the simulator recognizes a `CONVERSION` error as a valid condition indicating the end of the Nova Object Code, hence the input stream should be thoroughly checked for any undesirable non bit-string data items.

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Appendix I

PROGRAM LISTING

INTRPR: PRCC OPTIONS(MATN):

1 1

```

25      /* MODIFY POINTER TO POINT TO NEXT LOCATION          */ 23
26      LOAD_POINT=LOAD_POINT+1;                               */ 23
27      /* CHECK IF PROGRAM SIZE EXCEEDS CORE SIZE          */ 24
28      IF LOAD_POINT>CORE_SIZE-1 THEN                          */ 24
29          DO;                                                 4
30              PUT SKIP LIST('PROGRAM SIZE GREATER THAN CORE_SIZE JOB 25
31              TERMINATED');                                     4
32          STOP;                                                4
33          END;                                                 4
34      GO TO START;                                             2
35
36      /* START SIMULATION                                     */ 23
37      /* POINT PC TO NEXT MEMORY LOCATION                   */ 24
38      SIMULATE: PC=PC+1;                                       */ 24
39      /* CHECK IF A WRONG BRANCH HAS BEEN MADE             */ 25
40      IF PC<LOAD_POINT OR PC>CORE_SIZE THEN                  4
41          DO;                                                 4
42              PUT SKIP LIST('INVALID INSTR. ENCOUNTERED AT '||PC||'); 4
43          GO TO ENDS;                                          4
44      END;                                                     4
45
46      /* JOB HALTED?;                                       */ 4
47      GO TO ENDS;                                          4
48
49      /* SIMULATE NEXT INSTRUCTION                           */ 4
50      IF SUBSTR(NUVA(PC),1,8)='01101101'B THEN              4
51          DO;                                                 4
52              PUT SKIP LIST('JOB HALTED AT LOCATION '||PC||'); 4
53              GO TO ENDS;                                          4
54          END;                                                 4
55
56      /* CHECK FOR I/O INSTRUCTION                          */ 4
57      IF SUBSTR(NUVA(PC),1,3)='011'B THEN                    4
58          DO;                                                 4
59              /* SIMULATE I/O INSTRUCTION                   */ 4
60              CALL I/O_ROUTINE;                                4
61              /* GO BACK TO FETCH NEXT INSTRUCTION         */ 4
62              GO TO SIMULATE;                                    4
63          END;                                                 4
64
65      /* CHECK FOR ARITHMETIC/LOGIC INSTRUCTION             */ 4
66      IF SUBSTR(NUVA(PC),1,3)='1' THEN                        4
67          DO;                                                 4
68              /* SIMULATE ARITHMETIC/LOGIC INSTRUCTIONS    */ 4
69              CALL ARITH;                                       4
70              /* GO BACK TO FETCH NEXT INSTRUCTION         */ 4
71              GO TO SIMULATE;                                    4
72          END;                                                 4
73
74      /* CALCULATE EFFECTIVE ADDRESS OF MEMORY LOCATION    */ 4
75      CALL ADDR;                                               4
76      /* IF IT IS MODIFY MEMORY OR JUMP INSTRUCTION        */ 4
77      /* THEN GO TO THE PROPER PROCEDURE BLOCK             */ 4
78      IF SUBSTR(NUVA(PC),1,3)='1' THEN                        4
79          DO;                                                 4
80              UNSPEC(INSTR)=1; /* JUNK WOULD BE SUBSTR(NUVA(PC),4,8) 4
81              GO TO MEMORY_REF(INSTR);                        4
82          END;                                                 4
83
84      /* IT IS NOW FOR STA INSTRUCTION                      */ 4
85      UNSPEC(CK)=1; /* JUNK WOULD BE SUBSTR(NUVA(PC),4,2); 4
86      IF SUBSTR(NUVA(PC),1,3)='1' THEN                        4
87          DO;                                                 4
88              /* IF LDR, MOV- THE CONTENTS OF SIMULATED MEMORY LOCATION TO THE 4
89              /* IF LDR, MOV- THE CONTENTS OF SIMULATED MEMORY LOCATION TO THE 4

```

PAGE 4

INTRPR: PROC OPTIONS(MAIN); 1 1

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62 /* SPECIFIED SIMULATED DESTINATION ACCUMULATOR 4 78
63 REG(K)=NOVA(ADDRS); 4 78
64 GO TO SIMULATE; 4 79
END; 4 80
/* OTHERWISE STORE THE SPECIFIED SIMULATED INTO THE SPECIFIED 4 81
/* MEMORY LOCATION IN THE SIMULATED CORE 4 81
/* GO BACK TO FETCH THE NEXT INSTRUCTION 4 81
IF SUBSTR(NOVA(PC),1,3)='010'B THEN 4 81
DO; 4 82
NOVA(ADDRS)=REG(K); 4 83
GO TO SIMULATE; 4 84
END; 4 85
/* IT IS AN UNIDENTIFIABLE INSTRUCTION 4 86
PUT SKIP LIST 'INVALID INSTRUCTION ENCOUNTERED AT LOCATION' 4 86
JPC; 2 87
GO TO ENDS; 2 87
MEMORY_REF (1); 6 57
/* IT IS A JUMP INSTRUCTION 6 57
/* SET PC TO THE NEW ADDRESS AND GO BACK TO FETCH NEXT INSTRUCTION 6 57
/* FROM THAT ADDRESS 6 57
PC=ADDRS-1; 6 58
GO TO SIMULATE; 6 58
MEMORY_REF (1); 6 62
/* IT IS A JUMP INSTRUCTION 6 62
/* SAVE ADDRESS OF NEXT LOCATION IN SIMULATED ACCUMULATOR 3 AND SET 6 62
/* PC TO THE NEW ADDRESS 6 62
PC=PC+1; 6 63
REG(3)=UNSPEC(PC); 6 63
/* GO BACK TO FETCH NEXT INSTRUCTION FROM NEW ADDRESS 6 64
PC=ADDRS-1; 6 64
GO TO SIMULATE; 6 65
MEMORY_REF (2); 6 67
/* IT IS AN ISZ INSTRUCTION. CONVERT THE CONTENTS OF THE MEMORY 6 67
/* LOCATION TO A BINARY NUMBER. 6 69
UNSPEC(M)=NOVA(ADDRS); 6 69
M=M+1; 6 69
/* STORE THE UPDATED NUMBER BACK INTO THE MEMORY 6 69
RTN: NOVA(ADDRS)=UNSPEC(M); 6 72
/* IF THE NUMBER IS NOW ZERO, SET PC TO FETCH NEXT INSTRUCTION FROM 6 72
/* NEXT TO NEXT LOCATION 6 72
IF M=0 THEN 6 72
PC=PC+1; 6 73
GO TO SIMULATE; 6 74
MEMORY_REF (3); 6 74
/* IT IS A DS7 INSTRUCTION. CONVERT THE CONTENTS INTO A BINARY 6 74
/* NUMBER AND SUBTRACT 1 FROM THIS NUMBER. 6 74
UNSPEC(M)=NOVA(ADDRS); 6 74
M=M-1; 6 74
GOTO RTN; 6 74
/* IF THE BINARY VALUE FOR CARRY 6 74
/* SET THE BINARY VALUE FOR CARRY 6 74
IF SUBSTR(NOVA(PC),1,2)='01'B THEN 6 74
CARRY=1; 6 74
ELSE 6 74
IF SUBSTR(NOVA(PC),1,2)='10'B THEN 6 74

```

INTRPR: PRCC OPTIONS(MAIN):

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92      CARRY='1'B:
93      ELSE
94      IF SUBSTR(NOVA(PC),11,2)='11'B THEN
95      CARRY=-CARRY:
96      /* GET POINTERS TO THE SIMULATED SOURCE AND DESTINATION ACCUMULATORS*/
97      UNSPEC(J)='000000000000'B||SUBSTR(NOVA(PC),2,2):
98      UNSPEC(K)='000000000000'B||SUBSTR(NOVA(PC),4,2):
99      UNSPEC(INSTR)='000000000000'B||SUBSTR(NOVA(PC),6,3):
100      GOTO ARITH_LOGIC (INSTR):
101
102      ARITH_LOGIC(0):
103      /* IT IS COMPLEMENT INSTRUCTION
104      /* GET LOGICAL COMPLEMENT OF SOURCE ACCUMULATOR AND STORE IN SHIFTER*/
105      SUBSTR(SHIFTER,2,16)=-~(REG(J)):
106      /* SUPPLY THE BASE VALUE OF CARRY AS THE CARRY BIT
107      SUBSTR(SHIFTER,1,1)=CARRY:
108      GC TO SHIFT:
109
110      ARITH_LOGIC(1):
111      /* IT IS A NEGATE INSTRUCTION
112      /* GET LOGICAL COMPLEMENT OF SOURCE ACCUMULATOR
113      UNSPEC(M)=~REG(J):
114      /* ADD 1 TO LOGICAL COMPLEMENT TO GET 2'S COMPLEMENT
115      M=M+1:
116      /* STORE IT IN THE SHIFTER
117      SUBSTR(SHIFTER,2,16)=UNSPEC(M):
118      UNSPEC(M)=REG(J):
119      /* IF SOURCE ACCUMULATOR IS ZERO, SUPPLY THE COMPLEMENT OF CARRY AS
120      /* THE NEW CARRY BIT
121      IF M=0 THEN
122      SUBSTR(SHIFTER,1,1)=-CARRY:
123      ELSE
124      SUBSTR(SHIFTER,1,1)=CARRY:
125      GC TO SHIFT:
126
127      ARITH_LOGIC(2):
128      /* IT IS A MOVE INSTRUCTION
129      /* MOVE SOURCE ACCUMULATOR TO SHIFTER AND BASE VALUE OF CARRY TO
130      /* THE CARRY BIT
131      SUBSTR(SHIFTER,2,16)=REG(J):
132      SUBSTR(SHIFTER,1,1)=CARRY:
133      GC TO SHIFT:
134
135      ARITH_LOGIC(3):
136      /* IT IS AN INCREMENT INSTRUCTION
137      /* CONVERT SOURCE ACCUMULATOR TO A BINARY NUMBER
138      UNSPEC(M)=REG(J):
139      /* ADD 1 TO THE BINARY NUMBER AND STORE IT IN THE SHIFTER
140      M=M+1:
141      SUBSTR(SHIFTER,2,16)=UNSPEC(M):
142      M=M-1:
143      /*IF SOURCE ACCUMULATOR WAS -1 COMPLEMENT THE BASE VALUE OF CARRY
144      IF M=-1 THEN
145      SUBSTR(SHIFTER,1,1)=-CARRY:
146      /* OTHERWISE SUPPLY THE BASE VALUE OF CARRY AS THE CARRY BIT
147      ELSE
148      SUBSTR(SHIFTER,1,1)=CARRY:
149      GC TO SHIFT:
150
151      ARITH_LOGIC(4):
152      /* IT IS AN APC INSTRUCTION

```


INTRPR: PRC OPTIONS(MAIN):

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147 ARITH_LOGIC(7):
/* IT IS AN AND INSTRUCTION
/* AND THE SOURCE AND DESTINATION ACCUMULATORS TO EACH OTHER
/* STORE THE RESULT IN SHIFTER
SUBSTR(SHIFTER,2,16)=REG(J)REG(K);
/* SUPPLY BASE VALUE OF CARRY AS THE CARRY BIT
SUBSTR(SHIFTER,1,1)=CARRY;
SHIFT:
/* PERFORM THE SHIFTING OF BITS IN SHIFTER AS SPECIFIED BY
/* BITS 9 AND 10 OF THE INSTRUCTION
/* SIMULATION OF LEFT ROTATION
IF SUBSTR(NOVA(PC),9,2)='01'B THEN
DC;
STORE=SUBSTR(SHIFTER,1,1);
SUBSTR(SHIFTER,1,16)=SUBSTR(SHIFTER,2,16);
SUBSTR(SHIFTER,17,1)=STORE;
GC TO LOAD;
ENC;
/* SIMULATION OF RIGHT ROTATION
IF SUBSTR(NOVA(PC),9,2)='10'B THEN
DC;
STORE=SUBSTR(SHIFTER,17,1);
SUBSTR(SHIFTER,2,16)=SUBSTR(SHIFTER,1,16);
SUBSTR(SHIFTER,1,1)=STORE;
GC TO LOAD;
ENC;
/* SIMULATION OF SWAPPING
IF SUBSTR(NOVA(PC),9,2)='11'B THEN
DC;
STORE=SUBSTR(SHIFTER,2,8);
SUBSTR(SHIFTER,2,8)=SUBSTR(SHIFTER,10,8);
SUBSTR(SHIFTER,10,8)=STORE;
ENC;
LOAD:
/* IF NO-LOAD BIT IN THE INSTRUCTION IS OFF, LOAD THE SHIFTER OUT-
/* PUT IN THE DESTINATION ACCUMULATOR AND CARRY BIT INTO CARRY
IF SUBSTR(NOVA(PC),13,1)='0'B THEN
DC;
REG(K)=SUBSTR(SHIFTER,2,16);
CARRY=SUBSTR(SHIFTER,1,1);
END;
SKIP:
/* PERFORM CHECKING FOR DIFFERENT SKIP OPTIONS
/* SIMULATION OF SKP OPTION OF SKIPPING
IF SUBSTR(NOVA(PC),14,3)='001'B THEN
DC;
PC=PC+1;
RETURN;
ENC;
/* SIMULATION OF SZC OPTION OF SKIPPING
IF SUBSTR(NOVA(PC),14,3)='010'B THEN
DC;
IF SUBSTR(SHIFTER,1,1)='0'B THEN
PC=PC+1;
RETURN;
ENC;
/* SIMULATION OF SNC OPTION OF SKIPPING

```

INTRPR: PROC OPTIONS(MAIN);

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INTRPR: PROC OPTIONS(MAIN);

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INTRPR: PROC OPTIONS(MAIN);

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INTRPR: PROC OPTIONS(MAIN);

```

185 IF SUBSTR(INOVA(PC),14,3)='011'B THEN
186 DC;
187 IF SUBSTR(SHIFTER,1,1)='1'B THEN
188 PC=PC+1;
189 RETURN;
190 ENC;
191 UNSPEC(M)=SUBSTR(SHIFTER,2,16);
192 /* SIMULATION OF SZR OPTION OF SKIPPING
193 IF SUBSTR(INOVA(PC),14,3)='100'B THEN
194 DC;
195 IF M=J THEN
196 PC=PC+1;
197 RETURN;
198 ENC;
199 /* SIMULATION OF SNR OPTION OF SKIPPING
200 IF SUBSTR(INOVA(PC),14,3)='111'B THEN
201 DC;
202 IF M=0 THEN
203 PC=PC+1;
204 RETURN;
205 ENC;
206 /* SIMULATION OF SEC OPTION OF SKIPPING
207 IF SUBSTR(INOVA(PC),14,3)='110'B THEN
208 DC;
209 IF (M=0) || SUBSTR(SHIFTER,1,1)='0'B THEN
210 PC=PC+1;
211 RETURN;
212 ENC;
213 /* SIMULATION OF SDN OPTION OF SKIPPING
214 IF SUBSTR(INOVA(PC),14,3)='111'B THEN
215 DC;
216 IF (M=0) || SUBSTR(SHIFTER,1,1)='0'B THEN
217 PC=PC+1;
218 RETURN;
219 END ARITH;
220 ADPSR:
221 PROC;
222 /* CONVERT DISPLACEMENT TO BINARY NUMBER
223 UNSPEC(M)=00000000B || SUBSTR(INOVA(PC),9,8);
224 /* IF ABSOLUTE ADDRESSING, USE DISPLACEMENT AS EFFECTIVE ADDRESS
225 IF SUBSTR(INOVA(PC),7,2)='00'B THEN
226 DC;
227 ACDS=M;
228 GO TO TYPE;
229 ENC;
230 /* IF THE DISPLACEMENT IS NEGATIVE, IT IS IN 2'S COMPLEMENT
231 IF SUBSTR(INOVA(PC),9,1)='1'B THEN
232 UNSPEC(M)=11111111B || SUBSTR(INOVA(PC),9,8);
233 /* IF RELATIVE ADDRESSING, ADD DISPLACEMENT AND PC TO GET EFFECTIVE
234 /* ADDRESS
235 IF SUBSTR(INOVA(PC),7,2)='01'B THEN
236 DC;
237 ACDS=PC+M;
238 GO TO TYPE;
239 ENC;
240 /* IF INDEXED ADDRESSING, ADD INDEX REGISTER & DISPLACEMENT TO GET
241 /*
242
243
244
245
246
247
248
249
250
251
252
253
254

```

INTRPR: PRC OPTIONS(MAIN):

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231      /* EFFECTIVE ADDRESS
232      IF SUBSTR(NOVA(PC),7,2)='10'B THEN
233      UNSPEC(N)=REG(2);
234      ELSE
235      UNSPEC(N)=REG(3);
236      ADDR=M*N;
237      /* IF INDIRECT ADDRESSING
238      /* FETCH THE CONTENTS OF EFFECTIVE ADDRESS
239      TYPE: IF SUBSTR(NOVA(PC),6,1)='1'B THEN
240      DO:
241      UNSPEC(M)='0'8||SUBSTR(NOVA(ADDR),2,15);
242      /* CHECK FOR AUTOINDEXING
243      /* AUTO-INCREMENTING SIMULATION
244      IF ADDR<=16&ADDR->23 THEN
245      DO:
246      M=M+1;
247      WORK=UNSPEC(M);
248      SUBSTR(NOVA(ADDR),2,15)=SUBSTR(WORK,2,15);
249      END;
250      /* AUTO-DECREMENTING SIMULATION
251      ELSE
252      IF ADDR<=24&ADDR->31 THEN
253      DO:
254      M=M-1;
255      WORK=UNSPEC(M);
256      SUBSTR(NOVA(ADDR),2,15)=SUBSTR(WORK,2,15);
257      END;
258      /* IF THE CONTENTS AGAIN SPECIFY INDIRECT ADDRESSING, REPEAT THE
259      /* CYCLE USING THE CONTENTS OF EFFECTIVE ADDRESS AS NEW ADDRESS
260      IF SUBSTR(NOVA(ADDR),1,1)='1'B THEN
261      DO:
262      UNSPEC(ADDR)='0'8||SUBSTR(NOVA(ADDR),2,15);
263      GO TO BACK;
264      END;
265      /* OTHERWISE USE CONTENTS AS THE FINAL EFFECTIVE ADDRESS
266      ADDR=M;
267      END;
268      /* IF COMPUTED ADDRESS NOT WITHIN THE SCOPE OF OBJECT MODULE,
269      /* PRINT OUT A WARNING MESSAGE
270      IF ADDR<=LOAD_POINT|ADDR<SAVE THEN
271      PUT LIST('OUT_OF_PROGRAM_ADDRESS REFERENCE AT INS
272      TRUCTION'||PC);
273      END ADDR;
274      I_O_ROUTINE: PROC;
275      IF NOVA(PC)='0110000001001000'B THEN
276      RETURN;
277      IF NOVA(PC)='011001101001001'B|NOVA(PC)='01100111000
278      100'B THEN
279      DC PC=PC+1;
280      RETURN;
281      ENC;
282      IF NOVA(PC)='0110101001001001'B THEN
283      DO:
284      PUT LIST(REG(1));
285      RETURN;
286      END;
287      IF NOVA(PC)='0111001001001001'B THEN

```

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INTRPR: PRCC OPTIONS(MAIN):

```

273          DC;
274          PUT LIST(REG(2));
275          RETURN;
276          END;
277          IF NOVA(PC)='0111000101001000'B THEN
278          DO;
279          GET LIST(REG(2));
280          RETURN;
281          END;
282          PUT SKIP LIST('I/O INSTRUCTION BEING BYPASSED AT LOCATION
          *IIPC);
283          END I_O_ROUTINE;
284
          ENDS;
          /* PRINT OUT THE SIMULATED ACCUMULATORS, SHIFTER, CARRY, AND ALL THE*/
          /* MEMORY
          PUT SKIP(2)DATA(PC);
          PUT SKIP(2)DATA(REG);
          PUT SKIP(2)DATA(SHIFTER,CARRY);
          PUT SKIP;
          DO K=SAVE TO LOAD_POINT-1;
          PUT DATA(NOVA(K));
          END;
          ENF;
          END INTRPR;

```

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3 313
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Appendix II

TESTING RUNS


```

CORE_SIZE= 4096
NCVA(0)=0000100000000001'B;
NCVA(1)=0101100000000101'B;
NCVA(2)=0001100000000110'B;
NCVA(3)=0000010000000101'B;
NCVA(4)=0110011000111111'B;
NCVA(5)=0000000000000000'B;
NCVA(6)=0000000000010000'B;

FCBC CHECK
LCAL_POINT= 0 START_POINT= 0 RESTART_ADDRESS= 256;
JSR ABC
STA SAR
DSZ ONE
JMP @AB
HALT
AR: 0
ONE: 10
.END

END OF ECHO CHECK
4
JCB HALTED AT LOCATION
PC= 4;

```

```

REG(0)=0100010000000000'B
REG(1)=01110110101010'B
REG(2)=0100100000100000'B
REG(3)=0000000000000001'B;
CARRY=0'B;
NOVA(0)=0001010011000101'B;
NOVA(1)=0000100000000001'B;
NOVA(2)=0001100000000011'B;
NOVA(3)=0000010000000101'B;
NOVA(4)=0110011000111111'B;
NOVA(5)=0000000000000000'B;
NOVA(6)=0000000000000000'B;

```



```

00470 000701 LDA 2,X
00471 000702 STA 2,SV
00472 050713 STA 3,SAV
00473 135000 MOV 1,3
00474 175100 JLP:
00475 175100 MOV 3,3
00476 024705 LDA 1,C4
00477 167400 AND 3,1
00500 030710 LDA 2,5X
00501 147300 ADD 2,1
00502 030711 LDA 2,SV
00503 040703 STA 0,SAV+1
00504 023705 LDA 2,X
00505 112414 SUB# 0,2,54R
00506 050403 JMP +3
00507 030705 LDA 2,A
00510 147400 AND 2,1
00511 171800 MOV 3,2
00512 004407 JSR PRT
00513 020703 LDA 0,SAV+1
00514 155000 MOV 2,3
00515 030676 LDA 2,SV
00516 151405 INC 2,2,SNR
00517 000404 JMP 0LP
00520 175100 MOV 3,3
00521 175100 MOV 3,3
00522 175100 MOV 3,3
00523 053670 STA 2,SV
00524 000750 JMP LOP+2
00525 030673 LDA 2,F
00526 024667 LDA 1,B
00527 151400 INC 2,2
00530 132430 SC 1,2
00531 080716 JMP DN
00532 050656 STA 2,F
00533 024663 LDA 1,BLX
00534 004405 JSR PRT
00535 034404 JSR PRT
00536 024653 LDA 1,X
00537 044654 STA 1,SV
00540 000721 JMP RET
00541 063511 SKPBE ITO
00542 000777 JMP --1
00543 065111 DJAS 1,ITD
00544 001400 JMP 0,3
00545 023610 SKPDN TTI
00546 000777 JMP --1
00547 070510 DIAS 2,TTI
00550 071111 DJAS 2,TTD
00551 001400 JMP 0,3
00552 024700 LDA 1,STA
00553 024700 JSR PRT
00554 024663 LDA 1,BEL
00555 000764 JSR PRT
00556 000763 JSR PRT
00557 000762 JSR PRT
00560 150400 SUB 2,2
00561 151430 INC 2,2
00562 150400 NEG 2,2
00563 050625 STA 2,F

```

; SAVE CIRC ADDR
 ; SHIFT CHARACTER
 ; LOAD MASK
 ; SAVE BITS 13-15
 ; MAKE THE NUMBER
 ; LOAD CHAR COUNTER
 ; SAVE ACC
 ; LOAD FIRST CHAR NO.
 ; IF NOT FIRST CHARACTER
 ; SKIP AHEAD
 ; GET RID OF BIT 13
 ; RESTORE ACC
 ; LAST CHAR OF GP?
 ; SKIP IF YES
 ; CIRCULAR SHIFT 3 BITS
 ; LAST CHAR ON LINE?
 ; YES GO TO DN
 ; PRINT TWO BLANKS
 ; WAIT UNTIL PRINTER FREE
 ; OUTPUT AC1
 ; RETURN WHERE CALLED
 ; RETURN

```

---
00564 024615
00565 004754
00566 024612
00567 004752
00570 000630
00571 003077
00571 000420
LDA 1,CR
JSR PRT
LDA 1,LF
JSR PRT
JMP START
HALT
.END START

```

```

---
MODE: 5400, 5715
000420 000012 177772 000015 000044 000067 000017 000405 000572 000001
000410 000001 177772 177772 000060 177772 000061 000011 000040 000007
000420 024762 004520 004520 005110 102400 024771 004520 034756 173400
000430 132432 000406 000406 101120 101120 101120 143000 000767 034751
000440 173400 000405 000405 004740 004740 004740 000760 101400 024732
000450 054737 004470 004470 024746 004466 034733 030734 050735 152400
000460 050730 034724 034724 151005 000411 025400 116432 000464 175400
000470 030721 050722 050722 050712 050712 135000 175100 024705 167400
000480 030710 030710 147400 030711 040703 020705 112414 000403 030705
000490 147400 171400 171400 004427 000703 155000 030676 151405 000406
000500 175100 175100 175100 175100 050670 000752 030663 024667 151400
000510 132432 000716 000716 050656 024663 004405 004404 024653 044654
000520 000721 063511 063511 000777 000777 001400 063610 000777 070510
000530 071111 001400 001400 024632 004766 024643 004764 004763 004762
000540 152400 151400 151400 154400 050625 024615 004754 024612 004752
000550 000630 063077 063077

```


NOVA(313)='0101000111010010'8;
 NOVA(314)='0101100111001011'8;
 NOVA(315)='10111010000000'8;
 NOVA(316)='11110101010000'8;
 NOVA(317)='11111001000000'8;
 NOVA(318)='00100011100101'8;
 NOVA(319)='11101110000000'8;
 NOVA(320)='00100011001010'8;
 NOVA(321)='11001100000000'8;
 NOVA(322)='00110011101001'8;
 NOVA(323)='0100001100011'8;
 NOVA(324)='00100011100101'8;
 NOVA(325)='10101010001100'8;
 NOVA(326)='00000010001011'8;
 NOVA(327)='00110011100101'8;
 NOVA(328)='11001110000000'8;
 NOVA(329)='11100100000000'8;
 NOVA(330)='0001000001111'8;
 NOVA(331)='00100011101101'8;
 NOVA(332)='11011000000000'8;
 NOVA(333)='00100011111110'8;
 NOVA(334)='11010010000101'8;
 NOVA(335)='0000100001110'8;
 NOVA(336)='11111001000000'8;
 NOVA(337)='11111001000000'8;
 NOVA(338)='11111100000000'8;
 NOVA(339)='01100011110000'8;
 NOVA(340)='00000011101010'8;
 NOVA(341)='0011001111011'8;
 NOVA(342)='000000111111'8;
 NOVA(343)='11100100000000'8;
 NOVA(344)='10110110001010'8;
 NOVA(345)='000011100110'8;
 NOVA(346)='011001101110'8;
 NOVA(347)='0010001011011'8;
 NOVA(348)='000100000101'8;
 NOVA(349)='000100000100'8;
 NOVA(350)='001010101011'8;
 NOVA(351)='0100101110110'8;
 NOVA(352)='000000111001'8;
 NOVA(353)='01100110100101'8;
 NOVA(354)='000000111111'8;
 NOVA(355)='01101010100101'8;
 NOVA(356)='00000010000000'8;
 NOVA(357)='01100111001000'8;
 NOVA(358)='000000111111'8;
 NOVA(359)='0110010101000'8;
 NOVA(360)='01100100100101'8;
 NOVA(361)='00000110000000'8;
 NOVA(362)='00101001101000'8;
 NOVA(363)='0000011110110'8;
 NOVA(364)='0010101010011'8;
 NOVA(365)='00001001111000'8;
 NOVA(366)='00001011110011'8;
 NOVA(367)='00011011110010'8;
 NOVA(368)='11101000000000'8;
 NOVA(369)='11100100000000'8;
 NOVA(370)='11100100000000'8;
 NOVA(371)='0101101101101'8;
 NOVA(372)='00101011000101'8;

NOVA(286)='0000000111110111'B; NOVA(287)='00111001111101001'B; NOVA(288)='11111011100000
 100'B; NOVA(289)='000000010000010101'B; NOVA(290)='0101100111110011010'B;
 NOVA(291)='010000011111001010'B; NOVA(292)='1000010100000000'B; NOVA(293)='00000000111110
 000'B; NOVA(294)='1000001100000000'B; NOVA(295)='001010011101101010'B;
 NOVA(296)='0101100111011111'B; NOVA(297)='0000100100110000'B; NOVA(298)='00101000111010
 110'B; NOVA(299)='0000100100110110'B; NOVA(300)='0011100111011011'B;
 NOVA(301)='0011100111011010'B; NOVA(302)='0101000111011011'B; NOVA(303)='110101010000
 000'B; NOVA(304)='0101000111011000'B; NOVA(305)='0011100111010100'B;
 NOVA(306)='1101010000000101'B; NOVA(307)='00000001000001001'B; NOVA(308)='001010110000
 000'B; NOVA(309)='100111010001101010'B; NOVA(310)='0000000100110100'B;
 NOVA(311)='1111101100000000'B; NOVA(312)='0011000111010001'B; NOVA(313)='01010000111010
 111'B; NOVA(314)='01011001110101011'B; NOVA(315)='1011101000000000'B;
 NOVA(316)='1111101001000000'B; NOVA(317)='1111101001000000'B; NOVA(318)='0010100111100
 101'B; NOVA(319)='1110111100000000'B; NOVA(320)='0011000111001010'B;
 NOVA(321)='1110111000000000'B; NOVA(322)='0011000111001001'B; NOVA(323)='010000011100
 011'B; NOVA(324)='0010000111000101'B; NOVA(325)='10010101000001100'B;
 NOVA(326)='0000000100000000'B; NOVA(327)='0011000111000101'B; NOVA(328)='110011110000
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 NOVA(331)='0000000100110111'B; NOVA(332)='1101101000000000'B; NOVA(333)='001100011011
 110'B; NOVA(334)='1101001100100101'B; NOVA(335)='0000000100000110'B;
 NOVA(336)='1111101001000000'B; NOVA(337)='1111101001000000'B; NOVA(338)='111110100100
 000'B; NOVA(339)='1010000110110000'B; NOVA(340)='0000000111101010'B;
 NOVA(341)='0011011011011011'B; NOVA(342)='0010100110110111'B; NOVA(343)='110100110000
 000'B; NOVA(344)='1101010001100110'B; NOVA(345)='0000000111000110'B;
 NOVA(346)='0101000110110110'B; NOVA(347)='0010100110110011'B; NOVA(348)='000010010010
 111'B; NOVA(349)='0001001001000100'B; NOVA(350)='0010100110101011'B;
 NOVA(351)='0100110110011001'B; NOVA(352)='0000000111010001'B; NOVA(353)='0110011101001
 01'B; NOVA(354)='0000000111111111'B; NOVA(355)='0110101001001001'B; NOVA(356)='000000011111
 111'B; NOVA(357)='0110011100010000'B; NOVA(358)='00000001111101001'B;
 NOVA(359)='0111000101001000'B; NOVA(360)='0111001001001001'B;
 NOVA(361)='00000001000000'B; NOVA(362)='0010100110011000'B; NOVA(363)='0000100111101000'B;
 NOVA(364)='0010100110100011'B; NOVA(365)='0000100111101000'B;
 NOVA(366)='0001101111111111'B; NOVA(367)='0000100111110010'B; NOVA(368)='110101010000
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 NOVA(371)='0101000110010101'B; NOVA(372)='0010100110001101'B; NOVA(373)='000010011101
 010'B; NOVA(374)='0010100110001101'B; NOVA(375)='0000100111101010'B;
 NOVA(376)='0000000100000000'B; NOVA(377)='0110011000111111'B; NOVA(378)='00000001000000

A SOFTWARE SIMULATOR TO HOST
THE DATA GENERAL NOVA ON THE IBM 360

by

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AN ABSTRACT OF A MASTER'S REPORT

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MASTER OF SCIENCE

Department of Computer Science

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In order to use programs originally written for the Data General Nova on the IBM 360, a software simulator has been designed. This simulator consists of a single program written in IBM System 360 PL/1.

The input to the simulator is the Nova Object Code, written as 16 digit binary number. The simulator, when invoked, behaves as the central processor of the Data General Nova. It reads the object code of the Data General Nova into a variable size simulated memory and then starts simulating the Nova central processor by interpreting and executing the Nova Object Code in terms of the available 360 facilities.

The simulator is capable of simulating the Nova central processor for all the different instructions of the Nova, except the Input/Output instructions.

The report consists of a brief description of the Data General Nova, a detailed description of the working of the simulator, instructions on how to use the simulator, a discussion of the testing and debugging scheme of the simulator and a brief discussion on making the simulator more efficient.