RESEARCH ARTICLE | SEPTEMBER 21 2007

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Rev. Sci. Instrum. 78, 094702 (2007)
https://doi.org/10.1063/1.2785029

An auto-incrementing nanosecond delay circuit

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(Received 5 July 2007; accepted 25 August 2007; published online 21 September 2007)

We describe a circuit that acts as an auto-incrementing delay. The circuit allows the user to adjust the total number of delays in a cycle, the incremental delay value, and the amount of time that is spent at each delay step. The circuit is stand-alone, yet is readily interfaced to data acquisition systems. Depending on the delay chip used and the number of steps required, the delay step can be as short as 250 ps or as long as 640 ns. The circuit has been used to control the temporal separation between pulses from independent lasers. This was instrumental in our measurement of population dynamics in an optically excited three-level ladder system. © *2007 American Institute of Physics.* [DOI: 10.1063/1.2785029]

I. INTRODUCTION

Increasing requirements on timing precision and high-speed logic decisions in modern experiments demand the development of flexible control devices. Computer control using commercial hardware and software is a possible solution. However, for many applications a stand-alone hardware device can be more simply and conveniently integrated into an experiment. The auto-stepping delay module discussed here delays an input transistor-transistor logic (TTL) pulse through successively longer times. Both the total number of delays in a cycle and the increment in delay time are switch selectable, making the device extremely flexible. In this article we describe the delay module and demonstrate its use in a coherent excitation experiment in which one optical pulse is delayed by a variable amount with respect to a second optical pulse.

II. HARDWARE DESCRIPTION

A block diagram for the circuit is shown in Fig. 1. At the heart of the circuit is the DS1023 8-bit programmable timing chip, labeled "delay" in the figure. As inputs, this chip takes a TTL-level timing signal which is to be delayed, and a parallel 8-bit TTL level signal that tells the chip how much of a delay to create. As outputs, the DS1023 has the delayed TTL signal and a reference TTL pulse (unused in this application). The 8-bit signal is a binary number, X, from 0 to 255, and this number gives the total delay of the chip through the expression

$$\tau_{\text{total}} = \tau_0 + \tau X, \tag{1}$$

where τ_0 is the fixed propagation time of a signal through the chip, typically 16.5 ns, and τ is the unit delay of the chip. The DS1023 comes in five varieties, with τ=0.25, 0.5, 1.0, and 5.0 ns, respectively. For our application, the 5.0 ns version was the most suitable. In our implementation of the DS1023, X is automatically incremented using the combination of a clock and a binary counter. For maximum flexibility, the counter output passes through a "control logic module" which is nothing more than a hardware AND mask made up of a bank of 8 DIP switches. The AND mask is used to control the delay step time, the increment in delay for each step, and the number of steps in a cycle. As shown in Fig. 2, the switches are arranged such that any of the bits from the counter can be passed through to the DS1023 (at the mask position occupied by a "1") or replaced by a logical 0. The number of least significant bits (LSb) in the mask set to 0 (the "cleared" bits) gives the delay increment, given by $2^n\tau$, where n is the number of bits cleared. The cleared LSb also give the "dwell time" at each delay, t_{step}, using the formula $t_{\text{step}}=2^nT$, where T is the clock period. The number of most

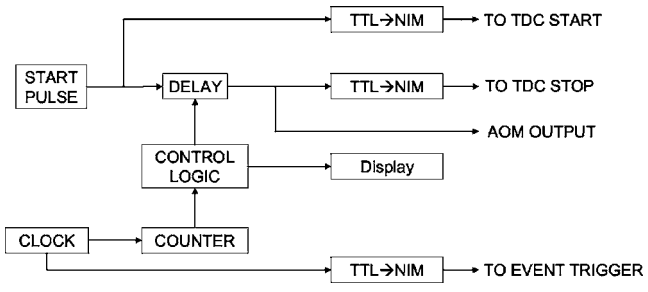

FIG. 1. Block diagram of the auto-incrementing delay circuit.

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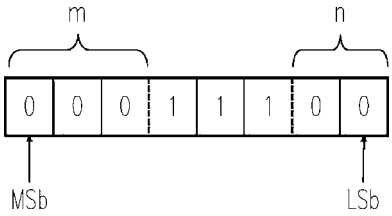

FIG. 2. The 8-bit hardware AND mask used to control delay increment, duration, and number of steps.

significant bits (MSb) cleared using the mask gives the total number of delays per cycle. That is,

$$N = 2^{8-(m+n)}, \tag{2}$$

where m is the number of cleared MSb, and $n+m \leq 8$. The total cycle time is then Nt_{step}. For example, in one of our applications, it was desirable to have 32 values of delay, to increment the delay by 10 ns at each step, and to dwell for 10 s at each delay. Then, $m+n=3$ so that N takes the desired value of $2^5=32$. We used the version of the DS1023 for which $\tau=5$ ns. Therefore, $n=1$, which means that $m=2$. In order for the dwell time at each delay to be 10 s, we set $T=5.0$ s. Thus, the least significant bit and the two most significant bits were zeroed, and the rest of the bits from the counter were sent through to the DS1023. That is, the bit pattern appearing on the mask would be "00111110," where the right-most bit is the least significant. The five 1's indicate that there will be 2^5 sequential delays, while the single zeroed bit on the right indicates that every other pulse from the clock will matter, giving a $2\times\tau$ delay increment and a 10 s period for each delay. The total cycle time is 32×10 s=320 s.

In our application, a TTL pulse, labeled "START," is generated by our PC-controlled data acquisition system.[1] (It should be pointed out that the otherwise flexible pulse generating card[2] contained in our data acquisition computer is not capable of pulse delays less than 50 ns.) After passing through a pair of inverters to "clean up" the TTL signal,

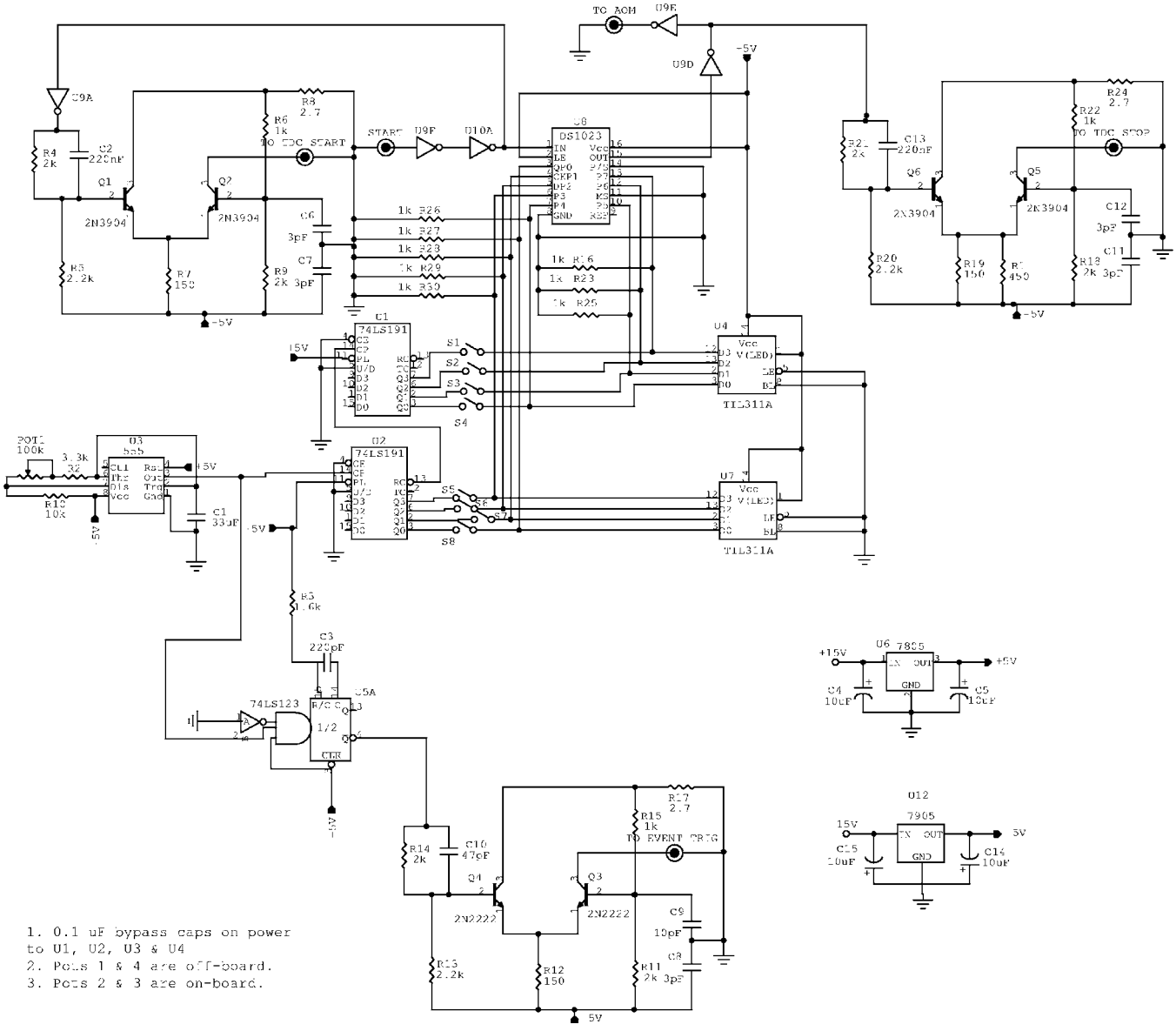

FIG. 3. Schematic diagram of the sequentially stepped nanosecond delay circuit.

the pulse is sent both to the DS1023 (U8) and to one of the TTL-to-NIM converters,[3] the output of which, labeled "TO TDC START," is used as the start signal for a time-to-digital converter (TDC). Figure 3 shows the actual schematic for the circuit. The clock circuit is based on the 555 timer chip (U3). For flexibility in choosing T, potentiometer POT1 can be adjusted to give clock periods ranging from $0.5\ \mathrm{s} \leq T \leq 7.0\ \mathrm{s}$. The clock output is split, with one part going to the clock input of a pair of 4-bit counters (U1 and U2) that generate X for the DS1023 after passing through the switches (S1–S8) that make up the AND mask described above. Following the mask, X also goes to a pair of LED displays (U4 and U7) that provide a visual indication of which delay step is being implemented. The other part of the clock output goes to a one-shot (to shorten its duty cycle) and from there to a second TTL-to-NIM converter. The converter's output, labeled "TO EVENT TRIGGER," is useful to synchronize a data acquisition system to the clock. The delayed TTL pulse, from pin 15 of the DS1023, is output as a TTL signal (labeled "TO AOM") and is used in our application to turn on the rf to an acousto-optic modulator. The delayed output is also converted to NIM and sent to our TDC's STOP.

III. APPLICATION EXAMPLE—STIRAP

Stimulated Raman adiabatic passage (STIRAP) is a coherent excitation scheme that has many potential applications.[4] Unlike other coherent excitation processes such as one- or two-photon π-pulses, STIRAP is relatively insensitive to variations in laser intensity, thus making it a potentially robust excitation scheme. In a three-level ladder system, one of the hallmarks of this excitation process is that peak excitation efficiency occurs when the pulse of laser light connecting the upper two levels (the "Stokes" pulse, referred to as "L2") in the ladder occurs before the pulse of laser light connecting the lower two levels (the "pump" pulse, referred to as "L1"). We wished to measure the populations of all three levels in the ladder system as a function of time, and as a function of the delay between the pump and Stokes pulses, using charge transfer as a probe of these populations.[5,6] The programmable delay circuit described in this article provides a convenient means of stepping through a range of delays.

The system under study is atomic ^{87}Rb. The "rungs" of the ladder are the $5s_{1/2},F=2$; $5p_{3/2},F=3$; and $4d_{5/2}$ levels in ^{87}Rb. (The hyperfine levels in the $4d_{5/2}$ level were unresolved.) The approximate wavelengths corresponding to L1 and L2 for this system are 780 and 1529 nm, respectively. The pulses are made by directing light from two separate cw diode lasers through corresponding acousto-optic modulators (AOMs). The rf signals to the AOMs are turned on and off with TTL-controlled rf switches.[7] A common TTL signal, originating from our data acquisition system, is split, with one branch going to a fixed delay before triggering the rf switch corresponding to L1, and the other branch going to the variable delay circuit described in this article. The output of the variable delay circuit triggers the rf switch corresponding to L2. Figure 4 shows the relative timing of the Stokes and pump laser pulses. The pulses are plotted as Rabi frequency (which is proportional to the square root of the intensity) versus time, for five selected values of delay. The data in this figure were taken by directing some portion of the optical beams emerging from their respective AOMs onto photodiodes, silicon-based in the case of L1, and InGaAs-based in the case of L2. The structures seen in the pulses, particularly the overshoot in the case of L1, are caused by impedance mismatches between the photodiodes and their amplifiers, and are not relevant to this discussion.

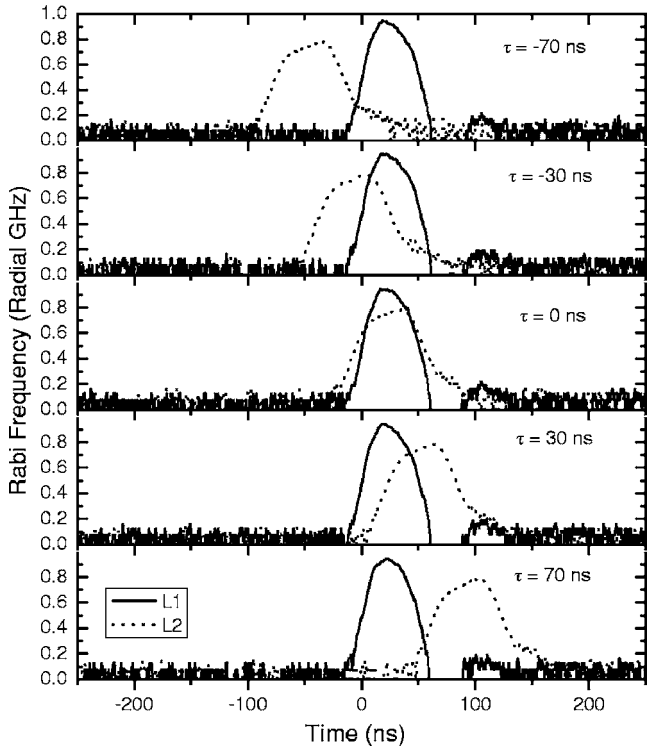

FIG. 4. Plots of the Rabi frequencies of L1 and L2 vs time for five different delays.

In the experiment, we set the timing circuit's mask to have 16 delay steps, with delays ranging from 0 to 150 ns, with each delay step lasting approximately 6 s. The fixed delay of L1 was set such that the two pulses were maximally overlapped in time for the eighth delay step. In the subset of data shown in Fig. 4, one can clearly see the steadily increasing delay of L2 with respect to the fixed delay of L1. Full experimental details of the data-taking apparatus, as well as the results of the STIRAP experiment, are given in Refs. 5 and 6.

IV. SUMMARY

The auto-stepping variable delay circuit described in this article has found many uses in our laboratory. Because it steps through a range of delays without the assistance of a computer, it is both portable and simple to operate. The AND mask allows the user to conveniently adjust both the number of delay steps in a cycle and the dwell time at each delay. One can choose between the TTL level pulses output by the delay chip, or the NIM level signals available from the on-board TTL-to-NIM converters. The DS1023 is available only

in a surface mount package. However, in order to facilitate changing from one delay base to another, we have mounted our delay chips on surface mount-to-DIP converters, and soldered a DIP socket on the PC board. It is therefore trivial for us to change from a minimum delay step of 5 ns to, for example, 250 ps. We have found the circuit to be convenient, easy to use, and inexpensive to build. Artwork for the circuit board layout is available upon request.

ACKNOWLEDGMENTS

This work was supported by the Chemical Sciences, Geosciences, and Biosciences Division, Office of Basic Energy Sciences, Office of Science, U.S. Department of Energy.

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