RADIO FREQUENCY TRANSISTORS

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TABLE OF CONTENTS

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INTRODUCTION

In recent years, transistors have been developed for applications in L-band and S-bands. Low noise, high power, and high efficiency microwave transistors are supplied by many manufacturers. Fifty watts at 0.5 GHz with 6dB gain and 70 percent collector efficiency, 10 watts at 1.2 GHz with 10dB gain and 50 percent collector efficiency and 7 watts at 2.2 GHz with 6dB gain and 40 percent collector efficiency are available. Noise figures in the order of 4 to 5 dB at 2 GHz have been reported. It is reasonable to believe that RF transistor power-handling capability will be boosted, power gain will be increased and noise figures will be improved in the near future.

Some important fundamental concepts and performance characteristics of RF transistors are described in the first two chapters. Large-signal RF transistors will be emphasized because small-signal RF transistors can be well characterized by the use of scattering parameters. In Chapter 3, power waves and scattering matrices defined by power waves are introduced. Methods of measuring scattering parameters for two-ports or transistors are presented in Chapter 4. A small-signal RF transistor amplifier designed by the use of scattering parameters is introduced in Chapter 5.

Large-signal RF transistors are normally characterized in a given circuit for a specific application. But if the dynamic input and output impedance of the RF transistors are determined with slotted-line or vector voltmeter measure-

ment techniques, the large-signal transistor circuits still can be properly designed. Hence, a setup for measurement of an RF transistor's dynamic impedance is given in Chapter 6. Some useful microwave design techniques for both large-signal and small-signal applications are also introduced in Chapter 6.

All materials in this report apply to a frequency range of 0.5 GHz to 3GHz. Both microstrip properties and the design of microwave integrated circuits are very important in designing RF transistor circuits. But these topics are not within the scope of this report.

Chapter I

RF TRANSISTOR BASIC CONSTRUCTION

Introduction

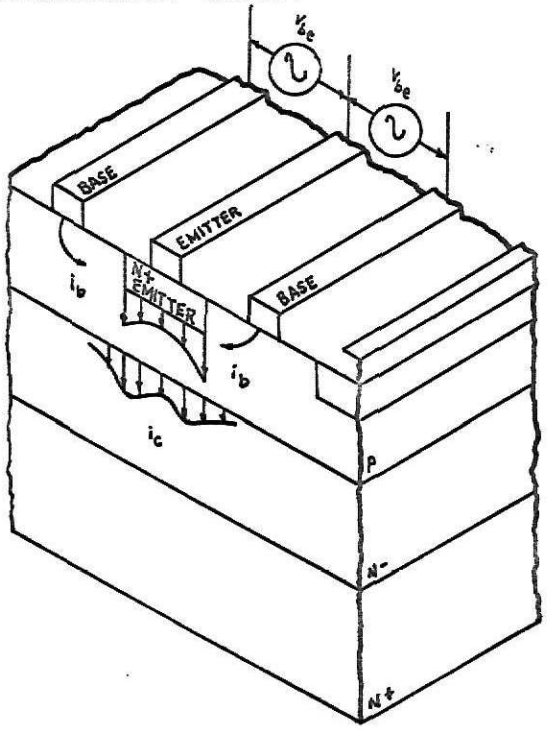
It seems to the author that an understanding of the basic construction of an RF transistor is very helpful in designing transistor circuits. From the basic concepts of device construction, the circuit designer will better understand the characteristics of RF transistors, and how transistor parameters affect each other in combination with circuit trade-offs. In this chapter, the two most widely used construction methods are introduced. A comparison between them is given. The RF transistor parameters and trade-offs in circuit design will be discussed in the next chapter.

Fundamental concepts

Figure 1-1 shows that base current i_b has to go through the region under the emitter. The more narrow the base width is, the higher the lateral sheet resistance of the structure will be; or the higher the effective base resistance is, the more voltage drop there will be for a given base drive. Furthermore, under the emitter, away from the base-contact area, less emitter base voltage is available and the current turn-on is less as well. What is more, as frequency increases the three-dimensional series resistance with a shunt capacitance will act as a low-pass filter. This built-in low-pass-filter allows less base-emitter junction drive.

Figure 1-1 shows how the current distribution looks at one frequency for a simple transistor model. Figure 1-2 shows a coarse geometry as compared to a finer geometry. For the same drive at the same frequency, the current distributions would be as shown in the figures. For a given physical area, there is much more active area in the transistor of Figure 2b. The reason for this is that the transistor of Figure 2b has a finer geometry. The greater active area gives more power-frequency capability. Based on this fundamental concept, both interdigitated transistors and overlay transistors are designed to increase active-to-physical area ratio in a given area.

Figure 1-1a.
Transistor current distribution for a simple transistor model



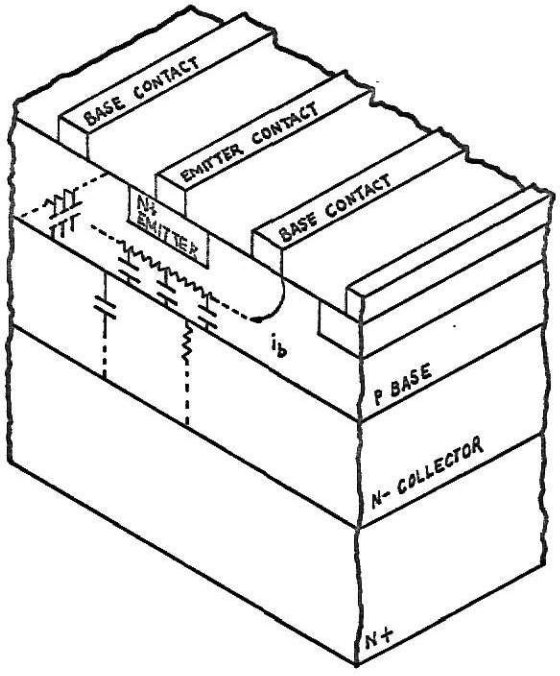


Figure 1-1b. Built-in low-pass-filter.

Figure 2. How finer geometry increases active area. For a given physical area, Figure 2a has less active area because of its coarse geometry.

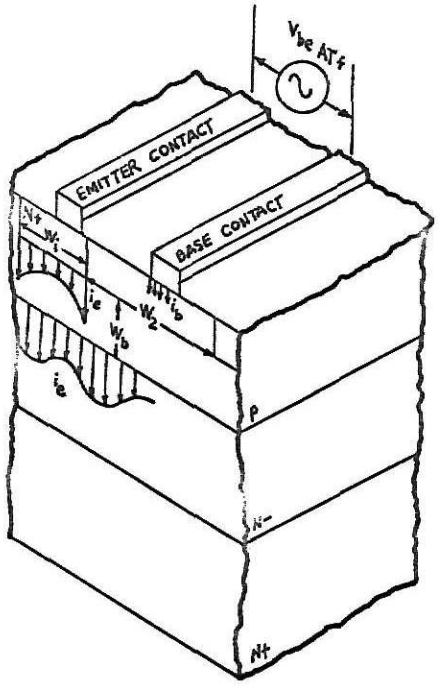
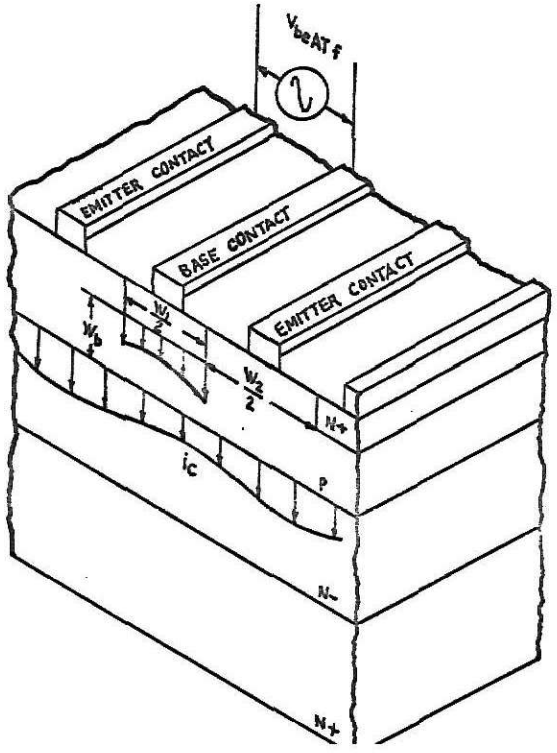


Figure 2a. A relatively coarse geometry.

Figure 2b. A relatively fine geometry.



The equation (1-1) shows that with suitable scaling transistors can be enlarged to increase power-handling capability without deterioration of frequency response.[3]

$$f_{max} = (PG)^{1/2} F = \frac{1}{4\pi} \left(\frac{1}{r_{bb'} C_c T_{ec}} \right)^{1/2} \qquad (1\text{-}1)$$

where

PG: Power Gain

F: frequency of operation

$r_{bb'}$: base-spreading resistance

T_{ec}: collector transit or signal-delay time

C_c: collector capacitance

This equation was derived from analysis of the transistor as a low-level class A amplifier, but it can also serve as a guide to performance in the class C circuit usually encountered in high-frequency power applications. To a first approximation, the frequency f_{max} at which the power gain is unity is independent of collector area. Although the collector capacitance C_c is directly dependent on the collector area, the value of r_{bb} varies inversely with this area. For example, if the stripes and base of an interdigitated or comb-type structure are made twice as long, the capacitance C_c is doubled, but $r_{bb'}$ is cut in half. Therefore, the length of a transistor can be extended and the power dissipation and current-handling capability improved without any increase of the $r_{bb'} \cdot C_c$ product. The collector-to-emitter transit time T_{ec} has four components: (1) the charging time of the emitter

capacitance, (2) the transit time through the base, (3) the transit time through the collector capacitance and (4) the collector series resistance. The last term is usually negligible in devices made with triple-diffused or epitaxial construction. Of the remaining terms, only the emitter transit time[3] T_e is current-dependent and can be expressed as

$$T_e = r_e C_{ea} = \frac{KT}{qI_e} C_{ea}$$

where

T: temperature in degrees Kelvin

r_e: emitter resistance

C_{ea}: emitter capacitance

K: Boltzmann's constant

q: electron charge

I_e: emitter current

Hence, if the emitter edge is increased proportionally as the area of the emitter is increased, the fraction C_{ea}/I_e remains a constant, and f_{max} is almost constant.

Basic construction

Figure 1-3 shows a top and cross-sectional view of a typical interdigitated transistor. The emitters and bases are built like a set of interlocking combs. The emitter and base areas are controlled by masking and diffusion. The oxide deposit masks the transistor against either an n- or p-type impurity. This oxide is removed by the photoetching techniques in areas where diffusion is required in a base or emitter.

Figure 1-4 - Top and cross-sectional view of a typical overlay transistor.

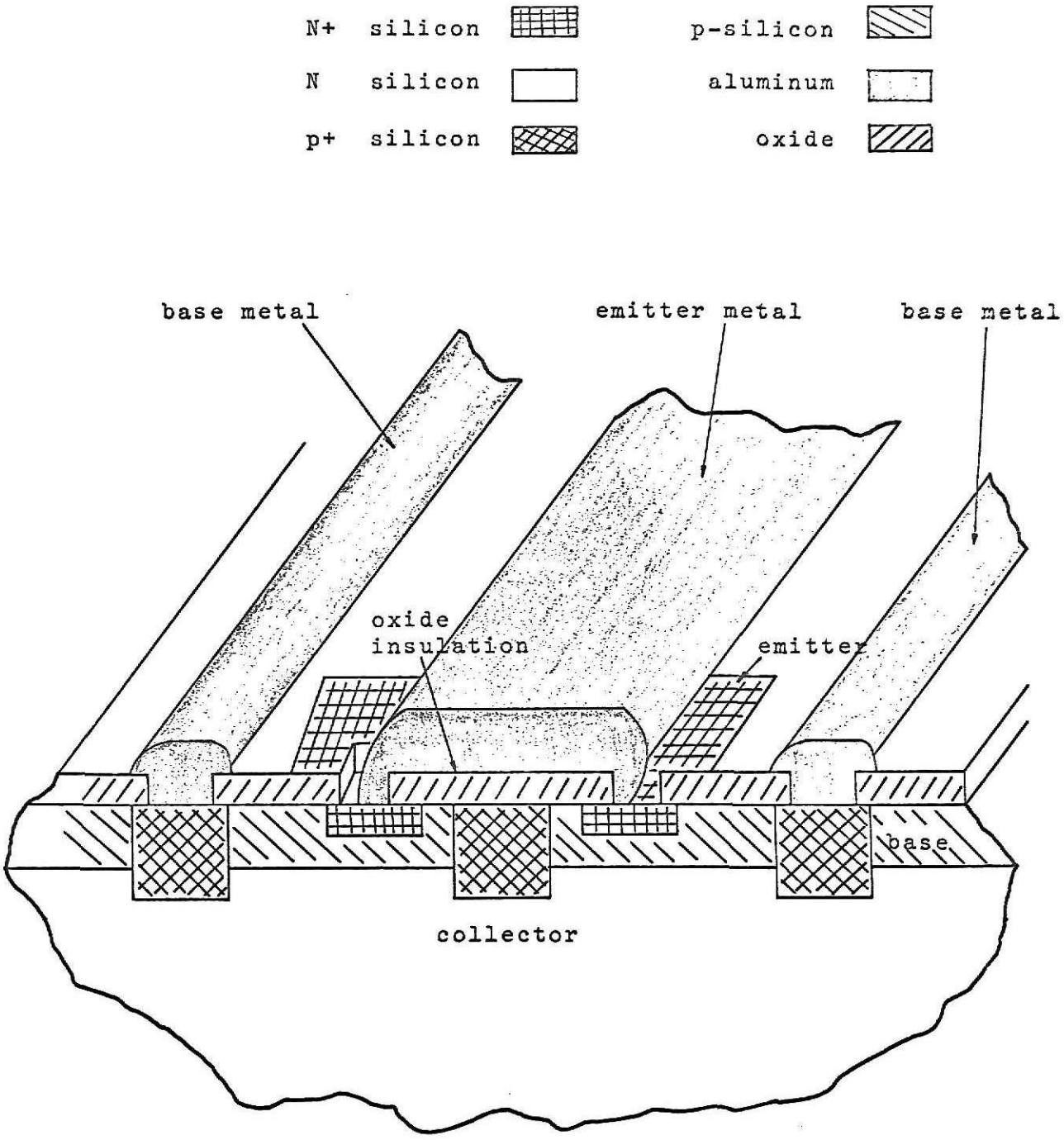


Figure 1-4 shows a top and cross section view of a typical overlay transistor.[6] An overlay structure differs from an interdigitated structure in three ways:

(1) Pattern---In Figure 1-4, many small, separate emitter sites are used instead of the continuous emitter strip shown in the interdigitated geometry of Figure 1-3.

(2) Composition---In addition to the standard base and emitter diffusions, an extra diffused region p^+, as shown in Figure 1-4, is made in the base to serve as a conductor grid.

(3) Metallization---The emitter metallization, as shown in Figure 1-4, lies over the base instead of adjacent to it as in Figure 1-3.

Comparison

In a comparison between overlay and interdigitated transistors, the former construction technique provides some advantages over the later technique:

(1) It provides a substantial increase in over all emitter periphery without requiring an increase in physical area of the device, and therefore raises the device power-frequency capability.

(2) The base current is distributed uniformly over all of the separate emitter sites.

(3) The distance between emitter and base is reduced and therefore the base resistance and contact resistance between the aluminum metallization and silicon material is reduced.

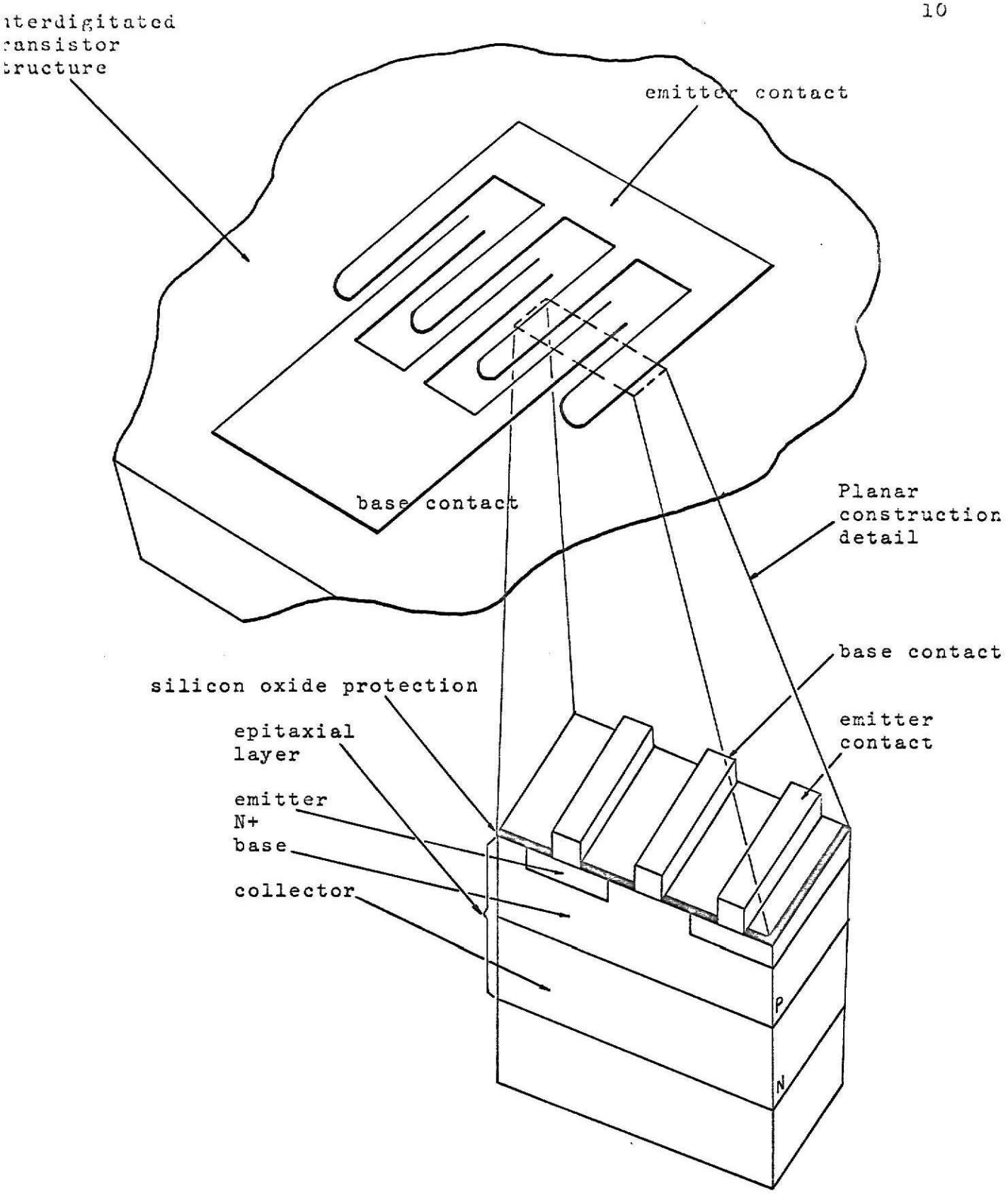


Figure I-3 Top and cross-sectional view of a typical interdigitated transistor.

Because of these advantages, the overlay transistor is currently the most popular design for achieving high-frequency performance in a power transistor. Certainly overlay transistor has accelerated the conversion from tubes to semi-conductor devices. The effect of fabrication on microwave performance--small-signal operation.

The important performance criteria in UHF small-signal amplifier circuits are gain and noise figure. These criteria can be expressed in terms of the transistor parameters as follows:[7]

$$MAG = \left[\frac{f_{max}}{f}\right]^2 = \frac{f_T}{8\pi f^2 r_{bb'} C_c} \qquad (1\text{-}2)$$

$$NF = 1 + \frac{r_{bb'}}{R_g} + \frac{r_e}{2R_g} + \frac{(r_{bb'} + r_e + R_g)^2}{2\alpha_o R_g r_e} \times \left[\frac{I_{co}}{I_E} + \left(\frac{f}{f_T}\right)^2 + \frac{1}{h_{FE}}\right] \qquad (1\text{-}3)$$

where

MAG: Maximum available power gain

f: frequency of operation

f_{max}: maximum frequency of oscillation

f_T: gain-bandwidth product

$r_{bb'}$: base-spreading resistance

C_c: intrinsic base-to-collector capacitance

NF: noise figure

r_e: emitter diffusion resistance

I_{co}: collector cutoff current

I_E: emitter current

αo: steady-state common-base current transfer ratio (gain)

R_g: source resistance

h_{FE}: steady-state common-emitter current transfer ratio (gain)

Equation (1-2) shows that maximum available power gain MAG of a transistor decreases at a theoretical rate of 6dB per octave. The MAG relates directly to transistor capability rather than to the circuit used. High MAG is obtained with f_T maximized and the $r_{bb'} \cdot C_c$ product minimized.

The f_T can be expressed in terms of the emitter-to-collector signal delay time T_{ec} as follows:

$$f_T = \frac{1}{(2\pi T_{ec})} \qquad (1\text{-}4)$$

As mentioned before, the emitter-to-collector transit time, T_{ec}, represents the sum of several constants, all of which affect the over-all time of a transistor's response to an input signal. The most important of these constants are the emitter capacitance charging delay, T_{ec}, the base transit time, T_b, and the collector depletion layer transit time, T_c. Base transit time can be cut by narrowing base layers; widths of about 0.3 micron are common in today's microwave transistor. Emitter capacitance charging delay drops as current densities rise, but a practical limit is reached when "base widening" sets in. This condition occurs when the excess of mobile charge in the collector depletion region changes the space charge distribution so that the neutral base layer extends

into the depletion region. Base widening increases the transit time. Collector depletion layer transit time decreases as the depletion layer narrows. At low currents, the width of the depletion layer depends on the collector doping level and the operating voltage. At high currents, it also depends partly on the thickness of the epitaxial layer. As current increases, the collector depletion layer moves toward the collector contact and can reach the substrate boundary. Therefore, transistors should be designed with depletion layers extending right up to the substrate boundary, even at low currents, to permit the use of high current densities and to reduce parasitic collector resistance. However, it should be noted that f_T is determined mainly by the vertical geometry of the transistor. The $r_{bb'} \cdot C_c$ product is determined by the horizontal geometry of the transistor. Base resistance is minimized in a small-signal UHF transistor through the use of long, thin, closely spaced emitter and base contact strips. A wide collector depletion layer is helpful in minimizing $r_{bb'}$ and C_c. Although this decreases f_T because of increased collector transit time, f_{max} is increased.

Equation (1-3) shows that low-noise performance requires high f_T, low $r_{bb'}$, and high steady-state current gain. In comparison with high power gain transistors, the low-noise transistors have been designed to operate at relatively low current densities. Because delay and dispersion of carriers traveling from emitter to collector increase the noise figure, it is essential to maintain as high a current ampli-

fication factor as possible. Hence, low-noise transistors emphasize a high f_T and sacrifice some gain. Their collector depletion layers are thin, and the voltage and current density operating bias is low. To minimize thermal noise a low base resistance is necessary. This low base resistance can reduce input circuit losses, which might otherwise degrade the noise figure. High h_{FE} is required to reduce noise from the base current created by carriers lost in transit between emitter and collector.

The effect of fabrication on microwave performance--- large-signal operation.

The important performance criteria in UHF large-signal power amplifier circuits are power output, power gain, and efficiency. Transistors used for power amplification must be capable of delivering power efficiently with sufficient gain at the frequency range of interest.

The power-output capability of a transistor is determined by the current and voltage-handling capabilities within the operating frequency range. The current-handling capability of a transistor is limited by its emitter periphery and epitaxial-layer resistivity. The voltage handling capability of a transistor is limited by the breakdown voltages. But the breakdown voltages of a transistor are limited in turn by the resistivity of the epitaxial layer and the penetration of the junction. The power-handling capability of a transistor is also limited by the saturation voltage $RFV_{CE(SAT)}$. The saturation voltage at UHF is significantly greater than the dc value because the active area is less at high frequencies

than at low frequencies.

In general, all RF power transistors have operating voltage restrictions. Therefore, the only difference between small-signal and large-signal operation is the current-handling capability. As mentioned previously at high current levels, the emitter current of a transistor is concentrated at the emitter-base edge. Hence, the transistor current-handling capability is increased by the use of emitter geometries which have high emitter-periphery-to-emitter-area ratios. Large-signal transistors are designed so that peak currents do not cause a base widening which would limit the current-handling capability of the device. But the need for low-resistivity material in the collector region in order to handle high currents without base widening severely limits the breakdown voltages.

The power gain of a microwave transistor power amplifier is determined by the dynamic $\int T$, the dynamic input impedance, and the collector load impedance. The power gain of a transistor power amplifier can be expressed as follows:[7]

$$PG = \frac{(T/f)^2 R_L}{4R_e(Z_{in})} \tag{1-5}$$

where

PG: power gain

$\int T$: dynamic gain-band width product

f: operating frequency

R_L: real part of the collector parallel equivalent load impedance

$R_e(Z_{in})$: real part of the dynamic input impedance

Equation (1-5) demonstrates that for high gain operation of a power transistor the device should have a high current gain (h_{FE}) which is constant for large current levels. Constant current gain can be obtained by the use of shallow diffusion techniques. The collector load impedance depends on the required power output and collector voltage swing. The dynamic input impedance varies considerably under large-signal operation as compared to small-signal operation. The resistive part of the input impedance is inversely proportional to the area of the transistor. The package parasitic inductance has significant effect also on the input impedance. However, a common emitter input impedance Z_{in} can be expressed as follows:

$$Z_{in} = (r_e + r_b + W_t L_e) + j \left(W e^{-(\frac{W_t}{W}) r_e} \right) \qquad (1\text{-}6)$$

where

$W_t = 2\pi f_T$

L_e: the emitter parasitic impedance

r_e: the combination of transistor emitter resistance and external emitter resistance.

r_b: base resistance

W: $2\pi f$

Substitution of Equation (1-6) into Equation (1-5) results in the following relation:

$$PG = \frac{(f_T/f)^2 R_L}{4(r_b + W_T L_e)} \qquad (1\text{-}7)$$

Equation (1-7) shows that the effect of the emitter parasitic inductance is to reduce the power gain.

Transistor efficiency is determined with the device operating under a signal-bias condition at which the collector-to-base junction is reverse-biased partially by the input drive signal. The collector efficiency is defined as follows:

$$\eta_c = \frac{P_{OE}}{P_{DC}} \times 100\% \qquad (1\text{-}8)$$

where

P_{OE}: RF power output at the frequency of interest

P_{DC}: dc input power

High efficiency implies that circuit loss be minimum and the ratio of the parallel output equivalent resistance to collector load resistance be maximum. Hence, the output admittance limits the collector efficiency. The output admittance consists of two parts: an equivalent parallel output resistance which approaches $\frac{1}{W_t C_o}$ at UHF frequencies under small-signal conditions, and an output capacitance C_o. In a common emitter circuit, the impedance leval at the transistor output is essentially the output capacitance, C_o. In power transistors, junction and epitaxial thickness variations cause variation in C_o with V_{CB}, as shown in Figure 1-5.

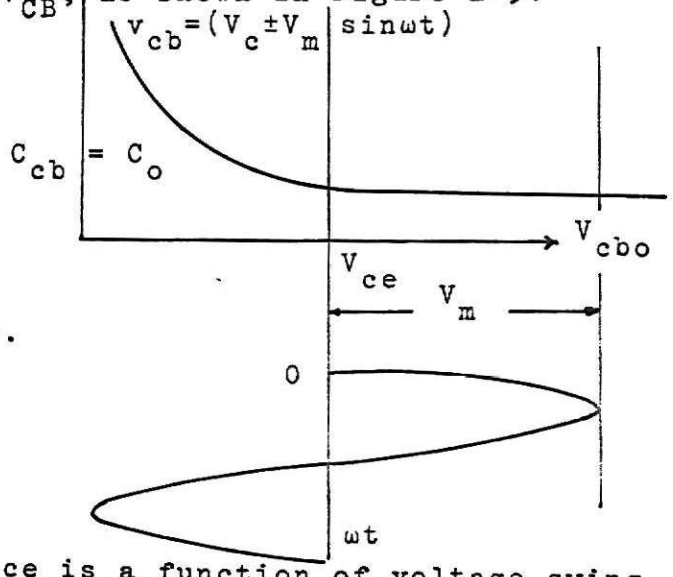


Figure 1-5. Collector to base capacitance as a function of collector to base voltage for a typical RF power transistor.

Hence, the output capacitance is a function of voltage swing

and power level. It can be shown that the average C_o under maximum voltage swing is equal to $2C_{cb}$. For a first approximation, the large-signal output resistance can be assumed to be inversely proportional to C_{cb}. For high efficiency a transistor with high output resistance and low C_{cb} is essential.

Another transistor parameter which affects the collector efficiency is the dissipation capability. The maximum power that can be dissipated before thermal runaway occurs depends on how well the internal transistor heat is removed. The amount of heat removed by conduction is an inverse function of the thermal resistance. The average junction to ambient thermal resistance of a device can be expressed as follows:

$$\sigma_{JA} = (T_j - T_a)/P_{diss} = \sigma_{jc} + \sigma_{CA} \ (^oC/W) \qquad (1\text{-}8)$$

where σ_{JA}: average junction to ambient thermal resistance

T_j: collector junction temperature

σ_{CA}: average case to ambient thermal resistance

T_a: ambient temperature

σ_{JC}: average junction to case thermal resistance

The thermal resistance, expressed in $^oC/W$ of dissipation, may be calculated for the sections of total heat flow path, as follows:[7]

$$\sigma_{th} = \frac{L}{KA} \qquad (1\text{-}9)$$

where

L: the length in inches that the heat travels

A: the area in square inches

K: equal to 2.12 for silicon, 5.2 for Beryllium Oxide, 9.7 for copper, and 3.1 for aluminum.

For a given length and width, the thermal resistance can be calculated for most geometries.

It should be pointed out that the dissipation of a microwave power transistor under RF operation is considerably higher than under dc operation. The junction temperature is more a function of the average device dissipation than of the peak dissipation. The dissipation of a microwave power transistor is also a function of the thermal time constant.

Chapter 2

TRANSISTOR PARAMETERS

Introduction

It can be seen from the last chapter that some important parameters control the UHF transistor amplifier. Hence, those parameters will be discussed in this chapter in more detail. At this point only the large-signal transistor parameters will be that emphasized. Scattering parameters for small-signal transistor operation will be introduced in the next three chapters.

Common emitter h_{FE}

The steady-state common-emitter current transfer ratio h_{FE} is an important transistor parameter as seen in the last chapter. It is typically measured at a low voltage and under pulse conditions so that power dissipation has no effect on it. Typically, h_{FE} increases with junction temperature. At high current levels, h_{FE} will decrease rapidly when the current density has reached a high level. Therefore, a low h_{FE} transistor will have more a linear h_{FE} versus collector current characteristic. A high h_{FE} transistor will have a more radical percentage variation in h_{FE} versus collector current, h_{FE} reaching a peak at a lower current level. In addition to the correlation of circuit performance directly with h_{FE}, it will be seen that many RF parameters also correlate directly to h_{FE}.

In general, high h_{FE} transistors have higher base resistance because the lateral sheet resistance of the base under

the emitter is higher. A high h_{FE} transistor is easy to match at the input port because it has a high input resistance and low inductance (see input impedance). And as seen from the last chapter, a high h_{FE} is the most important parameter in a UHF transistor amplifier. But a high h_{FE} transistor requires some trade-offs in circuit design.

(1) A high h_{FE} transistor has a greater tendency to oscillate and at lower frequencies.

(2) It is more difficult to maintain a constant bandwidth as a function of circuit layout.

(3) It will have lower saturated-power output, although it will have higher power gain at most frequencies.

(4) It will be a less linear device and hence will have higher intermodulation distortion and less dc bias stability for single-side band circuits.

Breakdown voltages

There are six static breakdown voltage modes, each relating to a specific collector current and base lead condition. In each case, a specified value of collector current flows in the reverse direction. These are:

BV_{CEO}: the collector-emitter breakdown when the base is open

BV_{CER}: the collector-emitter breakdown when a resistor of specified value, R, is connected between base and emitter

BV_{CEV}: the collector-emitter breakdown when the base is reverse biased with a voltage with respect to the emitter

BV_{CEX}: the collector-emitter breakdown voltage when the base is terminated through a specified circuit to the emitter

BV_{CES}: the collector-emitter breakdown when the base is shorted to the emitter

BV_{CBO}: the breakdown of the collector-base junction with the emitter open

Breakdown voltage characteristics are shown in Figure 2-1.

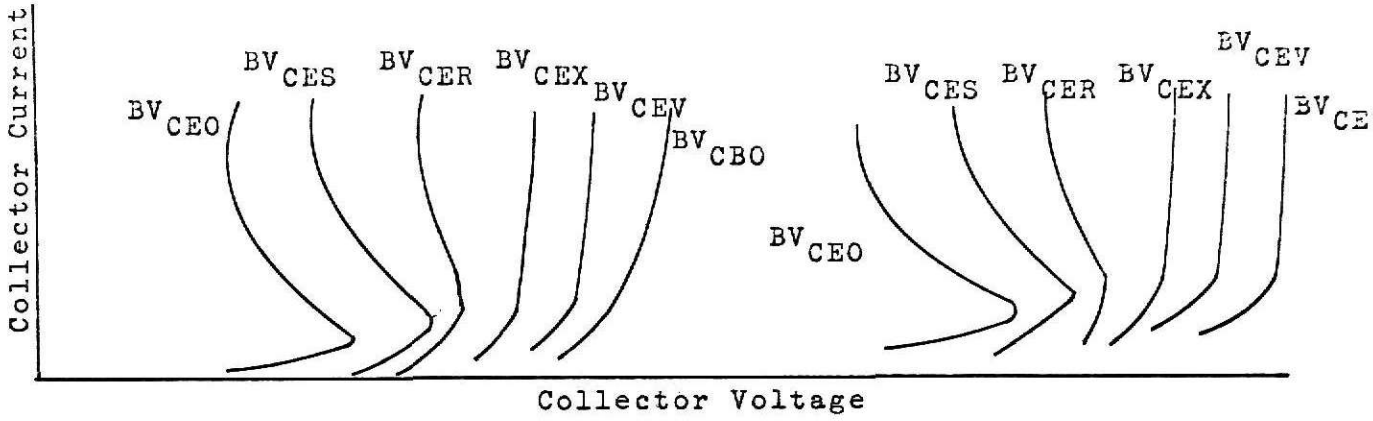


Figure 2-1. Breakdown voltage characteristics-typical transistor.

Curves at left are for a low-resistivity thin epitaxial layer; at right, for a high-resistivity relatively thick epitaxial device.

In the above, BV_{CEO} is an important parameter because both RF parameters and circuit operation parameters correlate to this breakdown voltage. A fairly broad range of collector-base breakdown voltage is possible for a given process depending on the resistivity variation of the material used. The higher the collector-base breakdown voltage, the lower the saturated power output capability of a transistor.

Output capacitance, common-base (C_{ob})

The parameter C_{ob} is important because it affects the circuit tuning and the output-impedance level of the transistor. In common-emitter circuits, C_{ob} is essentially the output

capacitance. This is because the impedance levels at the base are quite low relative to the impedance level at the transistor output. The large-signal value of C_{ob} can be as much as twice the small-signal value. The output capacitance of a transistor represents effectively its junction capacitance in series with resistance. If the collector resistivity is increased, the effective output capacitance is decreased as seen from the external terminals. Also, if the resistivity is increased, the collector-base breakdown voltage, BV_{CEO}, is also increased. Junction and epitaxial-thickness variation cause some variation in output capacitance, too. C_{ob} also varies with collector voltage, which is an important consideration in large-signal operation as seen in Chapter I.

Collector-emitter saturation voltage ($V_{CE(SAT)}$)

$V_{CE(SAT)}$ is an important parameter which is always specified as a dc characteristic, but actually it is the high frequency saturation voltage that is of major importance. However, these two parameters do correlate. The realtionship between them is partly controlled by the geometry of the transistor because it affects the active area. $V_{CE(SAT)}$ is also correlated to the collector-base breakdown voltage, which in turn is correlated to the resistivity of the collector epitaxial material in the transistor. Hence, a higher breakdown voltage device has a higher saturation voltage level at dc, and also at RF. In a large signal RF power circuit, the transistor is driven all the way from collector saturation to cutoff. Hence, the saturation level determines the extent of

the voltage swing.

RF breakdown voltage

The RF breakdown voltage of a transistor is higher than its dc value. A relation between the dc and RF breakdown voltage can be expressed as follows:[10]

$$BV_{CEX(r-f)} = \frac{BV_{CBO}}{\sqrt[n]{Kh_{FE}+1}} \qquad (2\text{-}1)$$

where n is an emperical number that varies from 2.5 to 4 for n-p-n silicon transistors, and K is a constant that modifies h_{FE} for RF. Once K is determined, any other RF breakdown behaviour can be calculated by inserting the values of h_{FE} and BV_{CEO} for a specific frequency.

RF saturation voltage (RF $V_{CE(SAT)}$)

At higher frequencies, the saturation voltage is significantly greater than the dc value. This is because the high-frequency active area is less than at dc. Typically, a high-breakdown voltage device utilizing high resistivity material will have higher saturation voltage levels than a low breakdown-voltage device. Therefore, it is not advisable to use a high-breakdown-voltage device for a low-voltage application. For a given power level, a much larger area device is necessary if the saturation voltage is a significant percentage of the supply voltage. The relation among power output, $V_{CE(SAT)}$, and supply voltage is given by the following equation.[12]

$$P_{OE} = \frac{V_{cc} - V_{CE(SAT)}^{2}}{2R_L} \qquad (2\text{-}2)$$

Equation (2-2) shows that $V_{CE(SAT)}$ has a significant effect on the maximum power output capability of a transistor. Hence, this is an important parameter from the standpoint of both circuit design and device design.

Output and input impedance

To design adequately a high-frequency power transistor amplifier circuit, the impedances to which the input and output must be matched need to be known. The large-signal impedances are especially important. These dynamic impedances are difficult to calculate at microwave frequencies.

In general, a high h_{FE} device will have low output impedance. The output resistance decreases significantly as the collector current is increased. Hence, the output resistance is significantly lower in a large-signal circuit of an RF power amplifier than for the small-signal case or where the transistor drive level is low. This implies that the harder a transistor is driven, the lower the output impedance becomes. Measurements of large-signal output impedance should bear this out. Output capacitance is fairly constant with current swing but not with voltage. Collector breakdown-voltage also effects the output impedance. For transistors of a single type, the units with a higher BV_{CBO} will have a lower output capacitance.

The input impedance of a transistor at high frequencies can be represented by the simple circuit as shown in Figure 2-2a. For a high power UHF transistor, the input capacitance is large. Therefore, the circuit can be reduced to that of a series inductance and a base resistance as shown in Figure 2-2b. In general, the input capacitance decreases as the h_{FE} of a transistor is increased. Hence, the UHF input inductance becomes effectively smaller as the h_{FE} becomes greater. This is because the capacitive reactance will be larger and cancel out more of the package and circuit inductance. If the transistor has a low h_{FE}, the input impedance has less variation with collector current. In addition, the large-signal input impedance is much lower than the small-signal value. The input impedance in a tuned circuit is affected both by the stored charge and by how the charge is drawn out of the device in the "off" part of the drive cycle. This lowers the input impedance further. Like the output impedance, the harder a transistor is driven, the lower the input impedance. The large-signal input inductance L_s depends on the stored charge of the transistor and the class of operation.

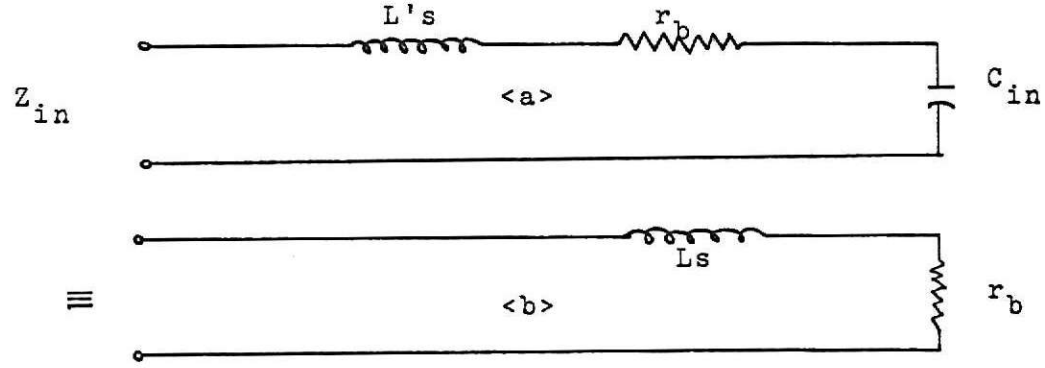


Figure 2-2. Input circuit representations. Where the input capacitance is large, as for high-power transistor, the general circuit (a) can be simplified to that at (b)

Packaging

Package parasitic inductance and resistive losses have significant effect on such circuit performance characteristics such as power gain, bandwidth, and stability and phase delay. The package is an integral part of an RF power transistor. A suitable package for microwave application should have good thermal properties, low interelectrode capacitance, and low parasitic inductances. The most critical parasitics are the emitter and base lead inductances.

A low-Q input to a transistor is important for ease of matching to the transistor; it also improves circuit stability. The package input-Q does not determine the circuit bandwidth in itself. However, the higher the ratio of the source impedance to the real part of the transistor input impedance, the narrower the bandwidth; also, the more difficult it is to maintain the bandwidth when designing a cascading network. A low package-input Q is of utmost importance as the first step in providing a good transistor for broadband applications and for ease of circuit design.

To maintain the low package Q, it is necessary to have a shunt capacitance to ground from the package input or from a point near it. It is also important for good circuit design that the input Q sensitivity to a change in the added series inductance external to the package be rather small.

Reliability and stability

Important parameters which are directly related to the reliability performance are RF breakdown voltage, thermal

characteristics and load mismatch capability of the transistor. Although a safe-area curve can be established for avoidance of second breakdown on the I_c-V_{CE} plane for forward bias or class A operation, such a curve for class B or C or pulsed operation is difficult to define, because the breakdown voltages under RF conditions are considerably higher than the dc breakdown voltages, and the thermal resistance is a function of V_{CE} and I_c. The safe operating area under class B or C conditions at RF frequencies would be a function of these parameters as well as the thermal time constant of the device. Generally, the safe operating area for class B or C operation can be expected to be higher than that under dc condition.

The VSWR capability, or the ability of an RF power transistor to withstand a high VSWR load, is another important consideration. VSWR is found to be a function of frequency of operation, operating voltage, and circuit configuration. A well designed circuit operated at low supply voltages at a frequency where power gain is not excessive is less prone to VSWR mismatch. There are four modes of difficulty experienced in the load mismatch test, as follows:[7]

(1) slow thermal failure due to low RF swing and very poor efficiency;

(2) high-speed failure due to the high positive peak value of the RF swing;

(3) an instability (non-destructive) which occurs due to the high value of V_{CE} causing avalanching (such a condition in the common emitter configuration produces a negative resistance characteristic and results in a spurious-signal generator);

(4) an instability as the result of the negative overswing which can severely forward-bias the collector-base junction, which in turn, will trigger a low-frequency oscillation.

The choice of transistor configuration at microwave frequencies is based on both performance and stability. From the performance point of view, common-base amplifiers provide high gains at frequencies higher than the f_T of the transistor. Collector efficiency for common-emitter and common-base circuits is about the same. From the stability point of view, it has been generally accepted that a common-emitter configuration will provide a more stable circuit at frequencies below the f_T of the transistor. This assumption can be demonstrated by a linear analysis of transistors, in which parasitic elements are not included. However, for high-power operations at UHF, transistor parasitics contributed by the package must be treated with the intrinsic transistor. Stable operation can also be obtained in common-base configurations provided parasitic elements can be controlled.

Because transistor parameters change with power level, certain forms of instability can be incurred in both common-emitter and common base circuits; for example, hysteresis in dynamic characteristics, parametric oscillations, and low-frequency oscillations. Usually, most of these difficulties can be eliminated or minimized by careful design of the bias circuit, by proper location of the transistor ground connections, and by the use of packages with minimum parasitic inductance and capacitance. Hysteresis refers to discontinuous mode

jumps in output power that occur when the input power or frequency is increased or decreased. It has been determined that this effect is caused by the dynamic detuning which results from the variation in the average value of the non-linear junction capacitance with RF voltage. The tuned circuit will have a different resonant frequency for a large input drive than for a weak input. Low frequency oscillations occur because the gain of the transistor at low frequencies is much higher than that at the operating frequency. This effect can be eliminated with small resistances placed in series with RF chokes used for the biasing circuit, as in Figure 2-3. Parametric oscillations result because spurious low-frequency modulation is added to the harmonic output. This affect can be eliminated with careful selection of the bypass capacitance C_2 in Figure 2-3 to provide a low impedance to the spurious component in addition to that provided by the bypass capacitance C_1.

Stable operation has been obtained at 2 GHz with both common-base and common-emitter configuration. However, common-base coaxial packages have empirically been found more stable at UHF.

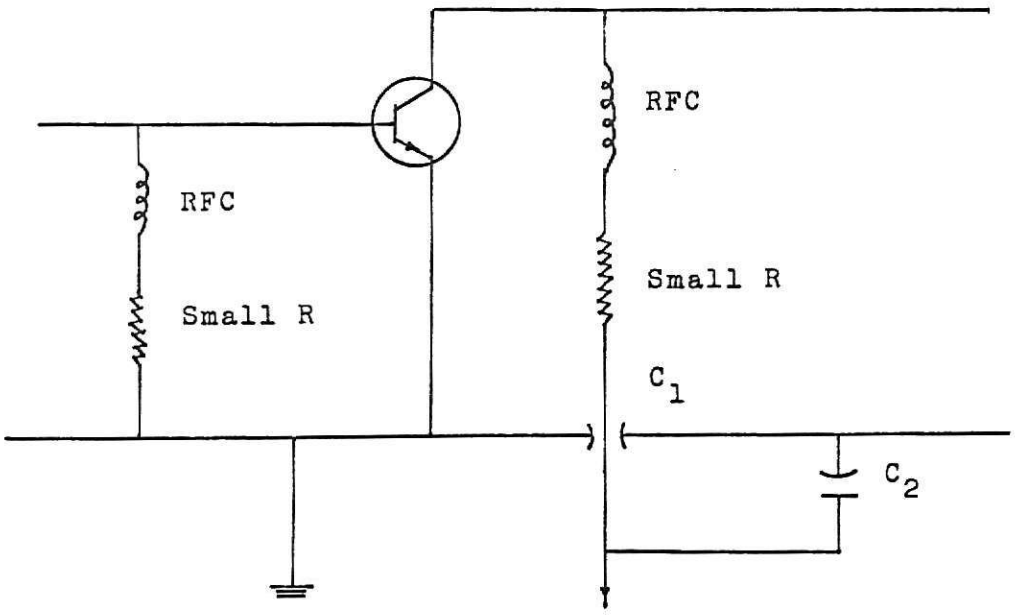


Figure 2-3. Use of biasing arrangement and bypass capacitances to eliminate instability in common-emitter power amplifiers.

Chapter 3

POWER WAVES AND THE SCATTERING MATRIX

Introduction

When the main interest is in the power relations between various microwave circuits in which the sources are uncorrelated, traveling waves are not the best independent variables to use for the analysis. Then incident and reflected power waves are introduced. In this chapter the physical meaning of these power waves will be discussed first. Some properties of the scattering matrix defined by incident and reflected power waves then will be discussed in general and than in particular for a two-part network. The method of using a scattering matrix in designing small-signal transistor amplifiers at high frequency will be introduced in Chapter 5. Measurements of scattering parameters for high frequency transistors will be introduced in the next chapter.

Physical meaning

The incident and reflected power waves a_i and b_i are defined by

$$a_i = \frac{V_i + Z_i I_i}{2\sqrt{R_e Z_i}}$$

$$b_i = \frac{V_i - Z_i^* I_i}{2\sqrt{R_e Z_i}} \qquad (3\text{-}1)$$

where

V_i: voltage at the ith port

I_i: current flowing into the ith port

Z_i: impedance looking out from the ith port

Z_i^*: conjugate of Z_i

$R_e Z_i$: real part of Z_i

The positive real value is chosen for the square root in the denominators.

To better understand the waves defined by (3-1), the fundamental concept of the exchangeable power of a generator is introduced. Figure 3-1 shows an equivalent circuit of a linear generator in which Z_i is the internal impedance, Z_L is load impedance, and E_o is the open circuit voltage of the generator. The power P_L into a load Z_L is given by

$$P_L = R_e Z_L \left| \frac{E_o}{Z_L + Z_i} \right|^2 = \frac{R_L |E_o|^2}{(R_L + R_i)^2 + (X_L + X_i)^2} \tag{3-2}$$

$$= \frac{|E_o|^2}{4R_i + \frac{(R_L - R_i)^2}{R_L} + \frac{(X_L + X_i)^2}{R_L}} \tag{3-3}$$

where

R_L: real part of Z_L

R_I: real part of Z_i

X_L: imaginary part of Z_L

X_i: imaginary part of Z_i

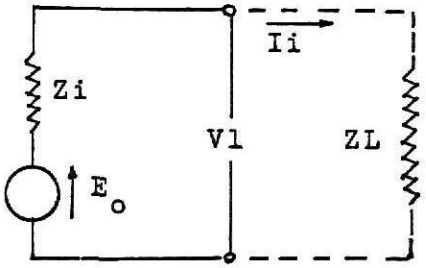


Figure 3-1

With $R_i > 0$, the denominator of (3-3) becomes minimum when

$$R_L = R_i \quad , \quad X_L = -X_i \tag{3-4}$$

The corresponding maximum power P_L is

$$P_a = \frac{|E_o|^2}{4R_i} \quad , \quad (R_i > 0) \tag{3-5}$$

This maximum power P_a is called the avilable power of the generator. From Equation (3-2), it is obvious that P_L becomes infinite as R_L and X_L approach $-R_i$ and $-X_i$ respectively, if the real part of R_i is negative, i.e., $R_i < 0$. In this case, (3-5) no longer represents the maximum power that can be drawn from the generator. However, the power represented by it is called the exchangeable power of the generator, for any nonzero R_i. That is,

$$P_e = \frac{|E_o|^2}{4R_i} \quad . \qquad (R_i \lesseqgtr 0) \tag{3-6}$$

Therefore, for $R_i > 0$, the exchangeable power P_e is the maximum power that the generator can supply. With $R_i < 0$, the P_e can be regarded as the maximum power that the generator can absorb.

The voltage at the generator terminal as shown in Figure 3-1, is given by

$$V_i = E_o - Z_i I_i$$

Inserting this into the first expression in (3-1), and taking the square of the magnitude, an expression,

$$|a_i|^2 = \frac{|E_o|^2}{4|R_i|}$$

is obtained, which is equivalent to

$$P_e = P_i |a_i|^2$$

where P_i is defined by

$$P_i = \begin{cases} 1 & \text{when } R_e Z_i > 0 \\ -1 & \text{when } R_e Z_i < 0 \end{cases} \tag{3-7}$$

It is worth to note that a_i becomes zero when E_o is equal to zero. Direct substitution of (3-1) into the expression

$$|a_i|^2 - |b_i|^2$$

gives

$$|a_i|^2 - |b_i|^2$$

$$= \frac{(V_i + Z_i I_i)(V_i^* + Z_i^* I_i^*) - (V_i - Z_i^* I_i)(V_i^* - Z_i I_i^*)}{4|R_i|}$$

$$= \frac{(Z_i + Z_i^*)(V_i I_i^* + V_i^* I_i)}{4|R_i|} = P_i R_e [V_i I_i]$$

from which another expression is obtained as

$$R_e [V_i I_i^*] = P_i (|a_i|^2 - |b_i|^2). \qquad (3\text{-}8)$$

The left-hand side of (3-8) expresses the power which is actually transferred from the generator to the load. Hence, this is called the actual power to the load (or from the generator.) The expression $-|b_i|^2$ is always negative whether the load contains some source or not. Therefore the magnitude of the exchangeable power of a generator $|a_i|^2$ can be identified as the maximum power that the generator can supply when $R_i > 0$, and as the maximum power that the generator can absorb when $R_i < 0$.

If P_i is equal to 1, then equations (3-7) and (3-8) can be interpreted as follows. The generator sends the power $|a_i|^2$ toward a load, regardless of the load impedance. If the load is not matched, that is, Equation (3-4) is not met, a part of the incident power is reflected back to the generator. This reflected power is given by $|b_i|^2$. Therefore the net

power absorbed in the load is equal to $|a_i|^2 - |b_i|^2$.

Reflection coefficients and scattering matrix.

The power wave reflection coefficient S is defined as

$$S = \frac{b_i}{a_i} \tag{3-9}$$

and $|S|^2$ is called power reflection coefficient. The power wave reflection coefficient S can be expressed in terms of impedances by using (3-1) and the relation $V_i = Z_L I_i$. That is

$$S = \frac{Z_L - Z_i^*}{Z_L + Z_i^*} \tag{3-10}$$

Substituting $Z_i = R_i + jX_i$, $Z_L = R_L + jX_L$ into (3-9), S can be rewritten in the form

$$S = \frac{R_L + j\,(X_L + X_i) - R_i}{R_L + j\,(X_L + X_i) + R_i} \tag{3-11}$$

Comparing Equation (3-11) with that of the conventional voltage reflection coefficient, it is obviously that S corresponds to the vector drawn from the center of the Smith chart to the point where the normalized impedance is given by $[R_L + j\,(X_L + X_i)]/R_i$. In other words, if the reactance part of Z_i is added to Z_L and normalized with respect to the real part of Z_i, then the corresponding point on the Smith chart gives the magnitude and the phase of S. It can be shown that $|S| < 1$, when R_i and R_L have the same sign and $|S| > 1$ when R_i and R_L have opposite signs.

By definition S and $|S|^2$ are the reflection coefficients

looking into the load from the generator side. On the other hand, the corresponding reflection coefficients S' and $|S'|^2$ looking into the generator from the load are given by

$$S' = \frac{Z_i - Z_L^*}{Z_i + Z_L} \quad , \quad |S'|^2 = \left|\frac{Z_i - Z_L^*}{Z_i + Z_L}\right|^2$$

It should be noted that the subscripts i and L have been interchanged from the expression of (3-10). Now S' is not necessarily equal to S. However, $|S'|^2$ is always equal to $|S|^2$ because $|Z_i - Z_L^*| = |Z_i^* - Z_L| = |Z_L - Z_i^*|$. Therefore, when the roles of generator and load are interchanged, the power reflection coefficient remains the same. The expression $1 - |S|^2$ is defined as the power transmission coefficient and remains constant when the roles of the generator and load are interchanged. It is worthwhile to note that the power transmission coefficient times the exchangeable power is equal to the actual power. Conversely, the actual power divided by the power transmission coefficient is the exchangeable power.

In order to define the scattering matrix in terms of a linear n-port network, let a, b, v, and i be vectors whose ith components are a_i, b_i, v_i, and I_i at the ith port of the network respectively. Then a and b can be written in terms of v and i as the following equation:

$$a = F(v + G_i), \qquad b = F(v - G^+_i) \tag{3-12}$$

where

F: the diagonal matrix whose ith diagonal components are given by $\frac{1}{2}\sqrt{R_e Z_i}$

G: the diagonal matrix whose ith diagonal components are given by Z_i.

+: indicates the complex conjugate transposed matrix.

There is a linear relation between v and i given by

$$v = Z_{\ell}\, i \tag{3-13}$$

where Z is the impedance matrix. Also, a and b are linear transformations of v and i. Hence, there is a linear relation between a and b as follows,

$$b = Sa \tag{3-14}$$

where S is called the power wave scattering matrix.
From (3-12), (3-13), and (3-14) the following expression for S can be obtained

$$S = F(Z - G^{+})\,(Z + G)^{-1}\,F^{-1} \tag{3-15}$$

Similarly, Z can be expressed in terms of S as follows

$$Z = F^{-1}\,(I - S)^{-1}\,(SG + G^{+})\,F \tag{3-16}$$

where I is a unit matrix.

Reciprocal condition

It is a necessary condition that the impedance matrix Z representing a reciprocal network has to satisfy the relation

$$Z = Z_t \tag{3-17}$$

where the subscript t indicates the transposed matrix. The corresponding relation for S is given by

$$S_t = PSP \tag{3-18}$$

where P is a diagonal matrix whose diagonal components are given by P_i^*. The proof of (3-18) can be found in the literature given by K. Kurokawa.[5] Equation (3-18) is equivalent to

$$S_{ji} = P_i P_j S_{ij} \tag{3-19}$$

which indicates that S_{ij} is equal to S_{ji} if the signs of $R_e Z_i$ and $R_e Z_j$ are the same, and S_{ij} is equal to $-S_{ji}$ if $R_e Z_i$ and $R_e Z_j$ have opposite signs. However, the following relation must also hold,

$$|S_{ij}|^2 = |S_{ji}|^2 \quad , \tag{3-20}$$

Suppose that all the circuits external to the n-port have no source except the one connected to the ith port of the network. The power from the jth circuit to the network is given by

$$P_j \left(|a_j|^2 - |b_j|^2\right),$$

where $a_j (j \neq i)$ is equal to zero. Hence, the power to the ith circuit from the network is given by $P_j |b_j|^2$. In this case, b_j is equal to $S_{ji} a_i$ and hence, the ratio of the actual power $P_j |b_j|^2$ into the load j to the exchange power $P_i |a_i|^2$ from the source i is equal to $P_i P_j |S_{ji}|^2$. According to Equation (3-20) the value of this ratio does not change when the subscripts i and j are interchanged. Therefore, in a reciprocal network, there is a power reciprocal relation, that is, the relation between the actual power into a load and the exchangeable power from the source stays constant when the roles of source and load are interchanged. The exchangeable power to the jth circuit is given by $P_j |b_j|^2$/

$1 - |S_{ij}|^2$. Thus, the ratio of the exchangeable power into the ith circuit to that from the jth circuit is equal to $P_j P_i |S_{ji}|^2 / 1 - |S_{jj}|^2$. Since $|S_{jj}|$ is not necessarily equal to $|S_{ii}|$, the value of this ratio does not remain constant when the roles of source and load are interchanged. Similarly, the ratio of the actual power into the jth circuit to that from the ith circuit is equal to

$$\frac{P_i P_j |S_{ji}|^2}{(1 - |S_{ij}|^2)} .$$

This ratio does not remain constant when the roles of source and load are interchanged, however, the ratio of the exchangeable power into the load j to the actual power from the source i is equal to

$$\frac{P_i P_j |S_{ji}|^2}{(1 - |S_{jj}|^2)(1 - |S_{ii}|^2)}$$

and remains constant.

Lossless condition

It was shown in the previous sections that the actual power into the network from the ith circuit is equal to $P_i(|a_i|^2 - |b_i|^2)$. Hence, the total power into the network is

$$\sum_i P_i (|a_i|^2 - |b_i|^2)$$

When the network is lossless, this total power must be zero, therefore,

$$\sum_i P_i (|a_i|^2 - |b_i|^2) = 0 .$$

This can be expressed in matrix form as follows:

$a^+Pa - b^+ Pb = 0$. Substitution of $b = Sa$ gives $a^+ (P - S^+PS)$ $a = 0$. Since a is arbitrary, this means

$$S^+ PS = P \tag{3-21}$$

Equation (3-21) is the condition that the scattering matrix representing a lossless network must satisfy.

Change of circuit impedance

If the impedances of the circuits connected to the junction are changed from Z_i to Z_i' ($i = 1, 2, \ldots, n$), the incident and reflected waves have to be redefined. The new scattering matrix S' differs from the original S. However equation (3-22) gives the new scattering matrix S':

$$S' = A^{-1} (S - T^+) (I - TS)^{-1} A^+ \tag{3-22}$$

where

T: diagonal matrices whose diagonal component is r_i

A: diagonal matrices whose diagonal component is $(1 - r_i^*) \sqrt{|1 - r_i r_i^*| / |1 - r_i|}$

I: unit matrix

+: indicates complex conjugate transposed matrix

r_i: power wave reflection coefficient of Z_i' with respect to Z_i^*

$$r_i = \frac{Z_i - Z_i}{Z_i + Z_i^*}$$

The proof of Equation (3-22) can be found in the literature given by K. Kurokawa.[5]

Two port network scattering parameters

To define scattering parameters the two-port, or transistor, is terminated at both ports by a so-called reference impedance Z_o, a pure resistance. As shown in Figure 3-2, (a_1, b_1) and (a_2, b_2) represent the incident and reflected waves for the two-port network at terminals 1-1' and 2-2' respectively. These parameters are defined as follows:[13]

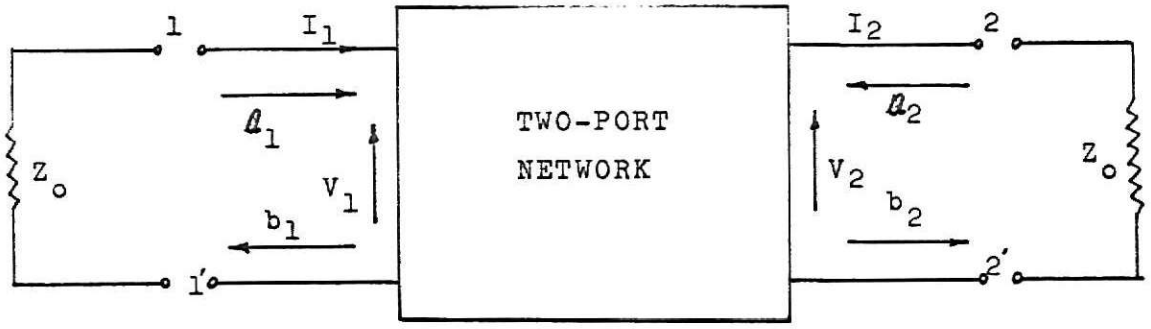


Figure 3-2. Scattering parameters are defined by this representation of a two-port network. Two sets of incident and reflected parameters (a_1, b_1) and (a_2, b_2) appear at terminals 1-1' and 2-2, respectively.

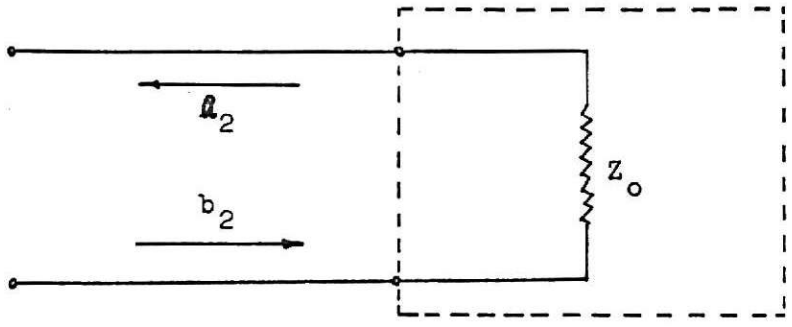


Figure 3-3. By setting a_2 equal to zero the S_{11} parameter can be found. The Z_o resistor is thought of as a one-port network. The condition $a_2 = 0$ implies that the reference impedance R_z is set equal to the load impedance Z_o.

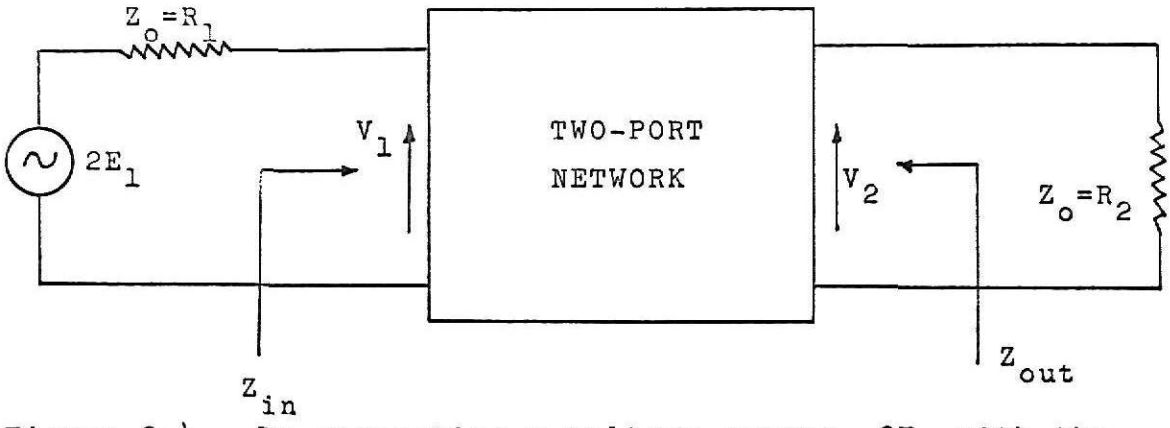


Figure 3-4. By connecting a voltage source, 2E, with the source impedance, Z_o, parameter S_{21} can be found using equation (3-27).

$$a_1 = \frac{V_1 + Z_o I_1}{2\sqrt{Z_o}} \tag{3-23a}$$

$$b_1 = \frac{V_1 - Z_o I_1}{2\sqrt{Z_o}} \tag{3-23b}$$

$$a_2 = \frac{V_2 + Z_o I_2}{2\sqrt{Z_o}} \tag{3-23c}$$

$$b_2 = \frac{V_2 - Z_o I_2}{2\sqrt{Z_o}} \tag{3-23d}$$

The scattering parameters S_{ij} for the two-port network are given by Equation (3-24),

$$\begin{aligned} b_1 &= S_{11}\, a_1 + S_{12}\, a_2 \\ b_2 &= S_{21}\, a_1 + S_{22}\, a_2 \end{aligned} \tag{3-24}$$

In matrix form equation (3-24) becomes

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3-25}$$

where the matrix

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{3-26}$$

is called the scattering matrix of the two-port network. Therefore the scattering parameters of the two-port network can be expressed in terms of the incident and reflected power waves as follows:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2 = 0} \qquad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1 = 0}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2 = 0} \qquad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1 = 0} \tag{3-27}$$

The parameter S_{11} is called the input reflection coefficient; S_{12} is the reverse transmission coefficient; S_{21} is the forward transmission coefficient; and S_{22} is the output reflection coefficient. All four scattering parameters are expressed as ratio of reflected power waves to incident power waves.

The terminating section of the two-port network with the parameters a_2 and b_2 of the 2-2' port is shown in Figure 3-3. If the load resistor Z_o is considered as a one-port network with a scattering parameter

$$S_2 = \frac{Z_o - R_2}{Z_o + R_2}$$

where R_2 is the reference impedance of port 2, when the reference impedance is set equal to the local impedance Z_o, then

$$S_2 = \frac{Z_o - Z_o}{Z_o + Z_o} = 0$$

Therefore $a_2 = 0$ under this condition. Similarly, if the reference impedance of port 1 is equal to the terminating impedance, a_1 will be equal to zero, too. The conditions $z_1 = 0$ and $a_2 = 0$ simply mean that the reference impedances R_1 and R_2 are chosen to be equal to the terminating resistor Z_o.

Using (3-23) and the relation $V_1 = I_1 Z_{in}$ and $V_2 = I_2 Z_{out}$, the reflection coefficient S_{11} and S_{22} can be expressed in terms of impedances. That is,

$$S_{11} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o} \tag{3-28}$$

and

$$S_{22} = \frac{Z_{out} - Z_o}{Z_{out} + Z_o} \tag{3-29}$$

These expressions indicate that if the reference impedance at a given port is chosen to equal the port's driving-point impedance, the reflection coefficient will be zero, provided the other port is terminated in its reference impedance. In the equation,

$$S_{21} = \left. \frac{b_2}{a_1} \right| a_2 = 0,$$

the condition $a_2 = 0$ means that the reference impedance R_2 is set equal to the load impedance. As shown in Figure 3-4, if a voltage source $2E_1$ is connected with a source impedance $R_1 = Z_o$, a_1 can be expressed as follows:

$$a_1 = \frac{E_1}{\sqrt{Z_o}}$$

Since $a_2 = 0$, therefore

$$a_2 = 0 = 1/2 \left(\frac{V_2 + Z_o I_2}{\sqrt{Z_o}} \right)$$

from which

$$\frac{V_2}{Z_o} = -\sqrt{Z_o} \quad I_2$$

and

$$b_2 = 1/2 \frac{(V_2 - Z_o I_2)}{\sqrt{Z_o}} = \frac{V_2}{\sqrt{Z_o}} .$$

Finally, the forward transmission coefficient can be expressed as follows:

$$S_{21} = \frac{V_2}{E_1} \tag{3-30}$$

Similarly, when port 1 is terminated in $R_1 = Z_o$ and a voltage source $2E_2$ with a source impedance Z_o is connected to port 2, the reverse transmission coefficient can be expressed as follows:

$$S_{12} = \frac{V_1}{E_2} \tag{3-31}$$

Both S_{12} and S_{21} have the dimensions of a voltage-ratio transfer function. But if $R_1 = R_2$, then S_{21} is the voltage ratio of the output to input voltage between the reference impedances and is a measure of the gain of active devices; S_{12} is the feedback term which gives the voltage gain (loss) in the reverse direction under the same condition.

When the two-port network is lossless as well as reciprocal, the equations

$$S_t = PSP \tag{3-21}$$

and

$$S^+PS = P \tag{3-24}$$

must be satisfied simultaneously.

Chapter 4

MEASURING S PARAMETERS

Introduction

The measurement of s-parameters for two-port networks or transistors is introduced in this chapter. The values of h, y, or z parameters, ordinarily used in small signal transistor circuit design at lower frequencies, can not be measured accurately above 500 MHz because of the following reasons:

(1) Establishing the required short and open circuit conditions is difficult.

(2) A short circuit frequently causes the transistor under test to oscillate.

Therefore, transistors used at higher frequencies are typically characterized by using the scattering parameters.

Two measuring systems, one considering the unknown transistor as a three-port network[17], the other considering the unknown transistor as a two-port network[13], will be introduced, and a brief comparison between two measuring systems will be made.

Method I-Two-port s-parameter system[13.7]

To measure scattering parameters, the unknown transistor is terminated at both ports by pure resistances; 50 ohms is usual. As mentioned in the last chapter, this connection has these advantages:

(1) The S_{11} and S_{22} parameters are power reflection coefficients that are difficult to measure under normal loading. However, if the unknown transistor is terminated at both ports by pure resistances, the parameters become equal to voltage reflection coefficients, and can be measured directly with simpler test equipments.

(2) The S_{12} and S_{22} are square roots of the transducer power gain, the ratio of power absorbed in the load over the source power available. But if the unknown transistor is terminated at both ports by pure resistances, S_{12} and S_{22} become a voltage ratio and can be measured with a vector voltmeter.

(3) The transistors can be placed in reversible fixtures to measure the reverse parameters S_{22} and S_{12} with the equipment used to measure S_{11} and S_{21}.

(4) The actual measurement can be taken remotely whenever the transmission line connecting the unknown transistor to the source and load has the same characteristic impedance as the load and source.

(5) Parasitic oscillations are minimized because of the broadband nature of the transistor terminations.

(6) Swept-frequency measurements are possible instead of point to point methods.

Two vector voltmeters are used to determine S_{21} abd S_{12} by measuring voltage ratios and phase differences between the input and output. A dual-directional coupler is used to sample incident and reflected voltages to measure the magnitude and phase of the reflection coefficient.

A block diagram[7] of a typical s-parameter measurement setup is shown in Figure 4-1. The basic procedure for measuring S_{11} and S_{22} is to measure the amplitude ratio and phase angle between the incident and reflected voltages with probe B in the B_1 position. S_{11} is measured with the jig in the forward direction, and S_{22} with the jig reversed. For S_{12} and S_{21}, the transmitted signals are measured with the B probe in B_2 position, with S_{21} resulting when the jig is reversed.

Method II-Three-port s-parameter system[17]

Three-port scattering parameters are obtained by measuring the incident and reflected waves, with all ports terminated in 50 ohms. The unknown transistor is inserted at a Y junction of three TEM 50 ohms transmission lines as shown in Figure 4-2. The three-port scattering parameters are defined by

$$\begin{bmatrix} b_b \\ b_e \\ b_c \end{bmatrix} = \begin{bmatrix} S_{bb} & S_{be} & S_{bc} \\ S_{eb} & S_{ee} & S_{ec} \\ S_{cb} & S_{ce} & S_{cc} \end{bmatrix} \begin{bmatrix} a_b \\ a_e \\ a_c \end{bmatrix} \qquad (4\text{-}1)$$

Equation (4-1) represents only the linear term of the transistor characteristics expanded about its operating point. Nonlinear terms can be expressed by including the higher order terms as follows:

$$b_i = \sum_j S_{ij}\, a_j + \sum_j \sum_k T_{ijk}\, a_j\, a_k + \sum_j \sum_k \sum_e U_{ijkL}\, a_j\, a_k\, a_L + \cdots \qquad (3\text{-}2)$$

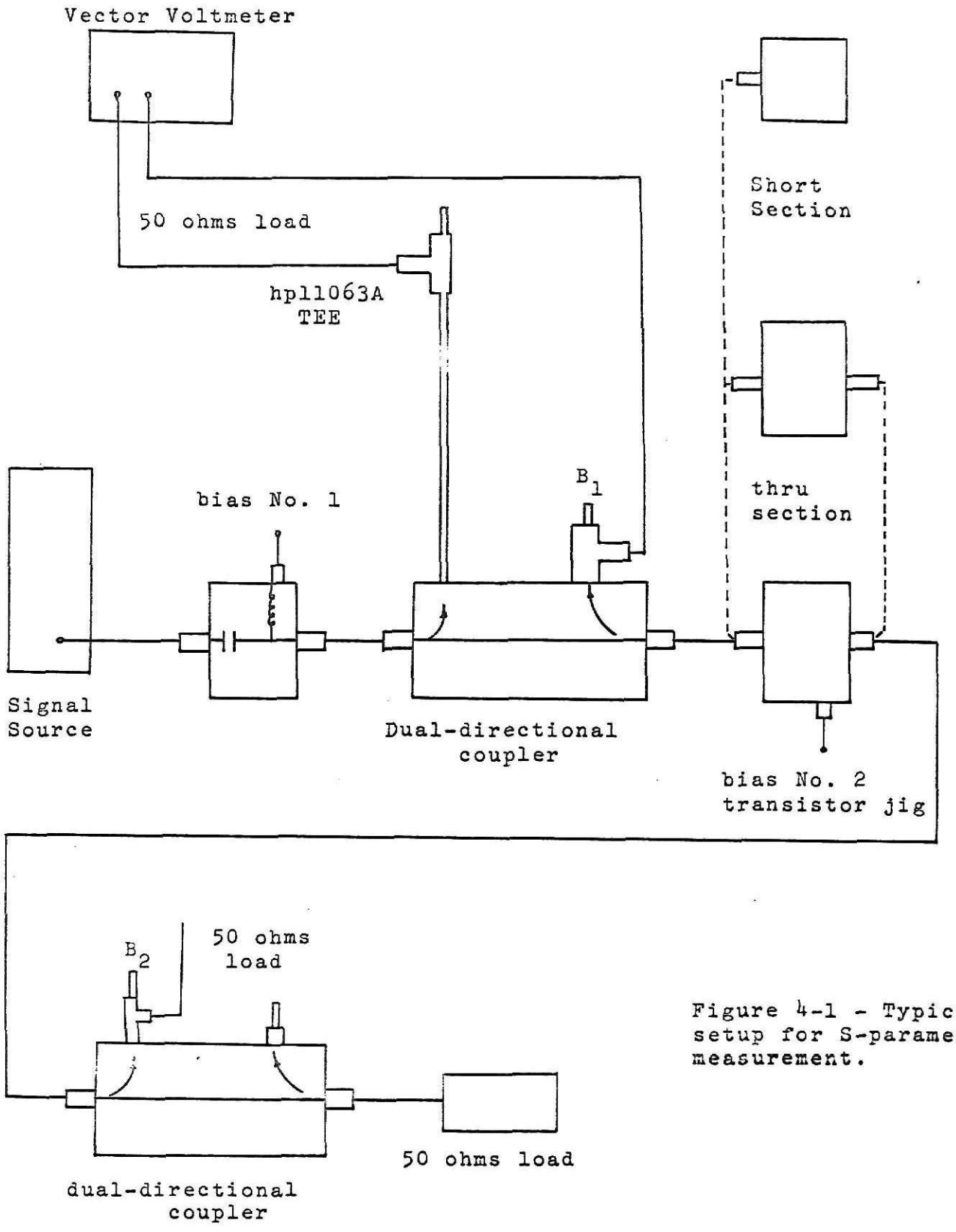


Figure 4-1 - Typical setup for S-parameter measurement.

where

T_{ijk}: element of tensor representing second order term.

ijkL: element of tensor representing third order terms.

Higher order terms are required only when the device is driven well into the non-linear region. Three couplers are connected to the Y junction as shown in Figure 4-4 to measure the reflected and incident signal, and another coupler is used to obtain the reference signal. The line lengths l_{REF}, ℓ_1, ℓ_2, and $_3$ are made so that the signal at REF and A, or B, or C has the same magnitude and phase while calibrating the system. Fine adjustments are made by using a phase shifter during the calibration. All of the dc biasing networks are outside the coupler so that they do not interfere with measurements. This system uses sampling and measures three-port s-parameters directly, displaying them on an oscilloscope.

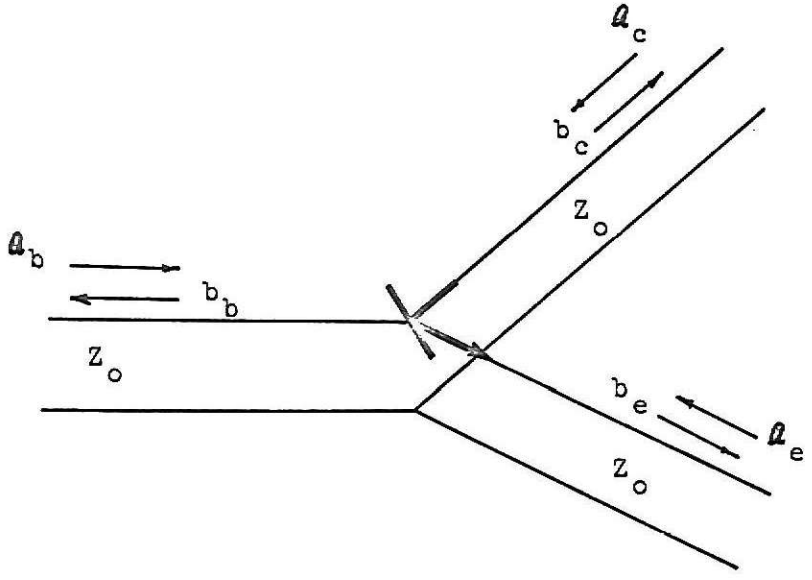


Figure 4-2. Three-port arrangement showing incident and reflected waves.

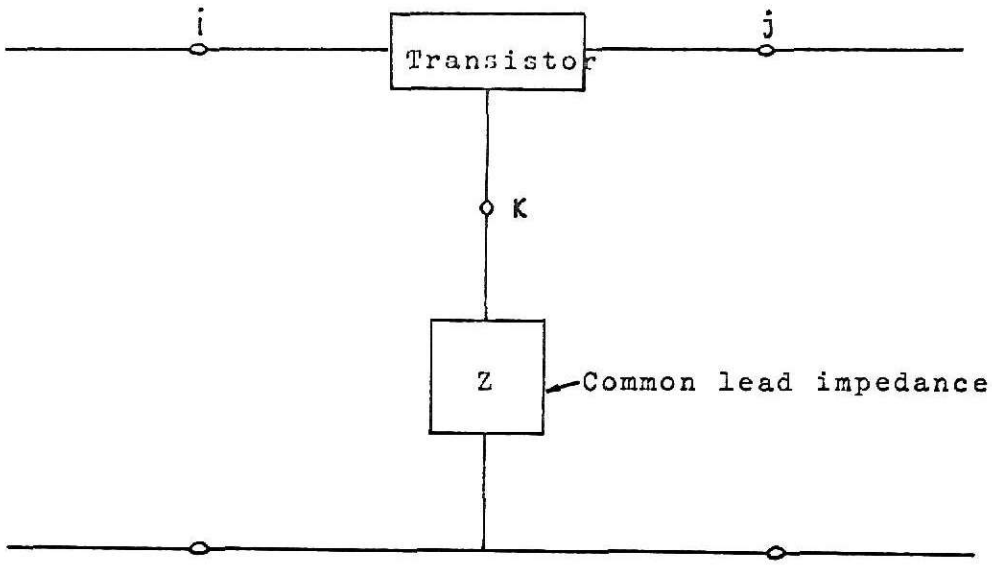
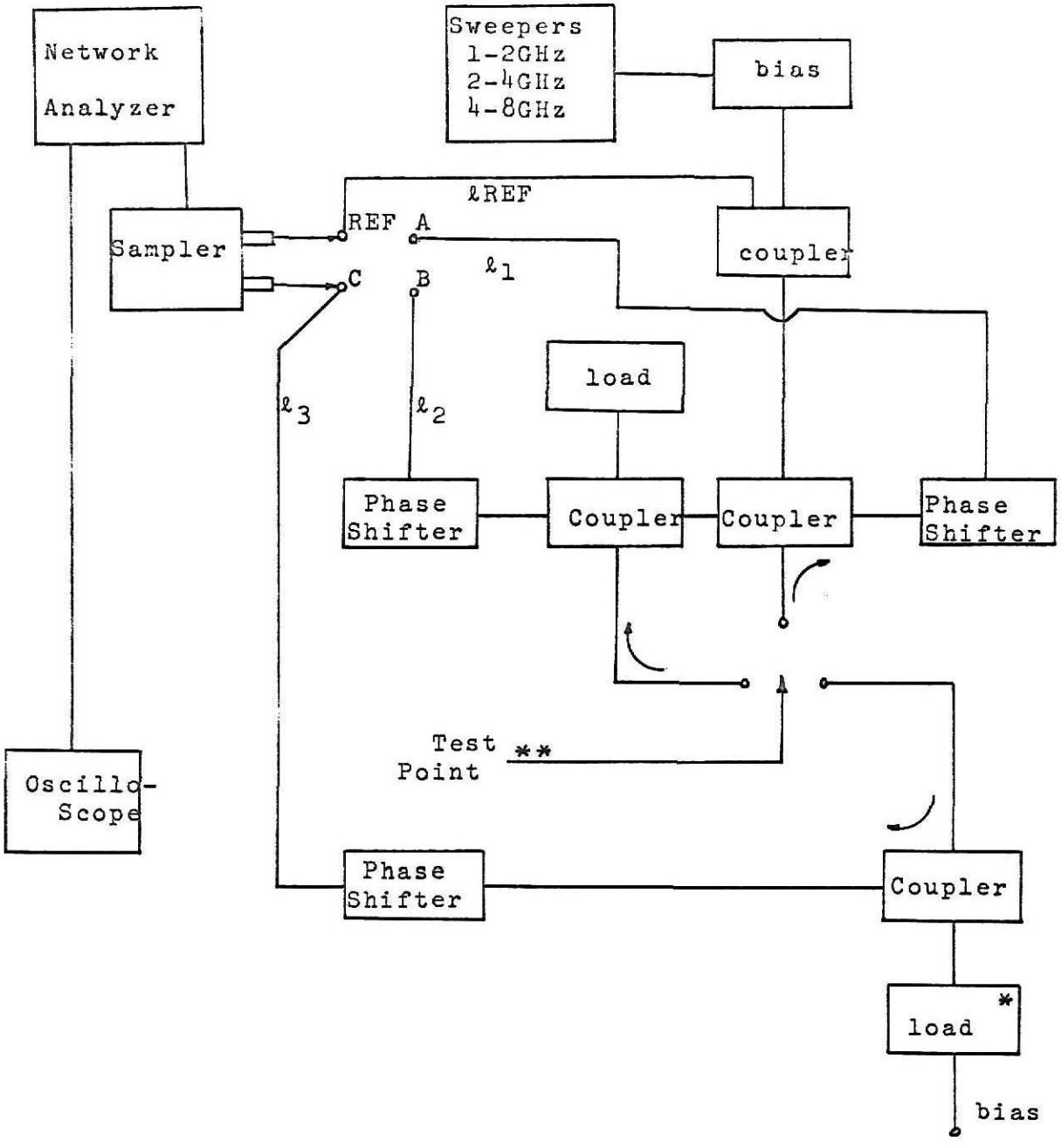


Figure 4-3. Common lead impedance configuration.



* 50 ohms load with dc feed thru

** calibration and text fixtures are inserted here

Figure 4-4 Three-port scattering parameters measurement system.

Comparison

When the three-port s-parameter measurement system is compared with the two-port s-parameter system, the former provides some advantages over the later.

(1) Once the nine parameters are measured, the two-port scattering parameters for common emitter, common base, common collector, and all common lead impedance configurations (Figure 4-3) are obtained by using a single equation[13],

$$S'_{ij} = S_{ij} + \frac{S_{ik}\, S_{kj}}{\frac{1}{P_k} - S_{kk}} \qquad (3\text{-}3)$$

where

$$P_k = \frac{Z - Z_o}{Z + Z_o}$$

Z: common lead impedance

(2) In general for an n-port matrix it can be shown that

$$\sum_{j=1}^{n} S_{ij} = 1 \quad , \quad \sum_{i=1}^{n} S_{ij} = 1 \qquad (3\text{-}4)$$

Hence, the rows and columns of the 3 x 3 matrix must add to unity and every set of data can be checked for its reliability. The proof of equation (3-4) can be found in the literature given by Yozo Satoda[17].

(3) The three-port scattering parameters measurement system is good for measuring microwave integrated circuits and thin film integrated circuits. The reasons for this are as follows:

(a) It is difficult to obtain the short-circuit terminal required for common base or common emitter orientation over a wide range of frequencies for swept-frequency systems.

(b) It is difficult to obtain circuit stability at the proper bias point over the frequency range from dc to max of the transistor.

Chapter 5

USING S PARAMETERS IN DESIGNING SMALL SIGNAL TRANSISTOR AMPLIFIERS

Introduction

An important step in design and analysis of transistor amplifier circuits is the representation of the device with a suitable equivalent circuit. For small signal analysis, it is customary to consider a transistor as a four-terminal "black box" with the voltage and current at the input and output terminals related by a set of four parameters. The most useful set of such parameters have been the h, y, and z parameters. It was mentioned previously that at frequencies above 0.5 GHz, the h, y, and z parameters are increasingly difficult to measure because it is difficult to obtain the required short and open circuits. And short circuits frequently cause the transistor under test to oscillate. However, the small signal transistor used at higher frequencies can be characterized through the use of scattering parameters. The measurement of s-parameters for transistors was introduced in the last chapter. In this chapter, a method of using s-parameters in the analysis and design of a small-signal transistor amplifier will be introduced.

Unilateral-circuit design

The transistors now used at high frequencies usually have relatively low noise figure, high power, and in most cases are approximately unilateral. Hence, the unilateral

design is, for many applications, sufficient. When designing a transistor amplifier with the aid of s-parameters, the unilateral approach is much simpler as the reverse transmission parameter S_{12} is neglected. A two-port network is terminated at the ports by an impedance containing resistance and reactance as shown in Figure 5-1.

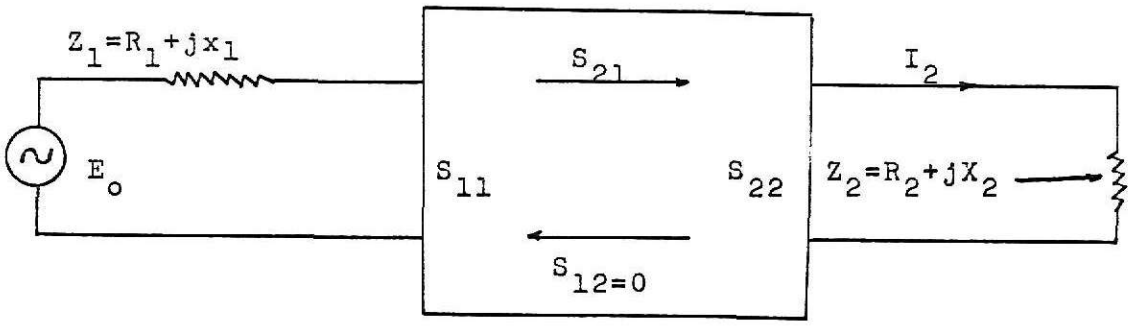


Figure 5-1

The transducer power gain is defined as the ratio of amplifier output power to available source power. That is

$$G_T = \frac{I_2^2 R_2}{\frac{E_o^2}{4R_1}} \tag{5-1}$$

For the unilateral circuit G_T can be expressed in terms of the scattering parameters S_{11}, S_{21}, and S_{22} with $S_{12} = 0$,

$$G_T = G_o, G_1, G_2 \tag{5-2}$$

where

$$G_o = |S_{21}|^2 = \text{transducer power gain for } Z_1 = Z_o = Z_2$$

$$G_1 = \frac{|1-|r_1|^2|}{|1-r_1 S_{11}|}$$ = power gain contribution when the source impedance changes from Z_o to Z_1.

$$r_1 = \frac{Z_1 - Z_o}{Z_1 + Z_o}$$ = reflection coefficient of source impedance with respect to Z_o.

$$G_2 = \frac{|1-|r_2|^2|}{|1-r_2 S_{22}|^2}$$ = power gain contribution when the load impedance changes from Z_o to Z_2.

$$r_2 = \frac{Z_2 - Z_o}{Z_2 + Z_o}$$ = reflection coefficient of load impedance with respect to Z_o.

Therefore, by an unilateral design method, once the s-parameters for a transistor have been measured, they can be used for determination of overall gain with various source and load impedances. When the input and output of the transistor are conjugately matched, the maximum gain of the device is

$$G_{max} = G_{o_{max}}, G_{1max}, G_{2max} = |S_{21}|^2 \times \frac{1}{(1-|S_{11}|^2)} \times \frac{1}{(1-|S_{22}|^2)} \quad (5\text{-}3)$$

where G_{max} is the forward power gain with the input and output terminated in Z_o; 50 ohms is usual. Also, G_{1max} is the additional power gain resulting from the impedance match between the device and source, and G_{2max} is the additional power gain resulting from the impedance match between the device and load. For any arbitrary source and load impedance, the actual gain can be determined by graphical constructions on a Smith chart, or by using Equation (5-2).

The stability factor k for a two-port network can be expressed in terms of the s-parameters as follows[5]

$$k = \frac{1 + |S_{11} S_{22} - S_{12} S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12} S_{21}|} \quad (5\text{-}4)$$

A necessary condition for absolute stability is that $k > 1$. For $k > 1$, the two-port network or transistor is unconditionally stable; that is, no passive load or source impedance will induce oscillations. For $k < 1$, the device is potentially unstable; that is, the application of some combinations of possible load and source impedances can introduce oscillations. It can be proved that simultaneous matching at input and output is possible for any amplifier which is unconditionally stable.[9]

A basic problem in designing transistor amplifiers is the synthesis of suitable input and output matching networks to provide a constant-gain broadband amplifier. One common technique is to provide a good conjugate match at the high end of the frequency band and introduce a mismatch at the lower end. This compensates for the higher gain of transistor at low frequencies and therefore gives a flatter response over the entire required bandwidth.

A graphical plot helps in designing an amplifier stage

In designing an amplifier stage the graphical procedure shown in Figure 4-2 is helpful. The measured values of the parameter S_{11} and its complex conjugate S_{11}^* are plotted on the Smith chart together. The center of the constant gain circles is located on the line through the origin of the Smith chart and S_{11}^* at a distance

$$d_i = \frac{|S_{11}|}{1 - |S_{11}|^2 (1 - G_1/G_{1max})} \qquad (5\text{-}5)$$

Figure 4-2. A graphical plot helps in design of an amplifier stage. Here the measured parameters S_{11} and S_{11}^* are plotted on the chart.

Ref: Philip H. Smith "Transmission Line Calculator" Electronics Jan. 1939 and Jan. 1944

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HILLSIDE 5, N.J.

Printed in U.S.A.

The radius of circles on which G_1 is constant is

$$P_1 = \frac{1 - G_1/G_{1max}\,(1 - |S_{11}|^2)}{1 - |S_{11}|^2\,(1 - G_1/G_{1max})} \qquad (5\text{-}6)$$

When the source reflection coefficient r_1 is made equal to S_{11}^*, then the generator is matched to the load and the gain becomes maximum. The same method is used to determine G_2 by plotting S_{22}, and S_{22}^* constant gain circles and r_2.

Steps for designing an amplifier stage[13]

(1) Using the method introduced in Chapter 4, the s-parameters over the frequency range desired are measured.

(2) The transducer power gain is plotted versus frequency using Equations (5-2) and the measured data from step 1. This determines the frequency response of the uncompensated transistor network. The plotted curve will give an idea for designing a constant-gain amplifier.

(3) The source and load impedances are chosen to provide the proper compensation for a constant power gain from the lowest frequency $_L$ to the highest frequency $_H$ of the desired band-width. Such a constant power gain amplifier is designed according to the following steps.

(3a) Plot S_{11}^* on the Smith chart. The magnitude of S_{11}^* is the linear distance measured from the center of the Smith chart. The radius from the center of the chart to any point on the locus of S_{11} represents a reflection coefficient r_1. The value of r_1 can be determined at any frequency by drawing a line from the origin of the chart to

a value of S_{11}^* at the frequency of interest. The value of r_1 is scaled proportionately with a maximum value of 1.0 at the perphery of the chart. The phase angle is read on the peripheral scale "angle of reflection coefficient in degrees".

(3b) Constant power gain circles for S_{22}^* at f_L and f_H are constructed similarly.

(3c) From the transducer power gain versus frequency diagram find the net power gain reduction n dB from the lowest frequency to the highest frequency.

(4) Find suitable source and load impedances each corresponding to a loss of $-\frac{n}{2}$ dB at f_L, and 0 dB at f_H. This is accomplished by choosing a value of r_1 and r_2 on the $-\frac{n}{2}$ constant gain circle at f_L, such at the same time this value of r_1 and r_2 falls on circles of 0-dB gain at f_H.

Chapter 6

MICROWAVE TRANSISTOR CIRCUIT DESIGN TECHNIQUES

Introduction

After knowing the dynamic input impedance and the load impedance of a packaged transistor, the input and output circuit of the packaged transistor can be properly designed. For most microwave applications, either airline or stripline circuit arrangements are usually used; the former are good for performance, while the later are good for economy. Microwave integrated circuits will be mentioned later in this chapter. Now some useful microwave circuit techniques are discussed below.

Half wave line sections

Sections of uniform transmission line which are electrically an integral number of half wave lengths ($\lambda/2$) in length can be used for transferring an impedance from one point to another, that is, a half wave length of uniform line may be considered as a one-to-one transformer. Such sections are very useful in connecting a load to a source in cases where the load and source can not be made adjacent. A group of capacitors can be placed in parallel by connecting them with sections of line n half waves in length. Insulators on a high frequency line should not be spaced at half wave intervals, otherwise, their effect would be cumulative, thus lowering the insulation resistance of the line.

Quarter wave line sections

Sections of uniform transmission lines which are electrically a quarter of a wavelength ($\lambda/4$) in length have many useful properties in microwave circuits. A quarter wave line which is short-circuited at one end will give a very high impedance at the open end. This property can provide high-resistance stub supports for RF structures, and RF choke action for dc bias circuits. Figure (6-1) shows an application of this property.

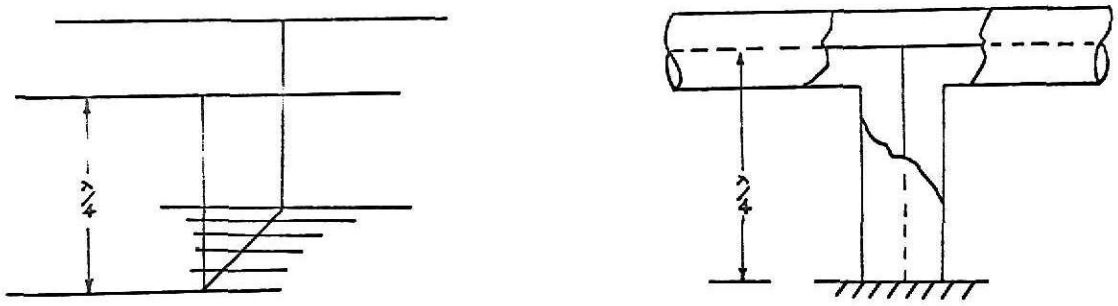


Figure 6-1. Quarter-wave lines as insulators

A $\lambda/4$ line can be used as an insulator to support an open wire line or the center conductor of a coaxial line. Such lines are sometimes called "copper insulators". The insulation resistance usually will have a value of some hundreds of thousands of ohms. It is high enough to be neglected in comparison with a characteristic impedance Z_o of only a few hundred ohms or less. The copper insulator is not only mechanically rugged, but also maintains the line at low potential to ground for all frequencies except the one desired.

If the characteristic impedance Z_o of a quarter-wave line is properly chosen to equal the geometric mean of the source and load impedance, that is, according to the equation,

$$Z_o = | \sqrt{Z_s, Z_R} |$$

where

Z_s: impedance of source

Z_R: impedance of load,

then the quarter-wave line can be thought of as an impedance transformer between real impedances. An important application of this property is the coupling of a transmission line to a resistive load such as an antenna. Here the quarter-wave line must be designed to have a characteristic impedance Z_o' according to equation

$$Z_o' = |\sqrt{R_A Z_o}|$$

where

R_A: real impedance of antenna

Z_o: characteristic impedance of transmission line

The transmission line then is terminated in its Z_o and is operated under conditions of no reflection. It is interesting to note that Z_o', the characteristic impedance of the matching section, is just the value required to achieve critical coupling and maximum power from transmission line to the antenna. If the physical spacing is greater than can be reached with a quarter-wave line, the same transformation can be made by a line any odd number of quarter-waves in length. But greater lengths will reduce the efficiency

slightly due to increased losses in a line of practical construction. The range of values of R_A and Z_o can be matched satisfactorily is limited for practical reasons roughly to about 10 to 1. A quarter-wave transformer may also be used in cases where the load is not a pure resistance. It should then be connected at points corresponding to I_{max} or E_{min}, at which places the transmission line has a resistive impedance given by Z_o/S or $S\ Z_o$. (S = SWCR)

If quarter-wave transformers are used to match a real impedance to an active device, it is necessary to tune out the reactive component of the complex impedance (or admittance) of the active device. For example, Figure 6-2 shows two quarter-wave line matching conditions for class C microwave transistor amplifier circuits. In the input circuit of Figure 6-2, the quarter-wave line matches the resistive component of the complex admittance of the device. Capacitance C_1 provides the necessary positive suceptance needed to cancel out the negative suceptance of the input admittance of the device. The inductive reactance of an input impedance in Figure 6-3 is turned out with a short line section having the necessary negative reactance. The length of this short line can be determined from the Smith Chart. This line section gives a real impedance at point A which is then the starting point of the quarter-wave transformer. A lumped-constant reactance might be used instead of L_1 to supply the capacitive reactance, but it is difficult to obtain a small reactance without excessive losses. For the output circuit, as shown in Figure 6-2, the positive

susceptance of the output admittance can be cancelled with proper design of the series feed inductance L_1 or a line section. By doing so, it will allow the quarter-wave line to present the required load resistance to the collector. In Figure 6-3, a line section $_2$ is used instead of L_1 shown in Figu

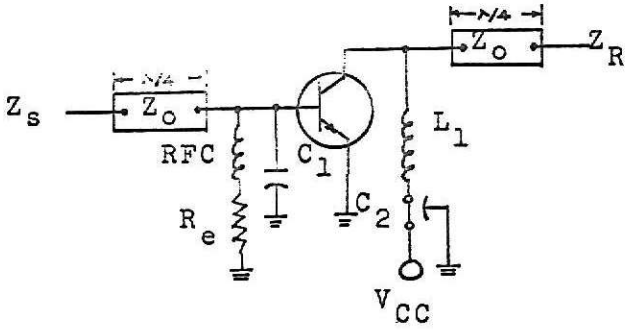


Figure 6-2. λ/4 lines matching to admittances.

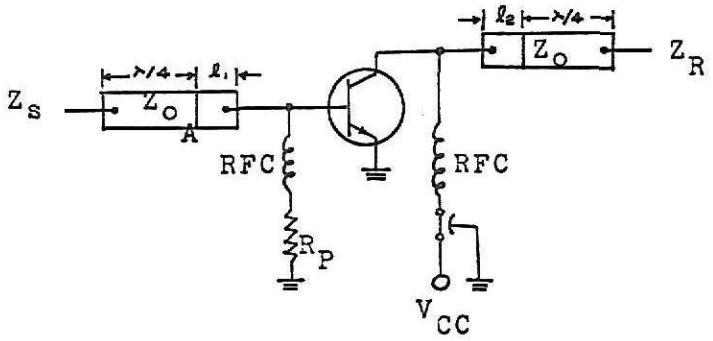


Figure 6-3. λ/4 lines matching to impedances.

Eighth-wave line sections

If the eighth-wave line is terminated in a pure resistance, the input impedance will have magnitude equal to the characteristic impedance Z_o of the line. Conversely, an eighth-wave line which is terminated in an impedance having a magnitude equal to Z_o, will have a real input impedance. Therefore, Z_s the input impedance is real if the following condition is met for $\lambda/8$ line section.

$$Z_o = |Z_R| = (R^2 + X^2)^{\frac{1}{2}}$$

Where

R: real part of Z_R

X: imaginary part of Z_R

The real impedance Z_s can be defined from the Smith Chart or the following relation:

$$Z_s = \frac{R}{\frac{1 - X}{|Z_R|}} \qquad (6\text{-}1)$$

Therefore, an eighth-wave line may be used to transform any resistance to an impedance with a magnitude equal to Z_o of the line. It is also used to obtain a magnitude match between a resistance of any value and a source of Z_o internal resistance. Eighth-wave lines are useful for microwave power transistor matching for the small complex impedance of these devices can be matched directly. It is not necessary to use tuning-out mechanisms, and provides a broader frequency response with lower line-losses. Figure 6-4 shows an application of the eighth-wave line in a typical microwave power transistor amplifier circuit. The device input impedance

R + jx ohms is the terminating impedance Z_R of the eighth-wave line. The Z_s is a real impedance if Z_{o1} is made equal to Z_R. Z_s can be determined from the Smith Chart or Equation 6-1. Matching to the output is made in a similar manner. The collector output load impedance Z_{CL} is then the source impedance Z_s of $\lambda/8$ line. Therefore, if Z_{02} is made equal to the magnitude of the transistor output load impedance, the load impedance of the line Z_R will be real. The real impedance of an $\lambda/8$ line is predetermined by the complex terminating impedance. Therefore, it is necessary to use additional transformations such as differential capacitors or additional transformers in cascade to match a real impedance which is different from this predetermined real impedance.

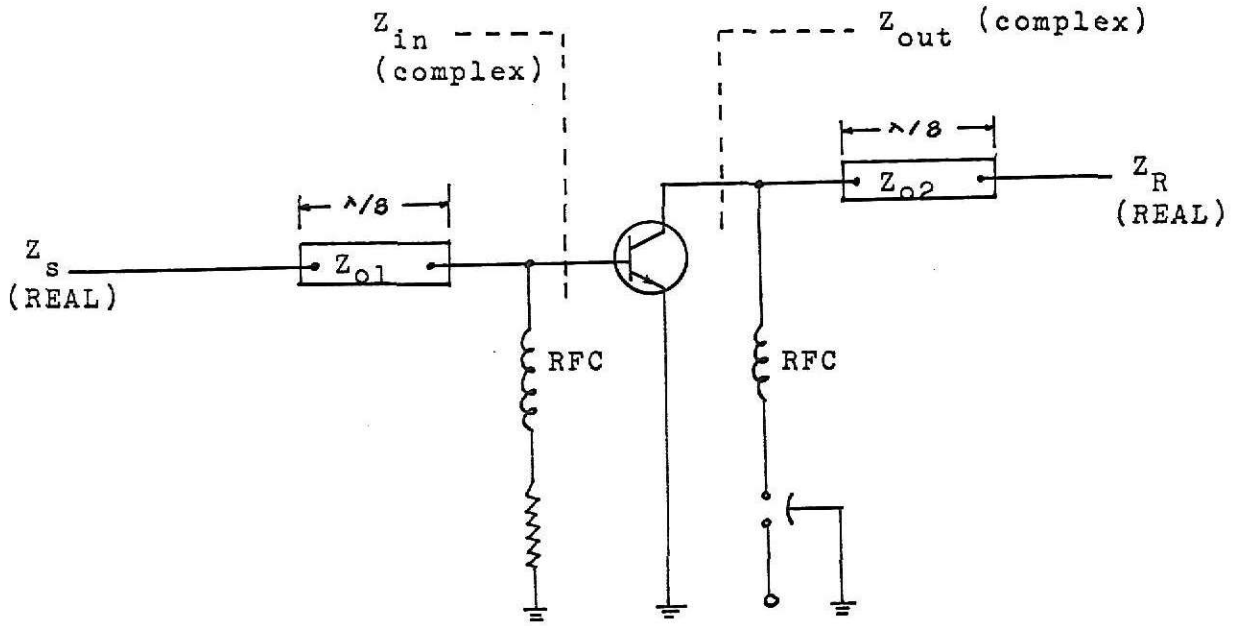


Figure 6-4. Eighth-wave transformers for RF power-transistor amplifier.

The exponential line[15] for impedance transformation and Chebyshev transformers[8].

The characteristic impedance Z_o of a line is a function of the spacing and size of the conductors, among other factors. If the spacing of a dissipationless transmission line is made to vary in a *uniform manner* along the length of a line, Z_o will likewise vary along the line. Using the image-impedance concept, such a tapered transmission line would not be symmetrical, the image impedance at the sending end differing from that at the load end, for some reasonable electrical line lengths. This variation shows the possibility of using lines of tapered spacing as matching sections between a line and a load. If such a dissipationless transmission line were matched on an image basis at both ends, it could serve as a magnitude matching transformer between some source impedance and some other load impedance.

Any arbitrary taper may be made, but an exponential variation of parameters may be easier handled mathematically. The exponentially tapered lines are not only useful for matching a source impedance of 50 ohms to the low real impedance of a microwave power transistor, but also provide the required capacitance at higher frequencies for a good conjugate match to the inductive component of the input impedance. The length of an exponentially tapered line as an impedance transformer has been found experimentally to be approximately 40 per cent less than the wavelength of the uniform line. The width of the low impedance side is designed to obtain a

match to R_e Z_s. It is calculated by the solution of equation[4]

$$Z_o = \frac{377h}{\sqrt{\varepsilon_r}\, W[1 + 1.735\varepsilon_r^{-0.0724}(W/h)^{-0.896}]}$$

where

W: width of the center conductor

ε_r: relative dielectric constant

h: thickness of the dielectric

The capacitive component C_T for the calculated width is

$$C_T = C_{pp} + C_j \approx \frac{\varepsilon_r}{V_\eta}\left(\frac{W}{h} + \frac{2.7}{\log \frac{4h}{t}}\right)$$

where

C_{pp}: fringing capacitance

C_j: formed by the edges of the center conductor

v: speed of light in free space

t: thickness of the center contor

η: free space impedance

More width can be added if it is necessary to tune out the inductance of the transistor at the high end of the frequency band. The width of the high impedance side of the exponentially tapered line is calculated to match the 50 ohms source impedance.

A short-step Chebyshev impedance transformer providing a good match between two different resistances over a wide bandwidth is useful for microwave transistor output networks. Figure 6-5 shows an amplifier consisting of a single overlay transistor, and covering the frequency range from 300 to 450 MHz. The exponentially tapered line provides the

impedance transformation between the 50-ohm driving source and the low input impedance of the transistor. The output circuit consists of a microstrip short-step Chebyshev impedance transformer derived from published tables.[8] The transformer provides the impedance transformation from a 50-ohm load to a 20 ohms calculated collector load impedance. The small inductance connected between collector and ground (through a 0.01 uf bypass capacitor) tunes out the output capacitance of the transistor at the high end of the band.

When the source impedance is 50 ohms, and the frequency range changes from 300 MHz to 450 MHz, the input exponential transformer presents an impedance having a real part which varies from 2 to 3 ohms, and an imaginary part which varies from -j8 to -j6 ohms. The imaginary part is capacitive reactance which tunes out the parasitic lead inductance of the transistor at the higher end of the band. At the same time, the output Chebyshev transformer presents an impedance having a real part which varies from 15 to 25.5 ohms, and an imaginary part which is j8 ohms at 400 MHz. This inductive inductance in conjunction with the reactance (j12 ohms) tunes out the collector capacitance of the transistor.

Coaxial Line and Stripline

Figure 6-6 shows some of the useful circuits in coaxial amplifier circuits. The circuits can apply to either input or output circuits of microwave transistor amplifiers, the specific illustrations being used for discussion only.

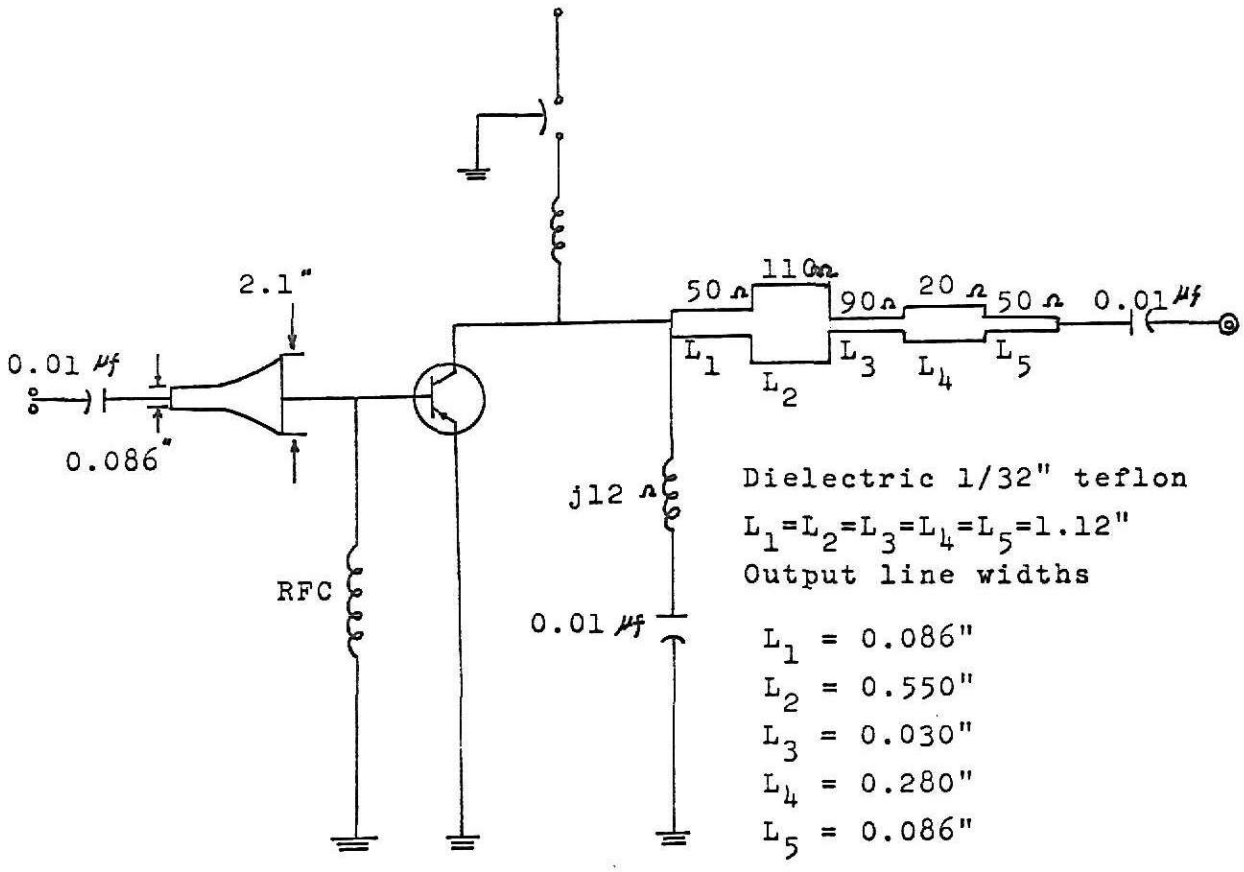


Figure 6-5. Single-stage microstrip amplifier, 300 to 450 MHz, using an RCA 2N5016

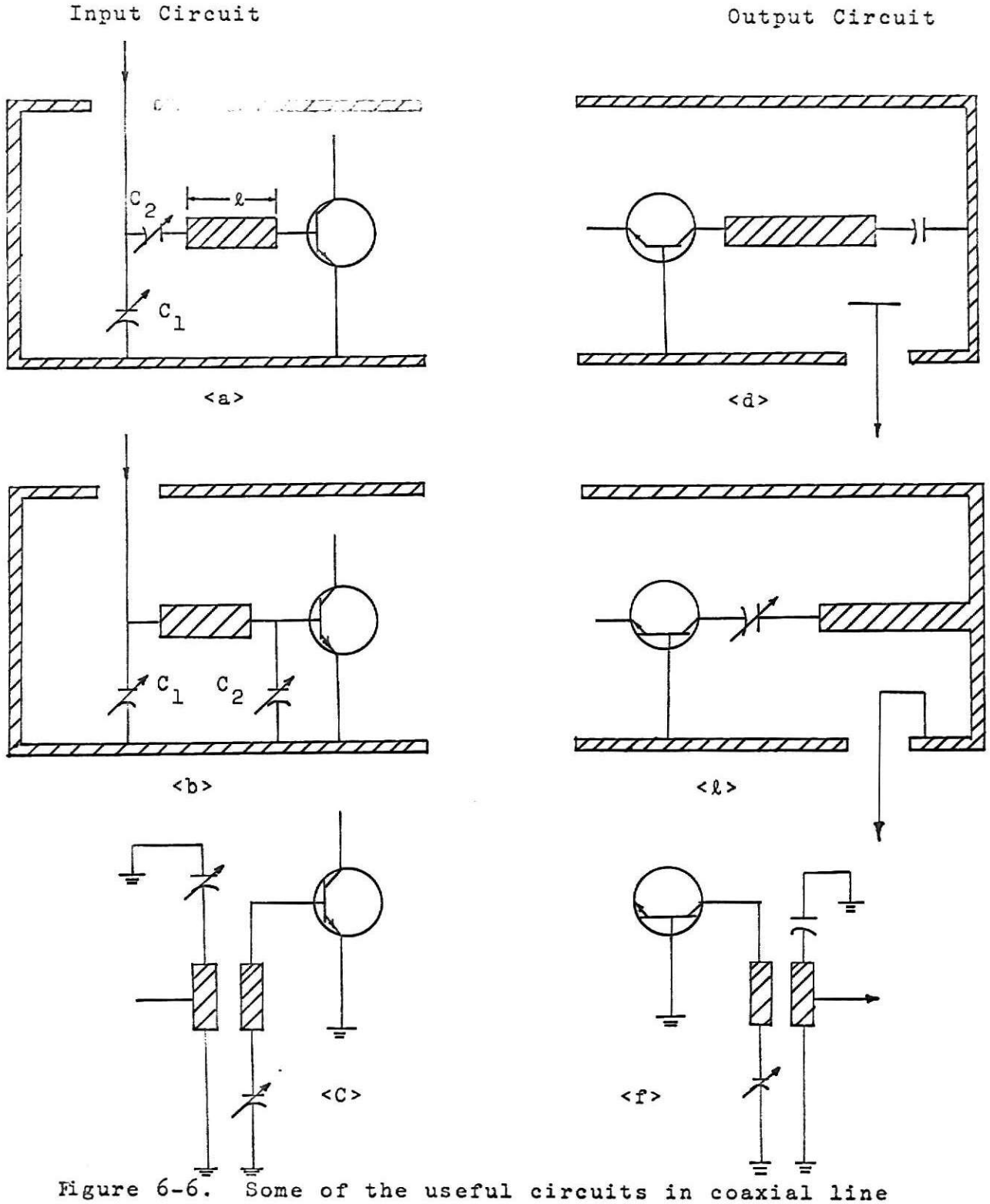


Figure 6-6. Some of the useful circuits in coaxial line configuration

The design procedures for the coaxial line configuration are similar to those described previously for other forms of TEM-mode distributed line sections. The line section of the circuit shown in Figure 6-6a transforms the small input impedance of the transistor to a value closer to the driving source resistance (50 ohms is usual). If ℓ is made $\lambda/8$ wavelength long, then the complex input impedance will be transformed to a real value at the other end of this line and the line VSWR will be minimum. Capacitors C_1 and C_2 are used as reactive dividers. The line length ℓ is less than $\lambda/4$ when the dynamic input impedance is inductive and greater than $\lambda/4$ for capacitive inputs. Capacitors C_1 and C_2 are also used to tune out reactive components, modify reactive components, or adjust the values of real components, depending on the frequency and the characteristics of the line section.

In Figure 6-6b, a quarter-wave line is used for the impedance transformation between the small input resistance of the transistor and the driving source resistance. Capacitor C_2 is used to tune out the inductive component of the input impedance. Capacitor C_1 is used for minor adjustments between transistors.

The design of the output circuits shown in Figure 6-6d and 6-6e are largely empirical. In Figure 6-6d, a capacitive probe is used for the output match to the desired real load. The location of this probe is determined empirically. In Figure 6-6e an inductive coupling loop is used. Again, the design of this coupling loop is largely empirical. In

general, the inductive loop is placed at the ground (or high-current) end of the line, while the capacitive probe is situated at the high voltage end of the line.

The circuits shown in Figure 6-6c and 6-6f make use of inductive coupling and are suitable for stripline circuits. As seen from Figure 6-6c and 6-6f, it is clear that this technique permits additional circuit isolation as well as additional filtering action. The technique can also be used to provide pass-band filtering as well. The design procedure is quite difficult, but in general Wheeler's[14] solution is used in design procedures for the determination of characteristic impedance and wavelength as a function of geometry. Since lengthy computor computations are required, this topic is outside the scope of this report.

Combining microwave power amplifiers

When more microwave power is required than can be provided by one transistor, combination techniques must be used. The conventional "brute force" method of paralleling several transistors at a single point is difficult at microwave frequencies.[16] Power sharing between two devices can not be equalized, and power imbalance in the two devices is high in the method of paralleling directly at the transistor terminals using common tuning. Parallel output using separate stage tuning is still far below the sum of the outputs of the two transistors individually. Hence, a more common method is the use of hybrids to combine several individual amplifier chains or modules, as shown in Figure 6-6. This arrangement

provides a reliable as well as an efficient method to achieve high microwave power. Reliable operation results because of the isolating properties of the hybrid. A failure of one amplifier chain or module reduces only the total power output, but does not cause failure of the other amplifier chains or modules.

A commonly used hybrid is the $\lambda/4$ sections shown in Figure 6-7. Each port is separated from the adjacent port by a $\lambda/4$ section. Because of this arrangement, power introduced at port 1 will appear at equal levels at the adjacent port. In a similar way, power introduced at ports 2 and 3 will combine or add at port 1. The VSWR and the isolation of the $\lambda/4$ hybrid of Figure 6-7 are sensitive to frequency deviations. Another version of the hybrid which is less sensitive to frequency deviation is the quadrature hybrid, as shown in Figure 6-8. The quadrature hybrid accepts an input signal at any of its four ports, and distributes half to a second port and half to a third port with 90 degrees or quadrature phase difference. The fourth port is isolated. Figure 6-9 shows the use of hybrid techniques to generate 10 watts of CW power at 2 GHz using 16 transistors.

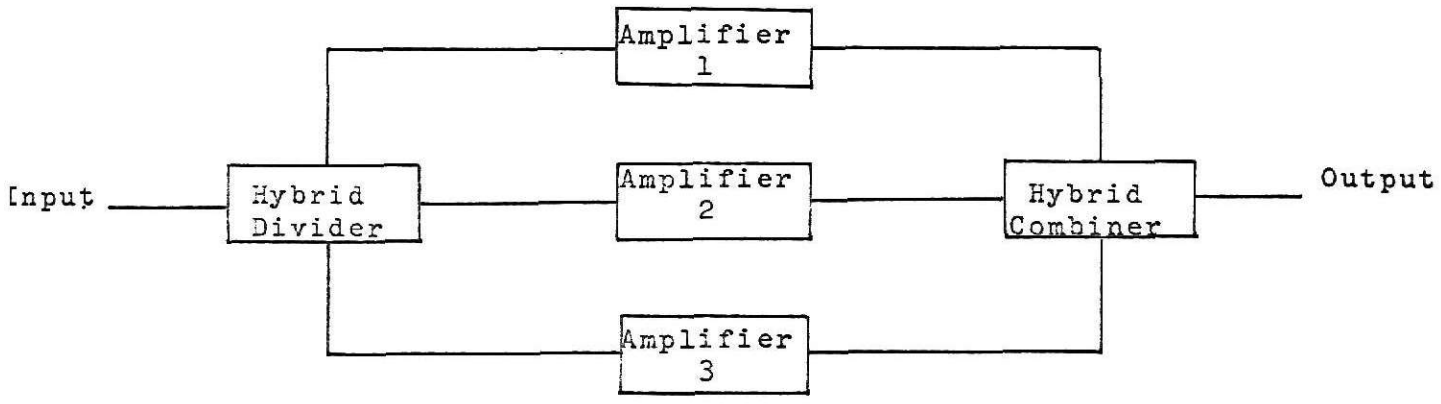


Figure 6-6. Use of hybrid to combine several individual amplifiers

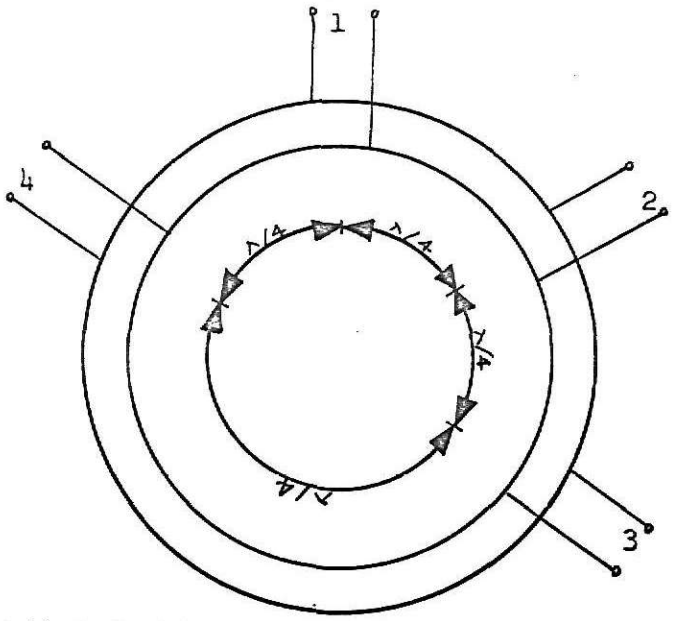


Figure 6-7. The λ/4 hybrid.

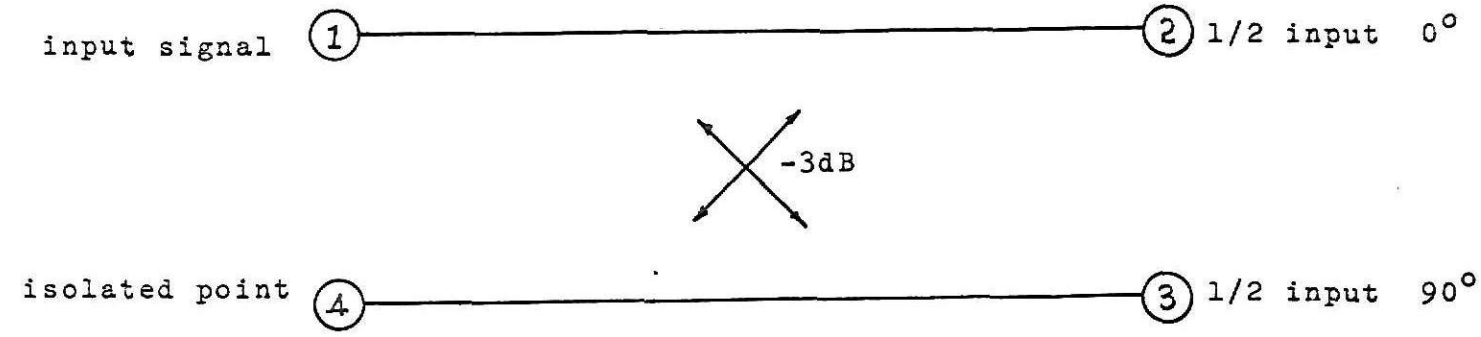


Figure 6-8. Quadrative hybrid.

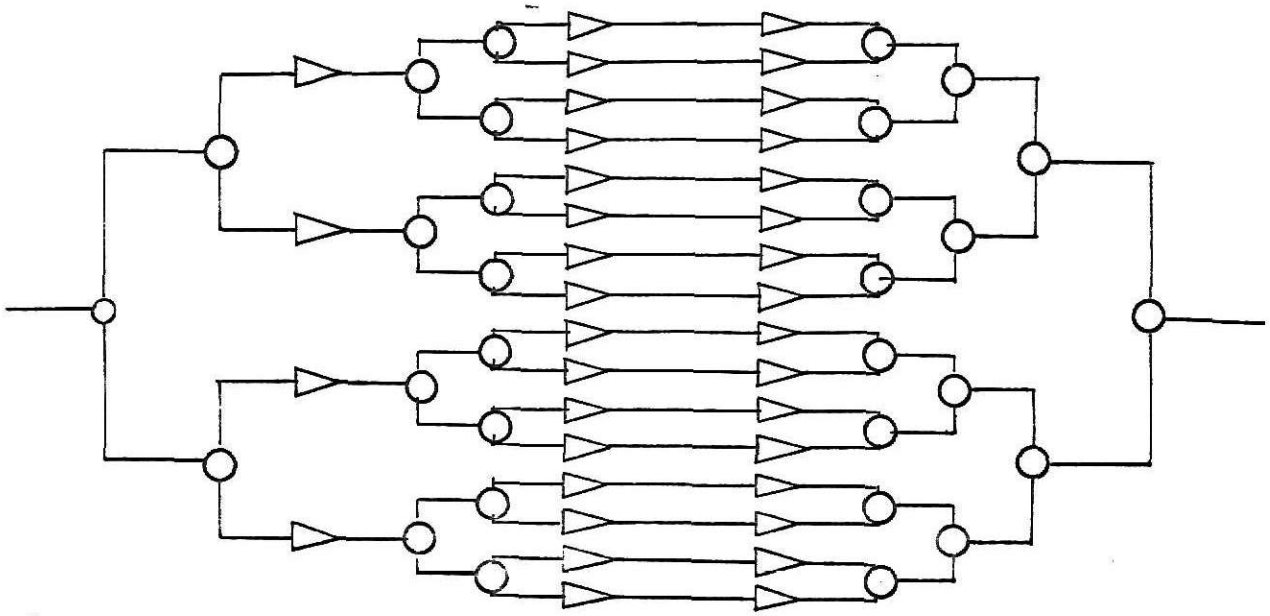


Figure 6-9. A 10-watt, 2 GHz amplifier system using hybrids.

○ hybrid

▷ Amplifier

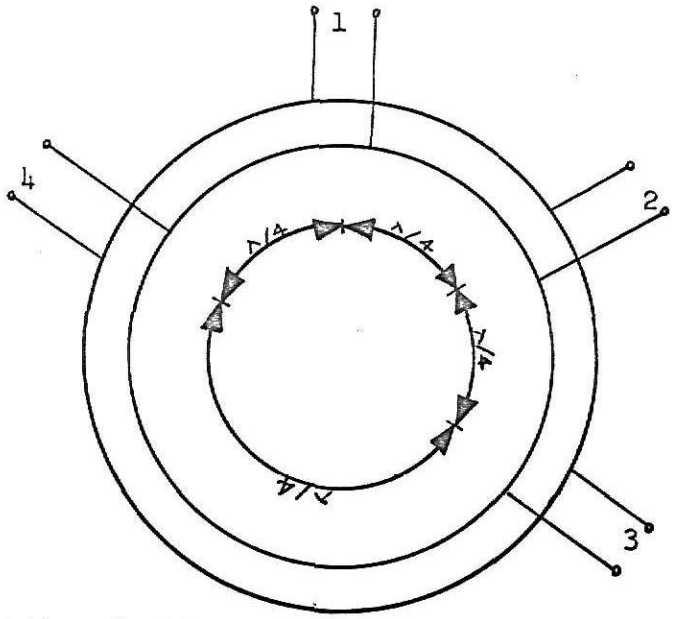


Figure 6-7. The λ/4 hybrid.

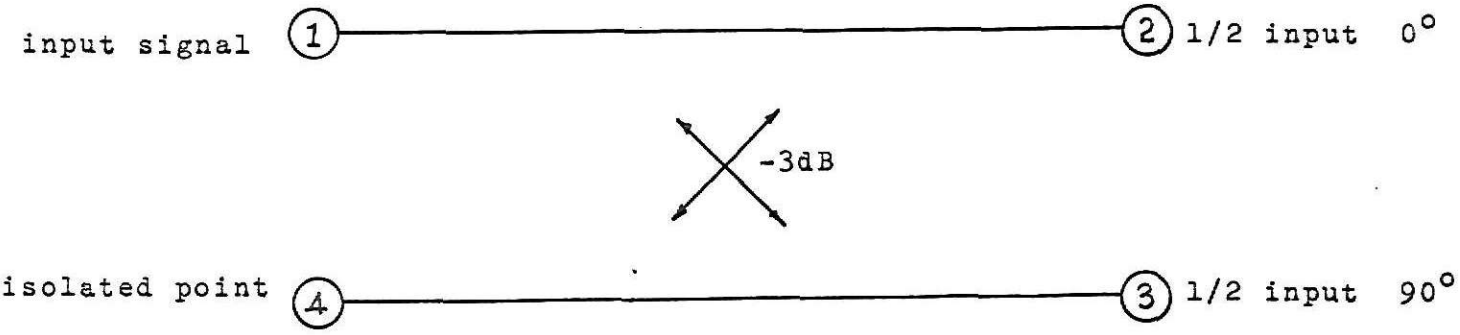


Figure 6-8. Quadrative hybrid.

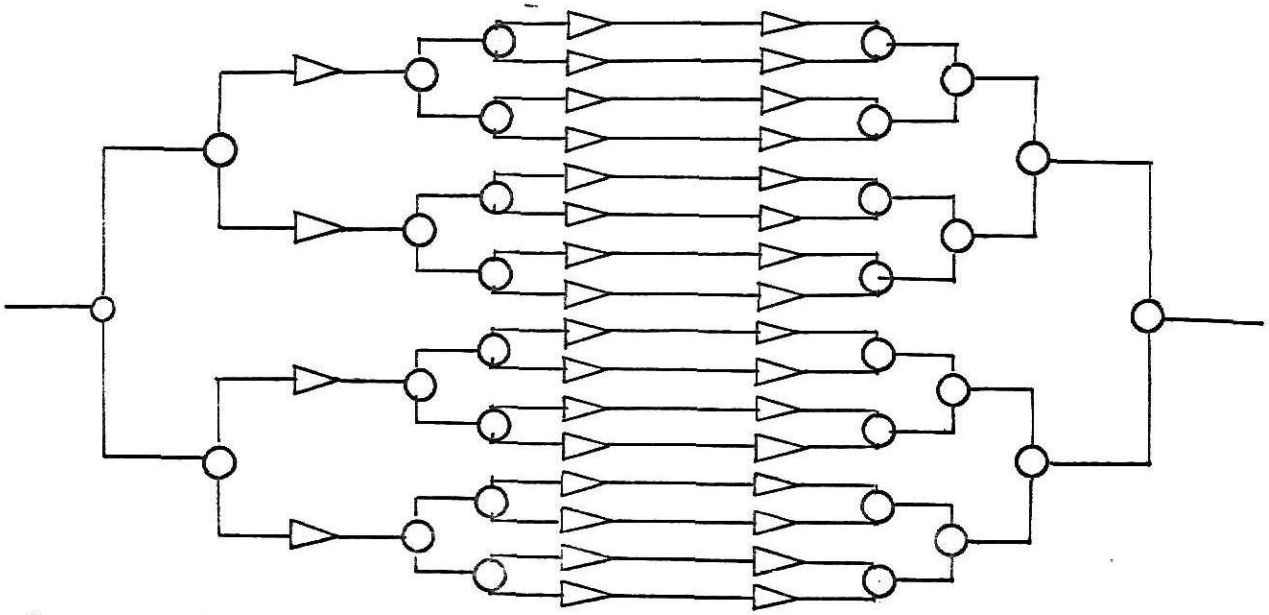
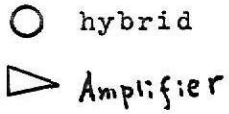


Figure 6-9. A 10-watt, 2 GHz amplifier system using hybrids.



Microwave integrated circuits

The reactance of a lumped element may far outweigh its calculated circuit distribution. Hence, it is necessary to use distributed circuits at microwave frequencies. For example, the use of lumped networks in the 1 to 2 GHz region is almost excluded except for isolated instances. And lumped networks could certainly not be used at any higher frequency. Obviously, the only form of interconnection that is acceptable to planar phototechnology, and still mechanically compatible with integration is microstrip. Using this in conjunction with active and passive elements gives by definition a microwave integrated circuit. There is little analytical work available in the literature to link microstrip geometry and transmission line characteristics over a practical range of variables so as to be generally useful. Recently, Wheeler[14] published an analytical solution whose results agree well with experimental data. Although his solution is of the TEM type, it seems to offer an excellent first approximation to the actual case. Microstrip is quite acceptable for implementing interconnections on a variety of substrates where circuit losses are not prohibitive. For higher frequencies (above X band) where surface finish is more critical, single crystal substrates such as semi-insulating gallium arsenide may be required.

At microwave frequencies a serious problem which has yet to be overcome is how to match the input impedance of the transistor to a 50 ohms source impedance over appreciable bandwidths. The devices operating at microwave frequencies

are running close to or above the common emitter cutoff frequency f_T. This means that when the device is turned on the resistive component of the input impedance is very small compared to the reactance of the device input circuit, and hence the input Q is large. This feature reflects itself in limitations in the maximum input power available and furthermore in the resulting bandwidth. By going to the integrated circuit approach the device is taken out of the package and considerable reduction in undesirable parasitics is realized.

A monolithic microwave integrated circuit runs aground between 500 MHz and 1 GHz because it is not economically feasible to hold the required tolerances and because silicon is not a satisfactory substrate for high performance circuits. Hence, for higher frequencies a hybrid approach must be used.

Measurement of large-signal RF transistor dynamic impedances

Small-signal transistor parameters such as the scattering parameters discussed in the previous chapters are different from large-signal values because of the following reasons:
(1) transistor parameters change with power levels.
(2) harmonic-frequency components must be considered in a microwave power amplifier in addition to the fundamental-frequency sinusoidal component in a small-signal amplifier. Thus, microwave power transistors are normally characterized in a given circuit for a specific application.

The design of microwave power-amplifier circuits involves the determination of input and load impedances. Before the

input circuit is designed the input impedance at the emitter-to-base terminals of the packaged transistor must be known at the drive-power frequency. Before the output circuit is designed, the load impedance presented to the collector terminal must be known at the fundamental frequency. These dynamic impedances are difficult to calculate at microwave frequencies because transistor parameters such as S_{11} and S_{22} vary considerably under large-signal operation and also change with the power level. Small-signal equations that might serve as useful guides for transistor design can not be applied rigorously to large-signal circuits. Because large-signal representation of microwave transistors has not yet been developed, transistor dynamic impedances are best determined experimentally with slotted-line or vector voltmeter measurement techniques.

The system used for the determination of transistor impedances under operating conditions is shown in Figure 6-10. This system[5] consists of a well-padded power signal generator, a directional coupler for monitoring the input reflected power, an input triple-stub tuner, a low-impedance line section, the transistor holder, an output line section, a bias tee, an output triple-stub tuner, another directional coupler for monitoring the output waveform or frequency, and an output power meter. For a given frequency and input power level, the input and output couplers are adjusted for maximum power output and minimum input reflected power. Once the system has been properly tuned, the impedance across terminals 1-1 (without the transistor in the system) is measured at the

same frequency in a slotted-line setup or with the vector voltmeter. The conjugate of this impedance equals the dynamic input impedance of the transistor. Similarly, the impedance across terminals 2-2 (without the transistor in the system) is the collector-load impedance presented to the transistor collector. Such measurements are performed at each frequency and power level. Thus, power output, power gain, and efficiency are readily determined. For optimum performance the line length and the characteristic impedance Z_o of the input line $_1$ and the output line $_2$ must be carefully chosen. Eighth-wavelength line sections are preferred for lowest line VSWR and losses.

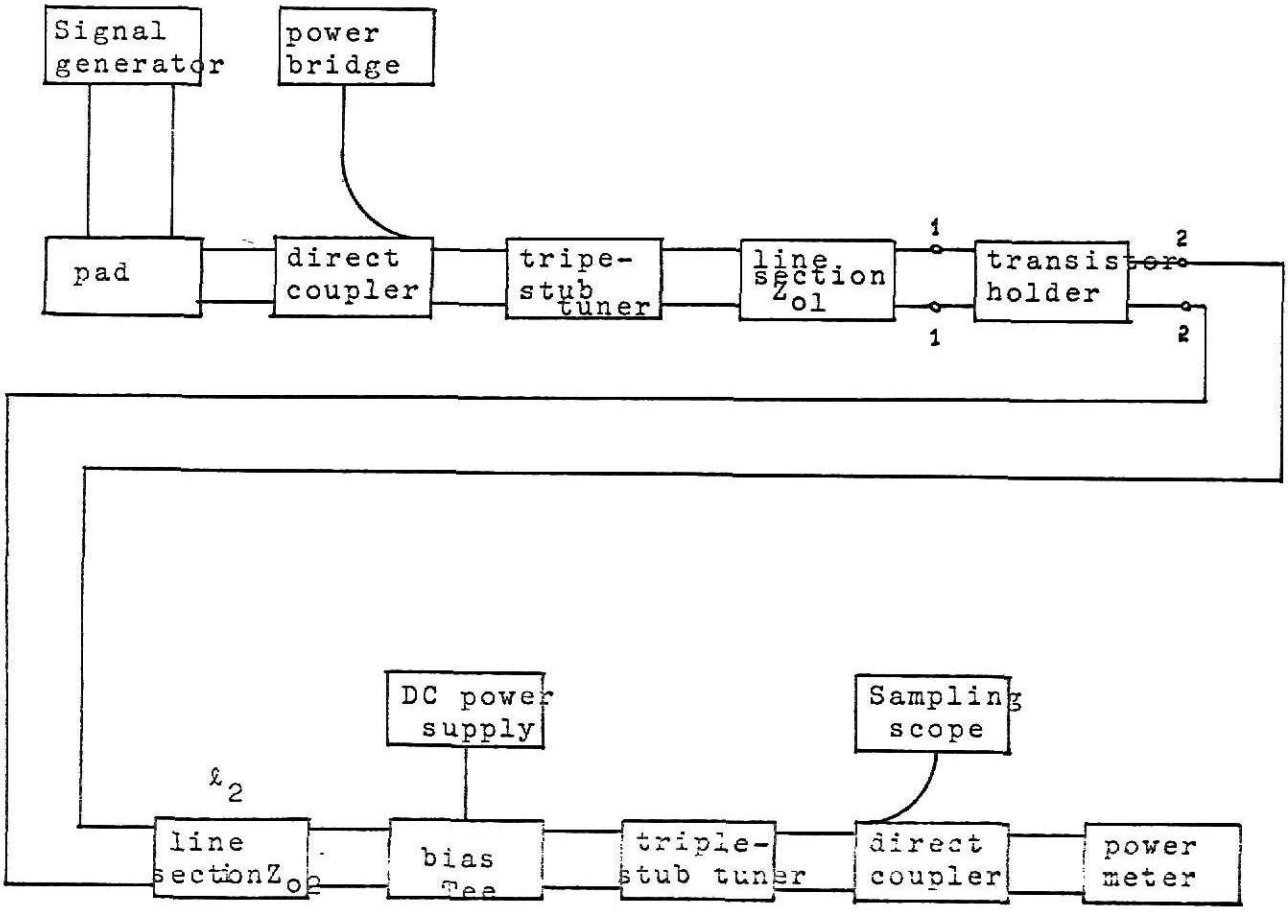


Figure 6-10. Setup for measurement of RF transistor dynamic impedance.

Chapter 7

CONCLUSION

All RF transistors are classified into small-signal and large-signal transistors. This classification depends upon the linearity of operation, not on any arbitrary signal level.

Because large-signal RF transistors are normally characterized in a given circuit for a specific application, a better understanding of the characteristics of a RF power transistor is necessary. The RF characteristics of a RF transistor almost always depend on the fabrication of the transistor. Hence, the basic constructions of the overlay and interdigitated transistors are introduced. Next the effect of fabrication on microwave performance is discussed in Chapter 1. In Chapter 1, the answers to the following questions can be found:

(1) Why is overlay geometry currently the most popular design for achieving high-frequency performance in a power transistor?

(2) Why have overlay transistors accelerated the conversion from vacuum tubes to semiconductor devices?

(3) What is the major difference between overlay and interdigitated RF transistors?

But above all, the concept that a transistor for higher frequencies and higher power outputs in a given physical chip area must have increased active-to-physical area ratio is the most important thing in Chapter 1. In Chapter 2, some important RF transistor parameters and the interrelation

between dc and RF parameters are discussed in more detail. These important parameters are common emitter h_{FE}, dc and RF breakdown voltages, dc collector-emitter saturation voltage, RF saturation voltage, output and input impedance, packaging, reliability, and stability. It is found that characteristics of a RF transistor depends greatly on the fabrication of the transistor.

In both Chapter 1 and Chapter 2, the characteristics of large-signal RF transistors are emphasized while the characteristics of the small-signal RF transistors are almost excluded in these two Chapters. In Chapter 3, 4, and 5, only small-signal RF transistors are considered. The values of the h, y, or z parameters, ordinarily used in small-signal transistor circuit design at lower frequencies, can not be measured accurately above 500 MHz because of the difficulty of establishing the required short and open circuit conditions. But from Chapter 3, 4, and 5, it is obvious that a small-signal RF transistor can be well characterized by the use of scattering parameters. In Chapter 3, the incident and reflected power waves are introduced. The physical meaning of these power waves and some properties of the scattering matrix as defined by incident and reflected power waves are discussed. It is worthwhile to mention that these power waves are very useful. They can be used for the discussion of noise performance of negative resistance amplifiers[9] and for the discussion of actual noise measure of linear amplifiers.[6] They can be used also to study the attenuation error in mismatched systems.[12] Noise figures of

RF transistors can be expressed in terms of these power waves or the scattering matrix.[11]

An equivalent circuit of a microwave transistor can be derived by the help of scattering parameters.[1] Two port power flow can be analyzed by the use of the scattering parameters. The fundamental concepts of the power waves introduced in Chapter 3 are very helpful for those people using them as a tool to analyze electrical networks[2]. Conditions for a lossless as well as reciprocal network are also given in Chapter 3. Two measuring systems, one considering the unknown transistor as a three-port network, the other considering the unknown transistor as a two-port network are introduced, and a brief comparison between two measuring systems is made in Chapter 4. When the three-port s-parameters system is compared with the two-port s-parameters system, the former provides some advantages over the later. The three-port scattering parameter system is good for measuring microwave integrated circuits and thin film integrated circuits.

In Chapter 5, a method of using s-parameters in the analysis and design of a small-signal transistor amplifier is introduced. If the reverse transmission parameter S_{12} of a RF transistor is neglected, and the transistor considered as an unilateral-circuit, the design of a RF small-signal transistor amplifier is easier. A step by step method is given for designing a small-signal transistor amplifier. Finally, in Chapter 6, some fundamental and useful microwave transistor circuit design techniques are presented. The

properties and applications of the following transmission line sections are discussed,

(1) Half-wave line sections

(2) Quarter-wave line sections

(3) Eighth-wave line sections

(4) The exponential line

(5) Chebyshev transformers.

The combining of microwave power amplifiers and microwave integrated circuits is briefly mentioned. A setup for measurement of large-signal RF transistor dynamic impedance is also briefly mentioned.

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RADIO FREQUENCY TRANSISTORS

by

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Diploma, Taipei Institute of Technology, 1962

AN ABSTRACT OF A MASTER'S REPORT

submitted in partial fulfillment of the

requirements for the degree

MASTER OF SCIENCE

Department of Electrical Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

1970

ABSTRACT

In recent years, transistors have been developed for applications in L-Band and S-bands. It is reasonable to believe that the frequency-power handling capability of a transistor will be boosted in the near future. In general, microwave transistor performance is affected by the fabrication of the transistor. Hence, the two most widely used construction methods are introduced first, and then the RF transistor parameters and trade-offs in circuit design are discussed. The values of h, y, or z parameters, ordinarily used in small signal transistor circuit design at lower frequencies, can not be measured accurately above 500 MHz because of the difficulty of establishing the required short and open circuit conditions. Therefore, the scattering parameters are introduced. The measurement of scattering parameters for transistors and a small signal RF transistor amplifier designed by the use of scattering parameters are briefly presented. Finally, some useful techniques in designing microwave transistor circuits are introduced, but the techniques of designing microwave integrated circuits are not within the scope of this report.