

Design of a photomultiplier tube high-voltage power supply base for
integration into three-dimensional additive manufacturing

by

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Abstract

A photomultiplier tube high-voltage power supply was designed to be additively manufactured. It includes a Cockcroft-Walton voltage multiplier circuit for voltage multiplication. The low component count and small volumetric design is an alternative concept to typical Cockcroft-Walton ladders used to power photomultiplier tubes. When properly implemented, the Cockcroft-Walton ladder can be simplified in both component size and circuit implementation for hybrid three-dimensional printing. The new design simplifies embedding circuitry into three-dimensional shapes, while helping achieve minimal package footprint and reliability such that it is more compatible with three-dimensional printing of electronic circuitry.

This work includes an overview of the Cockcroft-Walton ladder for use with photomultiplier tubes, basic nuclear pulse processing circuitry, an in-depth analysis of the Cockcroft-Walton configurations, and an initial design used as the basis of this research. Additionally, the Cockcroft-Walton control circuitry and ladder design were simplified and documented from component selection to finalized design. Finally, successful fabrication of a minimized Cockcroft-Walton voltage generation circuit on a standard printed circuit board was constructed.

Basic benchmark testing was conducted with the circuit to analyze the efficiency in power consumption and performance using radiation spectroscopy with a Cesium Iodide scintillation crystal. A 16-stage Cockcroft-Walton ladder design was able to achieve power consumption reduction of 8%, 7.5 mW to 6.9 mW. Component count was reduced by 17%, 166 components to 137 components with simplification of circuit architecture. Energy resolution of the photomultiplier tube with Cesium Iodide scintillation crystal was able to achieve 7.8%, in comparison to the manufacturer engineered base at 7.5% under similar operating conditions.

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Chapter 1

Introduction

1.1 Motivation

For the past couple of years, a research team at Kansas State University has been developing a high-voltage power supply and signal processing circuitry for the Hamamatsu R11265U series photomultiplier tube (PMT)¹. The design of this circuitry is intended to be manufactured at Kansas State University using an additive manufacturing technique through an nScript 3D printer⁴. This traditional circuitry representation has advanced through multiple revisions since its derivation, and has been put through laboratory testing to verify functionality.

Within the last year, the shift in terms of circuit design focused to optimizing the design to decrease the component volume and power consumption by altering the base circuitry. The goal was to develop the circuitry in such a way that the additive manufacturing technique could be fully realized, and the full advantages of three-dimensional (3D) design could be explored. Further efforts have been made to develop circuitry using a Cockcroft-Walton voltage multiplier to supply voltage for a PMT. Additionally, circuit parameters for pulse shaping circuitry, as well as any circuit dependencies were refined to support gamma-ray spectroscopy.

There are advantages to improving the circuitry design. The main advantage is the decrease in component volume and power consumption. It also provides students with the opportunity to explore the possibilities of circuit integration into additive manufacturing using the nScript 3D printer. This is an exploratory process since complicated circuitry embedded into 3D printed structures is still an emerging technology. Additional exploration of creating circuit sub assemblies with a laser welder to be coupled with the nScript 3D printer capability is also being investigated.

One of the most prominent portions of the circuit design for this application is the generation of the high-voltage used to power the PMT. The details of the work herein, highlight the design and verification of the circuitry configuration.

1.2 Prior Work

The high-voltage circuit configuration as a basis for this circuitry was originally invented between 1919 and 1921 by Heinrich Greinacher as a voltage doubler⁵. It was further used in 1932 by John Cockcroft and Ernest Walton to power their particle accelerator producing roughly 700 kV⁵⁻⁷. This eventually led to the pair gaining a Noble Prize in Physics in 1951⁸. This introduced the scientific community to the circuit now known as the Cockcroft-Walton ladder. In 1976, Dickson extended the Cockcroft-Walton circuitry by modifying it to multiply direct current (DC) producing a DC-to-DC converter using a circuit configuration known as a "charge pump" which requires a clocked pulse input to charge the capacitors⁵.

Regardless of name, the basic idea of the Cockcroft-Walton still is used today in multiple electronic devices that require a higher voltage than that of the supply. Examples of such electronic devices include cathode ray tube televisions, X-ray machines, microwave ovens, and photomultiplier tubes (PMTs)⁹.

PMTs are a common photon sensor and electron multiplier used in the nuclear industry as a method for radiation detection. These devices typically do not require large amounts of

current, however, they do require large voltages to drive each dynode stage of the PMT, normally on the order of 1 kV¹⁰. This makes the Cockcroft-Walton voltage multiplier a desirable candidate to act as a supply for the PMT. PMT manufacturers typically provide an optional base that will adequately supply the necessary voltage for the PMT, however, they are known to increase the size of the detector significantly, as well as have limitations that are not well suited for designing the system to be portable.

Previously documented work of the Cockcroft-Walton design used with PMTs was explored in 1998 as a removable base for the FEU84-3 photomultiplier tube¹¹. This design produced the desired voltage to power the FEU84-3 photomultiplier tube, but at the expense of an increased circuitry size. In this case, the Cockcroft-Walton design doubled the size of the FEU84-3 photomultiplier tube with a maximum power consumption of 150 mW¹¹. This design was an advancement as a new kind of device for the time period, but it did not focus on any reduction in power consumption and ripple voltage. It also did not reduce the overall size, as current trends in electronic circuitry focus on smaller more compact designs. Another use of the Cockcroft-Walton multiplier was for the photomultiplier tubes KM3NeT deep sea neutrino telescope which resulted in a 38 mm diameter enclosed system with power dissipation of 102.3 mW¹². The amount of power could still be reduced with some additional design adjustments and the size could greatly have been reduced. Finally, a group in collaboration with Matsusada Precision Incorporated developed a Cockcroft-Walton for use with a KOTO detector¹³. This design created a high-voltage control system that consisted of twelve separate controller modules connected to a computer¹³. This could then support up to twelve different Cockcroft-Walton voltage multiplier designs and twelve different photomultiplier tubes¹³. Each of these control modules had a power consumption of 60 mW¹³.

Additional refinement of physical size and power consumption could be made in each of the previous cases. This supports investigating what configuration would be optimal for use with photomultiplier tubes and allow for a reduction in size and power consumption, as well

as what modifications could be made to adapt such circuit to incorporate it into an additive manufactured circuit.

1.3 Design Goals

The main goal of this work was to design a Cockcroft-Walton necessary for powering the Hamamatsu R11265U PMT for additive manufacturing. However, there are many additional goals and considerations that were necessary to adhere to in order to achieve this overall goal. Overall, specific design goals included:

1. Optimizing the Cockcroft-Walton design to have low-power consumption.
2. Retain low-power consumption at increased radiation count-rates.
3. Minimize volumetric size for individual components selected for the design.
4. Minimal component count to allow straightforward integration into a 3D design.

1.4 Main Contributions

The design and verification of the high-voltage supply through a series of simulation and physical testing has made the following key contributions to the field of nuclear science:

1. Design of a Cockcroft-Walton ladder and supporting circuitry necessary for powering the Hamamatsu R11265U series photomultiplier tube.
2. Documentation of the design process for reconstruction with other photomultiplier tubes.
3. A list of lessons learned and possible improvements to guide future research endeavors for circuit design related to hybrid additive manufacturing.

Chapter 2

Background

2.1 Additive Manufacturing

Additive manufacturing, or 3D printing, is a process that produces a three-dimensional product from the successive build-up of layers through a variety of different substrates. Fused Filament Fabrication is an additive manufacturing approach that uses a plastic filament extruded through a heated nozzle, building up one layer at a time. This concept allows for creation of complex geometries without need for specific tooling such as dies or molds¹⁴. Over the past several years, 3D printing has evolved into adapting capabilities combining various processes, such as combining the placement of electrically coupled components with assistance from the pausing process of the 3D printer.

Placing circuit architecture inside of 3D printed structures is a recent process referred to as hybrid 3D printing. Research into the ability to embed circuits into 3D printed structures has taken place in RF design through 3D printed antenna and microstrip lines¹⁵. The antenna structures and RF microstrip circuitry are printed on varying surfaces¹⁵. An nScript 3D printer has been used to print embedded circuitry, such as simple LED circuitry to demonstrate resistor and capacitor placement tests^{4;15}. Furthermore, a complex 144 pin FPGA system was printed on a kapton substrate with around 30 additional passives¹⁶.

Additional work by another research group reported a new method in which a conductive electrode ink was applied to act as traces¹⁷. A pick-and-place machine was used to place electrical components into a soft electronic system based on thermo-plastic polyurethane (TPU) to apply power to an LED system¹⁷.

At this time, any additive manufacturing techniques coupled with electronic devices have been small sub-assemblies, or small demonstrative circuitry with minimal components, not fully functional or integrated systems^{4;14–16}. Many of these circuits previously identified have been planar configurations in nature, and have not leveraged the full three-dimensional capabilities that can be developed using a 3D printing medium. One advantage to using this medium would include the ability to place the components in a non-planar fashion. This in turn would allow for the circuitry size to greatly be reduced in comparison to the two-dimensional printed circuit boards typically used in electronics applications.

2.2 Photomultiplier Tubes

The photomultiplier tube was originally invented in 1936 by the RCA Corporation in the United States of America¹⁸. PMTs are optical sensors that detect varying levels of radiation in its surrounding environment, typically in the infrared wavelength of light. Using the photoelectric effect, the PMT absorbs the energy of a photon and as a result releases a free electron. Through each emission, the electrons are channeled through a series of dynodes, or specialized electrodes to multiply the gain of the electron signal as they propagate through the PMT^{18;19}. By providing a significant multiplication of electrons, the PMT produces a signal current large enough to be measured and used for signal measurement. A PMT will output 10 nA to 300 μ A of current, but radiation detection applications reduce that range to 10 nA to 100 nA²⁰.

In regards to nuclear radiation detection circuitry, the size of the PMT electrical system is governed by the size of scintillation crystal. The scintillator crystal is a primary component

of the detector and can vary in size from millimeters (14 mm x 14 mm), to several hundred millimeters (101.6 mm x 101.6 mm x 406.4 mm)^{21;22}. The PMTs that attach to these scintillators are designed to be a variety of sizes and shapes based on the necessary power and pulse processing needed for the crystal. However, a single base can adapt to support various sizes of scintillator crystal/PMTs with no additional circuitry.

One objective in this work was to minimize the volume of the electronics for the PMT. A goal was set to fit the entire electronic base of the PMT in the metallic housing that extended away from the body along the connector pins. However, it is crucial to understand that this thesis is focused on the design of the electronic system to be used and not the additive manufacturing technique. The overall component selection detailed herein was chosen to test the limitations with the nScript 3D printer and to optimize the circuit footprint provided a 3D structure be completed.

Scintillators are additional structures that can be attached to PMTs to provide sensitivity to ionizing radiation. Scintillators may also provide spectroscopic capability of gamma-rays, resolving different energies. Like many optical systems, scintillation crystals can vary in material, density, and refractive index¹⁸. The scintillation crystal will absorb gamma-ray energy and release a number of photons that are desired to be proportional to the absorbed energy. The photons collected by the PMT produce a measurable electrical signal.

For this particular design, however, the team focused on using the Cesium Iodide material, more specifically Cesium Iodide activated with Sodium (CsI(Na)). In particular, the CsI(Na) emits at 420 nm light, has an 85% photoelectron yield for gamma-rays²³. The high light yield makes CsI(Na) a candidate for fundamental radiation spectroscopy as it is able to yield 41 photons/keV²³. Furthermore, the CsI(Na) is a rugged option for mobile radiation detection environments. Additionally, the primary decay time for this scintillation crystal is 630 ns with decay constant of 1 μ s²³. The decay time will be integral for electronic design for timing applications related to pulse processing.

In this sensor configuration, the scintillator is integrated and attached to the PMT. The entire CsI(Na) crystal and PMT is seen in Figure 2.1.

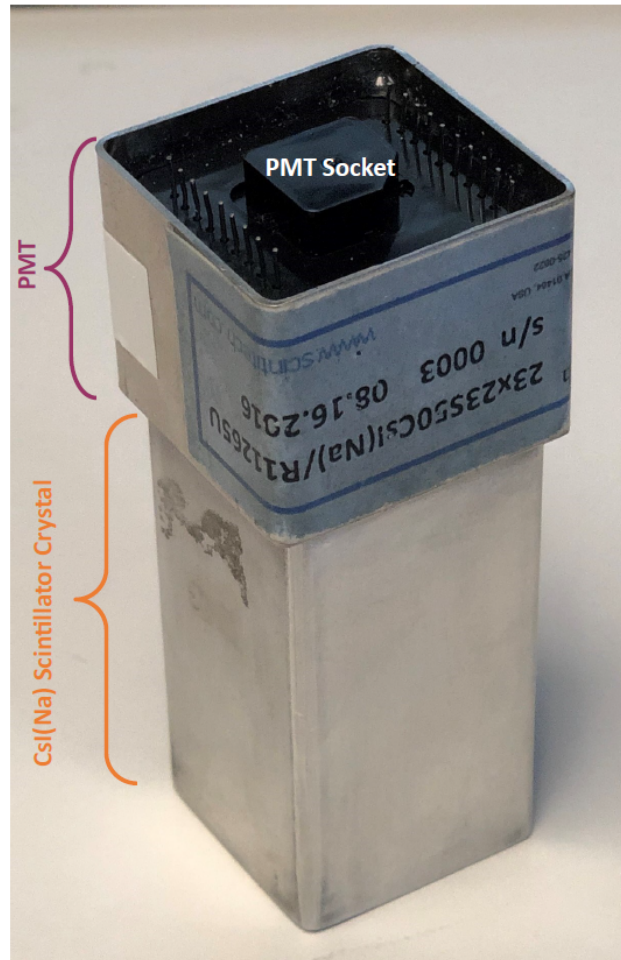


Figure 2.1: Hamamatsu R11265U series PMT with 1 inch by 1 inch by 3 inch CsI(Na) scintillation crystal and PMT socket connection.

As one could expect, the PMT needs a specially designed base that attaches to it in order to power the dynode structure used to amplify the gain of the electrons. Some PMTs require hundreds, even thousands of volts to adequately activate the electrode dynode stages. The scintillation crystal used for this design is either the 1 inch by 1 inch by 3 inch CsI(Na) or 1 inch by 1 inch by 2 inch CsI(Na), both integrated with the Hamamatsu R11265U Series PMT.

The Hamamatsu R11265 PMT base, in particular, is expected to energize a total of 12 individual dynode stages, with a manufacturer specified value for the the anode to cathode voltage. In the datasheet for the PMT, the value of this voltage is $\pm 900\text{ V}$ ¹. However, it was observed during initial testing with the manufacturer PMT base that the crystal would begin sending adequate signal out of the CsI(Na) anode at $\pm 650\text{ V}$. Originally, the goal of the 3D printed base designed for this additive manufacturing was to hit a target value of between 650 V and 1 kV between the anode and the cathode of the scintillator. Upon further review, the team decided to negatively bias the voltage but keep the similar constraints.

To physically energize the dynode stages, a voltage bias is applied to each dynode. The data sheet for the Hamamatsu R1125U PMT base specifies two different ratio configurations to distribute the bias voltage, the Standard and the Tapered divider type¹. These two configurations alter the linearity of the voltage divider between dynode stages. The Hamamatsu R1125U ratio divisions are summarized in Table 2.1, where K is the anode, and P is the photocathode component.

Table 2.1: Hamamatsu voltage distribution for Standard and Tapered divider ratio at $+900\text{ V}$ ¹. The number represents the ratio of the stage. For example, under the Tapered the 1.6 under Dy3 (dynode 2) represents a 1:1.6 ratio between dynode 2 and dynode 3.

Electrode	K	Dy1	Dy2	Dy3	Dy4	Dy5	Dy6	Dy7	Dy8	Dy9	Dy10	Dy11	Dy12	P
Standard		2.5	1.3	0.8	0.8	1	1	1	1	1	1	1	1	0.5
Tapered		3.3	1.6	1	1	1	1	1	1	1	1	1	2.7	1.3

In order to design circuitry to take the manufactured base's place, the configurations presented in Table 2.1, were examined. Getting voltage ratios of fractional magnitude is difficult due to the nature of the Cockcroft-Walton stages being identical, so values were rounded as seen in Table 2.2.

Table 2.2: Estimated voltage distribution for Standard and Tapered divider ratio at $+900\text{ V}$.

Electrode	K	Dy1	Dy2	Dy3	Dy4	Dy5	Dy6	Dy7	Dy8	Dy9	Dy10	Dy11	Dy12	P
Standard		3	1	1	1	1	1	1	1	1	1	1	1	1
Tapered		3	2	1	1	1	1	1	1	1	1	1	3	1

The sum of the ratios for the Standard and Tapered dividers in Table 2.2 results 15 and

17 respectively. An estimate of 15 stages for Standard, and 17 for Tapered stages are necessary to set voltage ratios to drive the PMT dynode stages. The average of the two values, resulted in 16 necessary stages to acquire the desired ratio. Taking a closer look at Table 2.1, Hamamatsu designed their base to have higher voltage ratios for the first couple of dynode stages, and then again at the last of the dynode stages with a ratio of 1:1 in between. Taking this into consideration, the 16 stage base ratios are found in Table 2.3.

Table 2.3: Custom divider ratio at 900 V.

Electrode	K	Dy1	Dy2	Dy3	Dy4	Dy5	Dy6	Dy7	Dy8	Dy9	Dy10	Dy11	Dy12	P
Custom		2	2	1	1	1	1	1	1	1	1	1	1	2

Comparing the estimated voltages for both the standard and tapered configuration to the Hamamatsu specified voltages, the voltages at each stage stay within $\pm 3\%$ except for the initial increase for the first dynode seen in Figure 2.2. The initial estimated voltage for the first dynode stage is less for the custom circuit because the standard and tapered design ratios were truncated from 3 to 2 to keep the number of stages to the estimated 16 for the custom circuitry.

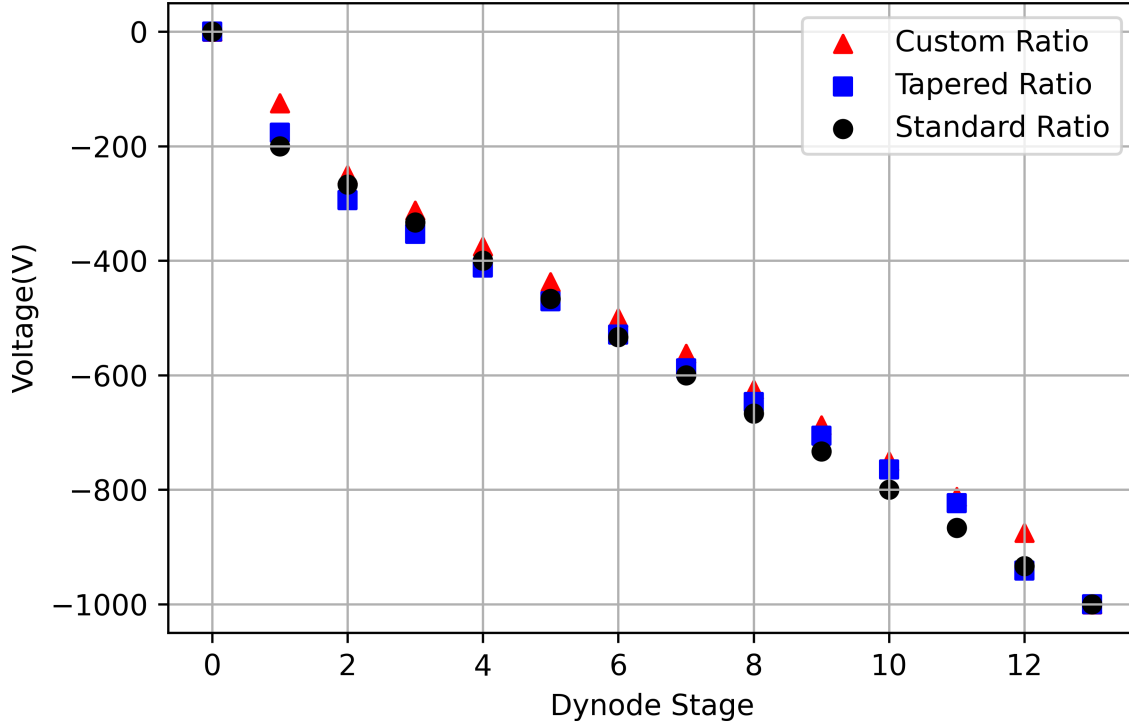


Figure 2.2: Estimated voltage distribution at -1000 V for standard and tapered configuration compared to the voltage for the designed ratio configuration. The estimated values stay within $\pm 3\%$ with the exception of the first stage which is crucial for energy resolution.

To connect the base to the PMT, the socket assembly has a series of 19 pins with various connections as seen in 2.3. Additionally, the socket connection contains a plastic key in the middle to ensure proper alignment when using the Hamamatsu manufactured socket connector. Another defining feature of the socket connection is that in each column of pins, there is a different number of pins. The PCB circuit presented uses the varying number of pins as the key to ensure the user is placing the circuit onto the PMT correctly, while the 3D circuit will use the alignment key structure similar to Hamamatsu.

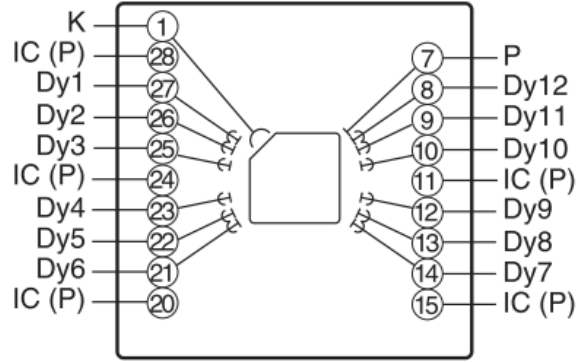


Figure 2.3: Hamamatsu PMT socket connection diagram with 19 pins. The cathode connection is represented by K, the anode is represented by P, the dynode stages are represented by Dy#, IC represents internal connections and are not connected to the to the external pins¹.

2.3 Radiation Detector Pulse Processing

When using PMTs pulse processing the output pulse is important in order to gather useful data. One common pulse processing arrangement is pulse shaping such that the output voltage pulse height is proportional to the detector pulse amplitude²⁴. Traditional nuclear instrumentation pulse processing for radiation detection can be summarized into two key elements: the preamplifier, and the shaping amplifier.

2.3.1 The Preamplifier

The preamplifier circuit is composed of amplifier circuitry used to transition the PMT current pulses generated by the releasing of the electrons into a detectable voltage signal. The function of the preamplifier is to extract the signal without interfering with the signal-to-noise ratio (SNR), or induce further noise into the system²⁴. The SNR is a ratio of the signal current, present when signal is produced by light, and the dark current, the current present without light input, often signal noise.²⁰.

A shunt resistor to ground, followed by a DC block capacitor is typically placed on the output of the detector before any additional amplifier circuitry as seen in Figure 2.4. The

resistor translates the current produced by the PMT to a detectable voltage, and the DC blocking capacitor filters out any DC components. This filter acts to blocks the high-voltage input into the signal processing circuitry.

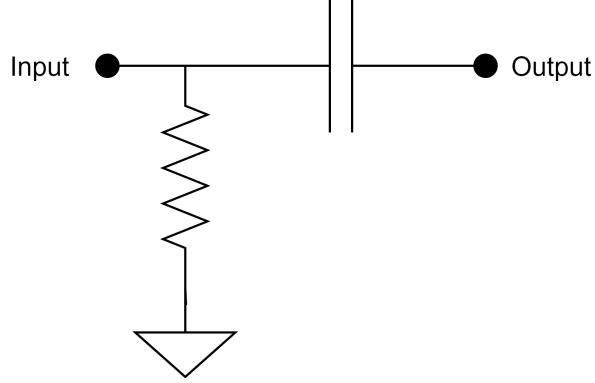


Figure 2.4: The resistor and capacitor network used to translate the current signal produced by the PMT to a voltage.

The subsequent pulse output, follows the general decay Equation 2.1, where the time constant, τ is defined by the time constant of the PMT crystal. This is generally the case as the preamplifier is designed to preserve the pulse characteristics²⁵. The amplitude, A , is dependent on the signal amplitude being produced by the PMT, and is primarily dependent on the particular particle energy detected²⁶.

$$Ae^{-t/\tau} \quad (2.1)$$

This detector pulse is then fed into the preamplifier. The preamplifier is responsible for integrating the charge, and consequently adding a long RC tail to return to the baseline. These input pulses can range from a few μs to a few ps in duration²⁴⁻²⁶.

A primary preamplifier configuration, the charge-sensitive preamplifier was the optimal choice for this implementation²⁴. This is due to the fact that the input of the preamplifier may be made small, such that this configuration is efficient for detecting the current signal of the detector²⁴. Typical parameters of interest when doing energy spectroscopy involve the quantity of charge and/or the event timing, which a charge-sensitive preamplifier

can be used to detect²⁵.

Additionally, a preamplifier allows for detector flexibility under a single design. Using a single design is possible due to the fact that the input charge is integrated over a feedback capacitor. Therefore, the gain is not as responsive to change in detector capacitance²⁵. For this reason, different detectors can be used with one design. An example of the charge-sensitive preamplifier circuit can be found in Figure 2.5.

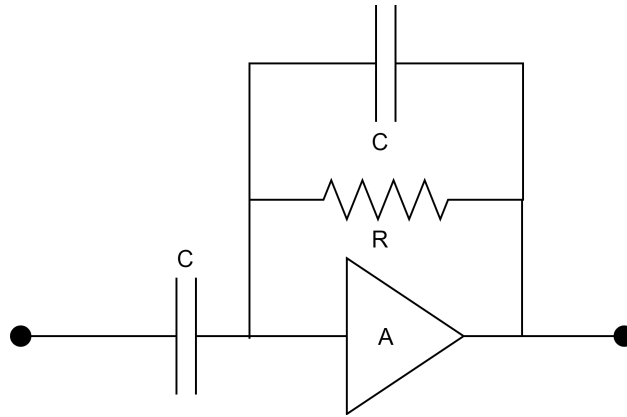


Figure 2.5: The preamplifier circuit used to integrate the charge into a voltage pulse that is fed into the shaping amplifier circuitry.

2.3.2 The Shaping Amplifier

The shaping amplifier is used to eliminate the long tail and provide suitable voltage levels for an analysis system, such as a multichannel analyzer (MCA). These values typically range between 0 V to 10 V²⁷. Because the preamplifier can output pulses on the range of a few 100 mV to 1 V, the gain induced in the shaping amplifier circuitry is 1 to 100 times. These amplifier systems must contribute large gain while minimizing loading to maintain the signal and avoid adding noise²⁷.

It is common that the shaping amplifier needs to combine bandwidth, low-noise, large slew rate, and high stability²⁷. Multiple designs are applicable for this process, but a common one is the CR-RC shaping amplifier. The circuitry is a combination of a CR differentiator and

RC integrator, thus the CR-RC shaper²⁷. This amplifier configuration is able to normalize the pulses to a constant height, while creating a filter time constant, τ or RC , different than that of the detector. This allows the signal to decay at a faster or slower rate as chosen usually minimizing noise while capturing all of the signal charge²⁴. An example of the amplifier configuration can be found in Figure 2.6.

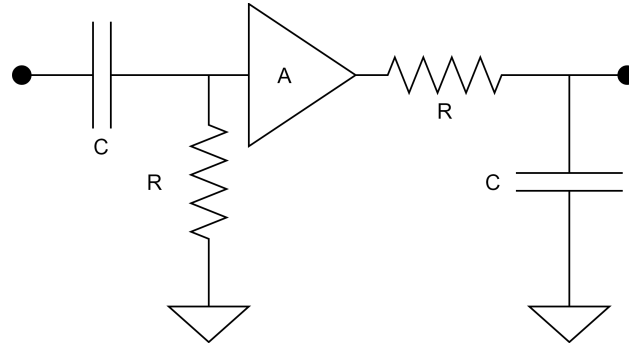


Figure 2.6: The CR-RC shaping amplifier used to induce gain and optimize the pulse timing, while not inducing additional noise on the system.

The τ value defines where the pulse reaches its peak before beginning to follow an exponential decay function, similar to Equation 2.1. An example of this concept for a $2\text{ }\mu\text{s}$ shaping time can be found in Figure 2.7.

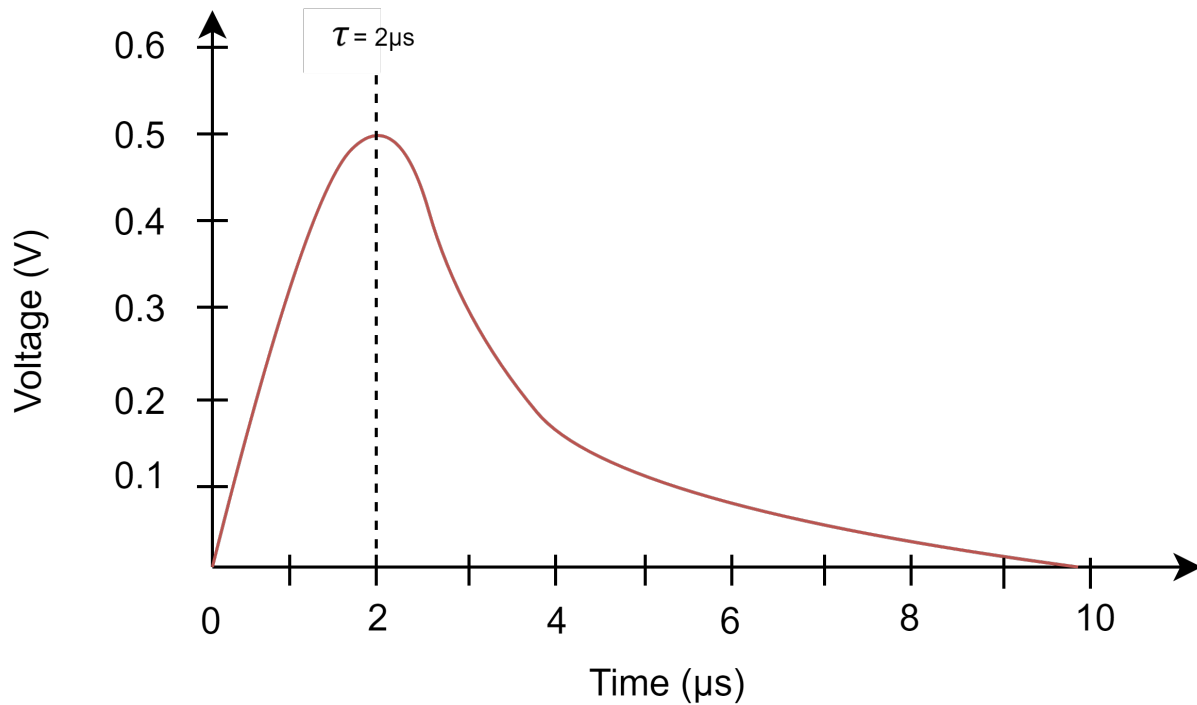


Figure 2.7: The signal that is produced by the CR-RC shaping amplifier, where τ is the time to maximum value before the signal begins to follow exponential decay.

For low count rate devices, a value for τ of $2\mu\text{s}$ would obtain optimal resolution, while the higher count rates might give optimal resolution at a τ of $0.5\mu\text{s}$ ²⁴. However, it is noted that this time constant may be best determined experimentally²⁴. Optimizing this time constant value will result in a reduction of pile-up at faster count rates as detected by the system. This keeps the data acquisition module, such as the MCA from missing counts. Missing counts would occur if the pulses arrive faster than the system can process, thus the system lumps the events together as one.

Chapter 3

Cockcroft-Walton Voltage Multiplier Topologies

3.1 Overview of the Cockcroft-Walton Multiplier

The Cockcroft-Walton voltage multiplier is a direct current (DC) voltage conversion technique used in the fields of research and industry²⁸. This type of voltage multiplier has wide applications in scientific instruments, television sets, oscilloscopes, x-ray systems, and photomultiplier tubes²⁸. The Cockcroft-Walton voltage multiplier can be configured in two configurations: the full-wave and the half-wave.

The basic operation of the voltage multiplier circuit is explained through the use of a Villard doubler, the stepping stone for the Cockcroft-Walton. The Villard doubler capacitor or diode network circuit transforms a cyclical wave input at a predefined frequency through a series of rectifier circuitry resulting in a constant DC output upon the final stage. As seen in Figure 3.1. In this example, the components are assumed to be ideal and the diode drop is ignored. The input wave, V_m , represents the full input voltage waveform, for instance, a square wave with $2V_{pp}$. During the negative half-cycle of the input voltage wave, the

capacitor C_1 charges through rectifier D_1 to the voltage V_m ²⁹. In this example, the voltage across C_1 would be 1 V. On the positive half cycle of the wave, the input voltage of C_1 charges capacitor C_2 through the rectifier circuitry D_2 providing the desired output voltage of $2V_m$ ²⁹. This results with point 1 on Figure 3.1 to be 0 V, point 2 to be a $2V_{pp}$ square wave, the voltage, V_{BA} across capacitor C_1 to be 1 V, and output point B on Figure 3.1 to be $2V_{pp}$ square wave with a 1 V DC offset. The rectifier circuitry on Figure 3.1 composed of D_2 and C_2 transition the switching waveform of $2V_{pp}$ to a steady DC of 2 V at V_{out} .

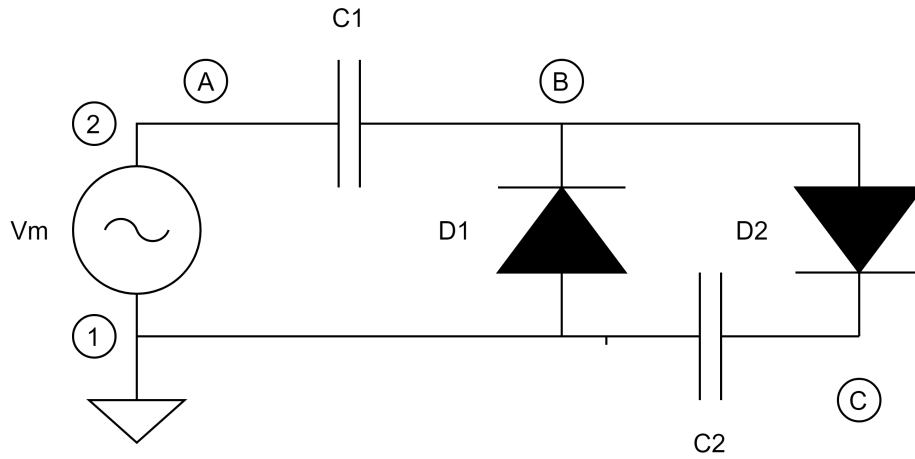


Figure 3.1: Basic voltage doubler operating circuit through a Villard voltage doubler.

At a signal level, assuming a similar example to that described for Figure 3.1, the signals would look similar to Figure 3.2 where nodes A, B, and C shown in Figure 3.1 are depicted in Figure 3.2. Node A refers to the $2V_{pp}$ square wave with a 0 V DC offset, node B refers to the shifted square wave of $2V_{pp}$ with a 1 V DC offset, and node C refers to the DC output voltage through the rectifier circuitry of 2 V.

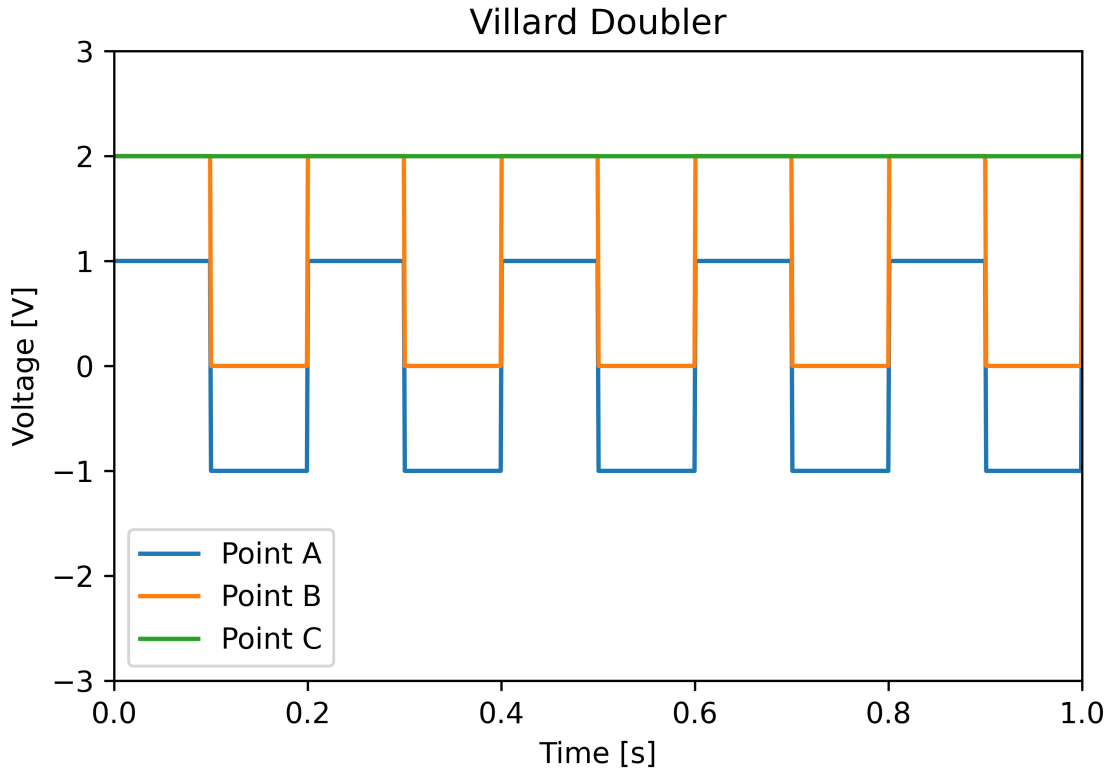


Figure 3.2: Voltage doubler signal level analysis for example described using Figure 3.1

Rearranging the Villard doubler and adding a repeating stage results in a configuration known as the half-wave Cockcroft-Walton multiplier, as seen in Figure 3.3. Similar to the operation of the Villard doubler, the switching signal is brought into the circuit and DC shifted as before, but instead another stage has been added to the circuit, thus resulting in an additional linear increase of the DC voltage with the addition of each stage.

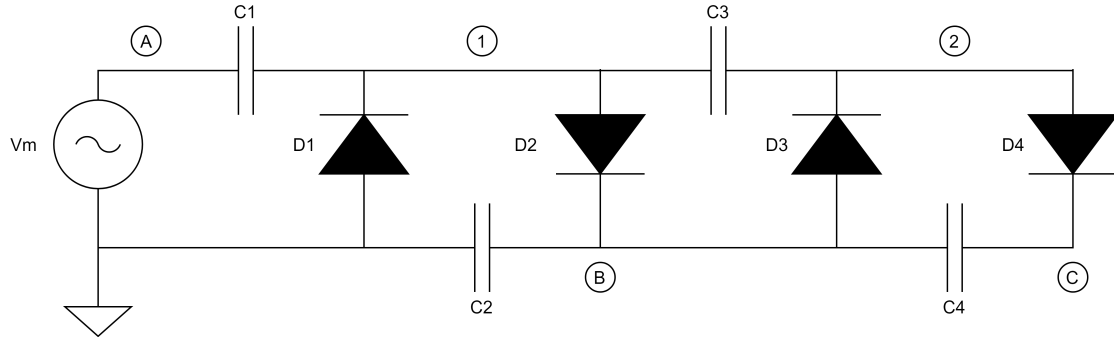


Figure 3.3: Basic Cockcroft-Walton voltage multiplier configuration to increase voltage each stage by multiplying an additional amount equal to the peak-to-peak voltage of the input waveform.

As the reference node for each adjoining stage begins to climb, the voltage on the output begins to shift the input waveform by an offset, as shown in Figure 3.4. For instance, as node B is now referenced to $2V$, the next stages AC switching square wave is now offset by $2V$, thus resulting in the square wave at node 2 switching at $2V_{pp}$ but shifted up by $2V$. This results in a DC voltage output value of $4V$ at node C.

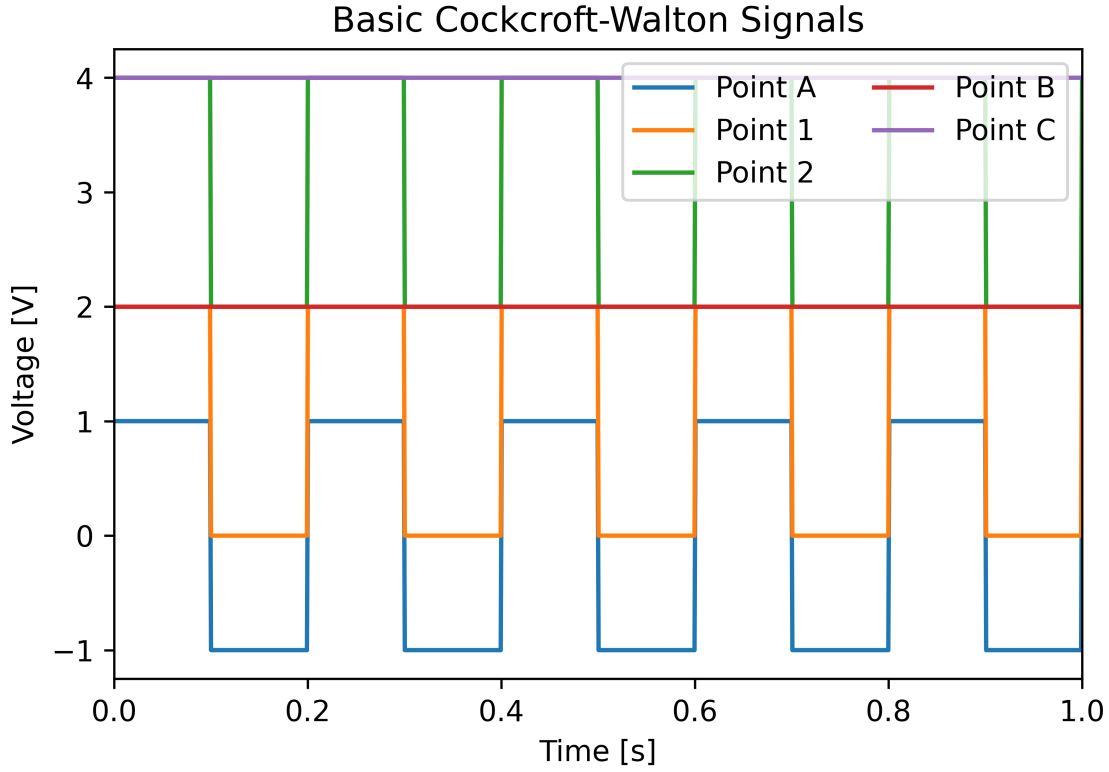


Figure 3.4: Basic Cockcroft-Walton voltage multiplier configuration to increase voltage level each stage by a multiple of the input peak-to-peak voltage level cascading the stages offsets the reference voltage for the input waveform.

Chaining together a series of these rectifier circuits can linearly increase the voltage every stage, thus resulting in a voltage increase to a desired output. In order to integrate the Cockcroft-Walton circuit into the PMT base, the Cockcroft-Walton can be tapped off the ladder at each stage as necessary. This flexibility in the design allows for varying dynode stage connections for the detector.

The half-wave Cockcroft-Walton configuration is the simplest configuration of the Cockcroft-Walton voltage multiplier. It is the most common circuit of its kind between the two possible configurations³⁰. This configuration provides a low cost as it is composed of rectifiers and capacitors³⁰. The half-wave Cockcroft-Walton configuration also has uniform stress on all diodes and capacitors³⁰. This is important because the load being distributed avoids stress on just one component, avoiding design with higher rated components than needed.

The half-wave configuration, as seen in Figure 3.5, produces a negative polarity DC output, similar to that used in the design for the Hamamatsu PMT. Unlike the example Cockcroft-Walton circuitry in Figure 3.3, the diode direction is rotated 180° in order to produce the negative voltage at the output nodes. This is what is required for the Hamamatsu PMT application.

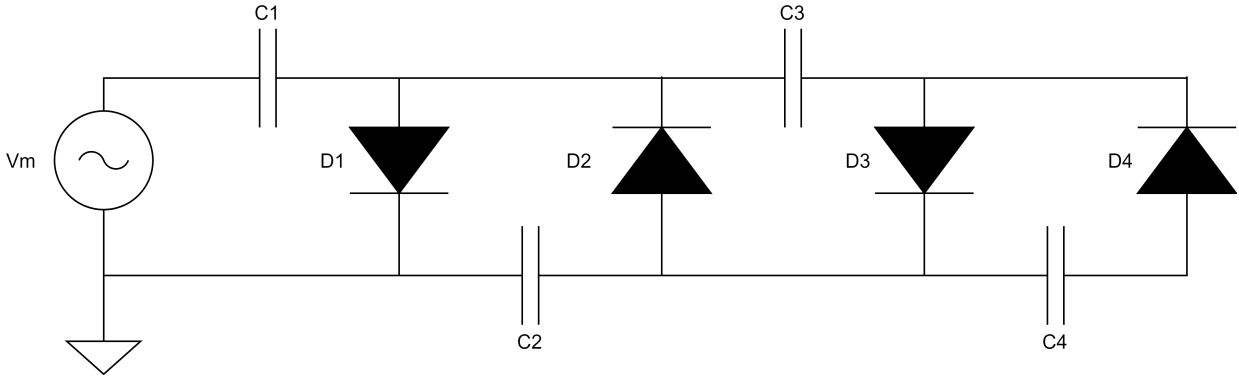


Figure 3.5: Basic configuration of a half-wave Cockcroft-Walton with a negative output.

The full-wave Cockcroft-Walton configuration is the more complex configuration³⁰. A full-wave Cockcroft-Walton configuration uses a mirrored design of rectifier circuitry to create the high voltage as seen in Figure 3.6. The circuit in essence works in a similar fashion to the half-wave. However, it is capable of using both the positive and negative segments of the AC wave to induce charging to the capacitors to double the voltage at a faster rate.

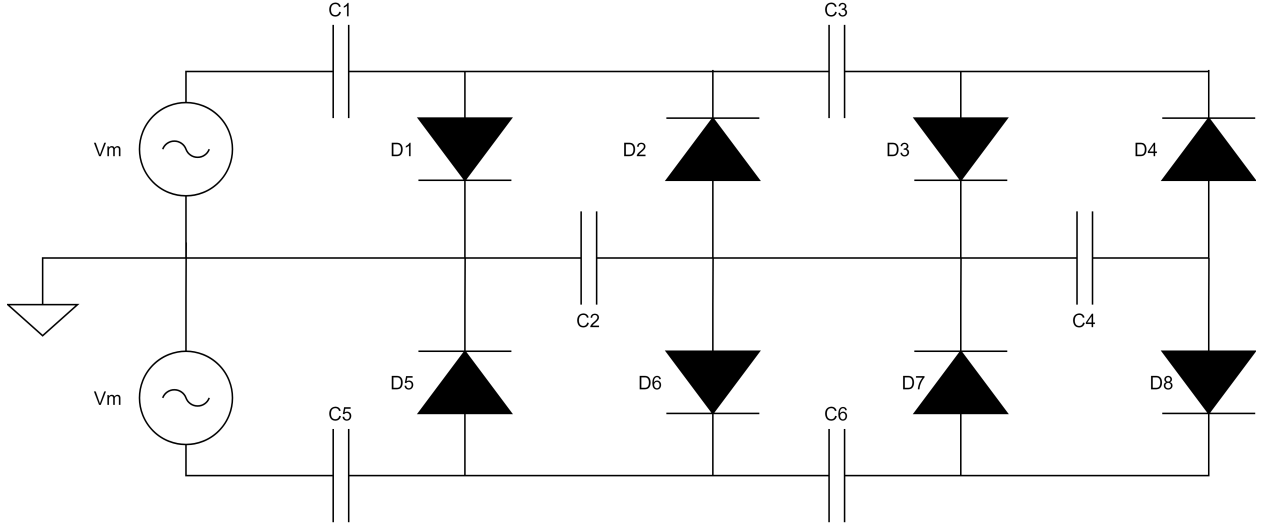


Figure 3.6: Basic configuration of a full-wave Cockcroft-Walton with a negative output. The circuit used an entire input waveform to charge to the desired voltage at a faster rate.

LTSpice simulation software was used to simulate both Cockcroft-Walton configurations for the half-wave and full-wave. Full simulation setup can be found in Appendix A. As indicated by Table 2.3, a 16-stage Cockcroft-Walton design is necessary to be able to apply adequate voltage ratios between each dynode of the PMT. The half-wave and full-wave Cockcroft-Walton voltage multiplier was generated with a 150 kHz $62.5 V_{pp}$ square wave, the ladder input pulse necessary to get to a 1000 V potential in 16-stages. Comparing the two LTSpice simulation results for the ladders, the main difference between the two configurations is in relation to the time it takes for the circuit to charge to a steady-state, and with the total number of components in each Cockcroft-Walton ladder. A comparison of the two configuration as a function of the voltage response can be found in Figure 3.7³.

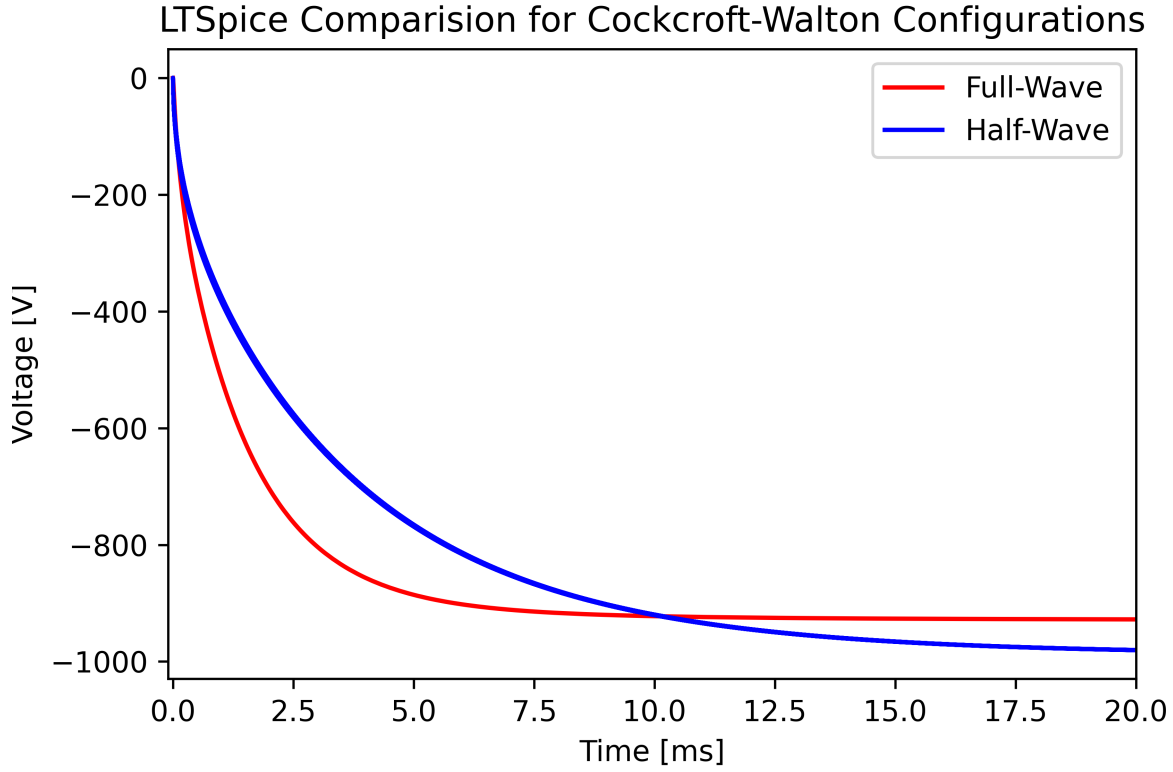


Figure 3.7: Comparison of LTSpice simulation results for a 16-stage half-wave Cockcroft-Walton ladder half-wave and full-wave configuration with input switching frequency of 150 kHz, $62.5 V_{pp}$.

The half-wave was expected to charge to steady-state in 15 ms with a potential of $-980.5 V$ while the full-wave configuration can charge to steady-state in 4.75 ms at a potential of $-927.8 V$. The full $-1000 V$ potential was not achieved as the software implements some loss through the diodes. Since the full-wave configuration is using both the positive and negative half of the switching input, rather than half, the full-wave is able to achieve the higher voltage potential in minimal time. The only positive to using the full-wave would be to speed up the overall charging time of the circuit by only a few milliseconds as seen in Figure 3.7. Although, speed is typically a design constraint for circuitry, the low volumetric footprint was more of a concern, as high-voltage is still achievable in both circuit configurations. Overall, the amount of time to a steady-state high-voltage does not impact the functionality of the PMT. Any reduction in components would reduce complication during the additive manufacturing process. This is of primary importance because embedding the components in 3D printed

design is still such a new technology. With the goal of additive manufacturing and having a low volumetric footprint, a half-wave configuration was chosen as the optimal Cockcroft-Walton voltage multiplier configuration because of its versatility, uniform load distribution exhibited upon the stages, low cost and size compared to its counterpart³⁰. Using the half-wave configuration over the full-wave configuration meant a 34% reduction in total ladder components opposed to the full-wave.

The dynode voltages necessary for the PMT operation can be tapped from the half-wave 16-stage circuit. Results of the LTSpice simulation show how each dynode stage charges³. Results for each dynode are shown in Figure 3.8. The results reflect the linearity between individual stages except to those that are tapered.

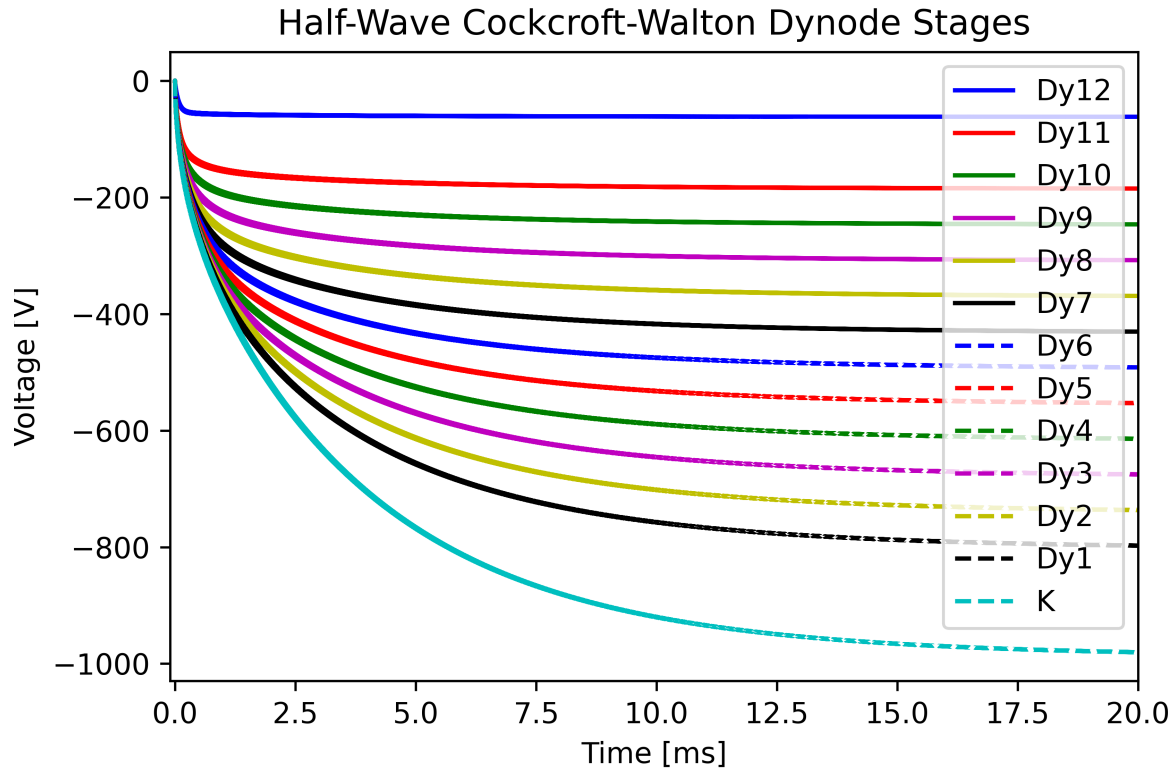


Figure 3.8: LTSpice results for a 16-stage half-wave Cockcroft-Walton ladder dynode voltages. These stages are tapped off to allow PMT socket connection.

3.2 Cockcroft-Walton Calculations

Additionally, filtering was added on the output of the Cockcroft-Walton stages before tapping off the ladder to the PMT dynode stages. This is designed to help smooth out the voltage rippling as the capacitors in the circuit charge and discharge under loaded conditions. For instance, using the LTSpice simulation for the half-wave configuration as above, and zooming in on the final stage while the circuit is in the process of charging, the ripple can be seen in Figure 3.9³.

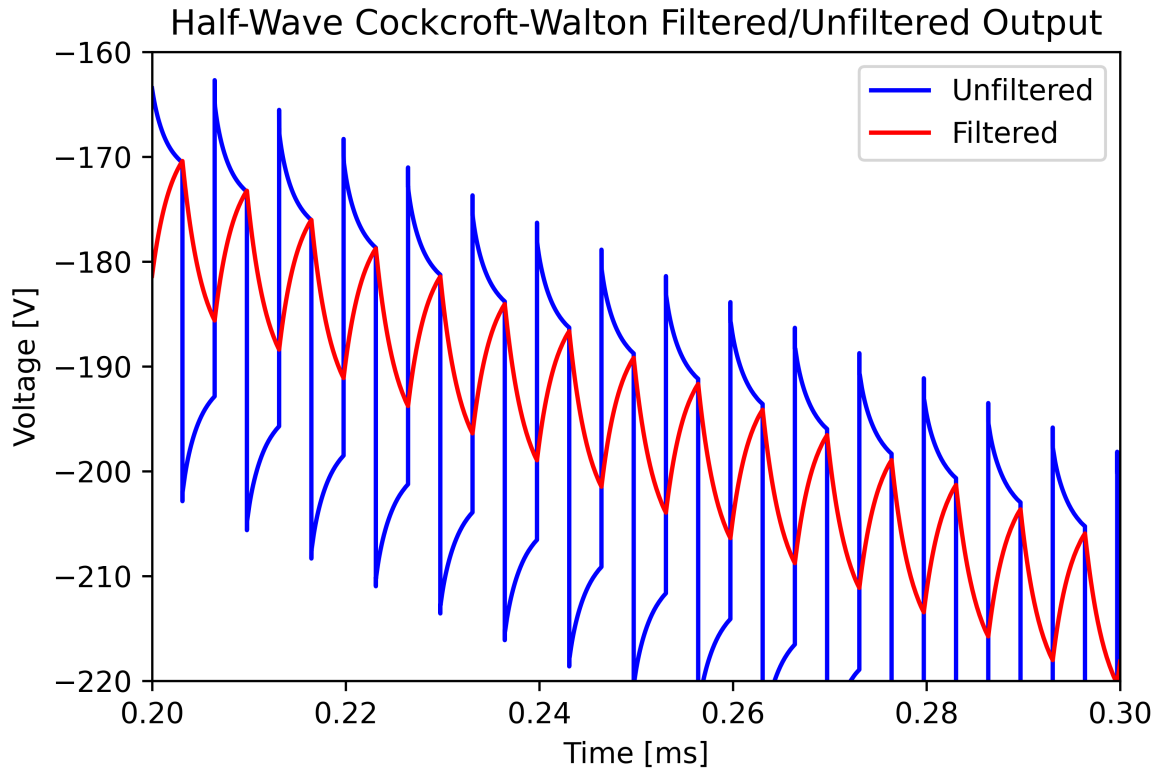


Figure 3.9: LTSpice simulation results for a 16-stage with and without RC filters on dynode connections.

A consequence of having voltage ripple on any of the dynode stages of the PMT is that the energy resolution of the system degrades. Since the photomultiplier tube has 12 internal stages, the output varies directly with the 10^{th} power of change in applied voltage³¹. As energy resolution of a few percent is desired, thus ripple noise and voltage stability must be small in comparison. As a result, it is important to understand that for a stable output, minimal ripple must be present.

To calculate the peak-to-peak voltage ripple for each stage of the Cockcroft-Walton ladder with equal capacitors Equation 3.1 can be used⁹.

$$V_{\text{ripple}} = \frac{I}{fC} \left(\frac{n(n+1)}{2} \right) \quad (3.1)$$

where I is the load current, f is the frequency of the input voltage, C is the capacitance, and n is the number of stages.

For this particular design, low-pass RC filters were used on the output of each stage. These were used in order to reduce the ripple and assist in fighting degradation in the output signal level as this ripple can interfere with the signal quality of the PMT. An example of the filter can be found in Figure 3.10.

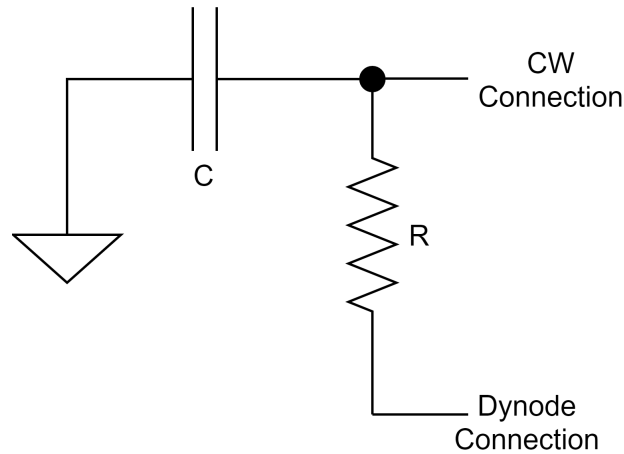


Figure 3.10: An example of the filtering network that is tapped off of the Cockcroft-Walton ladder. The filter may be chained together to filter along the stages.

These filters can be chained together across the Cockcroft-Walton ladder. Instead of a ground connection for the capacitor, the filter just hooks onto the next stage as seen in Figure 3.11. An advantage of filtering in this fashion allows for filtering along the ladder dynode connection points, rather than all at once off of the final stage typically found in PMT high-voltage supply base diagrams³².

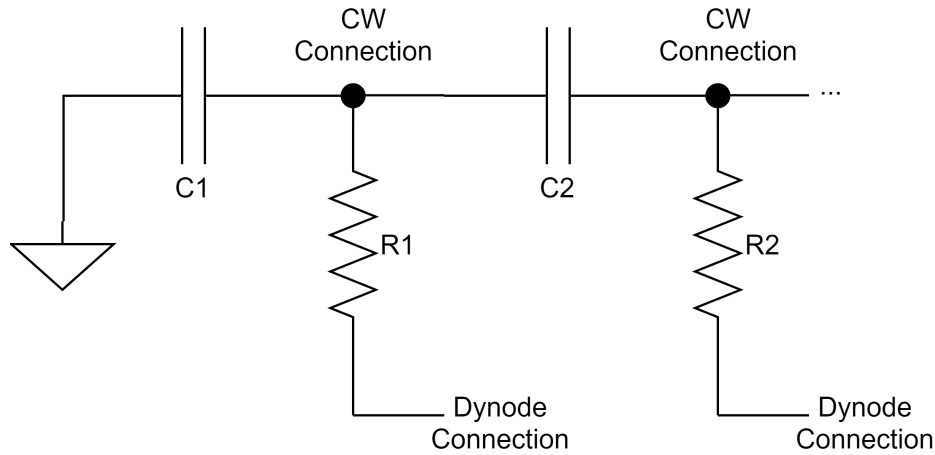


Figure 3.11: An example of the filtering network chain that is tapped off of the Cockcroft-Walton ladder to filter.

To figure out what values to use for the filtering circuitry, one must know the capacitance of the filtering network as it increases along each stage in order to figure out what resistance value to use. Assuming equal capacitance will be used in the filtering Equation 3.2 can be used.

$$C_{\text{stage}} = \frac{C}{n} \quad (3.2)$$

where C is the filtering capacitance value, which was selected to match, and n is the current stage. This equation is derived from how capacitors add in series.

To actually filter at each dynode connection, a frequency f is first selected. Then filtering cutoff frequency equation, found in Equation 3.3 was used with the C_{stage} to solve for the resistance R . For this design, E96 1% resistors were used in the filtering network.

$$f = \frac{1}{2\pi RC} \quad (3.3)$$

Optimizing the filtering frequency will ideally provide as much signal out of the PMT and scintillator as possible to avoid signal degradation. The current amplification gain, μ can be calculated via Equation 3.4³².

$$\mu = AV^{kn} \quad (3.4)$$

where A is a constant, assumed to be 1, V is the ratio of supply voltage and voltage increase per stage, k is a constant determined by the dynode structure/material, ideally between 0.7 and 0.8, and n is the total number of dynode stages³².

Chapter 4

Design Iterations

The approach to the finalized system was to follow the design process through a series of iterations. The iterations were completed when the design was able to meet all of the design requirements and retain functionality.

4.1 Design Considerations

In addition to meeting the goals of the project, there are other constraints to consider for a PCB for high-voltage applications. Component selection had to follow the voltage/current ratings required throughout the system. This alleviated immediate component failure upon startup. Secondly, component size had to be minimized while maintaining spacing to prevent arcing at high-voltage potentials.

The voltage potential and spacing between each stage is a concern due to arcing throughout the design. Using Saturn PCB Design Toolkit, it was identified with an electrical potential of 62.5 V between stages, assumed from the maximum voltage across 16-stages being 1000 V, the conductor spacing in air between the minimum altitude of sea level to maximum altitude of 3050 m would need to be at least 600 μm ³³. All component packages mentioned throughout the design were chosen with this spacing in mind. Unless otherwise specified, all of the

passive components were selected to be 0402 standard size (pads spaced 0.25 mm apart) with a safety margin of at least 1.5 with regard to the breakdown voltage³⁴.

To provide additional high-voltage protection, Dow Corning Sylgard 182 silicone elastomer was used to coat the circuit³⁵. Sylgard 182 has a dielectric breakdown of 22 kV/mm, making it an ideal to prevent arcing at a potential of 1 kV³⁵. Additionally, the silicone coating is removable to allow rework to the circuit.

4.2 Initial Design

The initial design was an adaptation from a previously constructed high-voltage circuit with positive bias. The two-board stack, on top of the CsI(Na) 1 inch x 1 inch x 3 inch crystal can be seen in Figure 4.1. All designs were created using Altium Designer, a circuit design suite software². This design suite was selected with it being an industry standard, as well as the ability to produce a three-dimensional representation of the PCB. A complete schematic set and bill of materials (BOM) can be found in Appendix A.

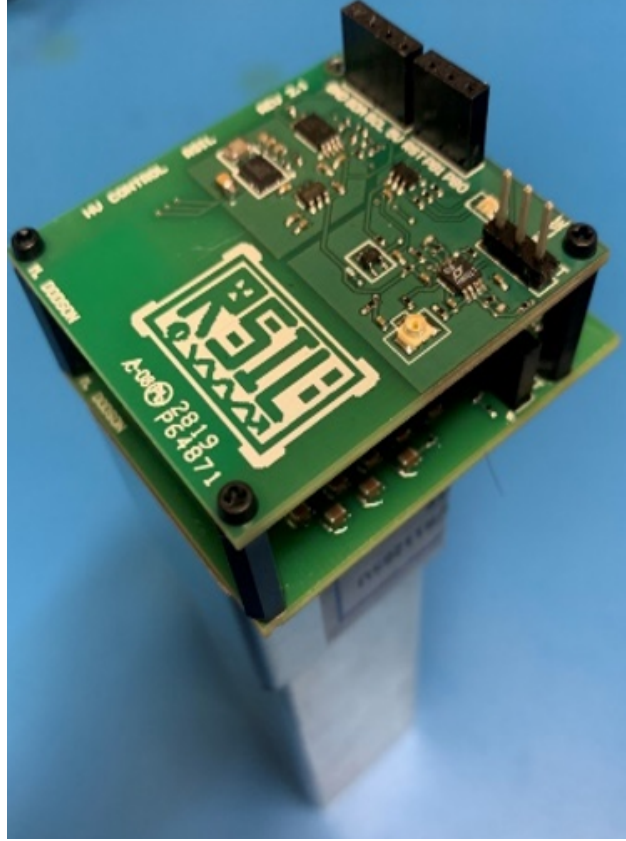
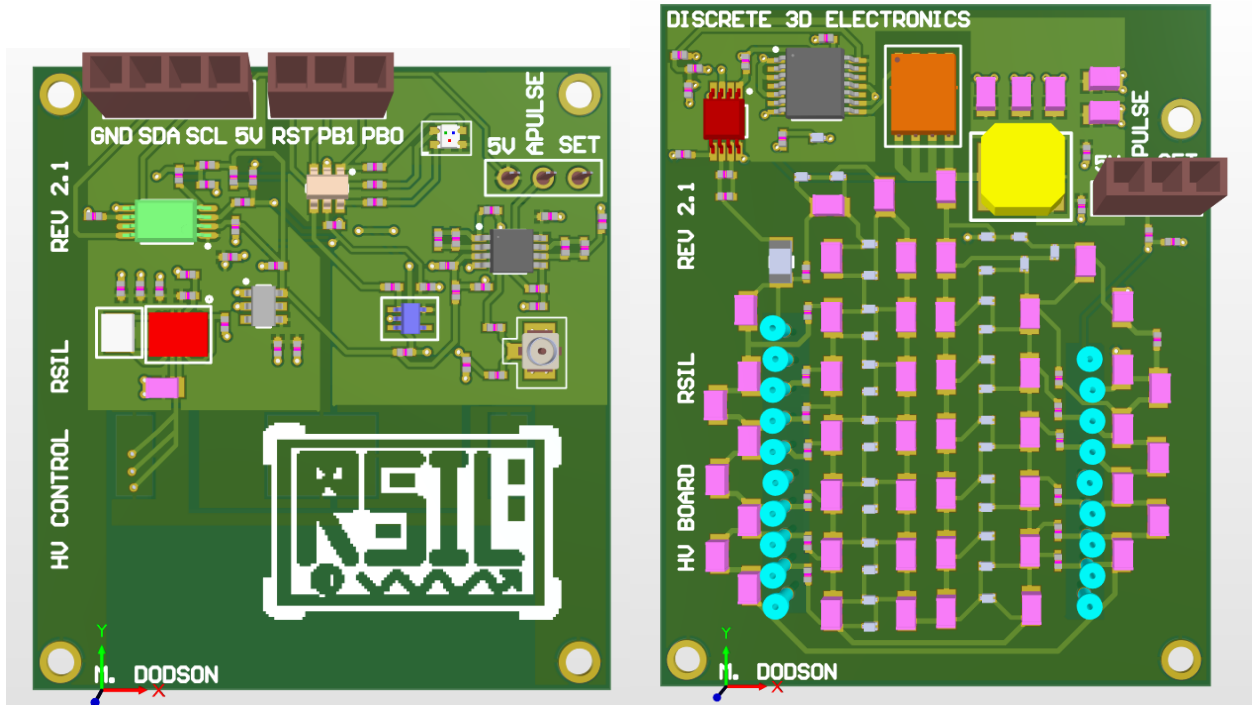


Figure 4.1: The two-board PCB stack on top of the CsI(Na) 1 inch by 1 inch by 3 inch PMT base.

4.2.1 Design Overview

The initial circuit was a two-board PCB stack with a high-voltage and a control board. The high-voltage board contained the Cockcroft-Walton ladder. The control board contained power regulation for the entire circuit, and pulse processing to shape the PMT pulses. This particular design incorporated both a visual count rate indicator with a light-emitting-diode (LED), and a preamplifier and shaping circuit for output to an MCA. Both circuit boards, as presented in Altium designer, are shown in Figure 4.2, where Figure 4.2a is the control PCB board, and Figure 4.2b is the high-voltage Cockcroft-Walton board. Overall, the design had a complete component count of 192 components: 54 components for the high-voltage control board and 138 of the components for the high-voltage board.



(a) High-voltage control PCB

(b) High-voltage Cockcroft-Walton PCB

Figure 4.2: The two-board stack design as presented in Altium Designer circuit design software². The high-voltage control board housed all of the control for the high-voltage Cockcroft-Walton board, used to generate high-voltage for the PMT. The high-voltage control board also housed an LED for count rate indication and pulse processing to send the PMT pulses to an external MCA.

The control board, pictured in Figure 4.3 contained six key component groups: the 2.5 V voltage reference, the power regulation, the high-voltage set point circuitry, the pulse processing circuitry, and finally the LED and microcontroller to visually indicate increased count rate.

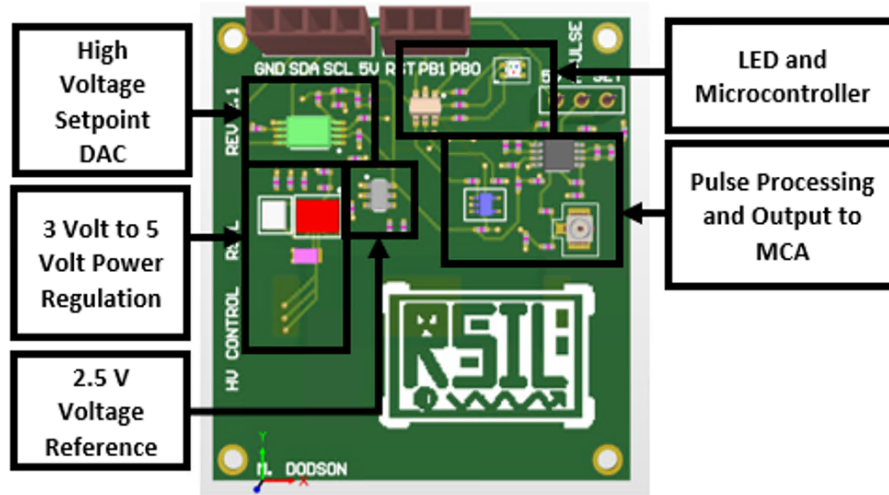


Figure 4.3: Breakdown of the component groups for the high-voltage control PCB.

The high-voltage PCB, presented in Figure 4.4, encompasses five main component groups. These groups are the Cockcroft-Walton voltage multiplier, the amplifier used in the feedback circuitry used to drive the charge pump, the inverting schmitt trigger used to create a square wave for the charge pump, the MOSFET and inductor combination used to drive the Cockcroft-Walton ladder, and then a generic 3-pin header used as the peripheral connection between the high-voltage and the control board.

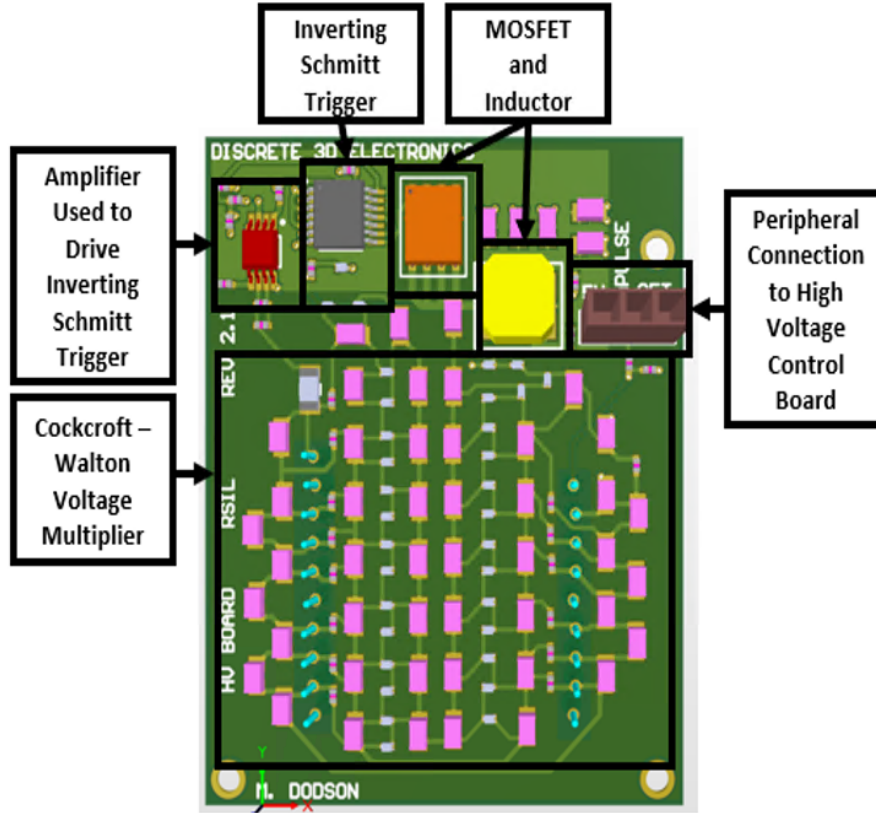


Figure 4.4: Breakdown of the component groups for the high-voltage Cockcroft-Walton PCB.

The two-board stack is shown as a block diagram in Figure 4.5. In the block diagram the blue outline represents the high-voltage control board while the orange outline represents the high-voltage board. The high-voltage control board contained the power regulation circuitry. The control board also used the high-voltage feedback and the set point to control the charge pump on the high-voltage board. The charge pump was composed of two parts, the schmitt trigger oscillator and the MOSFET. The signal produced by these two components was then fed into the Cockcroft-Walton ladder. The signal from the output of the PMT generated via the Cockcroft-Walton ladder was sent out as an 'Analog Pulse' which was shaped using a preamplifier and shaping amplifier such that the pulse is adequate for pulse-height spectroscopy and collected by the MCA for data acquisition. The shaped pulse is also sent to the circuitry used for count rate indication.

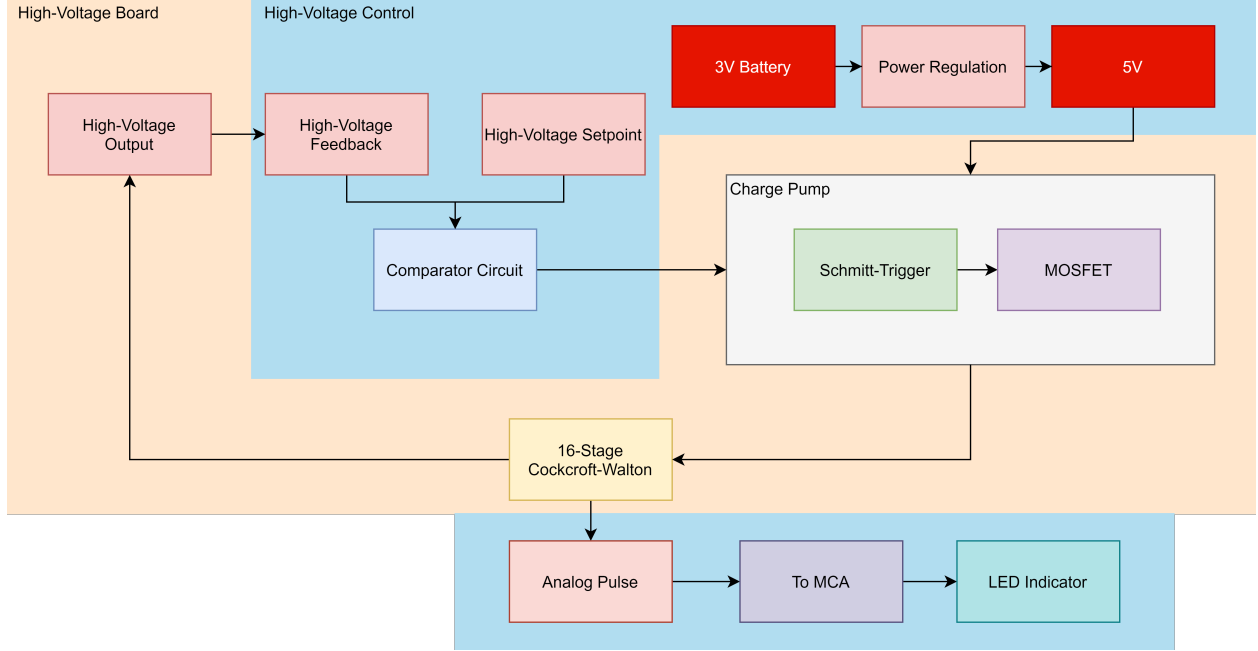


Figure 4.5: Full Cockcroft-Walton two-board stack block diagram.

4.2.2 Cockcroft-Walton Voltage Multiplier Design

As previously discussed the Cockcroft-Walton multiplier was chosen to be 16-stages, and negatively biased. The negative bias was selected based on manufacturer recommendation¹. This meant that the anode is at the ground potential enabling faster pulses since an output capacitor is not needed on the pulse to block DC components. Furthermore, negative bias was selected so that the highest current draw, typically seen in dynode 12, would be closest to the supply.

In the design, maintaining the required spacing to eliminate the possibility of the ladder arcing is important. In order to adequately accommodate this, 0805 standard capacitors (pads spaced 0.65 mm apart) were selected³⁴. At a 1000 V potential, each stage would be charged to a maximum value of 62.5 V. A rule-of-thumb when selecting components was to maintain safety margin necessary for operation. Therefore, at 62.5 V between each stage, 100 V was chosen to ensure the components will not naturally breakdown due to voltage.

To investigate the effect of capacitor values and assist in selection of the ladder capacitors,

LTSpice simulation software was used to vary the capacitor sizes in the half-wave Cockcroft-Walton³. This was completed by varying the simulation parameters to encompass $0.1\ \mu\text{F}$, $0.22\ \mu\text{F}$, and $1\ \mu\text{F}$ capacitors with the half-wave configuration. The results presented exhibit various charging times to the final steady-state voltage. The $1\ \mu\text{F}$ charges to a less potential than any of the counterparts. However, the steady-state is achievable with all capacitor values. The results presented in Figure 4.6, represent the charging of the Cockcroft-Walton ladder with these changes.

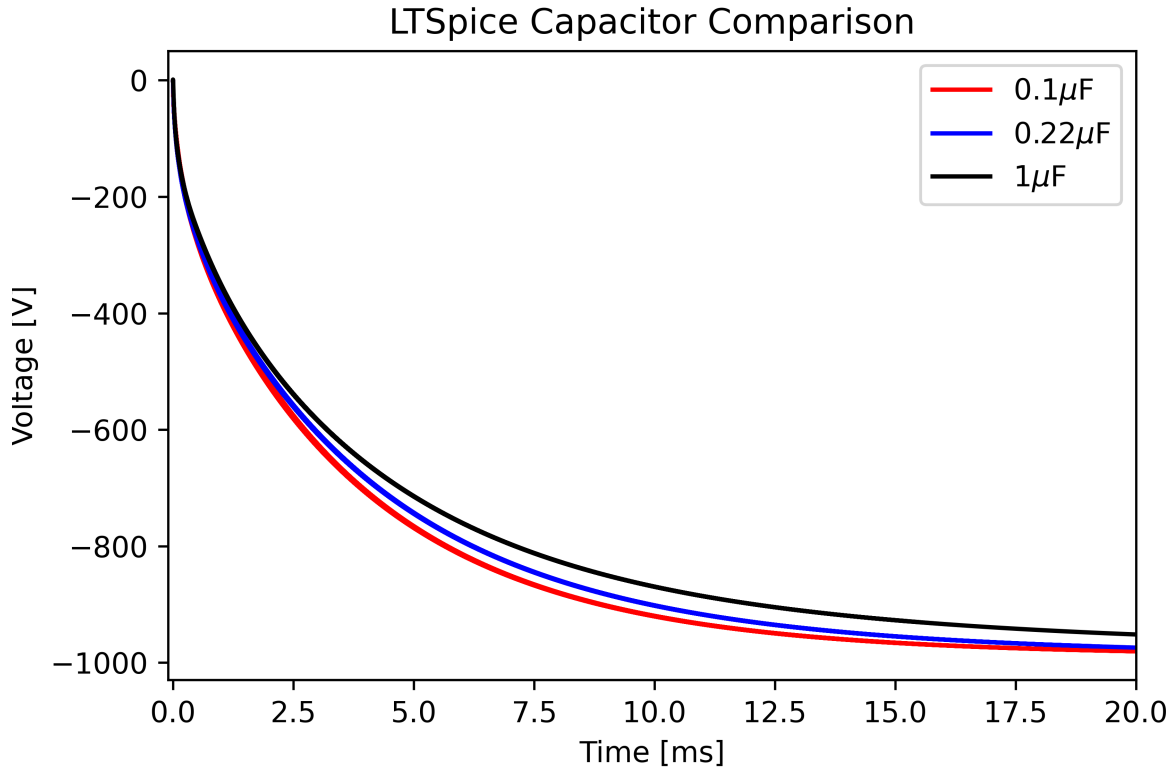


Figure 4.6: Comparison of various capacitor sizes and the half-wave Cockcroft-Walton ladder using LTSpice simulation software.

Design necessity for 0805 package size with 100 V breakdown, $1\ \mu\text{F}$ capacitors were chosen for the ladder capacitors. This was because $1\ \mu\text{F}$ was the largest ceramic capacitor value in that package. Additionally, the increased capacitance value will ensure that the stability remains under increased loading conditions.

For diode selection, a small package was the goal while being able to maintain the 62.5 V potential at 1 kV. Similar to the choice of the capacitors, the diode, NSD914F3T5G, were chosen as it specifies a maximum reverse voltage breakdown of 100 V³⁶. Furthermore, the diodes chosen for the device must be selected such that the switching speeds are able to handle the rise and fall time of the input²⁹. The NSD914F3T5G diodes were marketed for high speed switching applications and places where board space is a premium³⁶. The diode package size is SOT-1123, 3-pin diode with volumetric dimensions of 0.85 mm width by 0.65 mm length by 0.4 mm height³⁶. Despite the size, the NSD914F3T5G diode, allowed a maximum forward current of 200 mA to operate, and a peak current before breakdown in a single instant of 500 mA³⁶. The operating range of the PMT specifies a maximum current load of 1 mA, which is within the operating ranges of the diode¹. Ensuring that the maximum current for the diode are overspecked allow for the circuit to width stand the loading effects due to the capacitive load during turn-on²⁹.

The Cockcroft-Walton design in Altium Designer is shown in Figure 4.7. Note, the diodes contained a third pin that is left floating as it is not connected to the diode and is a mechanical attachment point. The dynode tap locations occur at the points defined in Table 2.3.

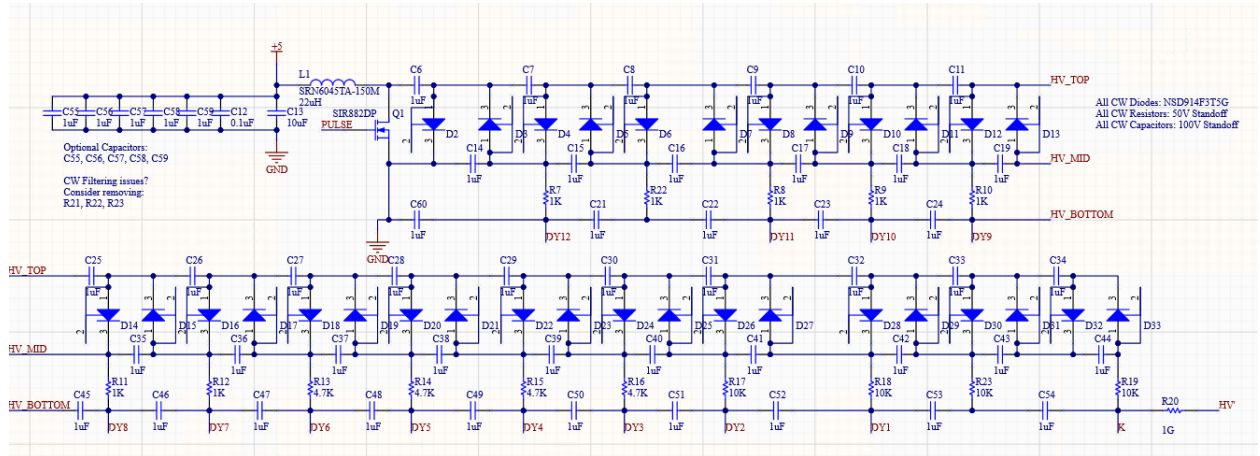


Figure 4.7: The schematic for the Cockcroft-Walton ladder two-board design.

Filtering at each dynode connection was added to reduce voltage ripple as much as possible. Resistor values were selected to increase as the capacitance to ground decreased along

progression of the ladder, reflected by Equation 3.2. This resulted in an increased cutoff frequency moving across the ladder. As a result of the decreasing capacitance the cutoff frequency of the filtering network must be increased by increasing the resistance. For this design, the filtering values were picked to increase further down the ladder and keep the variation in total components of the bill of materials low. The filtering cutoff frequencies range between 160 Hz and 1120 Hz, when calculated using Equation 3.3.

4.2.3 Front-End Charge Pump Design

The charge pump design is used to generate the switching input to the Cockcroft-Walton ladder. The charge pump enables the square wave input to ensure it does not overcharge based on a set point. The analog based control circuit can be found in Figure 4.8.

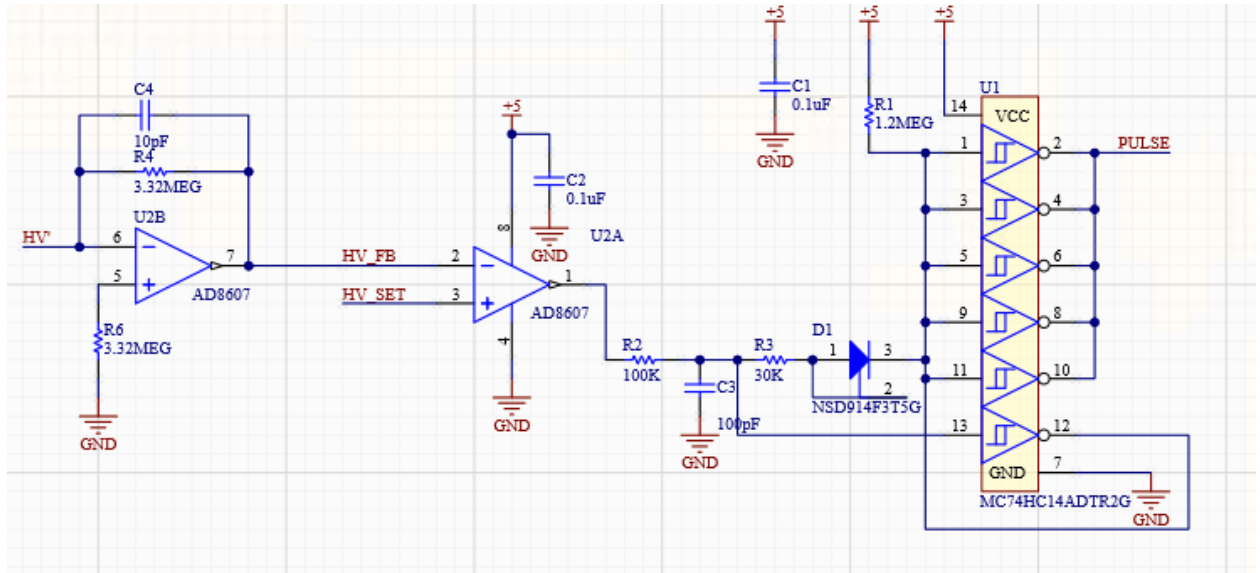


Figure 4.8: The high-voltage feedback and comparator circuitry used to control the charge pump that is used to energize the Cockcroft-Walton ladder. It does so by creating an oscillator with the schmitt trigger.

In Figure 4.8, the high-voltage taken from final stage of the Cockcroft-Walton ladder is inverted through a inverting amplifier, AD8607. The Analog Devices AD8607 was selected as a dual package operational amplifier³⁷. The operational amplifier package is 5 mm length by 4 mm with by 1.75 mm height³⁷. This resulted in the design being simplified to satisfy

the feedback network to control the charge of the circuit. Additionally, the AD8607 was selected due to its low noise, low signal distortion, stability at unity gain, an low power, only needing 50 μA of supply current per amplifier³⁷.

The resistor divider network created through the first operational amplifier (U2B) in Figure 4.8 generated a voltage such that it is inverted and stayed between 0 V to 5 V of the input voltage threshold. The design inverts and steps down the voltage using a 1 G Ω on the output of the high voltage (R20) and the 3.32 M Ω (R4) feedback resistor. This created a gain of -3.32 mV/V . Therefore, at -1000 V , the output would be 3.32 V. That voltage was fed into the other amplifier of the package. This acts as a comparator circuit to compare the value to the HV_SET voltage, generated via the threshold set point section of the high-voltage control board, Figure 4.14. The additional capacitor C4 of 10 pF was used to ensure the feedback network kept the operational amplifier stable. The HV_SET voltage was generated by a voltage divider circuit that utilized the 2.5 V reference and was created on the high-voltage control board. If the value from the first amplifier HV_FB was less than the HV_SET, then the comparator (U2A) would trigger the schmitt trigger to fire.

To activate the schmitt trigger oscillator, a low-pass filter (R2, C3) of 15 kHz was incorporated to reduce noise on consecutive pulses, and a diode (D1), the same that was placed in the ladder was used to ensure the signal goes one way.

The schmitt trigger (U1) in Figure 4.8 was created by ON Semiconductor, the MC74HC14A³⁸. The component was selected as it was compatible to drive CMOS devices, such as MOSFETs. The schmitt trigger oscillator had multiple output pins that were connected to drive the ladder using the summed current. The component was selected due to its low input current of 1 μA needed to activate the channels. One channel output was used as a feedback on the schmitt trigger to allow continuous output pulsing without interruption, such as on the startup of the Cockcroft-Walton ladder. This created an oscillator to charge up the ladder. The schmitt trigger component also operated at 150 kHz, 50% duty cycle 5 V_{pp} square wave³⁸. The frequency and duty cycle were internally set by the

component. The amplitude was set based on the operation voltage for the component. In terms of overall package size, this device was one of the largest in the design 8.75 mm length by 6.20 mm width with 1.75 mm height³⁸.

An N-Channel MOSFET and inductor combination depicted in Figure 4.9 was utilized to charge the actual circuit. The inductor was used to store up and release a charge into the ladder. This allowed constant current support to the PMT load upon increased count rate. The MOSFET was used as a switch to release the charge into the Cockcroft-Walton ladder at the command of the switching.

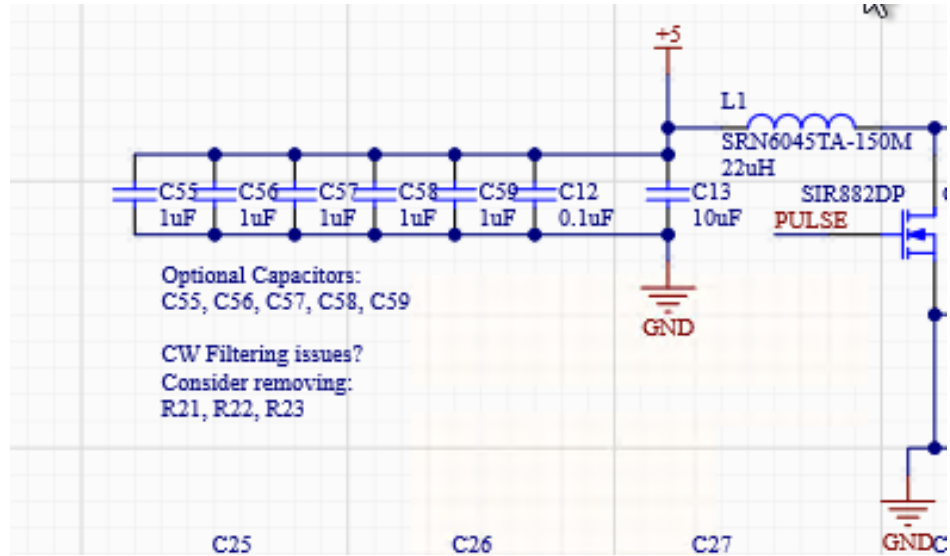


Figure 4.9: The MOSFET and inductor combination responsible for dumping large amounts of charge into the Cockcroft-Walton ladder.

When the inductor was selected, it needed to handle the current surge before steady-state was achieved in the ladder. Previous experience revealed that the current through the inductor upon startup would range from 1 A to 1.5 A. To avoid failure in the inductor and allow safety margin, a peak current rating of 1.8 A was selected. To minimize the circuitry for additive manufacturing, a shielded inductor was chosen as this removed the need for additional shielding devices, which can add volume. Furthermore, an inductor with low DC resistance (DCR) was chosen to avoid a voltage drop at large current. Using these assumptions, an inductor was chosen with an inductance of 22 μ H.

A SIR882DP was chosen for the switching MOSFET. Choosing the MOSFET was similar to the diode and capacitor in respect to the the maximum voltage between the drain and source pins, of at least 100 V. Moreover, I_D , the current through the drain of the MOSFET, needed to be able to handle the instantaneous current of the system and while being activated with 5 V. Therefore, the threshold voltage, V_{th} , was low enough to trigger on 5 V as the minimum V_{th} necessary to activate the MOSFET was 1.2 V³⁹. The MOSFET package was a 6.15 mm by 5.15 mm by 1.04 mm size³⁹.

To charge the Cockcroft-Walton ladder, a 5 V_{pp} square wave at 150 kHz, 50% duty cycle, was sent into the gate of the MOSFET. When the voltage between the gate and the source pin of the MOSFET, or V_{gs} , became higher than the threshold voltage, V_{th} , the MOSFET turns on and conducts current freely from the drain pin to the source. When the MOSFET is not conducting current, the body diode of the MOSFET is used to complete the loop. When the MOSFET is switched on and off fast enough, it will be able to charge up the inductor and pump current into the ladder.

As a result when the schmitt trigger pulse is high, the inductor is charging and not releasing any charge. The second the schmitt trigger pulse is low, the inductor is able to release the charge as a large spike, followed by a ringing pulse, known as a chirp. The height of the inductor pulse varies as a function of the time the inductor is able to charge over the amount of current released through the system. The DCR of the inductor translated the current into a voltage.

An example of this operation can be found in Figure 4.10 as measured on the output node of the inductor. Due to the nature of the two-board stack design, the pulses were taken independently through the oscilloscope to ensure to not disturb the board while probing and cause an arc. This could have potentially arced through the thin areas of the Sylgard coating, resulting in circuit failure. The switching output found in Figure 4.10a, pulses at 150 kHz, 50% duty cycle. The inductor charge, shown in Figure 4.10b, outputs a maximum

of 48 V at the peak emission before decaying off to the chirp. The inductor charge depicted here was captured after the circuit was already fully charged. Therefore, the charge was only released to reestablish the voltage.

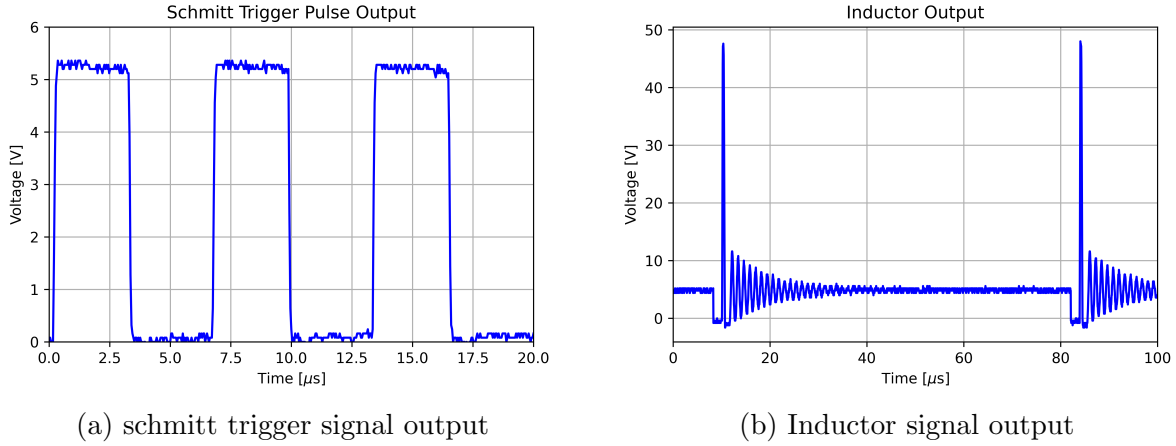


Figure 4.10: An example of the schmitt trigger oscillator output and the inductor output with ringing.

4.2.4 Pulse Processing Design

Pulse Shaping

The pulse processing design is composed of two key elements: the translated PMT pulse to the MCA, and a processing circuit used to provide visual feedback via an LED.

A block diagram for the circuitry breakdown can be found in Figure 4.11. The pulse generated from events detected by PMT are depicted as the "Analog Pulse". This segment was then brought into the preamplifier/shaping amplifier combination. The pulse was then sent out a connector to be hooked up to an external MCA for spectroscopy collection. The same signal is taken to a comparator circuit used as a threshold for a microcontroller, the ATTINY10, to figure out the pulse frequency and indicate the pulses on the LED.

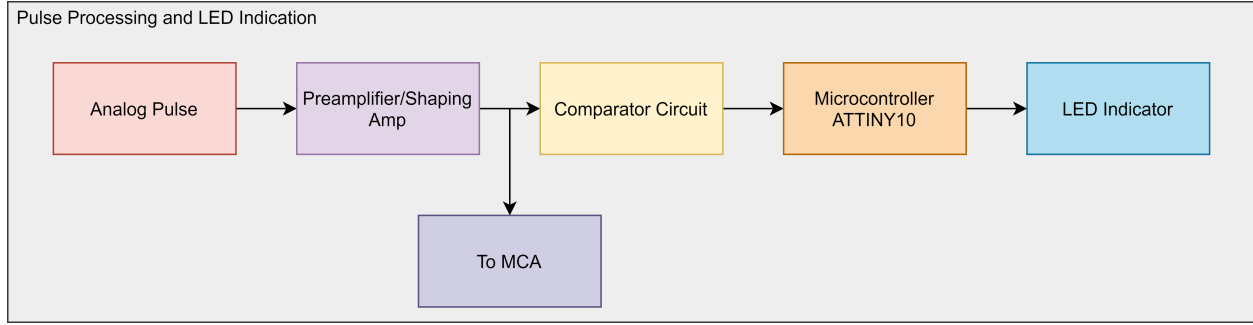


Figure 4.11: PMT pulse processing and LED count rate indication block diagram

As previously indicated, the high-voltage control PCB contains the pulse processing and LED indication circuitry used to complete the tasks designated in Figure 4.11. The schematic for this circuitry can be found in Figure 4.12.

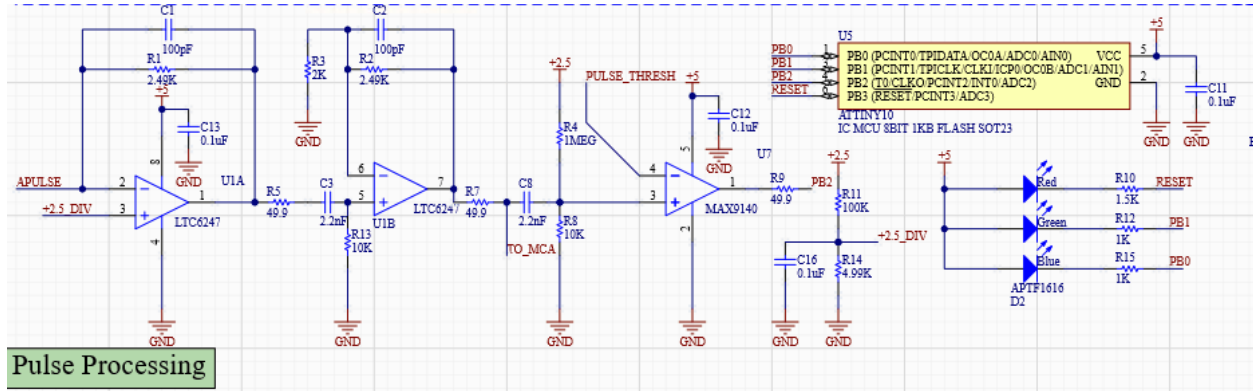


Figure 4.12: The pulse processing circuitry schematic complete with the preamplifier, shaping amplifier, and comparator circuit with microcontroller for LED indication.

As recognized in Section 2.3, pulse processing is used for data collection. To achieve this on the two-board stack design, a single dual operational amplifier package was chosen to be used for both the preamplifier and shaping amplifier, Analog Devices LTC6247⁴⁰. The LTC6247 was selected due to its low input bias current, only 350 nA⁴⁰. Considering this was a dual package, one component can cover both the shaping amplifiers. The LTC6247 occupied 2.9 mm length, 2.8 mm width and 1 mm height⁴⁰.

The preamplifier design used was represented via the operational amplifier U1A in Figure 4.12. The goal of this design was to elongate the pulses from the CsI(Na) crystal as the

charge is produced by the PMT and scintillation crystal. The pulse from the CsI(Na) crystal is composed of a fast and slow part, where the secondary component is 1 μs ²³. Using LTSpice simulation and testing, the values needed were iterated until a pulse was shaped and able to satisfy the timing requirement, typically taken to be 5 times as fast as the input pulse decay time. This allows the full amount of charge produced from the PMT to be captured when integrated over the capacitor in the charge sensitive preamplifier. Using Equation 4.1, 249 ns was found to be an ideal time constant of the charge sensitive preamplifier thus increasing the overall decay time. This constant was matched on the subsequent gain amplifier. The shaping and gain amplifier to create a semi-Gaussian shaped pulse for the MCA data collection was implemented via the second LTC6247 with reference designator U1B. It was designed to match the 249 ns decay time, while including 2.245 V/V amplification to create adequate pulse for data collection.

$$\tau = RC \tag{4.1}$$

ATTINY10 LED Indication

The pulse processing circuitry for LED count rate indication in the schematic in Figure 4.12. This used a MAX9140 comparator to compare the incoming pulse height, AC coupled by the coupling capacitor (C8) to the PULSE_THRESH set by the voltage reference⁴¹. This chip was selected for the low current consumption of 150 μA , and low propagation delay of 40 ns⁴¹. This allowed for a fast response to high numbers of incoming pulses. The integrated circuit package was a SOT23-5pin package with 2.9 mm length, 2.9 mm width, and 1.25 mm height.

If the pulse was higher than the threshold, it triggered an event on an pin that is internally connected to the Atmel ATTINY10 microcontroller⁴². The ATTINY10 microcontroller was selected as an 8-bit microcontroller mainly due to minuscule package size with 2.9 mm length 2.8 mm width, and 1.45 mm height⁴². The microcontroller was connected to the LED, the

APTF1616, a surface mount LED selected for its small size 1.6 mm by 1.6 mm by 0.7 mm thick⁴³. The LED was triggered via a software algorithm.

The software algorithm for the ATTINY10 can be depicted in Figure 4.13, and the algorithm can be found in Appendix B.1. A timer firing every 25 ms was used to help calculate the incoming pulse frequency. The input pin to the ATTINY10 gets triggered from the MAX9140 comparator on a separate routine that fires on the rising edge of the pin. This event increases the number of counts that are used to find frequency. The frequency was compared to the various threshold settings 1, 255, 511, 1023, or greater than 1024. These threshold settings were experimentally set based on moving a 10 μCi ^{137}Cs check source at varying distances. It was discovered that the green and blue segments of the LED pulled the least amount of current to keep the power consumption low. As a result, the green and blue were flashed at varying rates: 1 Hz, 1.42 Hz, 2.5 Hz, 10 Hz, 40 Hz respectively. These values were arbitrarily chosen such to ensure that elevated count rates were easily differentiated from lower.

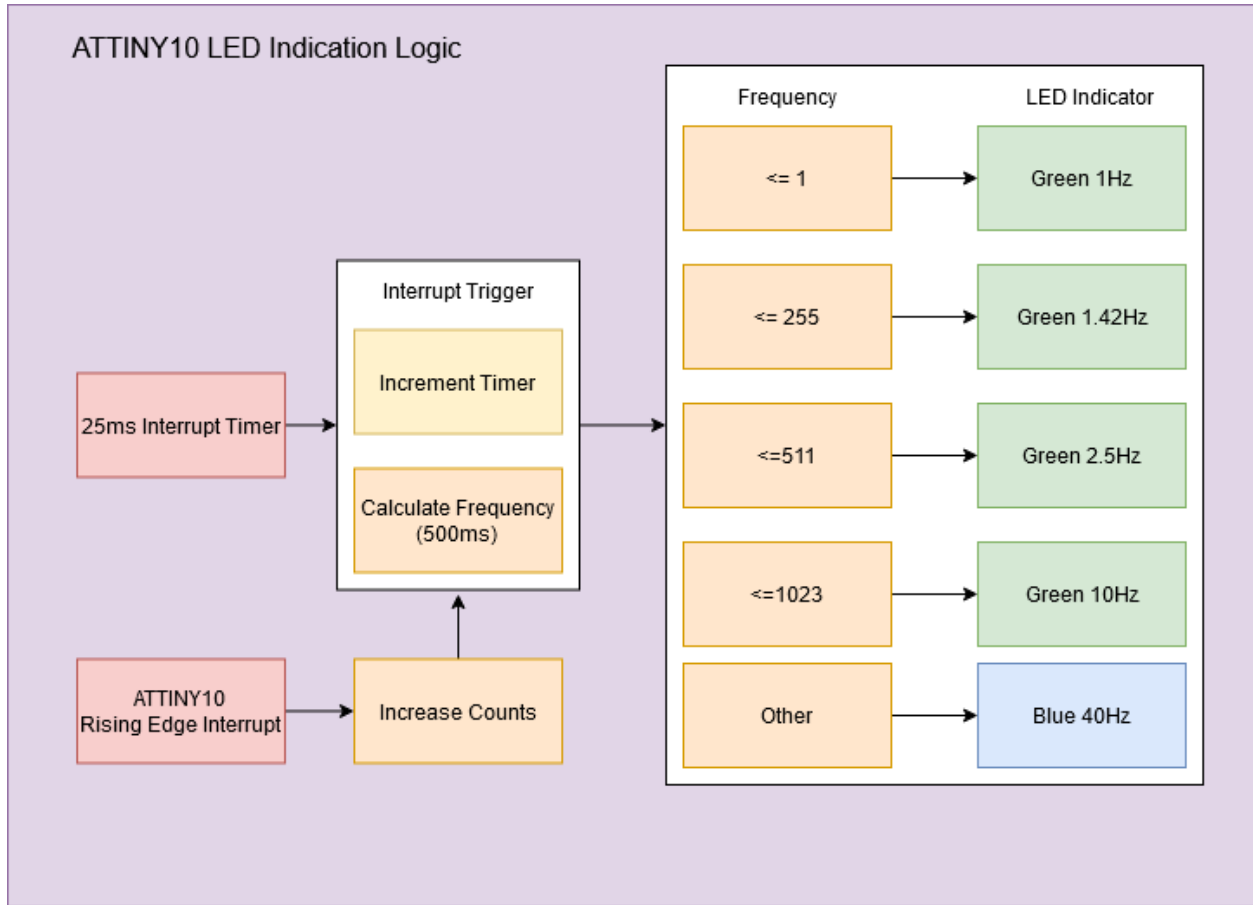


Figure 4.13: A logic diagram for the ATTINY10 and how count rate is indicated via the LED flash.

4.2.5 Threshold Set Points

The threshold set points are defined as HV_SET and PULSE_THRESH. HV_SET was the set point used to control the high-voltage feedback, and PULSE_THRESH was the set point used to control the pulse threshold for the LED indication. Both can be seen in Figure 4.14. The pulses were used throughout other parts of the circuit. To create these references, a Microchip 12-bit digital-to-analog (DAC) converter was selected to allow variable control over these set points⁴⁴. This was a dual package with volumetric size of 6.4 mm width, 3 mm length, and 1.2 mm height⁴⁴.

The DAC used the I2C communication protocol via a separate programmer and header. This allowed for HV_SET and PULSE_THRESH to be reprogrammed as necessary to reconfigure

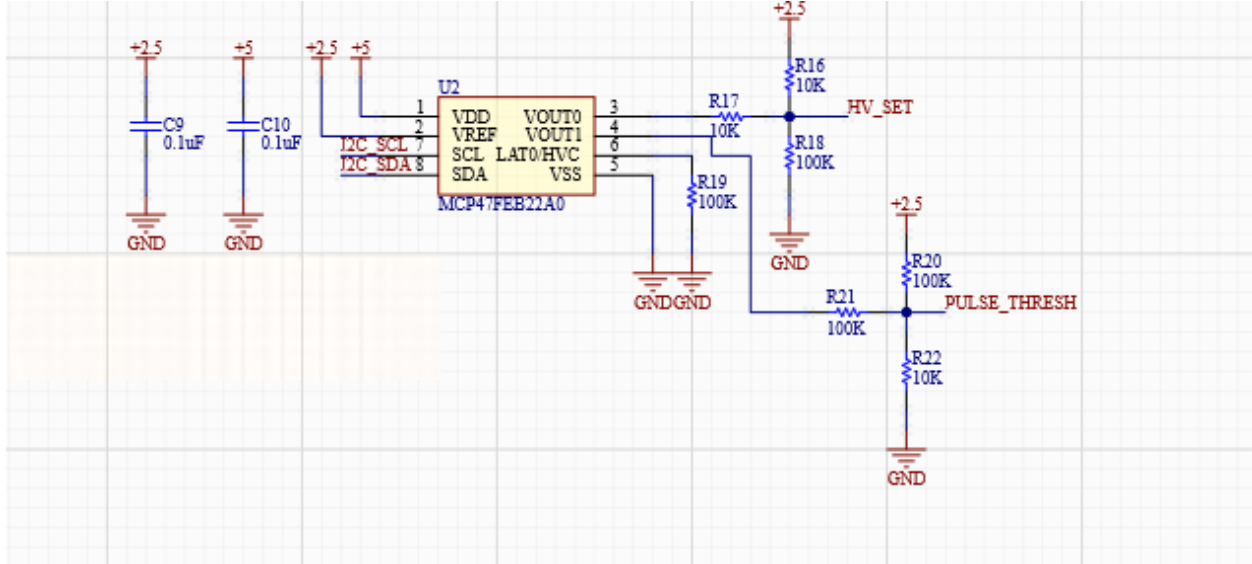


Figure 4.14: A schematic for the thresholds used in each analog operational amplifier design.

the thresholds. However, it was discovered that the device would output 2.5 V, the voltage reference for the chip automatically. This resulted in an adequate voltage for operation of the PMT. Therefore, the control scheme using the I2C protocol was not optimized for this component. However, the HV_SET then defaulted to 2.3 V and PULSE_THRESH defaulted to 75 mV. This value was enough to cause differentiation from noise for the signal to the MCA.

4.2.6 Power Regulation

The power regulation circuitry regulated the input battery voltage to the desired voltages for both boards. The power budget required tens of milliamperes of current. However, the startup current was unknown. To ensure a safety margin, the design was specified to operate within the 1.5 A range, similar to that of the inductor.

For the power regulation circuitry, the 3 V CR123A battery was boosted through a boost converter to 5 V. The circuit was designed to output 5 V with an input range of 2.8 V to 3.2 V, as new CR123A batteries hold voltage at 3.2 V. CR123A batteries are depleted upon 2.8 V as that is the point in which the battery can not remain stabilized under large current

load^{45;46}. From there, the boosted voltage was taken through a voltage reference chip, to output a steady 2.5 V for use in the threshold set points.

A boost converter, the TPS63020, was selected to take the 3 V to the 5 V reference⁴⁷. A boost regulator was selected using the Texas Instruments Webench Power Designer (TI Webench)⁴⁸. TI Webench is an online tool developed by Texas Instruments that allows the user to input desired current and voltage parameters and as a result generate reference designs using a variety of their components⁴⁸. Components can be filtered down by parameters, including size characteristics, number of external components required, and efficiency.

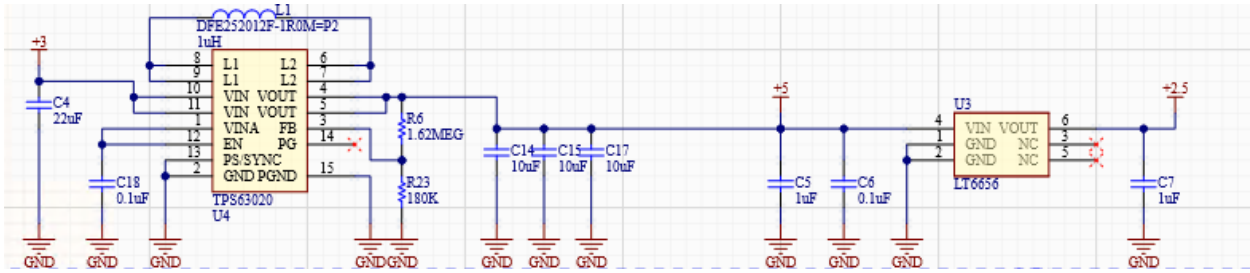


Figure 4.15: Two-board circuit stack power regulation schematic.

A boost switching regulator, was selected over a linear regulator because, because although less efficient than a linear regulator, the 3 V to 5 V potential jump required additional assistance from external components to boost⁴⁹. Furthermore, switching regulators have high efficiency, resulting in low power dissipation except at low load currents⁴⁹.

The TPS63020 boost regulator needed five additional components: an input capacitor, an output capacitor, a resistor divider, and inductor used to control the internal feedback⁴⁸. According to the TI Webench reference design, the design was between 80% to 90% efficient at current loads varying from 200 mA to 1.5 A⁴⁸. Due to the switching nature of the regulator circuit, the output voltage can have noise. As a result, additional filtering capacitors, C15, and C17 were added to the 5 V node. This was because the 5 V line was used to directly drive the Cockcroft-Walton ladder and any noise present would be amplified through the system. Overall, the TPS63020 regulator occupied a space of 2.85 mm by 3.85 mm by 1 mm⁴⁷.

For the 2.5 V voltage reference, the Linear Technology LT6656 was selected due to the fact that it pulls 1 μ A of current⁵⁰. A voltage reference could have been created via a standard resistor voltage divider. However, that would not be as stable as an integrated circuit, as the LT6656 was also capable of outputting within 0.1% of the target⁵⁰. The package was a 2.8 mm by 2.9 mm by 1 mm.

4.2.7 Initial Design Testing Results

This initial two-board stack design was tested using a Rigol DM3058E digital multimeter (DMM)⁵¹. It was found to have an output at the final stage of the Cockcroft-Walton ladder of -735 V.

Power Consumption

The power consumption for the two-board stack was examined using the DMM. The circuit charged instantaneously upon startup and was so fast that the DMM could not catch it with its sampling rate. Therefore, the current limit on the external bench top power supply was lowered from 2 A until the circuit tripped the current limit. This appeared to happen at 1.2 A. Therefore, the instantaneous power consumption can be considered 3.6 W.

The two-board stack was investigated in subsections for power consumption in three key areas. First, the board stack was powered without the PMT or LED indication circuitry. It was discovered that it drew 7.5 mW, 1.5 mA at 3 V. Next, the board stack was powered without a PMT but with the LED indication, the power consumption increased to 30 mW, 10 mA at 3 V. Finally, the two board stack was placed on the R11265u PMT with a 10 μ Ci source present. The two-board stack design consumed 42 mW of power, 14 mA at 3 V. It was found that 71% of the current draw, was due to microcontroller and LED indication light. The summary of these findings is presented in Table 4.1.

Table 4.1: The power consumption of the different measured segments of the two-board stack design. Most of the power consumption is a result of the LED indication.

	Current (mA)	Input Voltage (V)	Power (mW)
High-Voltage and Regulation	1.5	5	7.5
Signal Processing, Power, LED	10	3	30
On PMT with ^{137}Cs 10 μCi	14	3	42

Control Instability Voltage Measurement

Due to limitations with the DC input to an oscilloscope the control instability was measured as a rippling voltage across a large capacitor. A 6.2 kV, 2.2 nF through hole capacitor, acted as a DC block. This meant that the capacitor only allowed the alternating signals to pass through, and blocked any DC components making it possible for the any inconsistency to be viewed. This was possible due to two things, the insulation resistance of the capacitor and the internal impedance of the oscilloscope. The insulation resistance of the capacitor (DC leakage) was 10 G Ω while the oscilloscope internal impedance was 10 M Ω . The oscilloscope internal impedance and the capacitor insulation resistance create a voltage divider such that any ripple on a 1 kV signal would have appeared to have a maximum ripple of 1 V_{pp}.

Measuring the final stage of the Cockcroft-Walton ladder resulted in Figure 4.16, or a value of 784 mV_{pp}. Due to the nature of the circuitry, the value represented on the final stage of the Cockcroft-Walton circuit resulted is the maximum value, the dynode stages are exhibiting less.

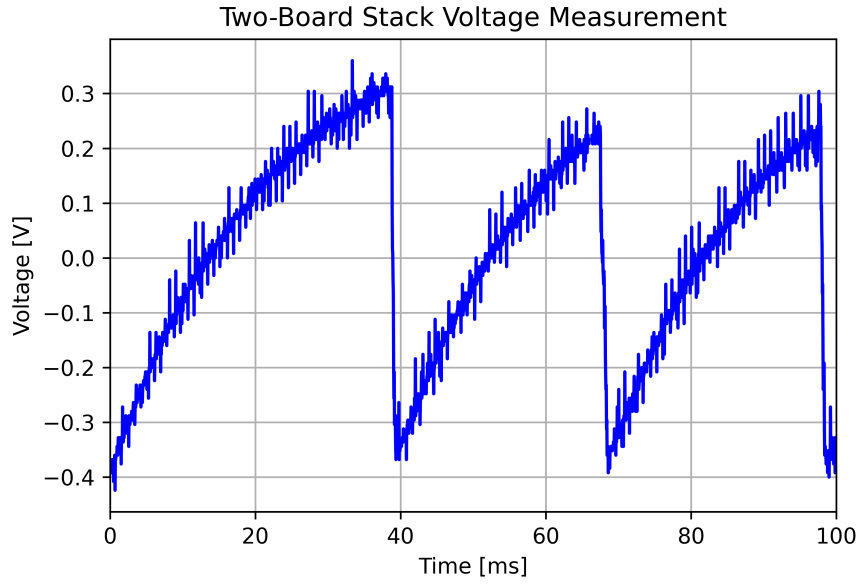


Figure 4.16: Two-Board stack control voltage instability measurement through at 2.2 nF capacitor.

Any ripple or inconsistency in voltage caused by the feedback control of the high voltage circuit voltage was detrimental to the validity to the PMT output, specifically with the energy resolution of the detector. The MCA correlated the incoming pulses into binned channels. The software used to capture this data was Ametek Ortec Maestro⁵². The MCA used for data collection was the Ortec 927, a NIM equipment module that allows the collection of high-performance data acquisitions for nuclear spectroscopy⁵³. The number of channels that Maestro was able to display was configured for 1024.

Energy range of concern is between 30 keV to 3 MeV for terrestrial gamma-ray spectroscopy. Correlation exists in energy MeV and the number of channels configured for Maestro, 1024. This resulted in a ^{137}Cs peak being located at channel 225, as ^{137}Cs releases energies at 0.662 MeV⁵⁴. For energy resolution for the CsI(Na) scintillation crystal of 7% at 0.662 MeV, the full width at half max (FWHM) of the peak divided by the peak location in MeV, was calculated to have a span of 16 channels due to the initial peak shift. For example, if a voltage ripple is induced that caused variance of 1% on the gain, then this correlates to 10 channels of variance for the FWHM, which represents a change in energy resolution of the

7% energy resolution up to 11.45%. An example of what happens to a Gaussian pulse can be found in Figure 4.17.

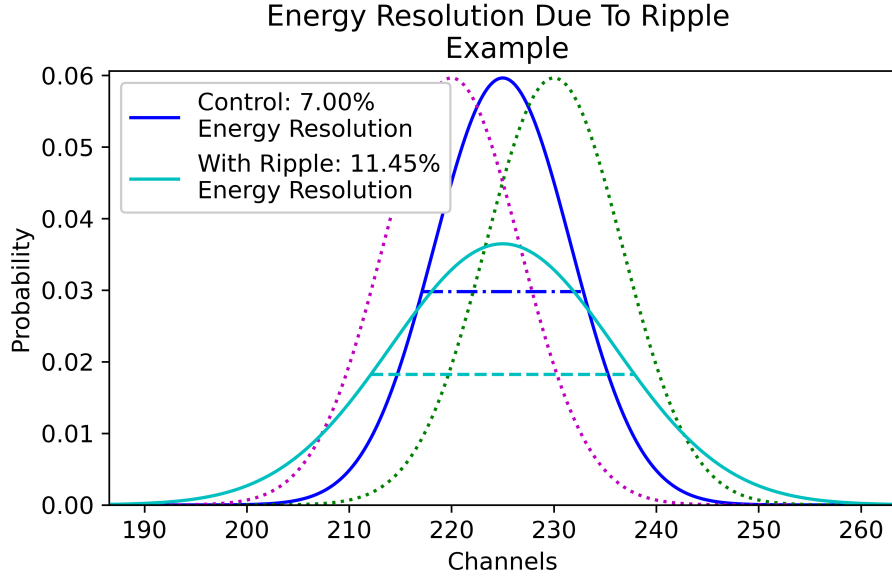


Figure 4.17: Example voltage ripple effect on energy resolution peak.

To investigate how the voltage fluctuation affected the signal out of the PMT the following parameters were defined. The gain of the PMT was proportional to the current gain defined in Equation 3.4. A new equation to represent this relationship was shown in Equation 4.2²¹.

$$G_{PMT} \propto \mu \quad (4.2)$$

Assuming that A^n was a constant value equal to 1, Equation 3.4 and a k-value provided by Hamamatsu for the R11265U PMT, the current gain equation was simplified to Equation 4.3⁵⁵.

$$\mu = V^{(0.74n)} \quad (4.3)$$

Using Equation 4.3, the overall operating voltage, and the measured ripple caused by the control loop, a percentage of which the PMT gain can fluctuate was calculated. For the 784 mV_{pp},

a current gain fluctuation of 0.94% is observed. This can cause an additional 9.6 channels to the FWHM, which represents a change in energy resolution of a 7% detector, to 11.27%. An example of what happens to a Gaussian pulse can be found in Figure 4.18.

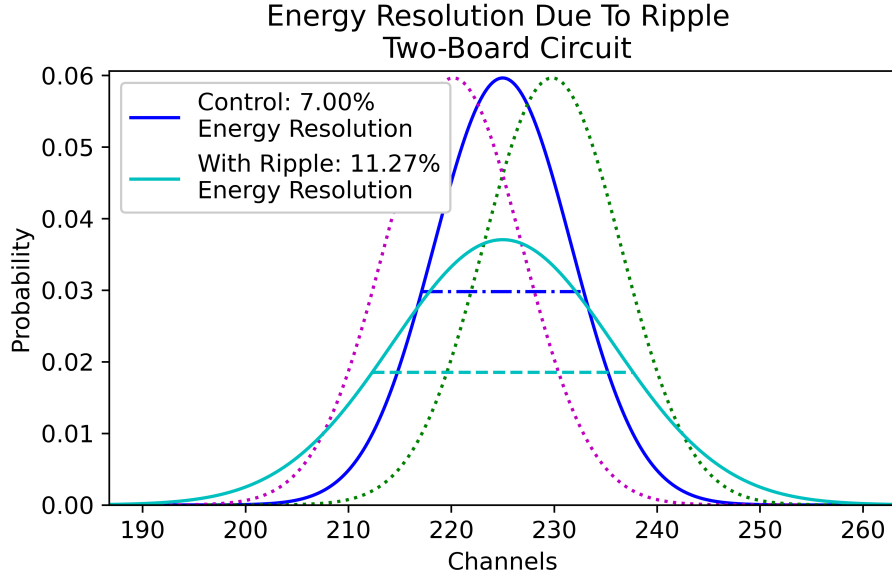


Figure 4.18: Two-board circuit control instability ripple effect on energy resolution peak.

Radiation Spectroscopy

Radiation spectroscopy was taken with the NIM equipment running at -750 V with the Hamamatsu R11256U base. The raw pulse from the Hamamatsu R11265U base was collected. The pulse, presented in Figure 4.19, was taken with a $10\text{ }\mu\text{Ci}$ ^{137}Cs check source 8 inches from the broad-side of the PMT with the manufacturer base. The pulse exhibited a rise time of 8 ns and decay time of $1.08\text{ }\mu\text{s}$. The pulse was negatively biased as a result of electrons being collected at the signal electrode. The results align well with the expected $1\text{ }\mu\text{s}$ decay time for the crystal²³.

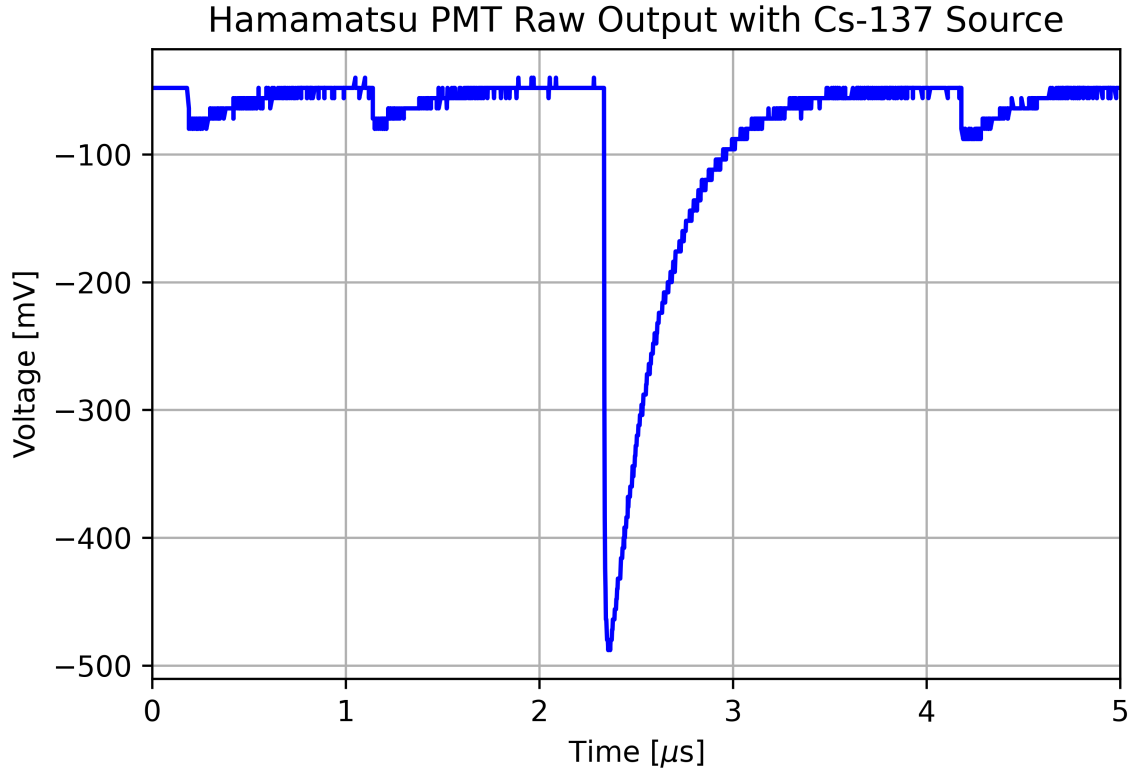


Figure 4.19: Calibration setup for the two-board stack with ^{137}Cs check sources.

The pulse with the Hamamatsu base was then calibrated with the ^{137}Cs 10 μCi source using the Ametek Ortec preamplifier model 113 and the Ametek Ortec amplifier model 571 (currently manufactured as model 570) before being fed into the Ametek Ortec 855^{53;56;57}. The Caen DT8033M bench top power supply was used operating at -735 V ⁵⁸. The preamplifier for this pulse was set to have an input capacitance of 500 pF such that it is large compared to the PMT capacitance. Additionally, a 100 k Ω terminator was placed on the output as to prevent bipolar output or baseline shift. The amplifier was selected to have a shaping time of 3 μs . As a result of the linearity between the number of channels use to process with the MCA and the 3 MeV spectral range desired, the ^{137}Cs source should show up around 0.662 MeV or channel 225⁵⁴. The gain value was adjusted experimentally to line up with channel 225 and the spectra were able to be gathered.

For a calibration spectra for direct comparison, a 10 μCi ^{137}Cs check source was placed near

the detector. A similar setup was reflected for the custom two-board stack, however there was no need for any preamplifier or amplifier electronics as they were integrated into the design.

For the two board stack, the raw signal pulse was inaccessible for an oscilloscope measurement. However, it should have been similar to that expressed previously. For pulse shape verification the ^{137}Cs shaped pulse was captured. The two-board stack pulse processing circuitry generated a pulse with amplitude 1.5 V, rise time of 312 ns, the time it takes for a charge from 10% of the maximum signal to 90% of the maximum signal, and decay time of 930 ns, the time it takes to fall to where the amplitude was 63.2% of the max³². Although the pulse is not perfectly Gaussian, it is shaped and amplified such that the MCA will be able to detect events. The pulse is seen in Figure 4.20.

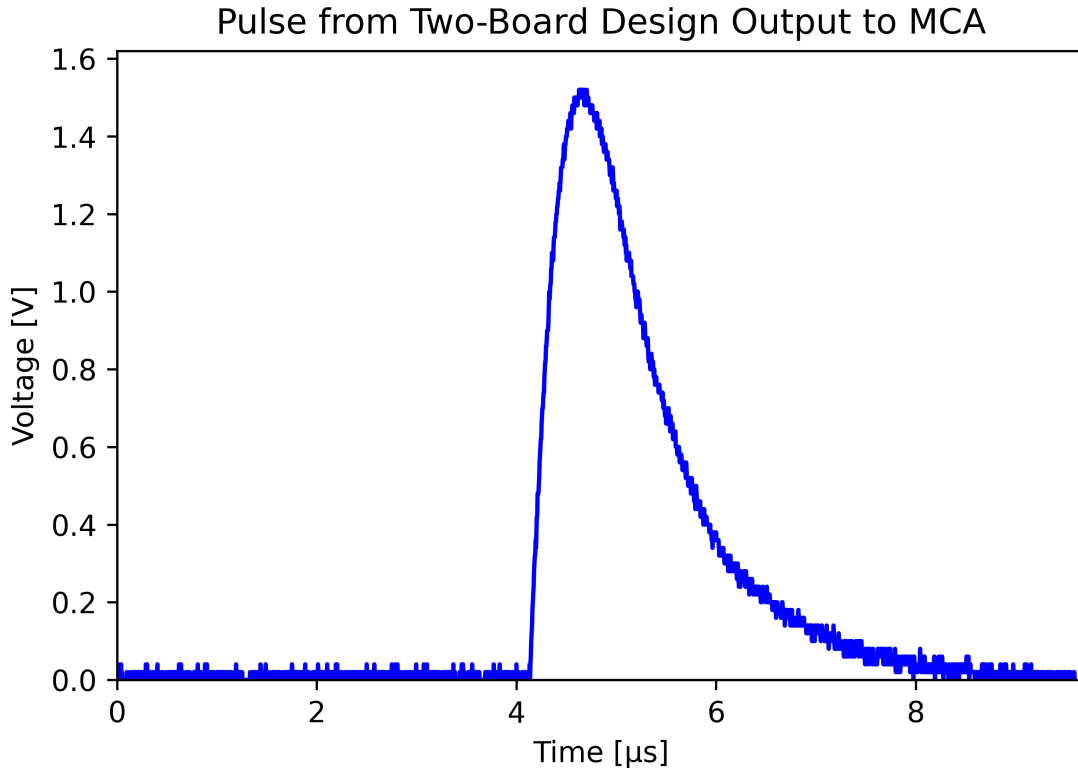


Figure 4.20: The two-board stack shaped pulse input to the MCA.

Spectra were plotted using Spectral Processing and Analysis Tool (SPAT), a custom written Python application for radiation spectral analysis and post processing. The spectra were software calibrated using a linear least squares regression resulting in a calibration in the form of a line, $y=mx+b$. The calibration points for all measurements were the isotope of ^{137}Cs , 0.662 MeV with photon x-ray at 32 keV⁵⁴. The Hamamatsu engineered base was able to obtain an energy resolution of 7.5% for ^{137}Cs as seen in Figure 4.21. The two-board stack presented in Figure 4.22, resulted in an energy resolution of 8.5% for ^{137}Cs .

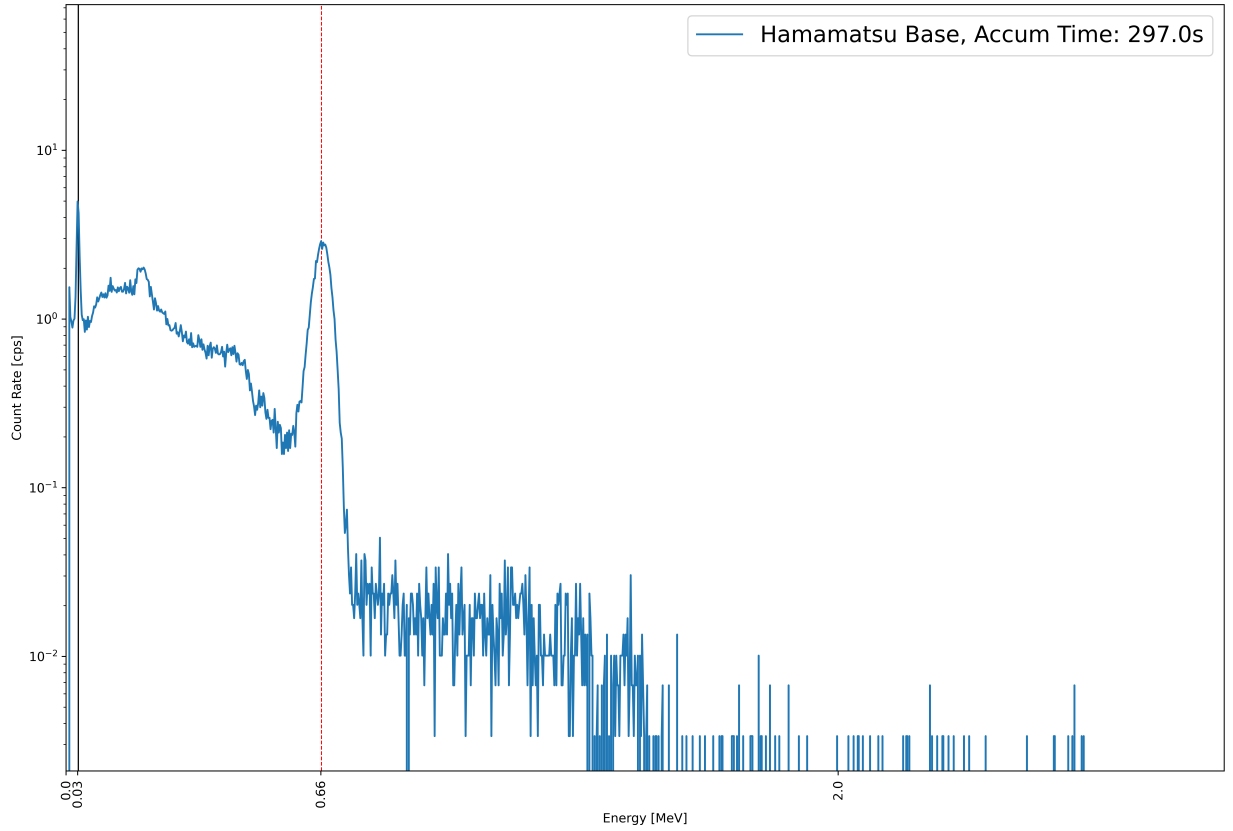


Figure 4.21: Hamamatsu R11256U PMT Base spectrum from a 10 μCi ^{137}Cs check source.

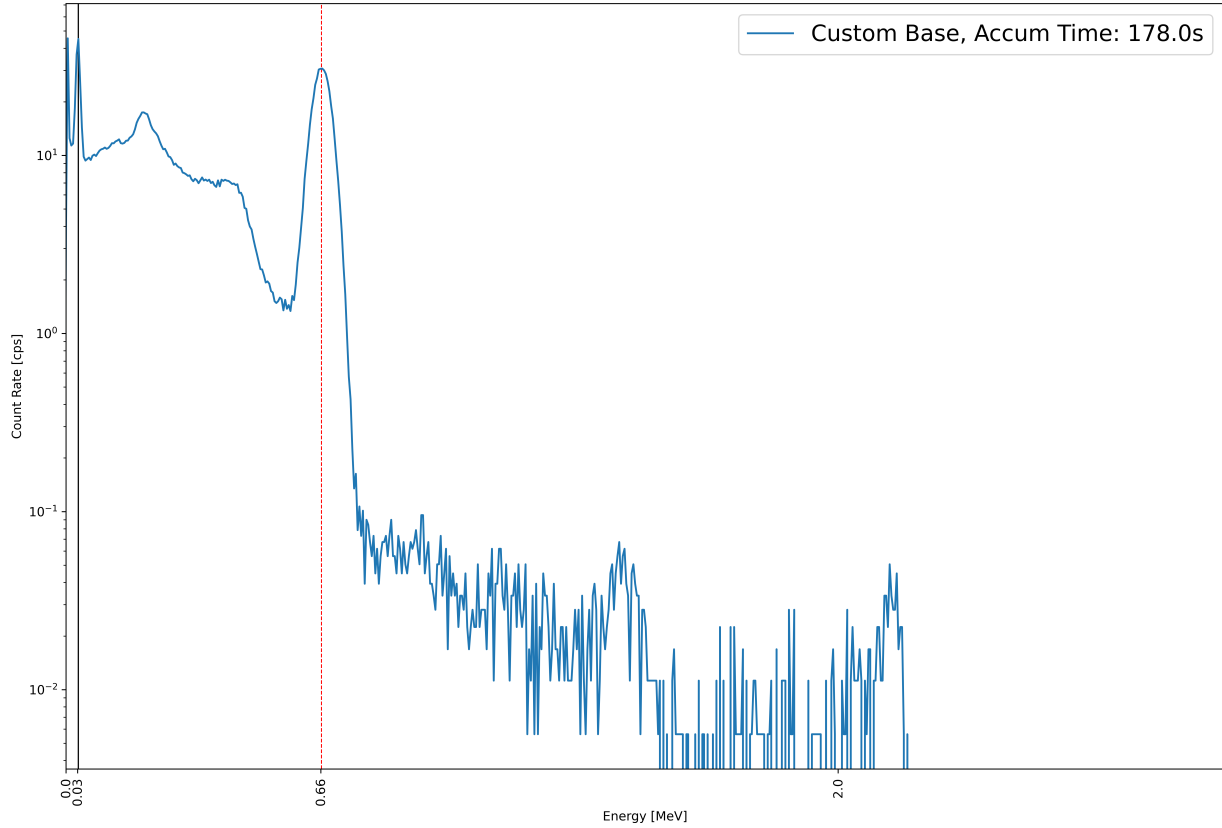


Figure 4.22: The two-board stack design spectrum from a ^{137}Cs check source.

Power Consumption vs Count Rate - Low Count Rate

To capture the effects of the count rate as a function of power consumption, an experimental setup was configured. A ^{137}Cs 10 μCi check source was moved along a surface in 2 inch increments from 20 inches to 2 inches away from the side of the PMT. The DMM was used to gather real-time data of the current consumption. When reviewing the data, it appeared to exhibit a square wave, as seen in Figure 4.23. Upon further inspection, it was discovered that the shape was a result of the blink of the LED.

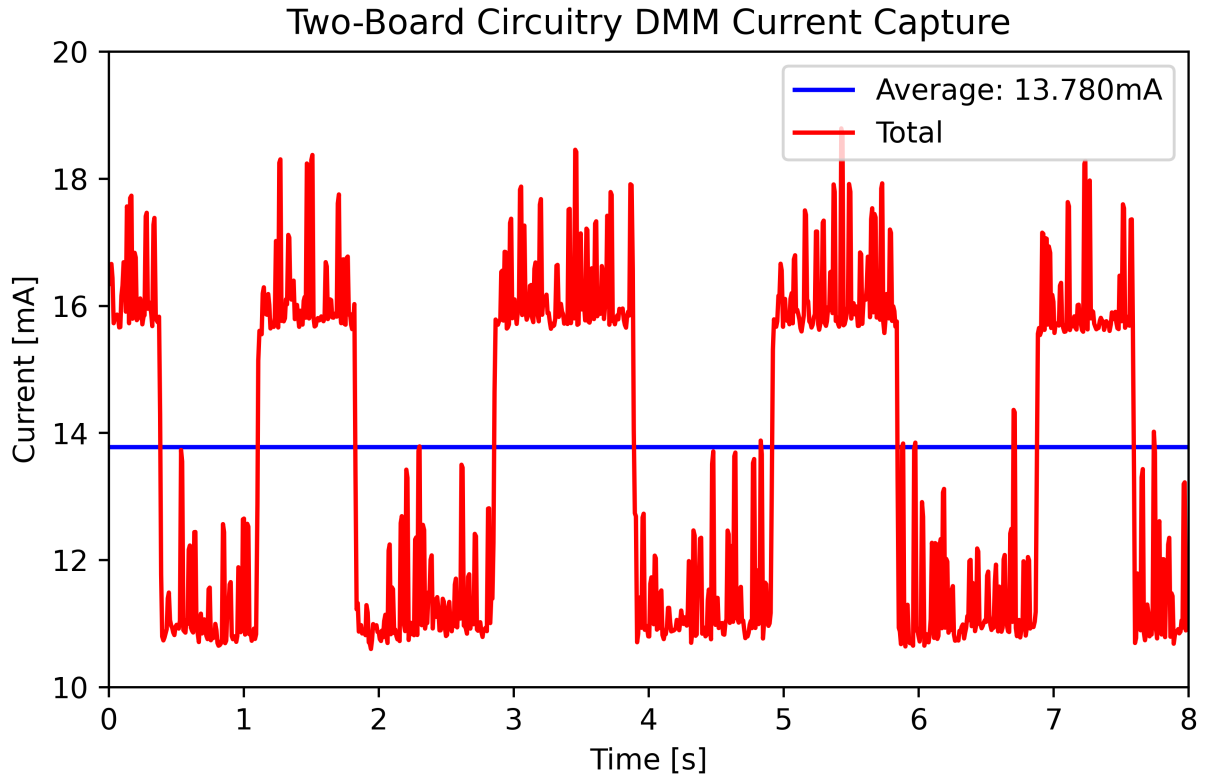


Figure 4.23: Example of Rigol DMM data capture for current for the two-board stack.

To verify the count rates accuracy, a ($distance^{2^{-1}}$) approximation was plotted as a function of the distance from the broad side of the detector as seen in Figure 4.24.

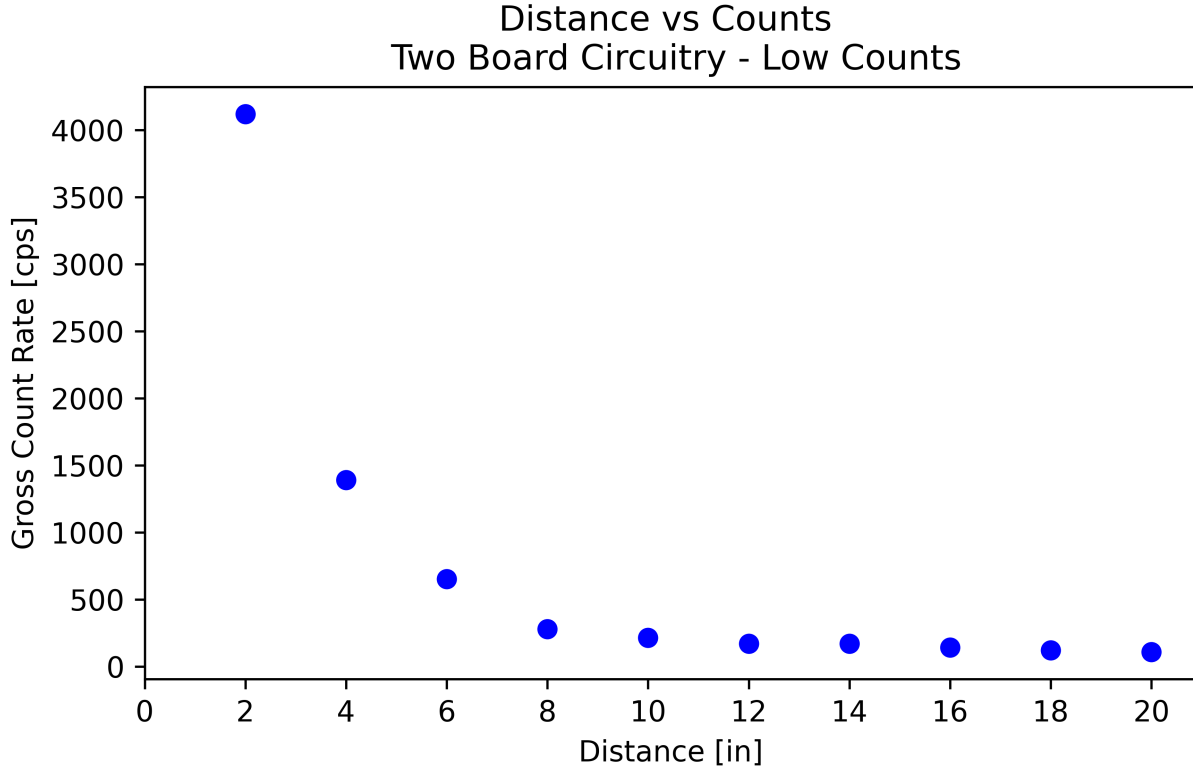


Figure 4.24: Count rate as a function of distance for the two-board circuit stack.

Consequently, the data was analyzed in three ways, the average power, for the current when the LED was on, and the current when the LED was off. The data was analyzed using a root sum squared method seen in Equation 4.4 for the uncertainty of each measurement. The average power was 40.2 mW with an uncertainty of 4.22 mW, the power during the LED on state was 47.5 mW with an uncertainty of 1.22 mW, and the power during the LED off state was 32.9 mW with an uncertainty of 1.46 mW. The result of the count rate and power consumption measured of the two-board stack can be found in Figure 4.25.

$$U_{\text{total}} = \sqrt{U_{\text{equipment}}^2 + U_{\text{linear}}^2 + U_{\text{random}}^2} \quad (4.4)$$

where $u_{\text{equipment}}$ is the uncertainty of the measurement device, the u_{linear} is the uncertainty due to the linear fit, and the u_{random} is the random uncertainty that encapsulates other potential error.

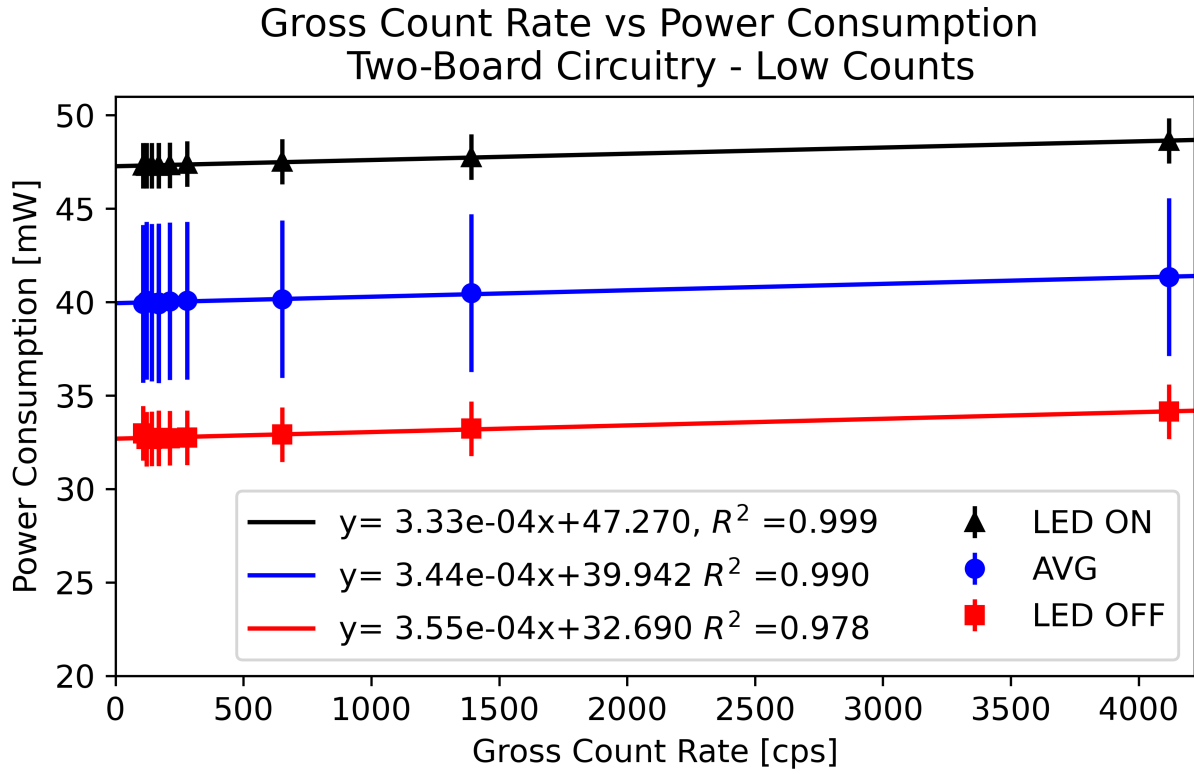


Figure 4.25: Power regulation for the two-board circuit stack as a function of count rate for the distance variation measurements.

Power Consumption vs Count Rate - High Count Rate

An alternate test using a variety of sources to achieve high count rates was conducted where the sources were touching the 4 broad sides of the detector. The test configurations can be found in Table 4.2.

Table 4.2: Check source setup for each test to achieve elevated count rates with the two-board circuit stack.

Check Source	Test						
	1	2	3	4	5	6	7
^{133}Ba 1 μCi	X	X	X	X	X	X	
^{109}Cd 1 μCi	X	X	X	X	X	X	X
^{137}Cs 0.25 μCi	X	X	X	X	X	X	X
^{57}Co 1 μCi	X	X					
^{60}Co 1 μCi	X	X	X	X			
^{54}Mn 1 μCi	X	X	X	X	X		
^{22}Na 1 μCi	X	X	X	X	X	X	X
^{65}Zn 1 μCi	X						
^{152}Eu 1 μCi	X	X	X				

As with the low count rates, the current consumption was measured using the DMM and the power consumption was then calculated. The data was analyzed using a root sum squared method seen in Equation 4.4 for the uncertainty of each measurement. The average power was 45.2 mW with an uncertainty of 4.21 mW, the power during the LED on state was 52.2 mW with an uncertainty of 1.64 mW, and the power during the LED off state was 37.7 mW with an uncertainty of 1.33 mW. The power consumption average increased by 12.4%, the power consumption for the LED on increased by 9.9% and the power consumption for the LED off increased by 14.6% between the low and high count rate tests. However, it is expected that the trend for each data set begin to level out upon reaching a certain count rate, however that value is currently unknown.

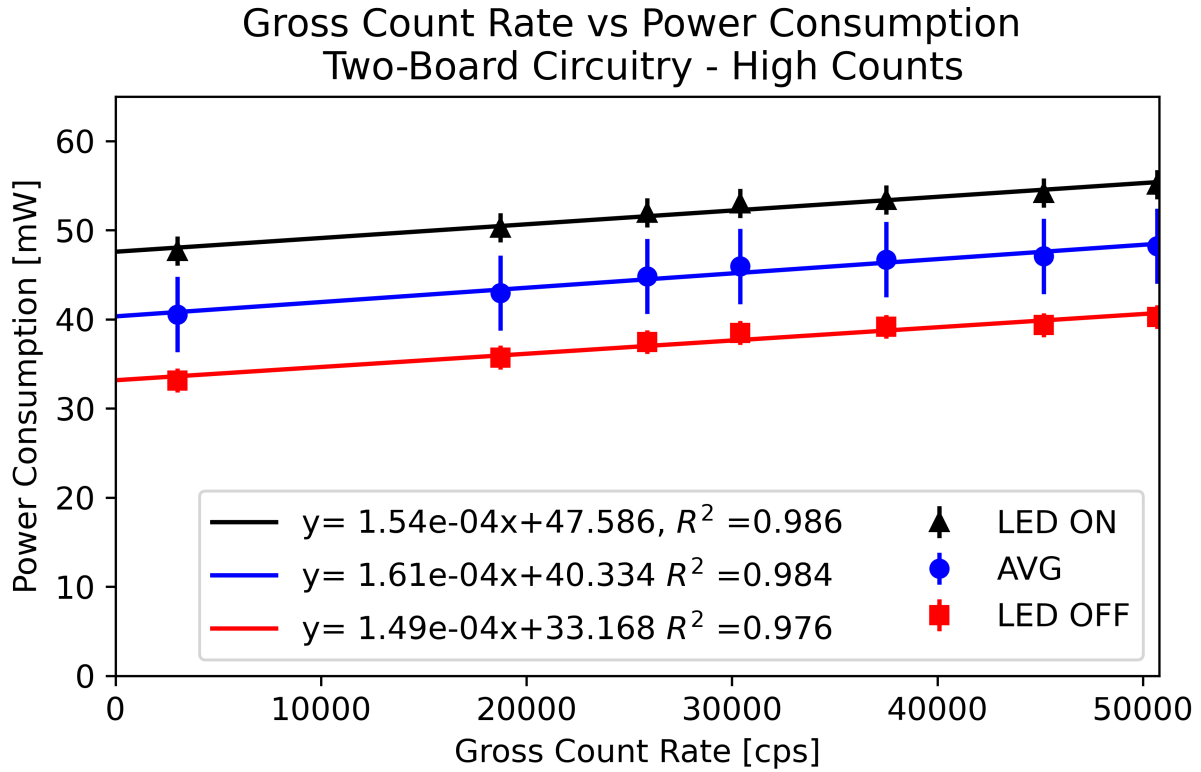


Figure 4.26: Power regulation for the two-board stack as a function of count rate.

Battery Life

Battery life is important in the 3D design, as size, weight, and power (SWaP) is beneficial in mobile detection systems. The battery will output at 3.2 V and is considered dead around 2.8 V. Battery life was investigated using a Raspberry Pi 3B+ and an Adafruit ADS1115 ADC^{59;60}. The voltage of a CR123A battery was measured on the two-board PCB attached to the PMT using the Adafruit ADS1115 ADC⁶⁰. The data was recorded every second and ended when the battery voltage reached 2.8 V. This resulted in lasting 2 d, 19 h. However, upon ending the experiment the LED was still flashing indicating some power still remained. This meant that the mobile detection unit would last longer in the field, however that time is currently unknown.

4.3 Iterations

The two-board stack was a prototype. However, design changes were made to improve performance. One of the main concerns was the number and size of components. Furthermore, the inconsistency of the Cockcroft-Walton high-voltage supply circuit was significant, as the energy resolution from the scintillation crystal was not optimized. Moreover, the power consumption was investigated and attempts were made to reduce it.

4.3.1 Front-End Charge Pump Simplification

ATTINY85 Microcontroller

The first design modification involved the Cockcroft-Walton charge pump, and feedback circuitry used to sustain high-voltage. It was investigated to see if any of the analog circuitry could be replaced with a digital counterpart. Other designers used digital control to control the front end with a pulse width modulation (PWM) and Complex Programmable Logic Devices (CPLD), a field-programmable gate array (FPGA), which controlled the bridge created by MOSFETs and a 1:1 high frequency transformer for the front end⁶¹.

The circuitry stepped a reference from the final stage of the Cockcroft-Walton ladder down through a series of comparator circuits. Since microcontrollers have built in ADCs, they are prime candidates for taking over the analog logic. Additionally, microcontrollers can output signals, such as a PWM square wave to mimic that of the switching circuit. To create a small form factor, a microcontroller is typically smaller than an FPGA. As a result, a microcontroller was beneficial. Due to familiarity with Atmel ATTINY family in the LED indication circuit, an ATTINY85 microcontroller was selected⁶². This 8-bit microcontroller operates up to 6 V with a DC current draw of up to 200 mA⁶².

Since the Cockcroft-Walton circuitry was negatively biased, the feedback control must be inverted. This was best done through an inverting amplifier. In order to step the voltage down for the ATTINY85 ADC input, a feedback voltage divider circuit was executed through the

amplifier. The procurement of the $1\text{ G}\Omega$ resistor for the high-voltage feedback circuit was difficult due to supplier inventory. Therefore, two $400\text{ M}\Omega$ resistors in series were used instead. LTSpice simulation software was used to simulate the response of the circuit as shown in Figure 4.27³. To get -1000 V high-voltage under 5 V for input into the microcontroller ADC, a $3.4\text{ M}\Omega$ feedback resistor was placed creating a gain of -4.25 mV/V producing an output of 4.25 V at -1000 V . A 100 pF capacitor was placed in the feedback loop to retain amplifier stability.

An over-voltage protection diode was also added to prevent the input pin exceeding 5 V . It is possible during testing, the addition of impedance of the oscilloscope can blow out the front end of the amplifiers.

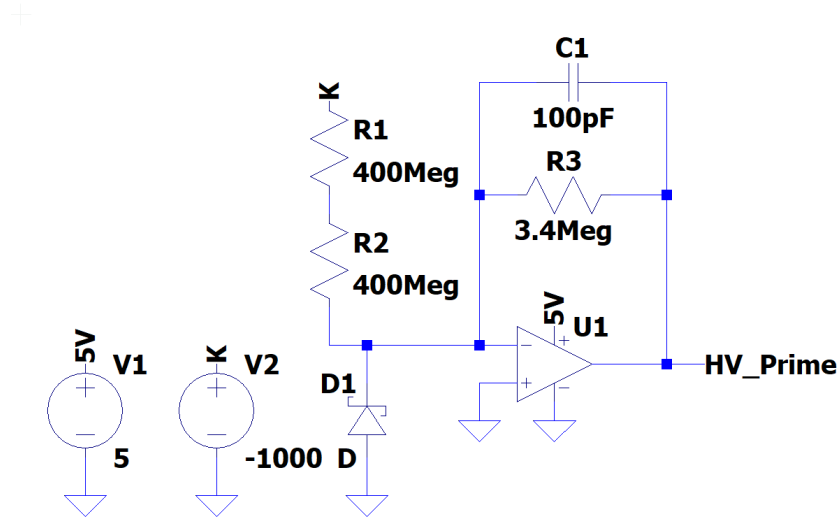


Figure 4.27: LTSpice simulation for inverting amplifier for new feedback circuitry³.

To reduce the size of components and reduce power consumption, an amplifier, the Rohm Semiconductor BU7445 was selected by filtering a component supplier for a low power consumption device in a small package size capable of being operated at 5 V⁶³. This operational amplifier only needed 40 μ A of supply current with low input bias. The package was 1.6 mm by 1.6 mm by 0.6 mm⁶³.

To verify the microcontroller control, the high-voltage Cockcroft-Walton ladder was stripped of all additional filtering circuitry and the PMT socket connection. The ATTINY85 test circuit was powered via an external bench top power supply removing the necessity of any regulation circuitry. Finally, a new Cockcroft-Walton diode variant, the NSD914XV2, with the same specifications as the two-board stack was used⁶⁴. These diodes were 1.2 mm by 0.8 mm by 0.6 mm⁶⁴. The diode size was chosen due to the intent in using the laser welder to create sub assemblies. The diode choice allowed for the size of the laser on the laser welder to not be larger than the component. The schematic and bill of materials can be found in Appendix A, but the circuit board in Altium Designer is shown in Figure 4.28².

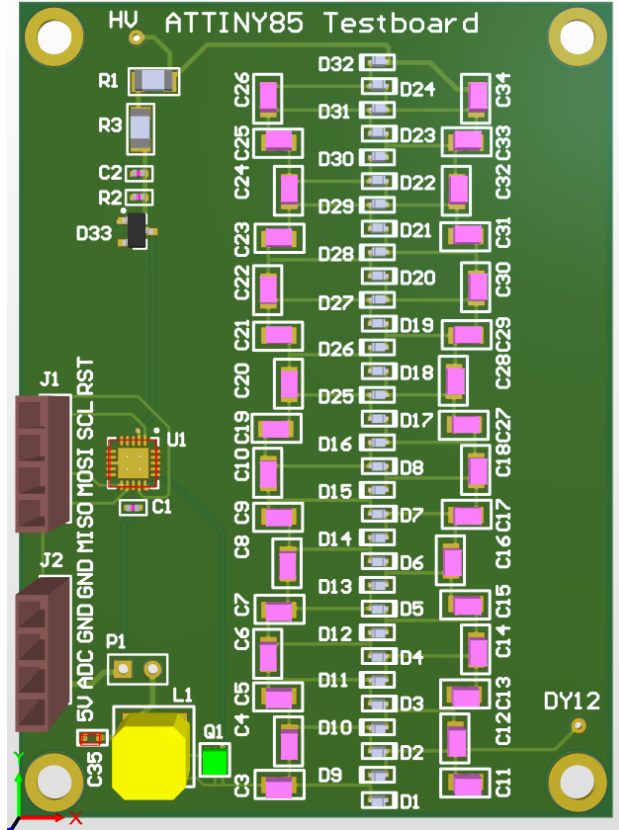


Figure 4.28: The stripped circuit using the ATTINY85 design as presented in Altium Designer². This circuit was used to verify that the microcontroller front-end was worth pursuit.

An 8-bit Microchip ATTINY85 microcontroller was programmed to act as the driver to the Cockcroft-Walton ladder. Using the built in ADC to process the high-voltage feedback through an amplifier, the built in PWM output was used and the circuit was able to implement a slow-start function to eliminate the large current draw seen in the two-board design. The circuit used a base equation following an exponential curve to slowly ramp up the duty cycle percentage of the PWM until it reached 50% or the circuit charged to the desired set point voltage as seen through the ADC. An approximation for the algorithm can be found in Figure 4.29 as a function of duty cycle over time.

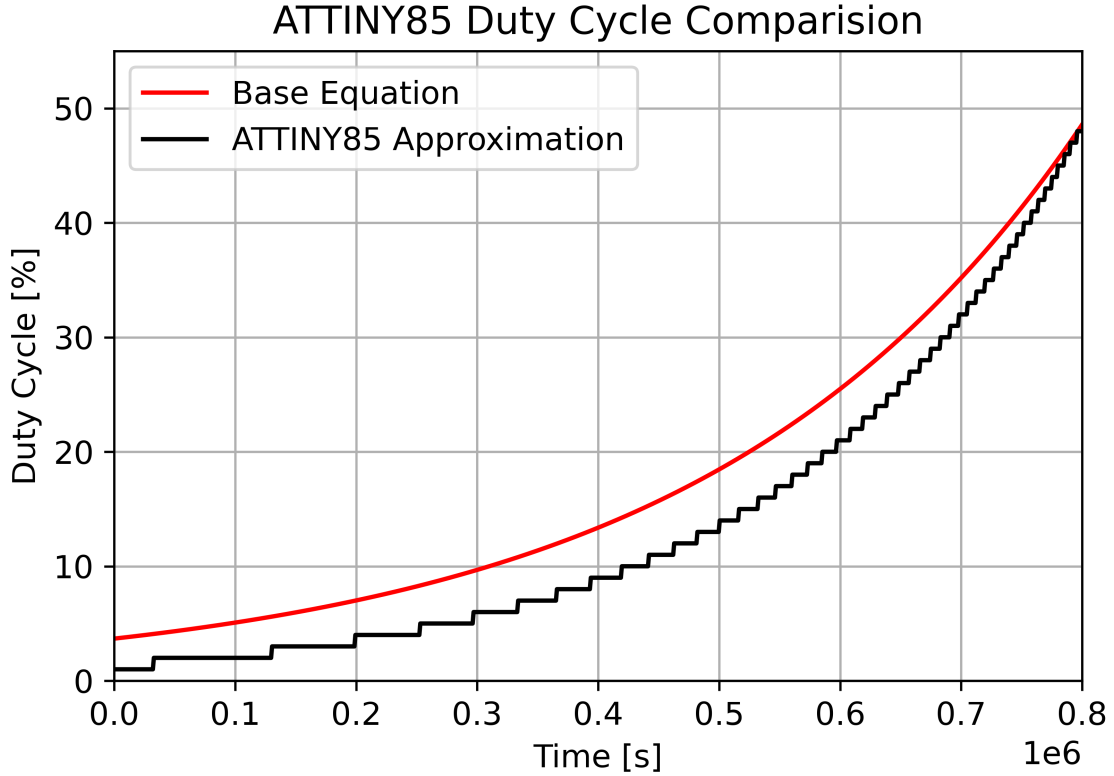


Figure 4.29: A comparison to an exponential curve created to ramp up the duty cycle for the PWM upon startup. This was approximated for the ATTINY85 implementation due to the accuracy of the microcontroller.

For the implementation of the algorithm, found in Appendix B, a delay was added between each step to allow adequate time for PWM signal to propagate through the ladder. The circuit charged up without any issues to -726 V with steady-state power consumption of 40.5 mW , comparable to the 48 mW two-board design.

The need to run the circuit at 5 V , as in the two-board design, was questioned. Therefore, the ATTINY85 test board was reconfigured to operate with a 3.3 V input, as the ATTINY85 and amplifier can function at this voltage^{62;63}. This meant that the PWM output to the MOSFET was 3.3 V_{pp} . This test concluded that the same -726 V could be achieved at an operating voltage of 3.3 V , and with a power consumption of 15.84 mW . This was a 67% decrease in power consumption and 22% reduction in the number of charge pump components compared to that of the two-board design.

PIC Microcontroller

Having the success with the ATTINY85 test circuit, the next goal was to reduce the power consumption of the microcontroller. After extensive research, the Microchip PIC12F1572 was selected⁶⁵. This was an 8-bit microcontroller that highlighted the low current consumption⁶⁵. This microcontroller featured a 16-bit PWM, 10-bit ADC and a graphical user interface (GUI) called the MPLABX development environment that allowed the user to select configuration options and have header files generated^{65;66}. A separate serial hardware programmer was necessary that allowed interfacing with the MPLABX development environment called the MPLAB PicKit4 In-Circuit Debugger^{66;67}.

A through-hole variation of the microcontroller was purchased to verify that duty cycle approximation was achievable due to the unfamiliarity with the PIC microcontroller family. It was discovered that the PIC microcontroller did not have floating point operation like the ATTINY85. As a result, a new approximation for the duty cycle startup was completed by creating a linear piecewise function between various duty cycle segments. Using a bench top power supply, the PIC microcontroller was measured to have a power consumption of 4.95 mW at 3.3 V with the startup animation running. The approximation used can be found in Figure 4.30.

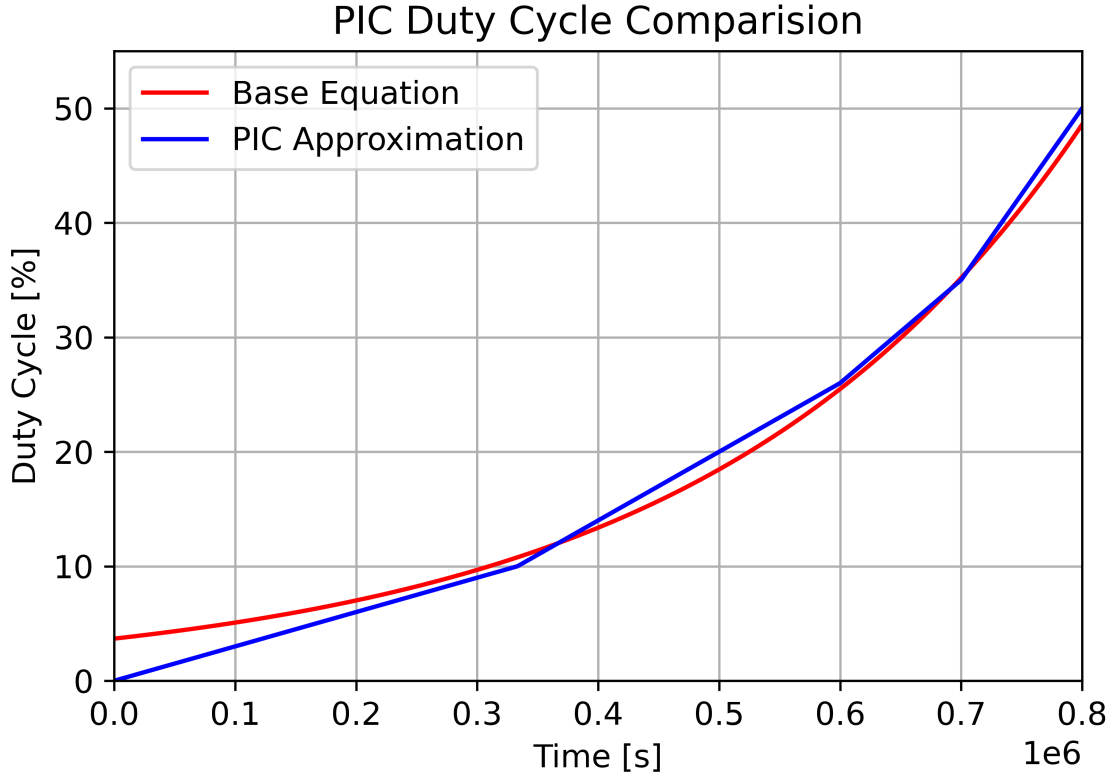


Figure 4.30: A comparison to an exponential curve created to ramp up the duty cycle for the PWM upon startup with the piecewise function of the PIC microcontroller.

4.3.2 Power Regulation Circuitry Simplification

Due to the ATTINY85 microcontroller success with operation at 3.3 V, the power regulation circuitry needed to be reconfigured. Using TI Webench resulted in the selection of the Texas Instruments TPS63001^{48;68}. The TPS63001 was selected due to the maximum 96% efficiency at varying load, and only needing 3 additional components for operation⁶⁹. This resulted in an overall component reduction of 70%. Furthermore, the package size was only a 3 mm by 3 mm by 1 mm component⁶⁹. The new schematic can be seen in Figure 4.31.

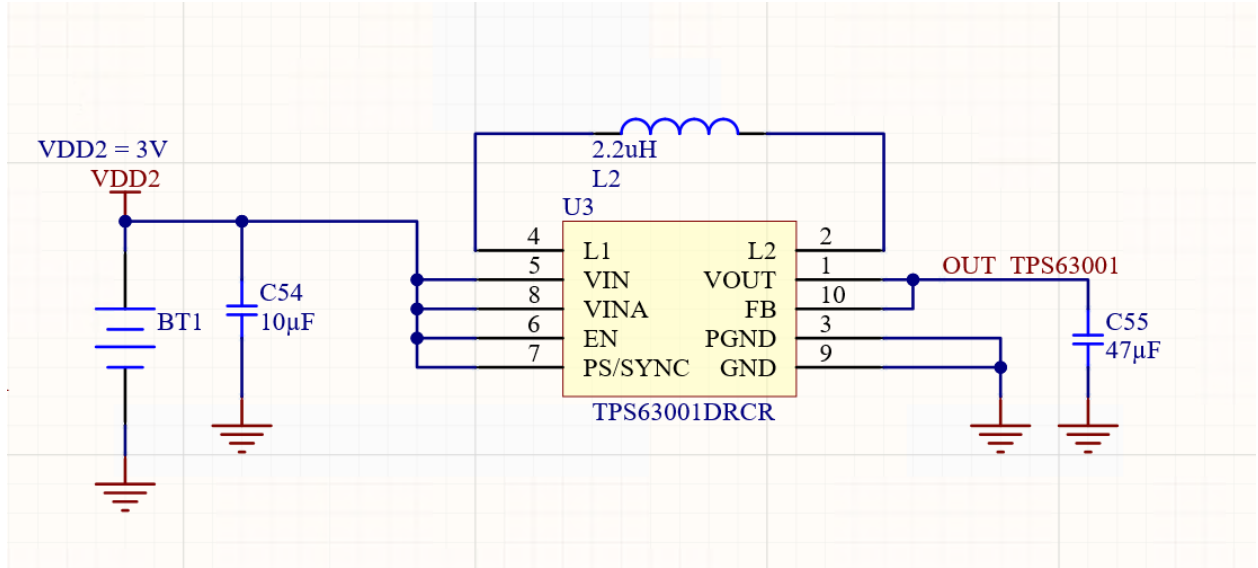


Figure 4.31: Updated circuitry for the power regulation as seen through Altium Designer².

4.3.3 Pulse Processing Simplification

To reduce the power consumption while also aiming to reduce the number of components, the ATTINY10 indication circuitry and indication LED was removed from the circuit to allow flexibility for the future needs of the project. All 9 components that make up the preamplifier and shaping amplifier from the two-board stack are included in the component count. An external NIM preamplifier and shaping amplifier was used going forward as a replacement for testing.

Chapter 5

Finalized Design

5.1 Design Overview

The Cockcroft-Walton high-voltage supply board was simplified relative to the two-board design into a single PCB. The PCB on the CsI(Na) 1 inch by 1 inch by 3 inch PMT and scintillation crystal can be found in [Figure 5.1](#).

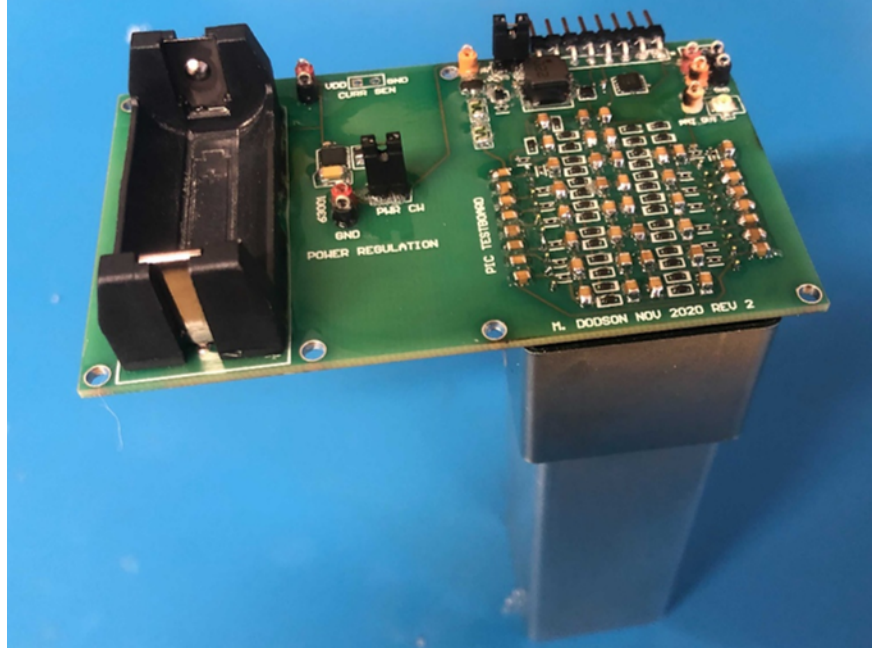


Figure 5.1: The simplified single board design on top of the CsI(Na) 1 inch x 1 inch x 3 inch PMT base.

This design incorporated aspects from the iteration tests such as the feedback design from the ATTINY85 board, and charge pump design using the PIC microcontroller. The PCB in Altium Designer can be seen in Figure 5.2. Full schematic and bill of materials for this design can also be found in Appendix A.

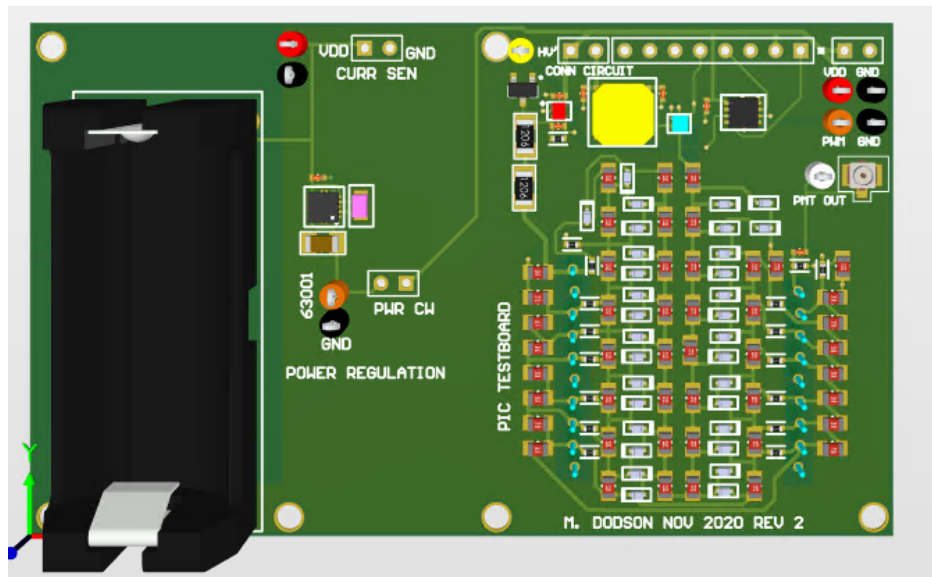


Figure 5.2: The simplified single board design as seen through Altium Designer².

Breaking down the circuit, seen in Figure 5.3, the groups were as follows: the power regulation circuitry, the amplifier, and microcontroller pulse processing circuitry. This was slightly adjusted to accommodate the 0 V to 3.3 V input to the PIC microcontroller to allow full range at -1000 V by using a $2.4\text{ M}\Omega$ resistor in the feedback of the amplifier rather than the $3.4\text{ M}\Omega$ for the 5 V as with the ATTINY85. The MOSFET and inductor configuration was similar to that used for the in the two-board stack. The same was true for the Cockcroft-Walton design. Finally, the preamplifier and shaping amplifier have been removed.

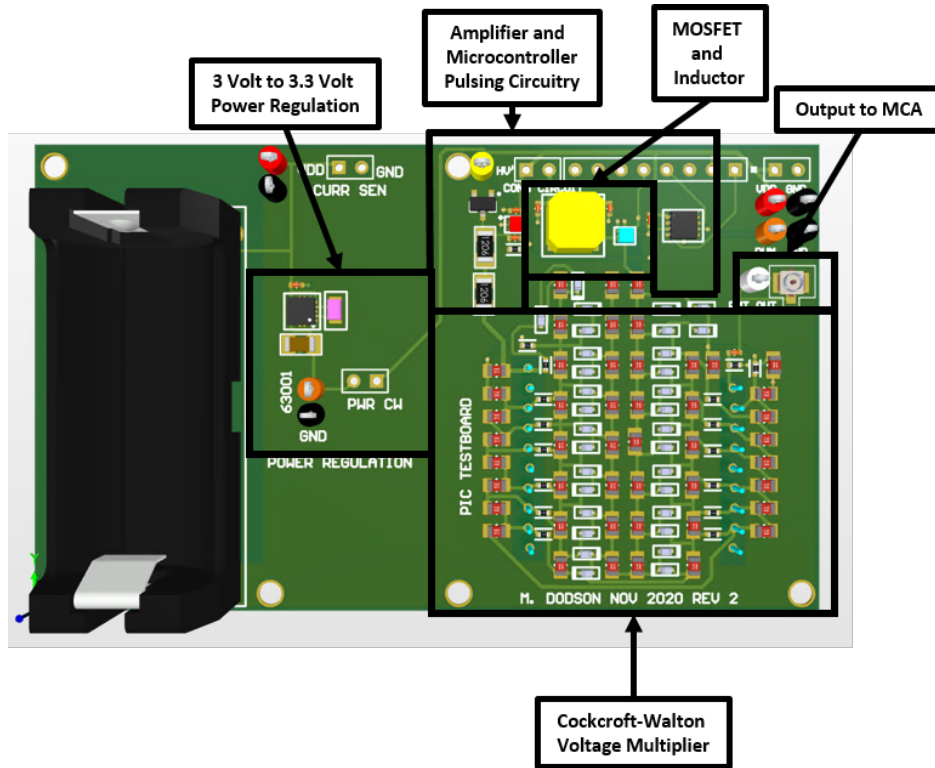


Figure 5.3: A breakdown of the component groups for the single board stack.

The design includes test points that will not be in the 3D design to allow for debugging and verification. Additionally, the circuit has a series of jumpers that allowed isolation of the power regulation circuitry and the microcontroller from the Cockcroft-Walton ladder. These jumpers will not be integrated into the 3D design. Finally, the voltage protection diode was on the input of the feedback amplifier. This voltage protection diode will not be into the final 3D design. Adding in the preamplifier and shaping amplifier circuitry from before, this would bring the total component count to 137 components.

5.1.1 Additional Circuit Changes

MOSFET

To reduce size, a smaller MOSFET was selected for the charge pump design. The MOSFET was selected based on successful use in other projects, as well as, operation characteristics and breakdown voltage. The new MOSFET was the Vishay SiB452DK an N-Channel MOSFET with breakdown voltage of 190 V, which allowed current of 1.5 A, and minimum switching voltage of 2.6 V⁷⁰. The package size for this MOSFET was 1.6 mm by 1.6 mm by 0.75 mm⁷⁰. This change reduced the MOSFET volume by 94% compared to the MOSFET on the two-board design.

Feedback Control Algorithm

In addition to a slow start algorithm, a feedback algorithm was necessary to adjust the duty cycle of the PWM. This was necessary to change the amount of charge released into the Cockcroft-Walton ladder. This algorithm must control the circuit by turning off the PWM to avoid overcharging. For this, a Proportional, Integral and Derivative (PID) controller was implemented. The PID allowed live adjust to the PWM based on a software setpoint. This controlling algorithm was selected because the PID is found in 97% of industry controllers⁷¹. Adjustment of the values needed for the controller were found experimentally⁷¹. The algorithm takes on the form as shown in Figure 5.4, and the PID equation is found in Equation 5.1.

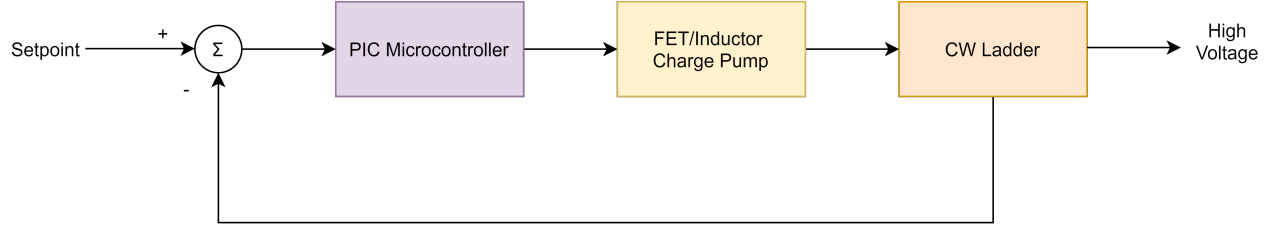


Figure 5.4: A block diagram of how the PID controller was used for the feedback control algorithm.

In practice, the PID controller takes on the following mathematical form:

$$PID = K_p E(t) + K_I \int E(t) + K_D \frac{dE}{dt} \quad (5.1)$$

where E is the error term between the current value of the system and the set point, K_P is the proportional gain, K_I is the integral gain, and K_D is the derivative gain term.

The K_P of the PID is able to tune the system to get the gain to a desired setpoint and eradicate steady-state errors, the K_I is proportional to the magnitude and duration of the error term, and the K_D is used to process the error in respect to time by changing the differential slope of the signal⁷². When properly tuned, the controller can be able to achieve desired effect.

Feedback Control Algorithm Implementation on PIC Microcontroller

For this system, the setpoint was the value for which we wanted the feedback term to be from 0 V to 3.3 V as a function of ADC 10-bits (1024 decimal). For example, if the desired voltage was -800 V at the final stage of the Cockcroft-Walton ladder, the desired value would be multiplied by the voltage gain of the feedback loop -3 mV/V. Then, the resultant, 2.4 V is the voltage expected at the input of the PIC microcontroller ADC. Due to linearity, the voltage from the voltage divider feedback loop can be expressed as a ratio to 3.3 V, multiplied by the decimal representation 1023. This results in a value of 744 as the setpoint for the -800 V output.

Due to limitations with the microcontroller only being capable of integer mathematics, the K_P , K_I , and K_D values were selected to be large values. However, the PID was scaled by 100 after being used in the calculations. Through experimental procedure, making K_D term negative removed the error over time and improved results for the high-voltage measurement. This accounted for any overshoot added by the other components. Furthermore, scaling the PID directly to the required output range for the PWM control, rather than scaling to the 10-bit value worked to control the feedback.

The circuit does not immediately implement the PID controller on startup. Rather, the startup algorithm begins varying the duty cycle to a maximum of 50%. The microcontroller is constantly checking to see if the feedback voltage has reached the setpoint. When it becomes 0.5 V from the setpoint, the PID is implemented. The 0.5 V offset value was found experimentally. This delayed to the PID implementation was necessary so that the circuit would not automatically apply a 50% duty cycle on startup and repeat the instantaneous power draw seen on the two-board stack at startup with a 50% duty cycle. The complete algorithm can be found in [Appendix B](#).

Filtering

To reduce adding additional voltage ripple in order to not degrade the signal produced by the PMT, two circuits were explored with the Cockcroft-Walton ladder filtering.

The original circuit, referred to here as the non-constant cutoff filtering configuration, used the same varying values for the filtering resistors as the two-board stack design. This varied the the cutoff frequencies between 160 Hz and 1120 Hz.

The circuit of the Cockcroft-Walton ladder circuit that was called the constant cutoff version was selected to have 150 Hz cutoff frequencies at all of the dynode stage connections. This was selected with the thought that filtering more extensively at all stages would reduce the ripple. The schematic can be seen in [Figure 5.5](#).

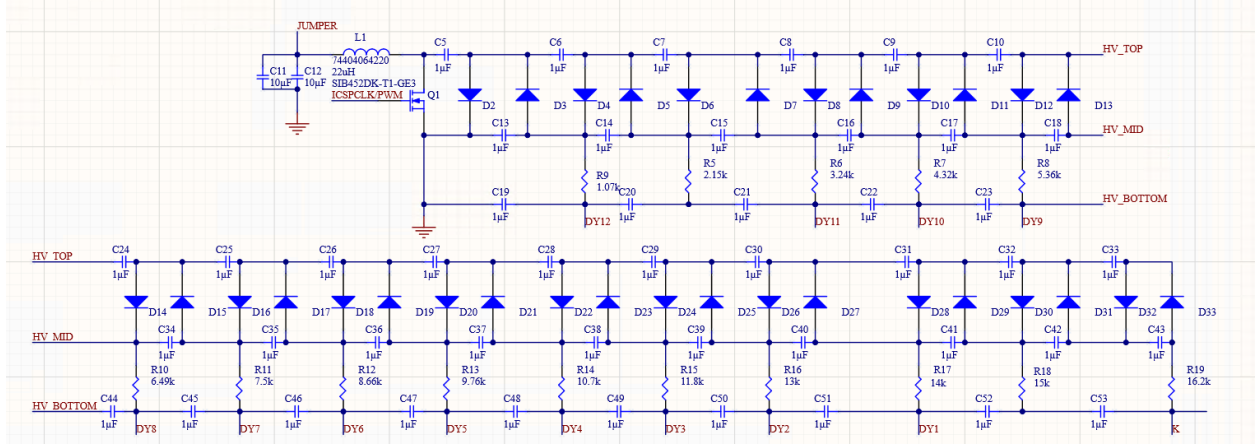


Figure 5.5: The schematic that created the 150 Hz cutoff frequencies for the Cockcroft-Walton ladder.

DC Block Capacitor

On the constant cutoff version, the 2.2 nF DC blocking capacitor on the output of the PMT signal was removed and jumped with solder. This was done due to the fact that during testing the capacitor was causing unwanted interactions with the external preamplifier capacitance.

5.2 Testing Results

Both circuits, the non-constant cutoff and the constant cutoff circuit, were explored during testing to see if there was any increase in energy resolution for the PMT or any major differences in the results.

5.2.1 Power Consumption

The power consumption for the single board stack was examined using the DMM. The circuit would charge to the expected potential with a maximum current draw of 130 mA resulting in current consumption on startup of 390 mW, an 89% reduction in power on startup compared to the two-board design. The circuit charged to the maximum potential in 2.5 s to 4 s. This delay was caused by the startup algorithm needing delay to allow signal to propagate through the circuit. An example of a charging event was recorded for -650 V output as seen in Figure

5.6.

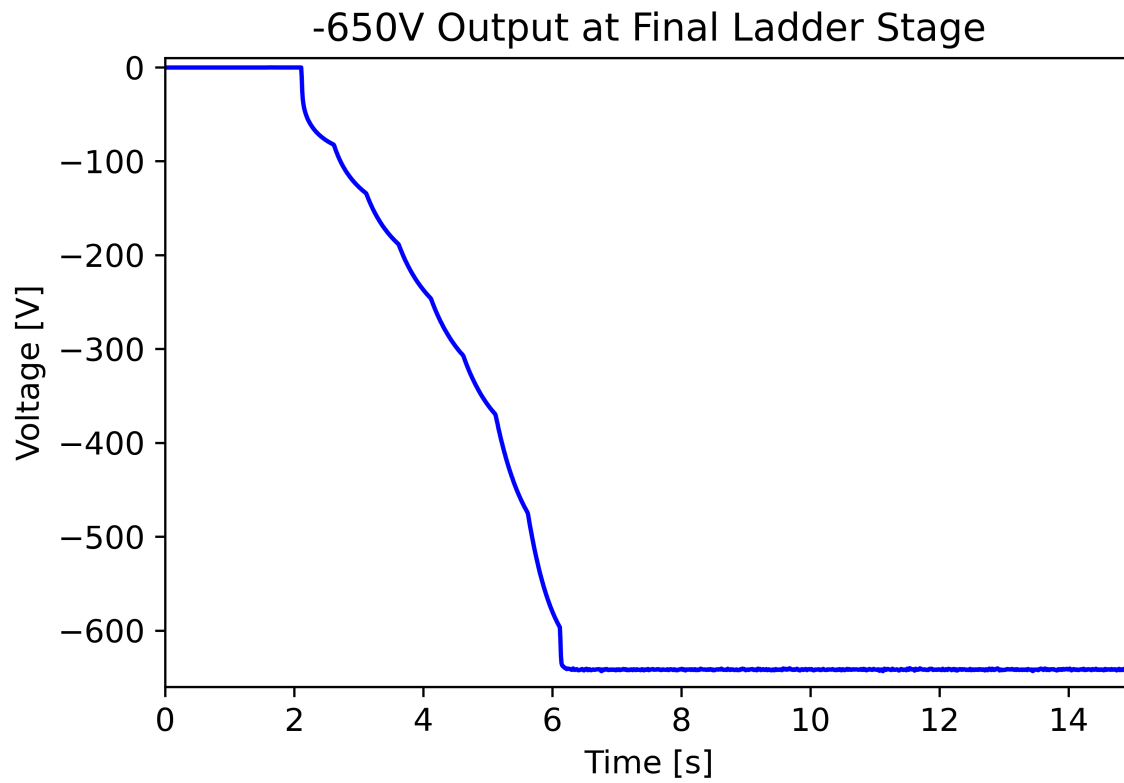


Figure 5.6: The output of the circuit as seen through the DMM charged to -700 V in around 2.5 s .

Using the removable jumpers, the power consumption was investigated for subsections of the circuit. The power regulation circuitry and PIC microcontroller consumed 15 mW of power, 5 mA at 3 V. The PIC microcontroller and high-voltage Cockcroft-Walton ladder consumed 6.9 mW of power, 2.1 mA at 3.3 V. The full system with and without a signal source on the PMT averaged out to consume similar power, 17.7 mW, 5.9 mA at 3 V. The removal of the LED indication circuit reduced the overall power consumption in the design by 59%.

Table 5.1: The power consumption of the different measured segments of the single board design. Most of the power consumption is a result of the power regulation.

	Current (mA)	Input Voltage (V)	Power (mW)
Power Reg, Microcontroller	5	3	15
Microcontroller, High-Voltage	2.1	3.3	6.9
On PMT, no source	5.9	3	17.7
On PMT ^{137}Cs 10 μCi	5.9	3	17.7

Control Instability Voltage Measurement

Both circuits were investigated for the constant and non-constant cutoff circuit through the 2.2 nF capacitor as with the two-board design. Investigating the results to see the response of the control system on the non-constant cutoff circuit, it was more noisy on the charging events at a 10 ms interval. These events were confirmed to be caused by the system picking up noise from the inductor, but overall the peak-to-peak voltage measurement was reduced to 672 mV_{pp} at -650 V. For the constant cutoff circuit, the signal was even more noisy than the non-constant cutoff circuit, picking up both events from the inductor ringing during discharge as well as generic 'white noise' from the atmosphere. Overall the peak-to-peak voltage was reduced to 246 mV_{pp} at -650 V as shown in Figure 5.7. The signals for the non-constant cutoff and constant cutoff circuits can be found in Figure 5.7.

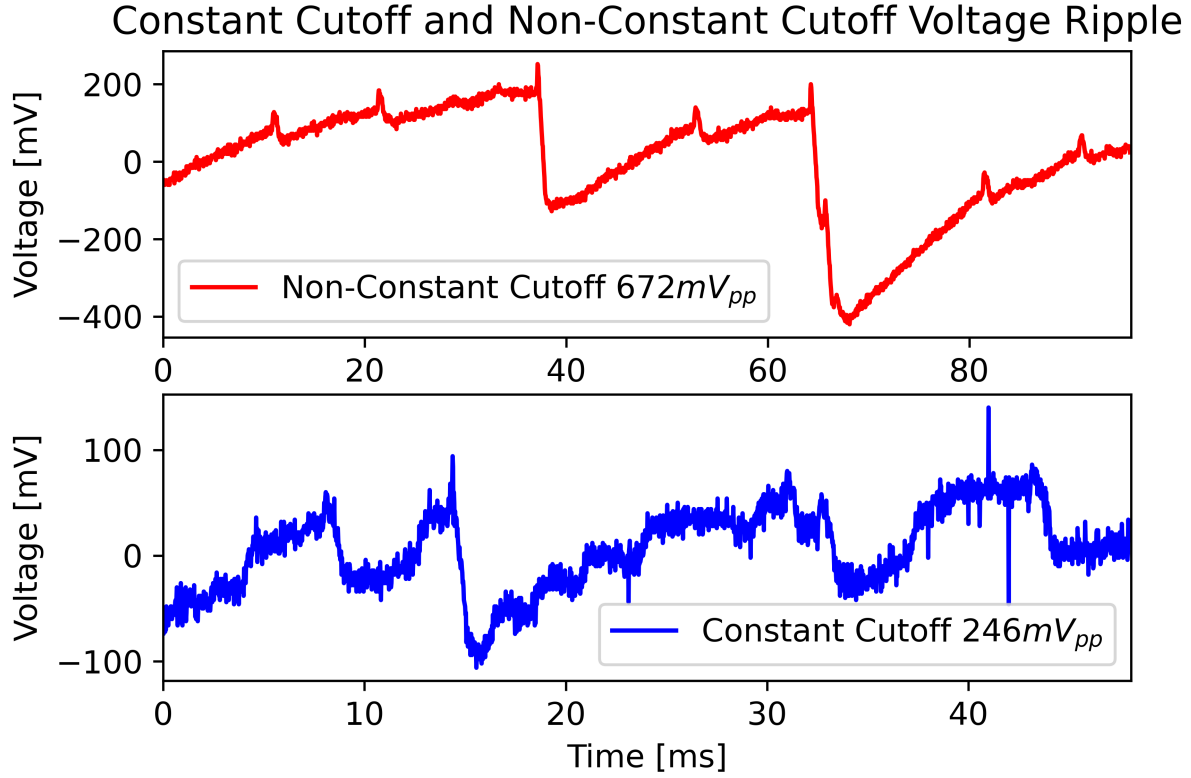
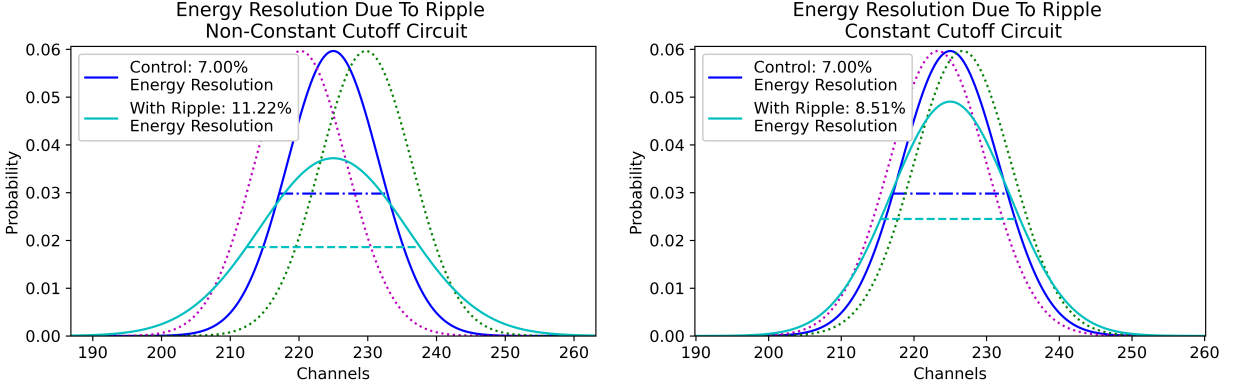


Figure 5.7: Output voltage measurement for a -650 V output with the non-constant cutoff and constant cutoff Cockcroft-Walton circuit as seen through a 2.2 nF capacitor.

For the non-constant cutoff circuit this peak-to-peak voltage created a 0.92% variance of the PMT gain, which correlates to 9.5 channels at FWHM making a projected energy resolution of 7% increase to an energy resolution of 11.22% . Therefore, this configuration may not improve the energy resolution of the detector. For the constant cutoff circuit the peak-to-peak voltage created a 0.33% variance in the PMT gain, which correlates to 3.4 channels at FWHM making a projected energy resolution of 7% increase to 8.51% . Therefore, this configuration should improve the energy resolution of the detector. The energy resolution increase to a Gaussian pulse for both circuits can be found in Figure 5.8.



(a) Non-constant cutoff board peak-to-peak voltage effect
(b) Constant cutoff board peak-to-peak voltage effect

Figure 5.8: A Gaussian signal response and energy resolution effect due to voltage fluctuation on the PMT base for both the non-constant and constant cutoff circuits.

5.2.2 Radiation Spectroscopy

The operating voltage was investigated for -650 V and -700 V to try to ensure the full 3 MeV range was covered for both the non-constant and constant cutoff circuits. These voltage ranges were selected as previous operating conditions at -735 V was too much gain to encapsulate the 3 MeV range. To provide a baseline of operation and energy resolution to compare the constant and non-constant circuit to the manufacturer, the Hamamatsu manufactured PMT base was first tested.

The Hamamatsu manufactured PMT base was tested for -650 V and -700 V using the Caen DT8033 high-voltage power supply an manufacturer base^{1;58}. The Ametek Ortec preamplifier 113 with 500 pF input capacitance was used, and then the Ametek Ortec 571 amplifier was used to shape the pulse to a Gaussian shape^{56;57}. The ^{137}Cs $10\text{ }\mu\text{Ci}$ check source was used for calibration. The Ortec 927 MCA was used for data collection, and the gain on the amplifier was increased until the ^{137}Cs peak was seen in Ortec Maestro at channel 225 out of 1023, the channel that would correlate for a full 3 MeV spectrum^{52;53}. To avoid any additional drift or baseline shift with the Hamamatsu base, a $100\text{ k}\Omega$ terminator was placed on the output of the signal. With the voltage running at -650 V , the energy resolution at ^{137}Cs was 7.5% and with the voltage at -700 V was 7.3% .

The non-constant cutoff board was configured for -650 V . Since this circuitry did not have the preamplifier and amplifier on it, the Ametek Ortec preamplifier 113 was configured for 200 pF input. The results of the non-constant cutoff board signal resulted in a rise time of $3.1\text{ }\mu\text{s}$ and decay time of $37.4\text{ }\mu\text{s}$. The constant cutoff board signal resulted in a rise time of $2.3\text{ }\mu\text{s}$ and $30.5\text{ }\mu\text{s}$ decay time. Ideally the decay time from the preamplifier should be $50\text{ }\mu\text{s}$, but due to limitations with the preamplifier only having select few input capacitance values, this was unobtainable²⁵. Furthermore, the 2.2 nF capacitor on the PMT output was removed to avoid having impact on the preamplifier. The signals can be found in Figure 5.9.

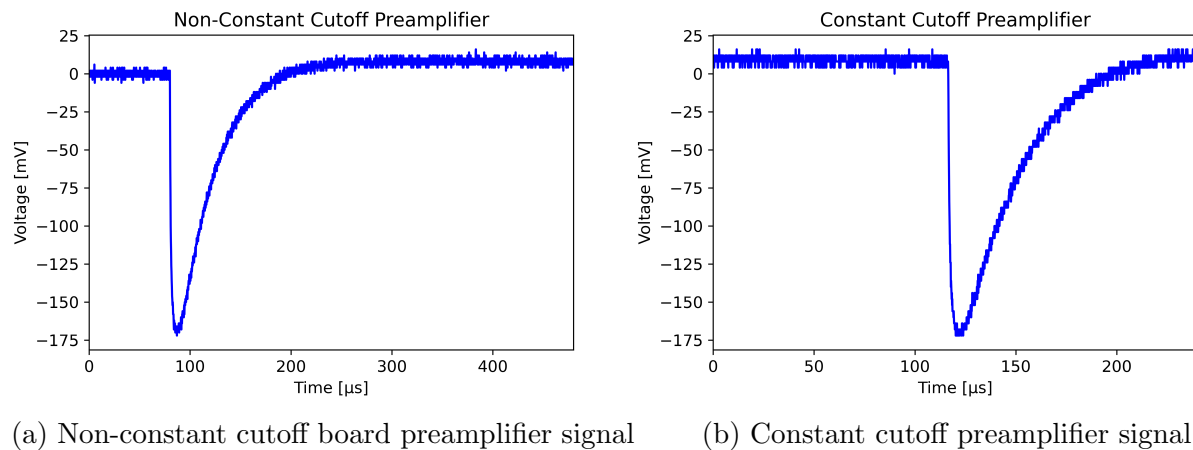


Figure 5.9: The preamplifier signals from the single board stack for both the non-constant cutoff version, Figure 5.9a, and the constant cutoff version 5.9b.

The preamplifier signal was then sent through the Ortec amplifier 571 and the signal was adjusted. The gain on the signal was turned all the way down. The NIM equipment was configured for a $3\text{ }\mu\text{s}$ shaping time for the non-constant cutoff circuit, and the constant cutoff circuit was configured for $0.5\text{ }\mu\text{s}$ shaping time. This was done to get a Gaussian shaped pulse and have minimal overshoot. Course gain for both was selected to avoid adding much gain to the signal. It was noted that the max of both signals with the ^{137}Cs check source was almost 2.5 V and the maximum input to the MCA was 3.3 V , so increased count rates could have the potential to rail the input to the MCA. Furthermore, the constant cutoff board was having a slight overshoot. This was unavoidable due to the NIM equipment limitations. The pulses are represented in Figure 5.10, where the non-constant cutoff version has a rise time

of $3.5\ \mu\text{s}$ with $3.88\ \mu\text{s}$ decay time, and the constant cutoff version has a rise time of $4.8\ \mu\text{s}$ and decay time of $5.7\ \mu\text{s}$.

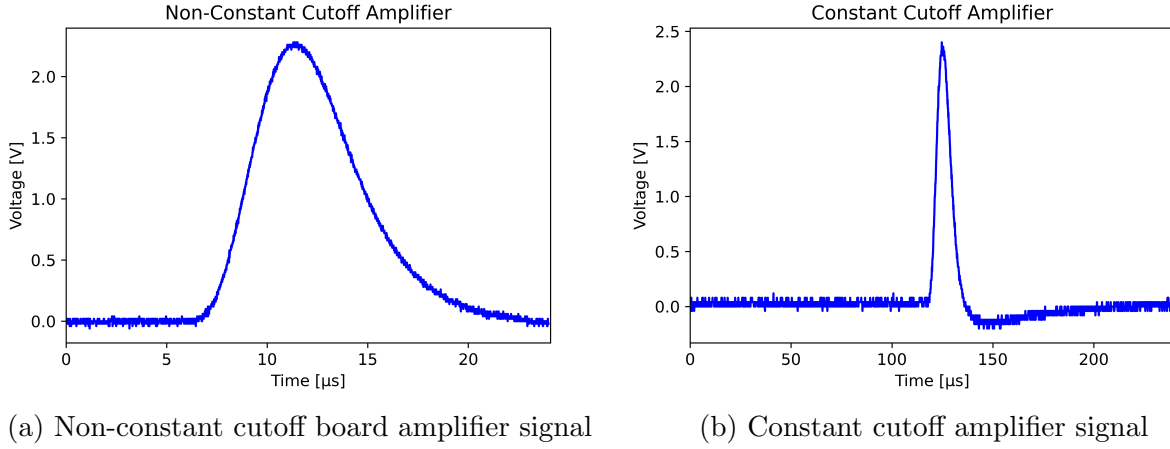


Figure 5.10: The amplifier signals from the single board stack for both the non-constant cutoff version, Figure 5.10a, and the constant cutoff version 5.10b

The spectra for the constant cutoff and non-constant cutoff base operating at $-650\ \text{V}$ is presented in Figure 5.11. The non-constant cutoff board had a count rate of 369cps and ^{137}Cs with energy resolution of 8.3% and the constant cutoff base had a count rate of 347cps and ^{137}Cs with energy resolution 7.8% when the $10\ \mu\text{Ci}$ check source was 8 inches from the side of the PMT. A differentiation is seen in the Compton continuum (32 keV to 0.5 keV), potentially due a difference in source location.

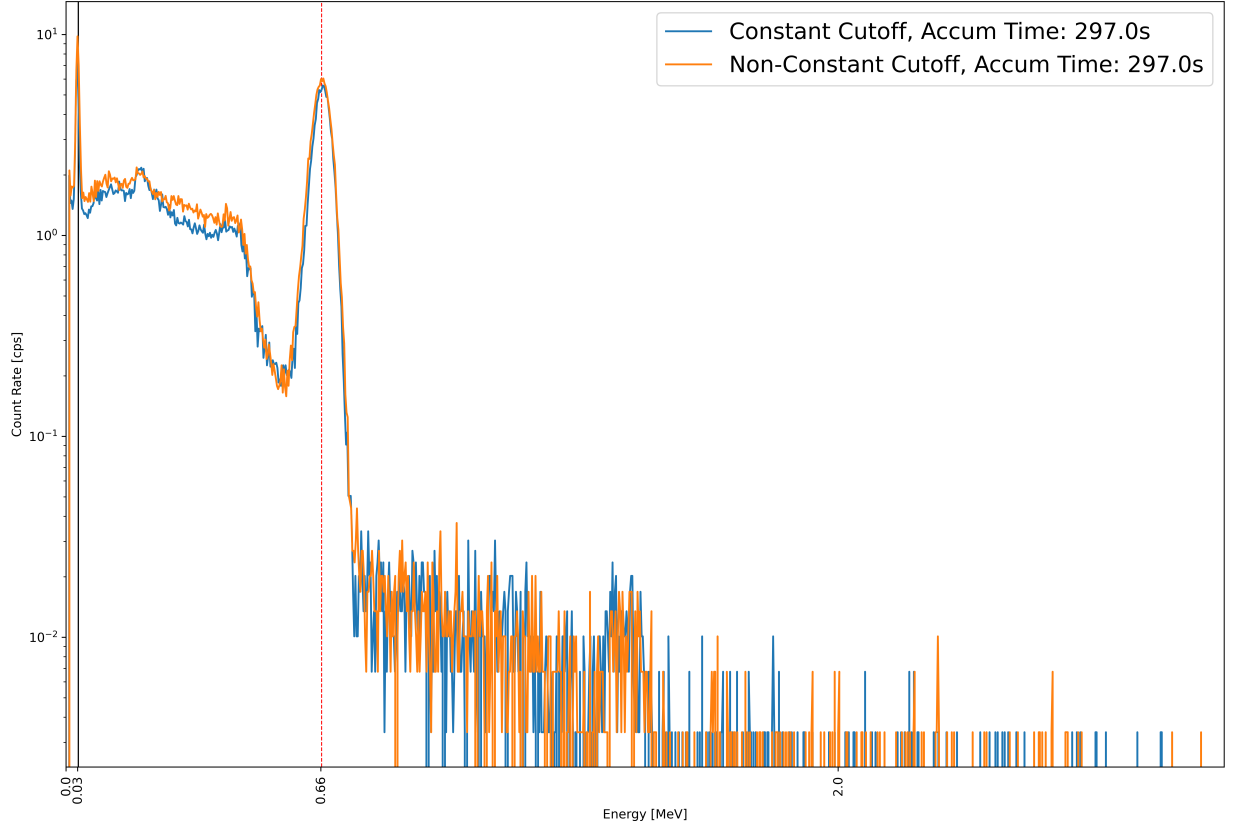


Figure 5.11: The comparison measurement for a -650 V output with the constant cutoff and non-constant cutoff Cockcroft-Walton circuit.

5.2.3 Power Consumption Vs Count Rate

Low Count Rate

Similar to the two-board setup, the single-board stack was tested by moving the check source from 20 inches to 2 inches. The current consumption was measured by the DMM. To verify the count rates accuracy, a $(distance^{2-1})$ approximation was plotted as a function of the distance from the broad side of the detector. This can be seen in Figure 5.12.

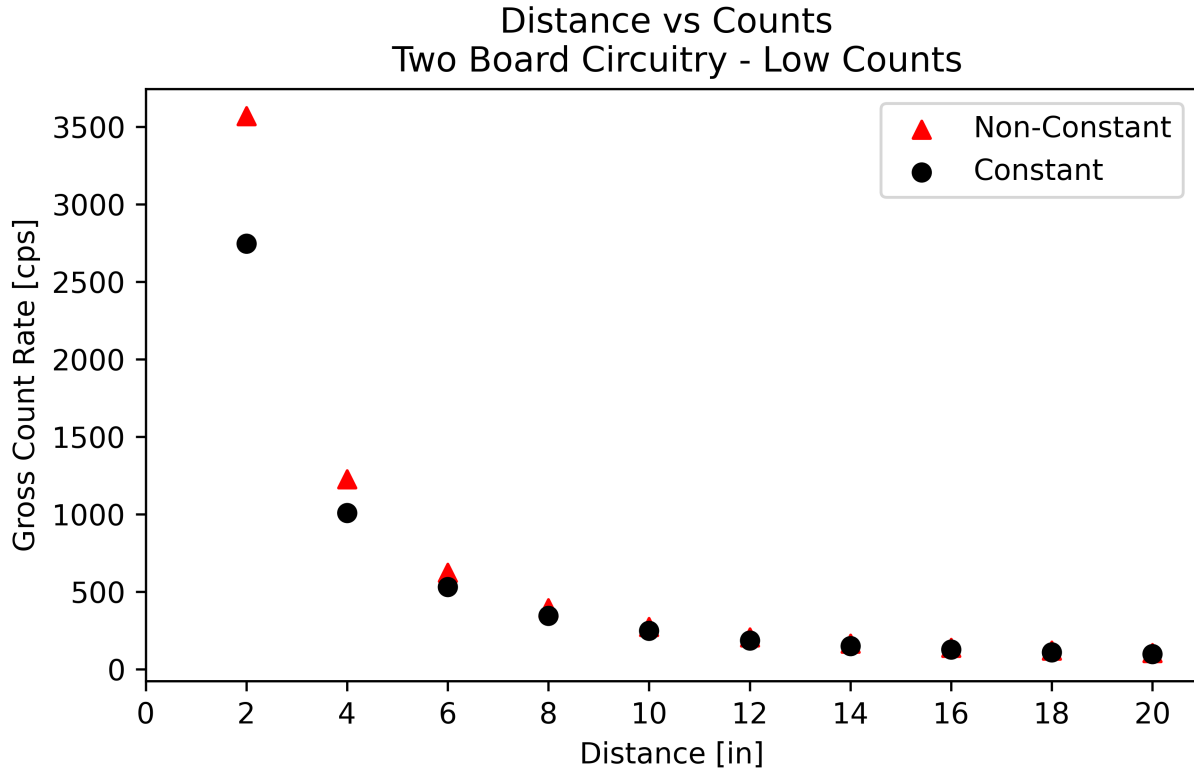


Figure 5.12: Verification of measurement for both the constant and non-constant cutoff circuit by plotting the distance versus the count rates observed.

The power consumption as a function of count rate was plotted using the average of 5 min data acquisitions. As with the two-board stack, the data was fit with a linear fit approximation, and error uncertainty was calculated using Equation 4.4. The power consumption for the non-constant cutoff board created an average of 17.6 mW with an uncertainty of 7.9 μ W for low count rates. The constant cutoff version, however, had a power consumption with an average value of 19.4 mW with uncertainty of 6.2 μ W for low count rates. The linear fit approximation was believed to not be a good fit for the non-constant cutoff due to the low correlation coefficient, believed to be caused by the single outlier in the data set at the lowest sample. It was believed that the power consumption difference between the two configurations was due to the microcontroller and PID requiring more current, and error induced in all components during the construction of the circuit. This is represented in Figure 5.13.

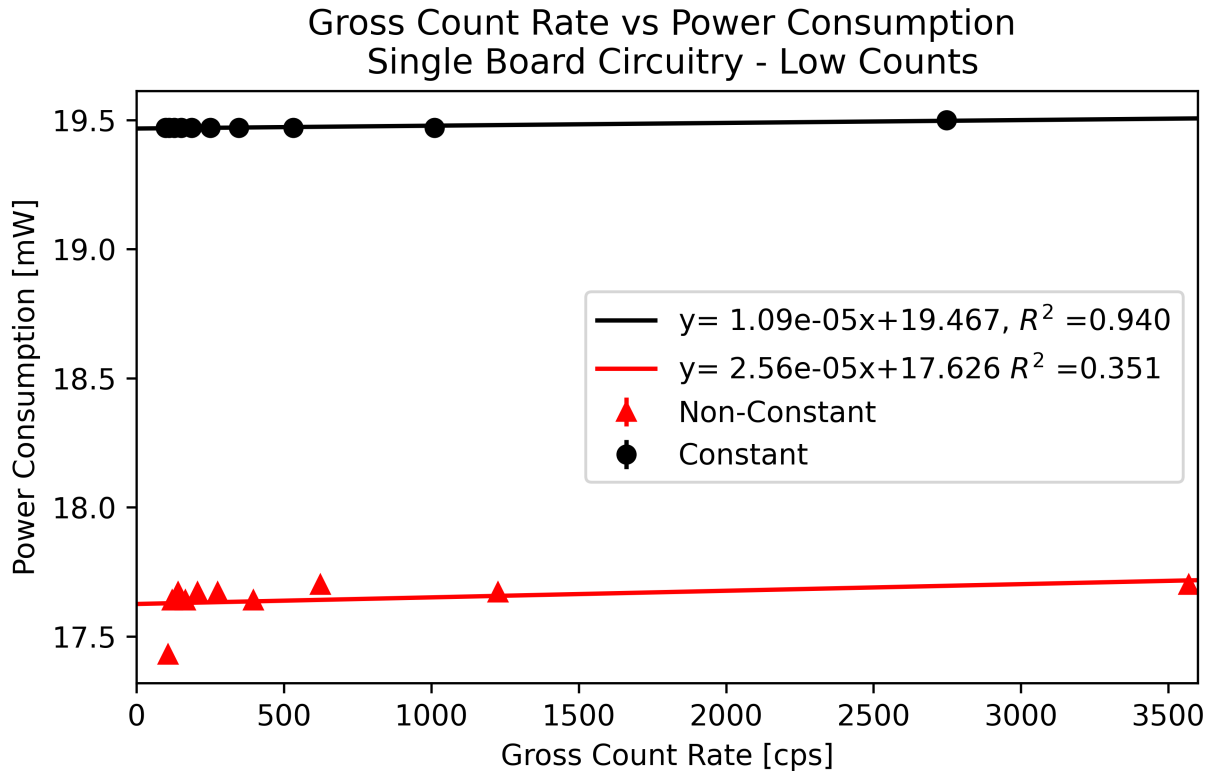


Figure 5.13: The comparison between the count rate and power consumption for a -650 V output with the constant cutoff and non-constant cutoff Cockcroft-Walton circuit for low count rates.

High Count Rate

Similar to the two-board stack circuitry, both the constant and non-constant cutoff circuits were tested with a variety of check sources placed touching the broad side of the detector while the current was monitored through the DMM. The tests can be found in Table 5.2.

Table 5.2: Check source setup for each test to achieve elevated count rates with the single circuits.

Check Source	Test							
	1	2	3	4	5	6	7	8
^{133}Ba 1 μCi	X	X	X	X	X	X	X	
^{109}Cd 1 μCi	X	X	X	X	X	X	X	X
^{137}Cs 0.25 μCi	X	X	X	X	X	X	X	X
^{57}Co 1 μCi	X	X						
^{60}Co 1 μCi	X	X	X	X				
^{54}Mn 1 μCi	X	X	X	X	X	X		
^{22}Na 1 μCi	X	X	X	X	X			
^{65}Zn 1 μCi	X							
^{152}Eu 1 μCi	X	X	X					

The power consumption as a function of count rate was plotted using the average of 5 min data acquisitions. As with the two-board stack, the data was fit with a linear fit approximation, and error uncertainty was calculated using Equation 4.4. The power consumption for the non-constant cutoff board created an average of 18.8 mW with an uncertainty of 54.2 μW for low count rates. The constant cutoff version, however, had a power consumption with an average value of 20.3 mW with uncertainty of 40.4 μW for low count rates. Between the low and high count rate tests, the non-constant cutoff board average power consumption increased by 6.8% while the constant cutoff circuit power consumption increased by 4.6%, a drastic improvement over the two-board design. It was believed that the power consumption difference between the constant and non-constant cutoff board was due to the microcontroller and PID requiring more current, and error induced in all components during the construction of the circuit. It is expected that the trend for each data set begin to level out upon reaching a certain count rate, although that value is currently unknown. This is represented

in Figure 5.14.

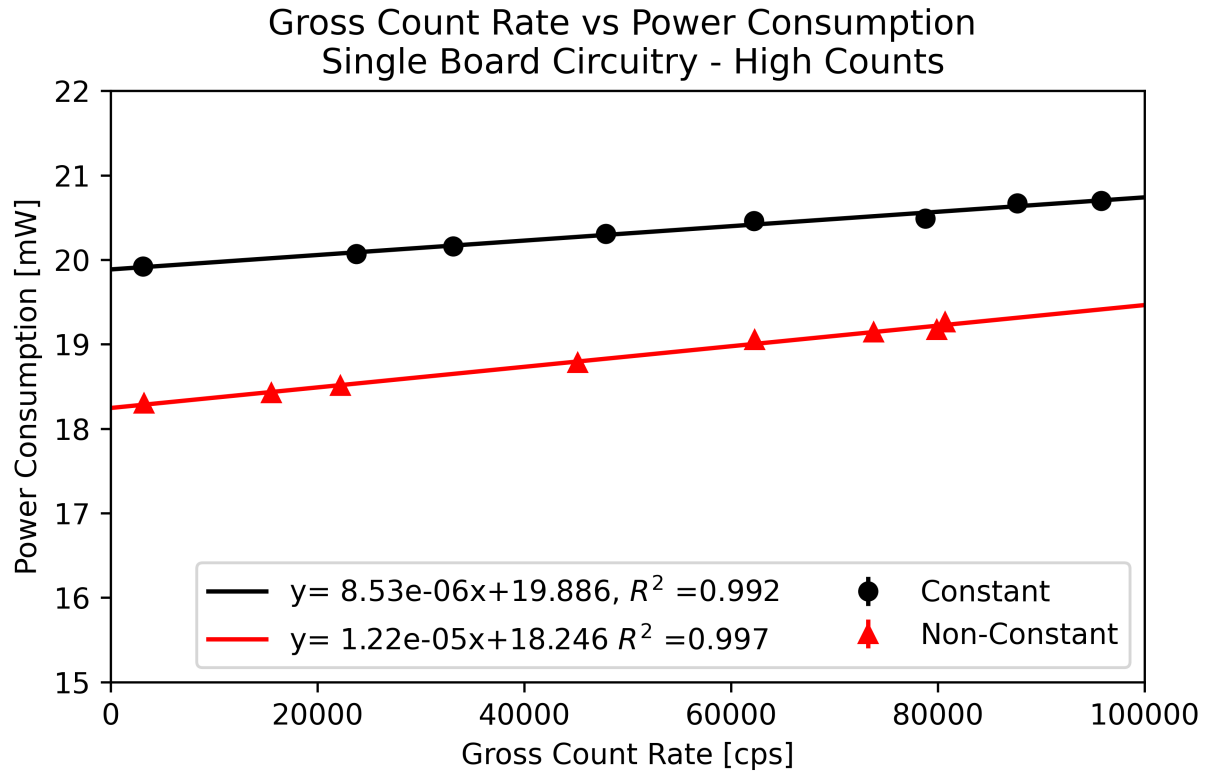


Figure 5.14: The comparison between the count rate and power consumption for a -650 V output with the constant cutoff and non-constant cutoff Cockcroft-Walton circuit for high count rates.

5.2.4 Battery Life

Using a similar setup to measure the battery level using the Raspberry Pi, the battery level was measured with the single board design on the PMT. The battery was able to discharge from 3.2 V to 2.8 V after 6 d, 6 h. Removing the LED indication and additional circuitry made the battery life of the circuit increase by 124% compared to the two-board design.

5.2.5 Power Consumption by Simplification

This comparison between the two-board stack and the single board design was key to understand how much the LED was depreciating battery life. Main comparison between the two-board design and the constant and non-constant cutoff would result in direct comparison between the high-voltage Cockcroft-Walton ladder supply. These values would best be compared through the high-voltage ladder and high-voltage regulation measurement for the two-board stack with power consumption of 7.5 mW and the microcontroller and high-voltage ladder for the single board at 6.9 mW. Simplifying the design to represent the ladder and the control of the charging aspect to the microcontroller ultimately reduces the power consumption by 8%.

Chapter 6

Lessons Learned, Discussion & Future Plans

Through these tests, the single board constant cutoff design implementation provided best performance. Compared to the two-board design, the single board constant cutoff circuit offered improved operation. The two-board design excluding peripheral connectors had a total component count of 166 components. The single board constant cutoff design had a total component count of 137 components, a 17% decrease in the number of components. Note that this value includes the preamplifier and shaping amplifier design, an additional 27 components, presented on the two-board design but not implemented in the single board circuit. Additionally, components for operation were swapped for smaller variants to reduce the volumetric size of components that need to be embedded into the 3D design.

Overall, the component count was reduced from the two-board design to the single board constant cutoff design for each category. The power regulation circuitry was reduced from 13 components down to 4 components by the introduction of the linear regulator. The front-end circuitry used to regulate the Cockcroft-Walton ladder was reduced from 29 components to 9 components through the implementation of the microcontroller and amplifier feedback control. Both of these reductions equal to a reduction of 69%. The Cockcroft-Walton

ladder itself was reduced from 103 components to 98 components by the removal of extra capacitors that were implemented on the two-board design to assist in the initial charging of the inductor due to the unknown current surge. These capacitors were no longer necessary due the slow-start algorithm varying the startup duty cycle.

Looking at the PMT signal metrics, the two-board stack design only had 8.5% resolution efficiency, while the constant cutoff single board design had an energy resolution of 7.8%. Due to the fact that the Hamamatsu engineered base for the Hamamatsu R11265U base had an energy resolution of 7.5%, that was considered the target goal. For the constant cutoff version, this value was only a 0.3% difference in energy resolution compared to the single board design.

The power consumption for the boards decreased between the two-board stack and the single board stack design. Ultimately, this was due to the removal of the LED indication circuitry and the change in the startup. However, the power consumption of the two-board stack to the single board design was ultimately decreased by almost 58% by moving to the single board design. This allowed for the circuit operation to last over twice the amount of time on a single CR123A battery. This is crucial to the 3D design becoming a standalone and portable radiation detection system. Comparing the high-voltage Cockcroft-Walton ladder operation individually, the design was able to achieve power consumption reduction of 8%, 7.5 mW to 6.9 mW.

6.1 Lessons Learned

For Altium, the library management was one of the greatest issues. Other PCB design suites have the schematic version and the footprint for the same component in the same folder structure. Altium Designer had a handful of file and folder structures in which everything had to be organized and where the components to use and the project files would not be directly integrated into one sub-directory. Having multiple files and folders scattered

across multiple directories caused confusion when passing the design around. To avoid any confusion, a single folder on the private server structure for the project was created. It was then setup to where the Altium software was pointed towards this folder to use for everyone involved on the project. This avoided keeping anyone that needed to view the design from having any outdated versions.

In fabrication, a challenge was with the components that were intended to be placed on a PCB via a pick-and-place machine rather than by hand. Since the design required such a small quantity of boards to be manufactured, they were all hand soldered. Without a pick-and-place machine, the best approach was the use of solder paste, a heat gun, and a curing oven to cure the solder paste. This took considerable care and precision with some of the components, especially those placed on the single board design.

From a coding algorithm standpoint, the Atmel ATTINY10 and ATTINY85 microcontrollers required more code to setup the microcontroller parameters, in comparison to the PIC microcontroller due to its graphical user interface (GUI) that allowed for selection of settings. The GUI allowed the selection of various chip settings, which would then generate the header files containing basic functions for the code. This had advantages and disadvantages. The original intention for the value read into the ADC was to implement an interrupt service routine, so that the ADC value would only trigger the PID on a signal change. This was assumed to reduce the power consumption used by the algorithm. A through-hole variant of the PIC microcontroller first to test the validity of the microcontroller. Issues getting the ADC to fire once the value changed by simply sending step impulses was one of the first tasks undertaken after completing the rewriting of the startup algorithm. However, after tedious debugging, it was discovered that the GUI generated header files did not implement the interrupt service routine as instructed via the manual. This was then fixed.

Another issue was noise picked up in the feedback circuitry caused by ringing of the inductor on the PCB board. This was due to the inductor switching and physically located close to

feedback circuitry. Although the inductor is marketed as shielded, it does not guarantee that all electric field is prevented from escaping and coupling to nearby components. To reduce this ringing, it is recommended that the inductor include additional shielding and the analog feedback circuitry be placed at a reasonable distance away.

From a testing standpoint, there were multiple mishaps that occurred when trying to verify signals on the Cockcroft-Walton high-voltage ladder that resulted in failures such as arcing, reaching the bench top power supply's current limit. All signals that needed to be investigated would be probed and connected to the measurement equipment prior to there being any power applied to the circuit. There exist mini grabber test probes that allow for small components to be clipped onto first, before being broken out to the measurement equipment. It is recommended these test probes be used.

6.2 Future Work

Currently, all 3D builds are being outsourced to other sources that have the capability to use the nScript 3D printer. An nScript machine has been ordered and is scheduled to be delivered in late May 2021.

Sub assembly builds are in the process of being constructed on a nScript 3D printer to verify the 3D implementation. One group is currently printing 6 of the 12 stages of the Cockcroft-Walton ladder design, while the other group is currently printing the microcontroller, feedback circuit (with a slight gain modification to allow for the a smaller input voltage that could be achieved through a bench top power supply) and the charge pump circuitry.

In terms of circuit improvement, it is recommended that the gain stage ratios be reevaluated to enhance the energy resolution, primarily the gain stage attached to the first stage of the dynode. Increasing this ratio would require additional components and a rework of the Cockcroft-Walton ladder, but would improve the energy resolution of the detection system.

Certainly, alterations to the circuitry or further improvements may be made, primarily to the control algorithm to optimize the PID. It is recommended that the PID control undergo a detailed control theory analysis to result in a full transfer function to optimize the PID gain values. Once this is completed, it is recommended to prospect other microcontrollers that have PWM and built in ADC functionality with the ability to implement floating point mathematics to allow finer gain control in the PID algorithm.

It is recommended to validate basic circuit functionality for the 3D configuration using the approaches as presented herein. It is also advised to investigate the lower dynode stage readouts with the 3D design to characterize the operation dynamic range⁷³⁻⁷⁵. This would require characterizing performance of the dynode stages with LED and cosmic rays^{73;74}.

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Appendix A

Reference Materials

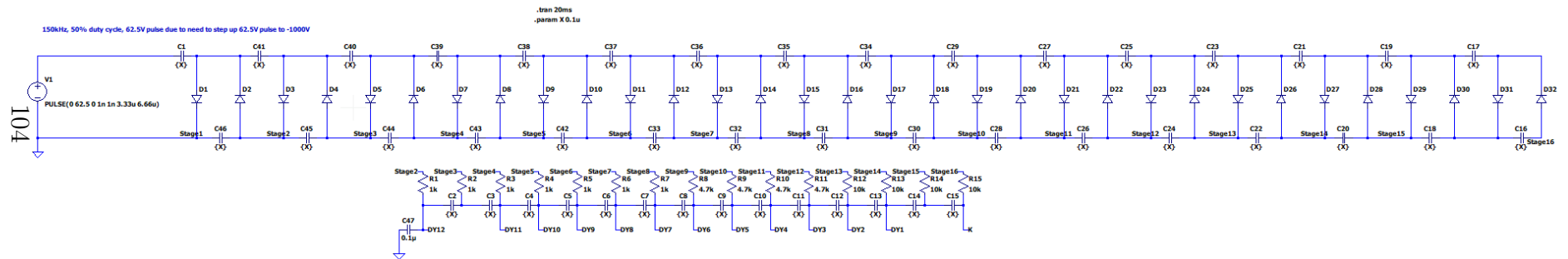
The LTSpice simulation configurations can be found for the following:

1. Half-Wave Cockcroft-Walton
2. Full-Wave Cockcroft-Walton

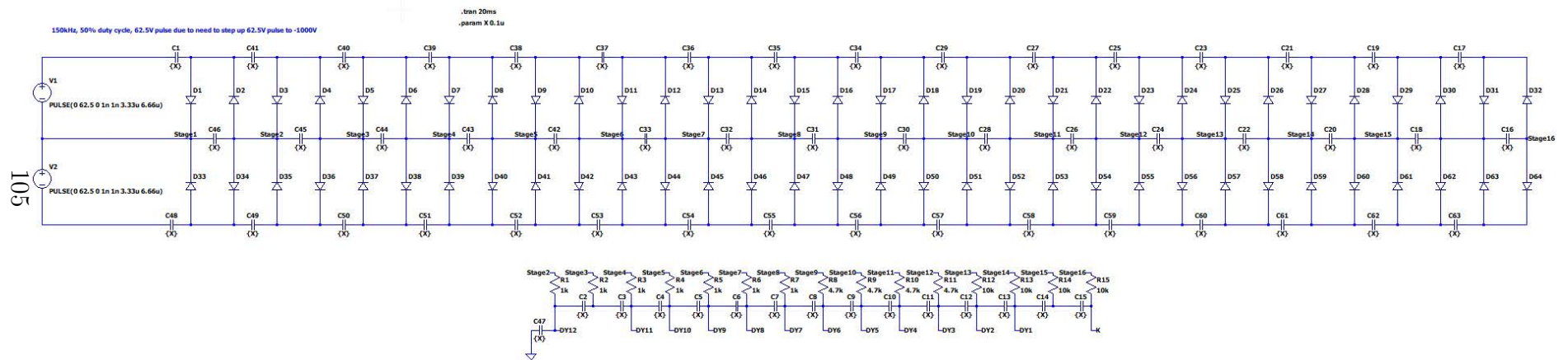
The reference schematics and bill of materials (BOM) can be found for the following:

1. Two-Board Stack - High-Voltage Board Schematic and BOM
2. Two-Board Stack - High-Voltage Control Board Schematic and BOM
3. ATTINY85 Test Article Schematic and BOM
4. Finalized Design Variant - Not Optimized Filtering and BOM
5. Finalized Design Variant - Optimized Filtering and BOM

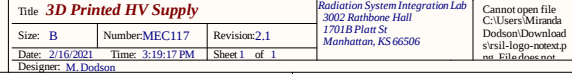
A.1 Half-Wave Cockcroft-Walton - LTSpice



A.2 Full-Wave Cockcroft-Walton - LTSpice



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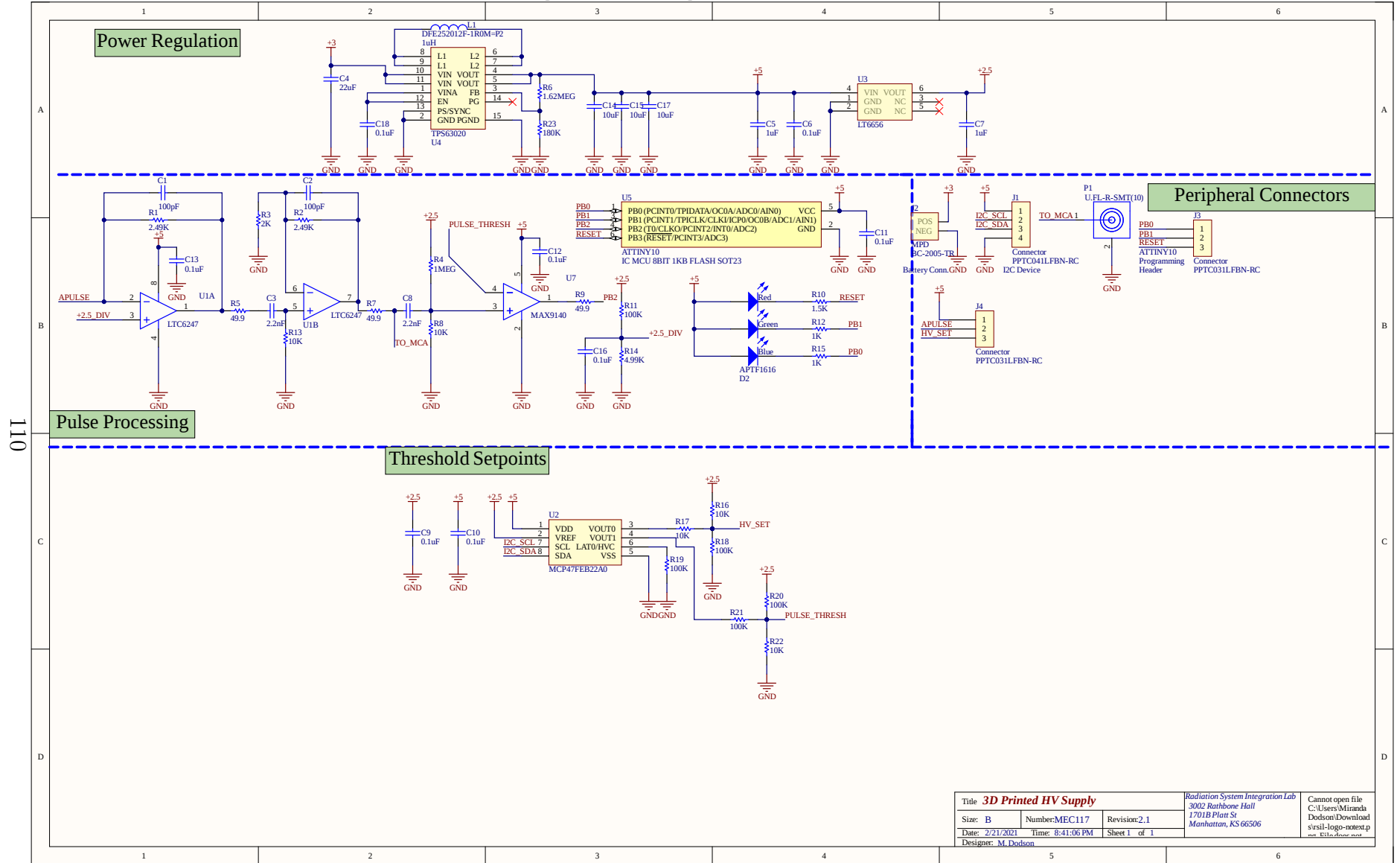


Name	Description	Designator	Quantity	Manufacturer	Part Number
CAP CER 0.1UF 25V X5R 0402	Capacitor 0.1uF 0402	C1, C2, C12	3	Samsung	CL05A104KA5NNNC
CAP CER 100PF 50V C0G/NPO 0402	Capacitor 100pF 0402	C3	1	Yageo	CC0402JRNPO9BN101
CAP CER 0.1UF 25V X5R 0402	Capacitor 10pF 0402	C4	1	Yageo	CC0402JRNPO9BN100
CAP CER 2200PF 50V X7R 0402	Capacitor 2.2nF 0402	C5	1	Murata	GCM155R71H222KA37D
CAP CER 1UF 100V X7S 0805	Capacitor 1uF 0805	C6-C11, C14-C19, C21-C60	52	TDK	C2012X7S2A105M125AE
Cap 10uF	Capacitor 10uF 0402	C13	1	Samsung	CL05A106MP8NUB8
Diode Standard 100V 200mA (DC)	Diode Standard 100V 200mA (DC) Surface Mount SOT-1123	D1-D33	33	ON Semiconductor	NSD914F3T5G
CONN HDR 3POS 0.1 TIN PCB	CONN HDR 3POS 0.1 TIN PCB	J1	1	Sullins	PPTC031LFBN-RC
22uH	22uH Shielded Wirewound Inductor 1.8A 89mOhm	L1	1	Würth Electronics	74404064220

Name	Description	Designator	Quantity	Manufacturer	Part Number
Pin Receptacle Connector No Tail Press-Fit	PMT Adapter	P1-P19	19	Mill-Max	0462015152127040
SIR882DP-T1- GE3	N-Channel 100V 60A (Tc) 5.4W (Ta), 83W (Tc) Surface Mount SO-8	Q1	1	Vishay Siliconix	SIR882ADPT1GE3
RES SMD 1.2M OHM 5% 1/16W 0402	Resistor 1.2MEG 0402	R1	1	Yageo	RC0402JR071M2L
RES SMD 100K OHM 5% 1/10W 0402	Resistor 100k 0402	R2, R5	2	Panasonic	ERJ2GEJ104X
Res 30k 0402	Resistor 30k 0402	R3	1	Panasonic	ERA-2AEB303X
RES SMD 3.32M OHM 1% 1/16W 0402	Resistor 3.32MEG 0402	R4, R6	2	Vishay	CRCW04023M32FKED
RES SMD 1K OHM 0.5% 1/16W 0402	Resistor 1k 0402	R7-R12, R22	7	Panasonic	ERA-2AED102X
RES SMD 4.7K OHM 0.1% 1/16W 0402	Resistor 4.7k 0402	R13-R16	4	Panasonic	ERA2AEB472X
RES SMD 10K OHM 0.5% 1/16W 0402	Resistor 10k 0402	R17-R19, R23	4	Panasonic	ERA2AED103X

Name	Description	Designator	Quantity	Manufacturer	Part Number
RES SMD 1G OHM 1% 0.3W 1206	Resistor 1G 1206	R20	1	Vishay Dale	CRHV1206AF1G00FKE5
Schmitt Trigger	IC INVERTER SCHMITT 6CH 14TSSOP	U1	1	ON Semiconductor	MC74HC14ADTR2G
IC OPAMP GP 400KHZ RRO 8MSOP	General Purpose Amplifier 2 Circuit Rail-to-Rail 8-MSOP	U2	1	Rochester Electronics	AD8607ARMZREEL
CAP CER 10pF 50V X5R 0402	Capacitor 10pF 0402	C1, C2	2	Yageo	CC0402JRNPO9BN100

A.4 Two-Board Stack - High-Voltage Control Board Schematic and BOM



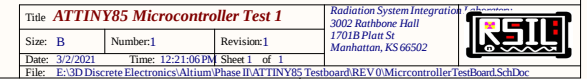
Name	Description	Designator	Quantity	Manufacturer	Part Number
CAP CER 2200PF 50V X7R 0402	Capacitor 2.2nF 0402	C3, C8	2	Murata	GCM155R71H222KA37D
22uF $\pm 20\%$ 10V Ceramic Capacitor X5R 0805 (2012 Metric)	Capacitor 22uF 0805	C4	1	Murata	GRM21BR61A226ME51L
CAP CER 1UF 25V X5R 0402	Capacitor 1uF 0402	C5, C7	2	TDK	CGB2A1X5R1E105K033BC
CAP CER 0.1UF 25V X5R 0402	Capacitor 0.1uF 0402	C6, C9, C10-C13, C16, C18	8	Samsung	CL05A104KA5NNNC
BATT HOLDER CR123A	Battery Holder (Open) CR123A 1 Cell PC Pin	J2	1	Keystone Electronics	1051
CONN HDR 3POS 0.1 TIN PCB	CONN HDR 3POS 0.1 TIN PCB	J3, J4	2	Sullins	PPTC031LFBNRC
Cap 10uF	Capacitor 10uF 0402	C14, C15, C17	3	Samsung	CL05A106MP8NUB8
LED RGB CLEAR 4SMD	LED RGB CLEAR 4SMD	D2	1	Kingbright	APTF1616SEEZGKQBKC
CONN HDR 4POS	CONN HDR 4POS 0.1 TIN PCB	J1	1	Sullins	PPTC041LFBN-RC

Name	Description	Designator	Quantity	Manufacturer	Part Number
Fixed Inductor	FIXED IND 1UH 3.3A 40 MOHM	L1	1	Murata	DFE252012F1R0MP2
CONN U.FL RCPT STR 50 OHM SMD	U.FL (UMCC) Connector Receptacle, Male Pin 50Ohm Surface Mount Solder	P1	1	Hirose	U.FL-R-SMT-1(01)
Res 4.99k 0402	Resistor 4.99k 0402	R1, R2	2	Panasonic	ERA2AEB4991X
RES SMD 2K OHM 0.1% 1/16W 0402	Resistor 2k 0402	R3	1	Yageo	RT0402BRD072KL
RES SMD 1M OHM 1% 1/10W 0402	Resistor 1MEG 0402	R4	1	Vishay Beyschlag	MCS04020C1004FE000
RES SMD 49.9 OHM 0.1% 1/16W 0402	Resistor 49.9 0402	R5, R7, R9	3	Panasonic	ERA2AEB49R9X
RES 1.62M OHM 1% 1/16W 0402	Resistor 1.62MEG 0402	R6	1	Stackpole Electronics	RMCF0402FT1M62
RES SMD 10K OHM 0.5% 1/16W 0402	Resistor 10k 0402	R8, R13, R16, R17, R22	5	Panasonic	ERA-2AED103X
RES 1.5K OHM 5% 1/16W 0402	Resistor 1.5k 0402	R10	1	Stackpole Electronics	RMCF0402JT1K50

Name	Description	Designator	Quantity	Manufacturer	Part Number
RES SMD 100K OHM 5% 1/10W 0402	Resistor 100k 0402	R11, R18-R21	5	Panasonic	ERJ-2GEJ104X
RES SMD 1K OHM 0.5% 1/16W 0402	Resistor 1k 0402	R12, R15	2	Panasonic	ERA2AED102X
Res 4.99k 0402	Resistor 4.99k 0402	R14	1	Panasonic	ERA-2AEB4991X
180 kOhms ±1% 0.063W, 1/16W Chip Resistor 0402 Automotive AEC-Q200, Moisture Resistant Thick Film	Resistor 180k 0402	R23	1	TE Connectivity	CRGCQ0402F180K
IC OPAMP GP 2 CIRCUIT 8MSOP	IC OPAMP GP 2 CIRCUIT 8MSOP	U1	1	Analog Devices / Linear Technology	LTC6247IMS8#TRPBF
MCP47FEB22A0- E/ST	IC DAC 12BIT	U2	1	Microchip	MCP47FEB22A0-E/ST
IC VREF SERIES 2.5V TSOT23-6	Series Voltage Reference IC ±0.05% 5mA TSOT-23-6	U3	1	Analog Devices / Linear Technology	LT6656BCS6-2.5#TRMPBF

Name	Description	Designator	Quantity	Manufacturer	Part Number
TPS63020DSJR	Buck-Boost Switching Regulator IC Positive Adjustable 1.2V 1 Output 3.5A (Switch) 14-VFDFN Exposed Pad	U4	1	Texas Instruments	TPS63020DSJR
IC MCU 8BIT 1KB FLASH	ATMEL ATTINY10- TSHR 8 Bit Microcontroller, Low Power High Performance, ATTINY, 12 MHz, 1 KB, 30 Byte, 6 Pins, SOT-23	U5	1	Microchip	ATTINY10-TSHR
Comparator General Purpose CMOS, Push-Pull, TTL SC-70-5	IC COMPARATOR R-R SC70-5	U7	1	Maxim	MAX9140EXK+T

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Name	Description	Designator	Quantity	Manufacturer	Part Number
CAP CER 0.1uF 25V X5R 0402	Capacitor 0.1uF 0402 25V	C1	1	Samsung	CL05A104KA5NNNC
CAP CER 20PF 50V C0G/NP0 0402	Capacitor 20pF 0402	C2	1	Murata	GJM1555C1H200FB01D
CAP CER 1uF 100V X7S 0805	Capacitor 1uF 0805	C3-C34	32	TDK	C2012X7S2A105M125AE
Cap 22uF	Capacitor 22uF 0603 10V	C35	1	Murata	GRM188R61A226ME15D
Diode	Diode Standard 100V 200mA (DC) Surface Mount SOD-523	D1-D32	32	ON Semiconductor	NSD914XV2T1G
D Schottky MA3X028WAL	Diode Standard 6V 100mA (DC) Surface Mount Mini3-G1	D33	1	Panasonic SSG	MA3X028WAL
CONN HEADER VERT 4POS 2.54MM	CONN HDR 4POS 0.1 TIN PCB MALE	J1, J2	2	Sullins	PPTC041LFBN-RC
74404064220	FIXED IND 22UH 1.8A 89 MOHM SMD	L1	1	Würth Electronics	74404064220
Header 2	Header, 2-Pin	P1	1	Harwin	M20-9990246

Name	Description	Designator	Quantity	Manufacturer	Part Number
N-FET IRL100HS121	MOSFET N-CH 100V 6PQFN	Q1	1	Infineon	IRL100HS121
Res 400MEG 1206	Res 400MEG 1206 1500V	R1, R3	2	Vishay Dale	CRHV1206AF400MJNE5
Res 3.4MEG 0402	Res 3.4MEG 0402 30V	R2	1	Vishay	CRCW04023M40FKED
ATTINY85	IC MCU 8BIT 8KB FLASH 20QFN	U1	1	Microchip	ATTINY85-20MUR

Name	Description	Designator	Quantity	Manufacturer	Part Number
BATT HOLDER CR123A	Battery Holder (Open) CR123A 1 Cell PC Pin	BT1	1	Keystone Electronics	1051
100pF	CAP CER 100PF 50V NP0 0402	C1	1	Murata	GCM1555C1H101JA16D
0.10uF	CAP CER 0.1UF 100V X5R 0402	C2, C3	2	Murata	GRM155R62A104KE14D
2200pF	CAP CER 2200PF 100V X7R 0402	C4	1	Murata	GCM155R72A222KA37D
1uF	CAP CER 1UF 100V X7S 0805	C5-C10, C13-C53	47	Murata	GRJ21BC72A105KE11L
10uF	CAP CER 10UF 6.3V X5R 0402	C11, C12	2	Murata	ZRB15XR60J106ME12D
10uF	CAP CER 10UF 6.3V X5R 0402	C54	1	Murata	GRJ155R60J106ME11D

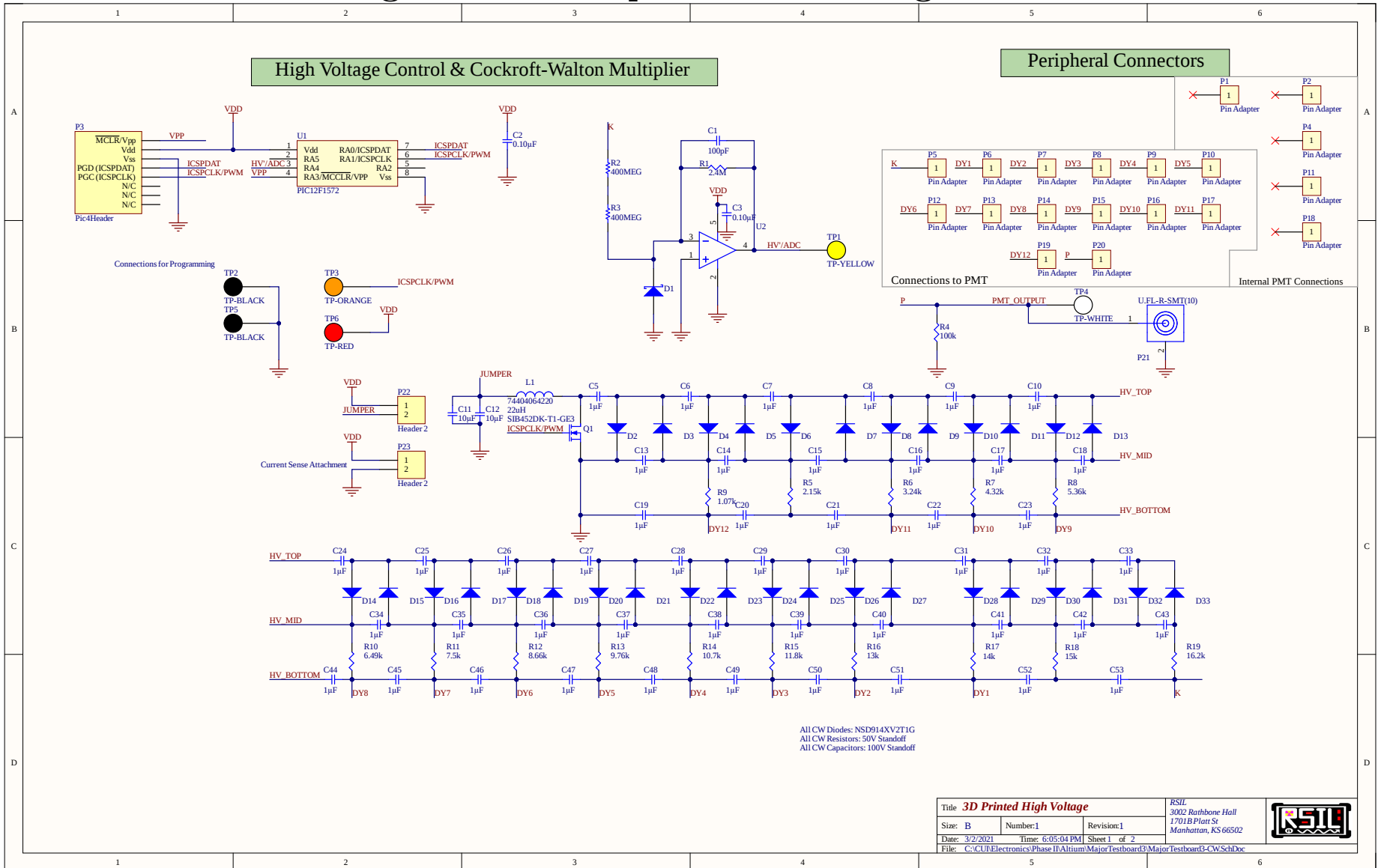
Name	Description	Designator	Quantity	Manufacturer	Part Number
Diode	Diode Standard 100V 200mA (DC) Surface Mount SOD-523	D2-D33	32	ON Semiconductor	NSD914XV2T1G
74404064220	FIXED IND 22UH 1.8A 89 MOHM SMD	L1	1	Wurth Electronics	74404064220
Inductor 2.2uH	FIXED IND 2.2UH 1.2A 228 MOHM	L2	1	Abracon	AIML-0805HC-2R2M-T
Pin Receptacle Connector No Tail Press-Fit	PMT Adapter	P1-P20	19	Mill-Max	0462-0-15-15-21-27-04-0
Pic4Header	Used with Pickit4	P3	1	Amphenol FCI	68016-108HLF
CONN U.FL RCPT STR 50 OHM SMD	U.FL (UMCC) Connector Receptacle, Male Pin 50Ohm Surface Mount Solder	P21	1	Hirose	U.FL-R-SMT-1(01)
Header 2	Header, 2-Pin	P22-P25	4	Harwin	M20-9990246

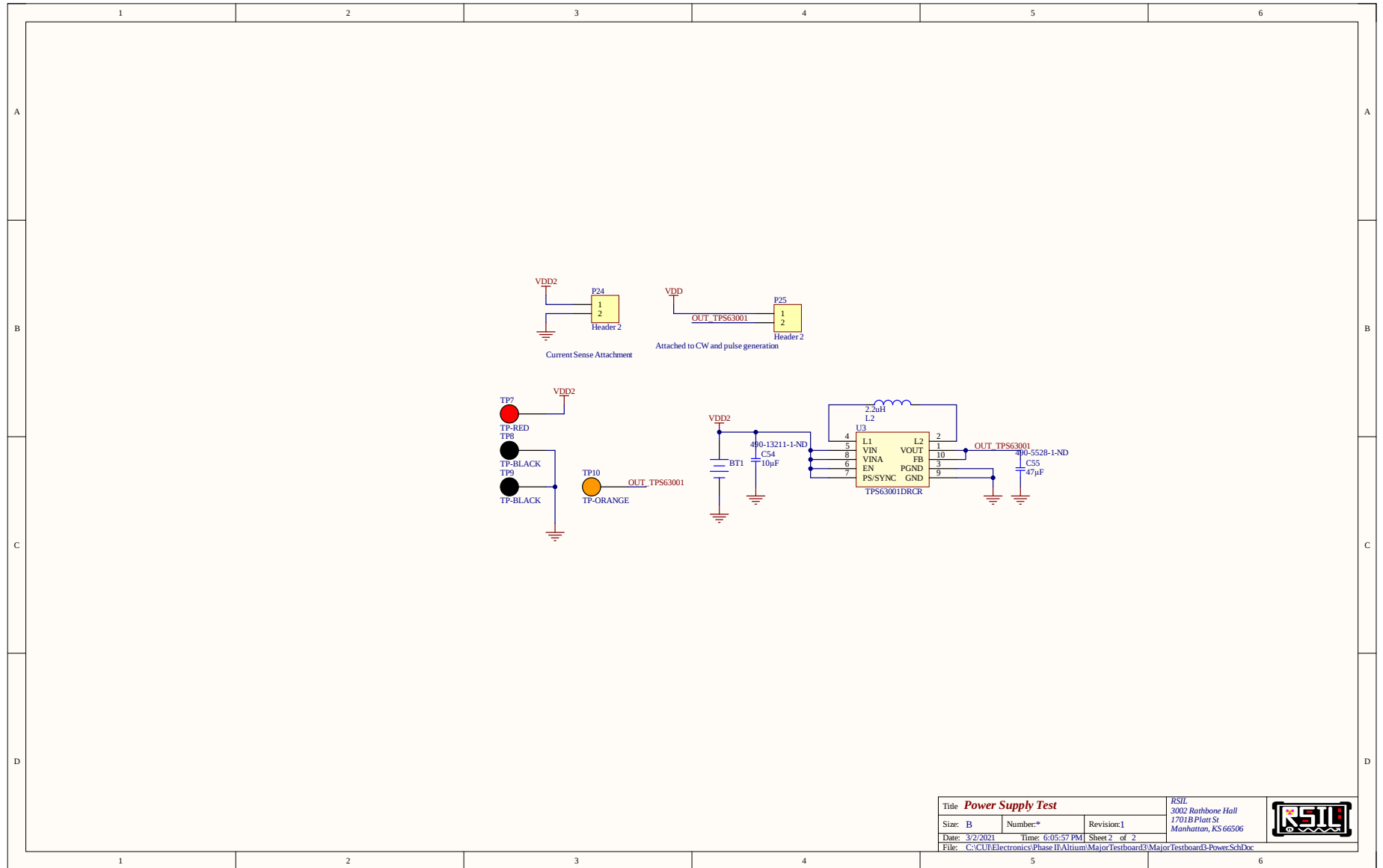
Name	Description	Designator	Quantity	Manufacturer	Part Number
3.4MEG	Res 3.4MEG 0402 30V	R1	1	Vishay	CRCW04023M40FKED
400MEG	Res 400MEG 1206 1500V	R2, R3	2	Vishay Dale	CRHV1206AF400MJNE5
100k	RES SMD 100K OHM 1% 1/10W 0402	R4	1	Panasonic	ERJ2RKF1003X
1k	RES SMD 1K OHM 1% 1/10W 0402	R5, R6, R7, R8, R9, R10, R11	7	Panasonic	ERJ3EKF1001V
4.7k	RES SMD 4.7K OHM 1% 1/10W 0402	R12, R13, R14, R15	4	Panasonic	ERJ-2RKF4701X
10k	RES SMD 10K OHM 1% 1/10W 0402	R16, R17, R18, R19	4	Panasonic	ERJ-2RKF1002X
TP-YELLOW	Yellow PC Test Point, Miniature Phosphor Bronze, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type	TP1	1	Terminal	5004
TP-BLACK	Black PC Test Point, Miniature Phosphor Bronze, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type	TP2, TP5, TP8, TP9	4	Terminal	5001

Name	Description	Designator	Quantity	Manufacturer	Part Number
TP-ORANGE	Orange PC Test Point, Miniature Phosphor Bronze, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type	TP3, TP10	2	Keystone Electronics	5003
TP-WHITE	White PC Test Point, Miniature Phosphor Bronze, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type	TP4	1	Keystone Electronics	5002
TP-RED	Red PC Test Point, Miniature Phosphor Bronze, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type	TP6, TP7	2	Keystone Electronics	5000
PIC12F1572	PIC PIC® 12F Microcontroller IC 8-Bit 32MHz 3.5KB (2K x 14) FLASH 8-DFN (3x3)	U1	1	Microchip	PIC12F1572T-I/MF
Op Amp - BU7445HFV-TR	IC OPAMP GP 1 CIRCUIT HVSO5	U2	1	Rohm	BU7445HFV-TR

Name	Description	Designator	Quantity	Manufacturer	Part Number
IC REG BCK BST 3.3V 1.6A 10VSON	Buck-Boost Switching Regulator IC Positive Fixed 3.3V 1 Output 1.6A (Switch) 10-VFDFN Exposed Pad	U3	1	Texas Instruments	TPS63001DRCR
47uF	CAP CER 47UF 10V X5R 1206	C55	1	Murata	GRM31CR61A476ME15L
D Schottky MA3X028WAL	Diode Standard 6V 100mA (DC) Surface Mount Mini3-G1	D1	1	Panasonic SSG	MA3X028WAL
N-FET SIB452DK-T1- GE3	MOSFET N-CH 190V 1.5A SC75-6	Q1	1	Vishay Siliconix	SIB452DK-T1-GE3

A.7 Finalized Design Variant - Optimized Filtering





Name	Description	Designator	Quantity	Manufacturer	Part Number
BATT HOLDER CR123A	Battery Holder (Open) CR123A 1 Cell PC Pin	BT1	1	Keystone Electronics	1051
100pF	CAP CER 100PF 50V NP0 0402	C1	1	Murata	GCM1555C1H101JA16D
0.10uF	CAP CER 0.1UF 100V X5R 0402	C2, C3	2	Murata	GRM155R62A104KE14D
1uF	CAP CER 1UF 100V X7S 0805	C5-10, C13-C53	47	Murata	GRJ21BC72A105KE11L
10uF	CAP CER 10UF 6.3V X5R 0402	C11, C12	2	Murata	ZRB15XR60J106ME12D
10uF	CAP CER 10UF 6.3V X5R 0402	C54	1	Murata	GRJ155R60J106ME11D
47uF	CAP CER 47UF 10V X5R 1206	C55	1	Murata	GRM31CR61A476ME15L
D Schottky MA3X028WAL	Diode Standard 6V 100mA (DC) Surface Mount Mini3-G1	D1	1	Panasonic SSG	MA3X028WAL
Diode	Diode Standard 100V 200mA (DC) Surface Mount SOD-523	D2-33	32	ON Semiconductor	NSD914XV2T1G

Name	Description	Designator	Quantity	Manufacturer	Part Number
74404064220	FIXED IND 22UH 1.8A 89 MOHM SMD	L1	1	Würth Electronics	74404064220
Inductor 2.2uH	FIXED IND 2.2UH 1.2A 228 MOHM	L2	1	Abracon	AIML0805HC2R2MT
Header 2	Header, 2-Pin	P22, P23, P24, P25	4	Harwin	M20-9990246
N-FET SIB452DK-T1- GE3	MOSFET N-CH 190V 1.5A SC75-6	Q1	1	Vishay Siliconix	SIB452DK-T1-GE3
2.4M	RES SMD 2.4M OHM 5% 1/10W 0402	R1	1	Vishay	CRCW04022M40FKED
400M	Res 400MEG 1206 1500V	R2, R3	2	Vishay Dale	CRHV1206AF400MJNE5
100k	RES SMD 100K OHM 1% 1/10W 0402	R4	1	Panasonic	ERJ2RKF1003X
2.15k	RES SMD 2.15K OHM 1% 1/10W 0402	R5	1	Panasonic	ERJ2RKF2151X

Name	Description	Designator	Quantity	Manufacturer	Part Number
3.24k	RES SMD 3.24K OHM 1% 1/10W 0402	R6	1	Panasonic	ERJ2RKF3241X
4.32k	RES SMD 4.32K OHM 1% 1/10W 0402	R7	1	Vishay	CRCW04024K32FKED
5.36k	RES SMD 5.36K OHM 1% 1/10W 0402	R8	1	Panasonic	ERJ-2RKF5361X
1.07k	RES SMD 1.07K OHM 1% 1/10W 0402	R9	1	Panasonic	ERJ-2RKF1071X
6.49k	RES SMD 6.49K OHM 1% 1/10W 0402	R10	1	Panasonic	ERJ-2RKF6491X
7.5k	RES SMD 7.5K OHM 5% 1/10W 0402	R11	1	Panasonic	ERJ-2GEJ752X

Name	Description	Designator	Quantity	Manufacturer	Part Number
8.66k	RES SMD 8.66K OHM 1% 1/10W 0402	R12	1	Panasonic	ERJ-2RKF8661X
9.76k	RES SMD 9.76K OHM 1% 1/10W 0402	R13	1	Vishay	CRCW04029K76FKED
10.7k	RES SMD 10.7K OHM 1% 1/10W 0402	R14	1	Panasonic	ERJ-2RKF1072X
11.8k	RES SMD 11.8K OHM 1% 1/10W 0402	R15	1	Panasonic	ERJ-2RKF1182X
13k	RES SMD 13K OHM 1% 1/10W 0402	R16	1	Panasonic	ERJ-2RKF1302X
14k	RES SMD 14K OHM 1% 1/10W 0402	R17	1	Panasonic	ERJ-2RKF1402X
15k	RES SMD 15K OHM 1% 1/10W 0402	R18	1	Panasonic	ERJ-2RKF1502X
16.2k	RES SMD 16.2K OHM 1% 1/10W 0402	R19	1	Panasonic	ERJ-2RKF1622X

Name	Description	Designator	Quantity	Manufacturer	Part Number
TP-YELLOW	Yellow PC Test Point, Miniature Phosphor Bronze, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type	TP1	1	Keystone Electronics	5004
TP-BLACK	Black PC Test Point, Miniature Phosphor Bronze, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type	TP2, TP5, TP8, TP9	4	Terminal	5001
TP-ORANGE	Orange PC Test Point, Miniature Phosphor Bronze, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type	TP3, TP10	2	Keystone Electronics	5003
TP-WHITE	White PC Test Point, Miniature Phosphor Bronze, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type	TP4	1	Keystone Electronics	5002

Name	Description	Designator	Quantity	Manufacturer	Part Number
TP-RED	Red PC Test Point, Miniature Phosphor Bronze, Silver Plating 0.040" (1.02mm) Hole Diameter Mounting Type	TP6, TP7	2	Keystone Electronics	5000
PIC12F1572	PIC PIC® 12F Microcontroller IC 8-Bit 32MHz 3.5KB (2K x 14) FLASH 8-DFN (3x3)	U1	1	Microchip	PIC12F1572T-I/MF
Op Amp - BU7445HFV-TR	IC OPAMP GP 1 CIRCUIT HVSO5	U2	1	Rohm	BU7445HFV-TR
IC REG BCK BST 3.3V 1.6A 10VSON	Buck-Boost Switching Regulator IC Positive Fixed 3.3V 1 Output 1.6A (Switch) 10-VFDFN Exposed Pad	U3	1	Texas Instruments	TPS63001DRCR
Pic4Header	Used with Pickit4	P3	1	Amphenol FCI	68016-108HLF

Name	Description	Designator	Quantity	Manufacturer	Part Number
CONN U.FL RCPT STR 50 OHM SMD	U.FL (UMCC) Connector Receptacle, Male Pin 50Ohm Surface Mount Solder	P21	1	Hirose	U.FL-R-SMT-1(01)
Pin Receptacle Connector No Tail Press-Fit	PMT Adapter	P1, P2, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20	19	Mill-Max	0462-0-15-15-21-27-04-0

Appendix B

Microcontroller Algorithms

The microcontroller algorithms can be found in Appendix [B](#) for the following:

1. LED Count-Rate Indication Code
2. ATTINY85 Microcontroller Test Article Code
3. PIC Microcontroller Code

- (a) `main.c`
- (b) `adc1.h`
- (c) `adc1.c`
- (d) `device_config.h`
- (e) `device_config.c`
- (f) `interrupt_manager.h`
- (g) `interrupt_manager.c`
- (h) `mcc.h`
- (i) `mcc.c`

- (j) pin_manager.h
- (k) pin_manager.c
- (l) pwm1.h
- (m) pwm1.c
- (n) tmr0.h
- (o) tmr0.c
- (p) tmr2.h
- (q) tmr2.c

B.1 LED Pulse Indication Code

The following C script generates the green LED pulse for visual indication of increased count rate for use with the ATTINY10.

```
// Discrete 3D Electronics
// LED Pulse Processing
// Date: June 25, 2019
// Updated: August 8, 2019

#include <avr/io.h>
#include <avr/interrupt.h>

volatile uint16_t counts = 0; //count rate limited by interrupt clock, i.e. 8
    MHz
volatile uint32_t timer_val = 0; //should reset before overflow
volatile uint32_t frequency = 1; //global for checking frequency
volatile uint32_t run_counter = 0; //live timestamp for total running time, in
    25ms increments. Overflows at 3.4 years
    //used for flashing the LED at a consistent
    speed
volatile uint8_t timer_int = 0;

//initialize interrupt settings
void init_isr(void);
//initialize ATTINY10 gpio
void init_gpio(void)
//switches the green led at an input clock interval
void switch_green(volatile uint32_t interval1)

//Timer interrupt, occurs once every 25ms
ISR(TIM0_COMPA_vect){
    timer_int = 1;
}

//Incoming pulse interrupt, occurs every rising pulse edge
```

```

ISR(INT0_vect) {
    counts++; //check for overflow
}

void init_isr(void) {
    //-----CLOCK SECTION-----
    // Ensure Clock doesn't accidentally switch from the 8 MHz
    CCP = 0b11011000; //Configuration Change Protection
    CLKPSR = 0x00; //Clock Prescaler Register - Division Factor 1
    WDTCR = 0x00; //Disable watchdog reset. Bad doggy.
    //-----END CLOCK SECTION-----

    //-----TIMER SECTION-----
    //Timer/Counter0 Control Registers Combined to make CTC mode
    TCCR0A = 0b00000000; //All 0's
    TCCR0B = 0b01001010; // ICES0 = 1, WGM02 = 1, CS0[2:0] = 010 (clk/8
    prescaler)

    //Output compare register high and low bytes Timer A
    //OCR0A max value = 65535
    OCR0A = 25000 - 1; //25ms interrupts for timer, 25ms/(1/(8MHz/8))
    TIMSK0 = 0b00000010; //Timer Interrupt Mask Register,
    //-----END TIMER SECTION-----

    //-----EXTINT SECTION-----
    //We are using INT0, not the PCINT
    EICRA = 0b00000011; //rising edge interrupt
    EIMSK = 0b00000001; //enable external interrupt
    //-----ENDEXTINT SECTION-----

    sei(); //enable global interrupts
}

void init_gpio(void) {
    DDRB = 0b00001011; //PB0 PB1 PB3 output. PB2 input
    PUEB = 0b00001011;
    PORTB = 0b00001011; //Set outputs high (turn off LEDs), and pulldown on
    input
}

void switch_green(volatile uint32_t interval) {
    if(run_counter >= interval){
        run_counter = 0;
        PORTB = PORTB ^ 0b00000010; //switch only green to save on power
    }
}

//Main program
int main(void) {
    init_gpio(); //Initialize the GPIO pins
    init_isr(); //Initialize the ISRs, timer and extint
    volatile uint32_t interval = 40;
    while (1) {
        //runs constantly, counting and frequency calculations are done through
        interrupts
        //convert the frequency value into an interval for the LED control
        if(frequency <= 1){
            switch_green(40);
        }
        else if(frequency <= 255) {
            switch_green(28);
        }
        else if(frequency <= 511){
            switch_green(16);
        }
    }
}

```

```

    }
    else if(frequency <= 1023){
        switch_green(4);
    }
    else switch_green(1);

//timer interrupt handler
if(timer_int >= 1) {
    timer_int = 0;
    run_counter++; //overflow at 3.4 years
    timer_val++; //increment timer
    if(timer_val >= 20) { //scales off of time_window
        frequency = counts*2; //this occurs once every time_window interval
        counts = 0; //reset counts for next interval
        timer_val = 0; //reset timer for next interval
    }
}
}
}
}

```

B.2 ATTINY85 Code

The following C script generates an appropriate PWM and control scheme for the ATTINY85 prototype circuit. This allowed the team to verify a microcontroller was adequate for a front-end replacement.

```

/*
Project: Attiny85 ADC and Comparator Code Front End Replacement
Date Created: 9/12/2019
Date of Last Revision: 3/2/2021

Project Description:
This Attiny85 code implements the ADC and Comparator functions of an
Attiny85.

The ADC will:
- Continue running while the rest of the Micro is asleep.
- Fire an interrupt to wake the Micro when it's completed it's conversion

The Comparator will:
- Compare the ADC value against a software-set value.
- If the ADC value is GREATER than the software-set value, then the script
  will set the Micro to "Sleep" again.
- If the ADC value is LESS than the software-set value, then the script
  will enable the PWM IO and send off to ADC again.

The PWM will:
- Control the NFET provides the signal to the inductor, generating our
  transient response to produce a high, DC voltage.
*/

#include <Arduino.h>
#include <avr/io.h>
#include <avr/sleep.h>
#include <avr/interrupt.h>
#include <util/delay.h>
#include <math.h>

```

```

float voltagesetpoint, desiredvoltage;
volatile float voltageread;
bool started;

/* gpio_init: initialize GPIO as inputs/outputs */
void gpio_init(void);
/*PWM_init: initialize PWM mode */
void PWM_init(void);
/*Use this function to "Soft Start" the system if the feedback voltage is
  below a certain threshold relative to the Set Point. */
void soft_start(void);
/*soft_start(): A function to set the MCU to sleep mode */
void sleep(void);
/*stopThatMut - disable the watchdog timer */
void disable_watchdog(void);
/* enableInterrupts(): enables the global interrupts */
void enable_interrupts(void);
/*adc_init() initialize the ADC */
void adc_init(void);
/*pwm_maintain() - calculates the output frequency for the PWM based on the
  feedback of the system.
  Parameters:
    setpointvoltage - voltage used as the setpoint (in this case it is 2.9)
    voltageread - voltage read by the ADC interrupt
*/
void pwm_maintain(float setpointvoltage, float voltageread);
/*pwm_setpoint - calculates the voltage feedback based on the time domain of
  the system.
  Parameters:
    setpointvoltage - voltage used as the setpoint (in this case it is 2.9)
    voltageread - voltage read by the ADC interrupt
*/
void pwm_startup(void);

int main(void)
{
  disable_watchdog();
  enable_interrupts();
  gpio_init();
  adc_init();
  PWM_init();

  desiredvoltage = 700; // Set our voltage value to compare against. We're
    aiming for a minimum of 700V
  voltagesetpoint = desiredvoltage * (3.4 / 800.0); //Voltage Divider on
    output of HV circuit

  started = false; // Initialize Start-up flag

  // Initialize voltage read variable to nothing.
  voltageread = 0.0;

  while (1)
  {
    if (!started)
    {
      soft_start(); //soft start only if circuit isn't already functioning
    }
    else
    {
      sleep(); //enable sleep function for interrupt to try to conserve power
      pwm_maintain(voltagesetpoint, voltageread);
    }
  }
}

```

```

void gpio_init(void)
{
    // Setup D0, or PB0, as an output, and set it LOW.
    DDRB |= ((1 << DDB0) | (1 << DDB1) | (1 << DDB2));
    PORTB &= ~( (1 << PB0) | (1 << PB1));
    // Setup PB3 as an input.
    DDRB &= ~(1 << DDB3);
}

void soft_start(void)
{
    if ((voltage_setpoint >= voltage_read))
    {
        pwm_startup();
    }
}

void PWM_init(void)
{
    /*
     * Set up the Fast PWM using Timer/Counter1 (pg. 83)
     * Want !OC1A to be toggled
     * LSM[0] = 1 enables the Low Speed Mode. We'll start with this to reduce
     * power consumption. Will change PCK from 64MHz to 32MHz.
     * PCKE[0] = 1 changes the clock source to the PLL and runs the clock
     * asynchronously.
     * PLLE[0] = 1 starts the PLL.
     * PLOCK[0] = ~ <- Wait until this is set to logic 1 before
     */
    PLLCSR |= ((1 << LSM) | (1 << PLLE));

    while (!(PLLCSR & 1 << PLOCK))
    {
        // We just need to wait here until we get confirmation that the PLL has
        // started (100us) and the PLOCK bit has been set.
    }

    PLLCSR |= (1 << PCKE);

    /* Timer/Counter Control Register A (pg. 89)
     * PWM1A[0] = 1 enables the PWMA signal
     * COM1A[1:0] = 01 to set the !OCR1A pin on compare match
     * CS1[3:0] = 0001 to set the Asynchronous Clock as PCK
     * OCR1C = 127 to set up 500kHz signal
     * Governing formula:
     * fPWM = fTCK1/(OCR1C + 1)
     * For what we've got so far, fTCK = 32MHz, OCR1C = 127, SO fPWM = 32,000,000
     * Hz/(127+1) = 250,000Hz.
     */
    TCCR1 |= ((1 << PWM1A) | (1 << COM1A0) | (1 << CS10));
    TCCR1 &= ~( (1 << CS13) | (1 << CS12) | (1 << CS11) | (1 << COM1A1));

    OCR1C = 212; // Set our output compare register C to set the PWM frequency
    // of the circuit.
}

void pwm_maintain(float setpoint_voltage, float voltage_read)
{
    // Initialize our PWM to have a changing duty cycle
    if (setpoint_voltage >= voltage_read)
    {

```

```

    float deltavoltage = setpointvoltage - voltageread;
    // Maintain the exponential increase with maximum value at 50%
    float duty_cycle = 88 - exp(2*deltavoltage + 2.5)/exp(setpointvoltage);
    OCR1A = duty_cycle;
}
else {
    OCR1A = 0xFF; //Set the output to completely off as pulse isn't necessary
}
}

void pwm_startup(void)
{
    // Starting up from OFF. Exponentially ramp up Duty Cycle. Time measured in
    // us.
    unsigned int startup_time = 1000;

    for (unsigned int i = 0; i <= startup_time; i++)
    {
        //Adjust duty cycle based on time.
        float duty_cycle = 212 - (3.75 * (exp(i / (0.3 * startup_time))));
        OCR1A = duty_cycle;
    }

    started = true;
}

void sleep(void)
{
    ADCSRA |= (1 << ADEN);

    /* Enable Sleep Mode:
       SLEEP_MODE_IDLE enables the ADC and IO clocks. Uses ~3.5mA.
       SLEEP_MODE_ADC enables only the ADC clocks. Uses ~2mA.
       SLEEP_MODE_PWR_DOWN shutdowns all but external interrupts. Uses ~ 300uA.
    */
    set_sleep_mode(SLEEP_MODE_IDLE);

    /*
       Using the Power Reduction Register to turn off specific peripherals.
       Disabling both of these peripherals decreases current consumption by 0.900mA
       .
       PRTIM0[0] = 1 disables the Timer/Counter 0 peripheral.
       PRUSI[0] = 1 disables the Universal Serial Interface.
    */
    PRR |= ((1 << PRTIM0) | (1 << PRUSI));

    //Disable the Brown-Out Detector. Testing shows that this saves roughly
    // 0.481mA
    MCUCR |= (1 << BODS);

    // Sets the Sleep Enable bit inside of the MCU register.
    sleep_enable();

    // Redundantly enable Global Interrupts.
    enable_interrupts();

    // Actually put the Attiny85 to sleep until woken by the ADC Conversion
    // Complete Interrupt.
    sleep_cpu();

    // Clear the Sleep Enable Bit.
    sleep_disable();
}

void disable_watchdog(void)

```

```

{
    WDTCR &= ~( (1 << WDE) | (1 << WDIE));
}

void enable_interrupts(void)
{
    sei();
}

void adc_init(void)
{
    /*For the Admux Register,
       Setting REFS[2:0] = Bx00 selects the internal VCC as the voltage reference
       .
       Configuring MUX[3:0] = B0011 selects PB3 as the ADC input.
       Configuring ADLAR[0] = 0 selects the RIGHT-ALIGNMENT for the ADC data
       registers.
    */
    ADMUX |= ((1 << MUX0) | (1 << MUX1));

    ADMUX &= ~( (1 << REFS0) | (1 << REFS1) | (1 << MUX2) | (1 << MUX3) | (1 <<
        ADLAR));

    /* Enable the ADC and clock prescaler. For our config of,
       ADPS[2:0] = 111, our prescaling division factor be 128.
       ADATE[0] = 1 enables the ADC Auto Trigger Enable. This allows it to begin
       conversions immediately.
    */
    ADCSRA |= ((1 << ADPS2) | (1 << ADPS1) | (1 << ADPS0) | (1 << ADATE));

    // Run in Free-running Mode.
    ADCSRB &= ~( (1 << ADTS0) | (1 << ADTS1) | (1 << ADTS2));

    // Disable digital inputs.
    DIDR0 |= (1 << ADC3D);

    // Enable the ADC Interrupt Flag
    ADCSRA |= (1 << ADIE);

    // Enable the ADC.
    ADCSRA |= (1 << ADEN);

    // Start a conversion
    ADCSRA |= (1 << ADSC);
}

ISR(ADC_vect)
{
    // For our 10-bit ADC, we must read the LOW ADC Data Register first.
    voltageread = ADCL | (ADCH << 8);
    // Convert ADC 10 bit value into actual voltage.
    voltageread = voltageread * 5.1 / 1024.0;
}

```

B.3 PIC Microcontroller Code

B.3.1 main.c

The following C script is the main function for the PIC microcontroller code. It implements the slow-start algorithm and the PID functionality.

```
#include <stdint.h>
#include "mcc_generated_files/mcc.h"
#include "stdlib.h"

uint16_t voltageSetPoint = 651; //HV = 700V -> 2.1V Feedback -> (
    DESIRED_VOLTAGE*(24/8000))*(1023/3.3V)
uint16_t offset = 155; //0.5V offset //31; // 0.1V offset //77; //77; //
    0.25V offset target for PID loop
bool Started;
uint16_t duty_cycle;

//PID gains are all scaled by 100 later
int16_t Kp = 100; //proportional gain
int16_t Ki = 1; //integral gain
int16_t Kd = 20; //derivative gain
int16_t errorIntegral = 0; //sum of errors
int16_t lasterr = 0;

void softStart(uint16_t voltsetpoint, uint16_t voltRead);
void pwm_maintain(uint16_t voltsetpoint, uint16_t voltRead);
void pwm_startup(void);
uint16_t pid_controller(int16_t error);

void main(void)
{
    // initialize the device
    SYSTEM_Initialize();
    Started = false;

    // Enable the Global Interrupts
    INTERRUPT_GlobalInterruptEnable();

    // Enable the Peripheral Interrupts
    INTERRUPT_PeripheralInterruptEnable();

    PWM1_PhaseSet(0);
    PWM1_PeriodSet(52); // 150kHz
    duty_cycle = 0; //Percent

    while (1)
    {
        if(!Started){
            softStart(voltageSetPoint, ADC1_GetConversion(ADC_INPUT));
        }
        else {
            pwm_maintain(voltageSetPoint, ADC1_GetConversion(ADC_INPUT));
        }
    }
}

void softStart(uint16_t voltageSetPoint, uint16_t voltRead) {
    if(voltageSetPoint - offset >= voltRead){
        pwm_startup();
    }
}
```

```

        else {
            Started = true;
        }
    }

void pwm_startup(void) {
    __delay_ms(500);
    PWM1_Stop();
    if(duty_cycle <= 5 ) {
        duty_cycle = duty_cycle + 1;
    }
    else if(duty_cycle <= 13 ) {
        duty_cycle = duty_cycle + 2;
    }
    else if(duty_cycle <= 18 ) {
        duty_cycle = duty_cycle + 3;
    }
    else if(duty_cycle <= 28) {
        duty_cycle = duty_cycle + 5;
    }
    else {
        duty_cycle = 26;
        Started = true;
    }
    PWM1_DutyCycleSet(duty_cycle);
    PWM1_Start();
}

void pwm_maintain(uint16_t voltsetpoint, uint16_t voltRead) {
    int16_t error; //error constant
    error = (int16_t)(voltsetpoint) - (int16_t)voltRead;
    uint16_t dutycycle;
    dutycycle = pid_controller(error);
    if(dutycycle == 0) {
        PWM1_Stop();
    }
    else {
        PWM1_Stop();
        PWM1_DutyCycleSet(dutycycle);
        PWM1_Start();
    }
}

uint16_t pid_controller(int16_t err) {
    //err += 10;
    int16_t P = Kp*err;
    errorIntegral = errorIntegral + err;
    int16_t I = Ki*(errorIntegral);
    int16_t D = Kd*(lasterr - err);
    lasterr = err;
    int16_t PID = P + I + D;
    PID = PID/100;

    if(PID >= 26) {
        return 26;
    }
    if(PID <= 0) {
        return 0;
    }
    return (uint16_t)PID;
}

```

B.3.2 adc1.h

The following C header file initialized the ADC options using timer0 as well as any functions associated with the ADC.

```
#ifndef ADC1_H
#define ADC1_H

/**
 * Section: Included Files
 */

#include <xc.h>
#include <stdint.h>
#include <stdbool.h>

#ifdef __cplusplus // Provide C++ Compatibility
    extern "C" {
#endif

//voltageRead declaration
uint16_t voltageRead;

// result size of an A/D conversion
typedef uint16_t adc_result_t;

/*
 * result type of a Double ADC conversion
 */
typedef struct
{
    adc_result_t adcResult1;
    adc_result_t adcResult2;
} adc_sync_double_result_t;

/* ADC Channel Definition */

typedef enum
{
    ADC_INPUT = 0x3,
    channel_Temp = 0x1D,
    channel_DAC = 0x1E,
    channel_FVR = 0x1F
} adc_channel_t;

/*
 * This routine initializes the ADC1.
 * This routine must be called before any other ADC1 routine is called.
 * This routine should only be called once during system initialization.
 */
void ADC1_Initialize(void);

/*
 * Starts conversion
 * This routine is used to start conversion of desired channel.
 * ADC1_Initialize() function should have been called before calling this
 * function.
 */

/*
 * Returns the ADC1 conversion value.
 * This routine is used to get the analog to digital converted value. This
```

```

        routine gets converted values from the channel specified.
        This routine returns the conversion value only after the conversion is
        complete.
        Completion status can be checked using
        ADC1_IsConversionDone() routine.
    */
    adc_result_t ADC1_GetConversionResult(void);

    /*
        Returns the ADC1 conversion value
        also allows selection of a channel for conversion.
        This routine is used to select desired channel for conversion
        and to get the analog to digital converted value.
        ADC1_Initialize() function should have been called before calling this
        function.
        Returns the converted value.
        Pass in required channel number.
        "For available channel refer to enum under adc.h file"
    */
    adc_result_t ADC1_GetConversion(adc_channel_t channel);

    /**
        Implements ISR
        This routine is used to implement the ISR for the interrupt-driven
        implementations.
    */
    void ADC1_ISR(void);

    /*
        Set Timer Interrupt Handler
        This sets the function to be called during the ISR
        Initialize the ADC1 module with interrupt before calling this.
        Address of function to be set
        None
    */
    void ADC1_SetInterruptHandler(void (* InterruptHandler)(void));

    /*
        Timer Interrupt Handler
        This is a function pointer to the function that will be called during the
        ISR
        Initialize the ADC1 module with interrupt before calling this isr.
    */
    extern void (*ADC1_InterruptHandler)(void);

    /**
        Default Timer Interrupt Handler
        This is the default Interrupt Handler function
        Initialize the ADC1 module with interrupt before calling this isr.
    */
    void ADC1_DefaultInterruptHandler(void);
#ifdef __cplusplus // Provide C++ Compatibility
}
#endif

#endif //ADC1_H
/**
    End of File
*/

```

B.3.3 adc1.c

The following C file initialized the ADC options using timer0 and implements the functions initialized in adc.h used with the ADC.

```
#include <xc.h>
#include "adc1.h"
#include "device-config.h"

/**
 * Section: Macro Declarations
 */

#define ACQ_US_DELAY 5

void (*ADC1_InterruptHandler)(void);

/**
 * Section: ADC Module APIs
 */

void ADC1_Initialize(void)
{
    // set the ADC1 to the options selected in the User Interface

    // ADFM right; ADPREF VDD; ADCS FOSC/2;
    ADCON1 = 0x80; //right justified

    // TRIGSEL TMR0_overflow;
    ADCON2 = 0x30;

    // ADRESL 0;
    ADRESL = 0x00;

    // ADRESH 0;
    ADRESH = 0x00;

    // GO_nDONE stop; ADON enabled; CHS AN0;
    ADCON0 = 0x01;

    // Enabling ADC1 interrupt.
    PIE1bits.ADIE = 1;

    // Set Default Interrupt Handler
    ADC1_SetInterruptHandler(ADC1_DefaultInterruptHandler);
}

adc_result_t ADC1_GetConversionResult(void)
{
    // Conversion finished, return the result
    return ((adc_result_t)((ADRESH << 8) + ADRESL));
}

adc_result_t ADC1_GetConversion(adc_channel_t channel)
{
    // select the A/D channel
    ADCON0bits.CHS = channel;

    // Turn on the ADC module
    ADCON0bits.ADON = 1;

    // Acquisition time delay
    __delay_us(ACQ_US_DELAY);
}
```

```

    // Start the conversion
    ADCON0bits.GO_nDONE = 1;

    // Wait for the conversion to finish
    while (ADCON0bits.GO_nDONE)
    {
    }

    // Conversion finished, return the result
    return ((adc_result_t)((ADRESH << 8) + ADRESL));
}

void ADC1_ISR(void)
{
    // Clear the ADC interrupt flag
    PIR1bits.ADIF = 0;

    if(ADC1_InterruptHandler)
    {
        ADC1_InterruptHandler();
    }
}

void ADC1_SetInterruptHandler(void (* InterruptHandler) (void)) {
    ADC1_InterruptHandler = InterruptHandler;
}

void ADC1_DefaultInterruptHandler(void) {
    voltageRead = ADC1_GetConversionResult();
}
/**
 * End of File
 */

```

B.3.4 device_config.h

The following C header file initializes the device parameters by setting the clock frequency of oscillation to 8 MHz. This was auto generated by MPLAB⁶⁶.

```

#ifndef DEVICE_CONFIG_H
#define DEVICE_CONFIG_H

#define _XTAL_FREQ 8000000

#endif /* DEVICE_CONFIG_H */
/**
 * End of File
 */

```

B.3.5 device_config.c

The following C file enables the internal oscillator to the 8 MHz, and additional timer settings. Most of these settings were adjusted to reduce unnecessary processing to reduce power consumption. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```
// Configuration bits: selected in the GUI

// CONFIG1
#pragma config FOSC = INTOSC    // ->INTOSC oscillator; I/O function on CLKIN pin
#pragma config WDTE = OFF       // Watchdog Timer Enable->WDT disabled
#pragma config PWRTE = OFF      // Power-up Timer Enable->PWRT disabled
#pragma config MCLRE = ON       // MCLR Pin Function Select->MCLR/VPP pin function is MCLR
#pragma config CP = OFF        // Flash Program Memory Code Protection->Program memory code protection is disabled
#pragma config BOREN = NSLEEP    // Brown-out Reset Enable->Brown-out Reset enabled while running and disabled in Sleep
#pragma config CLKOUTEN = OFF    // Clock Out Enable->CLKOUT function is disabled. I/O or oscillator function on the CLKOUT pin

// CONFIG2
#pragma config WRT = OFF        // Flash Memory Self-Write Protection->Write protection off
#pragma config PLLEN = OFF      // PLL Enable->4x PLL disabled
#pragma config STVREN = ON      // Stack Overflow/Underflow Reset Enable->Stack Overflow or Underflow will cause a Reset
#pragma config BORV = LO        // Brown-out Reset Voltage Selection->Brown-out Reset Voltage (Vbor), low trip point selected.
#pragma config LPBOR = OFF      // Low Power Brown-out Reset enable bit->LPBOR is disabled
#pragma config LVP = ON         // Low-Voltage Programming Enable->Low-voltage programming enabled
```

B.3.6 interrupt_manager.h

The following C header enables the interrupts for use with the ADC. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```
#ifndef INTERRUPT_MANAGER_H
#define INTERRUPT_MANAGER_H

/*
 * Enable global interrupts.
 */
#define INTERRUPT_GlobalInterruptEnable() (INTCONbits.GIE = 1)

/*
 * Disable global interrupts.
 */
#define INTERRUPT_GlobalInterruptDisable() (INTCONbits.GIE = 0)
/**
 * Enable peripheral interrupts.
 */
```

```

#define INTERRUPT_PeripheralInterruptEnable() (INTCONbits.PEIE = 1)

/**
 * Disable peripheral interrupts.
 */
#define INTERRUPT_PeripheralInterruptDisable() (INTCONbits.PEIE = 0)

#endif // INTERRUPT_MANAGER_H
/**
 * End of File
 */

```

B.3.7 interrupt_manager.c

The following C file enables the interrupts for use with the ADC. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```

#include "interrupt_manager.h"
#include "mcc.h"

void __interrupt() INTERRUPT_InterruptManager (void)
{
    // interrupt handler
    if(INTCONbits.PEIE == 1)
    {
        if(PIE1bits.ADIE == 1 && PIR1bits.ADIF == 1)
        {
            ADC1_ISR();
        }
        else
        {
        }
    }
    else
    {
    }
}
/**
 * End of File
 */

```

B.3.8 mcc.h

The following C header initializes states for the microcontroller. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

B.3.9 mcc.c

The following C file initializes states for the microcontroller. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```
#include "mcc.h"

void SYSTEM_Initialize(void)
{
    PIN_MANAGER_Initialize();
    OSCILLATOR_Initialize();
    WDT_Initialize();
    PWM1_Initialize();
    ADC1_Initialize();
    TMR2_Initialize();
    TMR0_Initialize();
}

void OSCILLATOR_Initialize(void)
{
    // SCS FOSC; SPLLEN disabled; IRCF 8MHz_HF;
    OSCCON = 0x70;
    // TUN 0;
    OSCTUNE = 0x00;
    // SBOREN disabled; BORFS disabled;
    BORCON = 0x00;
}

void WDT_Initialize(void)
{
    // WDTPS 1:65536; SWDTEN OFF;
    WDTCON = 0x16;
}

/**
 * End of File
 */
```

B.3.10 pin_manager.h

The following C header initializes the pins for the microcontroller. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```
#ifndef PIN_MANAGER_H
#define PIN_MANAGER_H

/**
 * Section: Included Files
 */

#include <xc.h>

#define INPUT    1
#define OUTPUT   0

#define HIGH     1
```

```

#define LOW          0

#define ANALOG       1
#define DIGITAL      0

#define PULL_UP_ENABLED      1
#define PULL_UP_DISABLED    0

// get/set RA1 procedures
#define RA1_SetHigh()        do { LATAbits.LATA1 = 1; } while(0)
#define RA1_SetLow()         do { LATAbits.LATA1 = 0; } while(0)
#define RA1_Toggle()         do { LATAbits.LATA1 = ~LATAbits.LATA1; }
                             while(0)
#define RA1_GetValue()       PORTAbits.RA1
#define RA1_SetDigitalInput() do { TRISAbits.TRISA1 = 1; } while(0)
#define RA1_SetDigitalOutput() do { TRISAbits.TRISA1 = 0; } while(0)
#define RA1_SetPullup()      do { WPUAbits.WPUA1 = 1; } while(0)
#define RA1_ResetPullup()    do { WPUAbits.WPUA1 = 0; } while(0)
#define RA1_SetAnalogMode()  do { ANSELAbits.ANSA1 = 1; } while(0)
#define RA1_SetDigitalMode() do { ANSELAbits.ANSA1 = 0; } while(0)

// get/set ADC_INPUT aliases
#define ADC_INPUT_TRIS      TRISAbits.TRISA4
#define ADC_INPUT_LAT       LATAbits.LATA4
#define ADC_INPUT_PORT      PORTAbits.RA4
#define ADC_INPUT_WPU       WPUAbits.WPUA4
#define ADC_INPUT_OD        ODCONAbits.ODA4
#define ADC_INPUT_ANS       ANSELAbits.ANSA4
#define ADC_INPUT_SetHigh() do { LATAbits.LATA4 = 1; } while(0)
#define ADC_INPUT_SetLow()  do { LATAbits.LATA4 = 0; } while(0)
#define ADC_INPUT_Toggle()  do { LATAbits.LATA4 = ~LATAbits.LATA4;
                             } while(0)
#define ADC_INPUT_GetValue() PORTAbits.RA4
#define ADC_INPUT_SetDigitalInput() do { TRISAbits.TRISA4 = 1; } while(0)
#define ADC_INPUT_SetDigitalOutput() do { TRISAbits.TRISA4 = 0; } while(0)
#define ADC_INPUT_SetPullup()      do { WPUAbits.WPUA4 = 1; } while(0)
#define ADC_INPUT_ResetPullup()    do { WPUAbits.WPUA4 = 0; } while(0)
#define ADC_INPUT_SetPushPull()    do { ODCONAbits.ODA4 = 0; } while(0)
#define ADC_INPUT_SetOpenDrain()   do { ODCONAbits.ODA4 = 1; } while(0)
#define ADC_INPUT_SetAnalogMode()  do { ANSELAbits.ANSA4 = 1; } while(0)
#define ADC_INPUT_SetDigitalMode() do { ANSELAbits.ANSA4 = 0; } while(0)

/*
 * GPIO and peripheral I/O initialization
 */
void PIN_MANAGER_Initialize (void);

#endif // PIN_MANAGER_H
/**
 * End of File
 */

```

B.3.11 pin_manager.c

The following C file initializes the pin configurations for the microcontroller. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```
#include "pin_manager.h"
```

```

void PIN_MANAGER.Initialize(void)
{
    /* LATx registers*/
    LATA = 0x00;

    /* TRISx registers */
    TRISA = 0x3D;

    /* ANSELx registers */
    ANSELA = 0x14;

    /* WPUx registers */
    WPUA = 0x00;
    OPTION_REGbits.nWPUEN = 1;

    /* ODx registers */
    ODCONA = 0x00;

    /* SLRCONx registers */
    SLRCONA = 0x37;

    /* INLVLx registers */
    INLVLA = 0x3F;

    /* APFCONx registers */
    APFCON = 0x00;
}

/**
 * End of File
 */

```

B.3.12 pwm1.h

The following C header initializes the PWM for the microcontroller. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```

#ifndef PWM1_H
#define PWM1_H

/**
 * Section: Included Files
 */

#include <xc.h>
#include <stdint.h>
#include <stdbool.h>

#ifdef __cplusplus // Provide C++ Compatibility
    extern "C" {
#endif

```

```

/**
  Section: PWM Module APIs
*/

/*
  This routine initializes the PWM1.
  This routine must be called before any other PWM routine is called.
  This routine should only be called once during system initialization.
*/
void PWM1_Initialize(void);

/*
  This function starts the PWM1.
  This function starts the PWM1 operation.
  This function must be called after the initialization of PWM1.
  Initialize the PWM1 before calling this function.
*/
void PWM1_Start(void);

/*
  This function stops the PWM1.
  This function stops the PWM1 operation.
  This function must be called after the start of PWM1.
  Initialize the PWM1 before calling this function.
*/
void PWM1_Stop(void);

/*
  Load required 16 bit phase count
  Set the expected phase count
*/
void PWM1_PhaseSet(uint16_t phaseCount);

/**
  Load required 16 bit Duty Cycle
  Set the expected Duty Cycle
*/
void PWM1_DutyCycleSet(uint16_t dutyCycleCount);

/*
  Load required 16 bit Period
  Set the expected Period
*/
void PWM1_PeriodSet(uint16_t periodCount);

#endif /* PWM1_H */
/**
  End of File
*/

```

B.3.13 pwm1.c

The following C file implements the PWM for the microcontroller. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```

#include <xc.h>
#include "pwm1.h"

/**
  Section: PWM1 APIs
*/

```

```

void PWM1_Initialize(void)
{
    // set the PWM1 to the options selected in the User Interface

    //PHIE disabled; DCIE disabled; OFIE disabled; PRIE disabled;
    PWM1INTE = 0x00;

    //PHIF cleared; OFIF cleared; DCIF cleared; PRIF cleared;
    PWM1INTF = 0x00;

    //PS No_Prescalar; CS FOSC;
    PWM1CLKCON = 0x00;

    //LDS reserved; LDT disabled; LDA do_not_load;
    PWM1LDCON = 0x00;

    //OFM independent_run; OFS reserved; OFO match_incrementing;
    PWM1OFCON = 0x00;

    //PWM1PHH 0;
    PWM1PHH = 0x00;

    //PWM1PHL 0;
    PWM1PHL = 0x00;

    //PWM1DCH 0;
    PWM1DCH = 0x00;

    //PWM1DCL 0;
    PWM1DCL = 0x00;

    //PWM1PRH 0;
    PWM1PRH = 0x00;

    //PWM1PRL 31;
    PWM1PRL = 0x1F;

    //PWM1OFH 0;
    PWM1OFH = 0x00;

    //PWM1OFL 31;
    PWM1OFL = 0x1F;

    //PWM1TMRH 0;
    PWM1TMRH = 0x00;

    //PWM1TMRL 0;
    PWM1TMRL = 0x00;

    //MODE standard_PWM; POL active_hi; OE enabled; EN enabled;
    PWM1CON = 0xC0;
}

void PWM1_Start(void)
{
    PWM1CONbits.EN = 1;
}

void PWM1_Stop(void)
{
    PWM1CONbits.EN = 0;
}

```

```

void PWM1_PhaseSet(uint16_t phaseCount)
{
    PWM1PHH = (uint8_t)(phaseCount>>8);           //writing 8 MSBs to PWMPHH
    register
    PWM1PHL = (uint8_t)(phaseCount);                //writing 8 LSBs to PWMPHL
    register
}

void PWM1_DutyCycleSet(uint16_t dutyCycleCount)
{
    PWM1DCH = (uint8_t)(dutyCycleCount>>8); //writing 8 MSBs to PWMDCH
    register
    PWM1DCL = (uint8_t)(dutyCycleCount); //writing 8 LSBs to PWMDCL register
}

void PWM1_PeriodSet(uint16_t periodCount)
{
    PWM1PRH = (uint8_t)(periodCount>>8); //writing 8 MSBs to PWMPRH register
    PWM1PRL = (uint8_t)(periodCount); //writing 8 LSBs to PWMPRL register
}

/**
 * End of File
 */

```

B.3.14 tmr0.h

The following C header initializes the timer 0 for the microcontroller. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```

#ifndef TMR0_H
#define TMR0_H

/**
 * Section: Included Files
 */

#include <stdint.h>
#include <stdbool.h>

#ifdef __cplusplus // Provide C++ Compatibility
    extern "C" {
#endif

/**
 * Section: TMR0 APIs
 */

/*
 * Initializes the TMR0 module.
 * This function initializes the TMR0 Registers.
 * This function must be called before any other TMR0 function is called.
 */
void TMR0_Initialize(void);

#ifdef __cplusplus // Provide C++ Compatibility

```

```

    }
#endif
#endif // TMR0_H
/**
End of File
*/

```

B.3.15 tmr0.c

The following C file implements the functions the timer 0 for the microcontroller. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```

#include <xc.h>
#include "tmr0.h"

/**
Section: Global Variables Definitions
*/

volatile uint8_t timer0ReloadVal;
/**
Section: TMR0 APIs
*/

void TMR0_Initialize(void)
{
    // Set TMR0 to the options selected in the User Interface

    // PSA assigned; PS 1:256; TMRSE Increment_hi_lo; mask the nWPUEEN and
    INTEDG bits
    OPTION_REG = (uint8_t)((OPTION_REG & 0xC0) | (0xD7 & 0x3F));

    // TMR0 236;
    TMR0 = 0xEC;

    // Load the TMR value to reload variable
    timer0ReloadVal= 236;

    // Clearing IF flag
    INTCONbits.TMR0IF = 0;
}

/**
End of File
*/

```

B.3.16 tmr2.h

The following C header initializes the timer 2 for the microcontroller. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```

#ifndef TMR0_H
#define TMR0_H

```

```

/**
  Section: Included Files
*/

#include <stdint.h>
#include <stdbool.h>

#ifdef __cplusplus // Provide C++ Compatibility
    extern "C" {

#endif

/**
  Section: TMR0 APIs
*/

/*
  Initializes the TMR0 module.
  This function initializes the TMR0 Registers.
  This function must be called before any other TMR0 function is called.
*/
void TMR0_Initialize(void);

#ifdef __cplusplus // Provide C++ Compatibility
    }

#endif

#endif // TMR0_H
/**
  End of File
*/

```

B.3.17 tmr2.c

The following C file implements the functions the timer 2 for the microcontroller. This was auto generated by MPLAB and then stripped down to omit methods not used⁶⁶.

```

#include <xc.h>
#include "tmr0.h"

/**
  Section: Global Variables Definitions
*/

volatile uint8_t timer0ReloadVal;

/**
  Section: TMR0 APIs
*/

void TMR0_Initialize(void)
{
    // Set TMR0 to the options selected in the User Interface

    // PSA assigned; PS 1:256; TMRSE Increment_hillo; mask the nWPUEN and
    INTEDG bits
    OPTION_REG = (uint8_t)((OPTION_REG & 0xC0) | (0xD7 & 0x3F));
}

```

```
// TMR0 236;
TMR0 = 0xEC;

// Load the TMR value to reload variable
timer0ReloadVal= 236;

// Clearing IF flag
INTCONbits.TMR0IF = 0;
}

/**
End of File
*/
```