DESIGN, FABRICATION AND EVALUATION OF A VARIABLE-PULSE-RATE VEHICLE SPEED CONTROL SYSTEM

by

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TABLE OF CONTENTS

LIST OF TABLES

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LIST OF FIGURES

List of Figures (cont.)

CHAPTER 1

INTRODUCTION

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INTRODUCTION

1-1 Introduction

The objective of the work presented in this thesis was to investigate the problems associated with the implementation of a variable pulse-rate control system. This investigation is carried out by the design, fabrication, and testing of a prototype variable pulse-rate vehicle speed control system.

The scope of the project includes the evaluation of the components required for a variable pulse-rate system and the integration of these components into a system. Bench and road experiments were conducted to investigate the capabilities and limitations of the system.

Section 1-2 provides an overview of the operation of the system while section 1-3 describes the operation of commercially available speed regulating systems. Chapter 2 provides a detailed description of each of the sys-systems and Chapter 3 presents the experimental results. Chapter 4 uses the results of the experiments to develop a mathematical model for the system. Chapter 5 provides a summary and recommendations. All detailed circuit diagrams are presented in Appendix A. Appendix B presents a cubic curve fitting algorithm used in plotting the data.

1-2 Description of the System

This section will provide a description of the operation of the variable pulse-rate vehicle speed control system. A detailed discussion of each subsystem will be given in the next chapter. The basic system consists of the following sub-systems:

1) The clock
2) Speed selector
3) Circular up/down binary counter
4) Acceleration and deceleration limit control
5) Stepping-motor logic circuit and power amplifier
6) Stepping-motor and clutch

7) Throttle linkage and limit switches
8) Pulse-rate tachometer
9) Power supplies

Figure 1-1 shows the interconnection of these sub-systems.

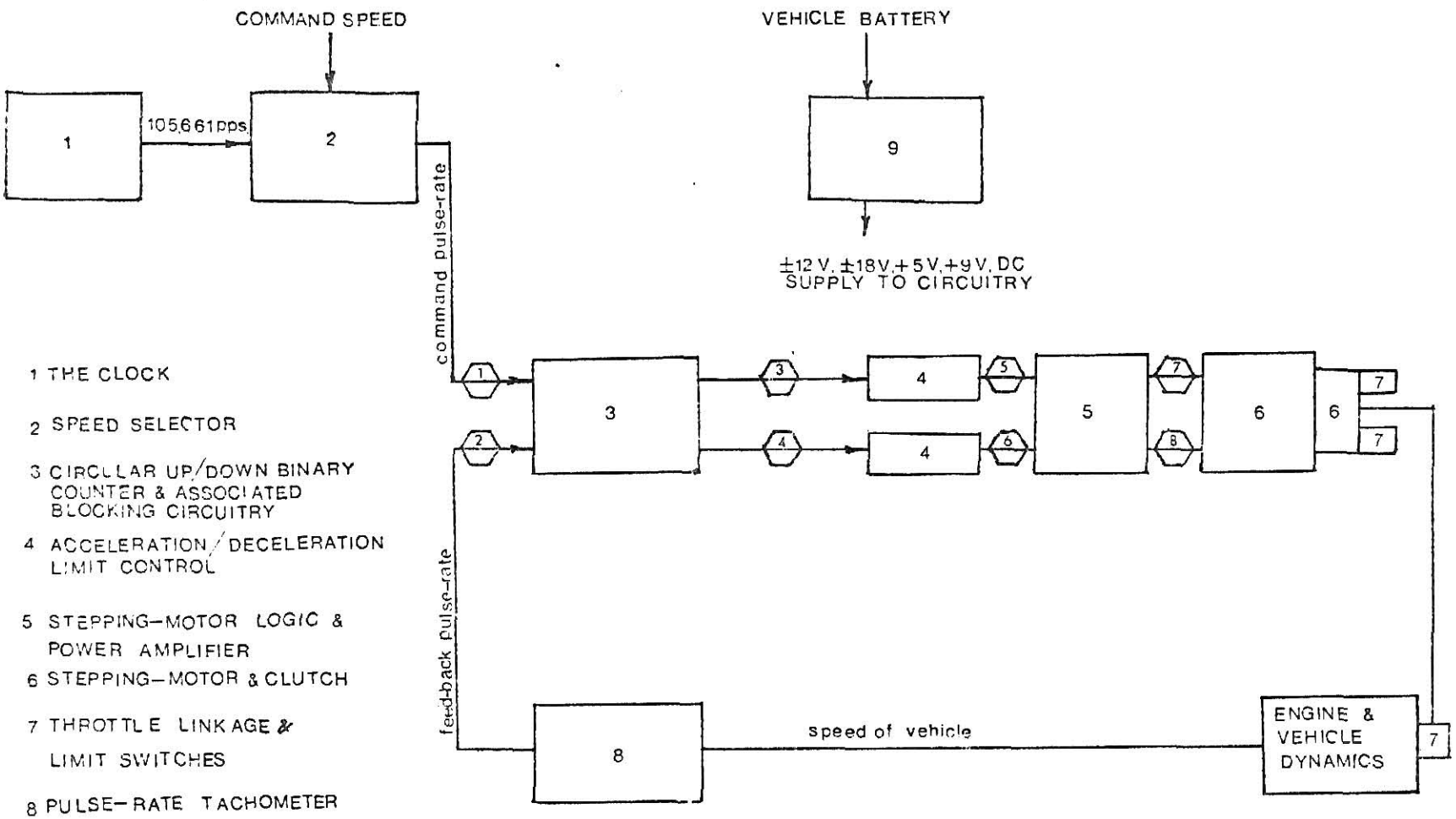
The clock is the basic source of the "command pulse-rate". The clock provides a train of pulses at a constant rate of 105,661 pulses per second. The clock signal passes to the speed selector.

The speed selector consists of a units speed selector and a tens speed selector. Both selectors are identical except for a divide by ten counter on the output of the units speed selector. The units speed selector enables one to select speeds from 0 to 9 mph in 1 mph increments and the tens speed selector enables one to select speed from 0 to 90 mph in 10 mph increments. Therefore, one can select any speed between 0 and 99 mph.

For the purpose of this investigation, only the tens speed selector has been implemented. Hence one can select 0 to 90 mph in 10 mph increments. Tens speed selection buttons along with indicator lights are mounted on the console.

The signal from the clock is divided down in the speed selector circuit by the necessary factor depending upon the command-speed. The signal from the speed selector to the up input channel of the up/down counter is referred to as the "command pulse-rate". The "command pulse-rate" is proportional to the command speed. The signal to the down input channel of this counter is the "feed-back pulse-rate", derived from the pulse-rate tachometer. The "feed-back pulse-rate" is proportional to the actual speed of the vehicle. Both pulse-rates have a proportionality constant of 106.67 pulses per second per mile per hour.

The up/down binary counter and associated circuitry, essentially takes the difference between the "command pulse-rate" and the "feed-back pulse-rate". If the "command pulse-rate" is greater than the "feed-back pulse-rate", a



VARIABLE PULSE–RATE VEHICLE SPEED CONTROL SYSTEM — FIGURE 1-1

stream of pulses with rate proportional to the difference between the two input signals will appear on the up output channel. The down output channel will be free of pulses. Conversely, if the "feed-back pulse-rate" is greater than the "command pulse-rate", the stream of pulses at a rate proportional to the difference between the two input signals will appear on the down output channel. The up output channel will be free of pulses. The constant of proportionality between the difference in the input pulse-rates and the output pulse-rates is the counter gain. The counter gain is adjustable by means of switches on the console. The up output channel is connected to the acceleration limit control circuit and the down output channel is connected to the deceleration limit control. In other words, this counter provides the error signals which are characteristic of feedback control systems.

The acceleration and the deceleration limit controls are independent, but identical circuits. The acceleration limit control receives a signal (pulse-rate) proportional to the error, when the error is positive. Similarly, the deceleration limit control receives the signal proportional to the error, when the error is negative. The purpose of this subsystem is to "limit" the pulse-rate to the stepping-motor. There are two reasons to limit the pulse-rate to the stepping motor. First, when large errors occur, like when there is a large change in command-speed, the pulse-rate exceeds the stepping rate capacity of the stepping motor. Second, the limit controls provide the capability to regulate the maximum rate the throttle is opened or closed; hence, the acceleration and deceleration rate of the vehicle. The limits are adjustable by means of a set of switches on the console.

The stepping-motor logic circuit converts the signal from the acceleration/deceleration limit controls into two square wave signals with a phase difference of $+90°$ or $-90°$. This phase difference controls the direction of

rotation of the stepping motor. The frequency of the square wave signals which is proportional to the puise-rate, controls the stepping rate of the stepping motor. The power amplifiers which follow this logic circuit, amplify the current capacity of the output signals of the logic circuit, so as to provide the current drawn by the stepping motor.

The two field windings of the stepping motor receive the signals from the power amplifiers. If one of the signals is leading the other by 90° the rotation of the stepping motor accelerates the automobile to a higher speed. Conversely, when the signal lags by 90°, the stepping motor rotates in the opposite direction. This will decelerate the automobile to a lower speed.

An electrically operated clutch is mounted on the stepping motor shaft. The output shaft of the clutch is connected to the throttle linkage. This shaft has a pointer which engages two microswitches at the two limits of travel of the throttle linkage. These two microswitches are referred to as "throttle limit switches".

A button on the console engages the clutch. The application of the brake of the automobile disengages the clutch. The disengagement of the clutch permits the throttle to return immediately to the idle position. The signal which controls the engagement of the clutch also operates on the stepping motor logic circuit to prevent the stepping motor from rotating while the clutch is disengaged.

The throttle limit switches prevent damage to the throttle linkage by limiting the travel of the stepping motor. When either of the limit switches is contacted by the pointer on the clutch output shaft, the appropriate signal in the stepping motor logic circuit is disabled to prevent further rotation in that direction. If the response of the vehicle is such that the system commands rotation in the opposite direction; the system returns to normal with no disabled signals.

The throttle linkage is composed of a tough cord and a small turnbuckle. The turnbuckle enables the adjustment of the tension in the cord which connects the clutch output shaft and the throttle linkage of the automobile. Rotation of the clutch shaft wraps the cord around the shaft and controls the position of the throttle.

The electrical power supply requirements for the system are +5, +9, ±12 and ± 18 volts DC. The +5 volt source supplies power to all the digital integrated circuits. The +9 volt source supplies power to the clock. The ±12 volt source supplies power to operational amplifiers used in processing the pulse rate tachometer signal and in the stepping motor logic circuit. The ±18 volt source supplies power to the stepping motor power amplifiers.

The +5 volt and +9 volt sources are obtained by zener diode regulated step down transistors on the +12 volt supply. The ± 12 volt and ± 18 volt sources are supplied by two dual regulated DC power supplies. For bench operation, these are powered by the conventional 60 cycle line. For road operation, power is derived from the automobile battery through a 60 cycle, 110 volts inverter.

1-3 Commercially Available Vehicle Speed Regulating System

Each of the three major American automobile manufacturing companies offers as optional equipment on their luxury models some form of speed regulator, commerically known as "cruise controls". All of these systems have certain common characteristics, yet each is different in some way. All of these regulators have pneumatic actuators. With each system the vehicle has to be brought to the desired speed by conventional accelerator pedal operation before the system can be engaged. The system then maintains that speed against the disturbances of hills and wind gusts until the set speed is adjusted or the system is disengaged. None of these systems provide

automatic braking to prevent over-speeding on steep downhill grades. Some of the particular operating characteristics of each type system are presented below.

i) GENERAL MOTORS:

a) Button on end of turn signal lever. (This button is depressed to engage while traveling at desired speed)

b) Hold button in to coast down to a reduced desired speed-- Release to hold speed.

c) Depress brake to disengage. Press button to reengage.

d) May use throttle to manually over-ride. Speed returns to previous setting after manual over-ride.

ii) CHRYSLER CORPORATION:

a) Button on end of turn signal lever, plus OFF-ON-RESUME switch (with this switch in ON position, depress the button to engage while traveling at desired speed.)

b) Hold button in to coast down to a reduced desired speed-- Release to hold speed.

c) Tap button to increase desired speed by 2-3 mph.

d) Depress brake to disengage. Press button to reengage.

e) Turn switch to resume to return to previous speed after brake disengagement.

f) May use throttle to manually over-ride. Speed returns to previous setting after manual over-ride.

g) May shut-off with OFF-ON-RESUME switch.

iii) FORD MOTOR COMPANY:

a) Rocker switches on each side of steering wheel.

b) Left rocker switch for ON-OFF. This switch turns the system on and off, but does not engage it.

c) Right rocker switch for accelerate-coast control. After

rocking the left rocker switch to the ON position, rocking the right rocker switch to either position engages the system at the current speed. Holding the right rocker switch in the accelerate position causes a slow steady acceleration of the vehicle. Releasing causes the system to lock on the current speed. Holding the rocker switch in the coast position permits the automobile to decelerate (coast). Releasing the switch to middle position causes the system to lock on the current speed.

d) May use throttle to manually over-ride. Speed returns to previous set-speed after manual over-ride.

e) Depress brake to disengage. Rock right rocker switch to either side to reengage.

None of these systems are capable of responding to an externally commanded speed. As a result, although they are convenient for regulating speed in the context of present driving systems, they are not amenable to the control that would be required in proposed futuristic systems where all automobiles are driven automatically and receive their speed control commands from some form of headway or spacing controller. The variable pulse-rate speed control system is capable of responding to an external speed command. The external command may call for an acceleration of the automobile to a higher speed or for a deceleration of the automobile to a lower speed.

Finally, the variable pulse-rate control system utilizes digital circuit elements which could be condensed by large scale integration techniques into very small, highly reliable, and inexpensive devices which might prove to be economically competitive, especially in the context of their expanded capability.

More detailed descriptions of each subsystem are provided in the next chapter.

CHAPTER 2

THE SUBSYSTEMS

CHAPTER 2

THE SUBSYSTEMS

2-1 INTRODUCTION

This chapter presents a detailed description of the design and function of each subsystem of the variable pulse-rate vehicle speed control system.

2-2 THE CLOCK

Figure A-1 represents the circuit diagram for the clock. The clock used for the system is a crystal oscillator type and provides a train of pulses at a constant rate of 105,661 pulses per second. It is possible to select other clock rates by replacing the crystal. This clock rate was used because of its availability and not because it represents the ideal rate for this application. A small error exists in the command speed pulse-rate as a result of the clock frequency not being specifically selected for this application. It turns out however, that this rate is a good compromise. Design with the ideal clock rate (2,688,000 pulses per second) requires significantly more elements in the speed selector circuit and is harder to work with because of the higher rate.

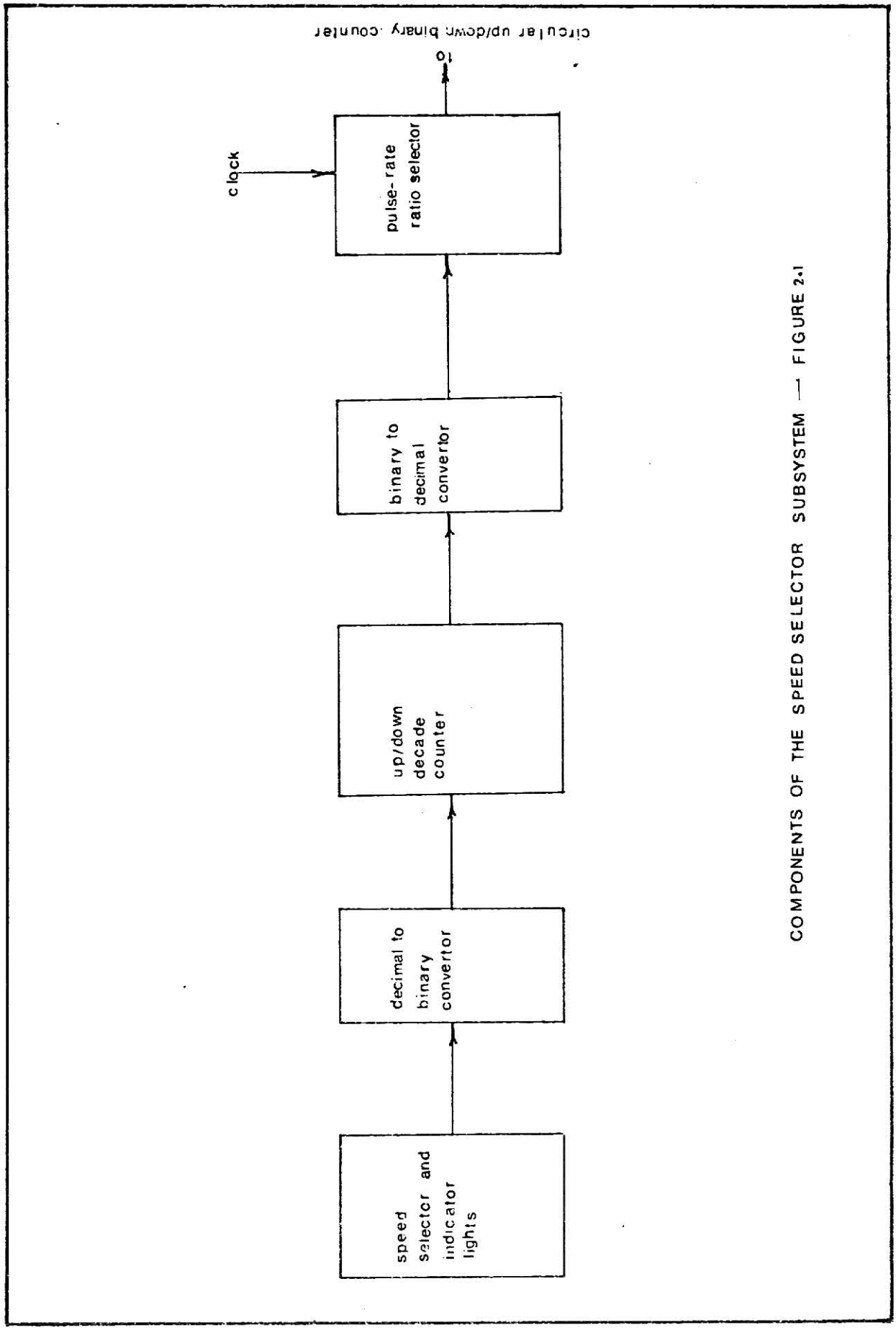
Specification of the Clock

Type: OT-1
Frequency Range: (22.2[illegible] Kz - 22.28 Mz)
Oscillator Crystal
Plate Volts: 9 volts dc, Current: 5mA
Mounting Plug-in T series
Manufacturer: International Crystal Mfg. Co., Inc.

2-3 SPEED SELECTOR

Figures A-3 and A-4 are the detailed circuit diagrams of the speed selector and Figure 2-1 shows the interconnection of the following components:

i) Command speed selection buttons with indicator lights.



COMPONENTS OF THE SPEED SELECTOR SUBSYSTEM — FIGURE 2.1

ii) Decimal to binary convertor.
iii) Up/down decade counter with parallel load.
iv) Binary to decimal convertor.
v) Pulse-rate ratio selector

i) Command speed selection button with indicator lights

The command speed is selected by depressing one of ten momentary contact push button switches on the console. An indicator light directly above the push button switch indicates the selected speed. These buttons enable the operator to select the desired speed between 0 to 90 mph in 10 mph increments. The original design included a units speed selector which would have included an additional ten push botton switches, indicator lights and other circuitry to provide speed settings between 0 and 9 mph in 1 mph increments. This would have provided a total range from 0 to 99 mph in 1 mph increments. The units speed selector was not implemented since it would have provided no additional information regarding the problems associated with the implementation of variable pulse-rate control system.

On Figure A-3 the push button switches are indicated by circles with numbers in them. Pushing one of these buttons delivers a +5 volt signal to the array of OR-GATES shown in the middle of the figure. These OR-GATES perform the function of converting the decimal value associated with the push button to a binary representation.

ii) Decimal to binary convertor

The decimal to binary convertor consists of the set of OR-GATES shown in the middle of Figure A-3. The binary representation of the decimal number associated with the push-botton switch is presented at the parallel load inputs (P_A, P_B, P_C, P_D) of the up/down decade counter designated M-16 in Figure A-3. At the same time, a signal is presented to the input of the single shot device designated M-19. This device generates a single clean pulse

which is used to trigger the parallel load control. The purpose of this device is to insure proper loading of the counter. Without this device, spurious results are obtained due to contact bounce in the switches and differences in accepted logic levels at different points in the circuit.

iii) Up/down decade counter

The up/down decade counter has a parallel load feature. When the parallel load control is triggered the value represented on the parallel load inputs (P's) is transferred to the counter outputs (Q's). The purpose of the counter in the original design was to provide the capability of increasing or decreasing the command speed with a rocker type switch like the one used on the cruise control marketed by Ford Motor Company. In this context depressing the accelerate switch would produce a slow stream of pulses to the up count input of the counter which would cause it to count up and increase the value of the command speed. Conversely, depressing the decelerate switch would cause the counter to count down and reduce the command speed. This operation was demonstrated on the bench. Since the unit speed selector was not implemented this feature was not included in the final model.

An additional function of this counter is to act as a latch for the command speed value. The signal from the push buttons is only present as long as the button is held down. When the corresponding binary value is loaded into the counter it is held until another value is loaded. The binary outputs of the counter are the inputs to the binary to decimal convertor.

iv) Binary to decimal convertor

The binary to decimal convertor designated as M-11 in Figure A-3 converts the binary representation of the command speed to decimal form. The output of the convertor provides the signal to illuminate the indicator lights and

to control the logic of the pulse-rate ratio selector circuit.

v) Pulse-rate ratio selector

The pulse-rate ratio selector is shown schematically in Figure A-4. The clock is the basic source of pulses for the pulse-rate ratio selector. This circuit divides the clock signal by the appropriate factor depending on the selected speed, e.g., if 30 mph is the selected speed, the output of the speed selector should be a pulse-rate of 3,200 pulses per second (106.67x30). Since the clock rate is 105,661 PPS, the required division factor is 33, i.e., one pulse in 33 pulses from the clock should be passed. To accomplish this the clock signal is counted by a pair of decade counters, designated M-4 and M-5 in Figure A-4. When the count reaches 33, the logic in the lower half of Figure A-4 is satisfied and a pulse is passed through it. At the same time, the two counters are reset to zero and the process starts over.

The count on the pair of decade counters is presented in binary coded decimal form on the eight outputs of the counters. These signals, together with the signals from the binary to decimal convertor are combined in the logic portion of the pulse-rate ratio selector to determine when a clock pulse should be passed through. Note that there is a slight error between the selected speed and the pulse-rate that is produced. The reason is that the clock rate is not an exact multiple of all possible selected speeds, e.g. for a selected speed of 30 mph, the nearest whole number division factor is 33. If, the clock rate of 105,661 PPS is divided by 33 and the result is again divided by 106.67 PPS/mph; a speed of 30.018 mph is commanded. Table 2-1 shows the division factor and the commanded speed for each selected speed. The percentage error is also shown for each case.

A clock rate of 2,688,000 PPS would make it possible to obtain all the

desired pulse-rates without error. This would require a great deal more circuitry in the pulse-rate ratio selector. For example, it would require four decade counters instead of two. The logic elements would also be increased significantly. Therefore, the present clock rate is a reasonable compromise between accuracy and expanded element count.

TABLE 2-1

COMMAND-SPEED MPH (SELECTOR PUSH BUTTON)	DIVISION FACTOR	COMMAND PULSE-RATE PPS/MPH	ACTUAL COMMAND-SPEED MPH	PERCENTAGE ERROR %
10.0	99	1067.290	10.006	+0.06
20.0	50	2113.233	19.812	-0.94
30.0	33	3201.867	30.018	+0.06
40.0	25	4226.465	39.018	-2.455
50.0	20	5283.091	49.529	-0.942
60.0	17	6215.398	58.269	-2.885
70.0	14	7547.398	70.757	+1.081
80.0	12	8805.152	82.548	+3.185
90.0	11	9605.606	90.053	+0.059

2-4 CIRCULAR UP/DOWN BINARY COUNTER

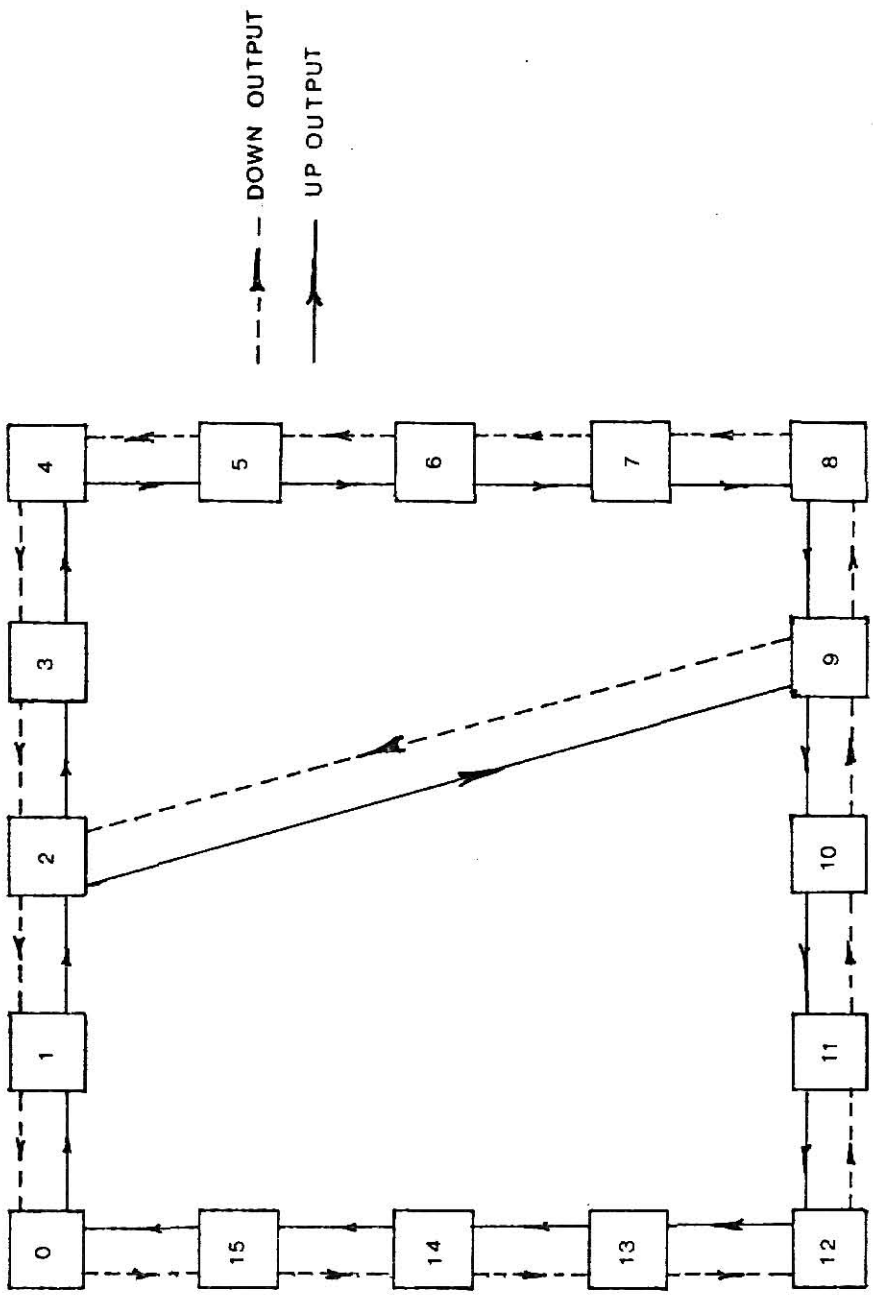
Figure A-2 provides the circuit diagram for the circular up/down binary counter and associated circuitry. This counter with its associated circuitry provides the error signals which are characteristic of feedback control systems. This subsystem is a most important element of the variable pulse-rate vehicle speed control system. It receives the "command pulse-rate" from the speed selector at its up input channel and the "feed-back pulse-rate" from

the pulse-rate tachometer at its down input channel. The counter and associated circuitry takes the difference between the "command pulse-rate" and "feed-back pulse-rate". The up output channel of this subsystem has a signal (pulse-rate) proportional to the error, when the error is positive and the down output channel has a signal (pulse-rate) proportional to the error when the error is negative. The ratio between the output pulse-rate and the difference between the input pulse-rates is the "counter gain". The counter gain is adjustable between the values 1/3 (0.333) and 1/15 (0.0666), by means of switches located on the console.

The operation of the circular up/down counter can be best explained by reference to Figure 2.2.

When pulses are presented on the up input channel of the counter, they cause the count to move progressively in the clockwise direction. Whenever the count passes from 15 to 0, a pulse appears on the up output channel of the counter. Conversely, when pulses are presented on the down input channel of the counter, they cause the count to move progressively in the counter-clockwise direction. Everytime the count passes from 0 to 15, a pulse appears on the down output channel of the counter. When pulses are presented on both the up and down input channels, the count moves in the appropriate direction with each pulse. Thus, if the pulse-rate on the up input channel is greater than the pulse-rate on the down input channel, the direction of the count is in the clockwise direction at a net rate equal to the difference between the input pulse-rates. Conversely, the direction of count is in the counter-clockwise direction when the pulse-rate on the down input channel is greater than the pulse-rate on the up input channel.

If the counting operation were a smooth and monotonic occurrance, the output signal would be a pulse-rate equal to the difference between the input



CIRCULAR UP/DOWN BINARY COUNTER — FIGURE 2·2

pulse-rates, divided by sixteen. The counting operation is not a smooth and monotonic occurrance as is evident from the following example. Suppose the pulse-rate on the up input channel is twice that on the down input channel. The count will then progress two counts in the clockwise direction followed by one count in the counterclockwise direction. This two counts forward, one count backward sequence continues around and around the cycle. At some point the sequence may be 13, 14, 13; 14, 15, 14; 15, 0, 15; 0, 1, 0; etc. This sequence would result in two pulses on the up output channel (each time the count passes from 15 to 0) and one pulse on the down output channel (each time the count passes 0 to 15). The pulse on the down output channel and the second pulse on the up output channel are spurious pulses which need to be eliminated to obtain the desired differencing function from the counter. To accomplish this objective, a pair of "blocking circuits" were developed.

The blocking circuits are shown in Figure A-2. They consist of the flip-flops designated M-11 and the AND-GATES designated M-6 and M-8 and they function as follows. The first pulse on the up output channel of the counter resets the flip-flop associated with the AND-GATE on the down output channel of the counter. This action blocks all subsequent pulses on the down output channel until the flip-flop is set. Similarly, the first pulse on the down output channel resets the flip-flop associated with the AND-GATE on the up output channel of the counter. This action blocks all subsequent pulses on the up output channel until the flip-flop is set. Both the flip-flops remain reset and the AND-GATES blocked until the count progresses around the cycle where both the flip-flops are set, unblocking the AND-GATES. The result is that the first output pulse is passed on each cycle of the counter and all subsequent output pulses are blocked until the counter progresses around the

cycle again. This logic is exactly the operation required to cause the counter to be a true error (differencing) device.

This counter also provides the function of an adjustable gain in the system. This is accomplished by using the parallel load feature of the counter to shorten the counting cycle from sixteen to any smaller number. The AND-GATES designated M-3 and M-4 with the associated switches, invertors and OR-GATES accomplish this function as follows. On the count of two and a pulse on the up input channel, the AND-GATE designated M-3 is "satisfied" and the counter is parallel loaded with the value set on the "up count gain switches". This bypasses the counter states between two and the value set on the switches, thus shortening the counting cycle. The "down count gain switches" would normally be set at the same value. When that value is present on the counter and a pulse appears on the down input channel, the AND-GATE designated M-4 is "satisfied" and the counter is parallel loaded with the value of two, bypassing the counter states and shortens the counting cycle. Therefore, by setting this pair of gain switches, any count cycle between fifteen and three can be achieved, providing an adjustability of gains between 1/3 (0.333) and 1/15 (0.0666). Table 2-2 gives the various gain values and the corresponding switch configuration. Setting the two sets of switches at different values might lead to spurious counter operation and should be avoided.

The setting of the blocking circuit flip-flop is accomplished using the parallel load signal. Therefore, the first output pulse on either of the counter output channels following the parallel load is passed through the blocking circuit with all subsequent output pulses being blocked until the occurrance of the next parallel load signal.

TABLE 2-2

"COUNTER GAIN" SWITCH-POSITIONS
(For Circular Up/Down Binary Counter)

	UP COUNT (Green Switches)				DOWN COUNT (White Switches)			
GAINS	S_1	S_2	S_3	S_4	S_A	S_B	S_C	S_D
1/2	U	U	U	U	-	-	-	-
1/3	D	U	U	U	D	D	D	D
1/4	U	D	U	U	U	D	D	D
1/5	D	D	U	U	D	U	D	D
1/6	U	U	D	U	U	U	D	D
1/7	D	U	D	U	D	D	U	D
1/8	U	D	D	U	U	D	U	D
1/9	D	D	D	U	D	U	U	D
1/10	U	U	U	D	U	U	U	D
1/11	D	U	U	D	D	D	D	U
1/12	U	D	U	D	U	D	D	U
1/13	D	D	U	D	D	U	D	U
1/14	U	U	D	D	U	U	D	U
1/15	D	U	D	D	D	D	U	U

NOTE: U = Up - Q position

D = Down - $\bar{Q}$ position

Q position = High (+5 Vdc - 1)

$\bar{Q}$ position = Low (GND - 0)

U = Up - $\bar{Q}$ position

D = Down - Q position

The function of the circular up/down binary counter and associated circuitry is to provide a signal (pulse-rate) proportional to the difference between the "command pulse-rate" and the "feed-back pulse-rate" multiplied by the "counter-gain". The "counter-gain" is adjustable by means switches on the console. The signal appears on the up output channel of the blocking circuit, if the difference between the pulse-rates is positive and on the down output channel of the blocking circuit, if the difference between the pulse-rates is negative. These signals pass to the acceleration and deceleration limit circuits respectively.

2-5 ACCELERATION AND DECELERATION LIMIT CONTROL

The purpose of the acceleration and deceleration limit control subsystem is to limit the pulse-rate to the stepping motor logic circuitry. There are two reasons to limit the pulse-rate. If the pulse-rate is not limited, there are circumstances when the pulse-rate exceeds the stepping-motor capacity, in which case, the stepping-motor does not step at all. Hence, the whole control system malfunctions. Furthermore, these circuits provide the capability to adjust the rate of throttle linkage motion; hence the acceleration and deceleration rates of the automobile. Figure A-5 provides a detailed circuit diagram of the limit control circuits. This subsystems consists of

i) Acceleration limit control.
ii) Deceleration limit control.
iii) Clock dividing circuit.

The acceleration and deceleration limit control circuits are identical but independent. Each circuit consists of a binary counter, a flip-flop, four AND GATES and a set of switches.

The limit control circuit is presented in Figure A-5. The clock dividing circuit (Figure A-6) is a pair of counters which divide down the

clock signal (105,661 PPS) to a slower clock signal (660.68 PPS). This slower clock signal is used to time the interval when the limit control circuit prevents pulses from passing to the stepping-motor logic circuitry. The first pulse coming from the circular counter and its associated circuitry, is passed to the stepping-motor logic circuit. This pulse also causes the flip-flop designated M-7 to change state closing the AND GATE designated M-4 at the top center of Figure A-5 preventing further pulses from passing to the stepping-motor logic circuit. At the same time, the flip-flop output causes AND_GATE M-4 at the bottom center of the figure to pass the slow clock signal to the counter designated M-6. The counter counts until the value set on the switches is reached. At this time the flip-flop and the counter are reset. The resetting of the flip-flop enables the AND-GATE to pass the next pulse from the circular counter to the stepping-motor logic circuit and prevents the slow clock signal from entering the limit counter. The next pulse from the circular counter restarts the cycle. During the time, the limit counter is counting any additional pulses coming from the circular counter are simply lost. Therefore, the selection of the slow clock signal rate and the value to which the counter counts, regulates the maximum pulse-rate passing to the stepping-motor logic circuit. Table 2-3 shows the pulse-rate limits and the corresponding switch configurations for both the acceleration and deceleration limit control.

The AND-GATES designated M-2 and M-1 inhibits the signals to the stepping motor logic circuit if the throttle linkage limit switches are engaged or the clutch is disengaged. The output of these AND-GATES are the inputs to the stepping motor logic circuit.

TABLE 2-3

"LIMIT SWITCH" - POSITIONS
(For Acceleration and Deceleration Limit Controls)

MAXIMUM PULSE-RATE	RATIO	ACCELERATION LIMIT CONTROL (Yellow Switches) S_1	S_2	S_3	S_4	DECELERATION LIMIT CONTROL (Red Switches) S_5	S_6	S_7	S_8
44.44	1/15	-	-	-	-	U	U	U	U
47.62	1/14	U	D	D	D	U	U	U	D
51.28	1/13	D	U	D	D	U	U	D	U
55.56	1/12	U	U	D	D	U	U	D	D
60.60	1/11	D	D	U	D	U	D	U	U
66.67	1/10	U	D	U	D	U	D	U	D
74.00	1/9	D	U	U	D	U	D	D	U
84.00	1/8	U	U	U	D	U	D	D.	D
95.00	1/7	D	D	D	U	D	U	U	U
111.11	1/6	U	D	D	U	D	U	U	D
133.00 *	1/5	D	U	D	U	D	U	D	U
166.00	1/4	U	U	D	U	D	U	D	D
222.00	1/3	D	D	U	U	D	D	U	U
333.00	1/2	U	D	U	U	D	D	U	D
666.67	1/1	D	U	U	U	D	D	D	U
PASSES ALL		U	U	U	U	D	D	D	D

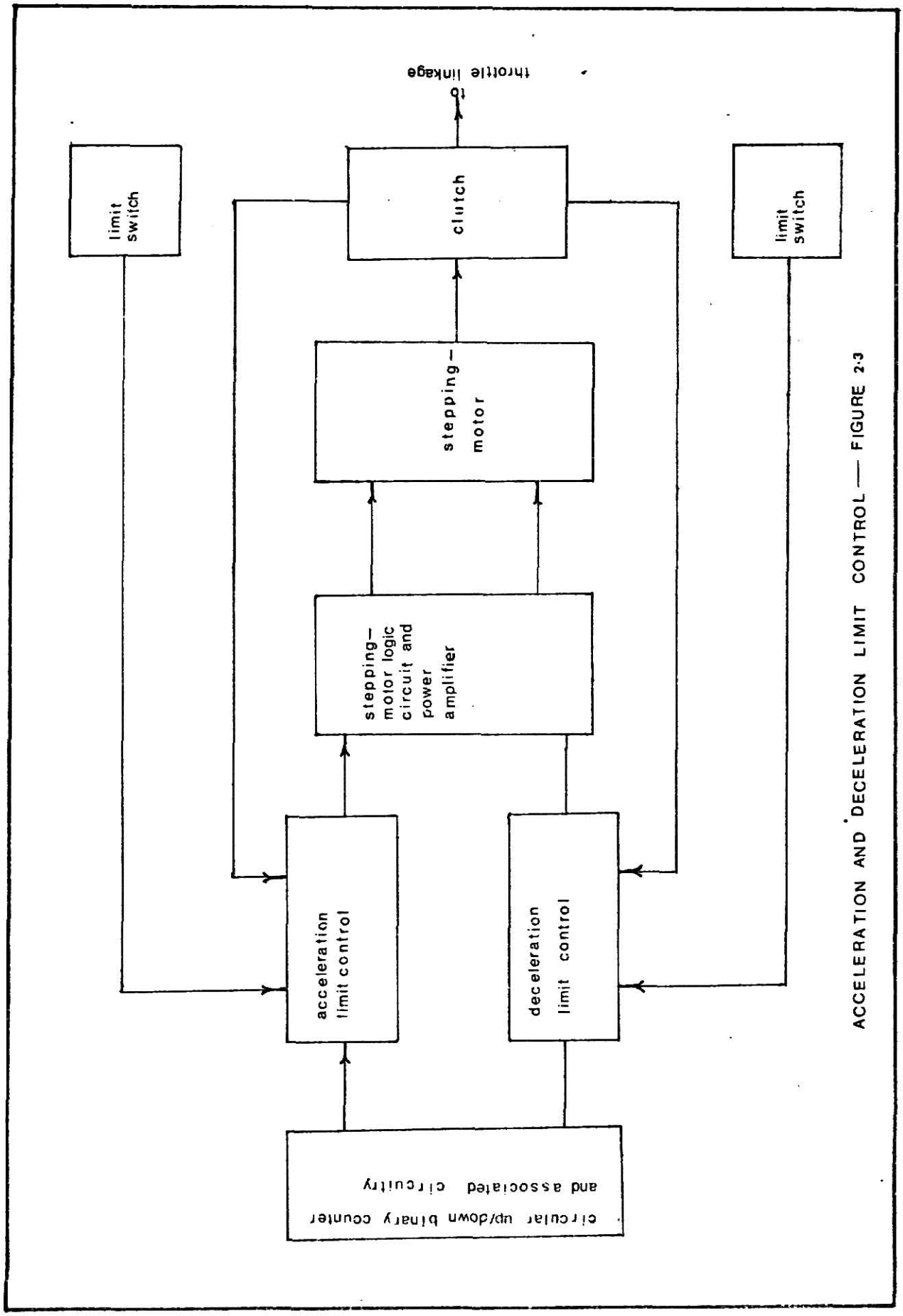
NOTE: U = Up - Q position U = Up - $\bar{Q}$ position

D = Down - $\bar{Q}$ position D = Down - Q position

Q position = High (+5 Vdc - 1)

$\bar{Q}$ position = Low (GND - 0)

*Beyond this pulse-rate, stepping motor loses its capability to step.



ACCELERATION AND DECELERATION LIMIT CONTROL — FIGURE 2-3

2-6 STEPPING-MOTOR LOGIC CIRCUIT AND POWER AMPLIFIER

The stepping motor logic circuit perform the function of converting the pulse signals into square wave signals with the correct frequency and phase relationships to control the direction and stepping rate of the stepping motor. These square wave signals are amplified in power amplifiers capable of providing the current necessary to drive the stepping motor.

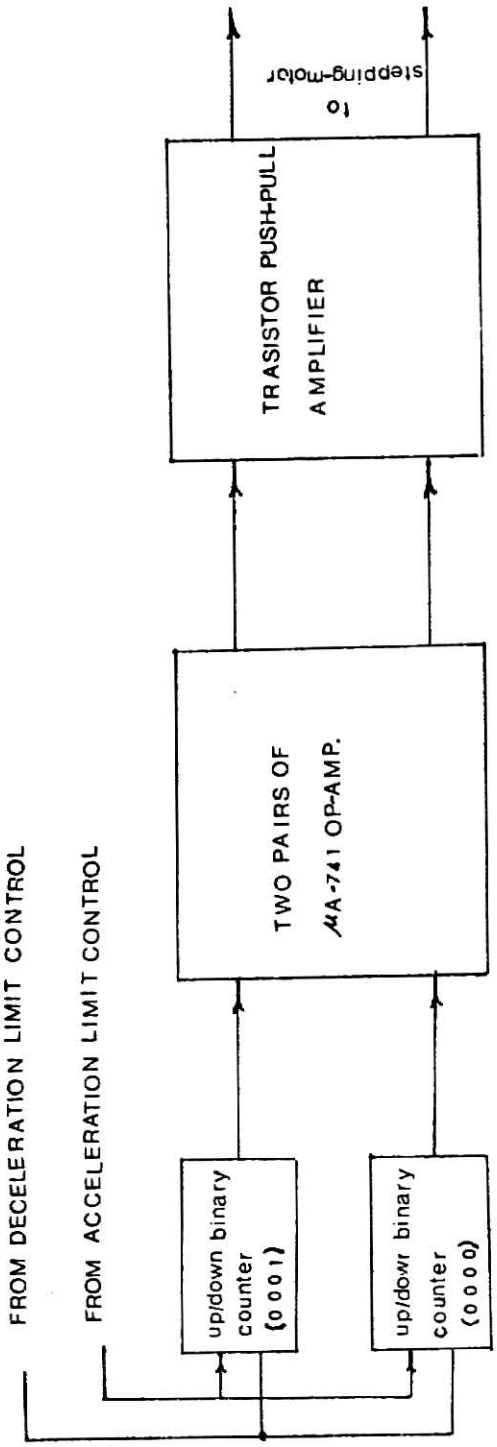
Figures A-7 and A-8 give the detail circuit diagrams of this subsystem and Figure 2-4 shows the interconnection of its components. These components are:

i) Stepping motor logic circuit.
ii) Two pairs of μA-741 operational amplifiers ($\pm$ 12 volts dc).
iii) Power amplifiers.

i) Stepping-motor logic circuit

Figure A-7 is a detailed circuit diagram of the stepping motor logic circuit. It consists of two up/down binary counters, three invertors and one AND-GATE. The purpose of these counters is to convert the signals from the acceleration and deceleration limit control circuits into two square wave signals; such that one signal leads the other by a phase of 90°. When the signal comes from the acceleration limit control circuit to the up-input channels of the two counters the phase of the square-wave signals is such that the stepping motor rotates to increase the throttle opening. Conversely, when the signal comes from the deceleration limit control circuit to the down input channels of the two counters, the phase is opposite and the stepping motor rotates to decrease the throttle opening.

This is achieved by connecting the two counters such that one starts counting from 0,1,2,3,... (i.e. it is initially set at the binary number 0000) and the other starts counting from 1,2,3,4,... (i.e. it is initially set at the binary number 0001). The up input channels of both counters receive the



STEPPING– MOTOR LOGIC CIRCUIT AND POWER AMPLIFIER — FIGURE 2.4

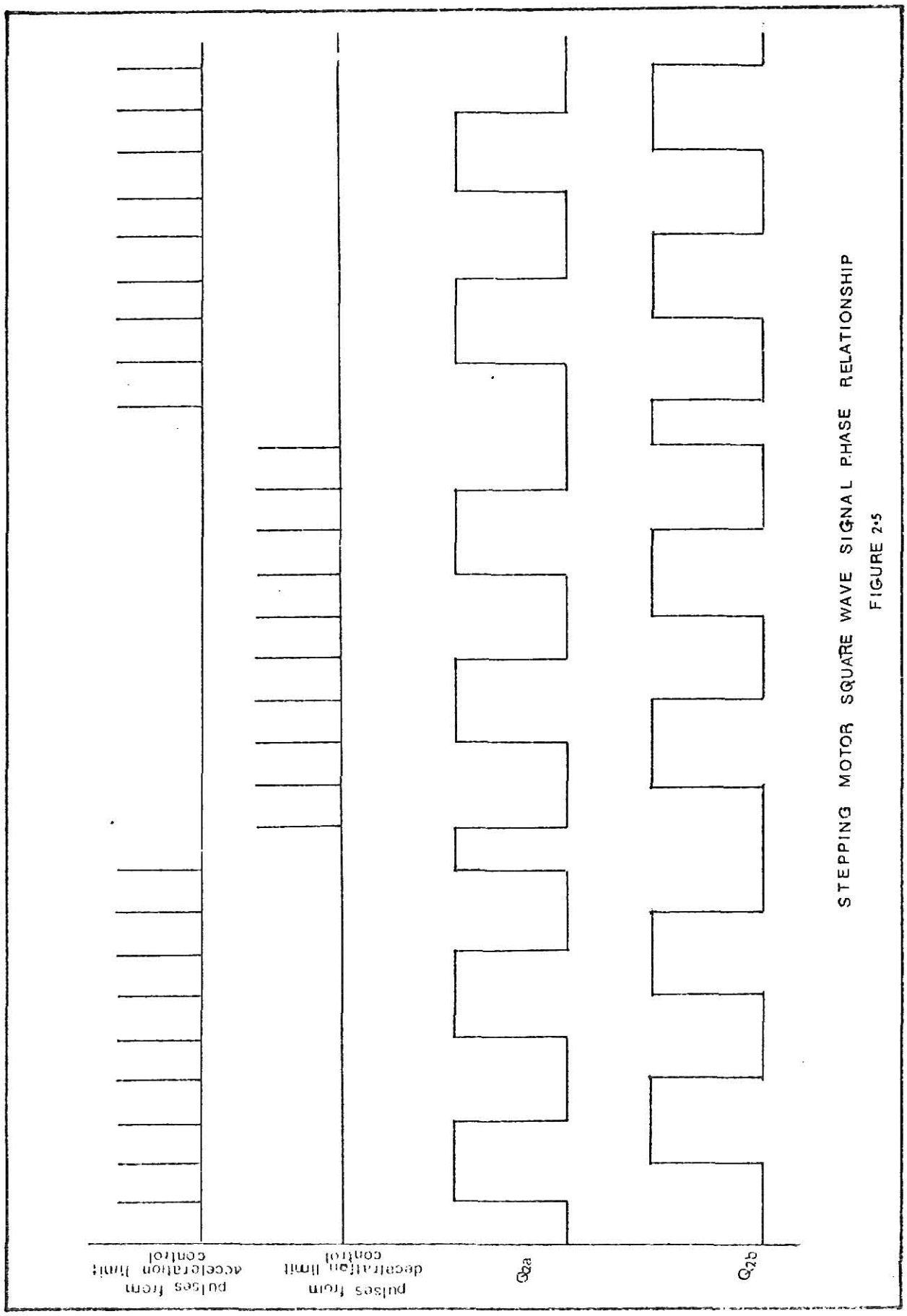
signal from the acceleration limit control circuit and the down input channels receive the signal from the deceleration limit control circuit. The two square-wave signals are taken from the second digit of the binary representation of the count on the counter. Table 2-4 shows the binary counting sequence for both counters while Figure 2-5 illustrates the phase relationship between the signals. The AND-GATE designated M-12 is to insure that the phase relationship is maintained between the signals. If the counters miss a count and lose their phase relationship, the AND-GATE circuitry resets the counters to binary numbers 0000 and 0001 respectively, restoring the proper phase relationship.

ii) Two pairs of μA-741 operational amplifier ($\pm$ 12 volts dc)

There are two pairs of μA-741 operational amplifiers. The first pair have a bias voltage applied to center the 0 to 5 volt input signals. They each amplify the signals to a 12 volts square wave. The first pair has a gain of 2.2 and the second has an adjustable gain of 4. The detail circuit diagram is given in Figure A-7.

iii) Power Amplifiers ($\pm$ 18 volts dc)

The system utilizes a pair of identical power amplifiers. Each amplifier consists of a μA-741 control amplifier driving a pair of complimentary push pull transistor stages connected in a darlington configuration. Figure A-8 gives a detail circuit diagram of the amplifier. The transistors are complimentary pairs to provide equivalent operating characteristics for positive and negative inputs and a smooth transistion at crossover. The power supplies to both the control amplifier and the transistors is $\pm$ 18 volts. The control amplifier provides stability and a quick, smooth response while the transistors provide current amplification.



STEPPING MOTOR SQUARE WAVE SIGNAL PHASE RELATIONSHIP

FIGURE 2-5

TABLE 2-4

STEPPING MOTOR LOGIC COUNTER SEQUENCE

Remarks	Q_{2B}				Q_{2A}			
ACCELERATION ↓	0	0	0	0	0	0	0	1
	0	0	0	1	0	0	1	0
	0	0	1	0	0	0	1	1
	0	0	1	1	0	1	0	0
	0	1	0	0	0	1	0	1
	0	1	0	1	0	1	1	0
	0	1	1	0	0	1	1	1
	0	1	1	1	1	0	0	0
	1	0	0	0	1	0	0	1
	1	0	0	1	1	0	1	0
↑ DECELERATION	1	0	1	0	1	0	1	1
	1	0	1	1	1	1	0	0
	1	1	0	0	1	1	0	1
	1	1	0	1	1	1	1	0
	1	1	1	0	1	1	1	1
	1	1	1	1	0	0	0	0

The amplifiers were designed and built specifically for this application.

2-7 STEPPING MOTOR AND CLUTCH

The detailed circuitry of the stepping motor and clutch is given in Figure A-9. The rotation (stepping) of the stepping motor pulls the throttle linkage against its return spring causing acceleration of the automobile. Rotation of the stepping motor in the opposite direction permits the throttle linkage to retract causing decleration of the automobile.

The stepping motor used is a 120 volt, 1 Amp, 60 Hz AC motor, but it has been modified to operate at a lower voltage. The $\pm$ 18 volt signal is still far below the specification value, but it does provide sufficient voltage to give a positive driving torque which is adequate to the need. The stepping motor has an integral gear box with a 4.0625 step down gear ratio. The stepping motor requires 200 steps (pulses) per revolution. With the gear box the output shaft requires (200 x 4.0625) 812.5 pulses per revolution.

An electrically controlled clutch is attached to the output shaft of the gear box. The clutch provides a quick and foolproof method of disengaging the system. The output shaft of the clutch actuates the throttle linkage.

The Specification of the Clutch

Code: SO 11-4-3-03

Manufactured by: Inertia Dynamics Inc.

Unit Type: SO; Size: 11; Torque: 6 lb-in

Voltage: ± 12 volts dc

Rotor Bore: 0.25 in

Armature Hub Bore: 0.25 in

Armature Hub Drive Type: Zero backlash drive

When the clutch push-botton on the console is pushed, -12 volts dc is supplied to one of the common terminals of relay 4 through its normally closed terminal. The common terminal of relay 4 is connected to the field coil at relay 3. One of the two normally open terminals of relay 3 is connected to -12 volts dc and the other to +12 volts dc. Its common terminal is connected to the clutch.

Operating the console button, -12 volts dc energizes relay 3 through normally closed relay 4. -12 volts dc on one of the normally open terminal keeps relay 3 closed while +12 volts dc on the other normally open terminal of relay 3, engages the clutch and latches it.

When the brake is depressed, relay 4 is energized by the +12V supply, which cuts off the -12V supply to relay 3, shutting off +12V supply to the clutch winding. This disengages the clutch, permitting the throttle linkage to return to idle position.

2-8 THROTTLE-LINKAGE AND THROTTLE LIMIT SWITCHES

The circuit diagram of the throttle limit switches is provided in Figure A-5. The motion of the stepping motor actuates the throttle linkage by wrapping a flexible cord around the output shaft of the clutch. The shaft

is 0.25 inch in diameter, so that the throttle linkage motion is 0.7854 inches per revolution of the clutch shaft. A small turnbuckle on the cord provides for easy adjustment of the cord tension.

Two limit switches are mounted so as to be actuated at the extremes of the motion of the throttle linkage. They prevent the over-stepping of the motor in either direction. The limit switches are actuated by a pointer attached to the clutch output shaft. When the pointer actuates either of the limit switches, the resulting signal blocks the corresponding pulse signal into the stepping motor logic circuit. Signals on the other channel are still passed to permit the system to come off the limit switch when it has responded to the condition where rotation in the opposite direction is commanded.

2-9 PULSE-RATE TACHOMETER

Figure A-2 provides the circuitry associated with the pulse-rate tachometer. The pulse-rate tachometer is the feedback device of this control system. It consists of

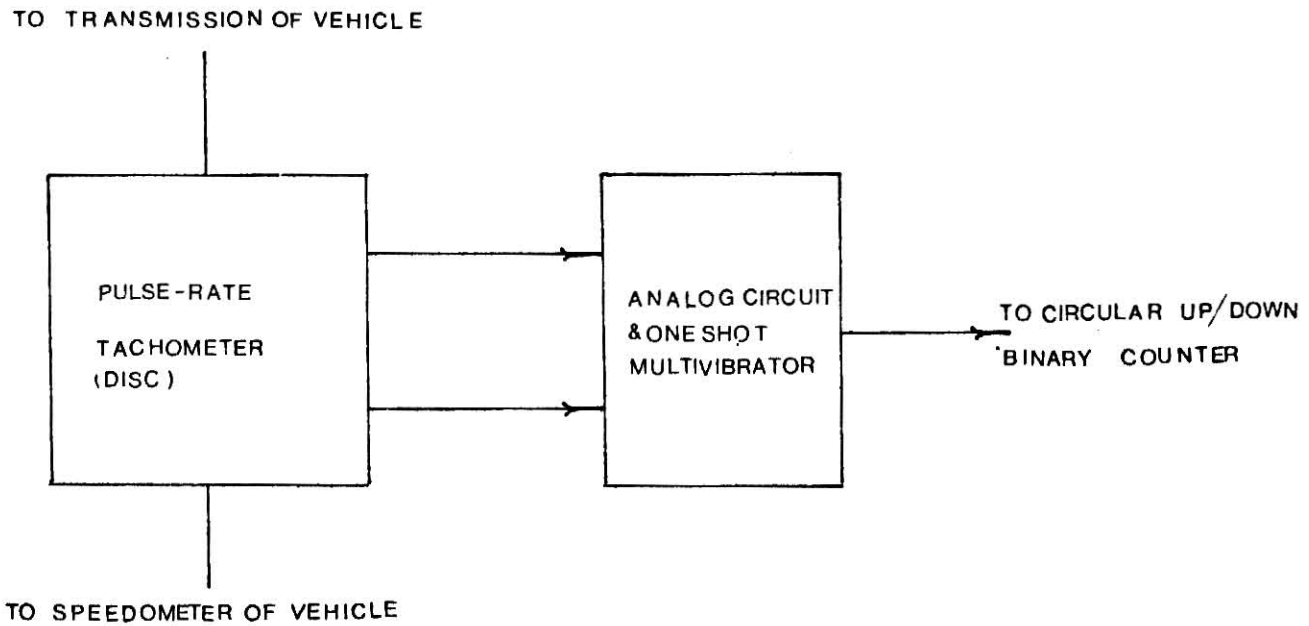
i) Tachometer.

ii) Analog circuit.

Figure 2-6 shows their interconnection.

i) Tachometer

The tachometer consists of a 5 in diameter, 1/8 in thick black plastic disc mounted on a bearing supported shaft. The disc has 96 slots around its periphery. The shaft is connected to the speedometer cable so that it rotates at a rate proportional to the speed of the vehicle (0.277 revolutions per second per mile per hour). As the disc rotates, it passes the slots between



FEED BACK SYSTEM — PULSE-RATE TACHOMETER — FIGURE 26

a pair of photodiodes mounted about 180° to each other on the bracket. Every-time the slot on the disc passes a photodiode it generates a signal. These signals are summed and shaped by the analog circuit. The analog circuit produces four pulses for each slot in the disc, thus providing 384 pulses per revolution or a pulse-rate of 106.66 pulses per second per mile per hour. The signal from the tachometer is the "feed-back pulse-rate" proportional to the automobile speed. It passes to the down input channel of the circular counter discussed in section 2-4.

Feedback Pulse-Rate Calculation

Number of slots on the disc periphery = 96

Number of pulses per slot = 4

Total number of pulses per revolution of the pulse-rate tachometer

= 96 x 4

= 384 pulses/rev

Number of revolutions per mile = 1000

Number of pulses per second per mph = $384 \times \frac{1000}{3600}$

= 106.66 pps/mph

ii) Analog Circuit

The analog circuit has three μA741 operational amplifiers and three potentiometers. It sums and shapes the signals generated by rotation of the tachometer. The one-shot multivibrator at the output of this circuit develops sharp and clean pulses from the analog signals.

2-10 POWER SUPPLIES

Figure A-10 provides the circuit diagram of the power supplies. The control system requires a ± 18 volt dc supply for the power amplifier, a

± 12 volt dc supply for the operation of the clutch, the operational amplifiers and for power supplies that provide + 9 volts dc for the clock circuitry and + 5 volts dc for the entire integrated logic circuitry. Both supplies are switched and fused to protect the circuitry.

All of the subsystems described in this chapter were tested in bread board form before being hard wired. Each subsystem was tested as it was integrated into the system. The entire system was extensively bench tested before it was installed in the vehicle. The system was tested in the vehicle both in the garage and on the highway. Chapter 3 presents the results of these tests while Chapter 4 discusses a mathematical model based on the test results. Figures A-11 to A-13 in Appendix A are the layout diagrams for the cards 1, 3 and 4.

CHAPTER 3

EXPERIMENTAL WORK AND TESTING

CHAPTER 3

EXPERIMENTAL WORK AND TESTING

3-1 INTRODUCTION

During the fabrication of the system a certain amount of experimental work was carried out. This involved bench testing of components, subsystems and the system as a whole. After thorough bench testing of the control system, it was installed in the vehicle and road testing was carried out. This chapter describes the tests that were conducted and presents the results of these tests.

3-2 BENCH TESTING

Each component and subsystem was first assembled on a bread board and was subjected to extensive testing before it was hardwired. As each subsystem was developed on the bread board, it was connected into the previously completed subsystem so as to insure compatability. All electronic components were mounted in sockets which provided for easy replacement and testing.

During subsystem assembly and testing many things were learned as modifications were required to obtain the desired performance. The blocking circuit developed to eliminate the spurious pulses on the outputs of the circular counter is an example. Another example which occurred several times has to do with the resetting of counters. Counters are used in several subsystems to count the pulses on a signal. When a predetermined count is reached, a pulse is passed to cause some action within the system and the counter is reset. Typically the pulse that is passed and the resetting pulse are derived from a set of logic gates which are satisfied when the predetermined count is reached. As the count is reached and the gates are satisfied, the reset pulse rises and rests the counter so that the gates are no longer

satisfied. Since the gates are no longer satisfied the pulse is cut off. This happens very fast and as a result the reset pulse is very, very short in time duration and frequently not of full voltage magnitude. In many cases, this pulse is not satisfactory for the action it was intended to cause. In most cases, this problem was solved by the addition of a one-shot multivibrator device. The logic gates trigger the one-shot multivibrator and its output which is a clean and sharp pulse is used to reset the counter as well as for any other purpose required. By selecting proper resistance and capacitance values, the time duration and amplitude of the multivibrator output pulse can be controlled independent of time duration and amplitude of the input pulse.

In the early stages of the project it was learned that the input terminals of the integrated circuit elements, if not being used, should be tied to either ground (Gnd) or Vcc (+5 volts dc) rather than being left open.

Several other practical lessons were learned while working on this project. Some of these are as follows:

1. a. It is helpful to make a list of connections from the circuit diagram. It is easier to wire the circuit from the list than from the circuit diagram. The list should include every pin of every socket.

   b. It is very important to correct this list immediately if a modification is made in the circuit.

   c. It is very helpful to make a layout diagram of the board on which the hard wiring is done, along with proper identification of components and terminals.

2. a. It is better to take the time to make a good connection the first time than to try to find and repair a bad connection after the board is wired. A good connection is essentially done by wrapping the wire around the pin or terminal and then solder it and not by just soldering the wire to the side of the pin. It saves a lot of time and trouble in the long run.

   b. It is worth the effort to place wires neatly on the board using square type bends and horizontal and vertical runs rather than direct pin to pin runs.

c. It is very easy to work with solid teflon coated hook-up wire.

3. Defective components or hardware should be clearly marked or disposed of immediately. It prevents them from getting mixed with good components or being put back into the circuit by mistake.

4. All wired boards should be carefully secured well into its proper places to prevent either connection or component coming loose. Especially in this automobile speed control application the automobile vibrations are hard on board connectors or sockets.

Following the fabrication of the entire system a bench test simulation was conducted. A DC motor was connected to the pulse-rate tachometer and a potentiometer was connected to the clutch output shaft. An electrical filter with time constant approximately equal to the expected time constant of the vehicle was installed between the potentiometer and the power amplifier used to drive the DC motor. This simulation successfully demonstrated the operation of the entire system. Stable operation was obtained. It was, however, observed during these tests that the system became quite oscillatory when the system gain was increased. At this time in the project very little was known about the response characteristic of the automobile. A very simple test to approximate the time constant and the gain of the vehicle was conducted. The response to step changes in the throttle setting were obtained using a stopwatch and the speedometer. The throttle changes were measured with a ruler. An attempt was made to match a simple model assumed at this time, to these bench tests. The gain of 160 mph/inch and time constant of 15 seconds were approximated on the electrical filter and DC motor.

During the bench testing, the operation of all the gain and limit control switches was varified. For this purpose a pulse generator (Interstate Electronic Corporation, Model F-34) was substituted for the pulse-rate tachometer. The pulse-rates were measured with a Beckman Corporation model 6146 counter. A large number of tests were conducted. Tables 3-1, 3-2, 3-3, and 3-4 are typical of the data taken during these tests.

Table 3-1 is typical of the sets of readings obtained for the up-channel counter gain.

Table 3-2 is typical of the sets of readings obtained for the down-channel counter gain.

Table 3-3 is typical of the sets of readings obtained for the acceleration limit control.

Table 3-4 is typical of the sets of readings obtained for the deceleration limit control.

3-3 ROAD TESTING

After satisfactory bench testing the control system was installed in the vehicle. It was powered by regulated power supplies that supplied ± 12 volts dc and ± 18 volts dc. These power supplies were powered by the automobile battery through a convertor which supplied 60 cycle, 120 volts power.

The first tests conducted in the vehicle were made in the garage, with the rear wheel of the vehicle lifted off the ground. The system was operated this way to provide the ability to use laboratory instruments to observe the signals to insure proper operation. The vehicle characteristics were, of course, not similar to what would be expected on the highway. The basic operational functions were observed, although the system appeared to be operating in a limit cycle mode. No specific data was taken during these tests.

Following the garage tests, the system was tested on the highway. The instrument used to record the response of the system on the highway was a battery powered "Event per Unit Time/Time Between Events (EUT/TBE)" digital instrument built for this purpose. The instrument provides a four digit display of the time between events or the number of events per unit time. Various rates can be selected by switches provided on the instrument. In EUT

TABLE 3-1

UP CHANNEL COUNTER GAIN

Command Speed MPH	Beckman Count Reading μsec	Actual Pulse Rate PPS/MPH	Actual Speed MPH
10	9369.537	1067.200	10.005
20	4732.090	2113.231	19.812
30	3123.180	3201.865	30.018
40	2366.046	4226.461	39.623
50	1892.837	5283.075	49.529
60	1608.911	6215.338	58.269
70	1324.986	7547.352	70.756
80	1135.702	8805.127	82.548
90	1011.061	9605.585	90.052

Up channel counter gain = 1/10 (0.1)

TABLE 3-2

DOWN CHANNEL COUNTER GAIN

Down Channel Counter Gain	Feedback Pulse-Rate Send PPS	Beckman Counter Reading μsec	Actual Feedback Pulse-Rate PPS
0.10	45.555	22087.746	45.274
0.10	90.909	11093.852	90.140
0.10	70.00	14485.450	69.035
0.10	110.00	9221.734	108.439
0.20	100.00	9988.540	100.115
0.20	200.00	5069.063	197.275
0.20	140.00	7159.035	139.683
0.20	220.00	4600.823	217.352

TABLE 3-3

ACCELERATION LIMIT CONTROL

Command Speed MPH	Beckman Counter Reading μsec	Actual Pulse-Rate PPS
10	14991.2	66.706
20	15142.6	66.039
30	14241.6	70.217
40	15142.6	66.039
50	13628.4	73.376
60	13643.5	73.295
70	13567.8	73.704
80	13628.4	73.376
90	13575.3	73.663

Acceleration Limit Control: 74.0 PPS

Up Channel Counter Gain: 1:8

TABLE 3-4

DECELERATION LIMIT CONTROL

Deceleration Limit PPS	Feedback Pulse-Rate Send PPS	Beckman Counter Reading μsec	Actual Pulse-Rate PPS
66.67	250.00	16046.9	62.3
	300.00	16698.7	59.8
	333.33	15172.6	65.9
	500.00	15275.4	65.4
47.62	250.00	22863.9	43.7
	300.00	22697.4	44.0
	333.33	21255.2	47.0
	500.00	21323.7	46.8

setting, with 4 seconds hold time, the instrument samples a pulse-rate signal for one second and displays (holds) it for 4 seconds. Hence, it was possible to measure the automobile speed every five seconds.

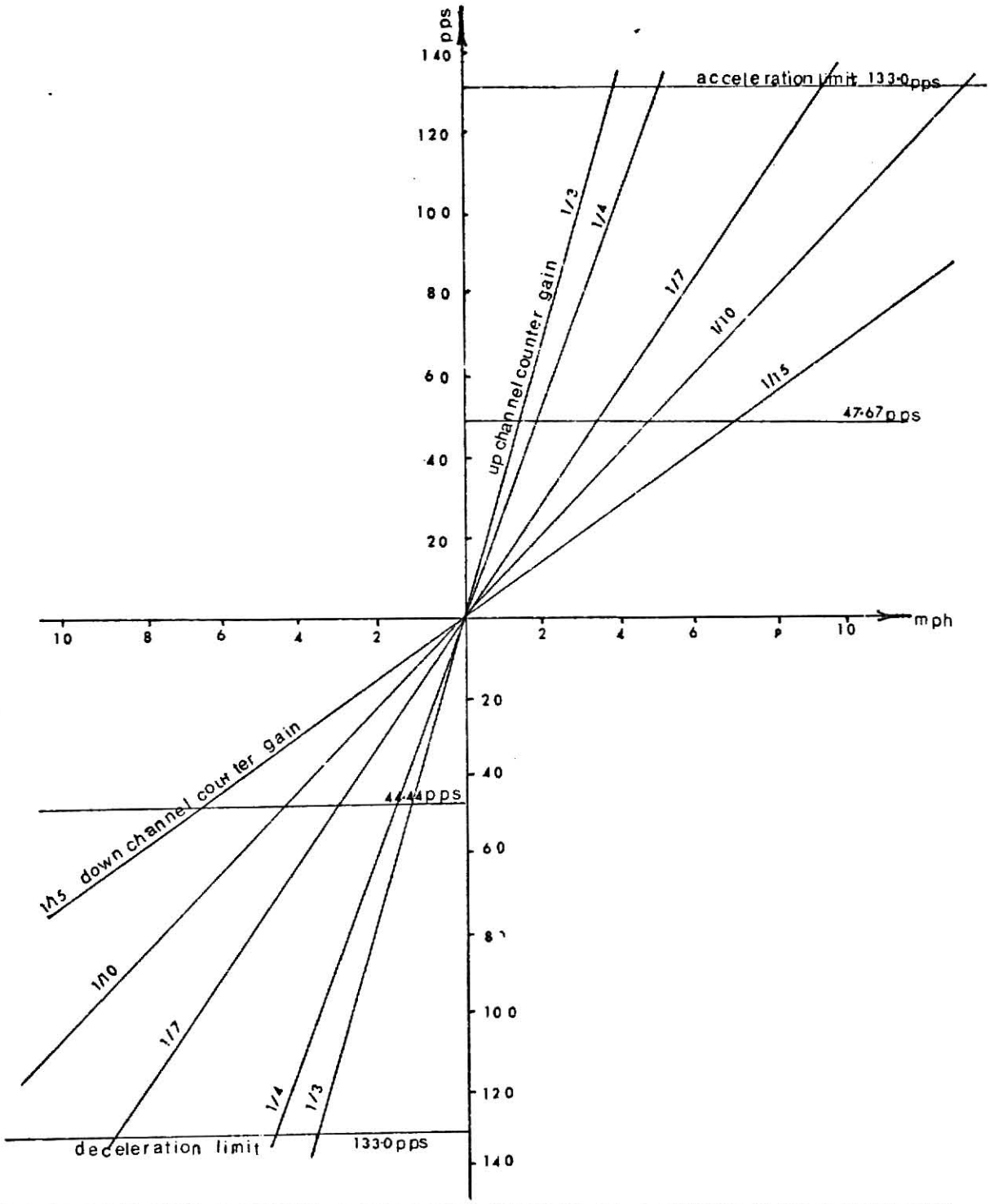
The purpose of the highway testing was to evaluate the performance of the system for various circular counter gains and acceleration/deceleration limits and at various command speeds.

Figure 3-1 shows the effect of circular counter gain and acceleration/deceleration limit values on the pulse-rate into the stepping motor logic circuit as a function of the difference between the command speed and measured speed. The system's response was evaluated at various gain and limit settings and various command speeds.

The response of the system as displayed on the EUT/TBE instrument was recorded by voice on a tape recorder. At the beginning of each run, the test conditions were recorded followed by the values read on the instrument each five seconds. Each test was conducted from a stationary condition with the system providing the transient from zero to the commanded speed. The data was later transcribed and punched onto computer cards for machine evaluation and plotting.

3-3 ANALYSIS OF DATA

The data obtained from the road tests was plotted as shown in Figure 1 to 25 at the end of this chapter. These plots were drawn with the help of the computer. A cubic curve fitting algorithm was developed to provide a smooth curve between the data values. The curve fitting algorithm selects the coefficients of a cubic polynomial to draw the curve between the i^{th} and the $(i + 1)^{st}$ data points. The coefficients are selected so that the curve passes through i^{th}, the $(i + 1)^{st}$ and the $(i + 2)^{nd}$ data points and has a continuous slope at the i^{th} data point with the curve drawn between the



PULSE-RATE INTO STEPPING MOTOR LOGIC CIRCUIT AS A FUNCTION OF DIFFERENCE IN COMMAND SPEED AND MEASURED SPEED FOR VARIOUS GAIN AND LIMIT VALUES

FIGURE 3-1

$(i - 1)^{st}$ and the i^{th} data points. This provides a smooth continuous curve through all the data points as may be observed from the plots. The equations for the algorithm are provided in Appendix B.

All the plots were examined. It was observed that there was no pattern or trends in the differences between tests made at different circular up/down counter gains, acceleration/deceleration limit settings and different command-speed values. The system exhibited a limit cycle type of operation. The amplitude of the limit cycle varied from 4.2 mph to 7.5 mph, and the frequency of the limit cycle varied from 0.0888 rad/sec to 0.176 rad/sec. Table 3-5 shows the parameter values for each test. Table 3-6 tabulates the data in terms of the various parameter changes.

The results of these tests have been used for developing a mathematical model for this control system in the next chapter.

TABLE 3-5

ROAD TESTS AND RESULTS

Test No	Fig. No	GAINS		LIMITS		Command Speed MPH	Amplitude V MPH	Freq. w rad/sec
		Up-Channel	Down-Channel	Acceleration PPS	Deceleration PPS			
1	1	1/15	1/15	133.0	44.44	50	7.50	0.139
2	2	1/10	1/10	133.0	44.44	50	4.375	0.142
4	4	1/10	1/10	66.67	66.67	50	7.031	0.170
5	5	1/10	1/10	47.62	133.0	50	6.25	0.164
*6	6	1/15	1/10	133.0	44.44	50	5.625	0.067
7	7	1/15	1/15	133.0	44.44	50	5.625	0.134
8	8	1/10	1/10	133.0	44.44	50	4.828	0.157
9	9	1/5	1/5	133.0	44.44	50	6.250	0.143
10	10	1/3	1/3	133.0	44.44	50	8.593	0.106
11	11	1/3	1/3	133.0	44.44	50	8.906	0.088
12	12	CONSTANT THROTTLE TEST ≈ 50 mph						
13	13	CONSTANT SPEED DRIVING TEST ≈ 50 mph						
14	14	1/10	1/10	74.0	74.0	50	5.625	0.176
15	15	1/10	1/10	74.0	74.0	40	4.219	0.168
16	16	1/15	1/15	133.0	44.44	30	5.938	0.092
17	17	1/10	1/10	133.0	44.44	30	5.938	0.147
18	18	1/5	1/5	133.0	44.44	30	5.781	0.143
19	19	1/10	1/10	66.67	66.67	30	5.781	0.163
20	20	1/10	1/10	47.62	133.0	30	5.469	0.160
21	21	1/15	1/15	47.62	133.0	40	7.812	0.157
22	22	1/5	1/5	47.62	133.0	40	7.188	0.167
23	23	1/3	1/3	66.67	66.67	50	7.188	0.139
24	24	1/5	1/5	133.0	133.0	50	6.797	0.168
25	25	1/10	1/10	66.67	66.67	50	7.50	0.157

* Up Channel and Down Channel gains are different

TABLE 3.6

TEST AND RESULTS

GAINS		LIMITS PPS		COMMAND SPEED						REMARKS
				50 MPH		30 MPH		40 MPH		
Up Channel	Down Channel	Acceler-ation	Deceler-ation	AMPL V mph	FREQ w rad/sec	AMPL V mph	FREQ w rad/sec	AMPL V mph	FREQ w rad/sec	
1/15	1/15	133.0	44.44	7.50	0.139	5.938	0.092	-	-	CHANGE IN GAINS
1/10	1/10	133.0	44.44	4.375	0.142	5.938	0.147	-	-	
1/10	1/10	66.67	66.67	7.031	0.170	5.781	0.163	-	-	CHANGE IN LIMITS
1/10	1/10	47.62	133.0	6.250	0.164	5.469	0.169	-	-	
1/15	1/15	47.62	133.0	-	-	-	-	7.812	0.157	CHANGE IN GAINS
1/5	1/5	47.62	133.0	-	-	-	-	7.188	0.167	
1/15	1/15	133.0	44.44	5.625	0.134	-	-	-	-	
* 1/10	1/15	133.0	44.44	2.813	0.157	-	-	-	-	CHANGE IN GAINS
1/5	1/5	133.0	44.44	6.250	0.143	-	-	-	-	
1/3	1/3	133.0	44.44	8.593	0.106	-	-	-	-	
				8.906	6.088	-	-	-	-	
1/10	1/10	74.0	74.0	5.625	0.176	-	-	4.219	0.168	CHANGE IN SPEED
1/10	1/10	66.67	66.67	7.50	0.157	-	-	-	-	CHANGE IN GAINS
1/3	1/3	66.67	66.67	7.188	0.167	5.781	0.143	-	-	
1/5	1/5	133.0	133.0	6.797	0.168	-	-	-	-	

* Up channel and down channel gains are different.

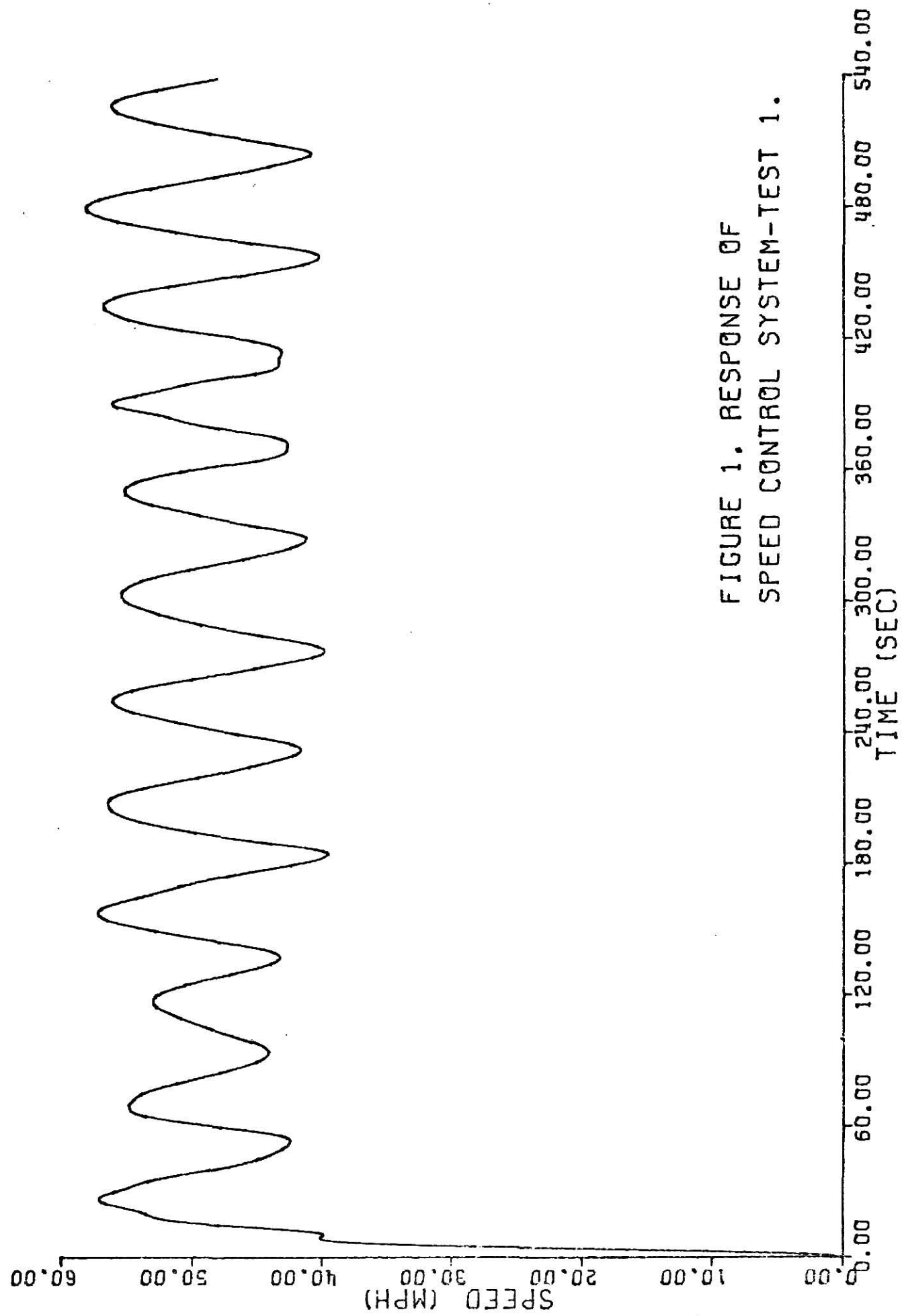


FIGURE 1. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 1.

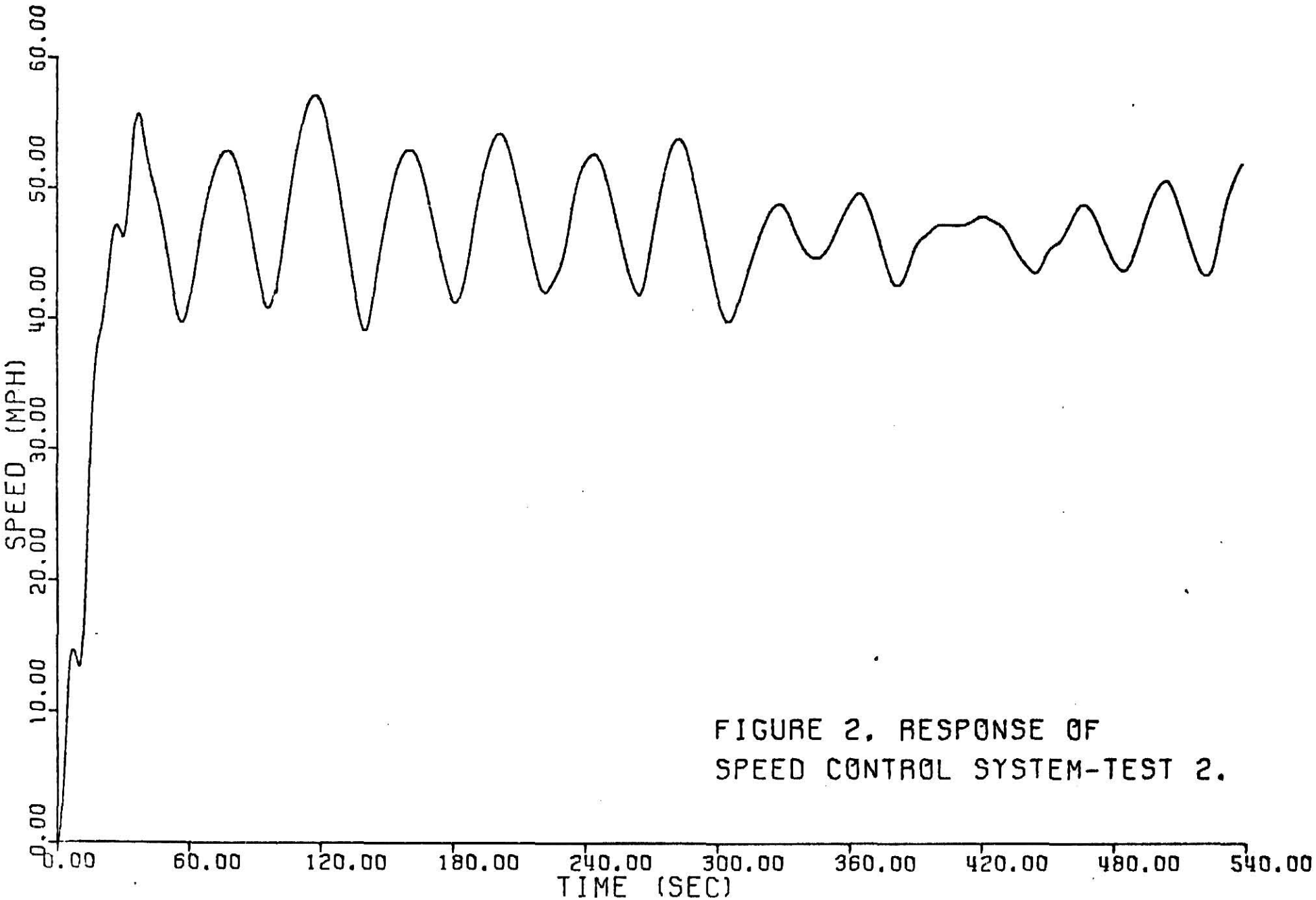


FIGURE 2. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 2.

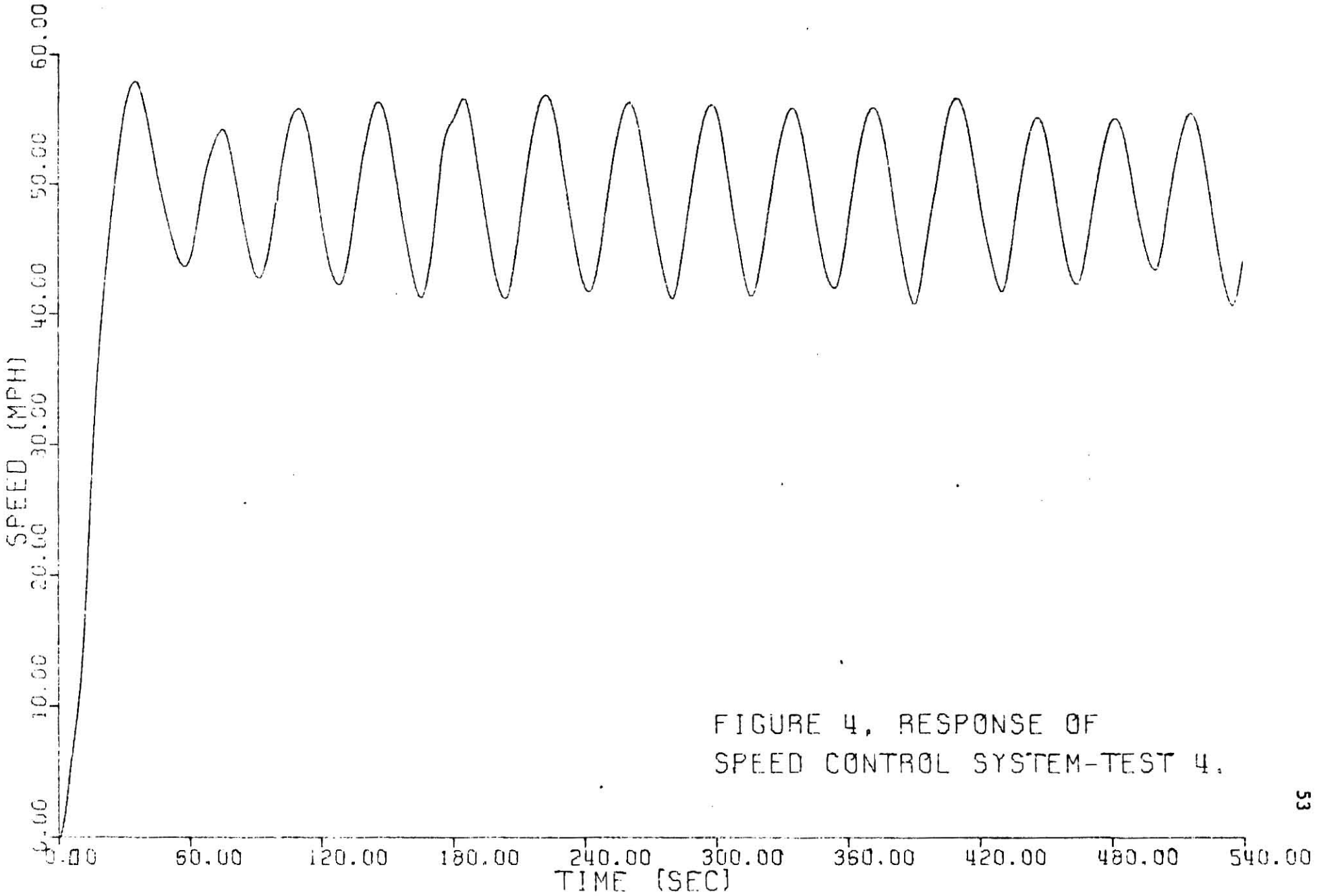


FIGURE 4, RESPONSE OF
SPEED CONTROL SYSTEM-TEST 4.

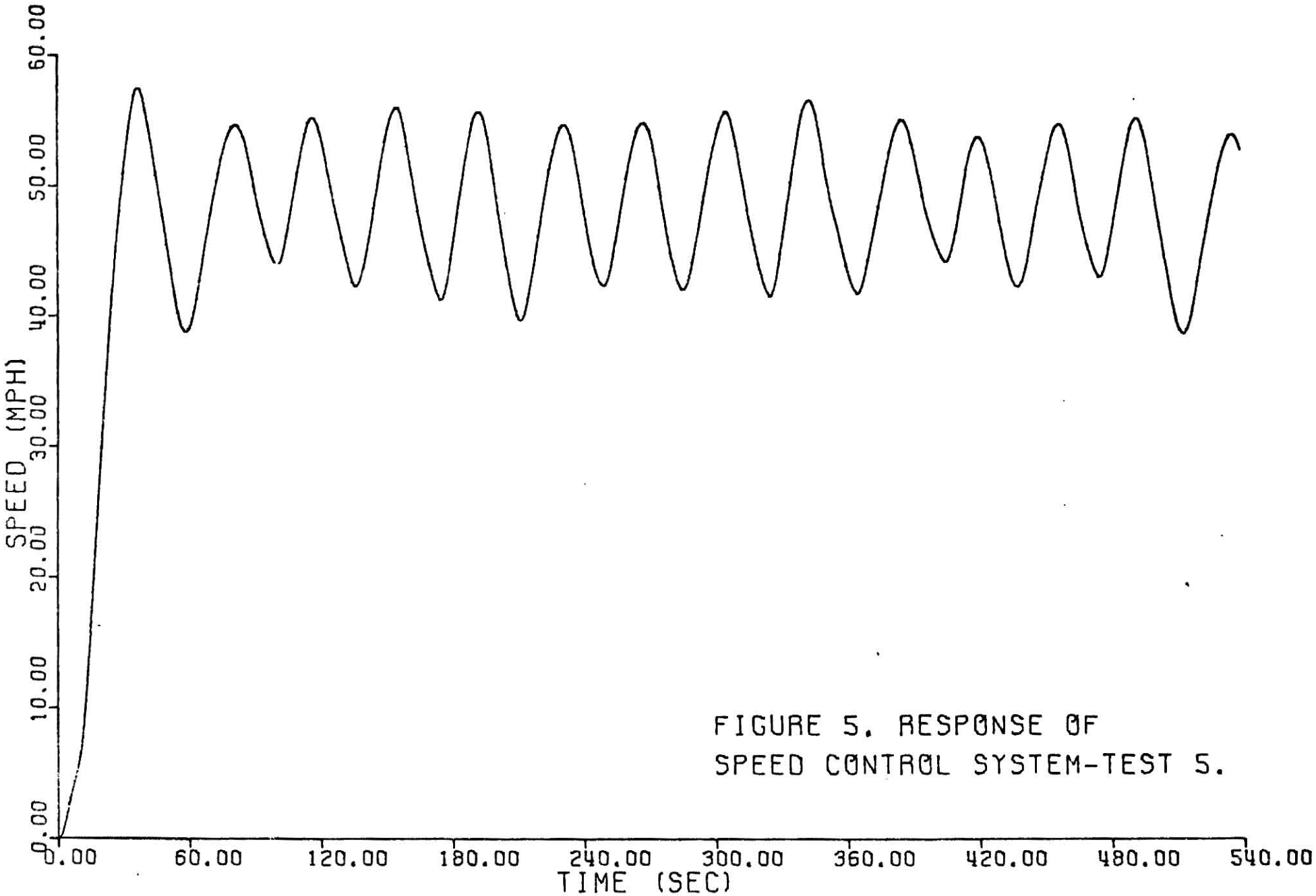


FIGURE 5. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 5.

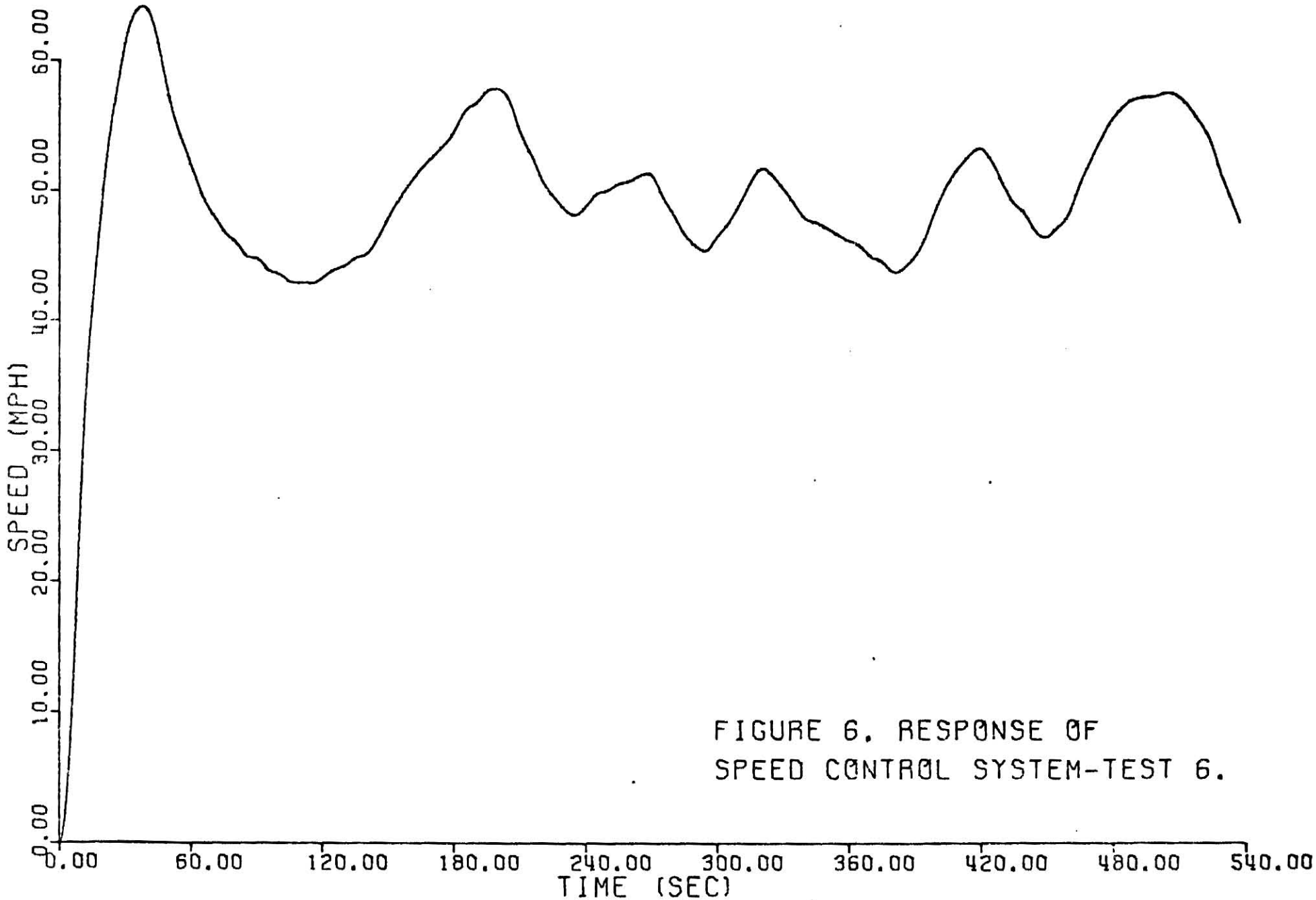


FIGURE 6. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 6.

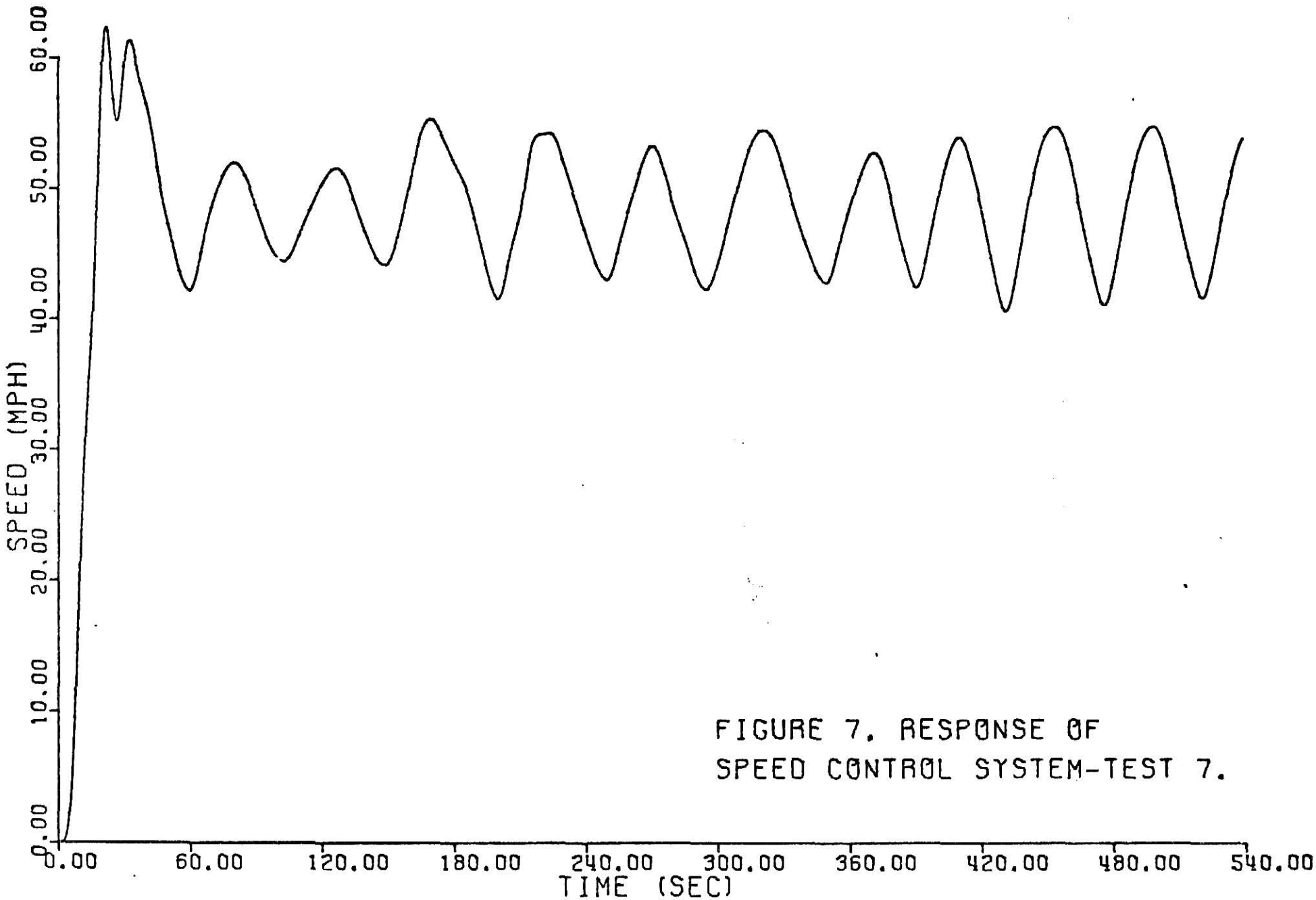


FIGURE 7. RESPONSE OF SPEED CONTROL SYSTEM-TEST 7.

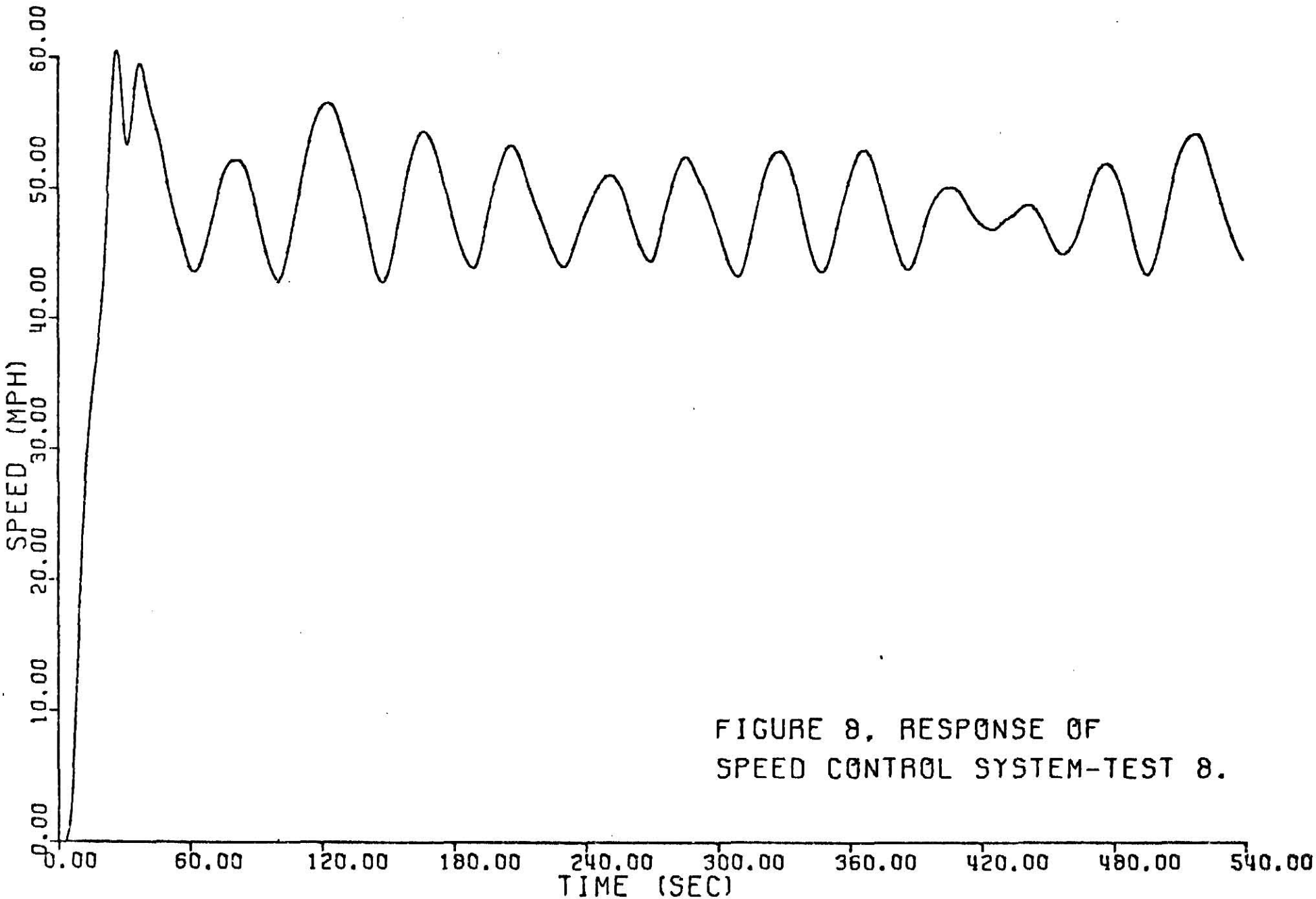


FIGURE 8. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 8.

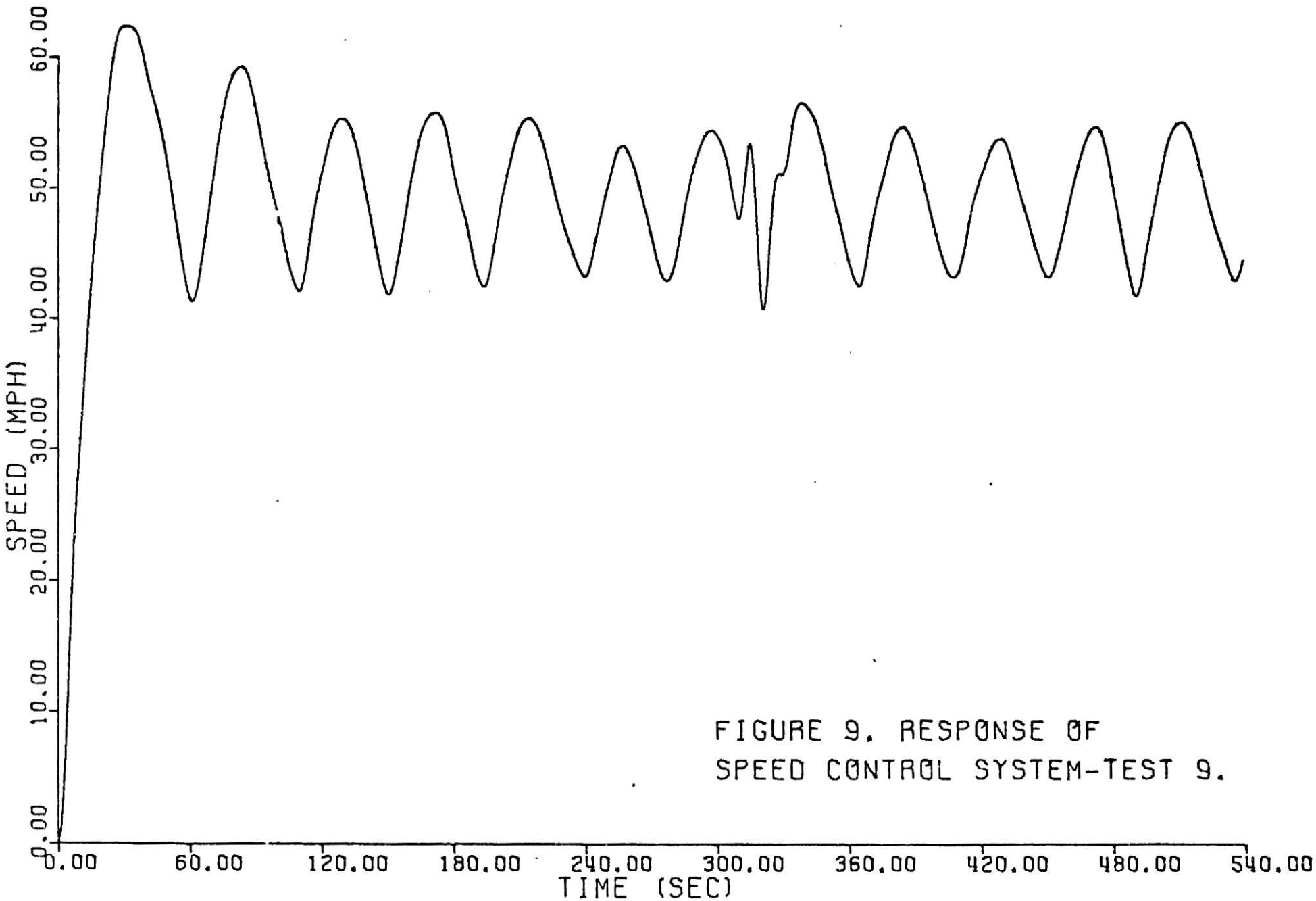


FIGURE 9. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 9.

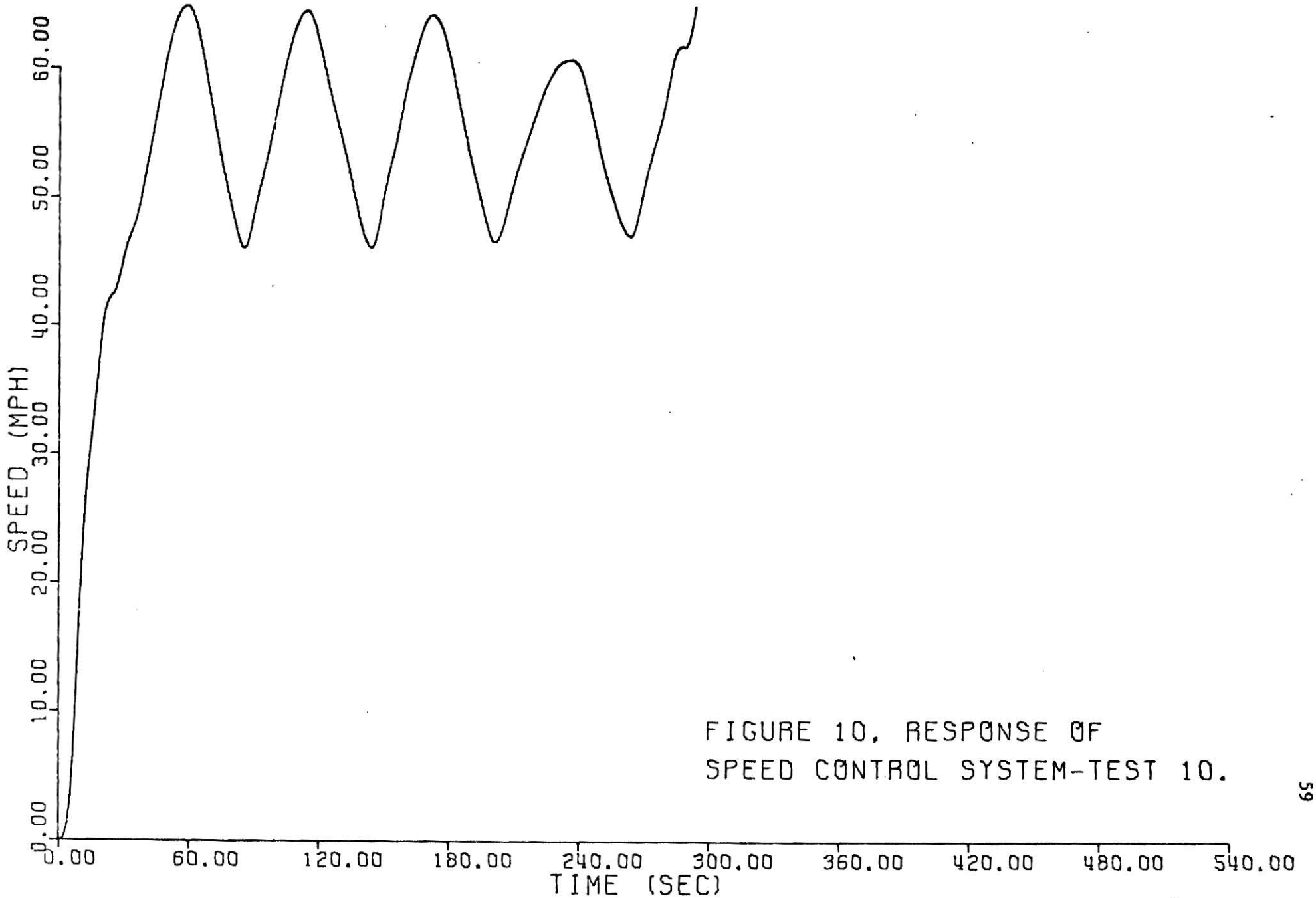


FIGURE 10. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 10.

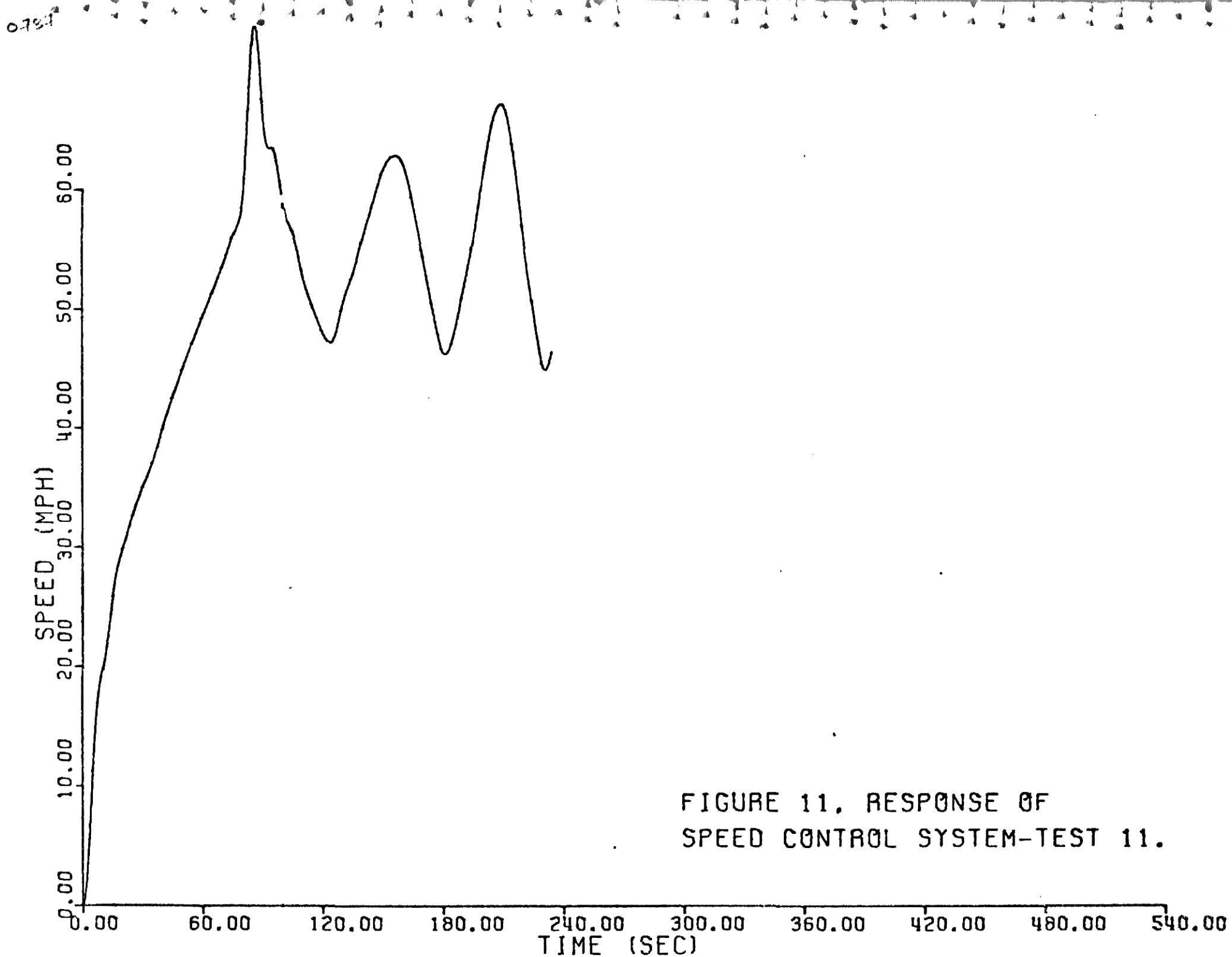


FIGURE 11. RESPONSE OF SPEED CONTROL SYSTEM-TEST 11.

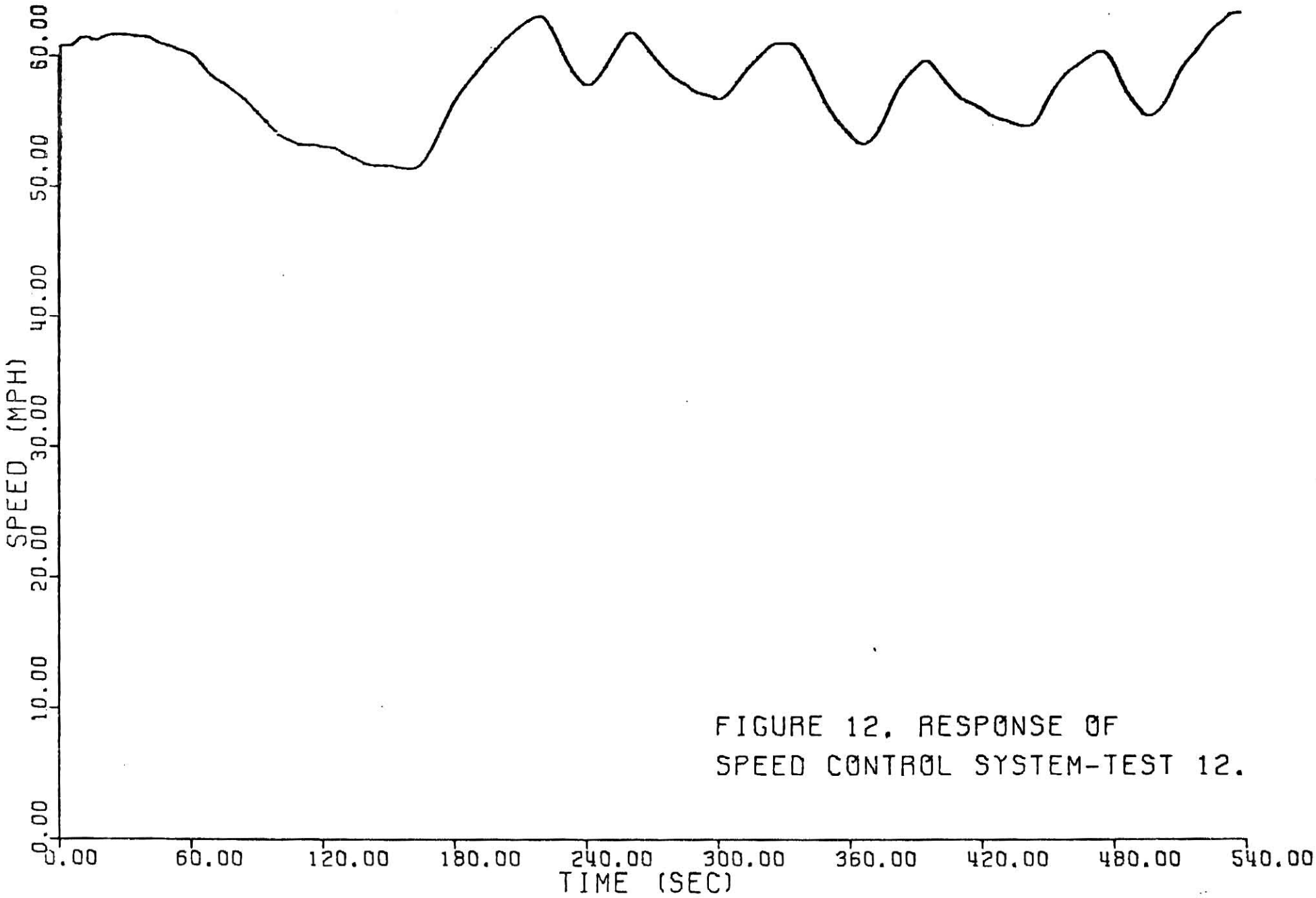


FIGURE 12. RESPONSE OF SPEED CONTROL SYSTEM-TEST 12.

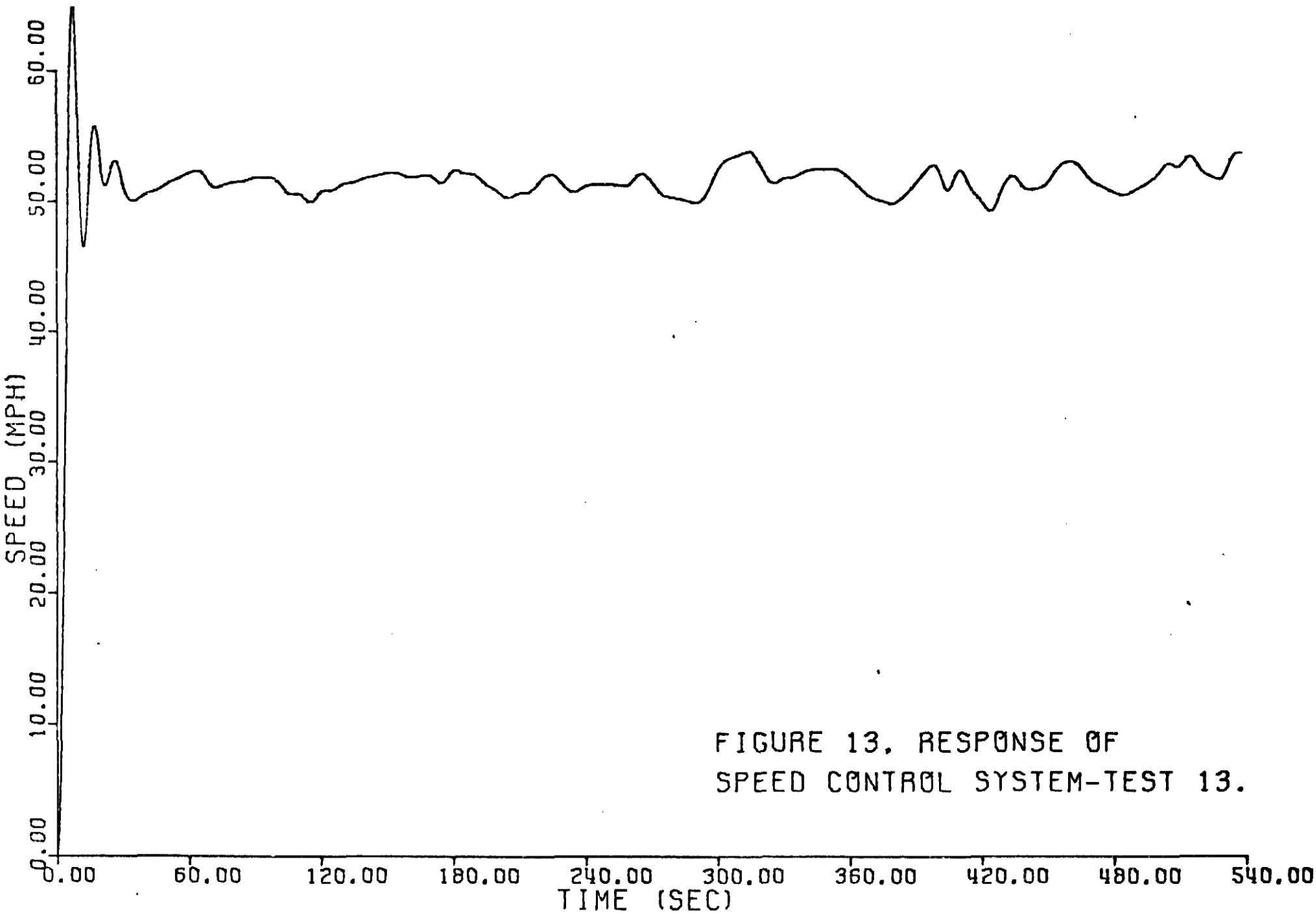


FIGURE 13. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 13.

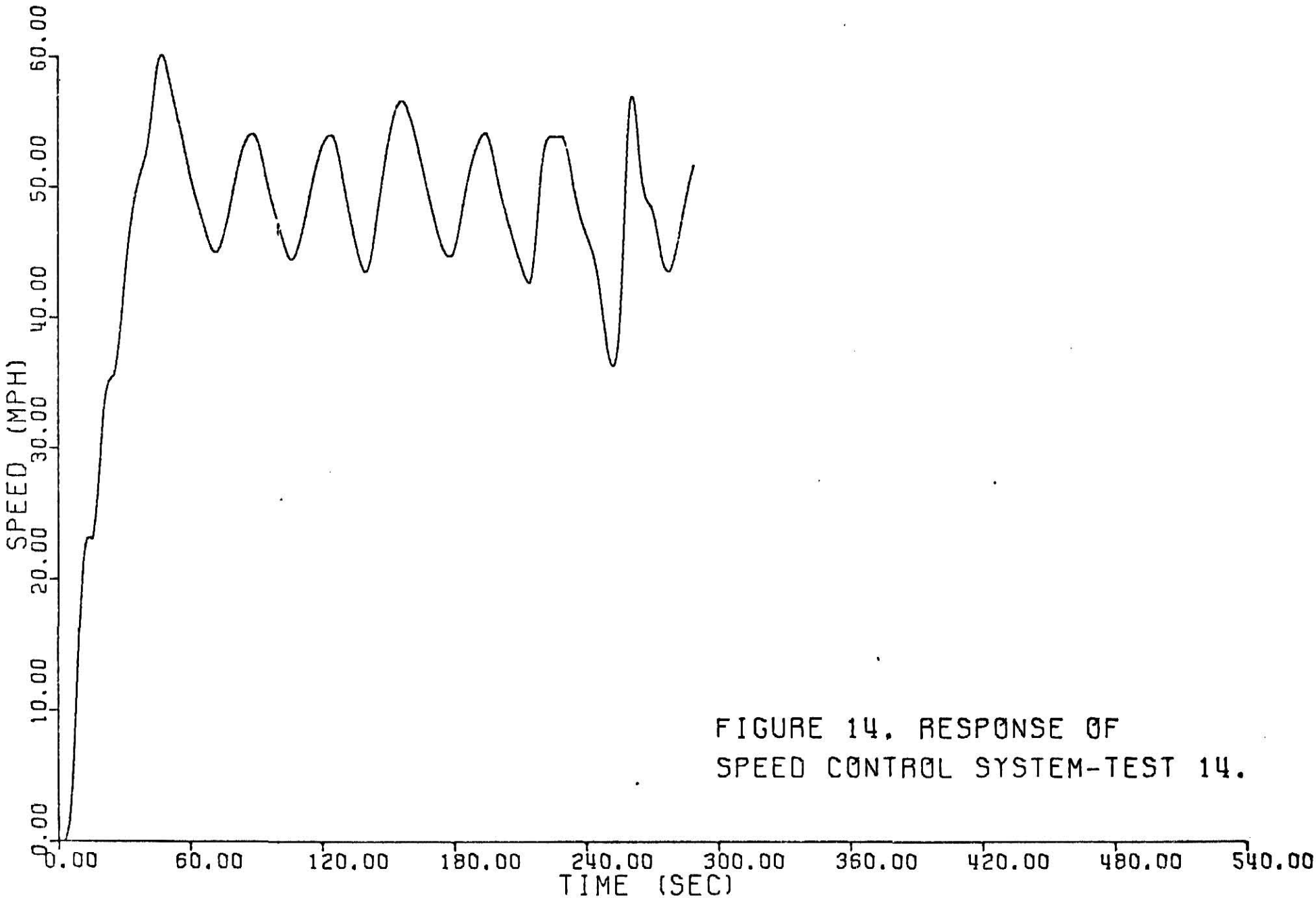


FIGURE 14. RESPONSE OF SPEED CONTROL SYSTEM-TEST 14.

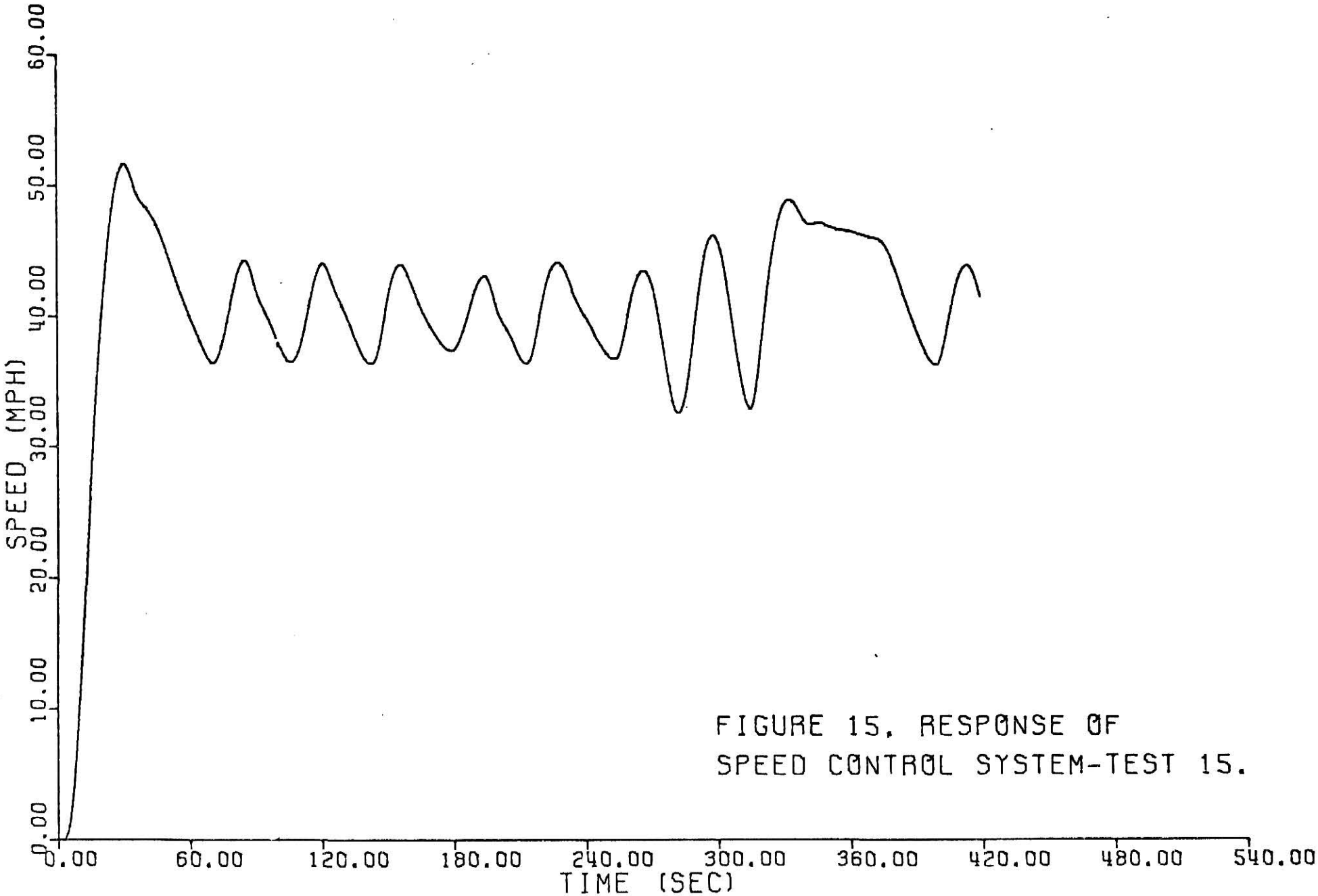


FIGURE 15. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 15.

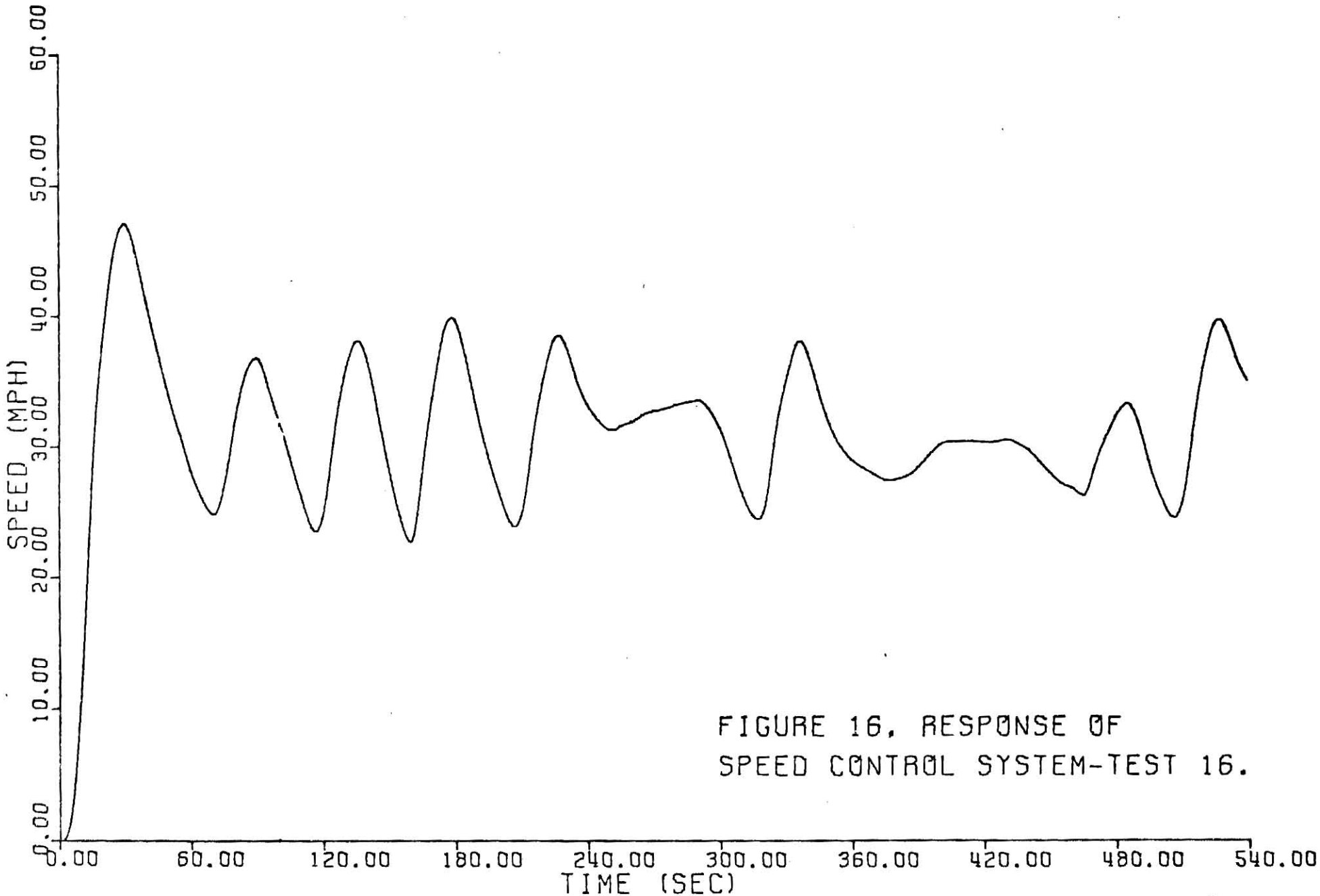


FIGURE 16. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 16.

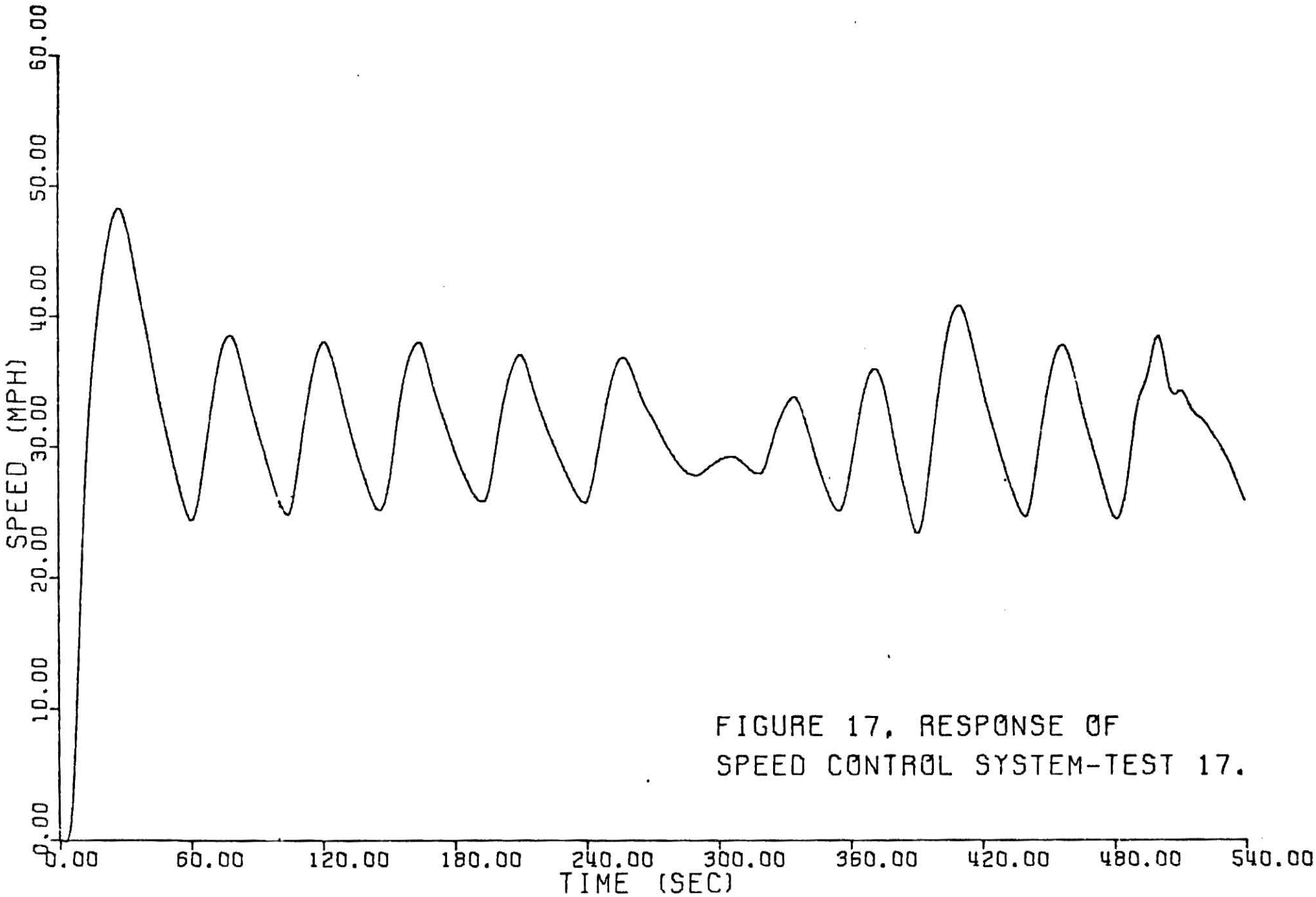


FIGURE 17. RESPONSE OF SPEED CONTROL SYSTEM-TEST 17.

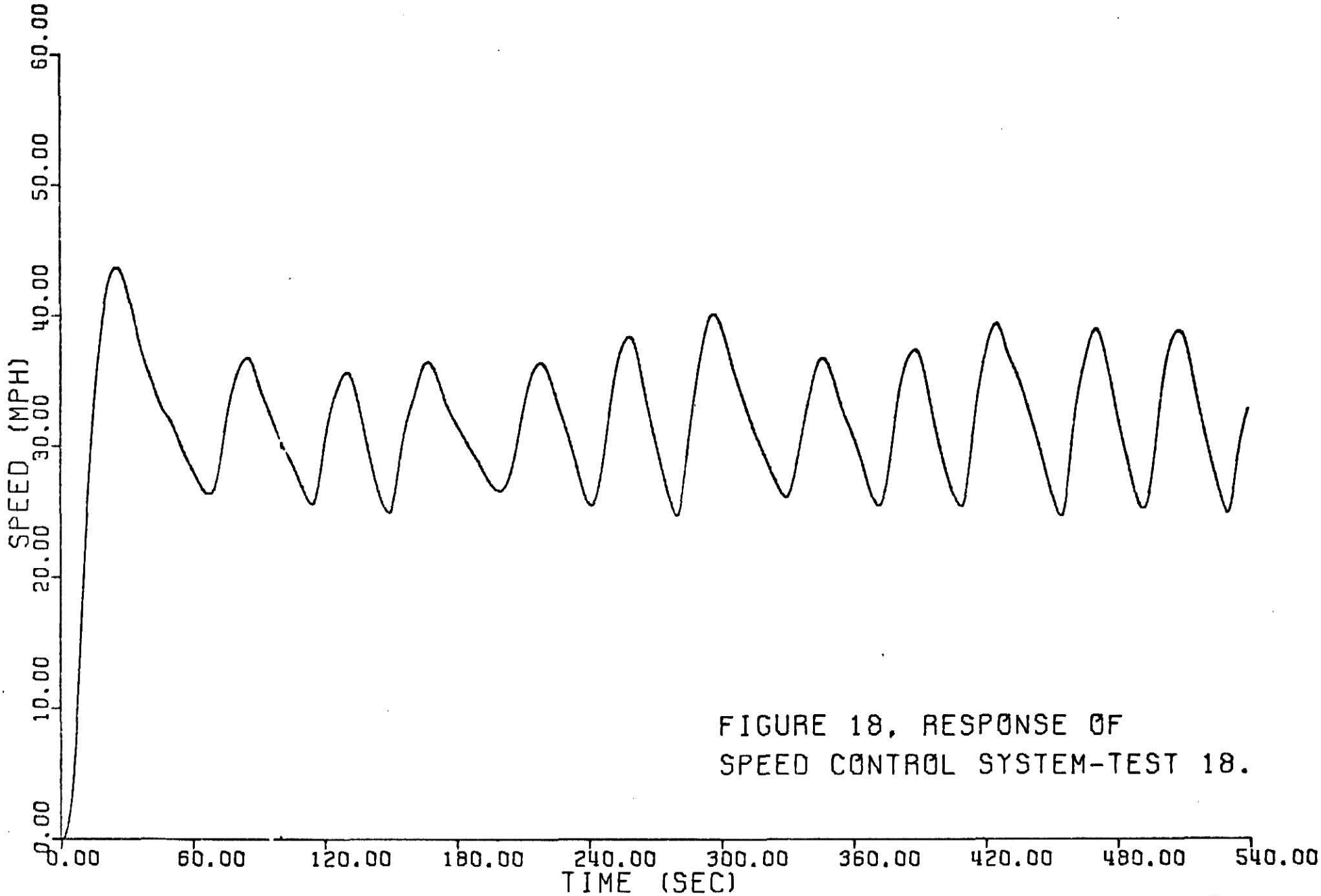


FIGURE 18, RESPONSE OF
SPEED CONTROL SYSTEM-TEST 18.

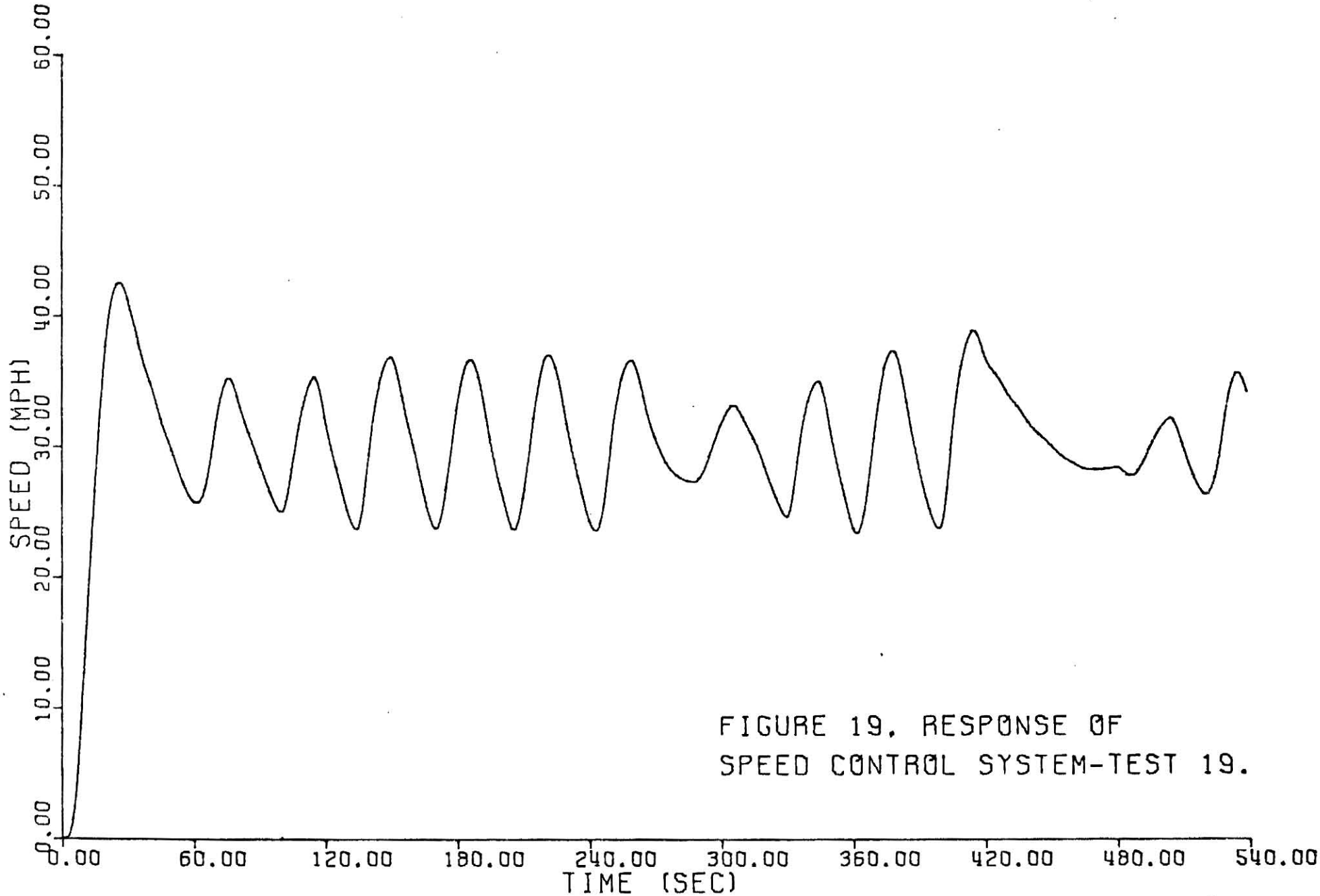


FIGURE 19. RESPONSE OF SPEED CONTROL SYSTEM-TEST 19.

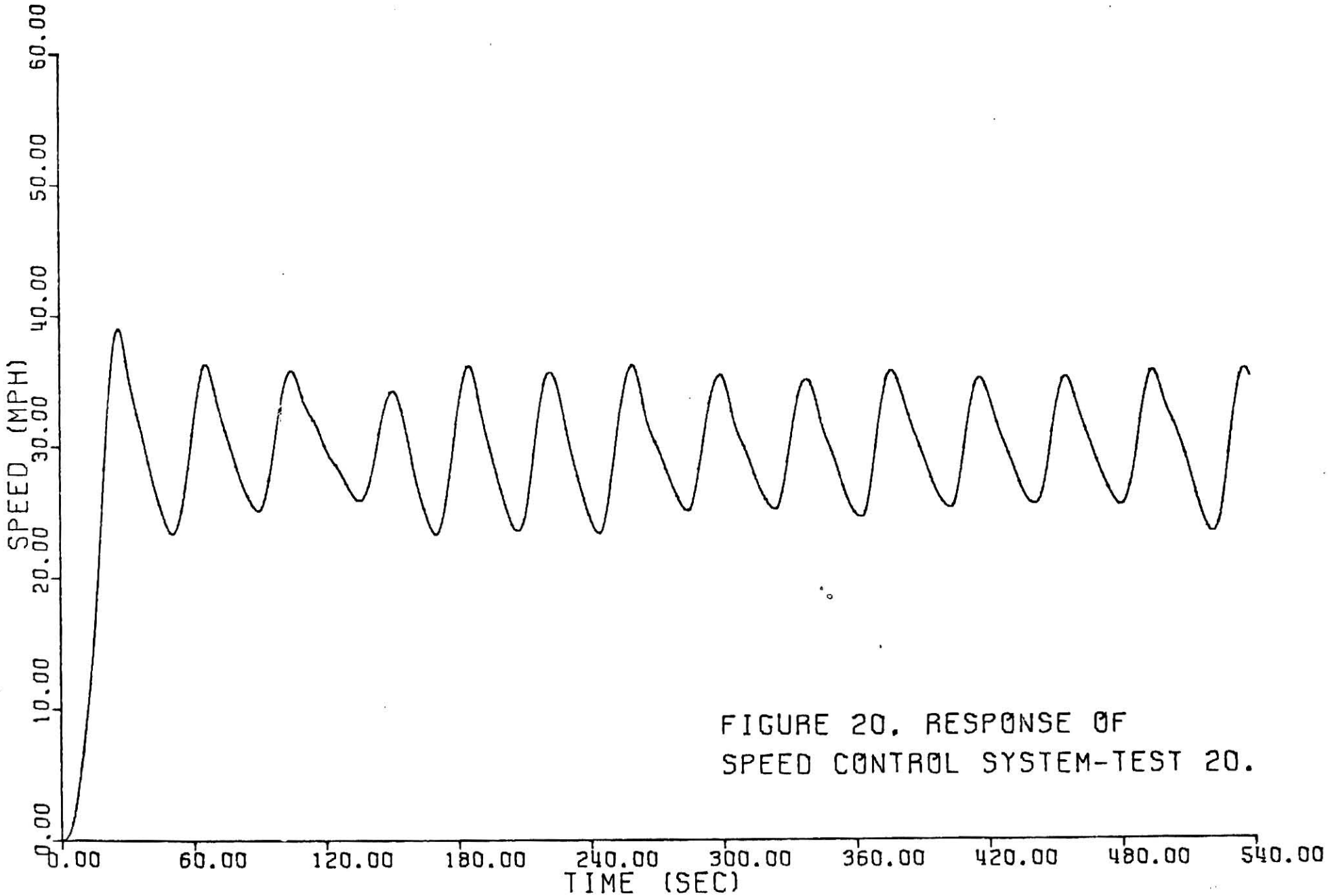


FIGURE 20. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 20.

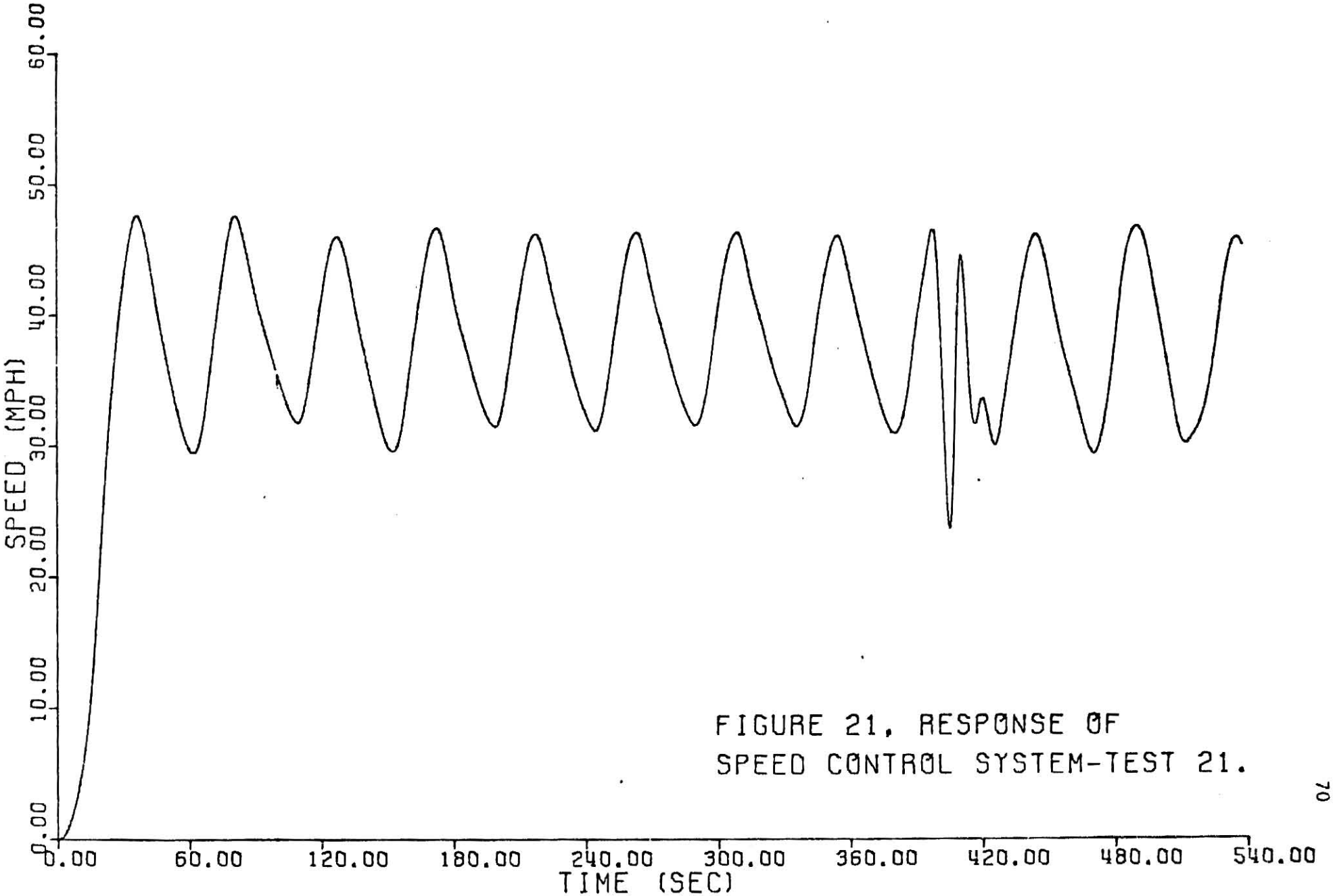


FIGURE 21. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 21.

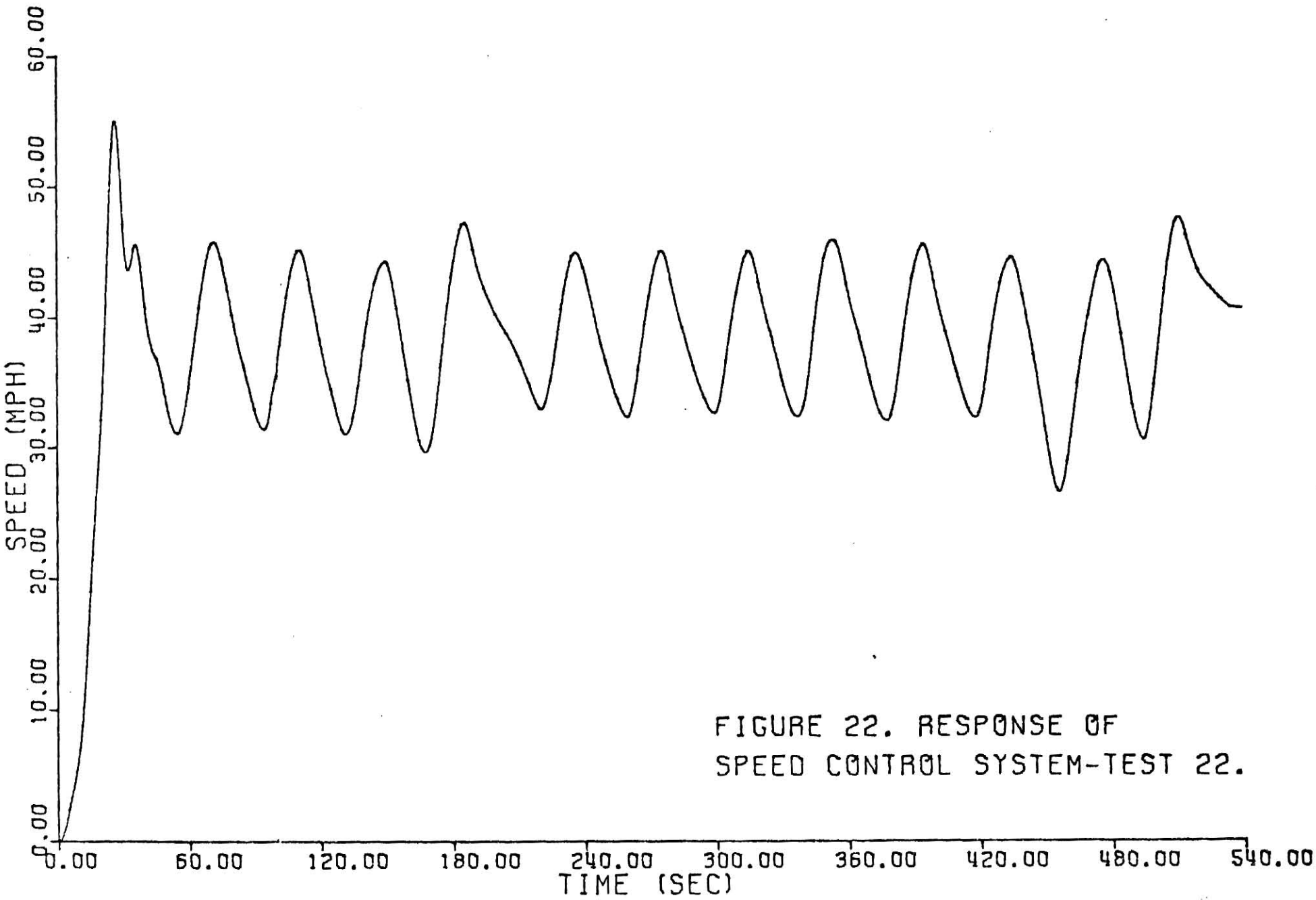


FIGURE 22. RESPONSE OF SPEED CONTROL SYSTEM-TEST 22.

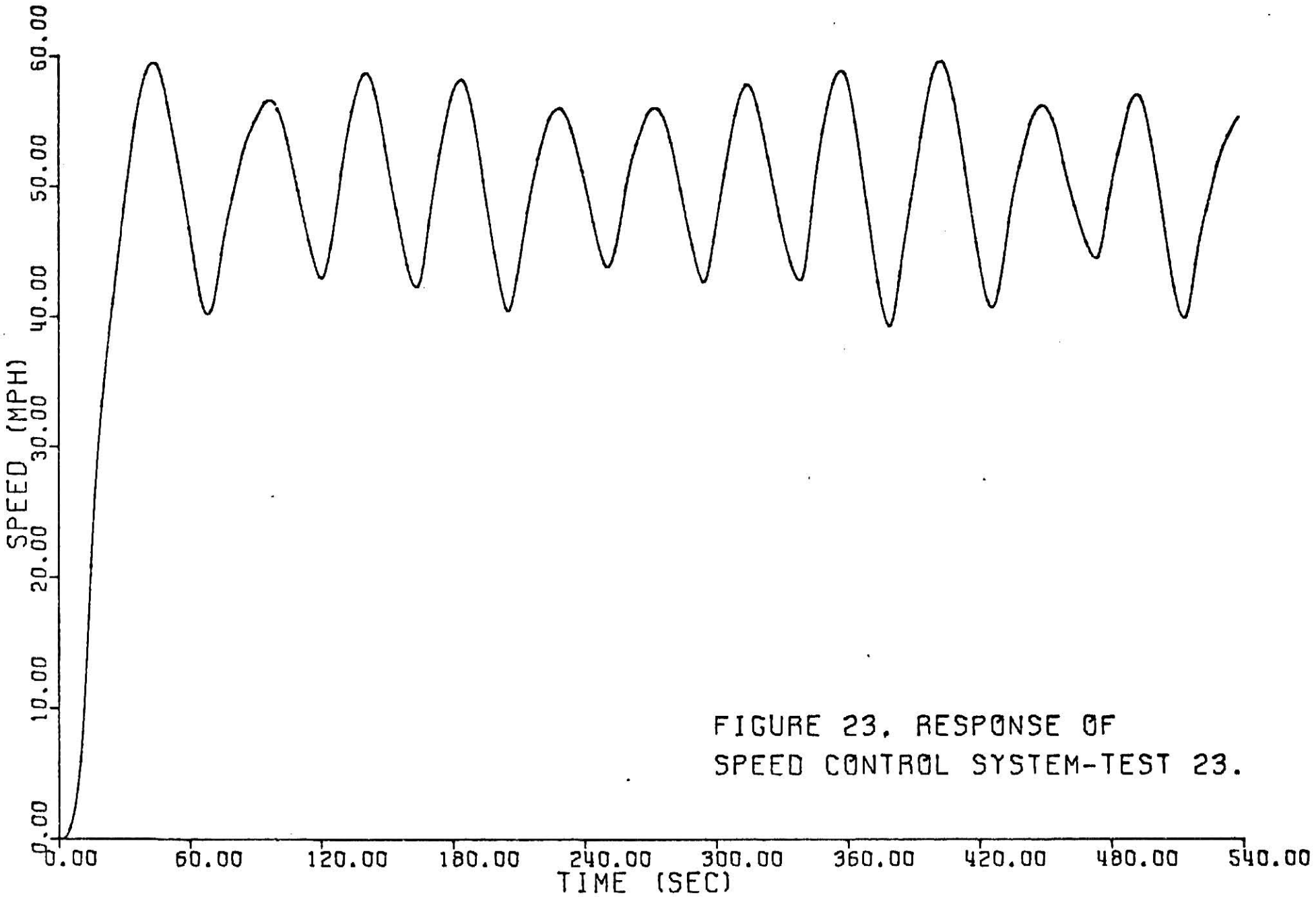


FIGURE 23. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 23.

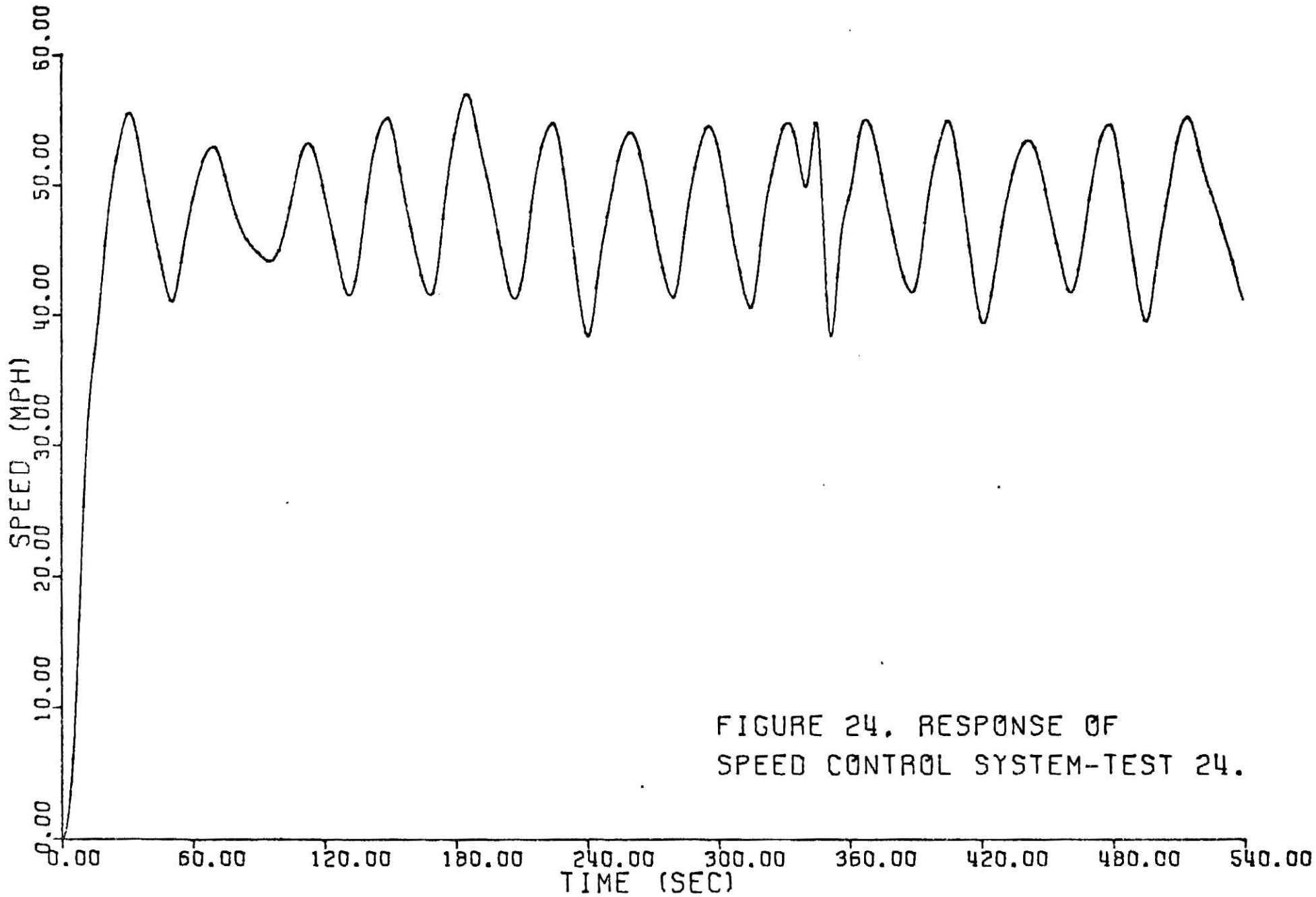


FIGURE 24. RESPONSE OF SPEED CONTROL SYSTEM-TEST 24.

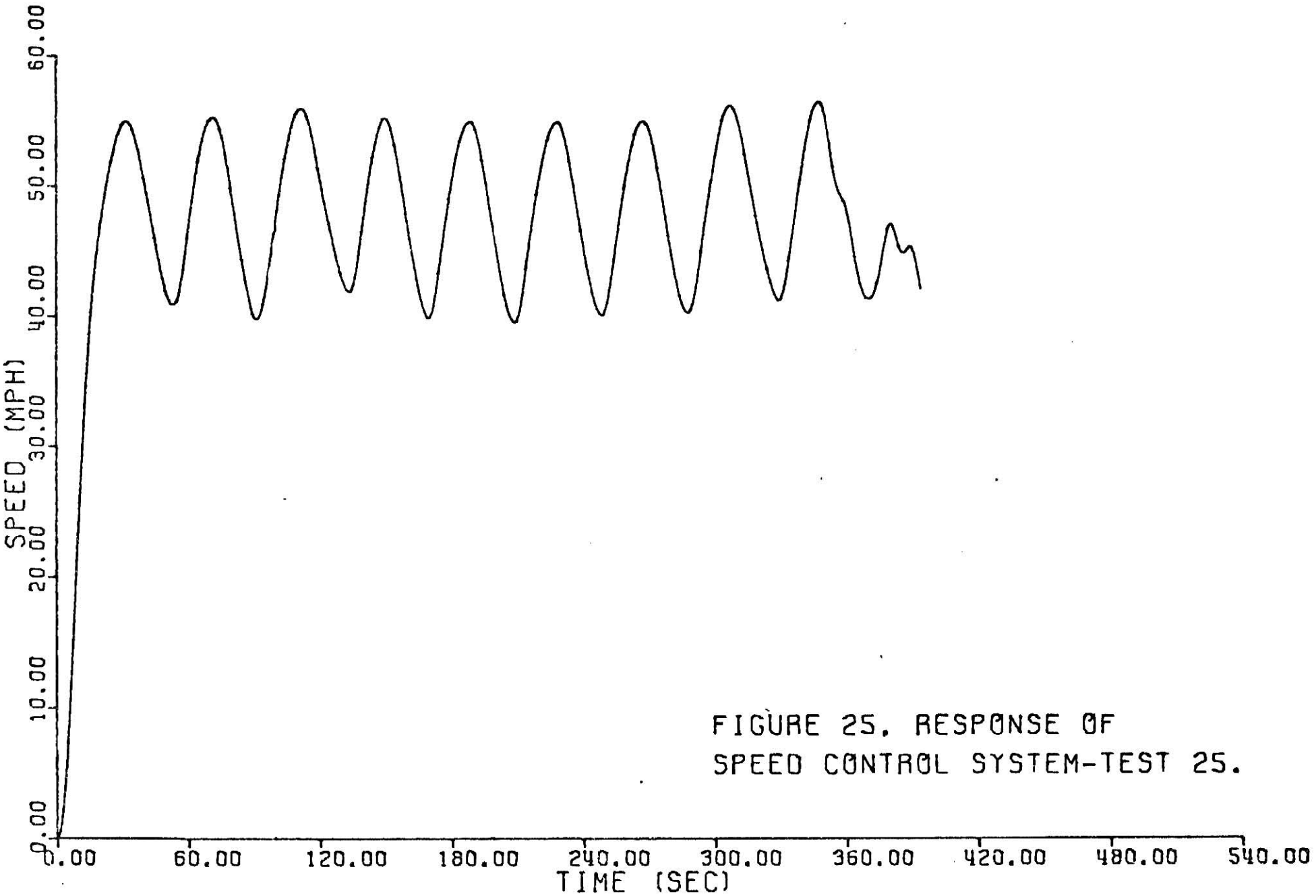


FIGURE 25. RESPONSE OF
SPEED CONTROL SYSTEM-TEST 25.

CHAPTER 4

THE MATHEMATICAL MODEL

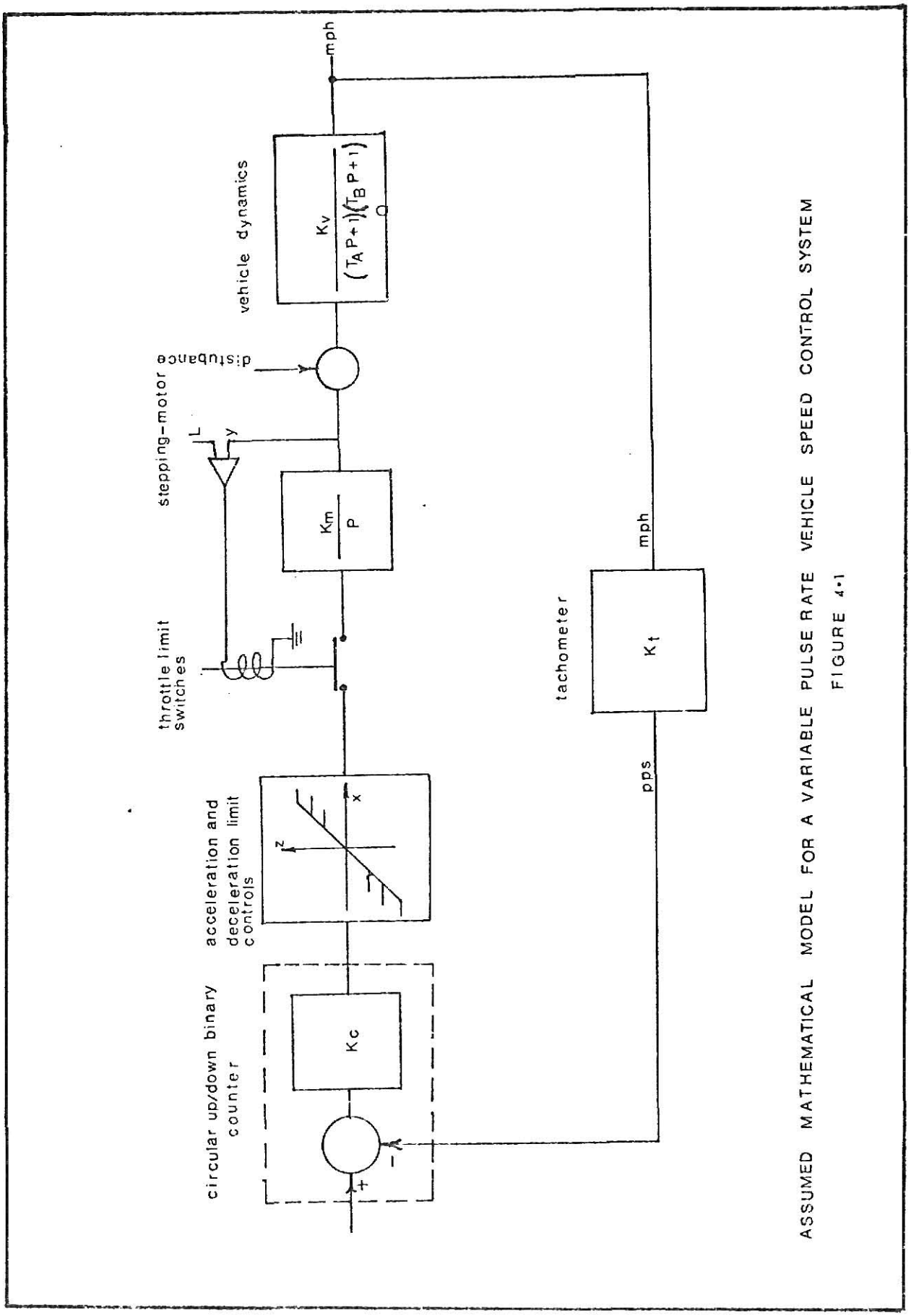
Chapter 4

The Mathematical Model

4-1 Introduction

The purpose of this project was to study the problems associated with the implementation of a variable pulse-rate control system. The application chosen, the control of the speed of an automobile, was a particularly challenging situation. As very little was known of the dynamic characteristics of the automobile, a variety of gain and limit adjustments were included in the design to provide the flexibility to search for an adequate set of parameter values. As has been pointed out in the previous chapter, the system exhibited a limit cycle type of operation for all gain and limit values within the range of the system. In this chapter the results of the many tests will be examined and a simple mathematical model for the system will be developed. In the next chapter the model will be used to suggest a stabilization scheme for the system.

Figure 4-1 shows the arrangement of components of the variable pulse-rate vehicle speed control system. Figure 1-1 is the block diagram of the system. It is recognized that many parts of the system exhibit nonlinear characteristics. A complete and careful analysis of these nonlinear characteristics is beyond the scope of this work. Attention will be focused on the nonlinear characteristics associated with the acceleration/deceleration limits and the throttle linkage limit switches. Consideration of these nonlinear characteristics will require a describing function analysis. In section 4.2 the assumptions underlying the analysis will be presented. Calculation of parameter values will be carried out in section 4.3. The describing function analysis will be presented in section 4.4 and the application of the describing function analysis to the development of the mathematical model of the vehicle dynamics will be presented in section 4.5



ASSUMED MATHEMATICAL MODEL FOR A VARIABLE PULSE RATE VEHICLE SPEED CONTROL SYSTEM

FIGURE 4·1

4.2 Assumptions

In this section, all assumptions and approximations underlying this mathematical analysis are presented. They are as follows:

1. The vehicle dynamics have a nonlinear gain. The amount of throttle movement for a change in vehicle speeds, in its lower speed range is more than when the change in vehicle speeds occurs in its higher speed range. In the mathematical model the vehicle gain is assumed to be linear.

2. It has been assumed that the limit cycle response of the speed control system is due to a second order lag in the vehicle dynamics. Hence, the open loop transfer function for the vehicle dynamics is assumed to be

$$G_V = \frac{K_V}{(T_A P + 1)(T_B P + 1)}$$

where

K_V is the vehicle gain in mile per hour per inch of throttle linkage travel.

P is the differential operator and T_A And T_B are timeconstants of the vehicle response.

It is well known that the dynamics of acceleration are different from deceleration. A detailed analysis of the parts of the cycle goes beyond the scope of this work and requires a data refinement which is not available. The difference between acceleration dynamics and deceleration dynamics is ignored.

3. Characteristics of various disturbances like wind loads, hills, etc. are not known. The tests were conducted when no appreciable wind was blowing. The tests were conducted over relatively level highways. It is assumed that the effect of the hills averaged out. Therefore, the effects of these disturbances are not included in the analysis.

4. The angle between the throttle limit switches is approximately 240°, ie 2/3rd of a clutch shaft revolution. It is assumed that the limit switches are located symmetrical with respect to the nominal operating position of the clutch shaft.

5. It is assumed that the acceleration and deceleration limit control and the throttle limit switches constitute the only nonlinear elements of the system.

6. The nonlinearity of the acceleration and deceleration limit control and throttle limit switches are considered separately. The describing function N1 represents the nonlinear element due to the acceleration and deceleration limit control. The describing function N2 represents the non-linearity of the throttle limit switches along with the stepping-motor.

It is recognized that this is not the conventional approach to describing function analysis, but it will be utilized here. The problem of developing the describing function for the combined elements is so great as to render that analysis almost impossible.

7. In several of the tests the limits on the acceleration control were different. Therefore, this nonlinearity is not symmetric in these cases. Since nonsymmetry results in a bias in the system and the analysis looks only at the amplitude and frequency of the signals, the non-symmetrical characteristics are neglected. A simple mathematical average of the two limits have been taken for the purpose of this analysis.

8. It has been observed from the response of the system that in many cases the overshoot above the command speed is less than the undershoot. But for the purpose of this analysis, the input and the output are assumed to be sinusoidal and symmetrical. (Only amplitude and frequency are considered.)

9. The acceleration/deceleration limit controls are not perfect limiters. A more detailed analysis of these elements requires considerations of the independence of the pulse trains and is quite complex. The simple ideal limiter will provide an adequate model for the present analysis.

4.3 Calculations

This section presents the calculations of the parameters of the variable pulse-rate vehicle control system. The parameter values to be calculated are:

i) Circular up/down bindary counter gain (Kc)

ii) Stepping-motor gain (Km)

iii) Pulse-rate tachometer gain (Kt)

iv) Vehicle dynamic gain (Kv)

v) Throttle linkage limit value (L)

i) Circular up/down binary counter gain (Kc)

The value of the gain for the up or down channels vary from 1/3 to 1/15 ie. 0·333 to 0·0666. The value may be selected by means of a set of switches on the console. The switches should be selected so that both up and down channel gains are equal.

ii) Stepping-motor gain (Km)

The number of pulses for one revolution of the stepping-motor = 200 pulses/rev. The gear ratio of the gear train is = 4.0625. Hence, the number of pulses per revolution of the clutch shaft - 200 x 4.0625 = 812.50 pulses/rev. The diameter of the clutch shaft = 0.25 in. Hence, linear distance travelled in one revolution of the clutch shaft is = Π x 0.25 = 0.7854 in/rev.

Therefore, the gain Km = $\frac{0.7854}{812.50}$ = 9.66 x 10^{-4} in/pulse

iii) Pulse-rate tachometer gain (Kt)

The number of slots on the tachometer = 96 slots. Number of pulses per slot = 4 pulses/slot. Total pulses per revolution of the pulse-rate

tachometer = 4 x 96 = 384 pulses/rev. Number of revolutions of the tachometer per mile = 1000 rev/mile. Hence, the tachometer gain Kt = $384 \times \frac{1000}{36000} = 106.66 \frac{\text{pps}}{\text{mph}}$.

iv) Vehicle dynamic gain (Kv)

A road test was conducted to obtain some insight into vehicle dynamics. The throttle linkage position in inches was measured against a linear scale. The test was conducted on a flat straight road. The accelerator was set to obtain various steady-state speeds and the throttle linkage displacement was measured. The following table gives the observed results:

Table 4.1

SPEED MPH	THROTTLE POSITION IN INCHES Test 1	Test 11
15	3 1/16	
20	3 5/32	3 1/8
30	3 3/16	3 5/32
35	3 7/32+	
40	3 1/4	3 3/16
45	3 1/4+	
50	3 5/16	3 7/32
55	3 3/8	
60	3 13/32	3 9/32
70	3 7/16	

A graph was plotted of vehicle speed verses throttle linkage position in inches. From the graph the value 1/16 inch per 10 miles per hour was chosen as the best value for $\frac{1}{K_V}$. Hence the vehicle dynamic gain K_V = 160 mph/inch.

v) Throttle Linkage Limit Value (L)

The two limit switches are placed approximately 240° apart. Assuming symmetry,

L = 1/3 rev x 0.7845 in/rev

= 0.261 inches.

4.4 DESCRIBING FUNCTION ANALYSIS

This section is devoted to the describing function analysis for the non-linear elements. The non-linear elements to be considered are the single-valued saturation non-linearity of the acceleration/deceleration limit control and limit switches coordinated with the stepping motor. As discussed in section 5.1, these two non-linearities are considered separately for this analysis.

A) Describing function analysis for single-valued saturation non-linearity of the acceleration and deceleration limit control

Figure 4.3 shows the non-linear element input/output characteristic. Figure 4.4 shows the effect of the non-linearity on a sinusoidal signal of the form

$$x(t) = X \sin wt \tag{4.1}$$

The output z(t) may be expressed as a Fourier series as follows:

$$z(t) = Ao + \sum_{n=1}^{\infty} (An \cos n\,wt + Bn \sin n\,wt) \tag{4.2}$$

where,

$$An = \frac{1}{\pi} \int_0^{2\pi} x(t) \cos n\,wt\, d(wt) \tag{4.3}$$

and

$$Bn = \frac{1}{\pi} \int_0^{2\pi} x(t) \sin n\,wt\, d(wt). \tag{4.4}$$

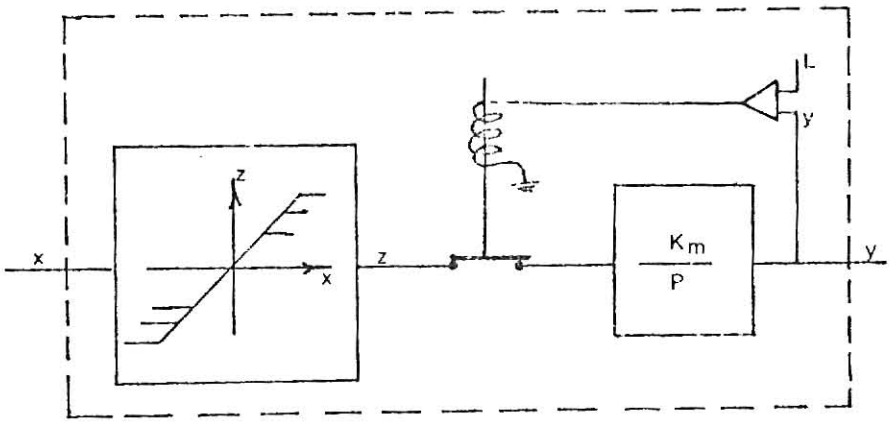
Assuming the non-linearity to be symmetric yields

$$Ao = 0. \tag{4.5}$$

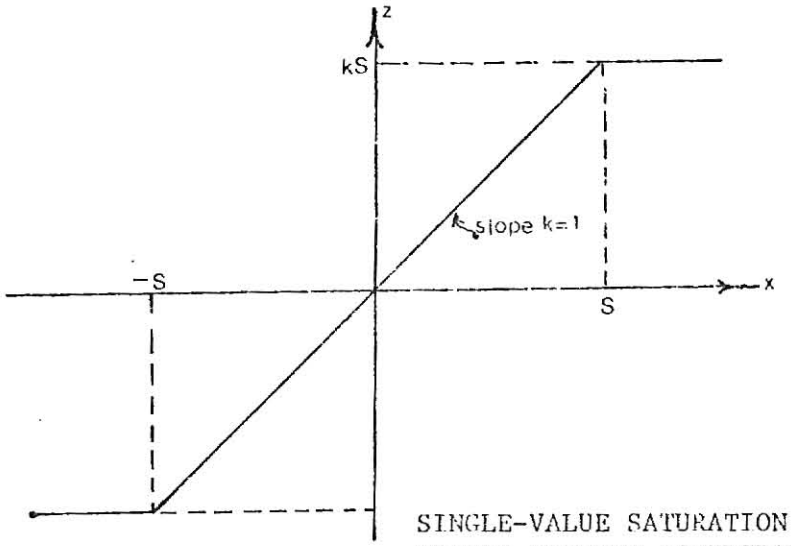
Neglecting the higher harmonics, yields

$$z(t) = A \cos wt + B \sin wt \tag{4.6}$$

$$= Z \sin (wt + \emptyset) \tag{4.7}$$

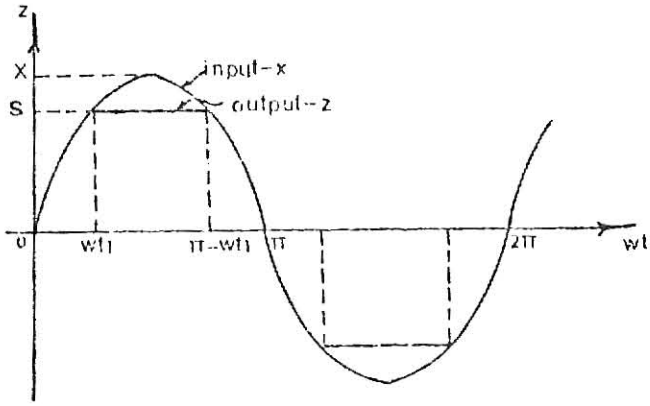


NON LINEAR ELEMENT — FIGURE 4-2



SINGLE-VALUE SATURATION NON-LINEAR ELEMENT ACCELERATION/DE-CELERATION LIMIT CONTROL

FIGURE — 4-3



CHARACTERISTIC OF ACCELERATION/DECELERATION LIMIT CONTROL

FIGURE — 4-4

where,

$$Z = \sqrt{A^2 + B^2} \text{ and } \phi = \tan^{-1}\left(\frac{A}{B}\right). \tag{4.8}$$

Since the input x(t) is an odd function and the output z(t) follows it with no phase shift

$$z(t) = B \text{ Sin } wt$$

$$= Z \text{ Sin } wt \tag{4.9}$$

where,

$$B = \frac{1}{\pi} \int_0^{2\pi} x(t) \text{ Sin } wt \, d(wt) \tag{4.10}$$

$Z = B$ and $\phi = 0°$.

For the symmetric case,

$$B = \frac{2}{\pi} \int_0^{\pi} x(t) \text{ Sin } wt \, d(wt) \tag{4.11}$$

where,

$$z(t) = \begin{cases} kX \text{ Sin } wt & \text{for } o<wt<wt_1 \\ S & \text{for } t_1<wt<\pi-wt_1 \\ kX \text{ Sin } wt & \text{for } \pi-wt_1<wt<\pi \end{cases} \tag{4.12}$$

and where,

k = slope of linearity of element = 1.

S = saturation of the element.

At $t = t_1$,

$$z(t_1) = k \text{ X Sin } wt_1 = S, \tag{4.13}$$

therefore, $\text{Sin } wt_1 = \frac{S}{kX}$

Substituting into the expression for B

$$B = \frac{2}{\pi}\left[\int_0^{wt_1} (k \text{ X Sin } wt) \text{ Sin } wt \, d(wt) + \int_{wt_1}^{\pi-wt_1} (S) \text{ Sin } wt \, d(wt) + \int_{\pi-wt_1}^{\pi} (k \text{ X Sin } wt) \text{ Sin } wt \, d(wt)\right] \tag{4.14}$$

which yields

$$B = \frac{4}{\pi}\left[k \text{ X } \frac{wt_1}{2} + \sqrt{1 - \text{Sin}^2 wt_1}\left(S - \frac{kX}{2} \text{ Sin } wt_1\right)\right] \tag{4.15}$$

Substituting,

$$\text{Sin } wt_1 = \frac{S}{kX} \text{ and } k = 1 \text{ yields,}$$

$$B = \frac{2X}{\pi}\left[\text{Sin}^{-1}\left(\frac{S}{X}\right) + \frac{S}{X}\sqrt{1 - \left(\frac{S}{X}\right)^2}\right] \qquad 4.16$$

The describing function is,

$$N1 = \frac{B}{X} \angle \emptyset$$

$$= \frac{2}{\pi}\left[\text{Sin}^{-1}\left(\frac{S}{X}\right) + \frac{S}{X}\sqrt{1 - \left(\frac{S}{X}\right)^2}\right] \qquad 4.17$$

B) Describing function analysis of the stepping motor including the throttle linkage limit switches

Figure 4-5 is a schematic representation of the non-linear element. Figure 4.6 shows the effect of the non-linearity on a sinusoidal signal of the form

$$z(t) = Z \text{ Sin } wt \qquad 4.18$$

The output y(t) may be expressed as a Fourier series as follows:

$$y(t) = Co + \sum_{n=1}^{\infty} (Cn \text{ Cos } n\,wt + Dn \text{ Sin } n\,wt) \qquad 4.19$$

where,

$$Cn = \frac{1}{\pi}\int_0^{2\pi} z(t) \text{ Cos } n\,wt\; d(wt) \qquad 4.20$$

and,

$$Dn = \frac{1}{\pi}\int_0^{2\pi} z(t) \text{ Cos } n\,wt\; d(wt). \qquad 4.21$$

Assuming the non-linearity to be symmetric

$$Co = 0. \qquad 4.22$$

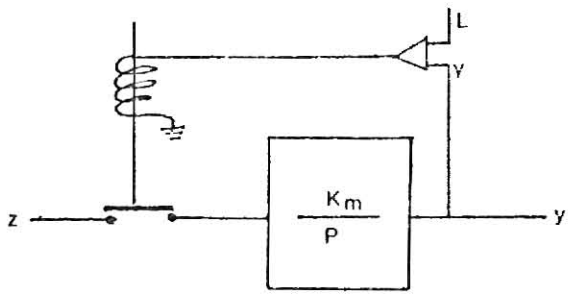
Neglecting the higher harmonics yields,

$$y(t) = C \text{ Cos } wt + D \text{ Sin } wt$$

$$= Y \text{ Sin } (wt + \theta) \qquad 4.23$$

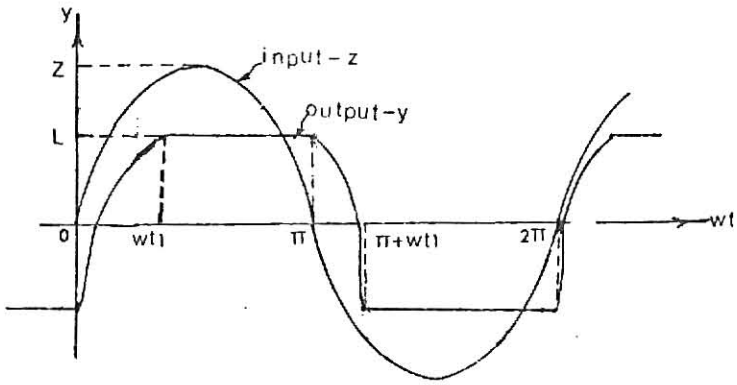
where,

$$Y = \sqrt{C^2 + D^2} \text{ and } \theta = \tan^{-1}\left(\frac{C}{D}\right) \qquad 4.24$$



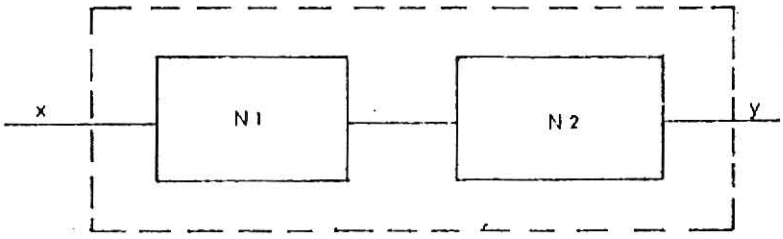
STEPPING-MOTOR AND THROTTLE LINKAGE LIMIT SWITCHES

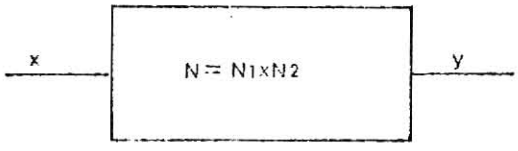
FIGURE-4·5



CHARACTERISTICS OF THE LIMIT SWITCHES AND STEPPING-MOTOR AS NON-LINEAR ELEMENT

FIGURE-4·6





DESCRIBING FUNCTION ANALYSIS OF NON-LINEAR ELEMENT

FIGURE-4·7

and where,

$$C = \frac{1}{\pi} \int_0^{2\pi} z(t) \text{ Cos } wt \; d(wt)$$

$$D = \frac{1}{\pi} \int_0^{2\pi} z(t) \text{ Sin } wt \; d(wt) \qquad 4.25$$

The characteristic of non-linearity is

$$y(t) = \begin{cases} Km \int z \, dt & o<wt<wt_1 \\ L & wt_1<wt<\pi \\ Km \int z \, dt & \pi<wt<\pi+wt_1 \\ -L & \pi+wt_1<wt<2\pi \end{cases} \qquad 4.26$$

Substituting the value of z(t) from equation 4.18 into equation 4.26 and evaluating the constants yields

$$y = \left[\frac{Km\ Z}{w} (1 - \text{Cos } wt) - L\right] \text{for } o<wt<wt_1 \qquad 4.27$$

and,

$$y = \left[-\frac{Km\ Z}{w} (1 + \text{Cos } wt) + L\right] \text{for } \pi<wt<\pi+wt_1 \qquad 4.28$$

At $t = t_1$,

$$y(t_1) = L = \left[\frac{Km\ Z}{w}(1 - \text{Cos } wt_1) - L\right] \qquad 4.29$$

which yields

$$\text{Cos } wt_1 = 1 - \frac{2\ wL}{Km\ Z} \qquad 4.30$$

Substituting into equation 4.25 yields

$$C = \frac{1}{\pi} \left[\int_0^{wt_1} \left\{-L + \frac{Km\ Z}{w} (1 - \text{Cos } wt)\right\} \text{Cos } wt \; d(wt) \right.$$
$$+ \int_{wt_1}^{\pi} (L) \text{ Cos } wt \; d(wt)$$
$$+ \int_{\pi}^{\pi + wt_1} \left\{L - \frac{Km\ Z}{w} (1 + \text{Cos } wt)\right\} \text{Cos } wt \; d(wt)$$
$$\left. + \int_{\pi + wt_1}^{2\pi} (-L) \text{ Cos } wt \; d(wt) \right] \qquad 4.31$$

Simplifying and solving yields

$$C = \frac{1}{\pi w} \left[(Km\ Z - 2\ wL) \text{ Sin } wt_1 - Km\ Z\ wt_1 \right] \qquad 4.32$$

Similarly, for D

$$D = \frac{1}{\pi}\left[\int_0^{wt_1}\left\{-L + \frac{Km\ Z}{w}(1 - \text{Cos } wt)\right\}\text{Sin } wt\ d(wt) + \int_{wt_1}^{\pi}(L)\text{Sin } wt\ d(wt) + \int_{\pi}^{\pi+wt_1}\left\{L - \frac{Km\ Z}{w}(1 + \text{Cos } wt)\right\}\text{Sin } wt\ d(wt) + \int_{\pi+wt_1}^{2\pi}(+L)\text{Sin } wt\ d(wt)\right] \quad 4.33$$

Simplifying and solving yields

$$D = \frac{2}{\pi}\left[\frac{Km\ Z}{w}(1 - \text{Cos } wt_1) + 2L\ \text{Cos } wt_1 - \frac{Km\ Z}{2w}\text{Sin}^2\ wt_1\right] \quad 4.34$$

Substituting the value of Cos wt_1 from equation 4.30 yields

$$C = \frac{Km\ Z}{\pi w}\left[\left(1 - \frac{2wL}{KmZ}\right)\text{Sin } wt_1 - wt_1\right]$$

or

$$C = \frac{KmZ}{2\pi w}(\text{Sin } 2\ wt_1 - wt_1)$$

and

$$D = \frac{4L}{\pi}\left(1 - \frac{wL}{KmZ}\right) \quad 4.35$$

where,

$$\text{Cos } wt_1 = 1 - \frac{2\ wL}{Km\ Z} \quad 4.36$$

Now,

$$Y = \sqrt{C^2 + D^2} \quad 4.37$$

and $\theta = \tan^{-1}\left(\frac{C}{D}\right)$ 4.38

The describing function is

$$N2 = \frac{Y}{Z}\angle\theta = \frac{\sqrt{C^2 + D^2}}{Z}\angle\tan^{-1}\left(\frac{C}{D}\right) \quad 4.39$$

In summary, let N be the describing function for the combined non-linear elements.

Then

$$N = N1 \times N2 \qquad 4.40$$

where,

$$N1 = \frac{2}{\pi}\left[\sin^{-1}\left(\frac{S}{X}\right) + \frac{S}{X}\sqrt{1 - \left(\frac{S}{X}\right)^2}\right]$$

and

$$N2 = \frac{\sqrt{C^2 + D^2}}{Z} \angle \tan^{-1}\left(\frac{C}{D}\right) \qquad 4.42$$

where,

C and D are given by equations 4.35.

4-5 CALCULATIONS OF THE PARAMETERS OF THE VEHICLE MODEL

The mathematical model of the vehicle has been assumed to be of the form

$$Gv = \frac{Kv}{(T_A P + 1)(T_B P + 1)} \qquad 4.43$$

The gain Kv has been approximated with the value 160 mph/inch. Utilizing the describing function analysis of the previous section, it is possible to calculate values of T_A and T_B which satisfy the conditions for the limit cycle amplitude and frequency observed. From describing function theory, the condition for a limit cycle is

$$Gv(jw) = -\frac{1}{K_c K_t N(w)} \qquad 4.44$$

where w is the frequency of the limit cycle.

Equating the phase angles in equation 4.44 yields

$$-\tan^{-1}(T_A w) - \tan^{-1}(T_B w) = -180^\circ - \angle N(w) \qquad 4.45$$

which may be simplified to

$$\frac{T_A w + T_B w}{1 - T_A T_B w^2} = \tan\left[180° + \tan^{-1}\left(\frac{C}{D}\right)\right] \qquad 4.46$$

Equating the magnitudes in equation 4.44 yields

$$\frac{Kv}{\sqrt{(T_A w)^2 + 1}\ \sqrt{(T_B w)^2 + 1}} = \frac{1}{K_c K_t |N|} \qquad 4.47$$

Solving equations 4.46 and 4.47 simultaneously yields values of T_A and T_B.

Table 4-2 shows the values of limit cycle amplitude and phase and corresponding values of T_A and T_B for the experimental results.

Average values of T_A and T_B from all tests is 47.1 seconds and 5.6 seconds, and the range of values found is 21.39 seconds to 72.06 seconds for T_A and 2.73 seconds to 17.7 seconds for T_B, respectively.

In Chapter 5, the average values of T_A and T_B are used to hypothesize a stabilizing controller for the control system.

TABLE 4-2

Test Number	Command Speed MPH	Counter Gains Up Channel K_c	Counter Gains Down Channel K_c	Accel/Decel Limit PPS Accel	Accel/Decel Limit PPS Decel	Average Accel/Decel Limit PPS	Limit Cycle Amplitude V MPH	Frequency of Limit Cycle W RAD/SEC	Time Constants T_A sec	Time Constants T_B sec
1	50	0.0666	0.0666	133.0	44.44	88.42	7.500	0.139		
2	50	0.10	0.10	133.0	44.44	88.72	4.375	0.142	66.028	17.70
4	50	0.10	0.10	66.67	66.67	66.67	7.031	0.170	46.70	4.632
5	50	0.10	0.10	47.62	133.0	90.31	6.250	0.164	37.90	3.619
6	50	0.0666	0.10	133.0	44.44	88.72	5.625	0.0666		
7	50	0.0666	0.0666	133.0	44.44	88.72	5.625	0.134		
8	50	0.10	0.10	133.0	44.44	88.72	4.690	0.157		
9	50	0.20	0.20	133.0	44.44	88.72	6.250	0.143	72.06	5.19
10	50	0.333	0.333	133.0	44.44	88.72	8.593	0.106		
11	50	0.333	0.333	133.0	44.44	88.72	8.906	0.088		
12	const. throttle	at ≈ 50 mph								
13	const. driving	at ≈ 50 mph								
14	50	0.10	0.10	74.0	74.0	74.0	5.625	0.176	33.86	2.044
15	40	0.10	0.10	74.0	74.0	74.0	4.219	0.169		
16	30	0.0666	0.0666	133.0	44.44	88.72	5.938	0.0921	68.53	7.910
17	30	0.10	0.10	133.0	44.44	88.72	5.938	0.147	62.17	5.129
18	30	0.20	0.20	133.0	44.44	88.72	5.781	0.143		
19	30	0.10	0.10	66.67	66.67	66.67	5.731	0.163	33.10	3.50
20	30	0.10	0.10	47.62	133.0	90.31	5.469	0.160	46.98	2.73
21	40	0.0666	0.0666	47.62	133.0	90.31	7.812	0.157	32.59	3.046
22	40	0.200	0.200	47.62	133.0	90.31	7.188	0.167	51.28	4.833
23	50	0.333	0.333	66.67	66.67	66.67	7.188	0.139	21.39	13.13
24	50	0.200	0.200	133.0	133.0	133.0	6.797	0.168	42.21	4.676
25	50	0.100	0.100	66.67	66.67	66.67	7.500	0.157		
								AVG	47.13	5.61

CHAPTER 5

SUMMARY AND RECOMMENDATIONS

CHAPTER 5

SUMMARY AND RECOMMENDATIONS

5-1 Introduction

The overview of the variable pulse-rate vehicle speed control system was presented in Chapter 1. Chapter 2 provided the detailed description of the subsystems. The experimental results were provided in Chapter 3 which were used to develop a mathematical model in Chapter 4. Appendix A provides all circuit diagrams and Appendix B provides equations for the curve fitting algorithm. This chapter provides a summary of results. Some recommendations are made, based on experience with the system.

5-2 Summary

A variety of problems were encountered during the study of the variable pulse-rate control system. Some of the problems encountered were concerning the kind of hardware used, the method of documentation, etc. For example, the importance of using solid teflon coated wire and making a good connection, making a list of connections which includes every pin of every socket, was realized. Most of these problems were solved, based on the experience gained with the system.

Some of the problems were related to the functioning of the integrated logic elements and circuits. For example, the problem related to the re-setting of the counters was serious. The counters were used in various sub-systems and they played a vital role in the operation of the variable pulse-rate control system. It was observed that the reset pulse was very short in time duration and frequently was not of full voltage magnitude. In many cases, this pulse was unsatisfactory for the action it was intended to cause. In many cases this problem was solved by addition of a one-shot multivibrator

device. This device was capable of giving a clean and sharp output pulse that was independent of the input pulse characteristic. Another good example in this category was the development of the blocking circuit associated with the circular up/down binary counter. The counting operation of the circular up/down binary counter was not a smooth and monotonic occurrence. The spurious pulses on the output channels of the counter prevented it from being a true error (differencing) device. The development of the blocking circuits enabled the counter to be a true error device.

There were problems related to the application of the variable pulse-rate system as a vehicle speed control system. It was possible to conduct the road tests with some constraints, for the evaluation of the system. The system exhibited a limit cycle type of operation. Basically, this mode of operation was unsatisfactory. It was concluded that the system is unstable. The nonlinear gain and second degree lag in the vehicle dynamics, results in the limit cycle type of operation of the system. The nonlinearities in the system preclude the establishment of a mathematical model based on simple linear system theory. An approximate linearization of the mathematical model has been made in Chapter 4.

The recommendations based on the problems which need further study and were beyond the scope of this investigation, are presented in the following section.

5-3 Recommendations

The following recommendations concern further research on the application of the variable pulse-rate control system as a vehicle speed control system.

A) Several attempts to operate the system without the DC to AC invertor

were made. Each time the attempt was made, it resulted in the failure of some electronic components in the system. It was observed that the automobile battery voltage was not constant at 12 volts. Usually it was higher than 12 volts. Also the noise on the battery supply resulted in a failure of some components in the system. This problem should be investigated so as to improve the usefulness of the system.

B) In the initial stages of the bench testing of the system a switch was introduced between the power amplifier and the stepping motor to avoid the failure of power amplifier components when the system was shut off. It was concluded that a possible cause of the failure of the power amplifier was the back voltage due to the inductive load of the stepping motor. The switch isolated the stepping motor from the rest of the system before the system was shut off. When the system was installed in the vehicle, there existed a problem of initially orienting the stepping motor. Everytime the system was initially started, there was 50% possibility that the stepping motor might lose its direction of rotation. The reason was, it could not sense the correct phase relationship of the power amplifier signals and therefore, reversed its direction of rotation. But it was observed that once it sensed the right phase relationship of the signals, its stepping (rotation) was consistant. The switch helped to shut off the system and orient the stepping motor in the right direction. The study of initial orientation of the stepping motor might lead to a study of developing a stepping motor that would sense the correct phase relationship of signals all the time.

C) The system operated in the limit cycle mode which is unsatisfactory for this application. For successful application of the system as a vehicle speed control system, the system should be stable. An attempt has been made in this section to discuss some of the stability techniques with reference

to the results of the mathematical model analysis in Chapter 4. This discussion is neither the only means of obtaining suitable performance nor has it been implemented or tested as a part of this work.

CASE I

In this case, the limit values will be avoided and assumed that the linear model is adequate. Then the counter gain K_c is calculated for the stable operation of the system.

For linear system,

$$GH = \frac{K_c K_m K_v K_t}{P(T_A P+1)(T_B P+1)} \qquad 5\text{-}1$$

where

K_m = Gain of the stepping motor and throttle limit switches

= 9.67×10^{-4} inch/pulse

K_v = Vehicle dynamic gain

= 160 mph/inch

K_t = Pulse-rate tachometer gain

= 106.66 PPS/mph

T_A = Vehicle time constant

= 46.70 sec

T_B = Vehicle time constant

= 4.632 sec

The characteristic equation 1 + GH = 0 gives

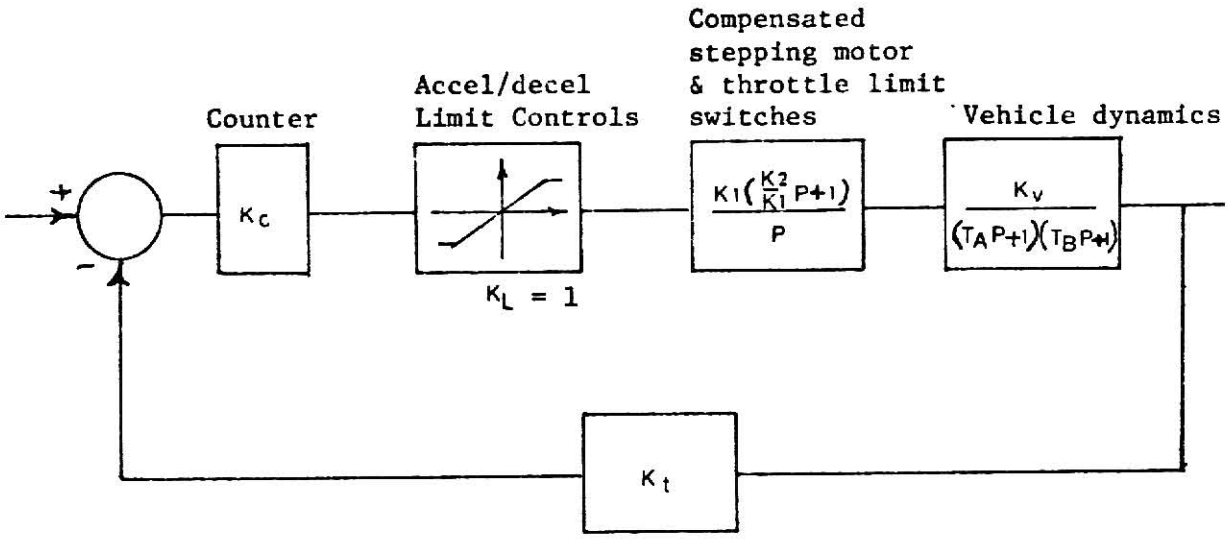
$$P(46.7\ P+1)(4.633\ P+1) + 16.504\ K_c = 0$$

$$216.3\ P^3 + 51.3\ P^2 + P + 16.504\ K_c = 0 \qquad 5.2$$

Using Routh's stability criterion, yields

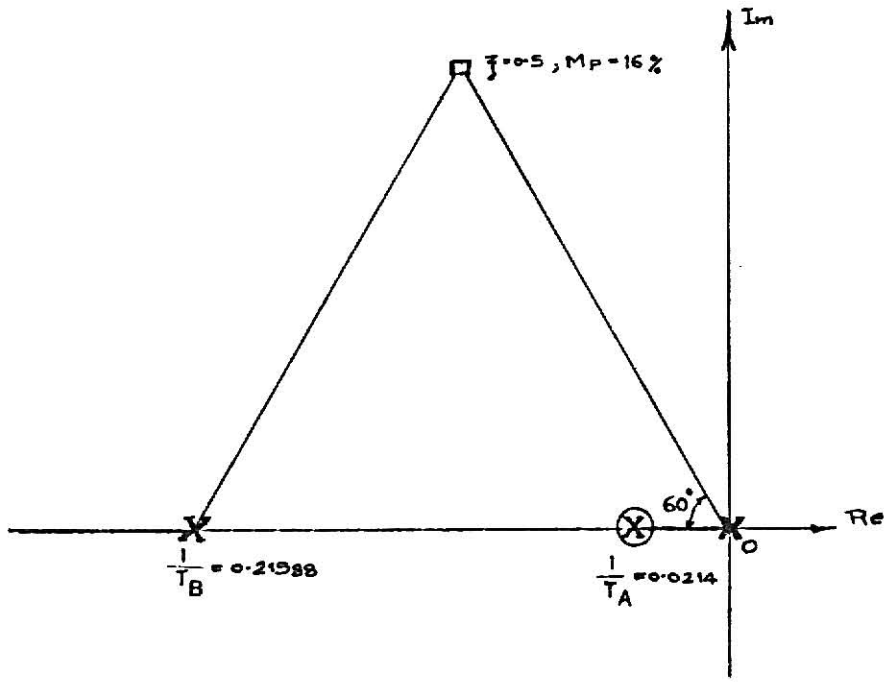
$$K_c = 0.0143785 = \frac{1}{69.548} \qquad 5.3$$

and w = 0.068 rad/sec.



ASSUMED LINEAR AND STABLE MODEL FOR THE SYSTEM

FIGURE 5-1



ROOT LOCUS — FIGURE 5-2

The counter gain $\frac{1}{69.548}$ is beyond the available counter gain range. To achieve the counter gain of the order of 1/69.548 requires more elements. Also the least peak time for w = 0.068 rad/sec, neglecting damping ratio, would be

$$tp = \frac{\pi}{w\sqrt{1-\zeta 2}} \qquad 5.4$$

$$= \frac{\pi}{0.068} = 46.20 \text{ seconds}$$

Picking a smaller value of gain so that

$\zeta = 0.5$ yields

$w \simeq 0.05$ rad/sec

and

$$tp = \frac{\pi}{0.05\sqrt{(1-0.5)^2}} = 72.21 \text{ seconds} \qquad 5.5$$

The above calculation suggests that by reducing the gain the system may be stabilized, but the response of the system is slower. The response time is in the range of 70 seconds while the system response time from the road tests is in the range of 25 seconds. Hence the system would become quite sluggish.

CASE II

In this case the system will be assumed to be linear and the stepping motor and the throttle linkage limit switch combination $(\frac{Km}{P})$ will be replaced by

$$\frac{K_1}{P} + K_2 = \frac{K_1(\frac{K_2}{K_1} P + 1)}{P}$$

For the linear system

$$GH(P) = \frac{K_c K_1 (\frac{K_2}{K_1})P + 1)}{} \times \frac{K_v K_t}{(T_A P+1)(T_B P+1)} \qquad 5.6$$

Assuming

$$\frac{K_2}{K_1} = T_A, \text{ yields} \qquad 5.7$$

$$GH(P) = \frac{K_c\ K_v\ K_t\ K_1}{P(T_B\ P+1)} \qquad 5.8$$

Test 4 will be used as a basis of calculation, where

K_c = Counter gain = 0.1

K_v = Vehicle dynamic gain = 160 mph/inch

K_t = Pulse-rate tachometer gain = 106.66 PPS/inch

T_A = Vehicle time constant = 46.70 sec

T_B = Vehicle time constant = 4.633 sec

Substituting these values in Equation 5.8 yields

$$GH(P) = \frac{0.1 \times 160 \times 106.67 \times K_1}{P(4.633\ P+1)}$$

$$= \frac{1706.72\ K_1}{P(4.633\ P+1)} \qquad 5.9$$

The characteristic equation is

$$1 + GH = 0$$

$$P(4.633\ P+1) + 1706.72\ K_1 = 0 \qquad 5.10$$

$$P^2 + 0.2158\ P + 368.38\ K_1 = 0 \qquad 5.11$$

Hence,

$$2\zeta w_n = 0.2158$$

and

$$w_n^2 = 368.38\ K_1 \qquad 5.12$$

Assuming a damping ratio $\zeta = 0.5$ which corresponds to a

percentage overshoot of Mp = 16% 5.13

yields

$$w_n = 0.2158$$

and

$$K_1 = 1.264 \times 10^{-4} = \frac{1}{7910.303} \qquad 5.14$$

It follows that for

$$K_2/K_1 = T_A = 46.70 \qquad 5.15$$

$$K_2 = 1.264 \times 10^{-4} \times 46.70$$

$$= 5.903 \times 10^{-3}$$

$$= \frac{1}{169.409} \qquad 5.16$$

Hence,

$$\frac{K_1 \left(\frac{K_2}{K_1}\right) P+1}{P} = \frac{(46.7\ P+1)}{7910.303\ P} \qquad 5.17$$

The above analysis suggests that it is possible to stabilize the system with a lead compensator. The hardware required to build the lead compensator might not be conventional. Therefore, a physical realization of the lead compensator for the variable pulse-rate system might not be simple.

D) The application of the variable pulse-rate system as a vehicle speed control system was difficult because of the vehicle time constants. Other applications of the variable pulse-rate system should be investigated which may not have the stabilization problem caused by the vehicle time constants.

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BIBLIOGRAPHY

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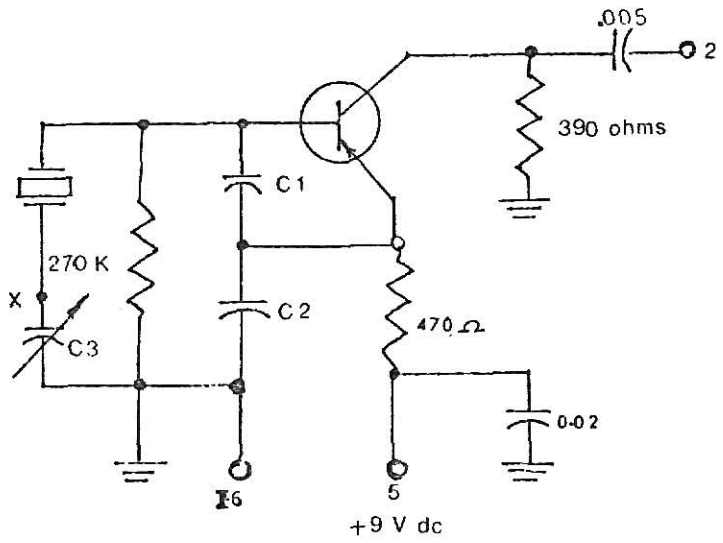
APPENDIX A



THE CLOCK — FIGURE A-1

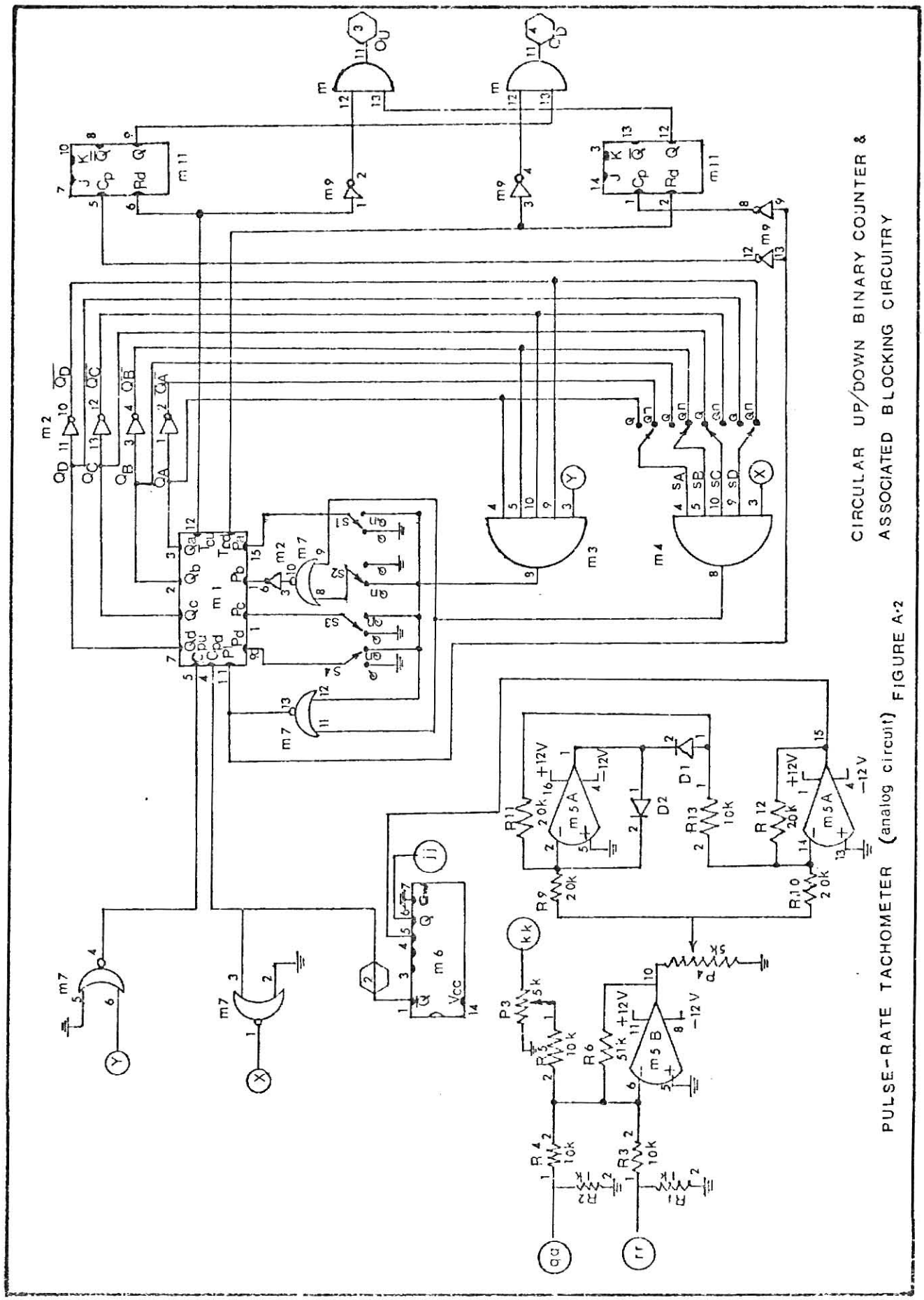
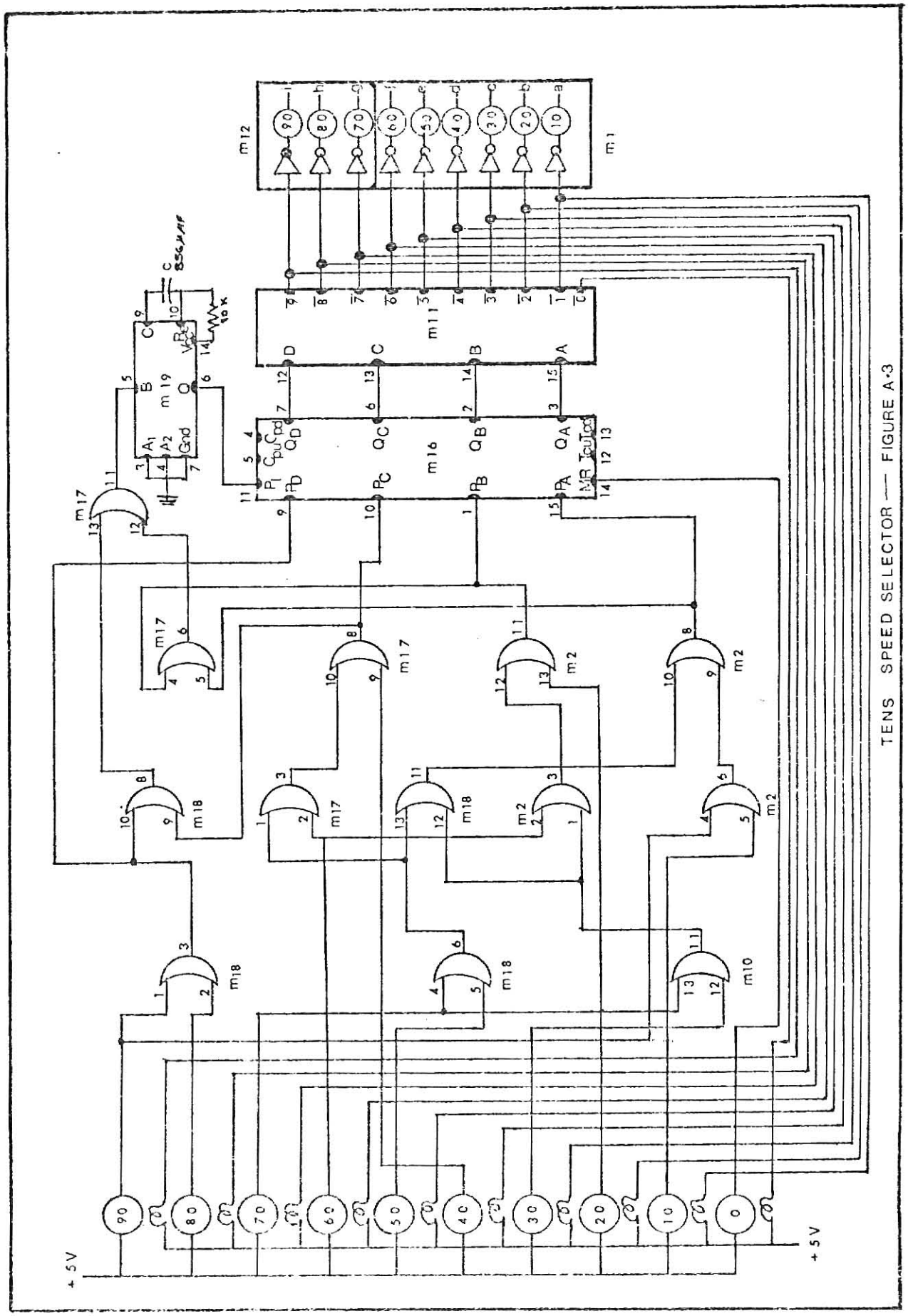
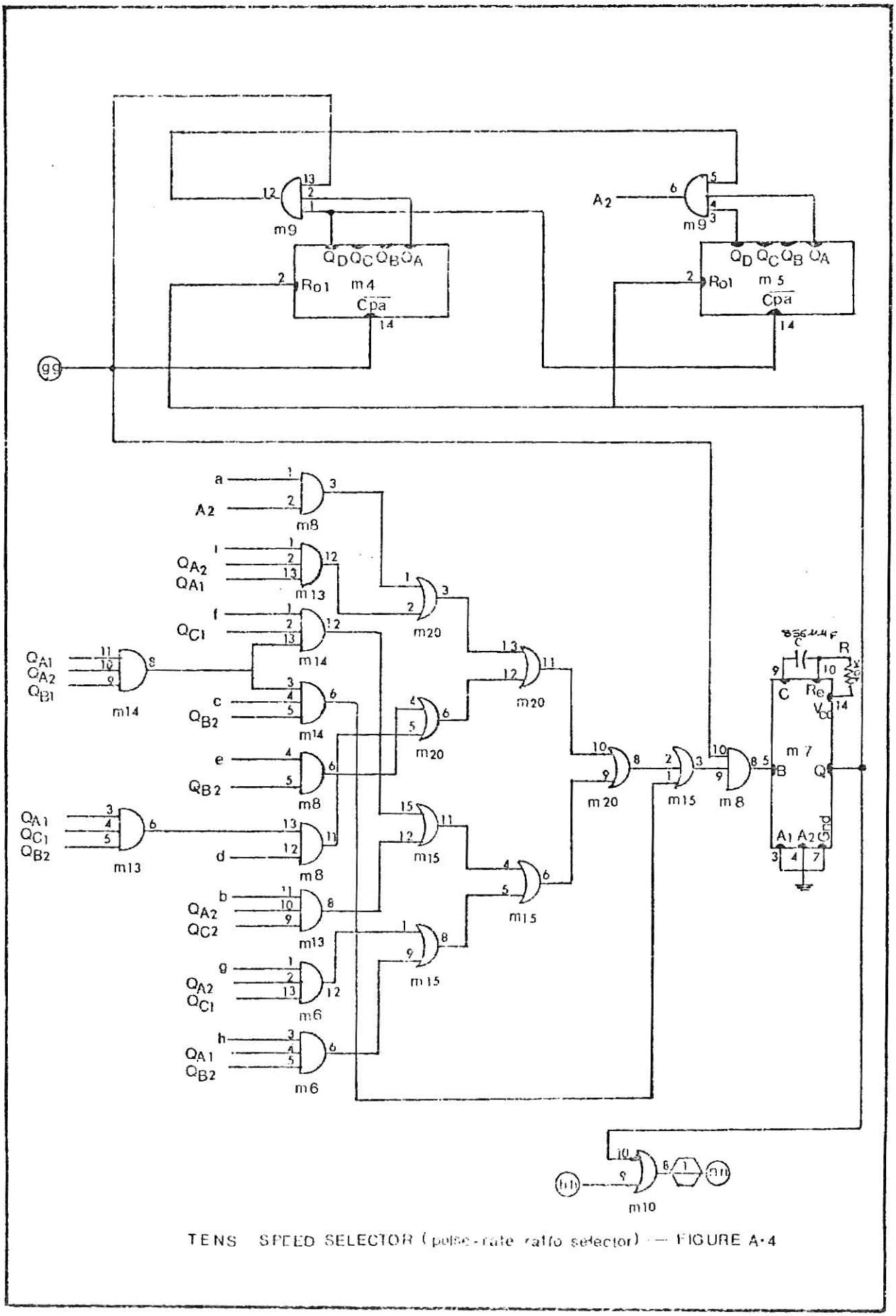

CIRCULAR UP/DOWN BINARY COUNTER &
ASSOCIATED BLOCKING CIRCUITRY
PULSE-RATE TACHOMETER (analog circuit)

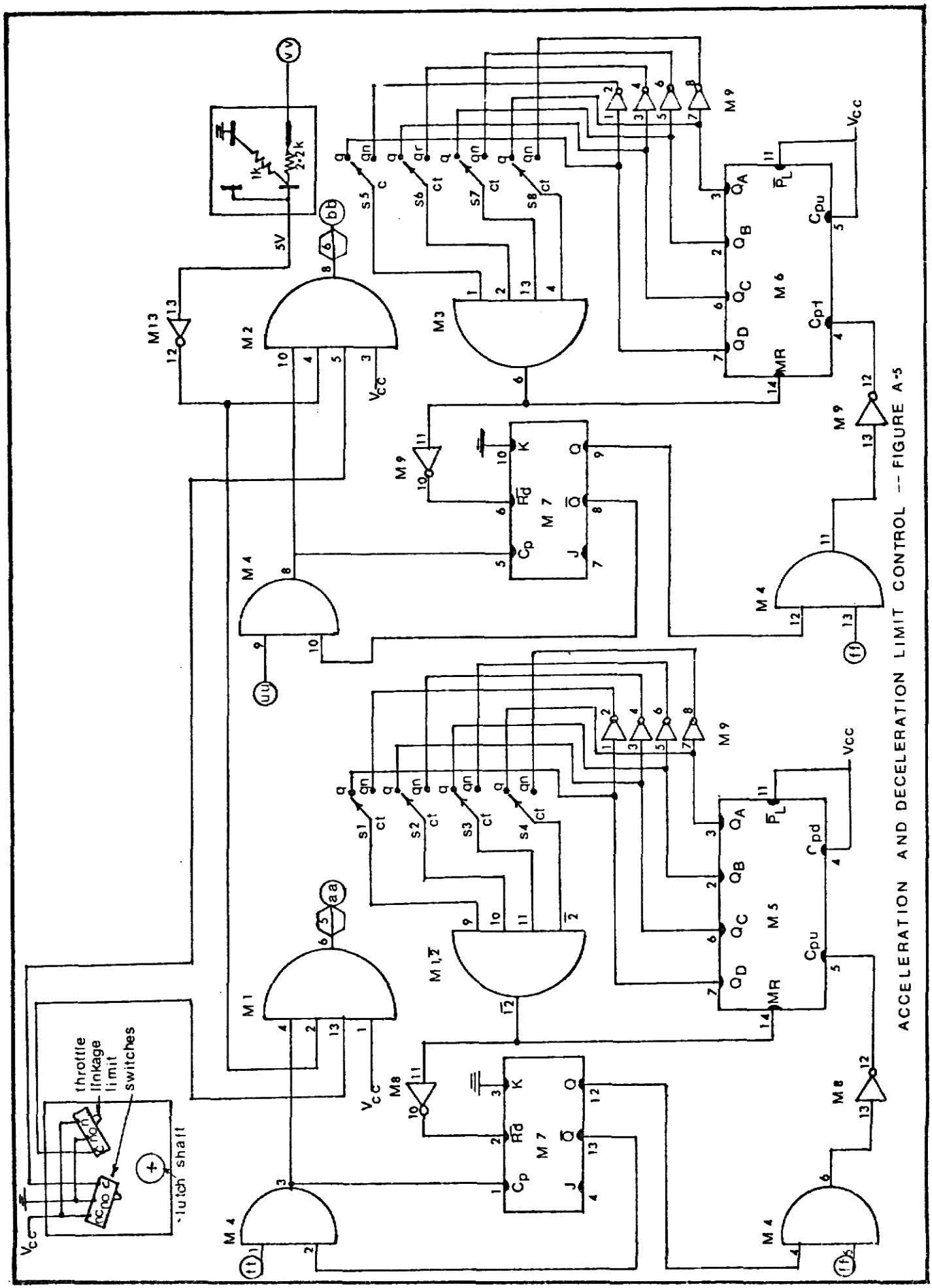
FIGURE A-2

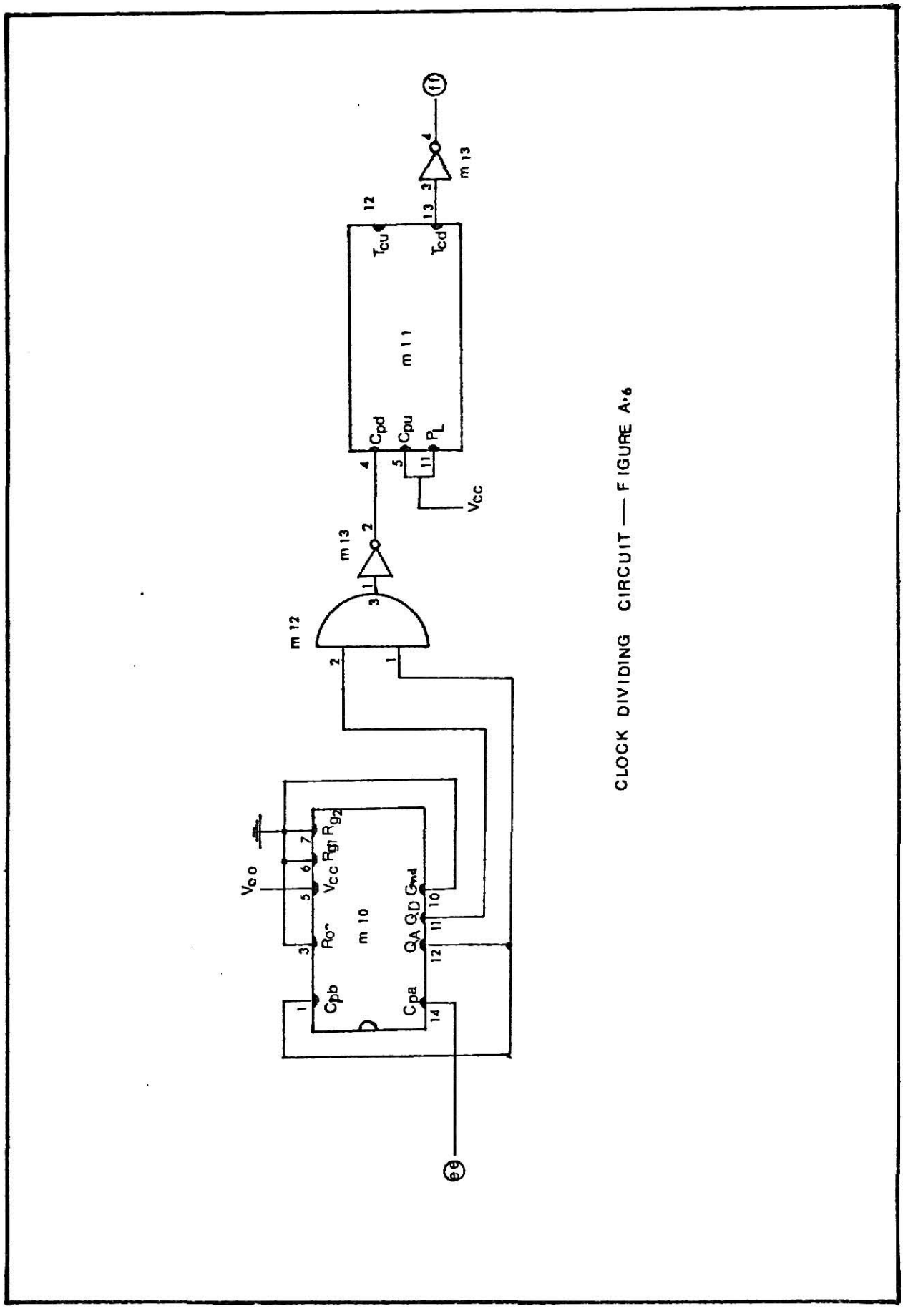


TENS SPEED SELECTOR — FIGURE A-3

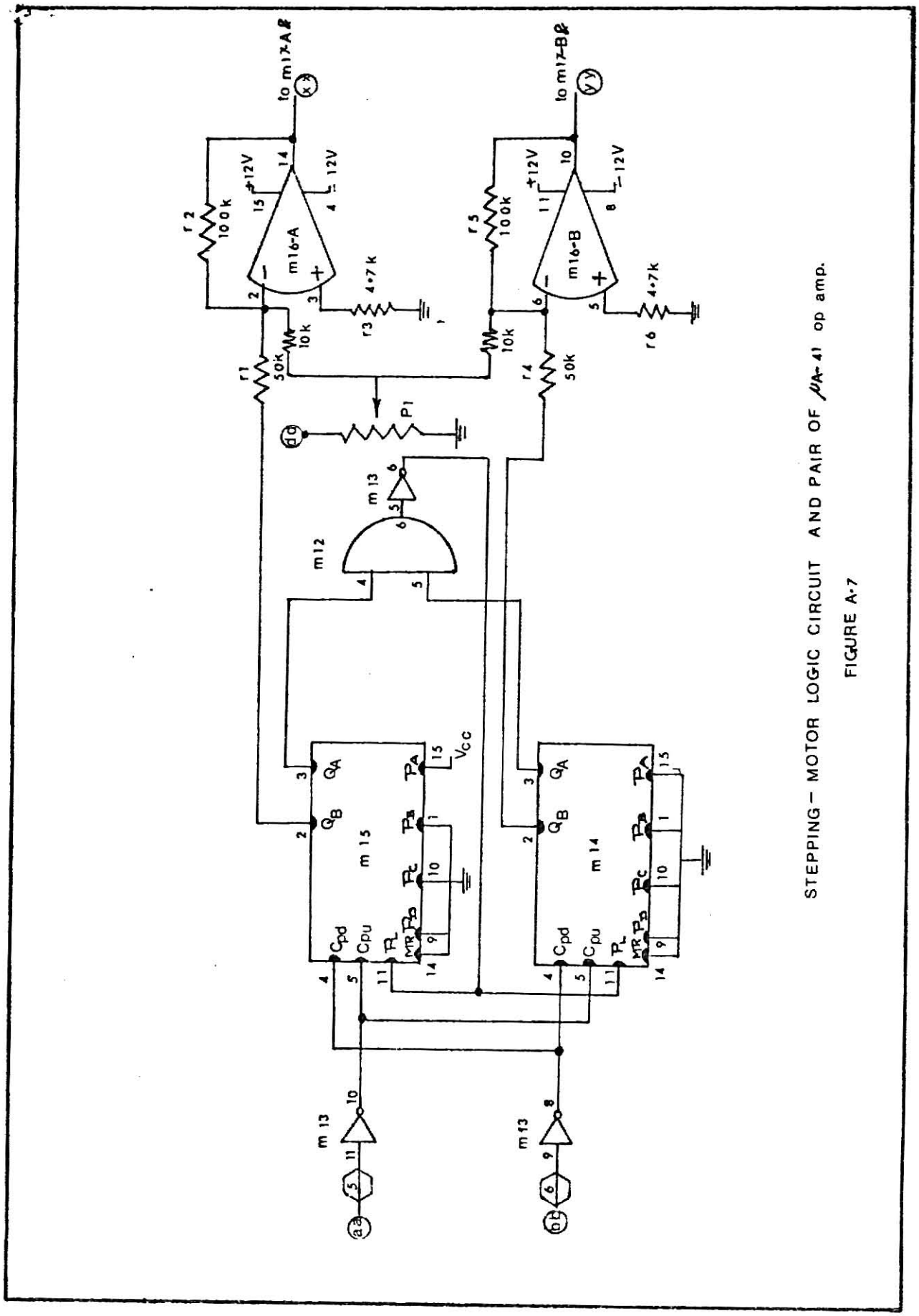


TENS SPEED SELECTOR (pulse-rate ratio selector) — FIGURE A-4


throttle linkage limit switches
clutch shaft
5V
1k
2.2k
M1
M2
M3
M4
M5
M6
M7
M8
M9
M13
M1,2
Vcc
s1
s2
s3
s4
s5
s6
s7
s8
aa
bb
uu
ff
ACCELERATION AND DECELERATION LIMIT CONTROL -- FIGURE A-5

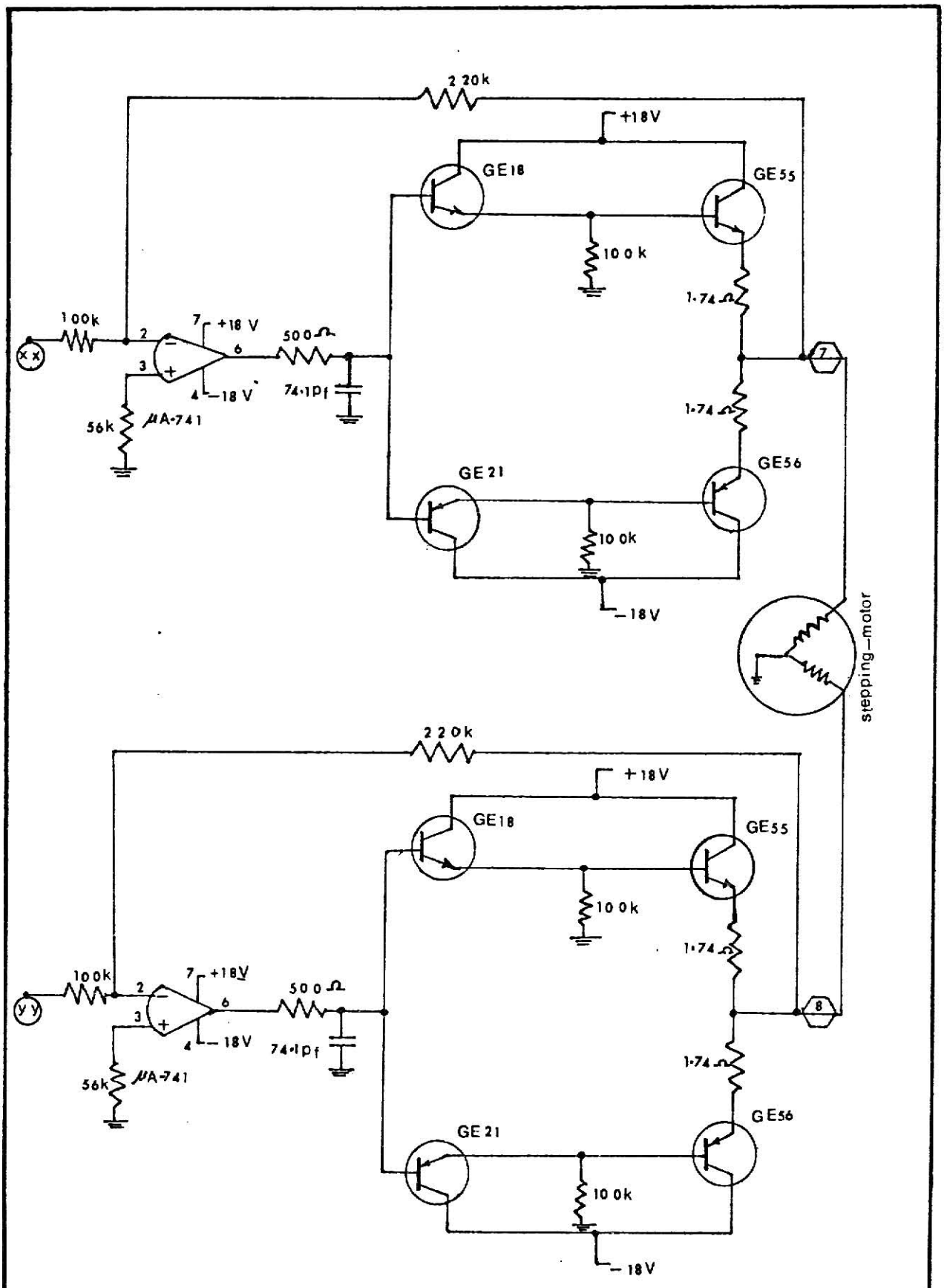


CLOCK DIVIDING CIRCUIT — FIGURE A·6

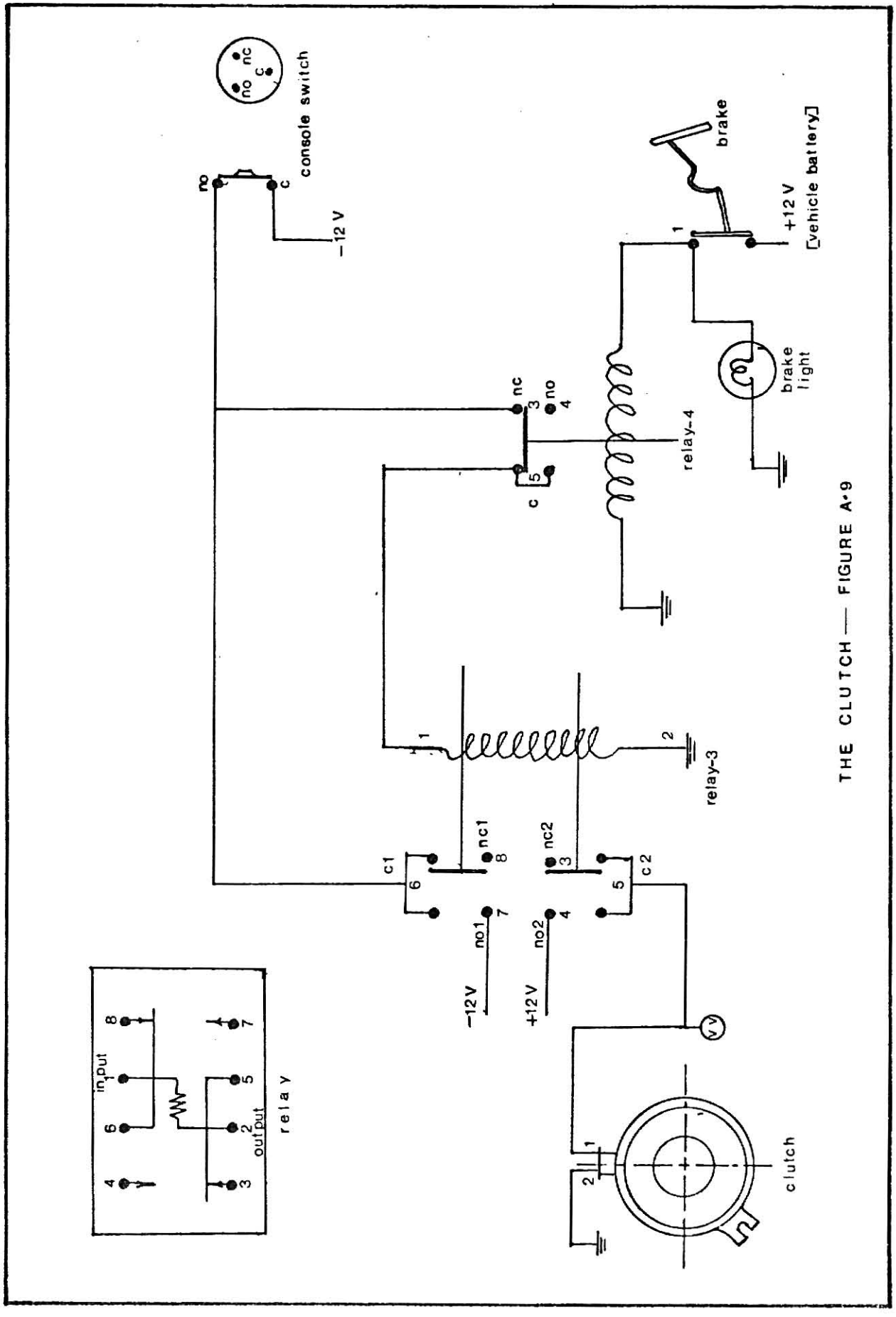


STEPPING – MOTOR LOGIC CIRCUIT AND PAIR OF μA-41 op amp.

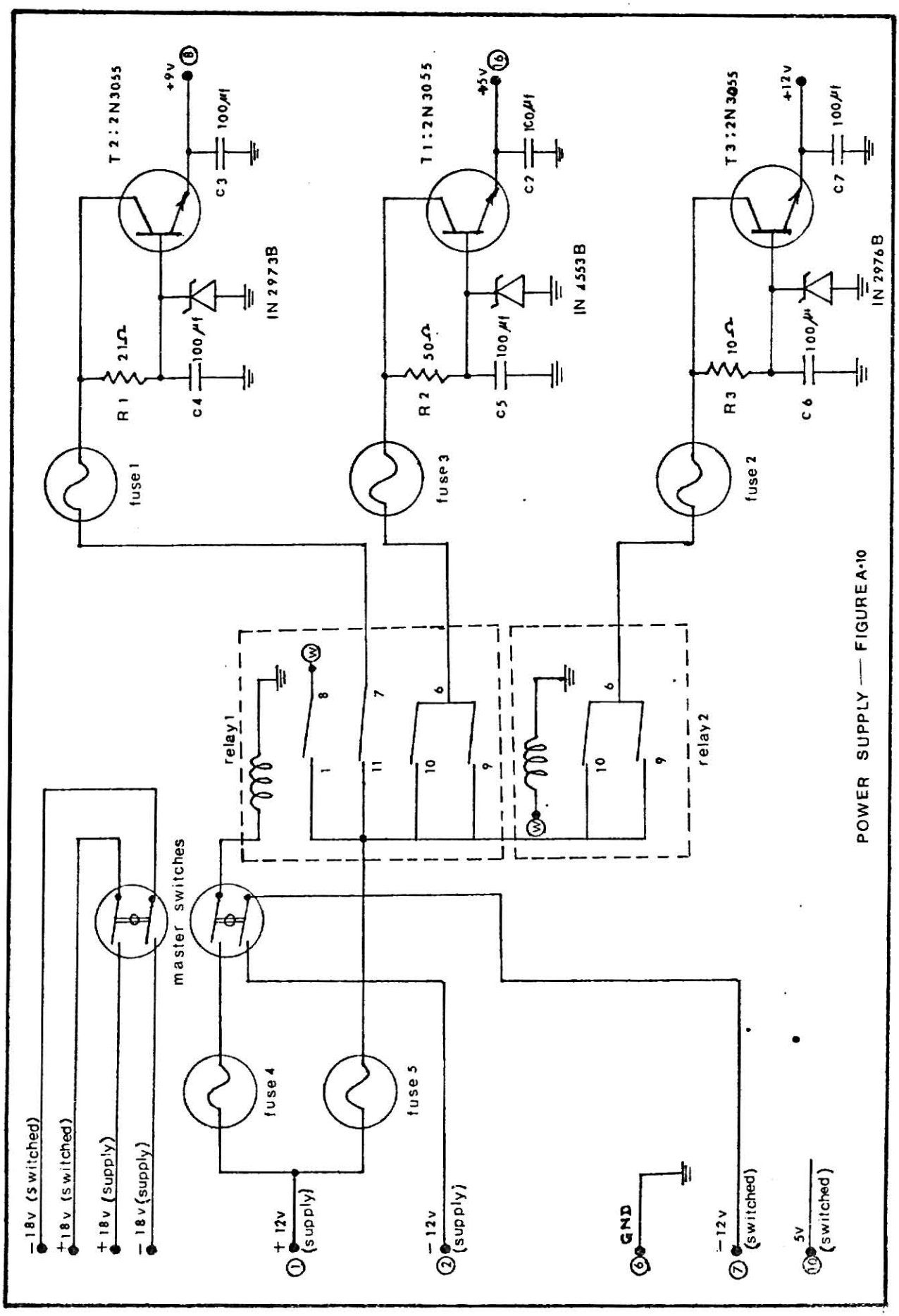
FIGURE A-7



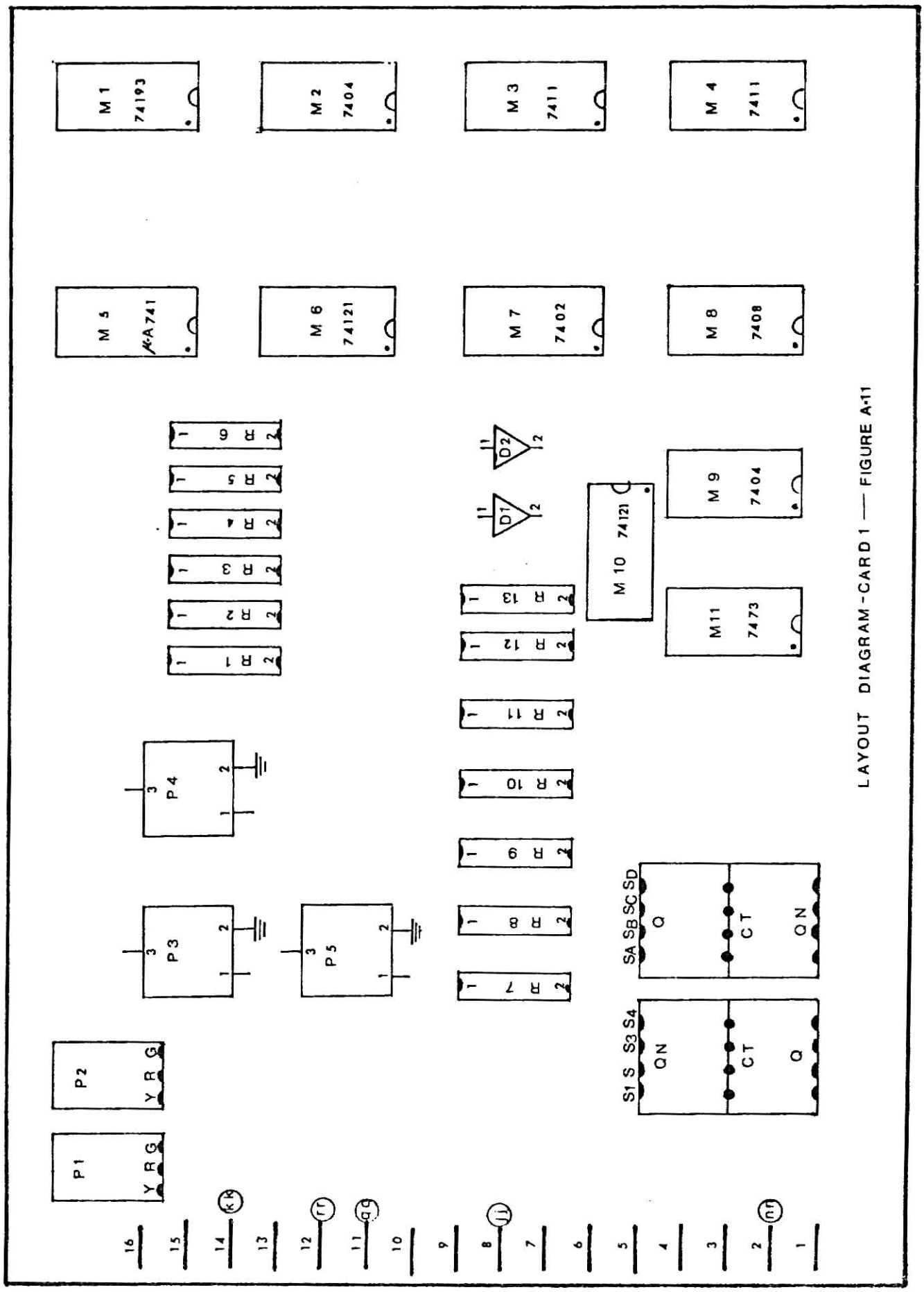
POWER AMPLIFIER — FIGURE A·8



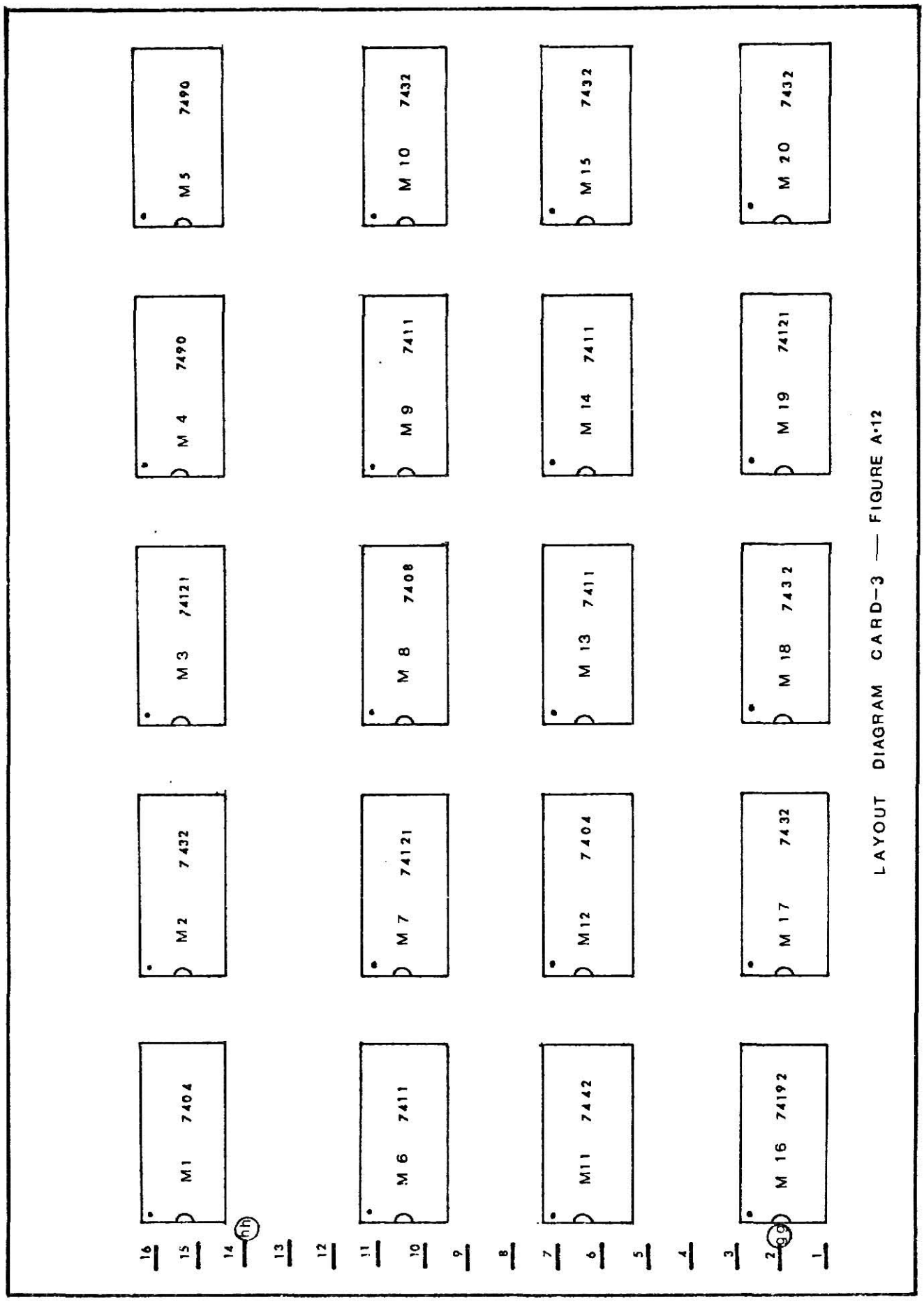
THE CLUTCH — FIGURE A·9



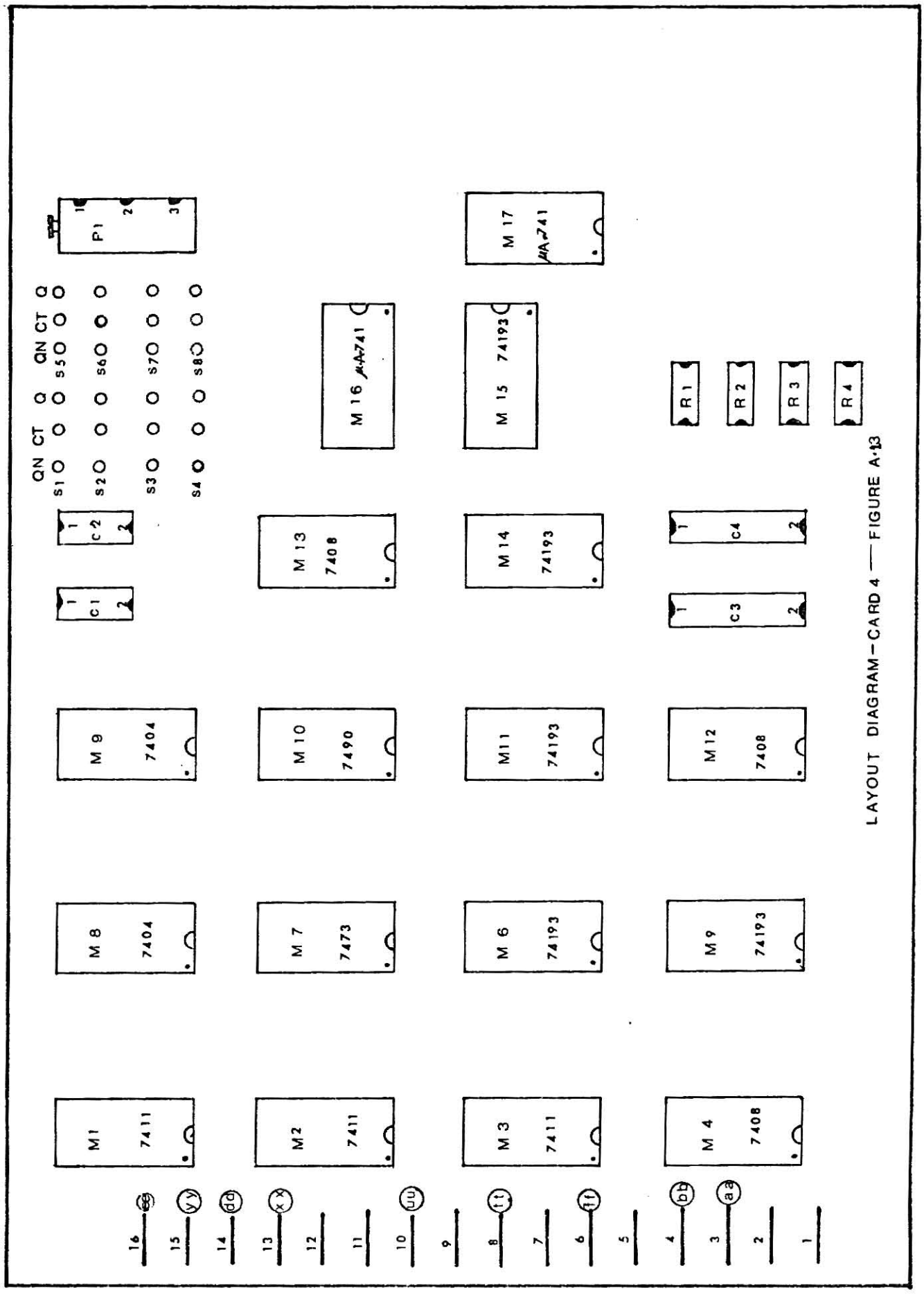
POWER SUPPLY — FIGURE A·10



LAYOUT DIAGRAM-CARD 1 — FIGURE A-11



LAYOUT DIAGRAM CARD-3 — FIGURE A-12



LAYOUT DIAGRAM—CARD 4 — FIGURE A-13

LIST OF SYMBOLS

SYMBOL	FIGURE NUMBER AND PAGE
①	1.1, 3; A.2, 105; A.4, 197
②	1.1, 3
③	1.1, 3; A.2, 105
④	1.1, 3; A.2, 105
⑤	1.1, 3; A.5, 108; A.7, 110
⑥	1.1, 3; A.5, 108; A.7, 110
⑦	1.1, 3; A.8, 111
⑧	1.1, 3; A.8, 111
a	A.2, 106; A.4, 107
b	A.3, 106; A.4, 107
c	A.3, 106; A.4, 107
d	A.3, 106; A.4, 107
e	A.3, 106; A.4, 107
f	A.3, 106; A.4, 107
g	A.3, 106; A.4, 107
h	A.3, 106; A.4, 107
i	A.3, 106; A.4, 107
aa	A.4, 107; A.7, 110; A.13, 116
bb	A.4, 107; A.7, 110; A.13, 116
dd	A.7, 110; A.13, 116
ee	A.6, 109; A.13, 116
ff	A.4, 107; A.6, 109; A.13, 116
gg	A.4, 107; A.12, 115
hh	A.4, 107; A.12, 115
jj	A.2, 105; A.11, 114
kk	A.2, 105; A.11, 114
nn	A.4, 107; A.11, 114
qq	A.2, 105; A.11, 114
rr	A.2, 105; A.11, 114
tt	A.4, 107; A.13, 116
uu	A.4, 107; A.13, 116
vv	A.5, 108; A.9, 112
xx	A.7, 110; A.8, 111; A.13, 116
yy	A.7, 110; A.8, 111; A.13, 116

APPENDIX B

APPENDIX B

The data obtained from the road tests was plotted as shown in Figures 1 to 25 at the end of Chapter 3. These plots were drawn with the help of the computer.

A cubic curve fitting algorithm was developed to provide a smooth curve between the data values. The cubic polynomial of the form

$$V = B_0 + B_1 + B_2\, t^2 + B_3\, t^3 \qquad \text{B-1}$$

was chosen. The slope of the curve is

$$\frac{dv}{dt} = B_1 + 2B_2 t + 3B_3 t^2 \qquad \text{B-2}$$

The values of B_o, B_1, B_2 and B_3 are to be chosen so that the curve between i^{th} and $(i+1)^{st}$ data points passes through the i^{th}, $(i + 1)^{st}$ and $(i + 2)^{nd}$ data points and has continuous slope at the i^{th} data point with the curve drawn between $(i-1)^{st}$ and i^{th} data points. This provides a smooth continuous curve through all the data points as may be observed from the plots.

The equations for the curve passing through point i^{th}, $(i + 1)^{st}$ and $(i + 2)^{nd}$ data points are given by

$$V_i = B_o + B_1\, T_i + B_2\, T_i^2 + B_3\, T_i^3 \qquad \text{B-3}$$

$$V_{i+1} = B_o + B_1\, T_{i+1} + B_2\, T_{i+1}^2 + B_3\, T_{i+1}^3 \qquad \text{B-4}$$

$$V_{i+2} = B_o + B_1\, T_{i+2} + B_2\, T_{i+2}^2 + B_3\, T_{i+2}^3 \qquad \text{B-5}$$

and continuous slope at the i^{th} point is $DVI = B_1 + 2B_2T_i + 3B_3T_i^2$ B-6

where DVI is the slope at the i^{th} point from the curve drawn between the $(i - 1)^{st}$ and i^{th} data points. This provides a smooth continuous curve through all the data points.

The equations B-3, B-4, B-5, and B-6 can be solved as follows to obtain the coefficients.

Equation B-6 gives

$$B_1 = DVI - 2\, B_2\, T_i - 3\, B_3\, T_i^2 \qquad \text{B-7}$$

Solving equation B-6 and B-3, yields

$$B_o = (V_i - DVI \times T_i) + B_2 T_i^2 + 2 B_3 T_i^3 \qquad \text{B-8}$$

Substituting B-7 and B-8 into B-4 and reducing yields

$$B_2 + (T_{i+1} + 2 T_i) B_3 = \frac{V_{i+1} - V_i}{(T_{i+1} - T_i)^2} - \frac{DVI}{(T_{i+1} - T_i)} \qquad \text{B-9}$$

Substituting B-7 and B-8 into B-5 and reducing yields

$$B_2 + (T_{i+2} + 2T_i)B_3 = \frac{V_{i+2} - V_i}{(T_{i+2} - T_i)^2} - \frac{DVI}{(T_{i+2} - T_i)} \qquad \text{B-10}$$

Substracting B-9 from B-10 and noting that

$$(T_{i+2} - T_i) = (T_{i+2} - T_{i+1}) + (T_{i+1} - T_i)$$

$$= 2(T_{i+1} - T_i)$$

yields

$$B_3 = \frac{V_{i+2} - 4 V_{i+1} + 3 V_i + 2 DVI (T_{i+1} - T_i)}{4(T_{i+1} - T_i)^3} \qquad \text{B-11}$$

Manipulating equation B-9 yields

$$B_2 = \frac{V_{i+1} - V_i}{(T_{i+1} - T_i^2)} - \frac{DVI}{(T_{i+1} - T_i)} - (T_{i+1} + 2T_i)B_3 \qquad \text{B-12}$$

where

$(T_{i+1} - T_i)$ = constant.

Solve equations in order of B-11, B-12, B-7 and B-8 and obtain the coefficients B_3, B_2, B_1 and B_0. These coefficients are then used by the curve fitting algorithm and it plots progressively a smooth curve between the data points.

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ACKNOWLEDGEMENTS

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I desire to dedicate this thesis to the memory of my grandfather, Ramchandra Trimbak Chande.

VITA

VITA

Dilip Dattatraya Chande was born March 31, 1950 in Maroli-Surat district, Gujarat State, India, to Dattatraya Ramchandra Chande and Vijoya Dattatraya Chande. He attended elementary and high school in Bombay, Maharoshtra State. He earned a diploma L.M.E. in mechanical engineering from Victoria Jubilee Technical Institute, Bombay in 1970 and a B.E. degree in mechanical engineerging from the University of Bombay in 1973.

During in-plant training required for the award of L.M.E., he worked with M/S Godrej and Boyce Mfg. Co. Pvt. Ltd., Bombay and completed a project entitled "Method Improvements and Standardization of Rivets", in their typewriter division. During summer vacations he had an opportunity to work with M/S Hind Rectifiers Ltd and M/S. Guest Keen Williams Ltd., Bombay. He completed a project carried out at M/S Hind Rectifiers Ltd., entitled "Introducing Corporate Planning at M/S. Hind Rectifiers Ltd.", as a partial requirement for his Bachelor of Engineering degree.

In August 1973, he enrolled in the Graduate School at Kansas State University, Manhattan, Kansas as a candidate for the Master of Science degree in mechanical engineering. While there he was a graduate research assistant in the Department of Mechanical Engineering.

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DESIGN, FABRICATION AND EVALUATION OF A VARIABLE PULSE-RATE VEHICLE SPEED CONTROL SYSTEM

by

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AN ABSTRACT OF A THESIS

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MASTER OF SCIENCE

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ABSTRACT

The design, construction and evaluation of a prototype variable pulse-rate system to automatically control the speed of an automobile are presented in this thesis.

The objective of this work is to investigate the problems associated with the implementation of a variable pulse-rate control system. This investigation is carried out by the design, fabrication and evaluation of a vehicle speed control system.

The variable pulse-rate vehicle speed control system controls the position of the throttle of the carburetor of an automobile such that the speed of the automobile is at all times maintained at an external command-speed value. A clock and speed selector and a pulse-rate tachometer are two of the subsystems of the variable pulse-rate control system. A pulse-rate proportional to the command-speed is derived from the speed selection circuit. The clock signal is divided down in the speed selector circuit by the necessary factor depending upon the command-speed value. The pulse-rate tachometer produces pulses at a rate proportional to the actual speed of the vehicle. These two pulse-rate signals are compared by a circular up/down binary counter. The up input channel of this counter receives the pulse-rate proportional to the command-speed. The down input channel receives the pulse-rate proportional to the speed of the automobile viz the "feed-back pulse-rate". The counter and associated blocking circuit, essentially takes the difference between the "command pulse-rate" and the "feed-back pulse-rate." If the "command pulse-rate"

is greater than the "feed-back pulse-rate"; a pulse stream with rate, proportional to the difference between the two input signals will appear on the up output channel. The down output channel won't have any pulses. Conversly, if the "feed-back pulse-rate" is greater than the "command pulse-rate", a stream of pulses at a rate proportional to the difference between the two input signals will appear on the down output channel. The up output channel won't have any pulses.

The constant of proportionality between the difference in the input pulse-rates and the output pulse-rate is adjustable and is referred to as the "counter gain."

The output of this circuit passes through an acceleration/deceleration limit control circuit before being applied to the circuit which controls the stepping-motor. The stepping-motor control circuitry includes the logic to control the direction and the rate of stepping as well as the power amplifier stage required to handle the current drawn by the stepping-motor. The stepping-motor controls the position of the throttle such that the speed of the vehicle is maintained at the command speed. A detailed description of the design, fabrication and evaluation of each component of the system is presented in the thesis.

Bench tests as well as road tests were conducted to evaluate the system's performance and to investigate its limitations. In the road tests the system exhibited a limit cycle type operation. An investigation of the effect of the various gain and limit adjustments and of command speed showed that they do not have a significant effect on the frequency or amplitude of this limit cycle. Basically, this mode of operation is unsatisfactory. Attempts to stabilize the operation by gain reduction

result in a system which is too sluggish. An active lead compensation stabilizing scheme is proposed, but its implementation is beyond the scope of this work. As mentioned above, the system has a variety of gain and limit adjustments. A detail discussion of the tests conducted and the results obtained with conclusions and recommendations for further improvement of the system is provided.