Microstructured silicon carbide neutron detectors

by

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Abstract

Silicon carbide is a material of interest in many ventures as an intriguing semiconducting material for use as high voltage, high temperature, high power, or high frequency devices. Silicon carbide is physically extremely tough and durable and is also very chemically resistant.

The work presented here details using silicon carbide (SiC) as the semiconducting substrate for a high-efficiency neutron detector. The work begins with the fabrication of planar SiC neutron detectors utilizing ^{10}B as the neutron conversion material. The SiC substrate was patterned via photolithography techniques prior to the deposition of an etchant mask. The following materials were used as etchant mask materials; nickel, indium tin oxide, and aluminum. The SiC devices were plasma etched using SF_6 based gas chemistries. The desired trench profile was 4 microns wide with desired depth between 10 and 20 microns. The formation of microfeatures within the trenches was observed during several etching trials as well as the trench profile narrowing to a point. After etching, titanium/gold contacts were fabricated using e-beam evaporation and various masking techniques. Next the devices were electrically tested for leakage current and capacitance. Typical leakage current was <10 pA at 100 V applied bias with a capacitance of <10 pF. Then the devices were backfilled with enriched ^{10}B powder.

The backfilled devices were tested with alpha particles, gamma rays, and neutrons. The neutron sources used were ^{252}Cf and the Kansas State University TRIGA Reactor diffracted beamport. The devices proved to have low gamma sensitivity with respect to neutrons. When the devices were irradiated by high-activity alpha particle sources, significant charge trapping and device polarization was observed.

The initial devices were 10 mm x 10 mm, but due to complications during the etchant mask formation, the device size was changed to 5 mm x 5 mm. The 5 mm x 5 mm devices were

tested for neutron sensitivity using the ^{252}Cf source and the diffracted beamport. Thermal neutron efficiency of 2.28±0.031% was measured.

The final SiC wafer was patterned with the top contact and etchant mask. However, during dicing, the layers delaminated and peeled of the SiC substrate. Substantial efforts were made to pattern the remaining partial wafer to little success.

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Acknowledgements

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And a special thank you to Dr. McGregor for his support and guidance.

Dedication

I want to dedicate this work to my wife, Ellaine, who always gives me her fullest support and love. My son, Keaton, with his positive outlook on all things and his ability to make me laugh. My daughter, Joslyn, with her bubbly demeanor and baby giggles. And last but not least, my parents, Steve and Trudi, for their endless support of all of our endeavors.

Chapter 1 - Introduction

Silicon carbide (SiC) exhibits characteristics that make it an intriguing semiconducting material for use as high voltage, high temperature, high power, or high frequency devices. SiC is physically extremely tough and durable and is also very chemically resistant. In 1893, Edward Goodrich Acheson was the first to manufacture SiC in powder form. From there, SiC was mass produced for use as the abrasive material on grinding wheels and other abrasive uses. Other commercial uses are high-strength items such as high-end brake pads, clutches, or embedded in bulletproof vest ceramic plates [1, 2].

SiC has been intriguing as an electronic material since 1907, when Henry Round demonstrated a functioning LED on SiC [1, 3, 4]. Jan Anthony Lely first reported the growth of SiC platelets in 1955 [5]. This early growth progress soon led to the growth of SiC crystal boules and widespread use of SiC as an electronic material. SiC has also been used to make heat dissipating substrates for other electronic materials.

In recent years, SiC has been used to fashion power electronics such as Schottky diodes, field effect transistors (FETs), capacitors, and radiation detectors. As stated above, SiC electronic properties give it numerous advantages over more conventional materials such as silicon or gallium arsenide. With its high voltage breakdown, SiC devices can be operated with substantially higher operating bias. Due to its excellent thermal characteristics, devices can function at several hundred degrees Celsius [3].

However, due to SiC's chemical inertness and durable physical characteristics, it is an extremely challenging material to grow high-quality single crystal boules. Temperatures during SiC crystal growth may be over 2700 ºC and the SiC source material will actually sublime into

the vapor phase instead of forming a melt solution. Extensive work has been conducted in analyzing the crystal growth processes and how to best reduce unintentional dopants, while improving on desirable dopants. With proper doping, the crystal's resistivity can be increased to the point where the material is considered semi-insulating versus semiconducting.

The purpose of this project was to create neutron detectors from semi-insulating SiC wafers. The detectors use ^{10}B as the neutron conversion material and the SiC substrate as the charged particle detectors. To improve device performance, the SiC substrate is dry etched using plasma etching techniques. By etching trenches into the substrate, it is possible to increase a device's overall detection efficiency. Standard thin film techniques such as photolithography, metal contact formation, device mounting, and wire bonding were used to manufacture the detectors. Detector performance was tested using alpha particle and gamma-ray sources. Neutron sensitivity was tested using a ^{252}Cf source and the TRIGA Reactor at Kansas State University.

Chapter 2 - Background

Within this chapter, common neutron reactive materials will be presented. Also discussed are the discoveries of silicon carbide, the evolution of the growth processes of silicon carbide, silicon carbide's polytypes, and methods for plasma etching of silicon carbides, Photolithography techniques and types of photoresist will be discussed. Also the neutron sources used to test the SiC detectors will be detailed.

2.1 Neutron Reactive Materials

Because neutrons possess a net charge of zero, they do not interact with their surrounding medium though coulombic interactions [6]. Therefore, neutrons will interact with a nucleus of the surrounding medium and either be scattered or be absorbed. The probability that a neutron will interact per unit path length is represented by that material's cross section. In other words, a material with a high cross section is more likely to interact with a passing neutron. When a material has a low cross section, a neutron is less likely to undergo any interactions within a unit distance.

To act as a good neutron detector it is important for a material to not only have a relatively high neutron cross section, but must also produce observable event after interacting with a neutron. Typically, the observable event is the release of charged particles or characteristic gamma rays. Some of the more commonly used neutron reactive radioisotopes are ^{3}He, ^{6}Li, and ^{10}B [7]. The radioisotope ^{3}He has an isotopic natural isotropic abundance of 0.00014% [8], however, most of the ^{3}He gas used in the detector industry is produced as a

byproduct of radioactive tritium decay [9]. ^{3}He has a cross section of 5333 barns [8]. When a neutron is absorbed by a ^{3}He nucleus, a triton and a proton are released (Eq. 2.1).

$$^{3}He(n,p)\ ^{3}H \qquad \textit{Eq. 2.1}$$

Natural lithium contains 92.5% ^{7}Li and 7.5% ^{6}Li, the latter of which has a cross section of 940 barns. When a neutron interacts with a ^{6}Li nucleus, an alpha particle and a triton are emitted.

$$^{6}Li(n,t)\ ^{4}He \qquad \textit{Eq. 2.2}$$

The primary neutron converter material used for this work was boron. Natural boron contains 80% ^{11}B and 20% ^{10}B. ^{10}B has a neutron cross section of 3835 barns [8]. When ^{10}B absorbs a neutron, it may undergo two different reaction branches as seen below in Eq. 2.3. For both branches, the boron is converted into a lithium ion and an alpha particle [6, 10] and have a combined energy of 2.792 MeV. However, the most common reaction (94%) leaves the Li atom in an excited state, which in turn will emit a 0.480 MeV gamma ray as it de-excites, which lowers the kinetic energy of the lithium ion and alpha particle. Therefore, the reaction products from the 6% branch will have greater kinetic energy than the 94% branch reaction products. Having greater kinetic energy gives the reaction products corresponding greater penetration ranges.

$$^{10}B(n,\alpha)\ ^{7}Li \rightarrow \begin{cases} ^{7}Li(1.015\ MeV) + \alpha(1.777\ MeV) & 6\% \\ ^{7}Li(0.840\ MeV) + \alpha(1.470\ MeV) + \gamma(0.480\ MeV) & 94\% \end{cases} \quad \textit{Eq. 2.3}$$

2.2 The discovery of Silicon Carbide

In 1893, Edward Goodrich Acheson was the first person to create silicon carbide in a laboratory setting. He named the new material carborundum, after carbon and alumina, which he believed were the constituent components. Acheson determined that loading silica and carbon into a high-temperature crucible and heating the mixture to ~2700 ºC would produce small silicon carbide crystals. Within the process chamber, the rough chemical reaction below (Eq. 2.4) would occur with the addition of heat. These resultant crystals could then be processed into various cutting and abrasion products. The process that he developed, referred to as the Acheson Process, is still the primary method of creating silicon carbide [1, 2].

$$SiO + 3C \rightarrow SiC + 2CO \quad \textit{Eq. 2.4}$$

In 1904, Henri Moissan collected meteorite samples from the Diablo Canyon in Arizona. Moissan identified the presence of silicon carbide crystals, which he termed moissanite. These meteorite samples were the first naturally occurring SiC specimens to be observed. Since then, naturally occurring moissanite has also been found in kimberlite and lamprorite samples [11, 12].

In 1907, Henry Round demonstrated a SiC light-emitting diode (LED). The LED was made by applying 10 V across contacts on a SiC crystal [1]. Round observed orange, yellow, and green luminescence, this was the first proof that SiC had potential as a viable electronic material.

2.3 Growth Processes for Silicon Carbide

Silicon carbide platelets were first grown by Lely, via sublimation in 1955 [5]. Lely used a graphite crucible with an internal SiC crucible. The outer graphite crucible was heated to ~2550 ºC, which allowed the SiC to sublimate from the hot exterior cylinder to form crystals on the cooler internal cylinder.

In 1978, Tairov and Tsvetkov [13], announced that they had successfully used seeded sublimation growth to grow bulk crystals (Figure 2-1) and were the first to grow single crystal ingots. For seeded sublimation growth, it is first necessary to identify a seed crystal with the desired crystal polytype (discussed below). Then the seed crystal was placed at the top of a silicon carbide cylinder which was the same diameter as the desired final ingot. Next, the SiC cylinder was loaded into an oversized graphite crucible and surrounded by high-purity polycrystalline SiC. The crucible was heated so that the seed crystal was the cold zone and the temperature gradient increased across the crucible. Tairov and Tsvetkov reported that they could successful grow SiC ingots with process temperatures ranging from 1800ºC to 2600 ºC and of 6H, 4H, and 15R polytype [13]. This growth process is known as the modified-Lely growth method. Currently, the modified-Lely method is almost always used to grow bulk SiC single crystals [1].

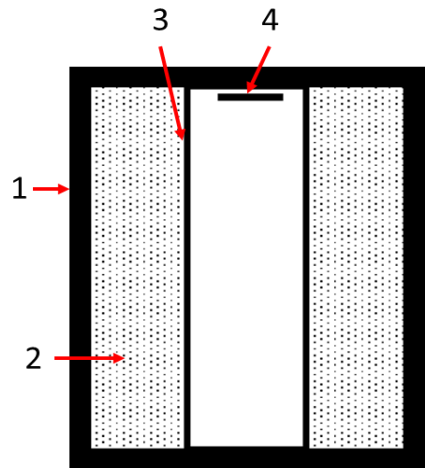

Figure 2-1: Depiction of crucible used to conduct seeded sublimation growth for bulk, single-crystal silicon carbide ingot. 1) Outer graphite crucible 2) Polycrystalline SiC bulk material 3) Inner SiC crucible, also determines the diameter of the final SiC ingot. 4) Seed crystal of desired polytype. Reproduced from [1].

2.3.1 Silicon Carbide Polytypism

Silicon carbide is very interesting in the fact that it has over 200 known polytypes [14]. Polytypism for SiC is defined as "the crystal structure exhibits a number of different one-dimensional ordering sequences without any variation in stoichiometry" [1]. What this means is that SiC consists of stacked bi-layers of silicon and carbon. Each silicon atom forms covalent bonds with 4 carbon atoms and likewise, each carbon atom forms covalent bonds with 4 silicon atoms [14]. In Table 2-1, the numeral represents the number of bi-layers within one unit cell, and the crystal lattice order is represented by the C, H, or R. Where C is cubic, H is hexagonal, and R is rhombohedral. The most common polytypes are 3C, 4H, and 6H. 3C has a cubic crystal orientation and requires three Si-C bi-layers per unit cell, while 4H and 6H are both hexagonal crystal structures. 4H has four Si-C bi-layers and 6H has six bi-layers per unit cell. Each bi-layer is given a designator such as, ***A, B,*** or ***C.*** These designators are used to provide

sequence notation explaining the ordering of the bi-layers. 2H is represented by the repeating sequence of ***AB***. The sequences for 3C is ***ABC***, 4H is ***ABAC***, and 6H is ***ABCACB*** [1].

Table 2-1: Sample of known SiC polytypes [1, 3].

3C	2H	4H	6H	8H	15R	21R	24H
27R	33R	40H	42H	51R	57R	66H	75R
80H	84R	87R	93R	105R	106H	111R	120R
130H	141R	146H	152H	189R	201H	342H	393R

The most common polytypes 3C, 4H, and 6H all have slightly different bandgap values. The bandgap of 3C is 2.39 eV, 4H is 3.023 eV, and 6H is 3.26 eV [2].

2.3.2 Silicon Carbide Single Crystal Defects

During the growth process, bulk silicon carbide ingots may form various intrinsic defects such as micropipes, screw dislocations, inclusions, or hexagonal pits [3]. Micropipes are hexagonal, tube-like cavities that form parallel to the crystal growth direction [1]. They may have diameters ranging from the sub-micron up to 50 μm. The micropipes are formed as impurity particles accumulate upon the crystal surface during bulk growth. As each successive silicon carbide layer is formed, the impurity particles "rise" along with the new layer, leaving a void region behind, forming the micropipe. Micropipes may even propagate the length of a crystal boule [3]. SiC manufacturers are now reporting <1 micropipe defect per cm^2. Screw dislocations [1, 15, 16] are imperfections that have emerged above a crystal plane and may act as a nucleation site. These imperfections will propagate in a direction that is normal to the

origination face. The resultant step will wind around itself, allowing crystal growth "up a spiral staircase" [15] (see Figure 2-2).

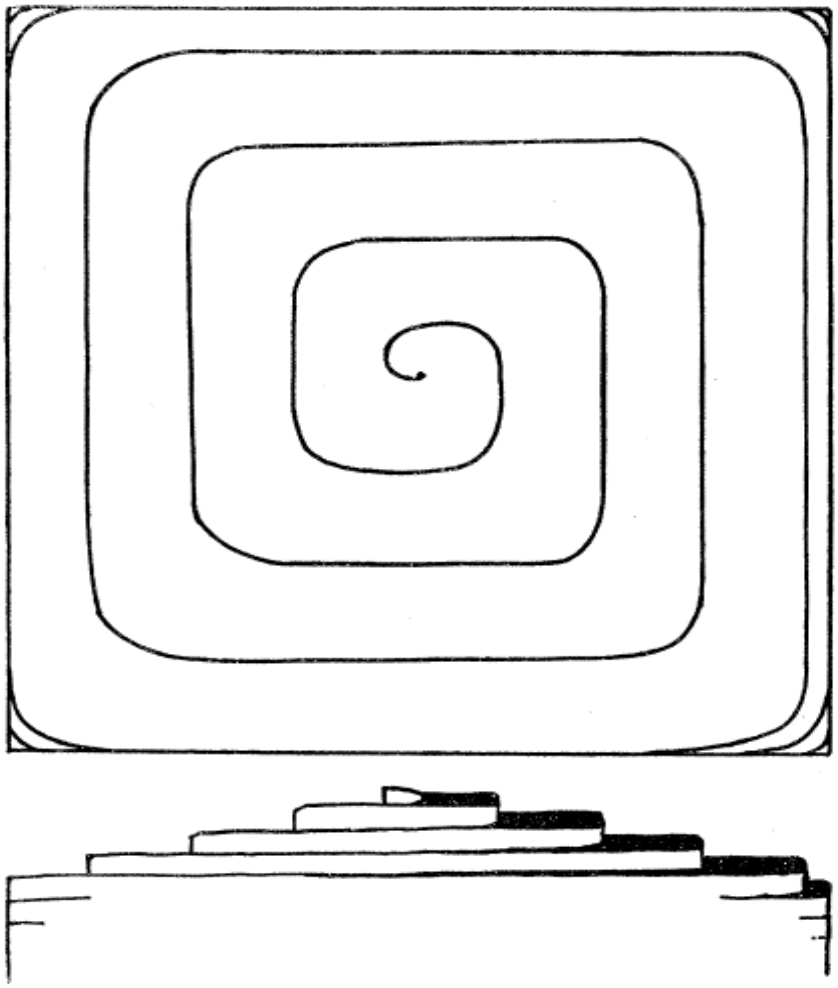

Figure 2-2: Screw dislocation and resultant spiral staircase or pyramidal-like growth that is normal to the crystal surface [16].

Also, Si and C inclusions have been observed using Auger analysis [1]. These inclusions may form when a large aggregate of source material deposits onto the crystal face during the sublimation process. These large pieces may be carbon that was not fully vaporized or from impurities in the source material. Also, an inclusion may be a section of the SiC boule that is of

a different polytype or of the same polytype but misoriented with the main crystal. Grain boundaries are the interface between different polytypes or misoriented crystal sections.

2.3.3 Semi-insulating Silicon Carbide

The term semi-insulating is used to refer to semiconductor materials with higher resistivity characteristics, typically greater than 1500 Ωcm. In literature, the terms semi-insulating and high resistivity are used interchangeably. The SiC wafers used for this work had a resistivity $>10^9$ Ωcm. Semi-insulating silicon carbide (SI SiC) was first realized for 50 mm diameter, 6H crystals by Hobgood, et. al. in 1995 [17-19]. The crystals were grown via physical vapor transport (PVT) with an additional vanadium dopant [20]. The commercial graphite used for the crucible is a known source of boron contamination during crystal growth [17]. Nitrogen is also a widely recognized process impurity. At the extreme high temperatures needed to grow SiC crystals, trapped nitrogen will escape from the actual process equipment and dope the SiC boule [21]. To counteract these impurities, vanadium acts deep level acceptor to balance the impurities that were present within the source material or the process equipment. However, the vanadium itself has the downside that it is a source of charge trapping during signal generation [18, 19, 22]. This property of vanadium is discussed in greater detail later.

High-purity, semi-insulating silicon carbide (HPSI SiC) is now being grown. HPSI SiC does not use vanadium as a deep level acceptor to achieve its semi-insulating behavior [21, 23]. To achieve semi-insulating material without vanadium doping, SiC crystal manufactures rely on a few process changes. The first change is to use a gas such as argon as the chamber gas instead of nitrogen. The change in chamber gas reduces the amount of unintentional nitrogen doping

that occurs. The other change is to rely upon intrinsic point defects at deep electronic states that occur naturally during the growth process [21, 23]. Annealing a crystal after growth can actually reduce the number of point defects within that crystal. However, this has the undesired effect of degrading the semi-insulating properties by reducing the concentration of point defects.

2.4 Silicon Carbide Etching

Extensive work has been reported on the etching processes of silicon carbide. Methods have included chemical/wet etching, photoelectrochemical etching, as well as plasma etching. The following sections will expound further on each methodology.

2.4.1 Wet Etching

To date, the attempts at finding a feasible method of conducting wet or chemical etching of silicon carbide features have proven futile. Wet etching has been successfully utilized for identifying crystal defects such as micropipes, screw dislocations, grain boundaries, or planar defects. The primary method is molten salt, particularly potassium hydroxide (KOH) at elevated temperatures (above 450 ºC) [1, 24].

Some other common chemical etching solutions are listed below [24];

NaOH	KOH	KNO_3	$NaNO_3$	PbF_2	$KClO_3$
K_2SO_4	Na_2O_2	PbO	Na_2SO_4	$Na_2B_4O_7$	

2.4.2 Photoelectrochemical Etching

An alternative method for etching SiC is photoelectrochemical etching (PEC). During this process, a silicon carbide wafer is placed inside of an electrochemical cell filled with an electrolyte solution consisting of dilute HF mixed with H_20 and ethanol. The silicon carbide wafer functions as the anode, while a Pt wire/plate is used as the cathode. The applied voltage is typically kept below 10 V. During the etching process, the working surface of the silicon carbide wafer may be exposed to UV light via a filtered Hg arc lamp [24].

2.4.3 Plasma Etching

Dry etching of SiC has been performed in variety of methods. Quality results have been observed using inductively-coupled plasma (ICP), reactive ion etching (RIE), magnetron ion etching (MIE), and electron cyclotron resonance (ECR). In addition to the various system types employed, numerous gas chemistries have also been studied. Gases including, but not limited to, fluorine-based chemistries with SF_6, C_2F_6, CF_4, CHF_3, NF_3, or chlorine-based chemistries such as BCl_3 and Cl_2. During plasma etching, the RF field within the chamber disassociates the process gas into radicals such as SF_x or free F_x radicals. These radicals interact with the Si or C atoms to form SiF_x or CF_x. Also Ar, H_2, and O_2 have all been utilized as additive gases during etching. These additive gases appear to help minimize the roughness of the final features and minimize the effect of micromasking due to the redeposition of etching products. Due to its extreme chemical resistance, SiC has a slower etching rate than silicon, so it is necessary to

employ alternate etchant mask materials. Some materials used as the etchant mask for plasma etching SiC have been nickel, aluminum, and indium tin oxide [3, 25-31].

2.5 Photolithography

Optical photolithography is the practice of applying a photosensitive (photoresist) material across the surface of the working substrate. Then the photoresist is patterned by shining UV light through a photomask onto the photoresist. Next, the photoresist is developed, during which, the photoresist is removed from select areas of the working substrate. Next, the substrate is ready for either chemical etching or metal deposition. Then, the remaining photoresist can be removed and the wafer cleaned for any following processing.

2.5.1 Photoresist Types

The two basic types of photoresist are positive and negative. When positive photoresist such as an AZ 1500 series photoresist is exposed to sufficient UV light (Figure 2-3), the exposed areas becomes more soluble when submerged within the correct photoresist developer solution. The developer opens windows within the photoresist, exposing the underlying substrate. For positive photoresist, there is a direct transfer of the photomask pattern to the photoresist (Figure 2-4).

For negative photoresist, such as the AZ nLOF 2000 series, exposure to sufficient UV light makes the exposed regions of negative photoresist less soluble when dipped into developer.

The removal of the unexposed photoresist leads to the opening of windows. Therefore, an inverse of the photomask image is formed (Figure 2-4).

In addition, there is also the image reversal process that converts positive photoresist to behave as a negative photoresist. To achieve positive image transfer, it is handled the same as a positive photoresist. However, to achieve an inverse image transfer, it is necessary to add an additional baking step after the exposure with the photomask and then perform an additional flood exposure with no photomask. After the double exposures, the device is ready for developing.

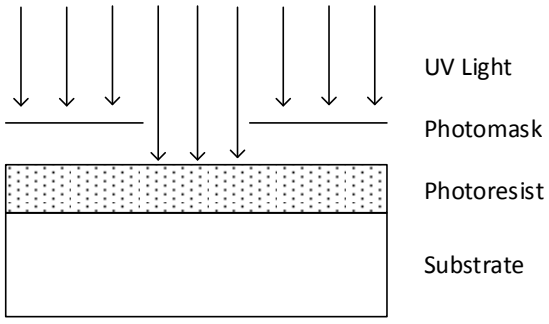

Figure 2-3: Depiction of photoresist under exposure, with photomask providing shadowing of select areas of photoresist.

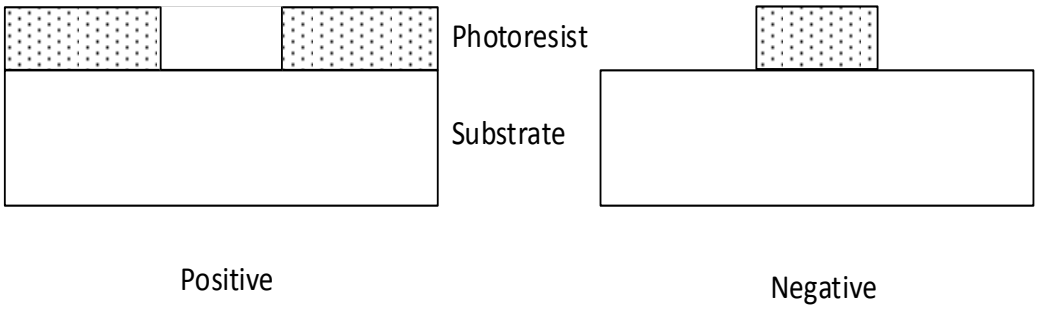

Figure 2-4: Depicting the differences of how positive and negative photoresist provide coverage over different regions when exposed using the same photomask.

2.5.2 Optical Photolithography Exposure

Optical photolithography may be conducted in proximity mode, contact mode, or projection mode. For proximity mode, there is a small air gap (typically 4-10 μm) present between the photomask and the photoresist layer. Proximity mode has the benefit of no direct contact between the photoresist and the photomask, which prevents photoresist residual from sticking to the photomask. Particulates or residue on the photomask may actually allow for contact between the photoresist and the photomask, which may cause the photomask to slightly flex. If the photomask flexes, there may be slight deviations on the transferred pattern if the pattern has very small feature resolution (a few microns). Also, the wafer may actually stick to the photomask, which will likely damage the photoresist layer and the resultant pattern. An image of the photoaligner used for this research is shown below in Figure 2-5.

For contact mode, the substrate holder is raised until the photoresist is physically pressed against the photomask and sealed either by pressure or by vacuum. Contact mode allows for improved resolution of the photomask image transfer. However, contact mode leads to greater particulate and residual transfer between the photomask and the processed wafer. Also, edge bead may have a sufficiently greater relative height than the photoresist layer (certain samples were measured with a DAQ-TEK profilometer to have a photoresist layer height of ~7 μm, while the height of the edge bead was ~21-28 μm) which may prevent proper contact between the photomask and the top of the photoresist layer across the entirety of the wafer, which may cause a distortion of the transferred pattern.

During projection mode, the photomask is stepped several times across the working surface and on each step, a small region or individual device area is exposed. This process is repeated until the entire working area is exposed.

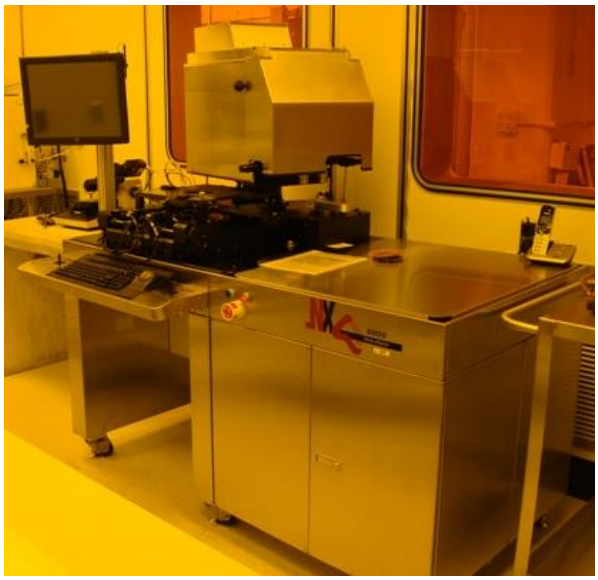

Figure 2-5: Quintel NXQ 8000 photoaligner, used for all photolithography work. It was used in both contact and proximity mode [32].

2.5.3 Patterning via Photolithography

A primary use for photoresist is to apply and pattern it on substrate for a process step. Using proper chemicals, the image can be transferred to the underlying layer(s) with wet chemical etching (Figure 2-6). Also, photoresist is often used during the dry etching of silicon (Figure 2-7). Alternately, photoresist (typically negative photoresist) may be patterned on top of a layer and then additional material is deposited across the entire surface. The deposited material will adhere to the exposed windows of the underlying layer and coat the top of the photoresist. When the work piece is submerged into a photoresist remover such as Kwik-Strip, the material

on the photoresist comes off of the underlying layer while the material deposited within the open windows remains. During plasma etching, the photoresist etches at a significantly slower rate than the exposed silicon areas.

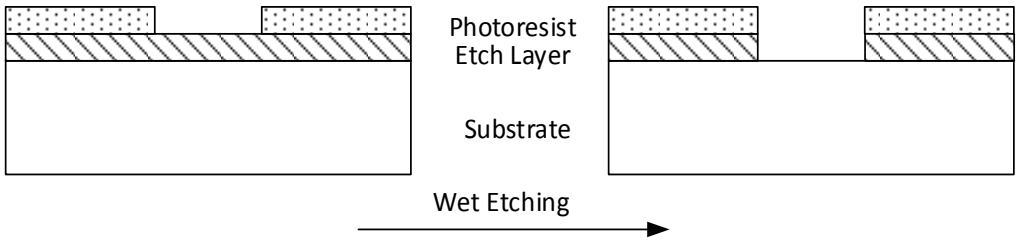

Figure 2-6: Depicts the usage of photoresist to pattern an underlying layer via chemical wet etching.

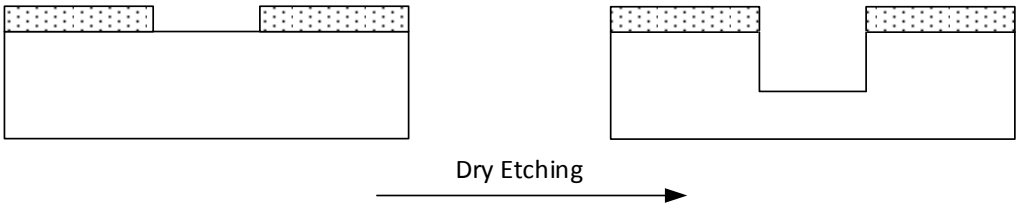

Figure 2-7 Depicts the usage of photolithography and plasma etching to etch features into a wafer. The photoresist acts as a sacrificial protective layer during the etching process.

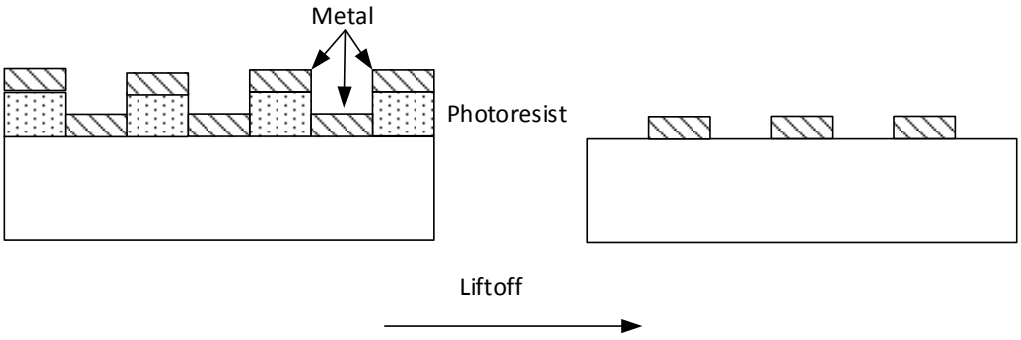

Figure 2-8 Depicts metal-liftoff processing where the photoresist is first spun onto a wafer and then patterned. Next, material may be deposited via methods such as evaporation. Then, the photoresist is removed with solvents and the metal ontop of the photoresist is removed. Leaving behind the metal that deposited directly onto the underlaying layer.

Photolithography was used for this project as means to properly pattern both the metal contact layers and the etchant mask. The two types of photoresist used were AZ 1512 and AZ 2070. The AZ 1512 photoresist is a positive type photoresist and has a typical thickness of 1.2 μm. The thin layer thickness of the AZ 1512 allows for accurate transfer of the photomask pattern to the photoresist, as well as accurate transfer of the pattern during chemical etching. AZ 2070 is a negative photoresist with a typical thickness of 7 μm. The thicker photoresist layer allows easier access for the Kwik-Strip chemicals when conducting a liftoff process. Due to being thicker, there can be significant undercutting of sidewalls (along the order of a few microns), which if using to pattern for wet etching may affect the final dimensions of etched features.

2.6 Neutron Sources

Multiple neutron sources were used for this work, including a ^{252}Cf source and the diffracted beam port at the Kansas State TRIGA Mark II Nuclear Reactor. The K-State TRIGA Reactor has an operating license for up to 1.25 MW [33]. The reactor has various research capabilities, including, neutron activation analysis, tracer isotope production, and 4 beamports. The beamports are as follows; 2 radial, 1 tangential, and 1 fast. As implied by the name, the radial beamports are situated radially with respect to the reactor core. The radial beamports are designed to penetrate all of the reactor shielding except for the graphite reflector. Therefore the emitted beam is comprised of a wide spectrum of thermal to fast neutrons as well as gamma rays. A concrete annulus collimator has been inserted within one radial beamport. The upstream section of the collimator has a sapphire crystal that provides some attenuation of the gamma rays

and higher energy neutrons. After the collimator is the diffractometer, made from pyrolytic graphite crystals. The diffractometer (Figure 2-9) is positioned within the beam so that thermal neutrons (0.0253eV) are diffracted out of the beam [34]. A detector instrumentation station is located near the diffracted beam so that detectors can be inserted into the thermal neutron beam for thermal neutron testing. The detector station includes a standard NIM bin with various electronics and a computer equipped with MAESTRO software.

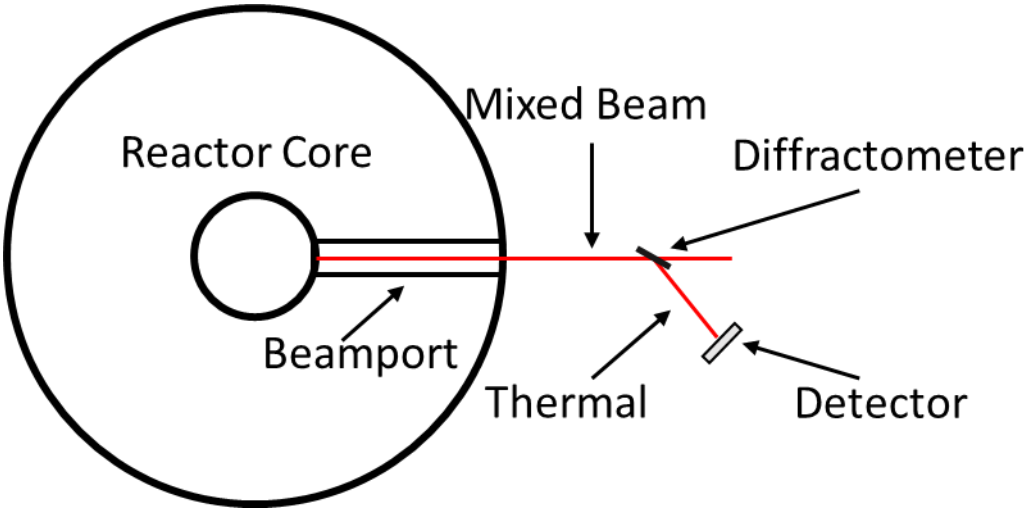

Figure 2-9: Depiction of the K-State TRIGA Reactor and one radial beamport. A mixed beam of neutrons and gamma rays is passed from the reactor core through a collimator inserted into the beamport. Then the mixed beam passes through the diffractometer. The thermal neutrons are diffracted out of the mixed beam. The detector test location is located within the diffracted thermal neutron beam.

An additional neutron source that was extensively used was ^{252}Cf. Californium decays by two modes, the primary mode is alpha decay with a branching ratio of ~97%. The secondary mode is spontaneous fission with a branching ratio of ~3%. [6, 35]. When an atom undergoes spontaneous fission, the nucleus splits into two fission fragments, as well as gamma rays. During the process, usually some number of neutrons are also emitted. Each radioisotope that

undergoes spontaneous fission has a characteristic average number of neutrons per fission event. ^{252}Cf has a spontaneous fission half-life of 85.5 years and emits ~3.7 neutrons per fission event [36]. A gram of ^{252}Cf will emit ~2.3 x 10^{12} neutrons per gram per second [35]. The neutrons that emitted during the fission process are not released with discrete energies like the reaction products from the ^{10}B or ^{6}Li reactions. Instead the neutrons have an energy value from a continuum of possible energies. As shown in Figure 2-10, the energy distribution reaches a maxima below 1 MeV for ^{252}Cf.

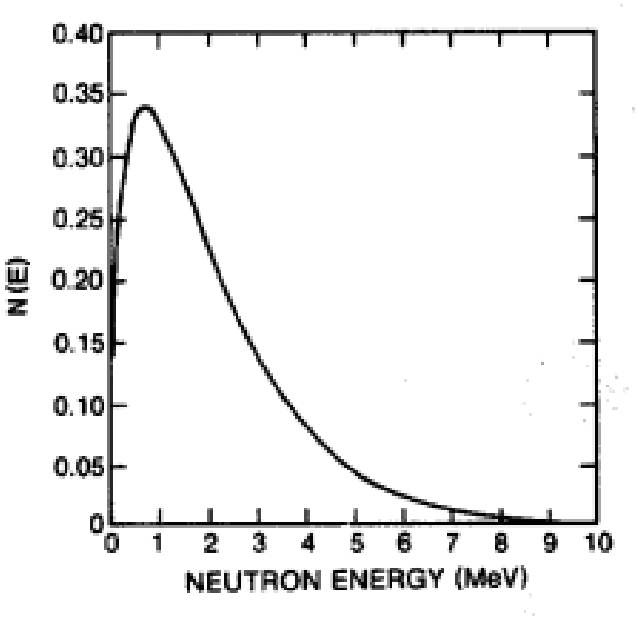

Figure 2-10: Calculated distribution of ^{252}Cf spontaneous fission neutron energies [36].

^{252}Cf was a very useful neutron source because due to the small amount of actual mass needed to conduct measurements. It is feasible to use small, encapsulated, portable sources to conduct benchtop measurements within the S.M.A.R.T. Lab facilities. At times, high-density polyethylene was placed between the ^{252}Cf source and the detector to help soften the emitted neutrons closer to the thermal region.

2.7 Laboratories

The majority of this project was conducted within the Kansas State University S.M.A.R.T. Laboratory Class 100 cleanroom. The cleanroom is a 1,000 ft^2 laboratory which contains various processing systems such as chemical benches, photoaligner, e-beam evaporator, sputtering system, and plasma etcher. It was designed and constructed by CleanAir Technologies. The cleanroom's heating, ventilation, and air conditioning (HVAC) was designed to maintain room temperatures around 65-70 °F while the relative humidity was kept around 35-45%. All of the lights and windows are covered with filters that prevent any UV and high-wavelength visible light (blue) from entering the working areas, preventing any premature exposure during photoresist work. Consequently, this filtering gives cleanroom photos the yellow/orange appearance.

Work was also conducted within the NanoMaterials and Characterization Lab and the Cooling and Heating Innovation Lab, both located within the Mechanical and Nuclear Engineering Department at Kansas State University. Neutron testing was conducted at the Kansas State University TRIGA Mark II Nuclear Reactor facility.

Chapter 3 - Theory

Thin film semiconductor neutron detectors have been examined in detail [10]. These devices are formed by applying a neutron-reactive-material thin film (such as ^{10}B or ^{6}Li) to the surface of a semiconductor detector. When a thermal neutron interacts with the film, charged particles are released. If one of these charged particles enters the detector, it will deposit a portion of its energy, inducing a current upon the detector.

Intrinsic efficiency is defined as the number of neutrons recorded by the detector divided by the number of neutrons that entered the detector [37]. Therefore, a detector's intrinsic efficiency is relative to the interaction probability of a neutron within the thin film and probability that a subsequent charged particle is captured within the detector volume.

3.1 Neutron Interaction Probability

As a neutron travels through any given material, it has some likelihood that it will interact in some fashion with the surrounding medium, such as scattering or absorption. To understand neutron interaction probability, first imagine a mono-directional, mono-energetic beam of neutrons, with initial intensity of $I^o(0)$ (Figure 3-1). The beam is normally incident upon the neutron absorbing thin film. $I^o(x)$ represents the *uncollided* neutrons or the neutrons that have travelled through some thickness *x* without any type of interaction. Next is σ_F, which is the material's microscopic thermal neutron absorption cross-section, N_F is the atomic density, and Σ_F is the material's macroscopic thermal neutron absorption cross-section (Eq. 3.1).

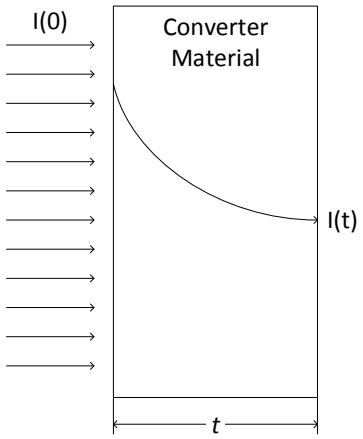

Figure 3-1: Depiction of the attenuation of incident flux through a converter material. I(0) is the incident beam. I(t) is the portion of the incident beam that has not interacted with the converter material at some thickness t.

$$I^o(x) = I^o(0)e^{-\sigma_F N_F x} = I^o e^{-\Sigma_F x} \quad \text{Eq. 3.1}$$

Therefore, the probability that an interaction does occur is shown in Eq. 3.2. Where *t* is the thin film thickness. The macroscopic cross-section for ^{10}B is approximately 500 cm^{-1}.

$$1 - \frac{I^o(t)}{I^o(0)} = 1 - e^{-\Sigma_F t} \quad \text{Eq. 3.2}$$

The percentage of incident neutrons that is absorbed represents the absolute, best possible detection efficiency value for a detector. However, as discussed below, just because a neutron is absorbed, it is not guaranteed that a signal will be produced within the detector. It is also necessary to determine the probability that a reaction particle from the neutron interaction reaches the detector active region.

3.2 Charged Particle Detection

Once a neutron interacts within the neutron absorbing material, in the case of slow neutrons and boron or lithium, the reaction particles are emitted with equal and opposite momentums. As discussed previously, ^{10}B will release a helium atom and a lithium atom. By using a publicly available program called SRIM (The Stopping and Range of Ions in Matter), the range of each charged particle can be found in any material or layers of materials as a function of energy [38]. The ranges of each reaction particle in SiC is shown in Table 3-1.

Table 3-1: Reaction products from boron, with energy, branching ratio, and range of particle within SiC [39, 40]. Ranges were calculated by TRIM, a functionality within SRIM.

Charged Particle	Energy (MeV)	Branching Ratio	Range (um)
^{7}Li	0.840	94%	1.58
	1.015	6%	1.78
^{4}He	1.470	94%	3.36
	1.777	6%	4.1

As to be expected the heavier and lower energy Li atoms have lower penetrating ranges within SiC crystal than the He atoms. It is necessary to account for particle range when determining a detector's feature size.

3.3 Signal Generation

As a charged particle travels through a material it is slowing down and transferring its kinetic energy to the surrounding medium. During this transfer of energy, electron-hole pairs are

generated within the substrate. Electron-hole pairs are formed when a passing charged particle transfers energy to electrons that subsequently jump from the valence band to the conduction band [6, 41]. The amount of energy needed to create one electron-hole pair is 3.6 eV in silicon [6, 41] and 2.96 eV in germanium [41]. However, for 4H SiC, the required energy is about 7.8 eV per electron-hole pair [1]. In other words, if two identical charged particles were to fully deposit their kinetic energy into a silicon substrate and a SiC substrate, the particle traveling through the silicon substrate would be expected to generate approximately 2.5 times as many electron-hole pairs as the particle traveling through SiC.

A basic semiconductor detector design with a single crystal semiconductor substrate that functions as the detector volume is shown in Figure 3-2. There are contacts formed on opposing faces and a voltage bias is applied to one contact. This applied voltage bias creates an electric field across the detector volume that will sweep any free space charge out of the detector volume. Therefore, when a charged particle enters the detector volume and deposits its energy into the detector, electron-hole pairs are formed (Figure 3-3). As these new electron-hole pairs form, they are subjected to the electric field and will begin to drift to their respective contact (Figure 3-4). This motion of the electrons and holes will induce a charge on the contacts. The measuring circuits are capable of reading this induced charge and forming a signal pulse for further analysis [1, 6, 10, 40, 41]. Signals are typically first collected as a pulse by a preamplifier, then the signal is measured as a voltage across a capacitor or as direct current. Next, the amplified signal could be sent to an oscilloscope for viewing and recording or to a computer with MAESTRO for spectrum analysis. A sample of amplified signals is shown in Figure 3-5.

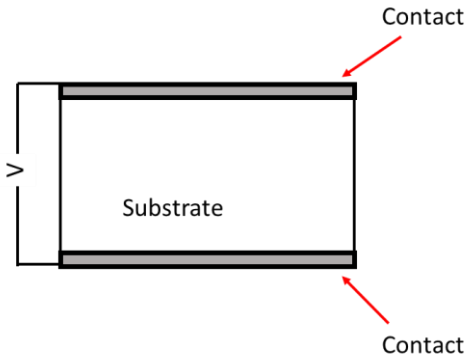

Figure 3-2: Basic semiconductor design sketch. The substrate would be comprised of a single crystal semiconductor material such as Si, Ge, or SiC. The contacts would be formed on opposing sides of the crystal and a voltage bias would be applied via the contacts.

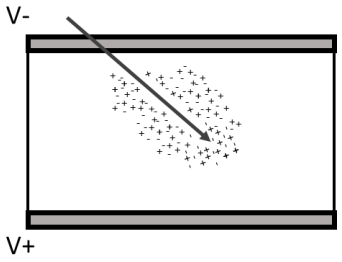

Figure 3-3: As a charged particle travels through the detector volume, it slows down. While slowing down, electron-hole pairs are generated. The applied bias across the volume will start drifting the electrons and holes to the appropriate contacts.

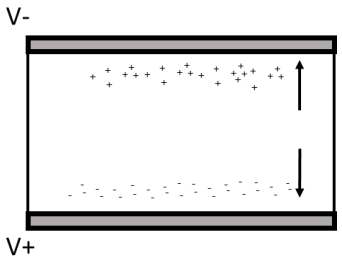

Figure 3-4: Electrons and holes are drifting through the detector volume to their appropriate contacts. This drifting motion induces a charge on the contacts. This induced charge is detected by electronics as current and will be seen as a pulse.

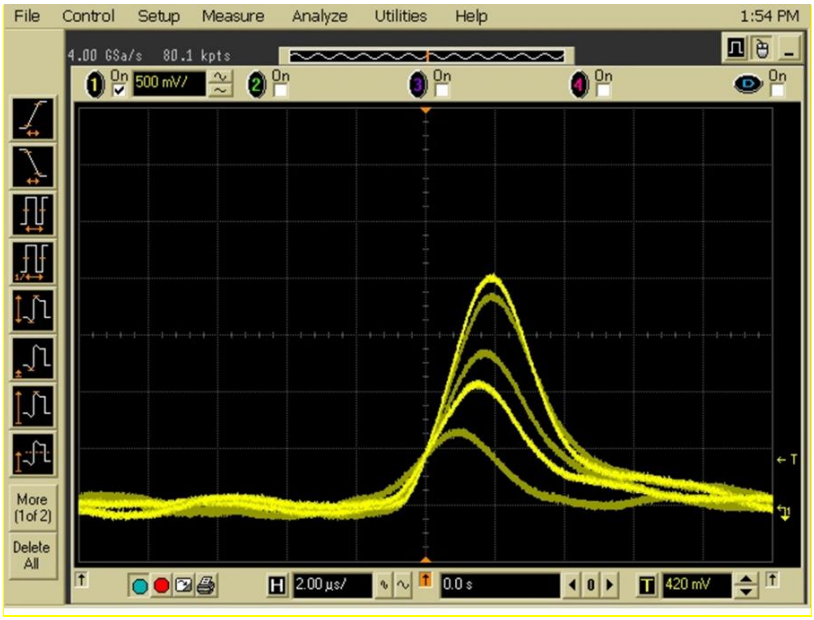

Figure 3-5: Amplified signals recorded with an oscilloscope. The y-axis is pulse height, each gradient is 500 mV. The x-axis is time, at 2.00 µsec per gradient.

3.4 Silicon Carbide Pulse Height

When a charged particle deposits its energy within a substrate and electron-hole pairs are formed, the number of electron-hole pairs depends upon that substrate's activation energy ε_a (for SiC ε_a is 7.8 eV) and the amount of energy that the charged particle deposits in the substrate *E*. The amount of charge is represented by *Q*. This relationship is shown below in Eq. 3.3. Since ε_a for SiC is about 2.5 times larger than the ε_a for Si, it is easier to realize that *Q* for any event would be correspondingly smaller than if the substrate was Si.

$$Q = \frac{E}{\varepsilon_a} \qquad \text{Eq. 3.3}$$

For a pulse to be counted, the value for *Q* must be greater than the equivalent lower level discrimination (LLD) value of the electronics. It is also important that the detector system's noise is lower than the generated signals. This property is known as the signal-to-noise ratio.

3.4.1 Charge Trapping

Some of the impurities that may be present within the crystal structure create energy levels near the middle of the bandgap. These are known as deep-level impurities. As discussed above, one method of making silicon carbide to possess semi-insulating characteristics was intentional vanadium doping. The vanadium forms deep-level energy sites in SiC, near the middle of the bandgap [21, 23], where it would act as a deep donor or deep acceptor to compensate for unintentional dopants such as nitrogen. One drawback of intentionally adding these deep impurities, is that while electrons and holes are drifting through the crystal, they may become "trapped" within one of these sites [6, 21, 23, 42]. Since the pulse height is dependent on the motion of the electrons and holes drifting through the electric field, as electrons or holes are trapped, the pulse height will be lowered accordingly. Also, if a sufficient number of traps are filled, then the detector may become partly polarized due to the trapped space charge. This polarization will affect the electric field across the detector, which will also lower the resultant pulse heights. After some time, the traps will slowly release their trapped charges.

The patents discussing the growth of vanadium-free semi-insulating SiC state that the semi-insulating behavior is due to the presence of point-defect related, deep-energy level sites located near the middle of the bandgap [21, 23]. The process parameters during these SiC crystal growths are tailored specifically to increase the number of deep-level traps to achieve the desired

semi-insulating characteristics. These deep-level sites likely have the same trapping behavior for drifting electrons and holes, as well as the subsequent reducing of pulse height.

3.5 Thin-Film Detector Efficiency

So, in practice, the intrinsic efficiency of a thin film device is equal to the number of events that are recorded divided by the number of particles that passed through the detector. A few methods may be used to determine the number incident particles. One is using a source's known activity and a detector's known geometry to calculate the number of emitted particles that pass through the detector. An example would be a 2π detector, where the source is physically inside of the detector. Another method is to simulate or model the number of emitted particles that will pass through the detector volume. This method may be done as a way to calculate the resultant spectrum when a moderator material is used to soften a source's energy spectrum.

The method primarily used for this research is to use a reference detector that has well-characterized performance. For this work, a Reuter-Stokes, 2-inch diameter, ^{3}He detector was used. The ^{3}He detector was previously determined to have an intrinsic thermal neutron efficiency of 80.7% ±0.50% [43]. To use a reference detector, first conduct a measurement using the reference detector. Then determine the actual number of incident particles by taking the number of events recorded and dividing by the reference detector's known intrinsic efficiency. Next, swap in the detector to be tested and conduct the desired measurements. Then the intrinsic efficiency would be calculated by taking the number of events recorded and divide by the actual number of particles determined using the reference detector.

Alternatively, one could take the number of events recorded by the tested detector and divide by the number of events recorded by the reference detector to determine the tested detector's relative efficiency. In other words, the detector would be stated as having some efficiency relative to the known efficiency of ^{3}He detector.

3.6 Thin-Film Detector Design Limitations

Thin-film neutron detectors may have slightly different intrinsic efficiencies due to the manner in which the detector is irradiated, i.e. frontside or backside irradiation [10]. To achieve optimal performance for a thin-film detector, it is necessary to find the balance between the desires for high thermal-neutron absorption and high charged-particle collection. This balance is due to the nature of the charged particles having limited ranges within the neutron absorbing thin-films. When the interaction occurs near the boundary between the converter material and the detector, there is a very large solid angle in which it is possible for one reaction product to reach the detector (Top case in Figure 3-6). As the interaction location moves further away from the boundary line, the solid angle is correspondingly reduced (Middle case, Figure 3-6). If the converter material is thick and *t* is greater than the range of the most penetrating reaction product, there is no possibility for an event to be recorded (Bottom case). Hence, for frontside irradiation, while simply adding more converter material will raise the intrinsic neutron absorption of the device. After a certain point, it will begin to lower the intrinsic charge particle capture of the detector. A rule of thumb is that the thickness of the converter material should not exceed the range of the most penetrating reaction product [10].

However, for backside irradiation, since the incident flux is always the highest at the boundary between the converter material and the detector volume, the addition of more converter material will provide small increases intrinsic detector efficiency with diminishing returns. Maximum achievable intrinsic thermal neutron efficiencies is about 4-4.5% for ^{10}B or ^{6}LiF thin films [10].

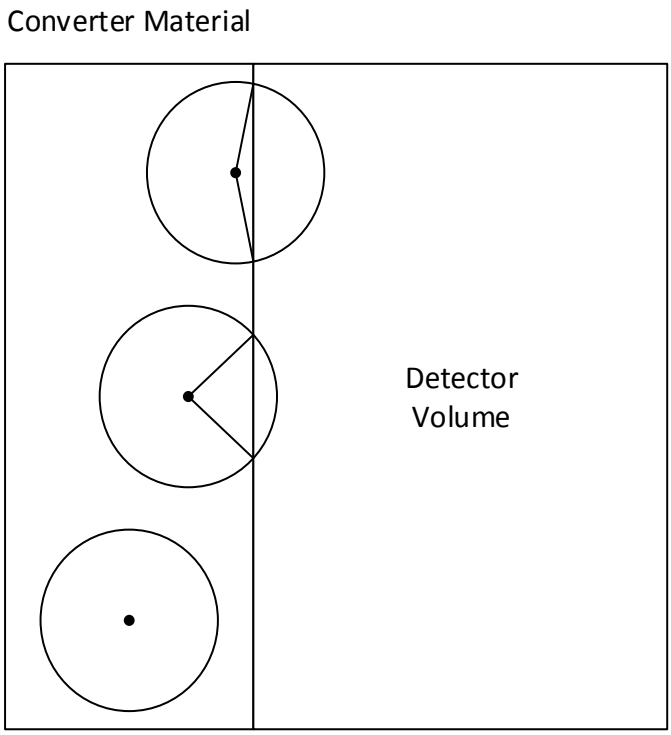

Figure 3-6: Image of a thin film device with different possible interaction locations. Top location has a high probability of generating a signal. Middle location has a reduced probability. Bottom location has no chance due to insufficient range of any reaction particle to reach detector volume.

3.7 Microstructured Detectors

As detailed in other works, the intrinsic efficiency of a detector may be improved with the formation of 3-dimensional microstructures [39, 44-48]. A few common types of structures that have been demonstrated are holes, trenches, and pillars. Microstructures are typically formed via wet or drying etching mechanics. These devices are known as microstructured neutron detectors (MSNDs). Next, the structures are backfilled with converter material (Figure 3-7). The structures allow for an overall increase in the amount of converter material present without a similar increase in self-attenuation concerns as discussed above. Therefore, increasing the probability that a neutron interacts with the converter material.

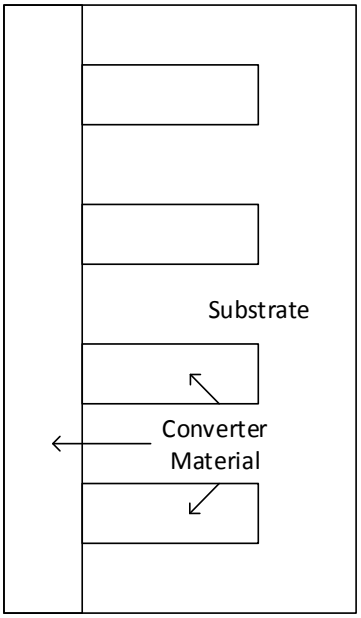

Figure 3-7: 2-D sketch of a microstructured device, with additional converter material located within the features.

Also, the probability that a reaction product enters the detector volume is also changed. The fact that the structures are within the substrate means that there is active detector volumes on both sides of the features (Figure 3-8), which allows for the possibility that both reaction products may enter the detector volume and deposit energy. The contributions from both products make it possible to generate signals that have a higher amplitude than signals from one reaction product. This combined signal may make the resultant spectra more complicated. In a thin-film detector an interaction may occur, that due to the emission angles one reaction product may not deposit sufficient energy to generate a signal greater than the LLD setting. However, with microstructures, both particles may enter the detector and deposit enough energy to generate a signal over the LLD and record a count.

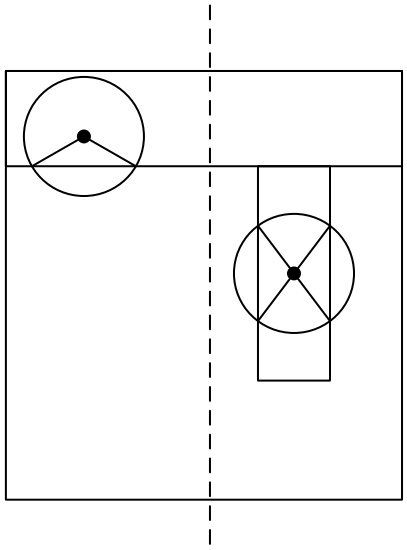

Figure 3-8: Sketch depicts the increased solid angles in which reaction products may enter the detector. Also, shows that it is possible to collect energy from both reaction products instead of just a single reaction product.

Extensive efforts were put forth into modeling MSND device efficiencies with MCNP [39, 44, 48, 49]. These efforts focused primarily on using ^{10}B, ^{6}Li, or ^{6}LiF as the neutron

conversion material. The works also explored several microstructure shapes such as, holes, pillars, straight trenches, sinusoidal trenches, or chevron trenches. For each conversion material and shape, various unit cell widths as well as trench/fin ratios were evaluated. Finally, the efficiencies for increasing trench depths were reported.

For SiC, efficiencies were modeled using ^{10}B as the conversion material with straight trenches as the microstructure shape. The cell width was stepped from 4 μm to 12 μm while the ratio of trench width to fin width was stepped from 0.1 to 0.90 for each cell width. The trench depths modeled were 10 μm, 20 μm, 40 μm, and 60 μm. The results are tabulated in Table 3-2. It is apparent that there are diminishing returns with respect to increasing overall cell width. This diminishing return is due to the overall short ranges of the charged particles from the boron reaction. As the cell width increases, there is a point where the charged particles no longer deposit enough energy within the substrate to overcome the LLD. As to be expected, increasing trench depth will result in an increase of detection efficiency. Also, there must be enough substrate material remaining in a SiC fin to allow for sufficient slowing down of the charged particle and the transfer of energy to the substrate.

Table 3-2: Simulated SiC microstructured device efficiencies for various cell width, trench and fin widths, as well as trench depths. The simulations were conducted using MCNP.

Silicon Carbide MSND Efficiency, Straight Trenches, B-10					
T/W_Cell	*Cell width W_Cell (um)*				
	4	**6**	**8**	**10**	**12**
			Trench depth H = 10 um		
0.10	3.93%	3.84%	3.73%	3.63%	3.52%
0.20	7.44%	7.04%	6.59%	6.21%	5.83%
0.30	10.51%	9.57%	8.68%	7.80%	6.98%
0.40	13.19%	11.56%	10.05%	8.52%	7.17%
0.50	15.44%	13.00%	10.66%	8.73%	7.51%
0.60	17.35%	13.91%	10.78%	9.04%	7.81%
0.70	18.86%	14.23%	11.10%	9.34%	8.11%
0.80	20.04%	14.37%	11.42%	9.67%	8.46%
0.90	10.76%	11.26%	11.60%	9.96%	8.77%
			Trench depth H = 20 um		
0.10	6.21%	6.07%	5.91%	5.74%	5.56%
0.20	11.75%	11.11%	10.42%	9.75%	9.12%
0.30	16.61%	15.07%	13.61%	12.10%	10.71%
0.40	20.78%	18.06%	15.54%	12.92%	10.69%
0.50	24.26%	20.16%	16.18%	12.93%	10.90%
0.60	27.12%	21.29%	16.03%	13.07%	11.05%
0.70	29.32%	21.48%	16.21%	13.22%	11.19%
0.80	30.94%	21.38%	16.39%	13.42%	11.42%
0.90	14.89%	15.86%	16.34%	13.56%	11.59%
			Trench depth H = 40 um		
0.10	8.36%	8.14%	7.89%	7.66%	7.46%
0.20	15.77%	14.86%	13.89%	13.01%	12.14%
0.30	22.23%	20.13%	18.09%	16.06%	14.12%
0.40	27.79%	24.08%	20.57%	16.99%	13.91%
0.50	32.39%	26.74%	21.25%	16.79%	13.99%
0.60	36.11%	28.08%	20.88%	16.81%	14.02%
0.70	38.94%	28.12%	20.91%	16.82%	14.05%
0.80	40.96%	27.81%	20.97%	16.89%	14.17%
0.90	18.72%	20.11%	20.72%	16.92%	14.21%
			Trench depth H = 60 um		
0.10	9.08%	8.83%	8.57%	8.33%	8.11%
0.20	17.12%	16.12%	15.07%	14.12%	13.19%
0.30	24.13%	21.84%	19.62%	17.42%	15.29%
0.40	30.16%	26.11%	22.27%	18.36%	15.02%
0.50	35.14%	28.97%	22.96%	18.08%	15.06%
0.60	39.16%	30.38%	22.52%	18.06%	15.03%
0.70	42.20%	30.37%	22.52%	18.03%	15.03%
0.80	44.35%	29.99%	22.52%	18.08%	15.11%
0.90	20.00%	21.53%	22.20%	18.06%	15.10%

3.8 Silicon Carbide Plasma Etching

Plasma etching SiC has been primarily accomplished using a variety of fluorine-based gas chemistries. These fluorine gases include SF_6, NF_3, CF_4, CHF_3 and $CBrF_3$. Less work has been reported using chlorine-based gas chemistry, primarily just Cl2 gas has been utilized. Various methods of plasma etching have also been used, including; reactive ion etching (RIE), inductively-coupled plasma (ICP), electron cyclotron resonance (ECR), or magnetron ion etching (MIE) [3, 31, 50]. The work presented here employed SF_6 as the SiC etching gas, within a RIE-ICP plasma etching system (Figure 4-7).

As discussed above, SiC is extremely resistant to chemical etching, therefore, most efforts at creating features within SiC substrates employ plasma etching. When the plasma is formed within the process chamber, various gas radicals are formed from the process gas (SF_6). The gas radicals are F_x and SF_x. These F_x radicals are then accelerated into the exposed SiC. This ion bombardment weakens the Si-C bonds, and improve the overall etching reaction. The F*x* radicals will bond with Si, forming SiF*x* (Eq. 3.4). In addition, the F*x* radicals may also bond with the C atoms, forming CF*x* (Eq. 3.5). These process products are then moved out of the working areas by interaction with other gas ions or removed from the process chamber by the process vacuum. Also, additional process gases such as oxygen have been shown to improve etching characteristics. The additional oxygen has been shown to bond with C, forming carbon monoxide or carbon dioxide (Eq. 3.6). The overall etching process and etching products using SF_6/O_2 is shown by Eq. 3.7 [3, 31, 50].

$$Si + xF \rightarrow SiF_x \qquad (x = 1 \text{ to } 4) \qquad \text{Eq. 3.4}$$

$$C + xF \rightarrow CF_x \qquad \text{Eq. 3.5}$$

$$C + yO \rightarrow CO_y \qquad (y = 1 \text{ to } 2) \qquad \text{Eq. 3.6}$$

$$SiC + xF + yO \rightarrow SiF_x + CO_y + CF_x \qquad \text{Eq. 3.7}$$

Plasma etching is a complex process with many parameters that may have multiple areas of effects on the final etching characteristics. For the plasma etching system used for this work, the following are possible process parameters; process gas(s), gas flowrate(s), chamber pressure, RF power, ICP power, step duration, and number of cycles. DC bias, RF reflected power, and ICP reflected power were under the indirect control of the user. As already mentioned, a multitude of process gases may be used. The operating system allows for user determined flowrates of each individual gas and mass flow controllers regulate the inlet flowrates of each gas. The chamber pressure had a set range between 5 – 100 mTorr. The operating system did not allow for any chamber pressure outside of this range. The chamber pressure is a function of the main turbo pump process speed (which was constant at 28000 rpm), inlet gas flowrate, and was regulated by the system throttling a slit valve located between the main process chamber and the turbo pump suction side. The step duration instructed the operating program how long to maintain that particular set of parameters. A step could be as short as a few seconds or could be hours in duration. Steps allowed for tailoring etching parameters to specific trench depth regions.

The number of cycles is important when performing BOSCHE type plasma etching. During BOSCHE etching, the system is continually switching between and etching step and a polymer (C_4F_8) deposition step. The polymer deposition step is to passivate the trench sidewalls to minimize trench width variation due to overetching. The number of cycles instructed the

system how many times to it must repeat a specific set of process parameters. As trench depth increased, this feature and the step feature combined to give the operator the ability to tailor the process parameters for specific depths. This ability is important in for reducing sidewall effects such as rippling or bottling when etching materials such as silicon [47].

The RF generator had an operating power range from 50 – 500 Watts. The ICP generator had an operating power range from 100 – 3000 Watts. The DC bias was displayed via the control program and was a related to the RF power and the overall cleanliness of the process chamber. It was noted during some experimental runs that the final DC bias value would be dramatically less than the initial values. Physically cleaning the process buildup from the chamber surfaces would restore the DC bias to expected ranges. The reflected power for both the RF and ICP generators were indications of how much power was applied within the process chamber and how much was reflected back into the generators. A reflected power of zero is desirable. The reflected power was typically automatically controlled by automatch units (large capacitance matching systems), but could also be manually adjusted by the operator. At times it was necessary to manually adjust the automatch units to either reduce the reflected power or to help the system initiate the plasma.

To strike a plasma, it is necessary to have the following; proper chamber pressure, proper gas(s), and a power source, RF or ICP, or both RF and ICP. All of these parameters are interconnected and have a "general rule" of necessary values and must be properly balanced. If the chamber pressure is too high or too low, the system may fail to strike its initial plasma for the selected power. Or if the gas flow is too low or too high, the system may be unable to maintain desired chamber pressure. Also if the selected power range is too high or low, the generators and automatch units may have difficulty striking a plasma and reducing the initial reflected power to

acceptable levels. Therefore, it was a common practice to utilize a short, common "strike" step that used moderate values to facilitate striking the initial plasma and then stepping into the desired process parameters.

When a plasma is present within the chamber, increasing the amount of gas within the process chamber via flowrate and/or raising chamber pressure increases the amount of gas radicals created. More gas equals more gas radicals; less gas equals less gas radicals. The RF and ICP both contribute to the strength of the plasma and the amount of gas radicals formed. RF and ICP also contribute the energy to the gas radicals for bombardment upon the SiC working surfaces. As RF and ICP powers are increased, the overall etching rate is expected to increase as well. Inversely, as the chamber pressure increases, there is an increasing likelihood that a radical will collide with other gas molecules and lose energy before it interacts with the SiC, thusly having a negative impact on etching rate. Also, having a lower chamber pressure allows for quicker evacuation of reaction products from the etching sites, which has a positive impact on etching rate and should help reduce the amount of redeposition.

Chapter 4 - Development

The following chapter details the steps taken during the work of making silicon carbide neutron detectors, including device size, etchant mask material, plasma etching, photolithography, material deposition, contact formation, and material backfill. Device testing and analysis will be discussed within Chapter 5.

Typical Device Fabrication Process

Below is a general process outline for the fabrication of a SiC neutron detector. The description starts with a bare silicon carbide wafer and will go through final device mounting prior to sensitivity testing. Process parameters were varied for specific stages and will be detailed later in the document.

1) Pattern a bare silicon carbide wafer with photoresist in preparation for etchant mask deposition
2) Load patterned SiC wafer into e-beam evaporator and deposit etchant mask
3) Soak the SiC overnight in KWIK-STRIP to dissolve the remaining photoresist and finish the liftoff process
4) Dice the wafer into individual die
5) Mount the die onto a carrier wafer (either silicon or silicon dioxide) for plasma etching. The die were mounted using a spot of high-vacuum grease.
6) Plasma etch
7) After plasma etching, the die was removed and then the backside was scrubbed using acetone and isoproponal and sterile microswaps.

8) Remaining etchant mask chemically stripped.
9) Chemically clean the die by soaking it in acetone, then isopropanol, rinse with deionized water, Piranha Etch, rinse, Baker Clean, and a final rinse.
10) Immediately load onto shadowmask and into the e-beam evaporator
11) Deposit contact onto front side
12) Remove the die, flip, and reload into e-beam evaporator
13) Deposit backside contact
14) Backfill trenches with boron powder
15) Spray with Humiseal to seal boron powder
16) Clean backside contact with acetone and isopropanol. Conductive silver epoxy is used to mount the die onto a testing substrate
17) Clean contacts with isopropanol and wire bond topside contact to the electrode on the testing substrate
18) Cover the wire bonds with non-conductive epoxy
19) Proceed to testing

4.1 Multi-Form Factor Design

The first design iteration consisted of several different feature sizes and pitches all on one wafer (Figure 4-1). The features ranged from 20 μm wide trenches down to 2 μm wide trenches. And overall device areas varied from 25 mm^2 to 100 mm^2. Also included on the design was a planar device. After multiple trial runs with silicon wafers, one test grade SiC wafer was patterned with a nickel etchant mask and then plasma etched (Figure 4-2). Due to the difficulties

in resolving the several different feature sizes and concerns of varying plasma etching behavior in the smallest features compared to the largest features, the decision was made to move to a different design methodology.

Figure 4-1: The initial mask design with several different pitches and feature sizes. Design efforts moved away from this mask to the 10 mm x10 mm design.

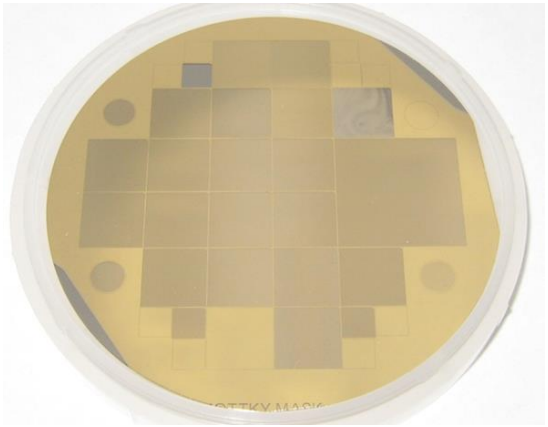

Figure 4-2: A SiC wafer patterned with the initial mask design. The wafer is arranged with devices of several different sizes.

4.2 10 mm x 10 mm Design

After the multi-form factor design, the decision was made to switch to a uniform pattern that allowed for the option of dicing the wafer into smaller samples for plasma etching and thus increasing the total number of trials possible per wafer. Therefore, the new SiC devices were designed with active areas that were 10 mm x 10 mm square (size was chosen because it was the same size as the final deliverable device). The trenches had a pitch of 40 μm with an aspect ratio of 0.5 (trench width was 20 μm). It was decided to progress with larger features that would yield more favorable plasma etching conditions. The bonding pad was located in the upper right corner (Figure 4-6). The decision to make the bond pad rectangular and located at a corner turned out to have an unforeseen benefit during processing. Because once an individual device was plasma etched and the remaining etchant mask was chemically removed, it proved to be very difficult to visually determine which side was etched. This difficulty was due to the fact that the SiC material is transparent and because the etched trenches were only a few microns in depth, each side was very similar in appearances. It was possible to determine the etched side by physically touching the surface or dragging a stylus transverse to the trenches. However, this method was avoided if possible after chemically cleaning the devices, to prevent contamination or damage to the SiC fins.

Initially, attempts were made to pattern the etching mask using nickel. Nickel is widely reported as an etching mask in literature [26-28, 51]. However, the evaporation of nickel was experienced to be very slow and accompanied by excessive “sparking” (emission of visible “sparks” or streaks when a large chunk would emit out of the source material). These problems were later eliminated by a complete replacement of crucible and source material, suggesting the

behavior was symptomatic of source contamination. Furthermore, severe adhesion problems were encountered with the nickel mask peeling off of the SiC wafer immediately after the completion of the evaporation.

It was then decided to switch to Indium Tin Oxide (ITO) as the etchant mask material. The ITO etchant mask was deposited via e-beam evaporation (Figure 4-3). The SiC wafer was first patterned with negative photoresist AZ 2070 with the etchant photomask. The ITO source material was in powder form and would actually not melt during the evaporation, but would undergo sublimation. The source powder was white, however, the final deposited layer would be gray-black in color. The overall deposition rate was relatively slow ~1-3 Å/s, while the chamber pressure would be high, approximately $3x10^{-5}$ Torr. The ITO would tend to spark a lot during an evaporation run, leading to inconsistent deposited layers. It was necessary to take care during the evaporation process to maintain an acceptable balance between deposition rate and excessive sparking. Also, if the chamber pressure increased too much (>5.5 $x10^{-5}$ Torr), the evaporator would trip off the current flow to the crucible. After the evaporation, the wafer was placed into Kwik-Strip overnight for the liftoff step. After the liftoff was complete and the resultant etchant layers would be examined by scanning electron microscope (SEM) imaging, large spots were noticed where no ITO had been deposited. Some spots would stretch across the entire width of the SiC fins. These spots allowed for etching to occur within the fin regions. This problem would be propagated into the contact formation step, since the over-etched areas of the SiC fins would not allow for contiguous contact formation down the length of the fin.

In an attempt to improve the quality of the etchant mask, it was also attempted to first deposit the ITO layer. Then apply and pattern AZ 1512 photoresist on top of the ITO to prepare for selectively wet etching the etchant windows. Literature states that ITO may be etched using

an HF solution that is 1 HF: 1 H_2O_2: 10 H_2O [52]. However, test silicon wafers with a sputtered layer of ITO proved resistant to the etching solution. Even after the complete removal of the AZ 1512 photoresist, the ITO remained resistant to chemical etching. So it was decided to continue using the liftoff process.

Figure 4-3: E-beam evaporator used for depositing contact and etchant mask layers onto silicon carbide wafers [32]. The system was capable of depositing several different materials sequentially such as titanium, gold, ITO, nickel, aluminum, copper, platinum, or chromium.

After the wafer was successfully patterned with the ITO etchant mask, it was diced into individual die in preparation for etching trials. During the mask design, accommodations to device spacing were made in order to leave sufficient room between devices to pass the dicing blade. The dicing was conducted using the laboratory's Disco DAD dicing

saw (Figure 4-4). The dicing saw is equipped with a diamond saw blade and would spray cutting fluid at the worksite for cooling and to flush away cutting debris. The dicing saw was programmed with the desired cutting speed, number of intended cuts, cut depth, and the step distance between each cut line. Once the first set of cuts in one direction were complete, the wafer would be rotated 90 degrees and realigned and a second set of cuts were conducted. Due to SiC being substantially harder than Si, the cutting speed used was about 1/10 of the speed for Si. Even with this precaution, the cutting blades would need to be replaced after each SiC wafer. A wafer is mounted onto the blue backing tape (Figure 4-5), while the backing tape is mounted onto a metal support frame (only partially visible). The metal frame locks onto the dicing saw work pedestal. The blue tape keeps the chips from flying free during dicing. After dicing, the wafer is rinsed with deionized water and allowed to dry overnight. After drying, the die can be individually peeled from the backing tape for further processing.

Figure 4-4: KSU S.M.A.R.T. LAB Disco DAD dicing saw. This saw was utilized for dicing the SiC wafers and was equipped with a diamond saw blade [32].

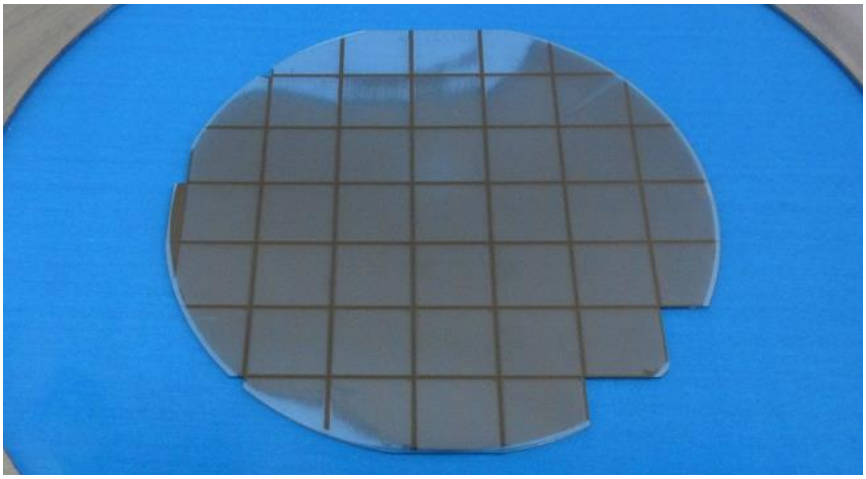

Figure 4-5: SiC with patterned ITO etchant mask. Wafer only contains 23 complete, usable devices. The partial devices were used for early etching trials and destructive cross-sectional analysis with a SEM.

An individual die after removal from the SiC wafer after dicing, is shown in Figure 4-6. This die is ready for further processing such as plasma etching. The bond pad is the rectangle located at the top right corner. It is apparent that the substrate is transparent even after the addition of the etchant mask.

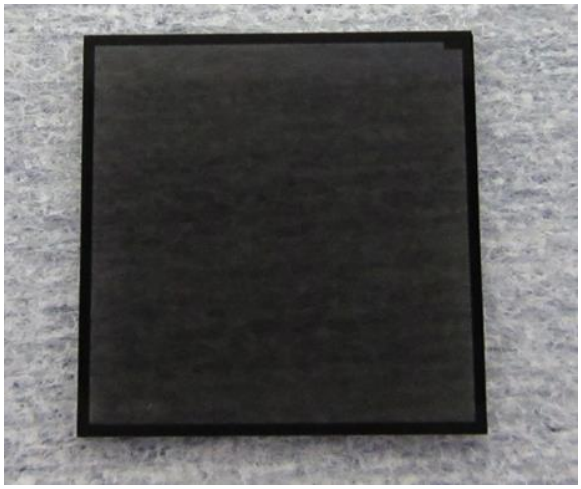

Figure 4-6: Individual (10 mm x 10 mm) die from SiC wafer in Figure 4-5. The silicon carbide substrate is transparent, hence the visible striations of the underlying cloth. The ITO etchant mask is oriented vertically. Top right corner is the bond pad. The location and rectangular shape of the bond pad allowed for easy identification of device orientation.

Plasma etching trials were conducted using the KSU S.M.A.R.T. Lab Oxford PlasmaLab 100 ICP-RIE (Figure 4-7). The Oxford was equipped with SF_6, C_4F_8, O_2, H_2, and N_2 as process gases. The system also had BCl_3 and Cl_2 capabilities, but those were not utilized for this project. The RF generator had a max power of 500 Watts and the ICP generator had a max power of 3,000 Watts.

Figure 4-7: Oxford PlasmaLab 100 ICP-RIE used for etching microstructures within the SiC devices [32].

Prior to plasma etching, a die would be peeled from the blue dicing tape, then soaked for 20 minutes in acetone, then isopropanol, and then rinsed with deionized water. Next, the die would be mounted onto a 3-inch, SiO_2 carrier wafer with a small amount of high-vacuum grease. The carrier wafer was used because the Oxford was configured for etching 3-inch wafers. After loading the carrier wafer into the loadlock, the system turbo pumps would start pumping down the system chambers. Once both turbo pumps were at speed, the system would automatically load the wafer into the main process chamber. Then the system would continue to pump down the process chamber to process pressure. Once process pressure ($<5.8 \times 10^{-6}$ Torr) was reached, the Oxford would autostart the preselected etching recipe. After the recipe was complete, the system would return the carrier wafer to the loadlock. The loadlock turbo could then be shutdown, allowing the loadlock to be vented. When the loadlock was finished venting to atmosphere, the wafer could be removed.

The program detailed process parameters including;

- Process Gas
    - 1 or more gases simultaneously.
- Process Gas Flowrate
    - Flowrate for process gas, measured in standard cubic centimeters per minute (sccm). Must be within a proper range to support desired chamber pressure.
- Chamber Pressure
    - Chamber operating pressure, between ~5 mTorr – 100 mTorr. If the chamber pressure is too low, there are issues in striking and sustaining a plasma. Too high, and it may decrease etch rate.
- RF Power
    - Affects plasma strength and etch rate.
- ICP Power
    - Affects plasma strength and etch rate.
- Step Duration
    - How long the process step lasts, may be as short as a few seconds or as long as a few hours.
- Number of Cycles
    - When running alternating processes (BOSCHE), the program will repeat alternating process parameters such as an etch step and a deposition step.

Various etching recipes and chemistries were used. Typical RF power was between 250 W to 400 W. The ICP power was between 1000 W to 2000 W. Only SF_6 was used as an etching gas. However, both oxygen and hydrogen were both used in some process runs. Some early results are shown in the following figures. It is important to restate that the nominal trench width was 20 μm. It can be easily seen that the ITO etchant mask recedes during the etching process (Figure 4-8). There is also an obvious microtrench where the sidewall meets the trench bottom. However, the trench bottom is relatively smooth.

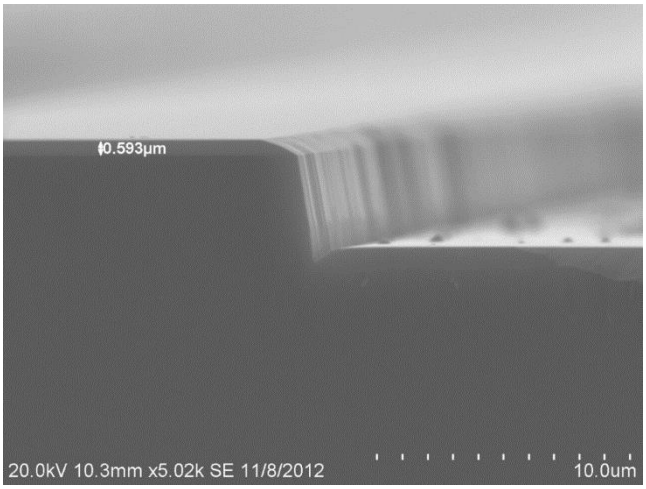

Figure 4-8: SEM image shows the erosion occurring at the edge of the etchant mask during plasma etching. Also evident is a microtrenching feature located between the sidewall and the bottom of the trench. It is possible to see that there is decent etching selectivity between the ITO and the SiC.

Changing the etching parameters could have unexpected etch results. The white spots within the trenches (Figure 4-9) are microstructures that formed during the etching process. A higher magnification view (Figure 4-10) shows the density of the pillars

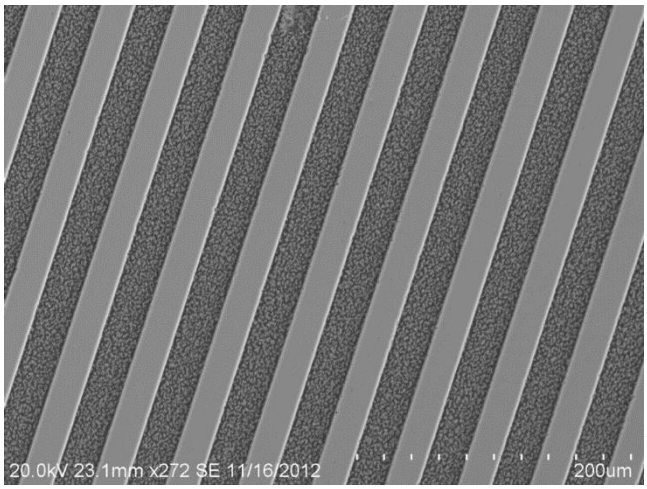

Figure 4-9: Low magnification SEM image of extensive microfeature formation at the bottom of the trenches, each white spot is the top of a micropillar.

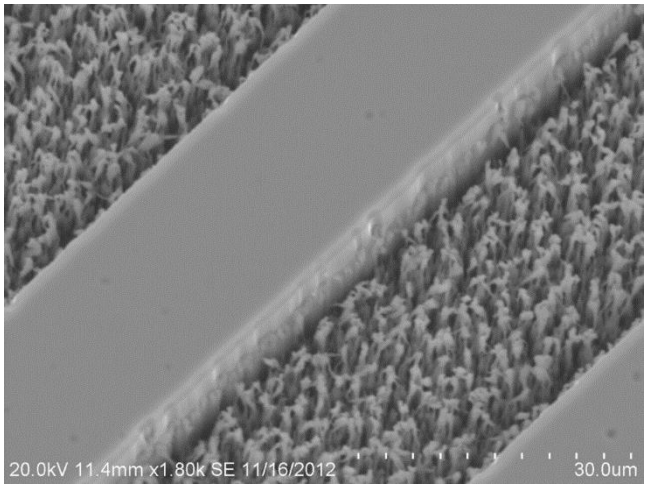

Figure 4-10: Increased magnification of the same sample as Figure 4-9, showing microfeatures in greater detail. Microfeatures were likely formed due to the redeposition of etching products.

A sample with longer etch times and trench depth of about 29 µm is shown in Figure 4-11. The sidewalls are relatively smooth, however the trench bottom is somewhat pitted. Also, the top of the fins appear chamfered from where the ITO receded during the plasma etch. When the etchant mask recedes, it will actually widen the etching window. This sample was processed with high-gas flowrate, with a combined flowrate of 200 sccm of SF_6 and oxygen. The RF

power was set at 400 W and the ICP power was 2000 W. The roughness of the trench bottom as well as vertical ribbing present on the trench sidewalls are shown in Figure 4-12 using higher levels of magnification.

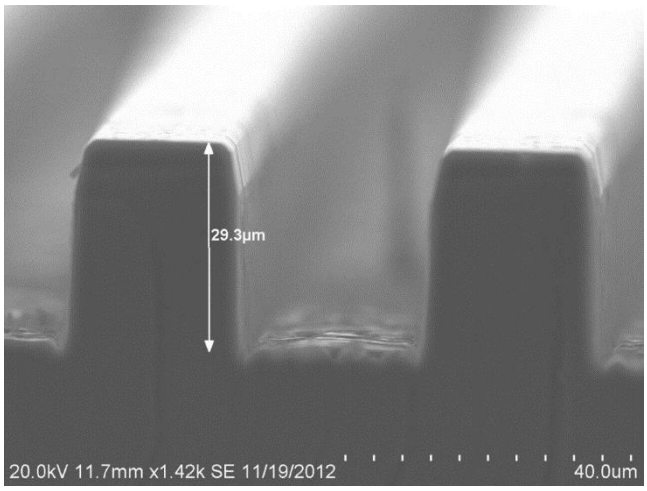

Figure 4-11: SEM image of a different etching sample that exhibited the recession of the etchant mask and allowed the top portion of the SiC fin to become "chamfered" as the mask pulled back, opening the etching windows. SiC trench with a depth of 29 µm and width of approximately 27 µm.

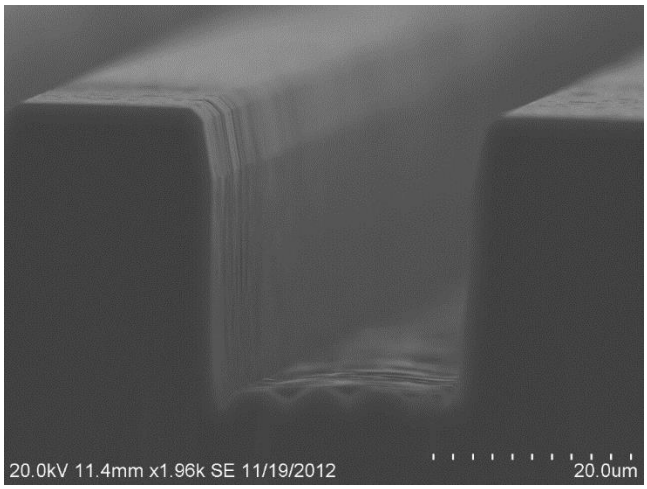

Figure 4-12: SEM image of the overall roughness of the bottom of the trench and the vertical striations along the sidewalls. Also shown is the widening near the top due to the etchant mask receding.

4.3 Planar 10 mm x 10 mm

It was decided to fabricate a planar device from a 10 mm x 10 mm die. To obtain a planar device, the ITO etchant mask was chemically stripped from a SiC die. The die was chosen due to the fact that the photoresist pattern had not developed correctly, so the etchant mask in that region was incomplete (Figure 4-5). The ITO was stripped using the solution of $HF:H_2O_2:H_2O$. Then the SiC die was chemically cleaned using acetone, isopropanol, piranha etch, and Baker Clean as discussed previously. A topside contact consisting of a layer of titanium (500 Å) followed by a layer of gold (2500 Å) was deposited. Titanium acts well as an adhesion material, while gold forms a reliable contact layer. A 2 μm thick layer of ^{10}B was deposited on top of the contact layer. After the deposition of the boron layer, the device was removed from the e-beam evaporator. The device was then immediately coated with Humiseal to prevent delamination of the boron layer. The backside contact was fabricated with the same Ti/Au (500 Å/2500 Å) layers. An additional planar device was also processed at the same time that did not have the boron layer.

Both detectors were mounted onto disposable detector boards (DDB) for initial leakage current and capacitance testing (the DDBs were remnants from a different project). A DDB is shown in Figure 4-13. The planar detectors were mounted using two-part, conductive silver epoxy. The topside contacts were cleaned with acetone and isopropanol. Then wirebonded to the contact pad on the DDB. The wirebonds were covered with a two-part, non-conductive epoxy for protection. The purpose of these planar devices was to provide baseline data for neutron and gamma testing as well as device characteristics, these results are presented in Chapter 5.

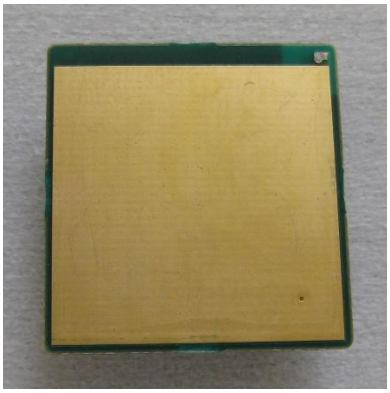

Figure 4-13: DDB prior to mounting of a SiC device, nominally 2 cm x 2 cm. Contact pad for wirebonds is in the top right corner.

4.4 Etched 10mm x 10mm

After the 10 mm x 10 mm design with a pitch of 40 µm, the work moved to a 10 mm x 10 mm design with a pitch of 8 µm and an aspect ratio of 0.5. This design change was necessary to properly utilize ^{10}B as the neutron reactive material. By referring to Table 3-2 it is possible to determine that the most optimal pitch and aspect ratio for microstructured devices within a silicon carbide substrate with ^{10}B is a 4 µm unit cell with a ratio of 0.8. This form factor would result in trench widths of 3.2 µm and fin widths of 0.8 µm. With trench widths of 4 µm and a ratio of 0.8, it would be necessary to etch depths of at least 10 µm for 15.4% and 20 µm for 31% maximum theoretical detection efficiency.

However, it was decided to proceed with a design pitch of 8 µm as a compromise between performance and fabrication capabilities. There were concerns regarding the etchant mask receding, which would result in the widening of the trench and narrowing of the top of the SiC fin simultaneously. Also, there were concerns about the etching rate of 3 µm wide trenches and gas loading. Gas loading is where the gas and etching products stagnate within the trench

and are not cleared away. If the products are not cleared out in a timely manner, it is possible for them to redeposit on the working surfaces. Gas loading can also prevent fresh etching gas radicals from entering the trenches and prevent further etching to work.

As shown below in Figure 4-14, AZ 2070 negative photoresist can be utilized to conduct liftoff processing even for features with gaps as small as a two microns. The characteristics of the photoresist can be somewhat manipulated via alterations to the photoresist recipe. Parameters such as the thickness can be increased by lowering the RPM of the spin-on step or decreased by raising the RPMs of the spin-on step. The amount of undercutting can be controlled by the developing time. The fact that the photoresist is tapered is actually somewhat beneficial. This tapering prevents materials from being deposited on the side of the photoresist lines, which would then inhibit the Kwik-Strip solution access to the underlying photoresist. If the Kwik-Strip is unable to reach areas of photoresist, it can be challenging to properly remove the deposited material during liftoff. The amount of tapering that may occur during the photoresist development is shown in Figure 4-14. This SEM image is of AZ 2070 photoresist lines that are about 7 µm tall and 4 µm wide at the top. At the bottom, the lines have tapered to about 2 µm wide, so the undercutting is about 1 µm per side.

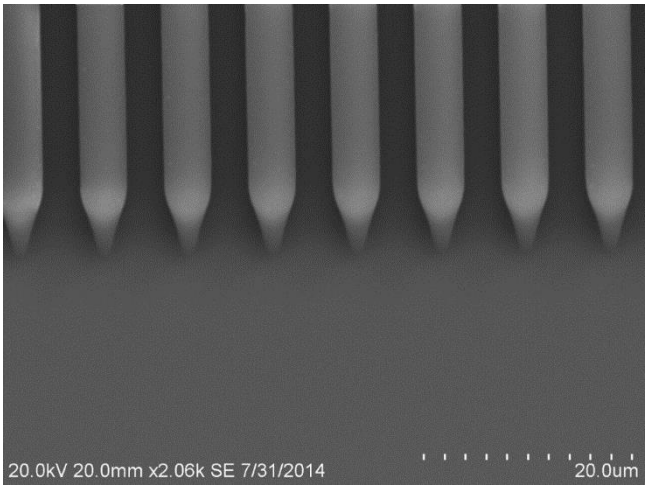

Figure 4-14: AZ 2070 negative photoresist prepared for the ITO deposition. Each photoresist line is approximately 7 µm tall and 4 µm wide at the top. The narrowing at the base is due to over developing of the photoresist.

Even though evaporation is nearly an anisotropic process, when working on these small feature sizes, there is still some variation in the thickness of the deposited layer due to shadowing affects. This behavior is evident in Figure 4-15, where the photoresist lines had substantial undercutting, which lead to deposition of material on the etching windows (arrow in Figure 4-15). The bottom of the photoresist lines are about 1.5 µm wide. It is detrimental to have ITO on the etchant window during the plasma etching process because this outcome will lead to unpredictable results due to trench widening. The trench widening during etching is not conducive to having a uniform trench bottom.

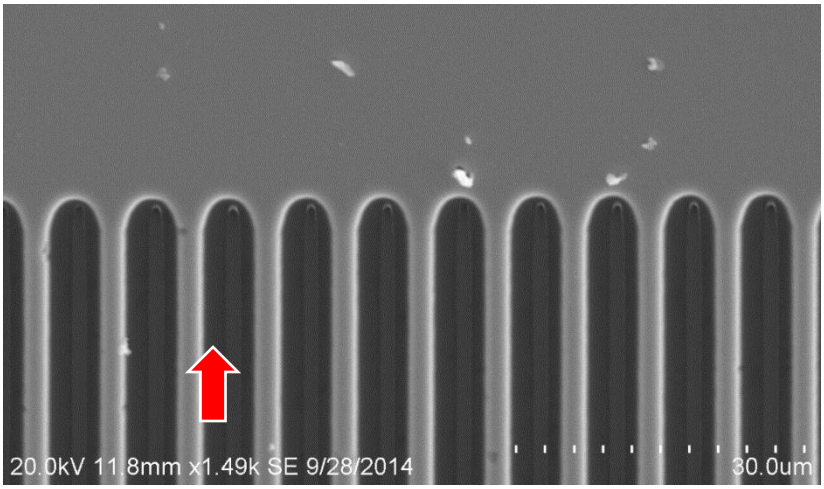

Figure 4-15: SEM image of the ITO etchant mask after the liftoff process. The ITO is the light gray regions, the silicon carbide substrate is the dark regions on the bottom half of the photo. ITO was also deposited within the etchant window due tapering of the photoresist lines (red arrow).

It was observed that the narrow regions between the photoresist lines took longer to fully develop. There were many photoresist attempts where (Figure 4-16 and Figure 4-17) the in-between regions did not fully develop. This incomplete developing would leave behind a thin-film of photoresist that prevented the deposition of the evaporated materials onto the actual wafer surface. Therefore, during the lift-off process, the materials would not adhere to the wafer and would be removed along with the photoresist. This effect is evident due to the lack of ITO on the main device area and the presence of the small remnants of ITO for the SiC fin areas.

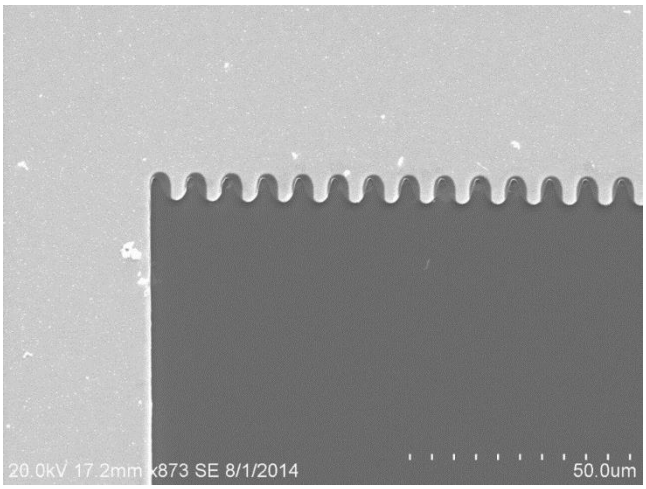

Figure 4-16: One issue due to the very small feature size was that if the developer was not fresh, then it would fail to properly develop away the photoresist between the lines of photoresist before the deposition of the ITO. The usage of old developer led to the etchant mask traces peeling away during liftoff. ITO is the light gray and the SiC wafer is the darker gray.

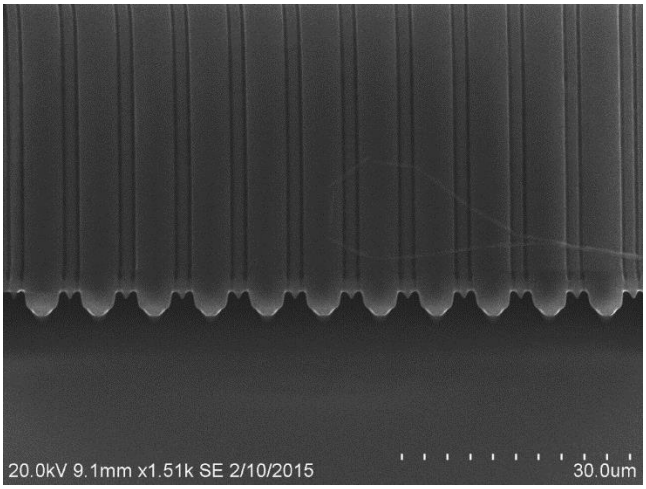

Figure 4-17: Image of photoresist remaining between the photoresist lines after developing. Likely due to the use of older developer.

Shown in Figure 4-18, it is apparent that the deposited layers would depend on the wafer orientation within the e-beam evaporator with respect to the source material and the photoresist orientation. It can be seen that the features on the deposited layer are not uniformly spaced around the photoresist lines, but instead, are shifted to one side. This effect could be handled

somewhat by careful orientation of the wafer upon the e-beam's planetary. Preferred wafer orientation allowed for the photoresist lines to be aligned vertically with respect to the source (Figure 4-19). Due to the e-beam evaporator's planetarium configuration, wafers are not loaded horizontally, but instead are angled to be normal with respect to the straight-line travel path from the source material crucible.

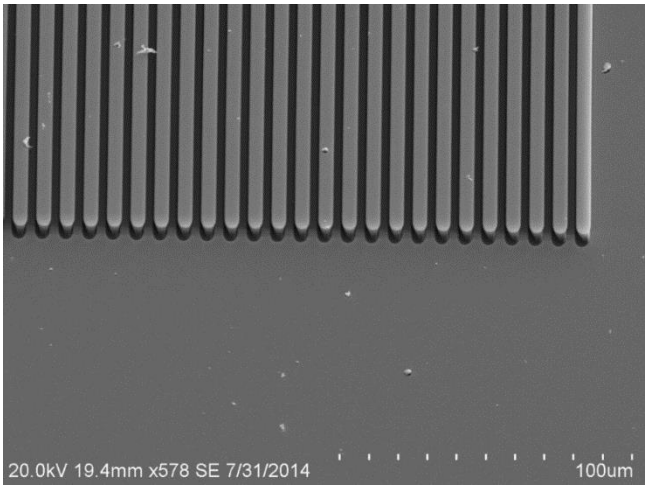

Figure 4-18: After the evaporation of ITO onto the wafer with patterned photoresist. From here the wafer would be Kwik-Stripped to remove the photoresist and the etching windows opened. Also evident is how the photoresist may not be centered within the windows of the deposited material.

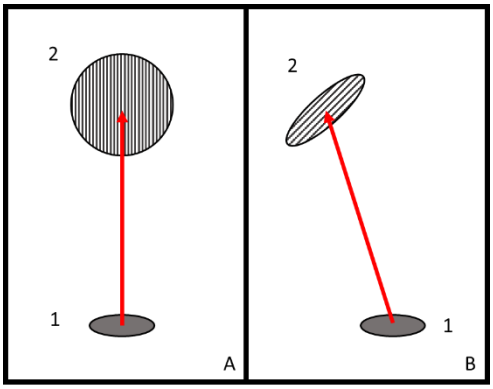

Figure 4-19: Wafer orientation within the e-beam evaporator. 1) Source material 2) Patterned SiC wafer. The view for panel B is rotated ~90º.

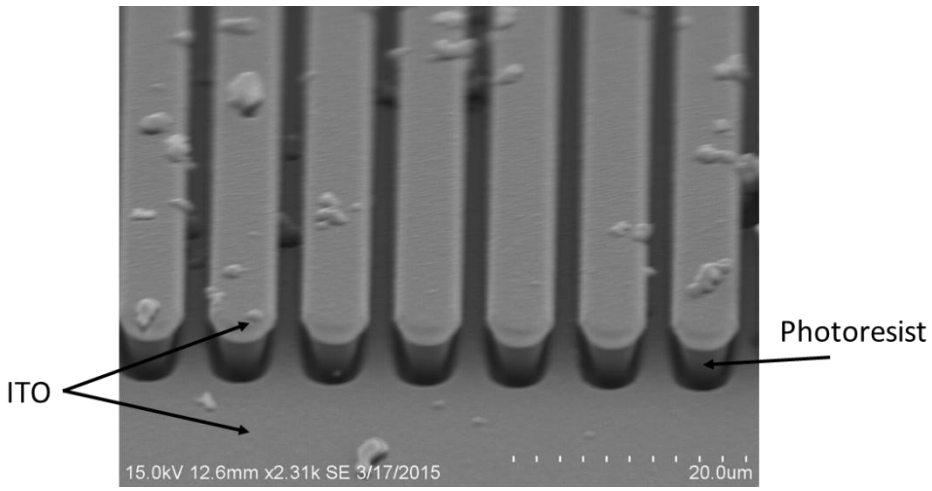

Figure 4-20: SEM image of a device-grade SiC wafer after the deposition of ITO, prior to lift-off processing. The sloping of the ITO edges is apparent. Also, there are numerous clumps of deposited material that is due to sparking of the source material.

A device-grade SiC wafer that was patterned with AZ 2070 photoresist and had ITO evaporated onto the surface is shown in Figure 4-20. There is a significant amount of material clumps present on all the surfaces and between the photoresist lines. These clumps are likely due to the ITO source material sparking during the evaporation. Sparking can be observed by the operator as small streaks or flashes of light traveling away from the source material. Sparking typically occurs when the source material is too hot, and may be remedied by slowly reducing power until the sparking stops. Another source of sparking is when a cooler chunk of source material falls into the molten region which causes very erratic behavior. This type of sputtering event can be avoided by slowly applying power and allowing for more uniform heating. Also, with careful maneuvering of the molten region the operator may eliminate any potential material that might fall.

After the evaporation of ITO onto a device-grade SiC wafer, the wafer was then diced. A partial edge piece was cleaved and the cross-section was examined using the SEM (Figure 4-21).

The evaporator's thickness monitor reported that ITO should be ~1.2 µm thick and it was measured via the SEM imaging as 1.5 µm, so the two systems are in fair agreement. Also, it is easily seen that the tops of the ITO lines are narrower than the bases. Again, this effect is due to the undercutting of the photoresist lines due to over-development.

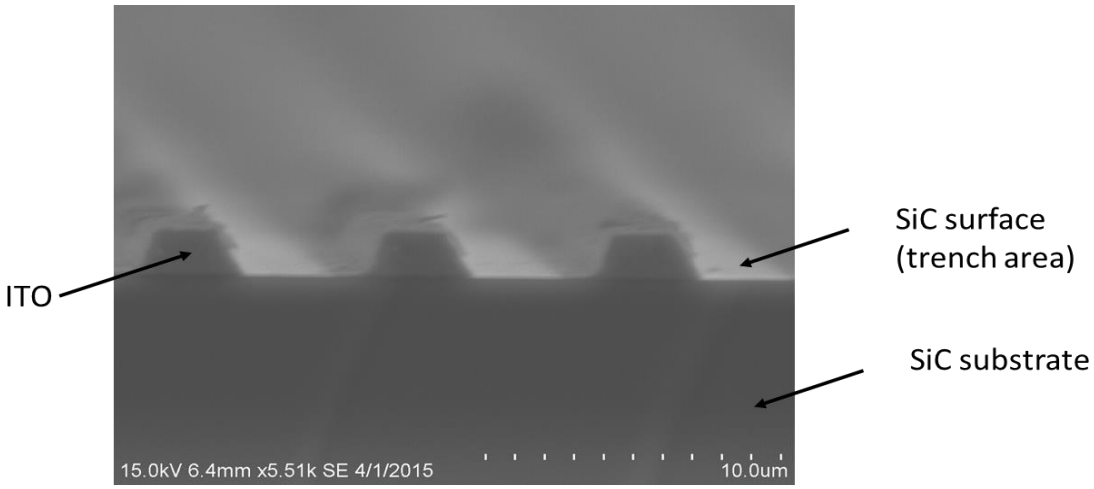

Figure 4-21: SEM image of a cleaved sample die from the SiC wafer in Figure 4-20 after lift-off processing. The sloped edges of the lines of ITO etchant mask material are readily apparent. As discussed above, this effect is due to the over-development and resultant undercutting of the AZ 2070 photoresist.

While the before "image" for the lift-off process is shown in Figure 4-18, the SEM image shown in Figure 4-22 is the "after" image. While the ITO etchant mask and etching windows are readily apparent. After close examination, it is possible to see that some ITO material was also deposited within the etching windows. As will be shown later, this undesirable deposition material leads to uneven plasma etching behavior.

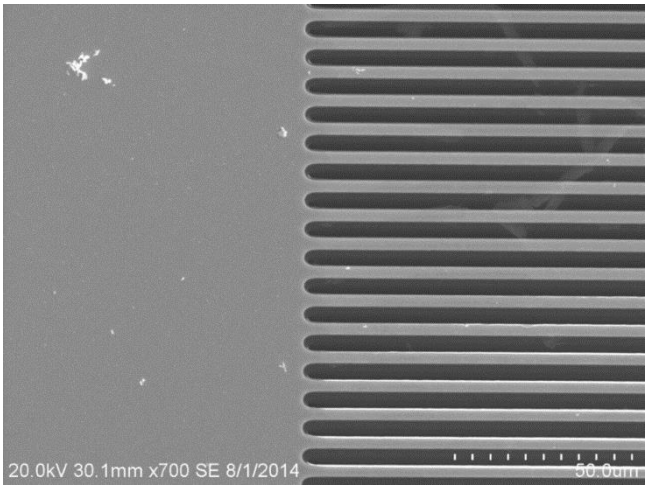

Figure 4-22: Remaining ITO etchant mask (the lighter areas and all of the left side) after lift-off process is completed. This image is after the wafer was Kwik-Stripped to remove the photoresist and open up the etching areas (the darker areas).

For the developing step, it is necessary to allow for sufficient time to ensure that the narrow strips of unexposed photoresist between the etching windows is properly developed away. Typically, this required the wafer to remain submerged in the developer longer than was needed for the large areas. As a result both ends of the photoresist lines would be slightly sloped or have a concave profile (Figure 4-23). This slope provided a region of photoresist that the e-beam would deposit material onto (Figure 4-24). Shown in Figure 4-15 and Figure 4-25 are SEM images of the same wafer after deposition of ITO and subsequent lift-off processing. However, between images, the area of the wafer under examination was shifted from the "top" region of the etching windows (oriented as in Figure 4-6 so that the bond pad up) to the "bottom" region of the etching windows (the opposite or bottom of the device area). Shown in Figure 4-15 and Figure 4-27, the smooth rounded etching windows of proper dimensions are easily recognizable. Shown in Figure 4-25, the ends of the etching windows taper to a point and the majority have a bright white spot located at the very end. These white spots are actually the points of material that deposited upon the sloped end of the photoresist. A closer image of the

endpoints is shown in Figure 4-26. This effect is only seen on one end of the photoresist lines due to the fact that the wafers loaded onto the planetarium are not perfectly normal to the source crucible and direction of flight for emitted atoms.

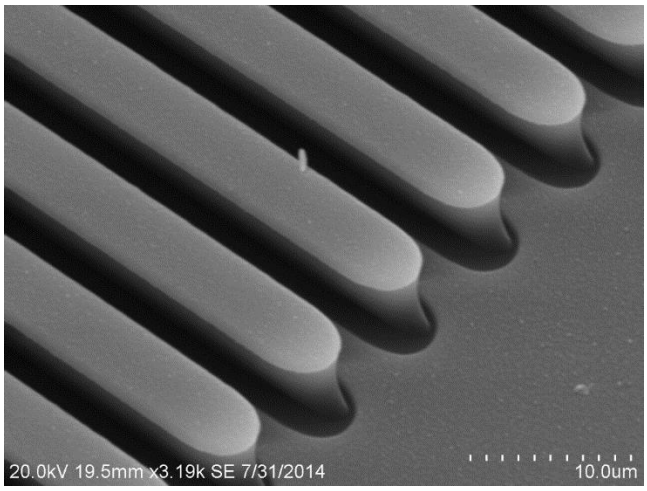

Figure 4-23: SEM image of the sloped, concave ends of the photoresist lines. This behavior is due to the over developing necessary to ensure the photoresist is completed removed from between the etching windows.

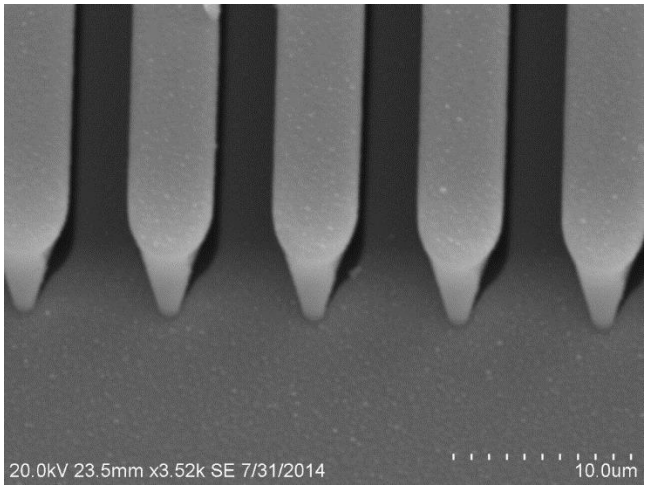

Figure 4-24: SEM image of the ITO deposited on the sloped end of the photoresist lines, which is also observed as white spots on the following figures. This image was taken prior to liftoff.

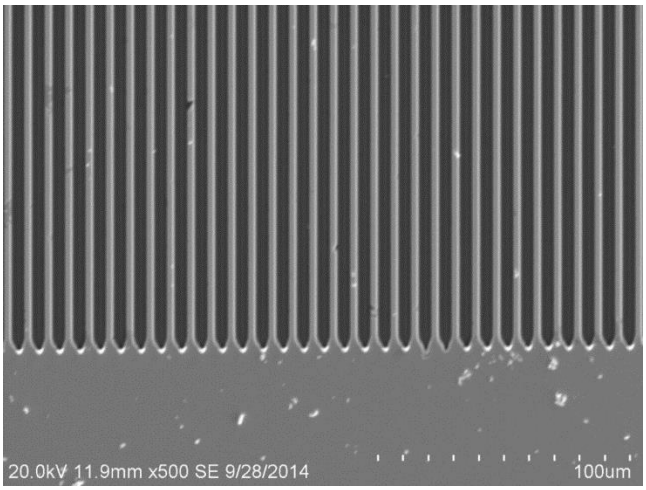

Figure 4-25: A lower magnification SEM image of the ITO etchant mask. Here the ITO is the light gray regions, primarily on the bottom of the picture. Again, the dark regions are the SiC substrate.

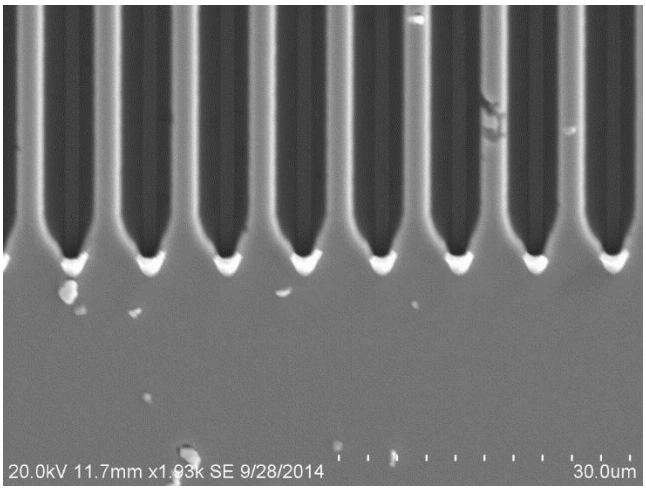

Figure 4-26: Higher magnification view of the endpoints of the etching windows after the ITO deposition. The white points are where the ITO deposited on top of the sloped end of the photoresist lines.

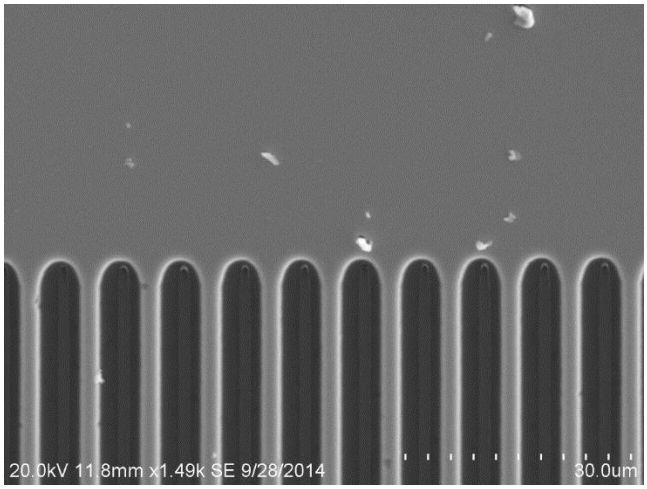

Figure 4-27: Opposite end of the same device. Note that the white points are not present, due to the fact that at these feature sizes, there is some variations of the deposition process within the e-beam evaporator.

The propagation of photoresist and material deposition issues through device processing is demonstrated in Figure 4-28. Each trench end is pointed instead of the desired rounded end. These sharp features may lead to issues later when a voltage bias is applied to the device. From Figure 4-28, one can conclude that these sites may lead to lower signal-to-noise ratio or lower maximum operating voltage bias.

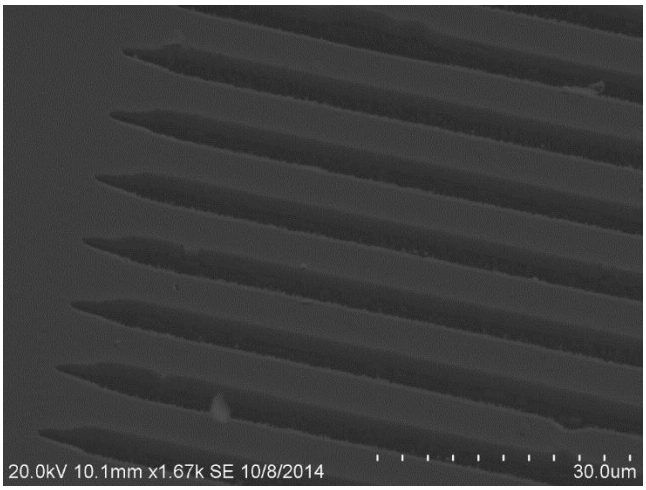

Figure 4-28: SEM image of an etched device that has had the remaining ITO etchant mask chemically removed. Of interest are the pointed trench ends due to the issues with the endpoints of the photoresist lines and ITO deposition.

Figure 4-29 is a low magnification SEM image of the patterned ITO etchant mask. The ITO is the solid gray region. This is an image of an intersection between 4 individual die. Note the bond pad for one die (red arrow) on the bottom-left die. Also visible are alignment marks at the junction of the dicing areas. This image was taken prior to dicing. Dicing paths are represented by the red, dashed lines.

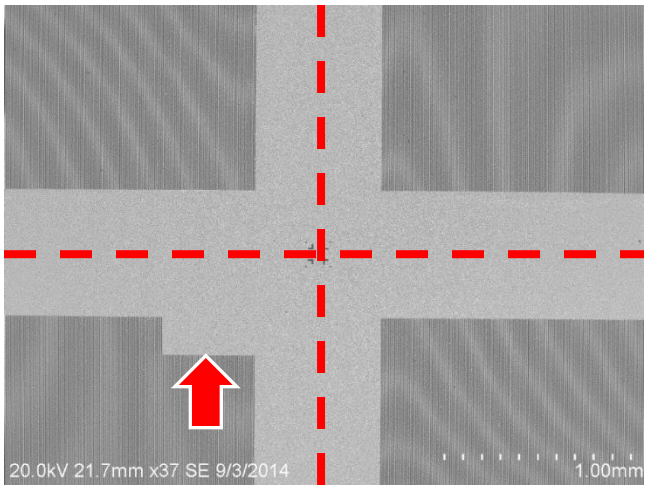

Figure 4-29: A very low magnification SEM image that contains corners of 4 devices. The ITO etchant mask is the lighter gray region. The large areas of ITO also provide the dicing areas. Note, this was imaged pre-dicing. Red arrow is pointing to the bond pad. Red, dashed lines represent the dicing lines.

Following are SEM images from several different plasma etching trial runs. As discussed above, there are several process parameters may be adjusted per trial run. These trial runs did show somewhat promising features. There are definitely some micropillars present. Also, it is obvious in Figure 4-30, that there was some biasing towards one side of the trench. This behavior is likely due to a thin deposition of ITO to one side of the etching window. Process parameters were as follows, relatively low process chamber pressure of 7 mTorr, high SF_6 gas (etching gas) flow rate of 200 sccm, and high process RF and ICP powers, 200 and 2200 W respectively.

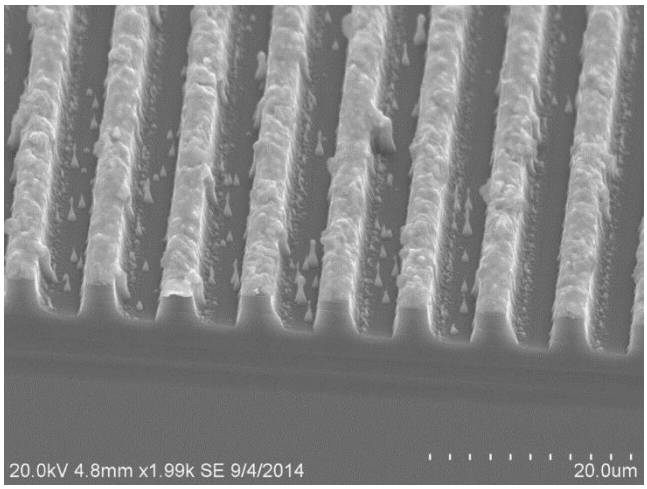

Figure 4-30: Top down SEM image of an etched silicon carbide device. Micro-features are visible in the trench areas

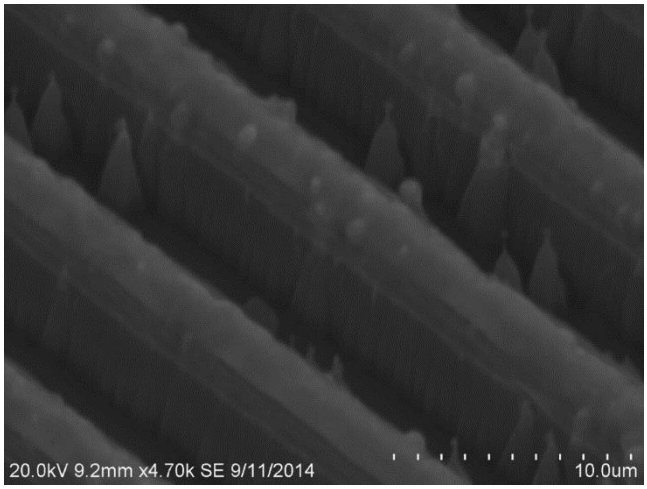

Figure 4-31: Angled SEM image of the sidewall and trench bottom of etched SiC device. Micro-features are evident in the trenched area.

As the process duration was increased to achieve deeper trenches, some undesirable changes were observed (Figure 4-32). It was apparent that the ITO etchant mask experienced severe receding during the etching, leading to widening of the etchant window. The mask withdrawal led to a V-shaped trench profile. Also, the remaining etchant mask is triangular in shape.

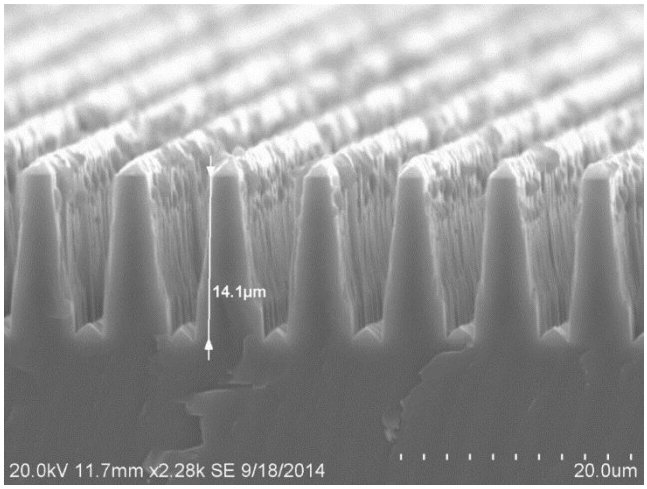

Figure 4-32: Cross-sectional view of a cleaved SiC device, etched to a depth of 14µm. Very rough sidewalls, with substantial tapering to the bottom of the trenches. No real trench bottom even present and the tops of the fins are extremely narrow.

Shown in Figure 4-33 and Figure 4-34 are SEM images of the same SiC die. A top-down look at the trenches and micropillars is shown in Figure 4-33. The cleaved edge is shown in Figure 4-34. This trial run did yield relatively straight sidewalls and trench bottoms. However, the presence of the micropillars likely indicates masking during the etching process either from etching products redepositing during the plasma etch or from ITO sputters during the etchant mask deposition.

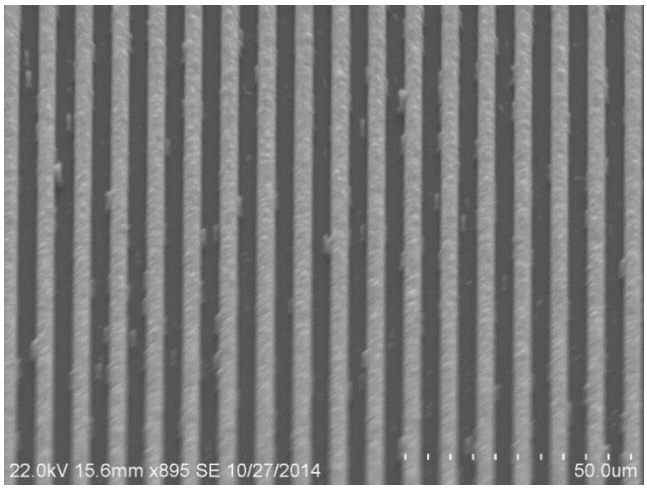

Figure 4-33: Top-down SEM image depicting the limited production of microfeatures within the trenches.

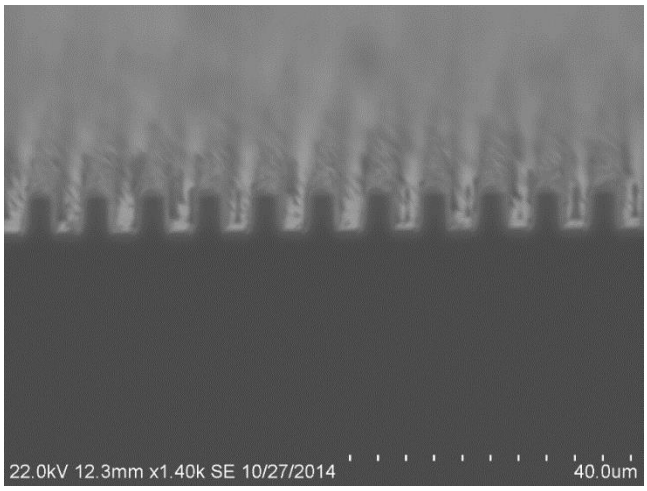

Figure 4-34: Cross-section view of a cleaved wafer. Approximate trench depth is 5 µm. Also, can see the improved trench uniformity. However, still showing a significant number of micropillars.

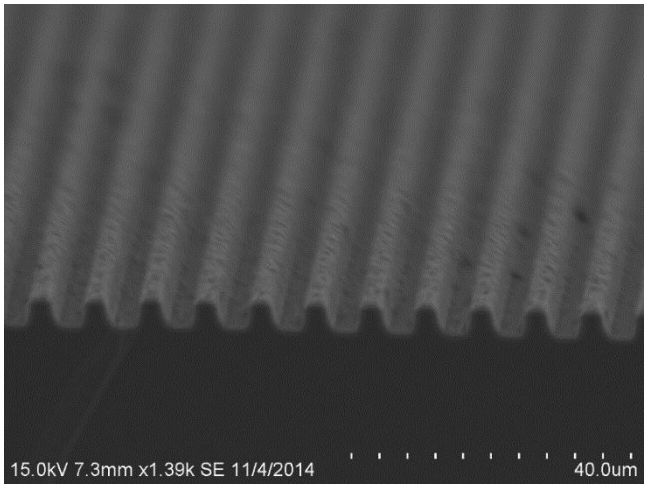

Figure 4-35: SEM image of cleaved wafer, approximate depth is 5 µm. Demonstration of the repeatability of etching results.

The sloped sidewall in Figure 4-35 and Figure 4-36 is likely due to the initial photoresist undercutting during developing. This behavior is another issue of the deposition of material

within the etching window. It is possible to observe some micropillars present within the trenches. Also, the remaining etchant mask material is extremely rough and textured on the fins. However, it has been observed that after the remaining etchant mask is chemically stripped, the top of the SiC appears smooth. Although the trench sidewalls are very rough.

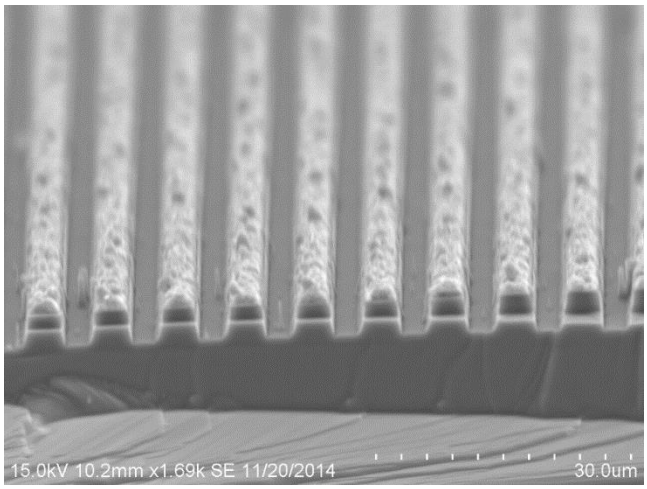

Figure 4-36: SEM image of cleaved wafer, approximate depth is 5 µm. Evident are the straight sidewalls and uniform trenches and minimal production of microfeatures.

4.4.1 Topside Contact Formation

It was decided to fabricate the contact layer prior to fabricating the etchant mask. To facilitate this work, a new photomask was designed via L-Edit (editing software used to layout photomasks for printing) that would work in conjunction with the current 10 mm x 10 mm mask with the 8 µm pitch. It was decided that the metal traces over the SiC fins were going to be about 2 µm wide and the open window would be ~ 6 µm wide. Also, the windows on the contact mask were longer than the windows of the etchant mask. This design feature was purposefully done to aid in alignment during photoresist processing, as well as prevent the plasma etching

gases from attacking the metal contact layers. The etchant windows remained constant at 4 µm wide. A cross-sectional view of the desired device layering is shown in Figure 4-37.

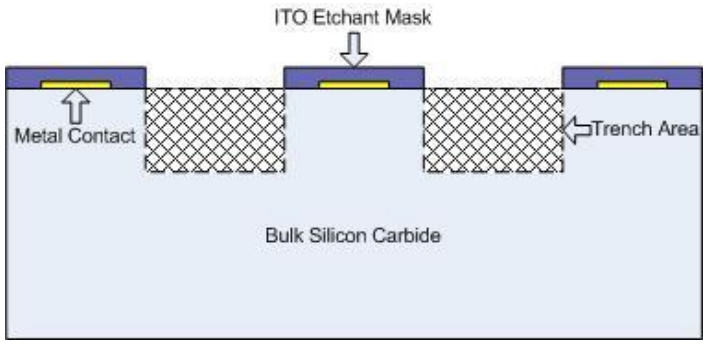

Figure 4-37: Cross-sectional view where the top contact is formed prior to the sputtering of the ITO etchant mask. The trench area illustrates where the trenching should occur. Note, the metal contact should be remain shielded from the etching gases by the ITO.

Initial efforts in fabricating the contact layer used selective wet etching. First, the SiC would be chemically cleaned and then loaded directly into the e-beam evaporator. Next, Ti/Au (300 Å/2500 Å) layers would be deposited. Then AZ 1512 positive photoresist was applied to the wafer and exposed using the metal contact photomask. The Au layer was etched using Aqua Regia. The solution was made from 1 part nitric acid and 3 parts hydrochloric acid. Aqua Regia is clear when freshly combined. After a few minutes of mixing, it quickly assumes a bright red color. Aqua Regia will etch gold very quickly, and a quick dip of less than one minute was sufficient to remove the gold layer. Then the Ti layer was etched using a solution of 1 part HF and 9 parts H_2O. After the metal layers were etched, the photoresist was removed using Kwik-Strip, then rinsed with acetone and isopropanol. The same area is shown in Figure 4-38 and Figure 4-39 under different levels of magnification. From Figure 4-39, it is easy to see that the metal traces were highly susceptible to over etching and the final traces are only about 1 µm wide instead of the intended width of 2 µm.

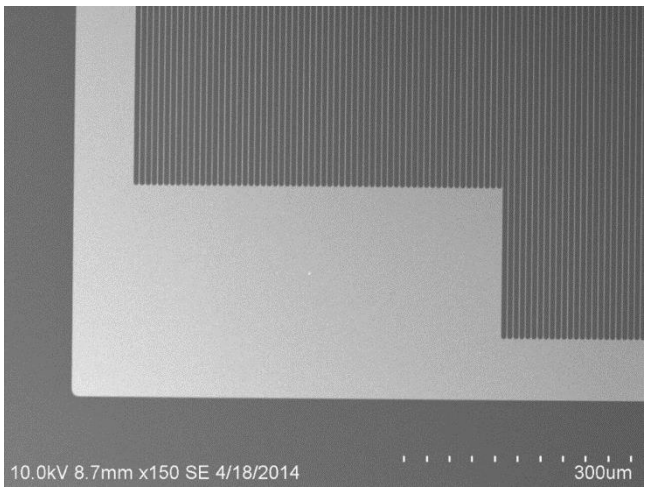

Figure 4-38: Metal traces formed by using AZ 1512 postive photoresist to selectively etch already deposited Ti/Au layers.

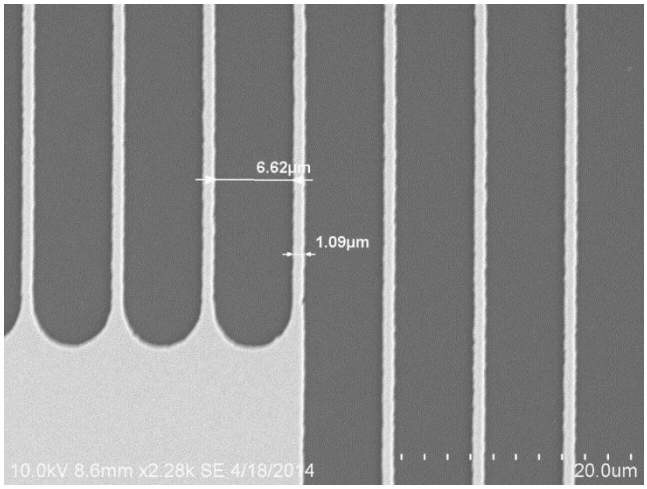

Figure 4-39: Higher magnification of the metal traces. Trace lines are approximately 1 µm wide and about 5 mm long. The traces were highly susceptible to over etching.

After several trials using silicon test wafers that resulted in severe overetching, it was decided to use liftoff techniques instead. Fabricating the metal contact layers via liftoff provided more repeatable results.

With the contact layer formed, the next step was applying AZ 2070 photoresist and forming the etchant mask. Due to the allowance of only 1 μm of space on either side of the etchant window and the length of 10000 μm (10 mm), it was necessary to be extremely exact with regards to the theta rotation between the metal contact and the etchant mask. Even a very small misalignment was sufficient to necessitate the reprocessing of the etchant mask photoresist layer. Also, if the photoresist was shifted too close to a particular side it would necessitate reprocessing. If the photoresist was only slightly biased to one side, it was possible, with careful positioning during loading to influence etchant mask deposition to shift the etchant window back into position (see Figure 4-69 and Figure 4-70). Possible outcomes when patterning the etchant mask are depicted in Figure 4-40. This process was further complicated by the fact that the High Magnification setting on the photoaligner was not strong enough to properly make out the existing patterns or alignment marks during exposure (Figure 4-41).

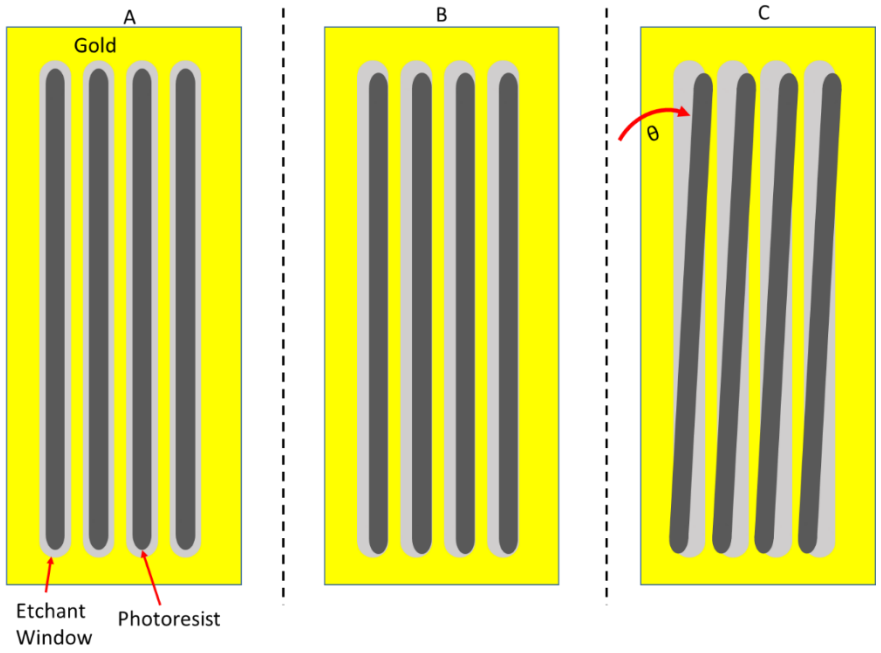

Figure 4-40: Panel A depicts correct positioning and alignment between the photoresist lines for the etchant mask and the existing metal contact layer. Panel B depicts the correct theta alignment, but poor positioning. Minor cases might be corrected with proper positioning. Panel C depicts improper theta alignment. In practice, the final result may be a combination of B and C.

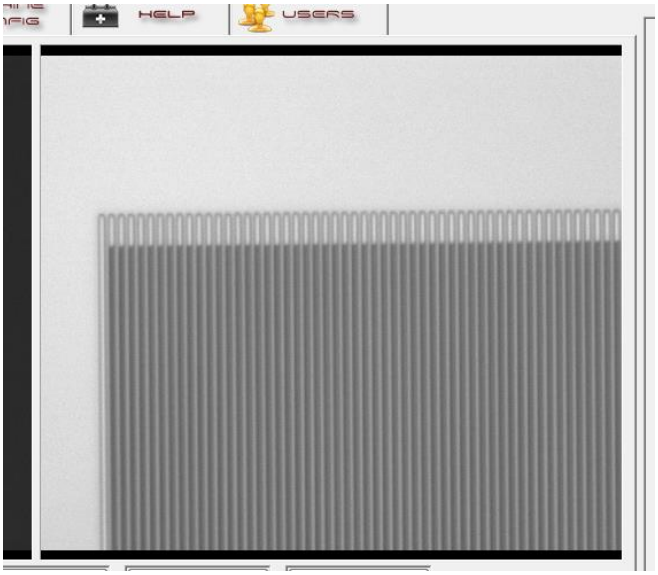

Figure 4-41: Screenshot of the photoaligner screen during alignment of the photomask to a wafer with metal traces. The traces are extremely difficult to see even at high magnification.

A low magnification SEM image of the bonding pad area of a wafer with the metal contact layer and AZ 2070 photoresist is shown in Figure 4-42. After the photoresist is developed, the wafer is ready for etchant mask deposition. Higher magnification views of the wafer in Figure 4-42 are shown in Figure 4-43 and Figure 4-44. Notice the gap at the top or bottom of the etchant windows between the lines of photoresist and the metal contact area. It can also be observed that the theta rotation is very good and there is very little bias on either end of the pattern.

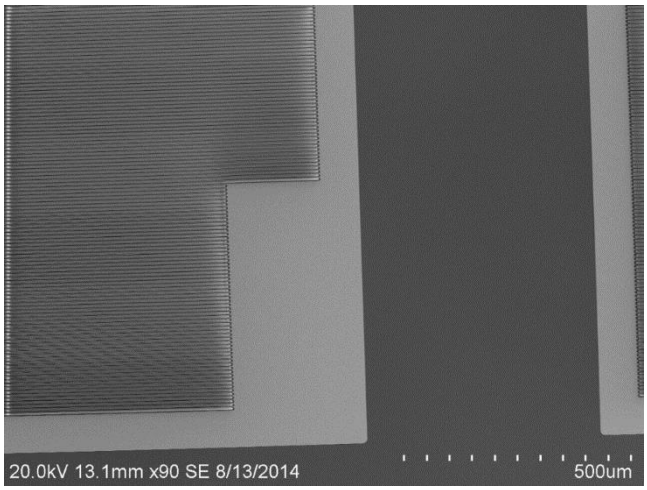

Figure 4-42: Low magnification image of the metal traces with the AZ 2070 photoresist in preparation for the etchant mask deposition.

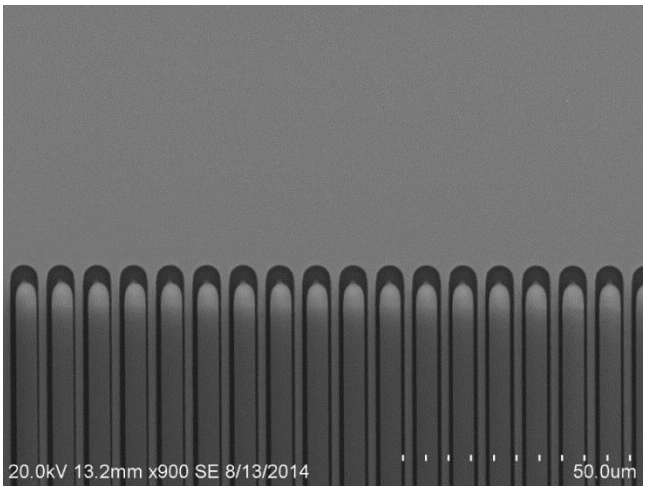

Figure 4-43: Top down view of AZ 2070 negative photoresist with gold contact/traces. The dark areas are the silicon carbide substrate. The thin, vertical strips with rounded ends, are the photoresist lines. The top area and vertically descending traces is the contact (Ti/Au 30nm/250nm).

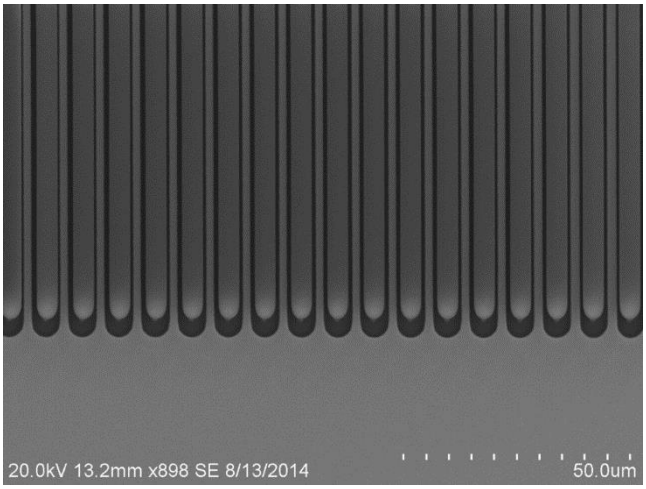

Figure 4-44: Top down view of the opposite end of one device to view the other end of the photoresist lines.

Higher magnification images (Figure 4-45 and Figure 4-46) of the same wafer to observe the undercutting that occurred during the photoresist developing. The photoresist appears to be centered within the open window.

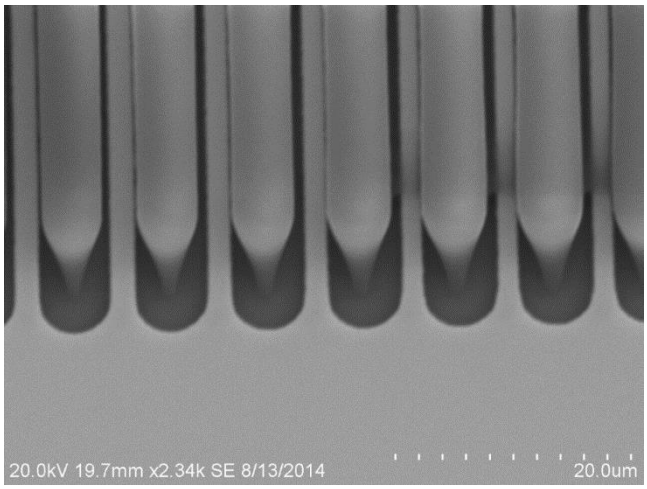

Figure 4-45: Substrate tilted 30°, view of the photoresist strips, the gold contact/traces, and the visible silicon carbide substrate. The undercutting of the photoresist is readily apparent.

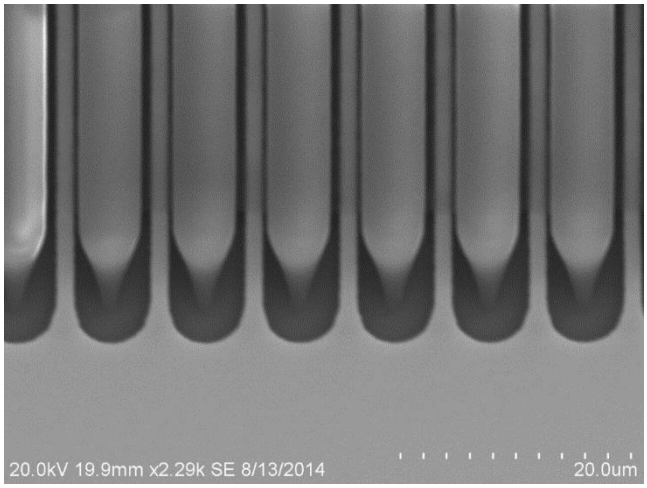

Figure 4-46: Same configuration as Figure 4-45, repositioned to a different location.

The photoresist lines on the edges of two adjacent devices is shown in Figure 4-47 and Figure 4-48. It can be seen on both images that the outermost lines "lean" towards the center of the device. This lean may have occurred during the developing stage as the liquid developer pushed against the photoresist lines.

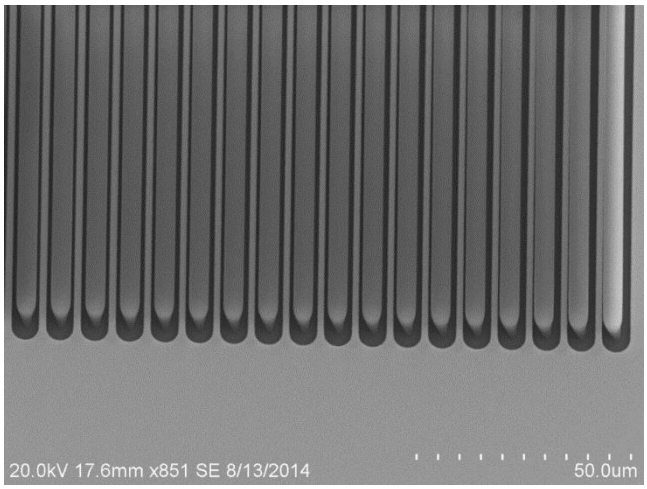

Figure 4-47: Substrate at 30° tilt. Image taken of the edge trench lines to demonstrate the "lean" of the photoresist near the perimeter of a single device.

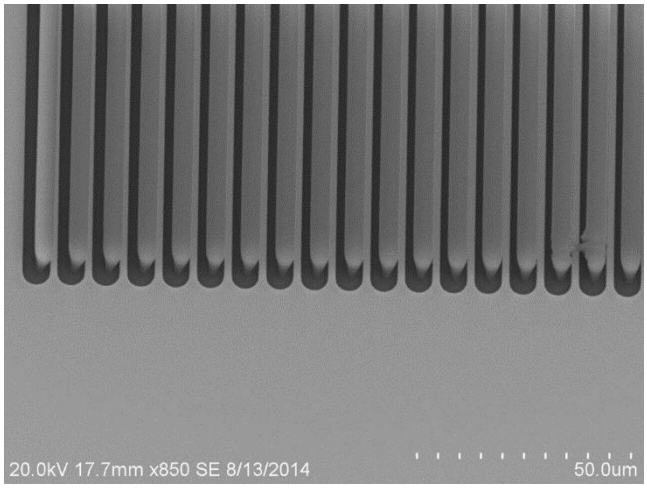

Figure 4-48: Same configuration as Figure 4-47. Image of neighboring device, to illustrate that the photoresist "leans" towards the inside of a device.

An optical microscope photo of the metal traces and photoresist lines is shown in Figure 4-49. This photo was taken within the cleanroom, at 100x magnification.

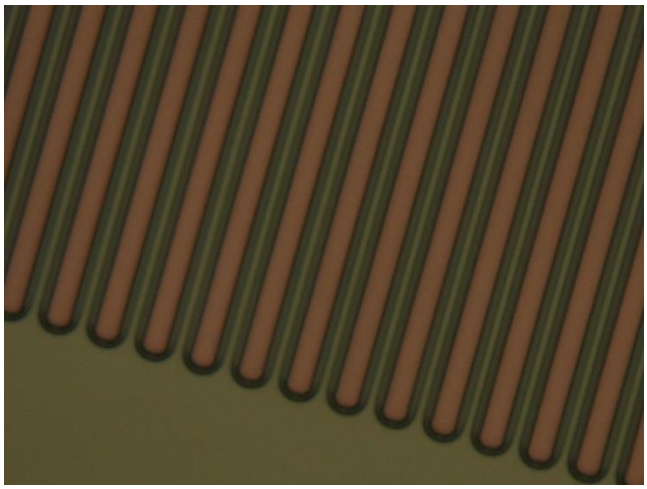

Figure 4-49: Optical microscope image of the metal contact layer with the photoresist lines prior to etchant mask deposition.

After several trials where the metal contact mask was properly formed via liftoff and substantial difficulty was encountered during alignment of the etchant mask, it was decided to not pre-form the metal contact layer but instead to form the contact layer after etching.

4.4.2 Post-Etching Contact Formation

A detector-grade SiC wafer was patterned with the etchant mask, diced, and a die was plasma etched. After plasma etching, the remaining ITO was removed with BOE and then cleaned via a multi-step process including acetone, isopropanol, Piranha Clean, and Baker Clean. Then the die was loaded into the e-beam and a Ti/Au contact was evaporated onto the backside. Next, the chip was flipped over and reloaded into the e-beam evaporator. This time, the SiC die was tilted at a high angle (approximately 70º - 80º) with respect to the source material. The device was also oriented so that the trenches were horizontal versus the vertical orientation used during etchant mask formation. This orientation was to force the metals to only deposit on the

top of the SiC fins and not within the trenches or on the sidewalls. It was observed that the Ti/Au contact was only being deposited on top of the fins (Figure 4-50 and Figure 4-51). The bottom left corner was covered with a piece of Kapton tape during the evaporation for comparison purposes. The bottom left corner has a different coloration than the remainder of the device. This boundary was more apparent during visual inspection.

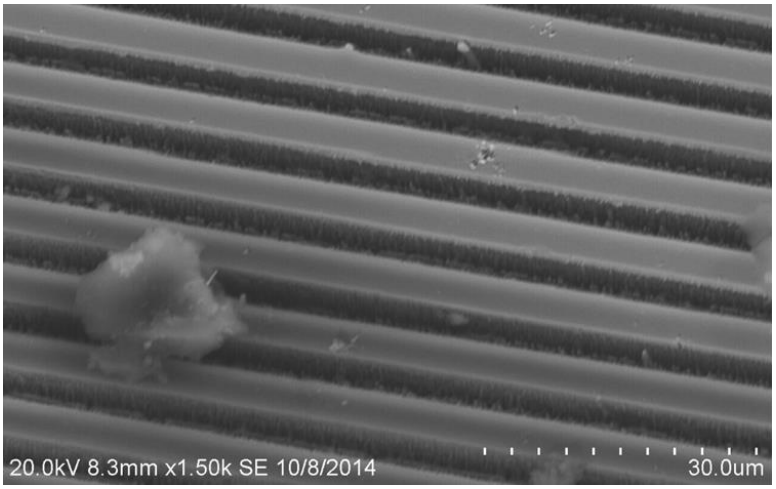

Figure 4-50: SEM image of the evaporated Ti/Au contact on an etched device. The region to the top right is the region that the material was deposited. Material was prevented from depositing on the bottom-left region by the Kapton tape.

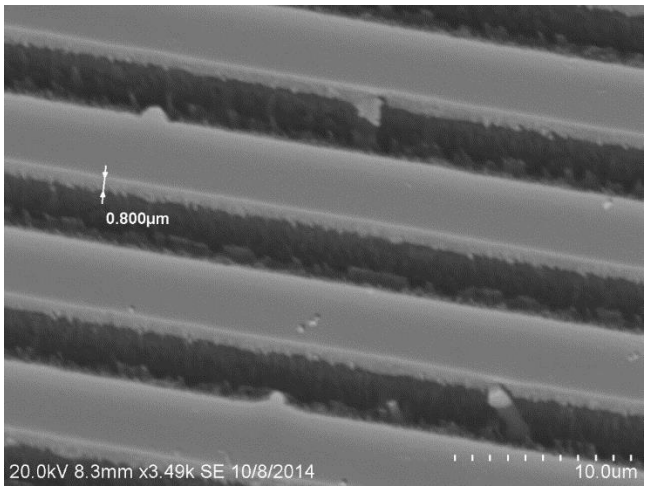

Figure 4-51: SEM image of the metal contact after evaporation. The Ti/Au contact layer is the light colored layer ontop of the SiC fin.

Initial formation of contacts used Kapton tape to mask the outlines of the contact area. 4 pieces of tape were used. Each piece of tape was placed so that it would cover a portion of the area between the trenches and the edge of the SiC chip. During the photomask design, it was determined that with the 10 mm x 10 mm devices, that the unit step size would be 10.65 mm per device for the photomask array. Because the trenches were centered within the design, there is approximately 0.325 mm of unetched space on any side of the trenches. After dicing, this space is reduced and is closer to 0.3 mm wide.

The use of Kapton tape as the masking method had various drawbacks. First was the fact that it was applied by hand, and getting proper placement could be somewhat of a challenge. It was difficult to correctly place the tape in a space that was only a couple hundred µm wide and was 10 mm long. If the tape was not perfectly aligned, it was necessary to pull the tape off and reapply it. Alternatively, the tape could be slightly realigned, which created non-uniform contact areas. It was possible to cover a portion of the trenches or for the tape to go off the edge of the device. Also, when viewing on the micron level, the edge of the tape was not smooth and there

were times that excess glue would squeeze out from under the tape. Furthermore, the deposited metal may partially adhere to the tape and peel or tear during the tape removal. Overall, while good for initial proof-of-concept trials, the use of Kapton tape as the masking method was unreliable.

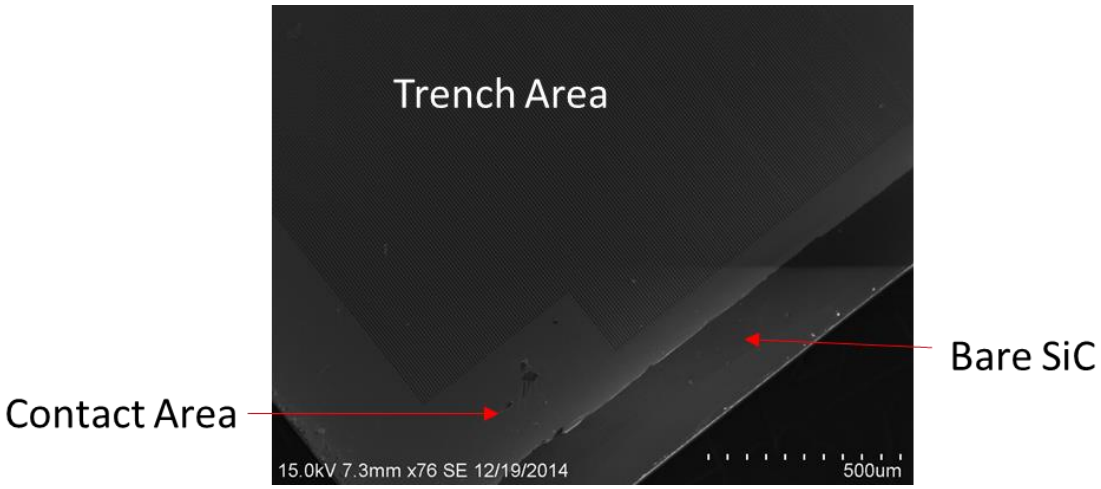

Figure 4-52: SEM image of the outer contact area. Note the irregularities on the edge due to the use of Kapton tape as the masking method. (The line/shading change is an image artifact from the SEM scan.)

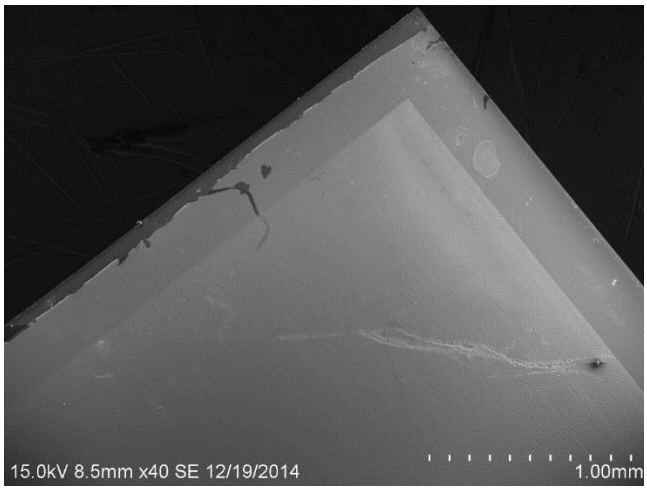

Figure 4-53: Another view of the issues with using Kapton tape for the contact formation. One side has multiple defects where the edge of the contact was damaged during tape removal. While the other side has the metal contact going all the way to the edge of the SiC substrate due to tape misalignment.

After the formation of the top and back side contacts, it was necessary to "load" the SiC detector with the neutron conversion material. For this project, enriched ^{10}B powder from Eagle Picher was utilized. A small amount of powder was placed onto the trenched area using a clean spatula. Next the powder was worked into the trenches by hand, with additional powder added if necessary. This process is not very precise and led to a fair amount of wasted product. Also, there is always a concern of damaging the metal contacts or the SiC fins. After backfilling, the device was coated with Humiseal and baked at 80 ºC for 1 hour. The Humiseal helps prevent the loss of the boron powder during handling.

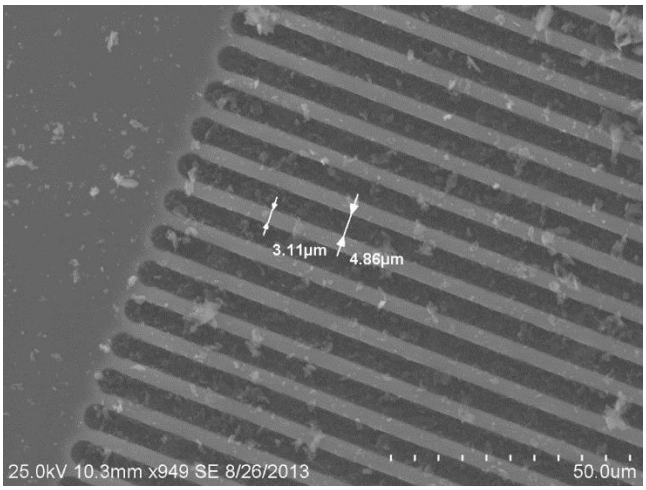

Figure 4-54: Low magnification of handfilled device. Shows relatively consistent filling across the device. No cap layer is present.

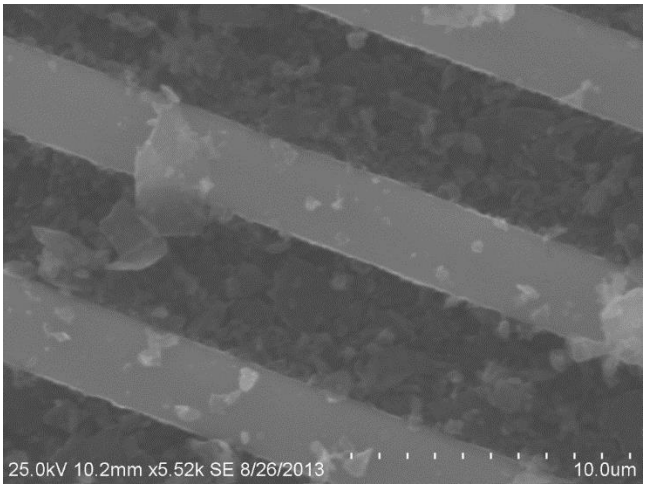

Figure 4-55: Higher magnification of handfilled device. Shows that the boron powder has chunks on the same scale as the device features..

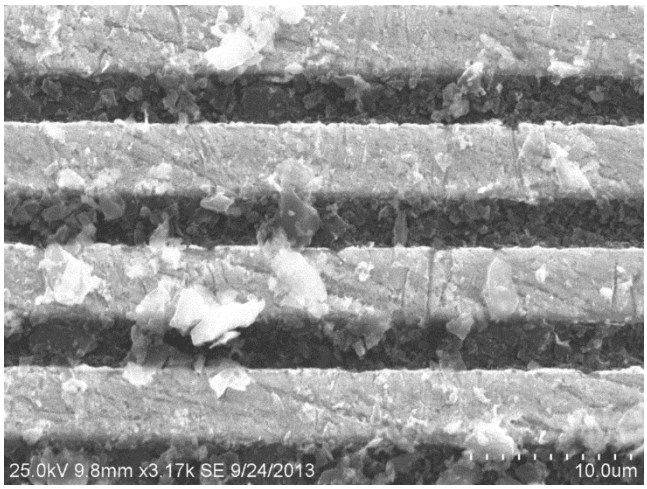

Figure 4-56: Another handfilled device. It appears that the surface of the material may be below the top of the trenches.

After the Humiseal is cured, the device is then mounted. The first step of the mounting process was to clean the Humiseal and any boron powder from the bonding pad with a micro-swab soaked with isopropanol. It was necessary to take care during this process so that the contact layer was not damaged. Next, the detector was mounted onto a DDB (as described in Section 4.3). The testing of these devices is presented in Chapter 5.

After testing the hand-filled devices, it was decided to deposit the ^{10}B via ebeam evaporation. For this purpose, SiC die were etched, stripped, cleaned, and Ti/Au contacts were fabricated on both sides. Next, the etched devices were loaded into the e-beam evaporator and approximately 0.5 μm of enriched ^{10}B was deposited into the trenches. This time, the devices were positioned so that the particles would be normally incident to the etched face. A metal shadow mask was used to restrict the boron deposition to only the trench area and no boron was deposited on the outer contact area. The darker region (of Figure 4-57) is the area coated with boron while the lighter regions are the gold contact. The evaporation did not appear to put appreciable material into the trenched areas. After the boron deposition, the devices were again

tested with alpha particles from ^{241}Am to ensure that there they were still sensitive to incident alpha particles.

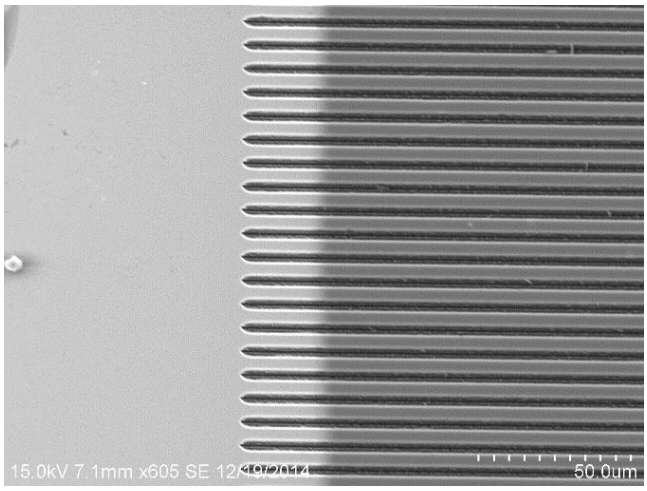

Figure 4-57: SEM image of the device after evaporated ~0.5 µm of enriched ^{10}B. A shadowmask was used to prevent the deposition of boron on the contact area. There appears to be no appreciable buildup of boron within the actual trenches.

Next, the etched SiC devices were bonded to alumina substrates with conductive silver epoxy. The switch to alumina substrates was made to allow for testing of detectors with alpha sources or to light sources. Then the top contact was wire bonded to the second contact area on the alumina substrate. Non-conductive epoxy was applied over the wire bonds to provide structural support and protection, as well as electrical isolation.

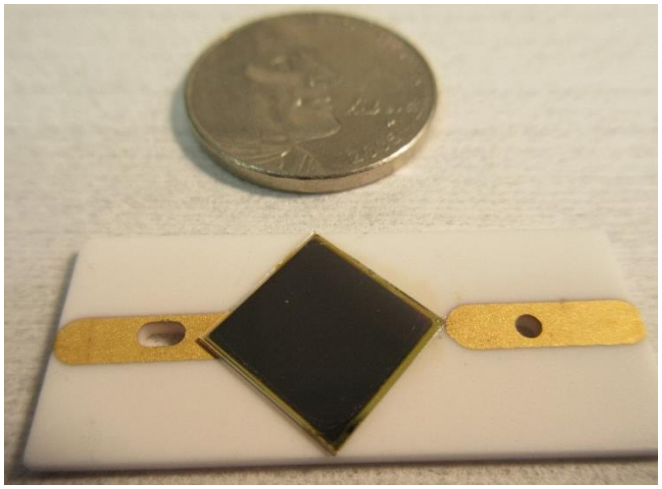

Figure 4-58: Picture of the mounted (10 mm x 10 mm) microstructured SiC detector on the alumina substrate with deposited gold contact pads for electrical connections. Nickel included for scale.

Figure 4-59: Etched and backfilled SiC device shown in Figure 4-64 after sealing with HumiSeal and mounting. On the right side is the black, non-conductive epoxy for the wirebond.

An additional change was the use of a micromachined shadow mask during contact fabrication. The mask was made from aluminum stock that was 8”x 3”x 1/16” (length x width x thickness). The milling programs were written in a basic text editor program (NotePad ++) in the G-Code format. G-Code provides the machine with instructions on bit rotation speed, and location in an XYZ format. The Z axis must be zeroed in relation to the work surface. During

the execution of the program, the operator can designate cut speed, length, depth, and direction. A simple pocket design was used where the large pocket was sized so that the SiC chips would fit snugly into the opening. Next, the opening was sized so that it was 0.200 mm smaller than the SiC chips (Figure 4-60). This design feature was chosen so that there was a 0.100 mm lip around the entirety of the SiC chip that would occlude the outer edge during the contact formation. The corners of the lip are rounded due to the fact that the end mill bit size was 0.030" or ~0.762 mm and is of a similar scale as the device dimensions (Figure 4-61).

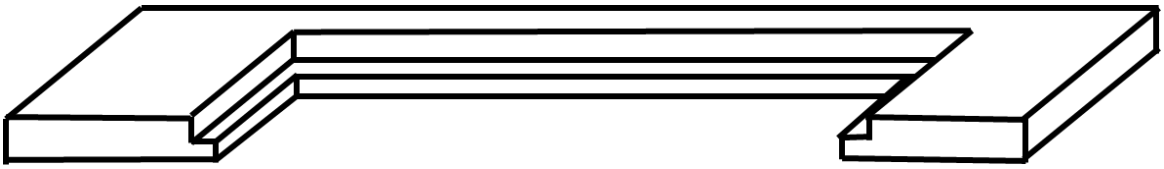

Figure 4-60: Sketch of the cross section of the shadowmask. Simple pocket design that had a lip approximately 0.1 mm wide that prevented the deposition of metal on the side of the SiC chip.

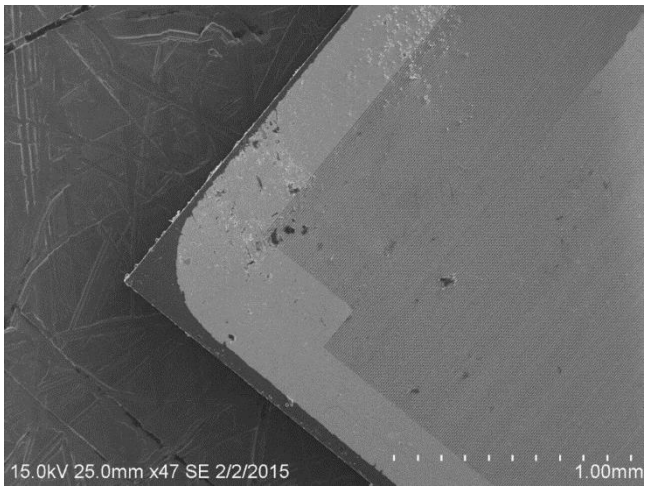

Figure 4-61: SEM image of Ti/Au metal contact layer on etched side. The metals were evaporated using the e-beam evaporator and the device was placed within a shadowmask, to prevent the deposition of metals on the sides.

4.5 Etched 5 mm x 5 mm

One reason for moving away from the 10 mm x 10 mm design to the 5 mm x 5 mm design was to increase the overall yield from less than 25 devices to over 100 devices per 3-inch wafer. During the design of the new photomask, the bonding pad was centered on the top of the trench region. This design change had the inadvertent effect of making it very difficult to determine which side was etched after stripping the etchant mask. During the chemical cleaning process, the SiC chips would move within the holder when being dipped into the chemical solutions or from the agitation from the gas bubbles released by the boiling solution.

It was also decided to make the switch from ITO to aluminum as the etchant mask material. Aluminum has several advantages over ITO. First, it is an elemental material not a compound, so there are no questions about the composition of the deposited material. Also, aluminum is a forgiving material for e-beam evaporation. It is relatively easy to melt and maintain a high deposition rate with minimal sparking. Aluminum evaporation also forms a smooth layer. Whereas ITO undergoes sublimation, never melts, operates at a high chamber pressure, and is prone to sparking at higher deposition rates.

An additional benefit of the smaller size, was less imperfections in the SiC fins after etching. The deposition of the ITO would create many spots where there would either be large chunks of deposited materials or voids. These spots would then become spots where the SiC fins would be over etched. During the contact formation, the Ti/Au contact layer would not be continuous across these areas, leading to potentially inactive regions. With fewer and shorter fins, this impact is reduced.

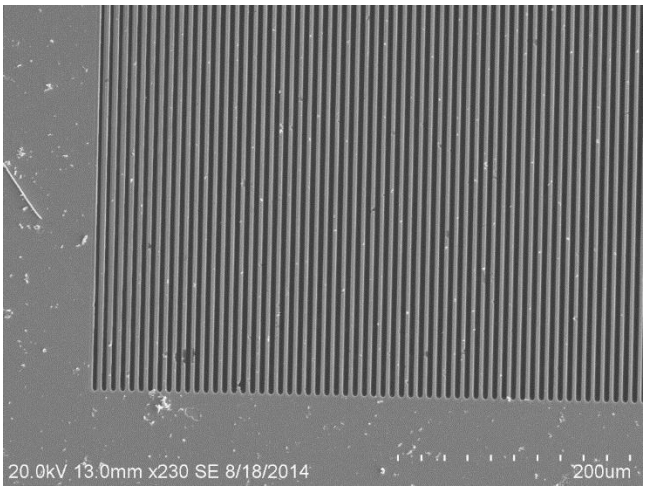

Figure 4-62: SEM image of effects of sputtering during the ITO deposition. Several large chunks of extra material around the trenches. Several spots where the ITO over the SiC fins is partially missing or completely broken.

A test grade SiC wafer was processed with the new 5 mm x 5 mm (8 µm pitch) pattern with aluminum for the etchant mask material. Next the wafer was loaded into the e-beam evaporator and a 1.5 µm thick layer of aluminum was deposited. The resulting etchant mask was much more uniform than the etchant masks formed with ITO, with less gaps present on the fins. For validation on how the aluminum would withstand plasma etching, a strip of partial devices along one wafer edge were diced. Preliminary etching trials were conducted on these partial devices. Note, edge pieces were used because it was possible to dice off one edge for initial trials. While the majority of the wafer would be preserved and could be stripped and reprocessed if needed. The aluminum was observed to be able to withstand the stresses of plasma etching quite well. As a result, the remainder of the wafer was diced for etching.

Multiple etching trial runs were conducted with a variety of process parameters. Various SF_6 etching recipes were tested. The RF power was varied from 100 W to 400 W, the process chamber pressure was typically either 7 mTorr or 40 mTorr. The samples were processed with a high-gas flowrate, with a combined flowrate of 200 sccm of SF_6 and oxygen. From the samples

examined within the SEM, it was identified that when the process chamber pressure was held at 40 mTorr, there was a dramatic increase in the number of microfeatures present within the trenches (Figure 4-63). Also, the deeper etches exhibit narrowing of the trenches near the bottom.

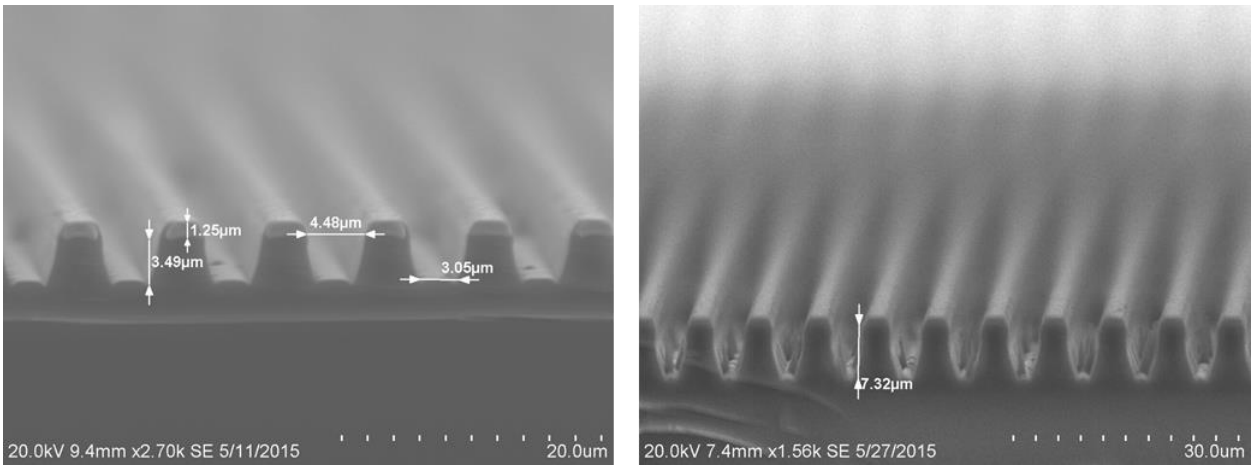

Figure 4-63: Left SEM image is of a low pressure process (7 mTorr). The right image is of a high pressure process (40 mTorr). There appears to be substantially more microfeature formation within the high-pressure process. Also, the trenches narrow substantially near the bottom.

After the trial runs with the test-grade SiC. A device-grade SiC was processed in the same manner with the 5 mm x 5 mm (8 µm pitch) pattern. For the device-grade wafer, the Al etchant mask was about 8 µm thick. After SiC die was etched, it was then loaded into the e-beam evaporator and Ti/Au contact layers were deposited. The first 5 mm devices were backfilled by hand same as the 10 mm devices (Figure 4-64). However, as evidenced by Figure 4-65, for some trench profiles, there are significant portions of trench volume that is not being filled with the boron powder.

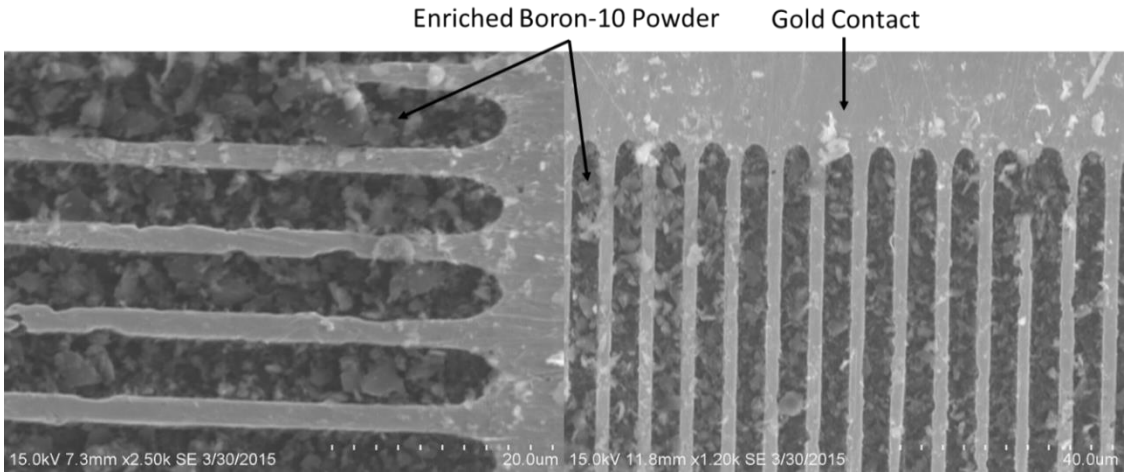

Figure 4-64: Top-down SEM images of an etched device backfilled by hand with enriched ^{10}B metal powder from Eagle Picher.

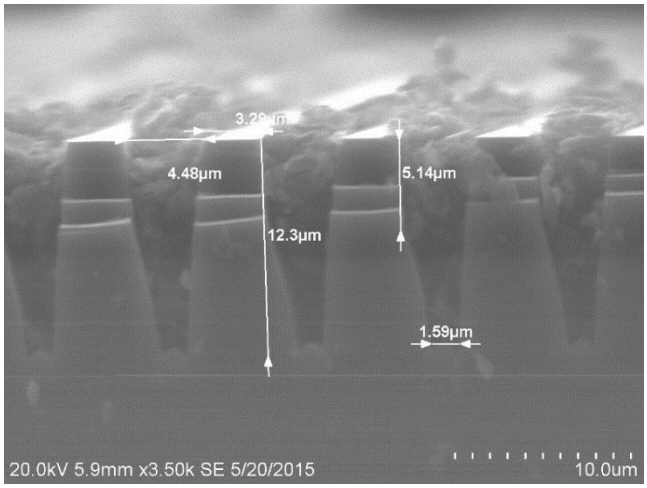

Figure 4-65: SEM image of the cross section of a cleaved device after backfilling by hand. It is obvious that at the bottom of some trenches are voids due to insufficient backfilling. Also, while the trenches have decent depth, ~12um, they are somewhat tapered to the bottom. However, the top of the SiC fins are flat which is key for proper contact deposition.

After manual backfilling, it was attempted to use a centrifuge to force the boron powder into the trenches. The device to be backfilled was placed inside of the holder seen below in Figure 4-66, and then inserted into a centrifuge tube. Separately, a small amount of boron powder was loaded into a second tube and 50 mL of menthol was added. This mixture was then

loaded into an ultrasonic bath for 30 minutes. The purpose of the ultrasonic bath was to disperse the boron powder as evenly as possible and to break up larger clumps. After mixing, the menthol/boron mixture was slowly added to the centrifuge tube as to not dislodge the SiC device. After balancing the centrifuge with additional dummy tubes, the centrifuge was ramped up to 5500 rpm and held at speed for 30 minutes. Once the centrifuge cycle was finished, the excess fluid was slowly poured off and SiC was removed from the holder and placed on a cleanroom cloth. Next, the device was allowed to fully dry (usually left overnight). After drying, the excess boron powder was manually removed from the surface of the SiC device. Then the device was sealed using Humiseal spray. After the Humiseal application, the device was baked at 80 ºC for 1 hour to cure the Humiseal.

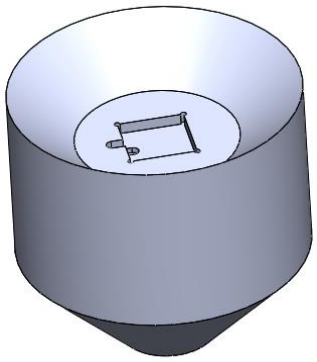

Figure 4-66: Solidworks image of the 3-D printed device holder used for centrifuging boron powder into an etched 5 mm x 5 mm device. Bottom was designed with a cone shape to better match the bottom of the centrifuge tube. The notch was to allow access underneath of the device to safely remove the device from the holder.

After backfilling and coating with Humiseal, the backside contact was cleaned with acetone and isopropanol. Then the device was mounted onto an alumina substrate. The top contact is wire-bonded to the second contact area and then coated with a non-conductive epoxy for protection. The circles within the black epoxy are actually the tops of pins that extended

below the alumina substrate. The pins were adhered to the gold contact areas with conductive silver epoxy. The pins would then be inserted into connectors on the test box. This substrate was only used briefly, as there were issues with the pins breaking loose when being loaded into the test box.

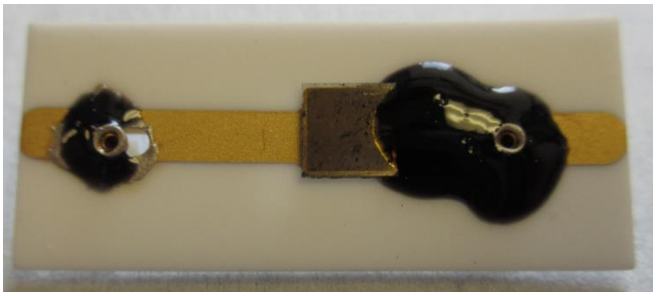

Figure 4-67: 5 mm design SiC detector mounted on alumina substrate. Wire bonds are protected with the black epoxy. A problem associated with this design became apparent after swapping devices a few times, the pins would break free from the epoxy.

Due to the mechanical failures of the connectors, the change was made to a different alumina substrate (Figure 4-68). This substrate had larger holes and it was possible to use bolts to hold the detector in place. For this test box, wire ring terminals were soldered onto the anode and cathode wires. The anode wire was connected to the central conductor on the BNC connector and the cathode wire was connected to the aluminum test box. The bolts that held the device in place also sandwiched the wire ring terminals firmly into the contact pads on the alumina substrate.

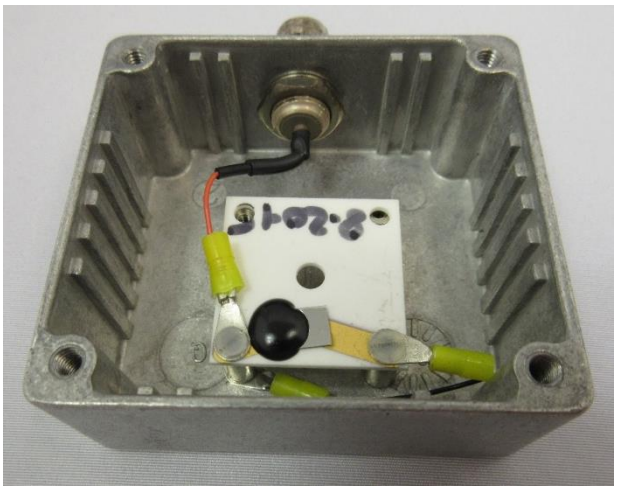

Figure 4-68: Test box configuration, with plastic bolts establishing a pressure contact between the electrical leads and the bonding areas on the alumina substrate.

4.5.1 Metal Contact Layer

After fabricating multiple devices where the top contact was formed after etching, it was decided to fabricate the metal contact layer before depositing the Al etchant mask. As detailed previously, the intention was that the contact would be more uniform across the surface of the device. Using photolithography to pattern the contact would reduce any possible edge effects due to the relative roughness or imperfections that were transferred from the shadowmasks or Kapton tape. Also, the SiC fins would have a much more uniform thickness contact layer when formed via liftoff than the current method of tilting.

The typical contact layers of 300 Å of titanium and 2500 Å of gold were patterned via liftoff process onto the final device-grade SiC wafer using AZ 2070 photoresist (Figure 4-69). Then the etchant photomask was used to pattern the AZ 2070 photoresist prior to the Al deposition. After multiple attempts, a satisfactory photoresist pattern with the proper alignment was made. Next, about 7.5 kÅ of aluminum was deposited (Figure 4-69). Then the wafer was

soaked overnight in Kwik-Strip to remove photoresist and finish the liftoff process (Figure 4-70). It is readily apparent which regions are covered by the etchant mask and also where the underlying metal contact layer is located.

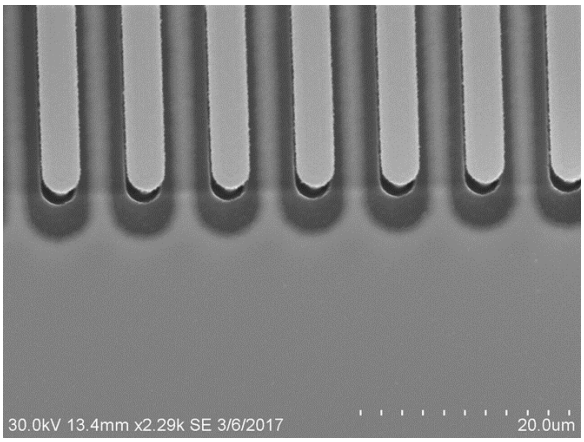

Figure 4-69: SEM image of AZ 2070 photoresist used for liftoff process for the formation aluminum etchant mask. This wafer was coated with 7.5 kÅ of aluminum on top of the selectively etched metal traces/contact areas. Even though the photoresist was biased towards one edge, it was possible to "realign" the etchant window by adjusting how the device was positioned during evaporation.

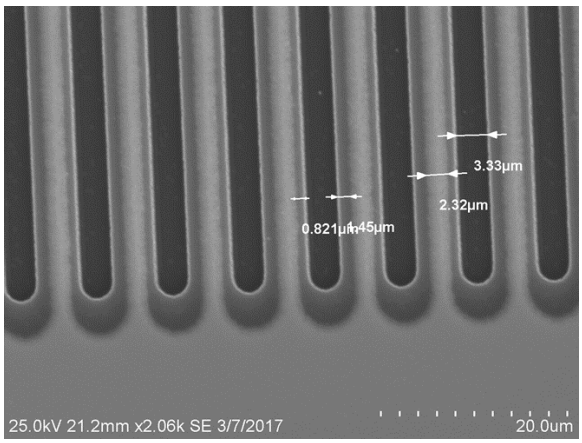

Figure 4-70: SEM image of same wafer after completing liftoff process. The open etching windows for the trenches are visible as the dark regions. The regions where the aluminum etchant mask is covering the Ti/Au contact areas are visible as the light regions. The middle-tone gray where the aluminum is protecting the bare wafer.

After the formation of the contacts and etchant mask, the SiC was diced. During the dicing process, it was observed that both layers had suffered extensive peeling across the majority of the wafer. Approximately, two thirds of the wafer had been diced in one direction (Figure 4-71).

Figure 4-71: One-half of the remaining partial SiC wafer after the Al etchant mask peeled during dicing. The yellow tint is due to the filtered lighting within the cleanroom.

Substantial efforts were put forth into processing the partial wafer. However, due to the non-circular shape, the photoresist would develop a substantial edge beading. The edge bead would be on the order of 3 times the nominal thickness of the AZ 2070 photoresist (20-25 µm thick compared to the typical 7 µm). Since the wafer was patterned via contact exposure, the edge bead would cause a gap to form between the top of the photoresist and the bottom of the photomask. This gap would then distort the transferred pattern. Where the design called for the lines of photoresist for the metal contact layer to be approximately 6 µm wide with a separation of 2 µm, the actual patterned features would be wider, nearly touching with negligible gap

remaining. Also, the exposure time would be insufficient to properly expose photoresist of that thickness, which prevented accurate developing.

It was attempted to spray acetone on the edge of the partial wafer to remove the edge bead. This process worked only partially, as only 3-4 potential devices would have the proper photoresist pattern. Other attempts were made to try dipping each edge of the partial wafer into a shallow dish of acetone to remove the edge bead. Both methods had a tendency of creating a new edge bead. They would also unevenly remove the photoresist which would again prevent uniform contact between the photomask and the photoresist resulting in a distorted pattern.

While efforts were made to process the partial pieces of the SiC wafer, planar devices were fabricated from the diced portions of the device-grade SiC wafer. The goal was to have a more reliable test box configuration for when new etched devices could be fabricated. The new holder for the 5 mm x 5 mm devices, is shown in Figure 4-72. These holders were leftovers from a different project and had both contact pads on the bottom of the holder. The SiC device was epoxied to the bottom plane using conductive silver epoxy. The topside was wirebonded to the ledge at the top of the holder.

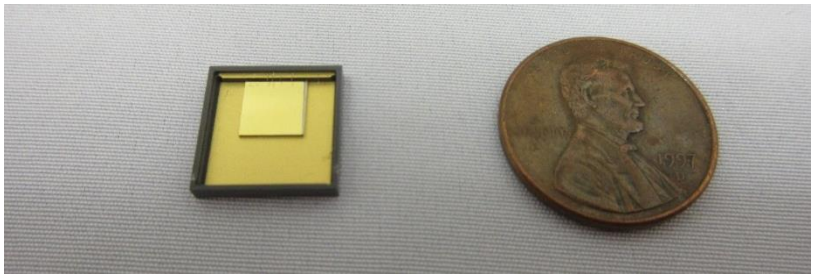

Figure 4-72: Final planar mounting design in attempt to make a more reliable test box configuration.

The new test box configuration for test devices mounted on the new holder, is shown in Figure 4-73. The contact pads on the backside of the holder was placed on top of a modified two pin connector and held in place with an additional piece of aluminum. A large piece of aluminum was used to prevent the devices from shifting during handling.

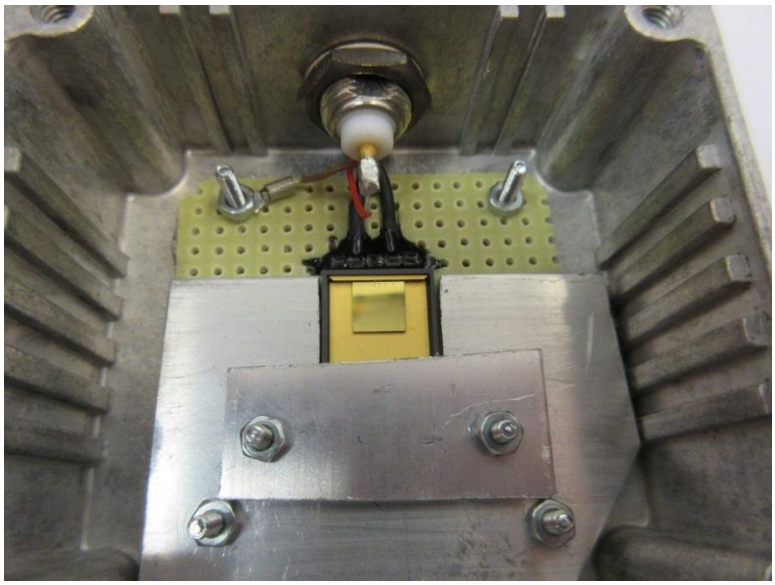

Figure 4-73: Final test box configuration, where the device terminals on the back of the device mount are pressed into electrical leads from the BNC connector.

A planar device used during alpha particle source testing, is shown in Figure 4-74. Also shown is a 3D printed collimator with a centrally-positioned, 2 mm aperture. The aperture size

was intentionally designed small to reduce the overall count rate and therefore reduce the amount of charge trapping and peak shift during a measurement.

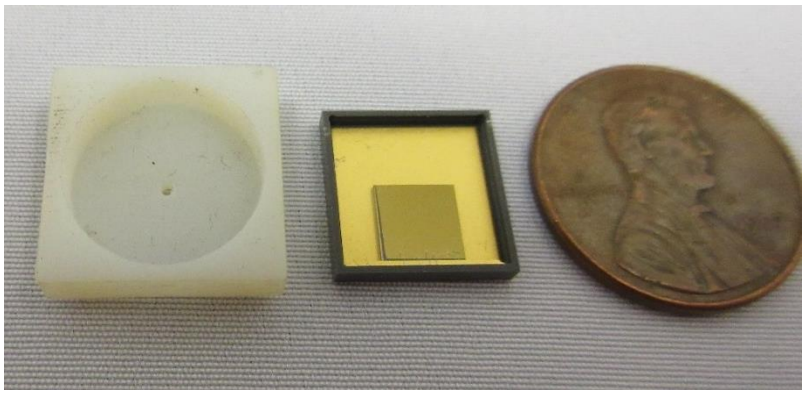

Figure 4-74: Planar detector along with a 3-D printed collimator used for alpha particle sensitivity testing.

Chapter 5 - Analysis

This chapter will detail the device characterization including leakage current and capacitance. It will also cover the analysis and testing conducted for alpha particle testing, gamma-ray testing, and neutron testing. As discussed previously, neutron testing was conducted with both ^{252}Cf and the KSU TRIGA Reactor. Also device charge polarization during irradiation is also covered within this chapter.

5.1 Planar 10 mm x 10 mm

After the detectors were mounted onto DDBs, they were loaded into the custom-built test box (Figure 5-1). This test box was used to conduct leakage current and capacitance testing as well as neutron or gamma testing. The box was simple in construction. The DDB holder was 3D printed. Spring pins were mounted in the bottom of the holder. Three spring pins pressed against the back plane of the DDB. One pin made contact with the DDB through-connection to the wirebond pad to the topside contact. The topside pin was connected to the anode of the BNC connector. One backside pin was connected to the cathode side of the BNC connector. There was also an electrical connection between the BNC connector and the metal case.

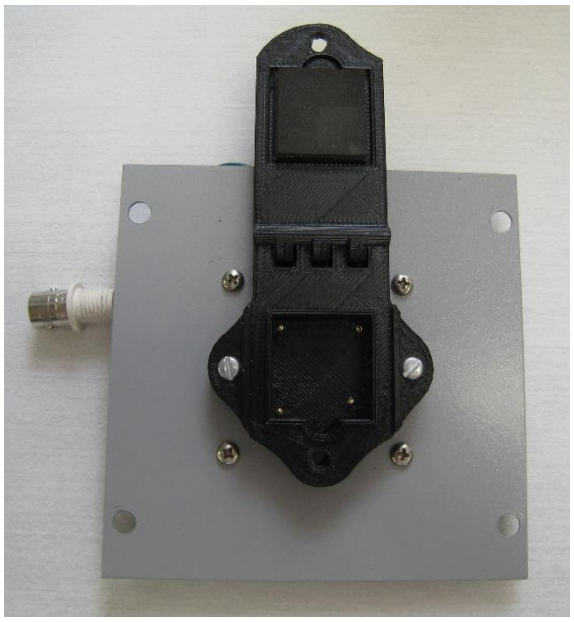

Figure 5-1: DDB test box custom built to test a SiC device mounted onto a DDB, the holder is made by 3D printing. Spring pins make electrical connection to the DDB. A preamplifier is connected via a BNC connector.

For the SiC devices, the leakage current was tested with a probe station attached to a Keithley 237. The Keithley was controlled via a computer. The system applied a voltage across the device and measured the resulting current. Typical test parameters were 100 V to -100 V with 0.5 V step. A representative resultant I-Vcurve is shown in Figure 5-2. The leakage current is very linear with respect to the applied bias. The maximum current seen was on the order of 10 nA at ±100 V.

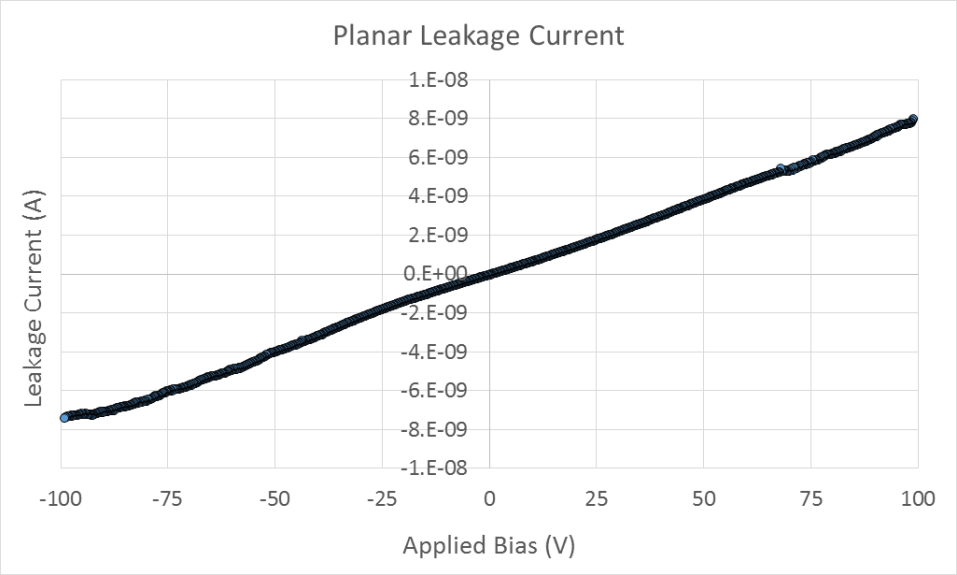

Figure 5-2: Leakage current of a 10 mm x 10 mm planar device. The, device exhibits linear, highly-resistive ohmic behavior. Max leakage current is less than 10 nA at 100 V.

The capacitance testing was conducted using a Hewlett Packard 4280A, controlled by the laboratory computer. As the DC voltage sweep is applied across the device, the impedance of the device is measured as an AC voltage is applied. For the testing presented here, the AC voltage was operated at 1 MHz and the DC bias was stepped from 0 V to 10 V. This setup may be represented as a simple RC circuit (Figure 5-3), where R is the resistance of the material and C is capacitance. The impedance, *Z*, of the RC circuit is shown in Eq. 5.1, where, ω is the frequency of the applied voltage, and *j* is the imaginary unit. When *R* becomes very large, the $j\omega RC$ term dominates the denominator, allowing for the *R* terms to cancel, reducing to Eq. 5.2. The result of $j\omega C$ for the impedance indicates that there is no change in capacitance during the DC voltage sweep. This agrees with the behavior of the linear C-V measurements (see Figure 5-25).

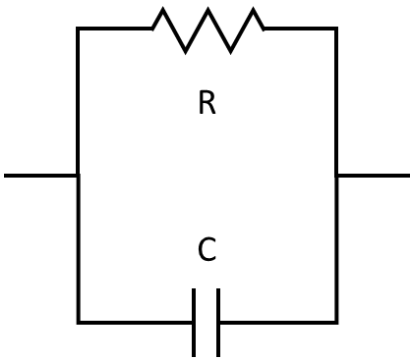

Figure 5-3: Simple RC circuit that represents the capacitance-voltage (C-V) measurement.

$$Z = \frac{R}{1+j\omega RC} \quad \text{Eq. 5.1}$$

$$Z = \frac{R}{j\omega RC} \rightarrow \frac{1}{j\omega C} \quad \text{Eq. 5.2}$$

For the 10 mm planar devices, the capacitance was approximately 25 pF. These measured capacitance values were used to aid in preamplifier selection. The measured values can be verified by taking the basic equation for parallel plate capacitance, where the area is ~100 mm, the thickness is 365 μm, and ε_{SiC} (permittivity of silicon carbide) is about 9.6. The ε_0 (permittivity of free space) is 8.854187 F/m. It can be shown by applying the values into Eq. 5.3, that the experimentally measured capacitance is comparable to the parallel plate capacitance using the total thickness of the substrate.

$$C = \frac{\varepsilon_0 \varepsilon_{SiC} \cdot Area}{t} \quad \text{Eq. 5.3}$$

Since there were concerns that the 3D printed plastic would cause neutron scattering in the thermal beam, the DDBs were mounted onto printed circuit boards (Domino boards) see Figure 5-4. The printed circuit boards (PCBs) used were Domino electronics board, unused from ongoing silicon-based MSNDs projects. The Dominos were designed for use with 2 cm x 2 cm devices. A connector was mounted at the bottom of the Domino that supplied signal, ground, and power. A new test box (Figure 5-5) was assembled that connected the new SiC Domino device to the Ortec 142A Preamp. Next the signals were processed by a Canberra 2022 amplifier. Typical amplifier settings were 300x coarse gain and 1.0x fine gain, while the pulse shaping time was set at 2 μs. The amplified signal was then passed to an oscilloscope and/or a computer running Maestro MCA. High voltage was provided by an Ortec 556 High Voltage Power Supply, the actual applied voltage was verified using a digital multimeter.

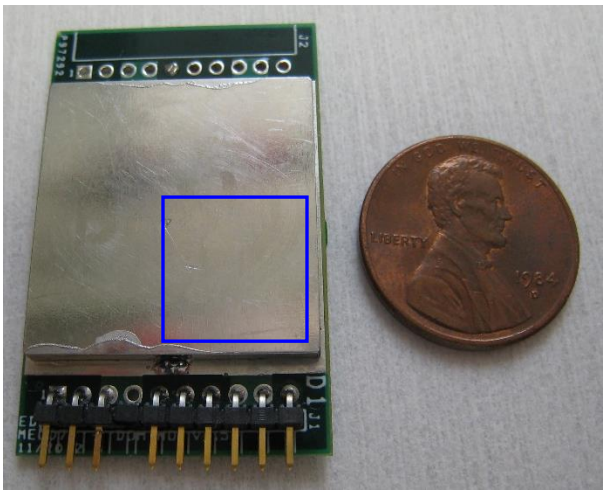

Figure 5-4: A 10 mm x 10 mm detector mounted onto a Domino PCB. The blue square outlines the detector's location.

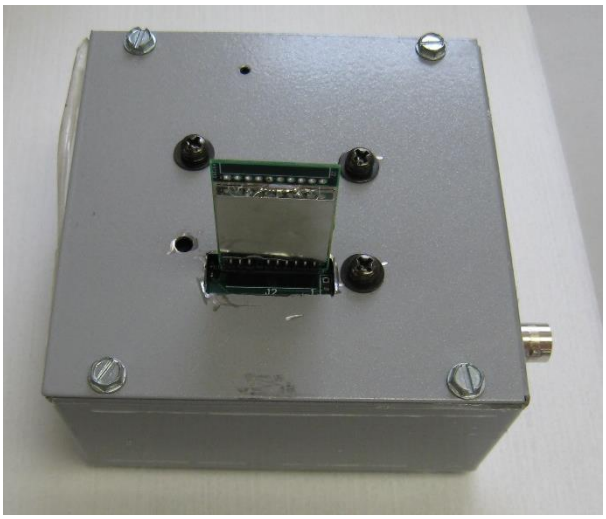

Figure 5-5: SiC device and test box. BNC connector for signal and power is visible on the right. It was possible to conduct I-Vand C-V measurements as well as neutron sensitivity testing using this test box.

The operational range of the detectors was determined by conducting 20 minute measurements starting at 20 V applied bias and increasing 10 V for each successive measurement. If excessive spurious counts were observed, the measurement was immediately stopped and the voltage was reduced to safe levels. Then, an ^{241}Am source was positioned above the detectors and the measurements were conducted again for each applied bias.

The new SiC Domino was subjected to various test configurations: First, the SiC detector was positioned inside of a vacuum chamber with a ^{252}Cf source located outside. Then twenty minute measurements both with the source and without the source were taken with the vacuum chamber at atmospheric pressure. After the atmospheric tests were completed, the chamber was evacuated to ~ 40 mTorr. This test was accomplished using a liquid nitrogen sorption pump to reduce spurious noise signals from mechanical vibrations. Then both source and no-source measurements were retaken. Finally, the chamber was vented to atmospheric

pressure and both measurements were repeated. The results of the ^{252}Cf measurements are shown in Figure 5-6. Also, one measurement with no source is included.

It is apparent that the presence of air or vacuum did not have any appreciable effect on the resultant spectrum and that the spectrum did not change when the chamber was vented. The second purpose of this experiment was to prove that the recorded signals were due to neutrons interacting with the neutron conversion material and the resultant charged particles entering the detector volume and inducing a signal. This test demonstrated that the signals were not being generated by charging of the surrounding air.

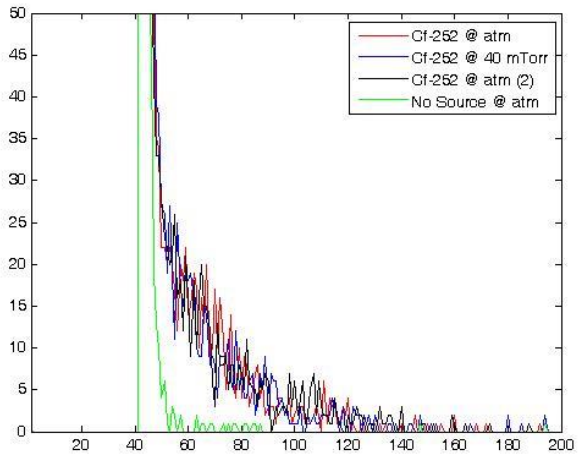

Figure 5-6: Measurements taken at atmospheric pressure and at vacuum with the ^{252}Cf source. Each measurement was 20 minutes in duration. Definite change in detector behavior when comparing source versus no source measurements.

A longer measurement of 10 hours (Figure 5-7) was taken with the detector located within the vacuum chamber at atmospheric pressure and the ^{252}Cf source located outside of the chamber. The 10 hour spectrum shows similar response as the 20 minute spectrum. The data shown in Figure 5-8 is the same data as shown in Figure 5-7 but with a different scaling applied

to the Y-axis. Again, there is a significant difference in detector behavior when comparing source and no-source.

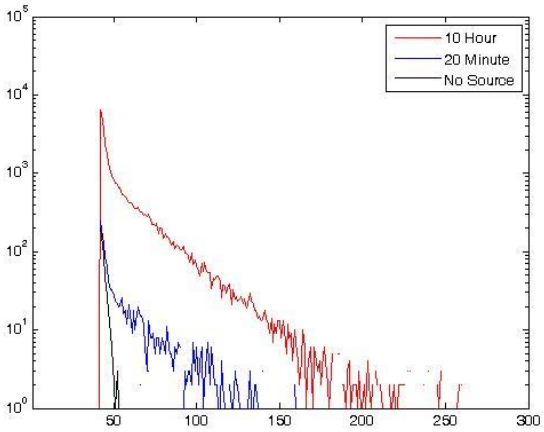

Figure 5-7: Measurements with the ^{252}Cf source while the detector located within the vacuum chamber. Measurement durations were 20 minutes (blue) and 10 hours (red). No source measurement was for 20 minutes (black).

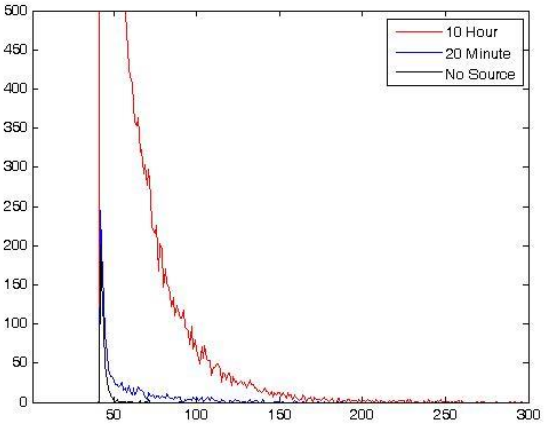

Figure 5-8: Measurements with the ^{252}Cf source with the detector located within a vacuum chamber. Measurement durations were 20 minutes (blue) and 10 hours (red). No source measurement was for 20 minutes (black).

With the new test box configuration, it was possible to put only the SiC detector and the Domino board into the thermal neutron diffracted beam port at the K-State TRIGA Reactor. Preliminary test results are shown in Figure 5-9, where the "No Shutter" red line is the spectrum taken as the detector is placed within the neutron beam and the "Cd Shutter" blue line is the detector response when a 3 mm-thick cadmium shutter was placed in front of the detector. The measurement duration for each was 3 minutes. This measurement demonstrates that the SiC detector is responding to incident neutrons.

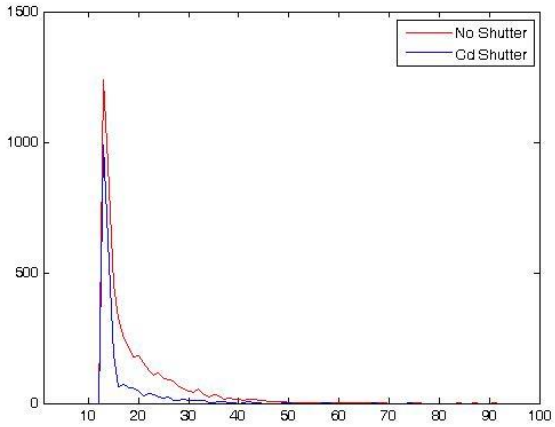

Figure 5-9: Measurements at the thermal neutron diffracted beam port. The red data line is the neutron beam response. The blue line is the detector response when the cadmium shutter is closed. The test duration was 3 minutes. This measurement demonstrates that the SiC detector is responding to incident neutrons.

Gamma response measurements were conducted using a ^{22}Na gamma-ray source. As shown in Figure 5-10, the resultant spectrum with the gamma-ray source is very similar to the No Source response spectrum. The spectrum with the ^{252}Cf source had a definite increase in counts. This result is further indication that the SiC detector signal responses are due to incident neutrons interacting with the neutron conversion material.

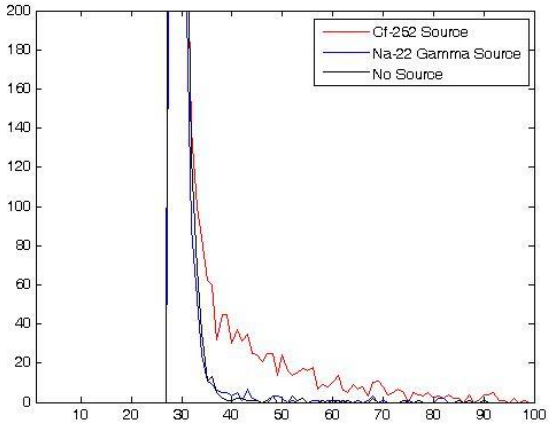

Figure 5-10: Detector response for a ^{22}Na gamma source, the ^{252}Cf source, and with no source present. Each measurement was 5 minutes in length.

5.2 Etched 10 mm x 10 mm

The etched 10 mm x 10mm devices were tested for its I-V and C-V characteristics. The devices exhibited a leakage current of approximately 10 nA at 100 V applied bias. The capacitance of the devices was measured to be 25 pF to 35 pF. While the detector was in the probe station, a ^{241}Am source was positioned above the detector and a 900 second measurement was conducted. The resultant spectrum is shown in Figure 5-11. There is a clear separation between the alpha peak and the noise region.

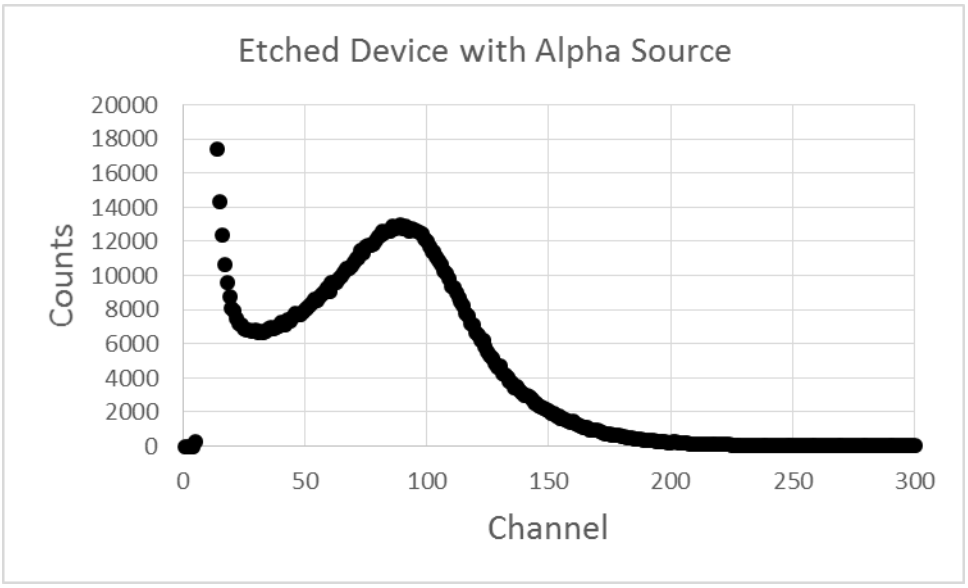

Figure 5-11: Alpha particle spectrum with a 10 mm x 10 mm etched device. The duration of the measurement was 900 seconds. This measurement was taken before the etched device was backfilled.

Using the custom test box constructed by Electronics Design Laboratory (EDL) at Kansas State University, the backfilled SiC device was connected to an Ortec 142A pre-amp and then to an Ortec 672 amplifier. The amplified output was then displayed on an oscilloscope. A 1 inch thick piece of HDPE was placed directly on top of the detector housing to provide some moderation and a ^{252}Cf source was placed directly on top of the HDPE. The signals were sent to an oscilloscope and the trigger level was adjusted upwards until only large amplitude pulse events were displayed. The oscilloscope display was changed to infinite persistence, so all pulses were kept. The results after approximately 45 minutes of steady operation are shown in (Figure 5-12). A small sample of recorded signals to better see pulses is shown in Figure 5-13. The brown lines and blue area are from the histogram feature (blue lines on the left) and have no effect on the pulses.

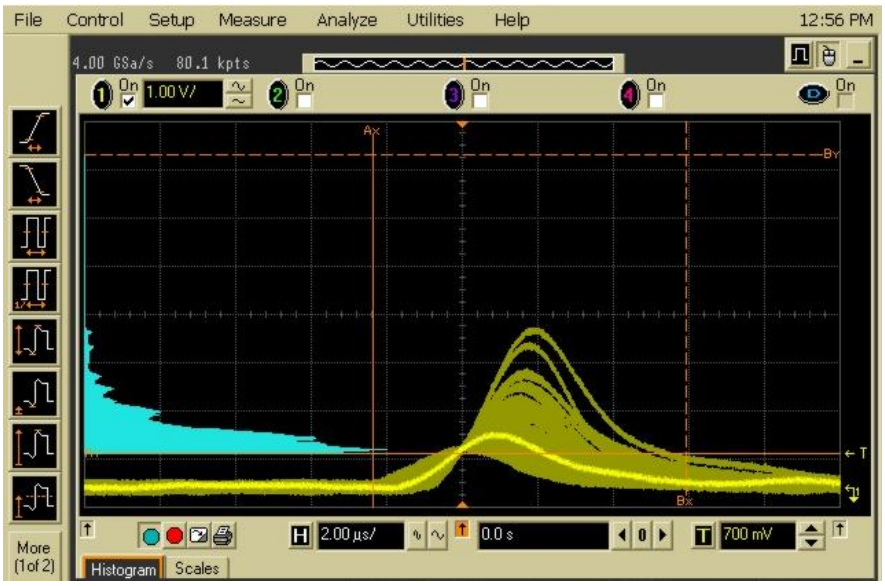

Figure 5-12: Sum of all pulses above the trigger level, after approximately 45 minutes of operation. The blue area is from the histogram feature of the oscilloscope where the x-axis is total number within a bin and the y-axis is the amplitude of the pulses.

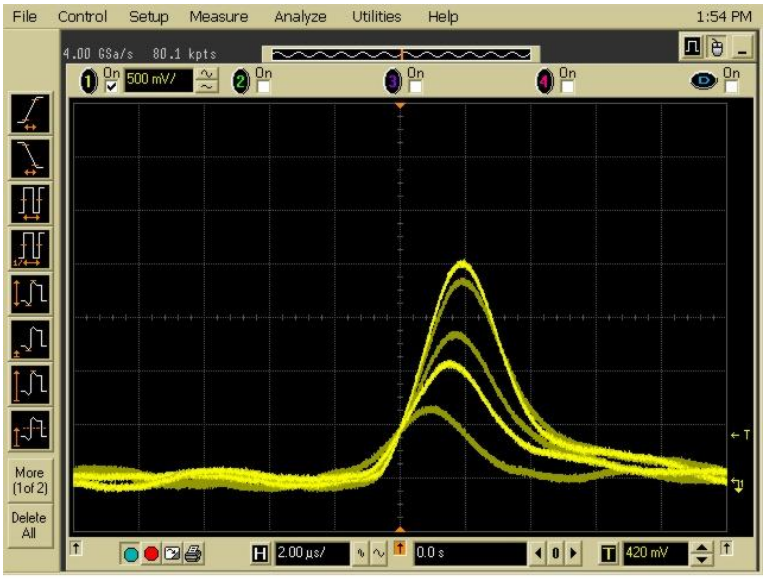

Figure 5-13: Small sample of pulse heights during an approximately 2 minute measurement. The x-axis is time (2 µsec per division) and the y-axis is amplitude (500 mV per division).

To show that the observed events are not noise related, the ^{252}Cf source was removed and an additional 45 minute measurement was conducted (Figure 5-14). After the measurement was completed, the trigger level was lowered into the noise region to demonstrate that the detector was still operating.

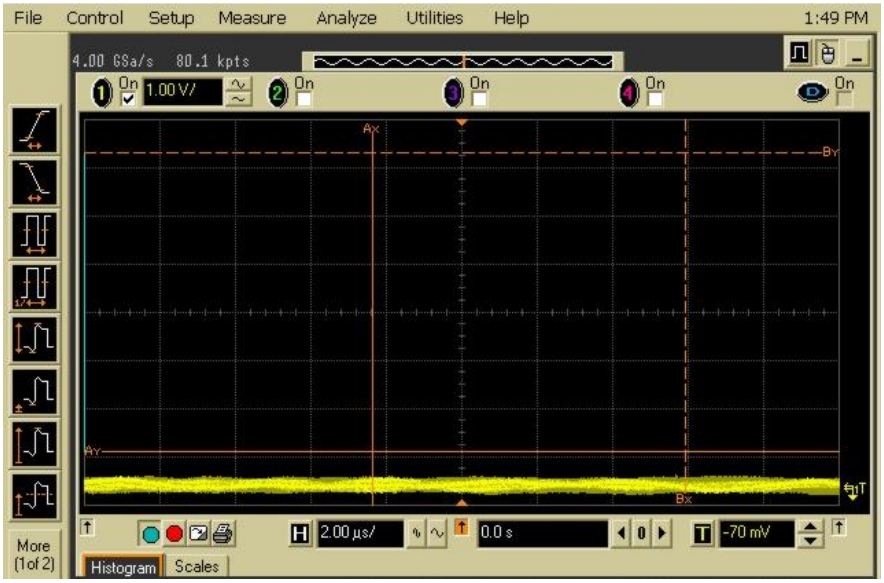

Figure 5-14: Measurement conducted with ^{252}Cf source removed. At the completion of the measurement, the trigger level was lowered into the noise region to indicate detector was operational. The x-axis is time (2 µsec per division) and the y-axis is amplitude (1 V per division).

5.2.1 Device Charge Polarization

Next a planar detector was tested with alpha particles using a ^{241}Am source. The source was suspended about 2 mm above the top of the detector. Each measurement was taken with minimal delay and lasted for 60 seconds each (Figure 5-15). It was observed that as the detector was left under bias and continuously irradiated, the alpha peak would shift to progressively lower

channels. The peak would shift back to higher channels if the alpha source was removed for an appreciable amount of time.

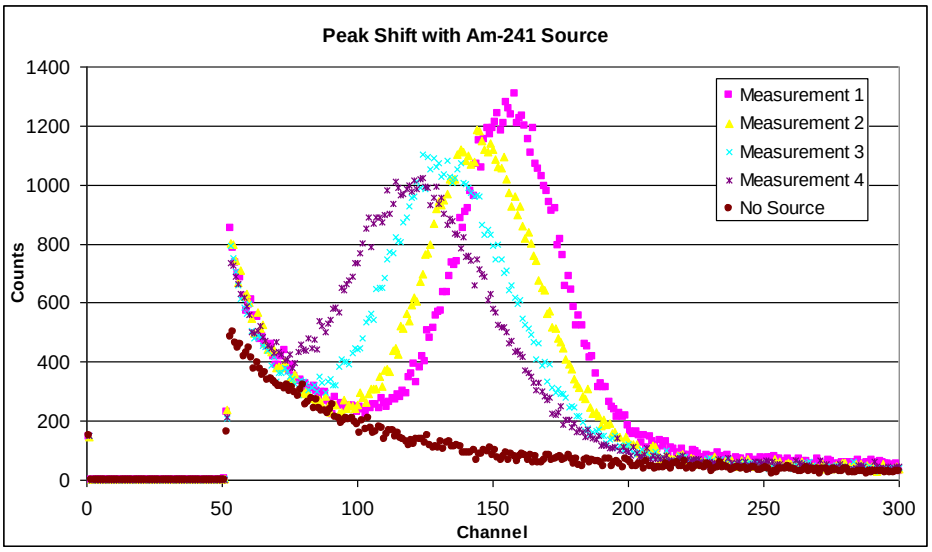

Figure 5-15: Each measurement was conducted for 60 sec and was taken consecutively where Measurement 1 was first and Measurement 4 was last. The peak continually shifts to lower channels. When taking additional measurements, the peak would continue shifting left until it was indistinguishable from noise.

It is surmised that a couple of mechanisms may be responsible for the peak shift. The most likely mechanism was an increase in leakage current during the testing. Internal to the preamplifier, the bias voltage is passed through a large load resistor and then applied to the detector. The increase in leakage current will the bias voltage potential across the load resistor resulting in a lower applied bias voltage to the detector. A decrease in the applied voltage bias would result in a corresponding decrease in pulse height, which would shift the spectral peak to the left. Another possible mechanism is the charge trapping or charge polarization that may have occurred either within the bulk silicon carbide material or at the contact-silicon carbide interface. In the literature, there is considerable mention of charge trapping occurring within high-purity semi-insulating 4H silicon carbide bulk material. As discussed previously, the primary methods

of creating SiC with semi-insulating properties is either doping with vanadium or the formation of deep level traps. It was observed that it was possible to "clear" or reset the trapped space charge by removing the applied bias for a few minutes. Alternatively, it was possible to expose the detector arrangement to direct light, which would temporarily cause a dramatic increase in noise (full scale amplitude on oscilloscope). Once the light was removed and the system returned to stable operation, the peak would shift again to the higher energy channels. Lastly, the source could be removed.

5.2.2 Boron Deposition

Enriched boron was evaporated onto a 10 mm x 10 mm etched device. The device was tested for alpha particle sensitivity before and after boron deposition. No appreciable change in performance was noticed. Next the device was mounted onto an alumina substrate (Figure 5-16) and prepared for neutron testing with the 48 ng ^{252}Cf source.

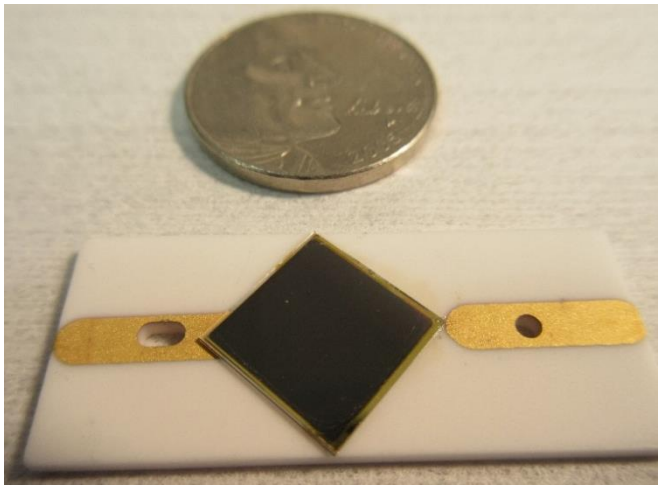

Figure 5-16: Picture of the mounted (10 mm x 10 mm) microstructured SiC detector on the alumina substrate with deposited gold contact pads for electrical connections. Nickel included for scale.

The detector on the new substrate was mounted in the new test box (Figure 5-17) and was secured using flexible metal clips that doubled as the electrical connections. The blue connector is the device ground and is also connected to the box enclosure. The red connector is the applied bias. The printed circuit board provides an electrically-insulating, mounting platform. Both wires are connected to a basic BNC connector, which was connected to a standard preamplifier. The lower level discriminator (LLD) on the MAESTRO software was tuned so that the program reported deadtime of less than 3%. The applied voltage was approximately 50V as measured by a digital multimeter across the blue and red connectors shown in Figure 5-17.

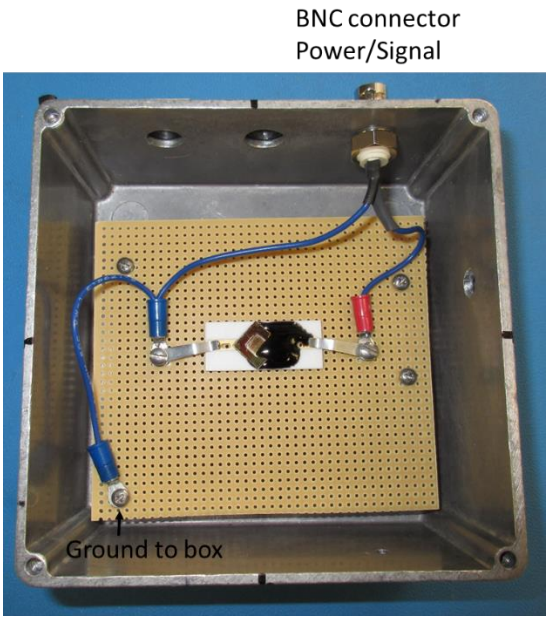

Figure 5-17: Test box design for device testing. The blue connector is the device ground and is connected to the enclosing box. The red connector is the applied bias. The actual electrical connections are made by a pair of flexible metal clips that could be loosened/tightened as needed. The blank printed circuit board is used as the mounting platform.

Measurements were conducted with no source present and then the 48 ng ^{252}Cf was positioned on top of the test box lid directly above the detector. Each measurement had a duration of two minutes. The resultant spectra are shown in Figure 5-18. It is clearly evident that the detector's response behavior changed when irradiated with the ^{252}Cf source. There are significant number of events with energy above the noise channels.

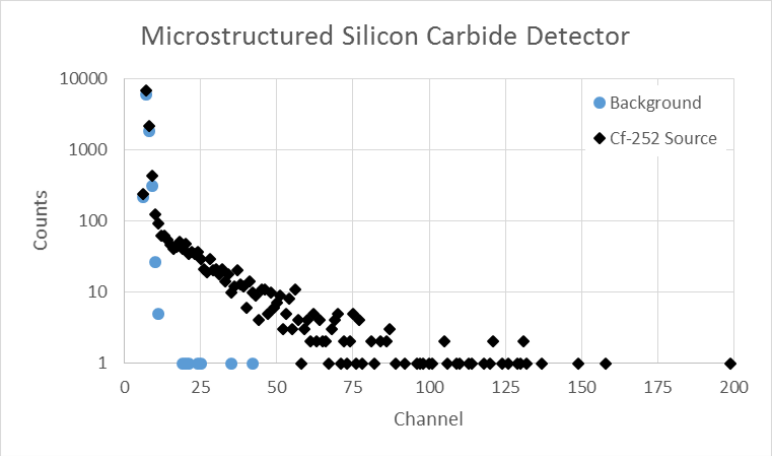

Figure 5-18: Depicts detector response spectrum when exposed to the 48 ng ^{252}Cf source versus background spectrum. Each measurement duration was 2 minutes. Spectrum is from the etched device with ^{10}B layer deposited within the e-beam evaporator.

It was observed that as the device was left under bias (more than 30 minutes), the upper edge of the noise region would steadily shift to higher channel numbers. If the bias was temporarily turned off and on, the noise regions would shift back to lower channel numbers. The downshift would typically move the noise region to the same general operating channel numbers as other measurements. But, again if the device was allowed to dwell under bias, the noise region would once again increase.

It was theorized that the evaporated boron material was providing an alternate conduction path for the applied bias. In other words, instead of relying upon the highly resistive silicon carbide to maintain bias, the bias was actually generating a current through the boron coating instead of the silicon carbide fins (Figure 5-19). Boron actually has a lower resistivity of approximately 10^5 Ωcm versus the 10^9 Ωcm of semi-insulating silicon carbide. So the alternate conduction path and the presence of additional surface trapping between the boron and etched silicon carbide was surmised to be responsible for increasing the amplitude of the noise.

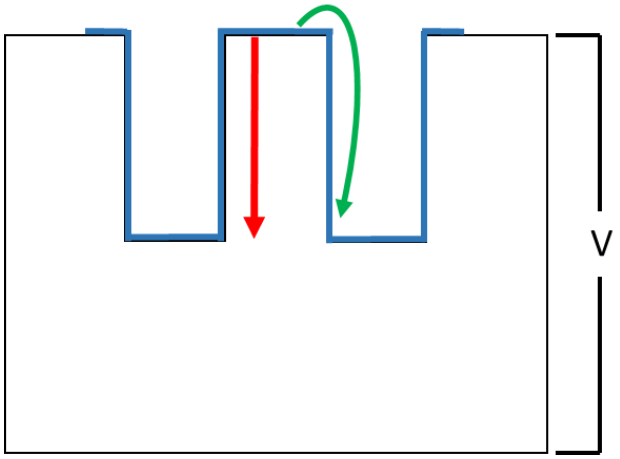

Figure 5-19: Sketch of the boron-coated device and the theorized current path (green arrow) versus the desired current path (red arrow). The blue is the deposited boron coating.

To counteract the increase in noise amplitude behavior, two high-resistivity devices were etched and Ti/Au contacts were evaporated on both sides. Then, approximately 300 Å of silicon dioxide (SiO_2) was sputtered onto the device top. Silicon dioxide was chosen because it is an insulator and the sputtering target was available within the laboratory. The purpose of the SiO_2 was to act as an electrically insulating layer between the gold contact and the evaporated boron material. The benefit of using the sputtering system (Figure 5-20), is that sputtering is an isotropic process. This process trait allowed for more complete coverage in the trenches and on the fins. For testing purposes, the bonding pad area was masked with Kapton tape to prevent any potential interference with the test probe connection. The SEM imaging of an etched test-grade SiC chip that was used as a test run to determine the feasibility of sputtering SiO_2 onto the etched SiC devices is shown in Figure 5-21. It is readily apparent that the sputtering system achieved relatively uniform coverage of the top surfaces. Although it is fairly hard to determine the quality of the coverage within the trenches.

Figure 5-20: Sputtering system, used for the deposition of metals such as titanium or gold and other materials including indium tin oxide (ITO), silicon dioxide, and boron [32].

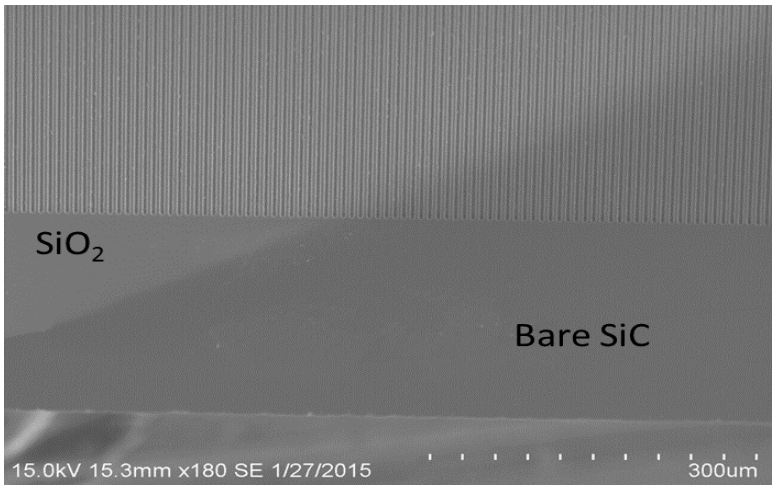

Figure 5-21: SEM image of the boundary line of the device area covered with sputtered SiO_2 and the bare SiC on a test device. The bare region on the right was intentionally masked with Kapton tape to cover the bond pad, as well as provide a boundary region for inspection.

The devices were tested for alpha sensitivity, leakage current, and capacitance both before and after the formation of the SiO_2 layers to monitor any changes in device performance. No appreciable changes were observed. After the evaluation tests were

completed, the devices were reloaded into the sputtering system this time with the purpose of coating the devices using an enriched ^{10}B sputtering target. As seen in Figure 5-22, the center 6 mm x 6 mm region of the device area was coated with the enriched boron material. As stated before, it is possible to see the actual boundary between the trenches that have been coated with SiO_2 and the regions that were shadow masked during the sputtering. The approximate thickness of the sputtered boron layer is 0.5 µm. As per usual, the SiC device was mounted upon an alumina substrate with silver epoxy and the top contact was wirebonded and epoxied (Figure 5-23). The detector had a capacitance of about 30 pF.

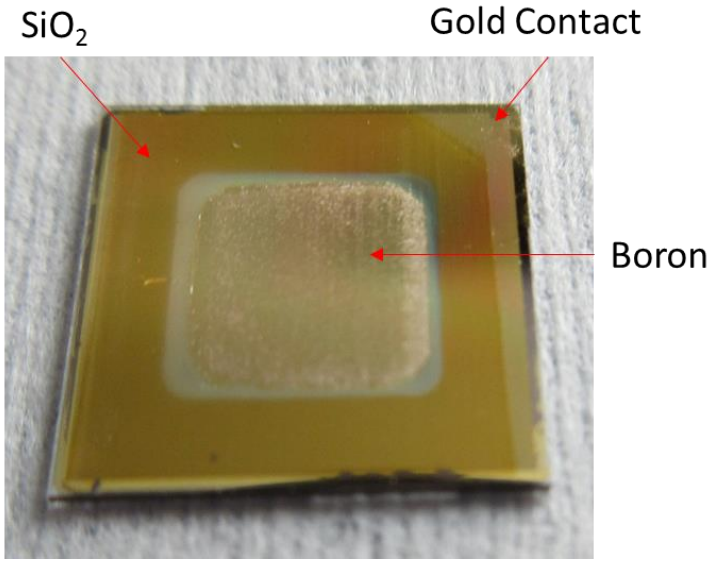

Figure 5-22: Photograph of an etched silicon carbide device that was coated with SiO_2 over the majority of the device area via sputtering. Then the center region (approximately 6 mm x 6 mm) was coated with enriched ^{10}B via sputtering. The mask used for the ^{10}B coating allowed for substantial undercoating, hence the halo effect around the boron.

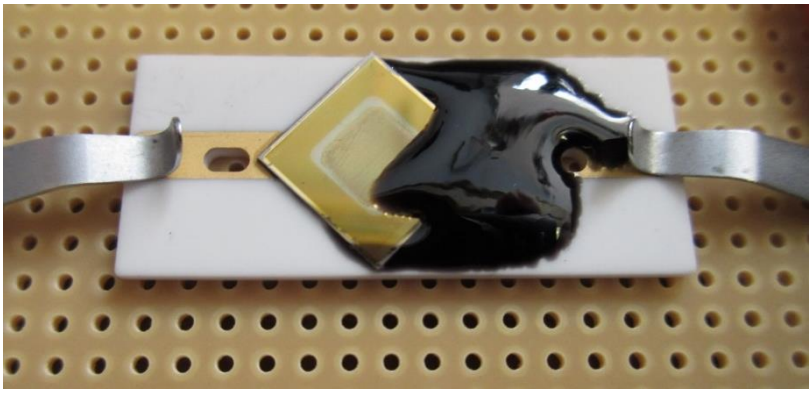

Figure 5-23: Photo of the SiC device after being mounted, wirebonded, and epoxied onto an alumina substrate for testing.

Next, the device was left under continuous bias for approximately 60 hours while conducting 10 hour long measurements with and without the ^{252}Cf source. There was no evidence of charging or shifting of the noise channels. The results from a background measurement and a ^{252}Cf measurement are presented in Figure 5-24. It is obvious that the detector experienced a marked increase in signals above the noise region when the neutron source was present.

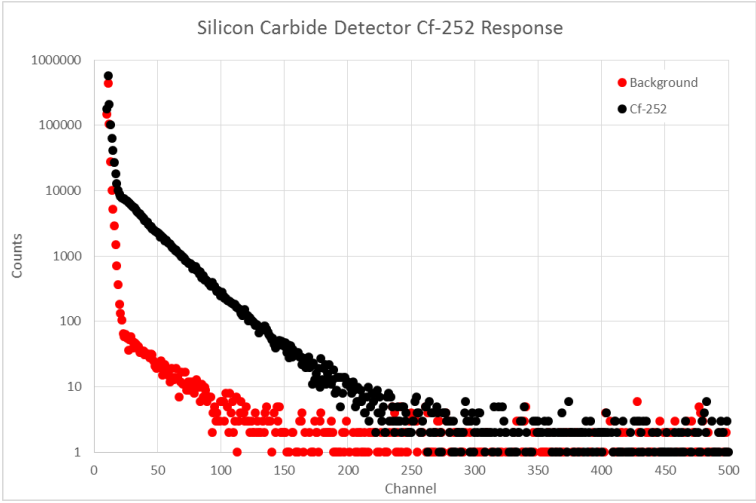

Figure 5-24: Plot of the detector responses over 10 hour measurements with and without the 48ng ^{252}Cf source.

This testing was accomplished using the same test setup seen above in Figure 5-17 and the test box would perform admirably while on the test bench with very low system noise. However, while attempting to conduct thermal neutron testing at the diffracted beam port within the reactor bay, the system became very noisy due to outside interferences. Therefore, it was not possible to acquire good thermal neutron detection data during this testing. It was decided more work was needed to change the test configuration to reduce the system susceptibility to outside interference and system noise.

5.3 Etched 5 mm x 5 mm

The etched 5 mm x 5 mm devices were tested for its I-V and C-V characteristics before and after backfilling and again with mounting. The I-V characteristics remained consistent. However, the device capacitance did change from approximately 5 pF to approximately 12 pF after mounting (Figure 5-25). The former capacitance value is of just the SiC device, the latter value is the combined capacitance of the SiC device and the substrate it is mounted upon. This capacitance value was useful when selecting testing components such as the preamplifier.

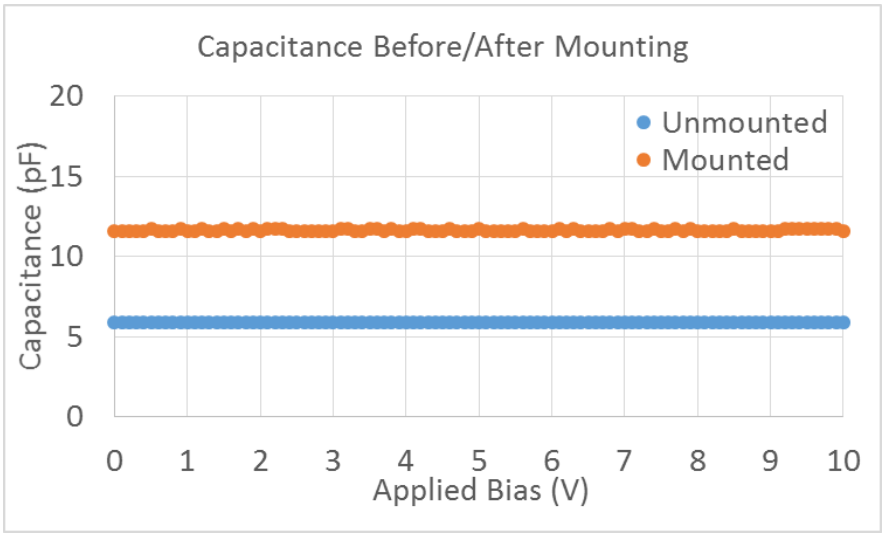

Figure 5-25: Capacitance of a SiC device before and after mounted onto the substrate for sensitivity testing. The capacitance changed from ~ 5 pF to ~12 pF.

The 5-8 pF capacitance for a 5 mm device directly compares to the 10 mm x 10 mm device capacitances of around 25-35 pF. The maximum leakage currents were around 50 pA when the applied voltage was ranged from 100 V to -100 V (Figure 5-26).

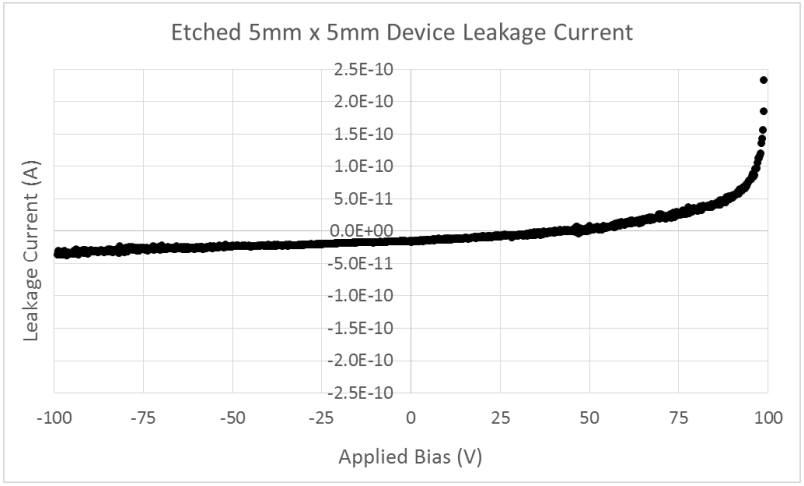

Figure 5-26: Leakage current for an etched 5 mm device. Device exhibits the expected linear characteristics with a leakage current of less than 50 pA at -100 V applied bias. Power was stepped from 100 V to -100 V.

The steep, upwards curve on the right-hand side of Figure 5-26 is shown in log-log scale in Figure 5-27. When plotted in log scale, the curve becomes nearly vertical, this behavior is characteristic of the traps-filled-limit voltage, V_{TFL} [53]. If the voltage was increased, the value for the current would approach Child's Law, where the current is proportional to the square of the voltage.

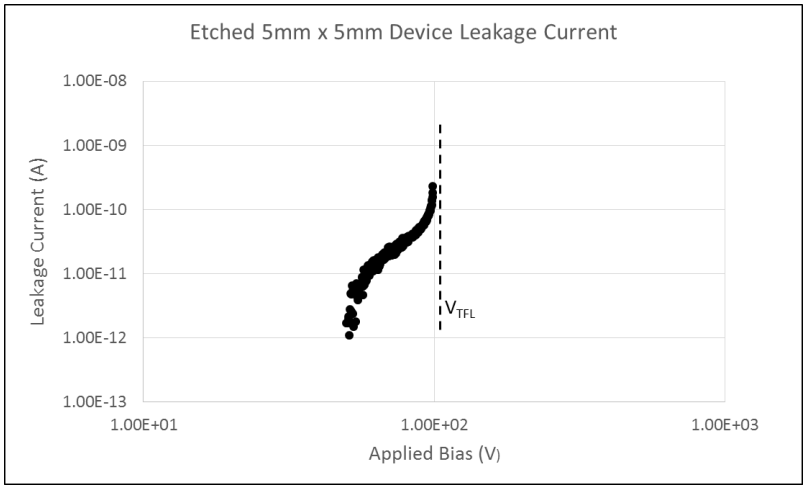

Figure 5-27: Log-log plot of the leakage current of the data from 50 V to 100 V (Figure 5-26). The upwards curve, which appears as a nearly vertical line on the log-log plot, is characteristic behavior of traps-filled-limit voltage or V_{TFL}.

Neutron response testing was conducted using both a ^{252}Cf source and the diffracted neutron beamport at the Kansas State University TRIGA Reactor. For the ^{252}Cf testing, the detector was loaded into a metal project box. The induced signals were collected by an Ortec 142A preamplifier and then processed by a Canberra 2022 amplifier. Typical amplifier settings were 1.0x fine gain and 300x coarse gain, while the pulse shaping time was set at 4 μs. The amplified signals were passed to an oscilloscope for visual inspection as well as a computer running Maestro MCA for data recording. An Ortec 556 High Voltage Power Supply High provided the applied bias. A 1 inch thick sheet of high-density polyethylene was placed on top

of the detector enclosure. Then the 48 ng ^{252}Cf source was positioned directly above the detector. The results from 6 hour measurements with the source and without the source are shown in Figure 5-28. No settings were changed between the measurements. There is an obvious difference in the recorded counts in the channels above the noise region for the resulting spectra.

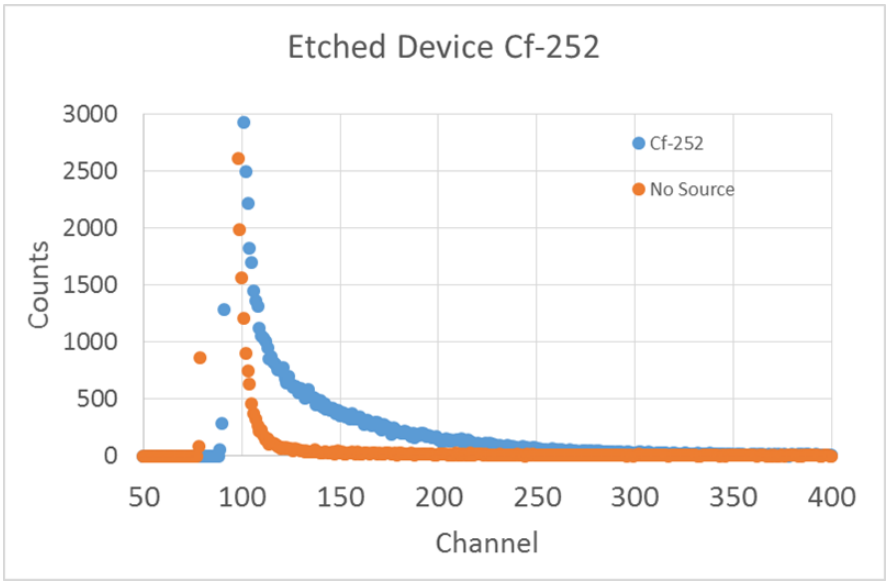

Figure 5-28: Spectra with 5mm etched device backfilled with enriched boron powder. The blue line shows the detector response to a ^{252}Cf source. The orange line is the measurement with no source. Each measurement was 6 hours in duration. There is a very evident change in detector response to the neutron source.

The thermal neutron sensitivity testing was conducted at the thermal neutron diffracted beamport. The reactor power was maintained at 200 kW for the duration of testing. These measurements were taken with the same test equipment as the ^{252}Cf testing. The results of the thermal neutron sensitivity testing are shown in Figure 5-29. Each measurement was 300 seconds in duration. The measurements were conducted with the cadmium shutter closed, with

the 2.5 mm diameter cadmium shutter aperture, and fully open. There are definite differences in the amount of counts recorded for each of the three measurements, which demonstrates that the detector is responding to incident thermal neutron beam and not albedo neutrons.

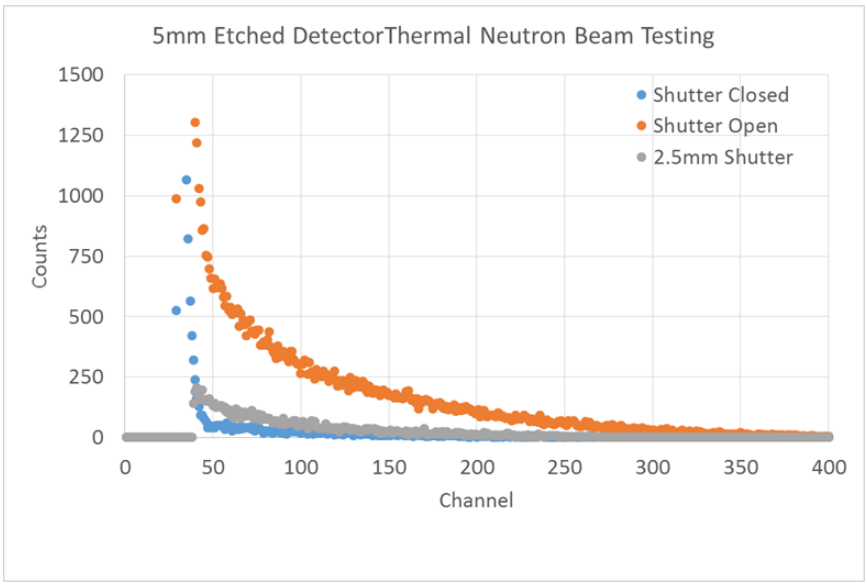

Figure 5-29: Thermal neutron beam testing. Reactor power at 200 kW. Each measurement was 300 s. Evident change in recorded counts when the incident beam was fully or partially occluded by the Cd shutter.

During testing at the beamport, it was very challenging to determine if the detector was properly positioned within the diffracted beamport. As seen in Figure 4-68, the actual detector is substantially smaller than the test box. With a 5 mm x 5 mm detector and a neutron beam stopped down to 2.5 mm diameter, positioning was crucial. One action taken to somewhat alleviate this issue was the use of an XZ motion stage. The detector box was mounted onto the stage and then roughly positioned within the neutron beam. With the cadmium shutter at a large aperture, either 5 mm or 10 mm, the detector was systematically stepped through the neutron beam. Short measurements were taken after each adjustment and recorded. After traversing in one direction, the detector was repositioned to the position with the highest counts. Next, the

detector would be stepped along the other axis and again, short measurements were recorded. This process allowed the operator to map the detector's location relative to the neutron beam. After mapping along both axes, the detector would be returned to the location with the greatest counts.

Also, a 5 mm x 5 mm planar detector was fabricated. Approximately 400 nm of enriched ^{10}B was deposited via e-beam evaporation. The purpose of this detector is to evaluate the resultant MCA pulse height spectrum of the boron reaction particles with no trenches (Figure 5-30). Reactor power was at 600 kW, measurement duration was 900 s. There is evidence of a valley separating the higher energy α-particles from the lower energy lithium ions. It is also possible to see the contribution of the 1.777 MeV α-particles. However, there is not a separation between the 840 keV lithium ion from the noise regions, which may be due to poor charge collection due to accumulated charge trapping. Also, if the boron cap layer was thicker than expected there would be additional self-attenuation of particles.

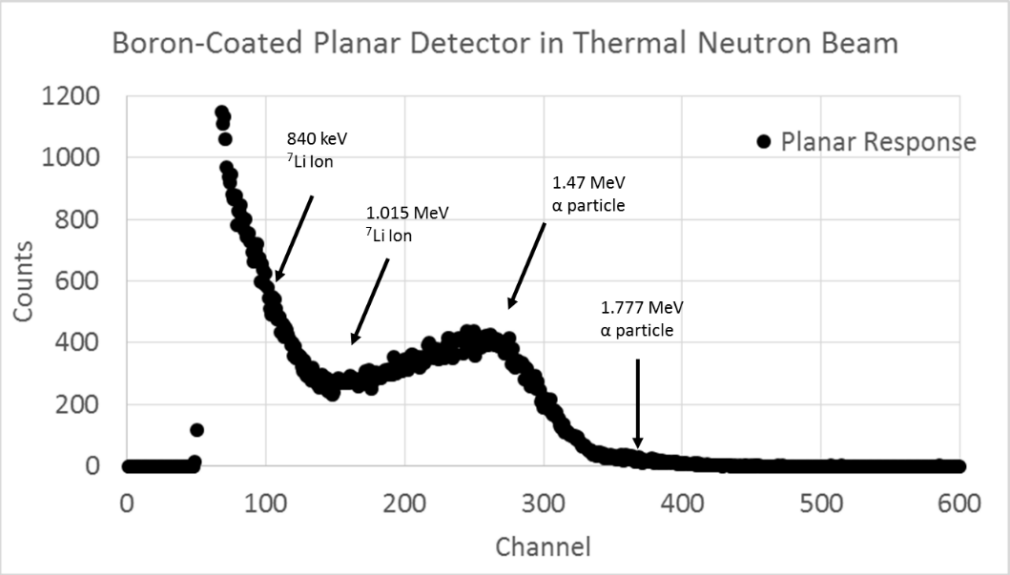

Figure 5-30: Pulse height spectrum for boron-coated planar detector within the thermal beam. Reactor power was at 600 kW, measurement duration of 900 s. The relevant spectral features are labeled.

The 5 mm x 5 mm etched detector featured in Figure 5-31 was etched to approximately 8 μm, backfilled with enriched boron powder, and then approximately 10 μm of enriched LiF was evaporated onto the detector. The purpose of this configuration is two-fold; first, was to evaluate the combined pulse height spectrum to determine if the contributions from both neutron reactive materials are identifiable. Second, if the LiF cap layer would improve neutron sensitivity with shallow trenches.

The operating conditions during testing were; 300x coarse amplification, 1.0x fine amplification, 1.0 μs, shaping time, applied bias ~ 20 V, and reactor power was maintained at 300 kW. Standard NIM bin equipment was utilized and the amplifier output signal sent to a PC running Ortec Maestro MCA Emulator for further analysis.

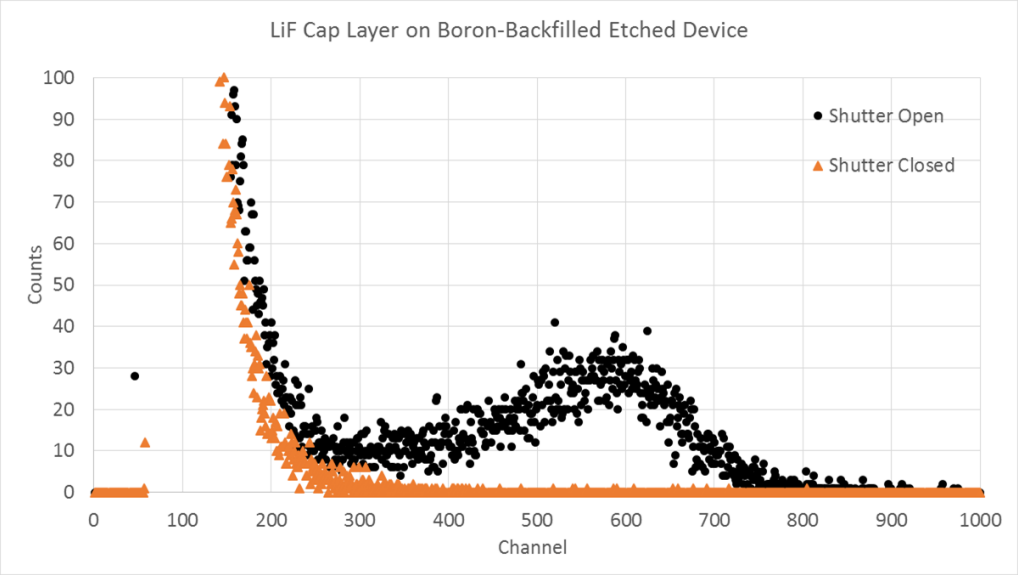

Figure 5-31: Pulse height spectrum for dual conversion material detector within the thermal beam. Reactor power was 300 kW and the measurement duration was 900 s. This detector generated similar features as the detector performance shown in Figure 5-30.

To determine thermal neutron efficiency, a SiC detector was positioned within the thermal neutron beamport of the TRIGA reactor. Measurements were conducted for 300 seconds with the 2.5 mm aperture and with the cadmium shutter fully shut. Next, the SiC detector was removed and the Reuter-Stokes ^{3}He detector was positioned into the thermal beamport. Again, 300 second measurements were conducted with the shutter full shut and with the 2.5 mm aperture. The best thermal neutron efficiency measured was 2.28±0.031%. Overall, the measured efficiency was substantially less than predicted in Table 3-2. This may have been due to poor charge collection, poor neutron conversion material packing within the trenches, or etching damage.

Chapter 6 - Conclusions and Future Work

Discussed within this chapter are the general conclusions drawn from the presented work. This chapter will also discuss reasons for the observed neutron sensitivity and device performance. Future work and suggestions for pathways to move forward with microstructured silicon carbide neutron detectors will be presented.

5.1 Conclusions

This project worked to turn bulk, high-purity, semi-insulating silicon carbide wafers into functioning neutron detectors. Efforts towards that goal began with fabricating and testing 10 mm x 10 mm planar devices both for charged particle and neutron response. Concurrently, several etching trials were conducted, with early efforts yielding good results with the larger 40 µm pitch. Etching with the 8 µm pitch, proved to be more challenging to achieve desired trench depths, while maintaining proper trench profile. The ITO used as plasma etching mask was determined to have detrimental characteristics during e-beam evaporation. The material had a tendency to spark, which would result in the deposition of large chunks of material. These large chunks, would lead to inconsistencies after the liftoff process. These inconsistencies would then lead to deviations in the final SiC features during the etching processes.

Another complication was excessive undercutting of the AZ 2070 photoresist used for liftoff process. It was possible for the etchant mask material to deposit within the etching window. These extraneous material would slowly be removed during the plasma etching processes, which would widen the etching window, leading to poor trench profiles.

Plasma etching trials were conducted with RF power ranged from 100 to 400 Watts and the ICP power was ranged from 1000 to 2200 Watts. Chamber pressure was maintained at 7 or 40 mTorr. After each etch, the sample was cleaved and examined using the SEM for etch depth and for any microfeature formation, such as microtrench or micropillars. An increase in micropillar formation was observed at the higher chamber pressures. Therefore the decision was made to use 7 mTorr for further etching trials. As the RF and ICP powers were increased, the final etched depth would also increase slightly, however, etching damage also appeared to increase. The typical settings used were 250 W for RF and 2000 W for ICP as these provided good tradeoff between etch rate and etching damage. Also, the addition of oxygen to process gas was observed to help reduce micropillar formation.

The switch to aluminum as the etchant mask did alleviate many of the complications experienced while using ITO. Aluminum is an easy metal to use for evaporation. It melts easily and can maintain a high deposition rate, which is good when depositing several microns of material in one process run.

The reduction of detector size from 10 mm x 10 mm to 5 mm x 5 mm, not only increased the total number of samples, it also decreased the leakage current of the devices. The 10 mm design had leakage currents in the nano-amp range, while the 5 mm design had leakage currents that were tens of pico-amps at 100 V applied bias. Also, as expected, the device capacitance was reduced by a factor of 4, from 25 pF to 6 pF. Several iterations of mounting substrates and test boxes were used during this project. The primary design decisions for the test boxes were as follow, reduction of outside noise, ease of use, minimal damage to detector, reduction of system noise, and improved device performance. The final designs did a fair job of providing a test box with minimal noise and good ease of use when alpha testing.

The final 5 mm x 5 mm detectors did demonstrate neutron sensitivity to both the ^{252}Cf source and the thermal neutron beam. There was a very obvious increase in spectral channels beyond the noise region when a neutron source was present. The difference in recorded spectrum when comparing the cadmium shutter being positioned open versus closed or the 2.5 mm diameter aperture, gives strong evidence to the detectors' neutron response. The best thermal neutron efficiency measured was 2.28±0.031%. This relatively low device efficiency may be a result of several factors, including, charge trapping and poor charge collection, low packing density of the enriched boron within the trenches, or due to etch damaging. Also, the SiC detectors had limited gamma sensitivity as evidenced by measurements using a ^{22}Na source.

However, the SiC devices suffered from severe charge trapping and charge polarization when under continuous irradiation. This trapping effect was evident when using high-activity alpha sources. This charge trapping behavior is inherent to the current production growth processes for bulk, HPSI SiC. Whether growth method includes the addition of vanadium as a deep-level donor or the intentional formation of deep-level point defects, the current bulk SiC material will continue to experience charge trapping effects until different production methods are invented. Alternate material such as doped epilayer SiC would be of interest for fabricated etched devices.

The failure of the final SiC wafer during dicing prevented the evaluation and testing of devices which had the topside contact formed prior to plasma etching. It was hoped that having the contact in place before etching would lead to better charge collection from the reaction products.

5.2 Future Work

Future work on silicon carbide detectors may experience better results for neutron efficiency by exploring different types of silicon carbide crystals as the semiconductor substrate. It is possible that advancements in the growth of high-resistivity SiC lead to substrates that experience less charge trapping. If the highly resistive characteristics can be obtained by methods other than intentional Vanadium doping or the formation of deep level point defects.

Extensive work has been conducted using planar epi-layer SiC devices for a variety of detection objectives. It would be interesting to see if the epi-layers would have better charge collection performance after trench formation than the bulk, semi-insulating SiC devices.

The evaluation of lithium fluoride as the neutron conversion material instead of boron may have merit as well. This change would require deeper trench etching with significantly longer etch times and etchant mask thickness. However, the trenches would also be wider (15-30 μm) which would facilitate more favorable etching characteristics than the 4μm wide trenches. The wider trenches would allow for better removal of etching products and may reduce the formation of microstructures.

Also, the reaction products of lithium have higher initial energies than the boron reaction products and are also smaller particles. These two characteristics lead to much greater penetration depth of the reaction products.

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