# The Seebeck enhancement of thermoelectric devices in CMOS technology through quantum well confinement

by

Samuel Warren Oxandale

B.S., Kansas State University, 2014

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AN ABSTRACT OF A DISSERTATION

submitted in partial fulfillment of the
requirements for the degree

DOCTOR OF PHILOSOPHY

Mike Wiegers Department of Electrical and Computer Engineering
Carl R. Ice College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2023

# Abstract

Thermoelectric devices convert convert between thermal and electrical energy. The performance of these devices is measured by the thermoelectric figure of merit $ZT = (S^2\sigma/\kappa)T$ where $S$ is the Seebeck coefficient, $\sigma$ is the electrical conductivity, $\kappa$ is the thermal conductivity, and $T$ is the temperature. Improving the thermoelectric figure of merit has proven a significant research challenge due to the interdependence of the properties involved. The Seebeck coefficient and electrical conductivity are both tied to the curvature of electron bands, and increasing one almost always results in a decrease in the other. While thermal conductivity can be decreased through phonon scattering, scattering mechanisms also scatter electrons, decreasing the electrical conductivity, counteracting any gains. Aside from material engineering, pushing beyond the current limits on the thermoelectric figure of merit will depend on our ability to decouple the Seebeck coefficient, electrical conductivity, and thermal conductivity.

This dissertation details such a path, where we enhance thermoelectric materials using quantum confinement to decouple the three properties. While quantum confinement has historically been achieved through physically small devices, such as two-dimensional superlattices, nanowires, and quantum dots, here we achieve it through electrical isolation using two-dimensional electron and hole gases in metal-oxide-semiconductor field effect transistors (MOSFETs). Under strong inversion, the two-dimensional gases form in the channel of the MOSFETs, separating the electrical path from the thermal path. Furthermore, the channel depth is constrained to quantum sizes, enabling the non-zero saturation of the Seebeck coefficient as electrical conductivity is increased. The result is a non-classical, linearly increasing power factor $S^2\sigma$ that is decoupled from thermal conductivity.

This work compares the MOSFET thermoelectric devices to similar silicon devices doped to the same concentration as the MOSFET channel in order to isolate the quantum

confinement effects in the two-dimensional gases formed in the MOSFET channel under strong inversion. The electrical conductivity, thermal conductivity, and Seebeck coefficient of the devices were measured and compared. In the p-type MOSFETS, we observe a 12-factor increase in performance over bulk silicon devices. The n-type MOSFETs showed a similar 8-factor increase in performance. This work is the first demonstration of the quantum enhancement of the Seebeck coefficent and power factor using an electrically defined quantum channel, laying the foundation for microelectronic-based, chip-scale thermoelectric cooling and energy-scavenging applications.

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Approved by:

Major Professor
Dr. Suprem R. Das

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This dissertation details such a path, where we enhance thermoelectric materials using quantum confinement to decouple the three properties. While quantum confinement has historically been achieved through physically small devices, such as two-dimensional superlattices, nanowires, and quantum dots, here we achieve it through electrical isolation using two-dimensional electron and hole gases in metal-oxide-semiconductor field effect transistors (MOSFETs). Under strong inversion, the two-dimensional gases form in the channel of the MOSFETs, separating the electrical path from the thermal path. Furthermore, the channel depth is constrained to quantum sizes, enabling the non-zero saturation of the Seebeck coefficient as electrical conductivity is increased. The result is a non-classical, linearly increasing power factor $S^2\sigma$ that is decoupled from thermal conductivity.

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# List of Abbreviations

| | |
|---|---|
| 2DEG | Two-dimensional electron gas |
| 2DHG | Two-dimensional hole gas |
| BN | Boron nitride |
| BOX | Buried oxide |
| BP | Black phosphorus |
| CVD | Chemical vapor deposition |
| DMM | Digital multimeter |
| IV | Current-voltage |
| MOSFET | Metal-oxide-semiconductor field-effect transistor |
| PS | Power supply |
| SEM | Scanning electron microscope |
| SEU | Single event upset |
| SM | Source meter |
| TEC | Thermoelectric cooler |
| TEG | Thermoelectric generator |

| | |
|---|---|
| TMAH | TetraMthylAmmonium Hydroxide |
| TMD | Transitional metal dichalcogenides |
| TRC | Temperature resistance calibration |

# List of Symbols

| | |
|---|---|
| $\epsilon$ | Permittivity |
| $\eta$ | Efficiency |
| $\hbar$ | Reduced Planck's constant |
| $\kappa$ | Thermal conductivity |
| $\mu$ | Electron mobility |
| $\overrightarrow{j}$ | Current density |
| $\overrightarrow{q}$ | Heat flux vector |
| $\Pi$ | Peltier coefficient |
| $\sigma$ | Electrical conductivity |
| $\tau$ | Phonon relaxation time |
| $\zeta$ | Chemical potential |
| $\zeta^*$ | Reduced chemical potential |
| $A$ | Area |
| $a$ | Quantum-well depth |
| $C$ | Specific heat |
| $COP$ | Coefficient of performance |
| $d$ | Depth |

| | |
|---|---|
| $E$ | Energy |
| $e$ | Free electron charge |
| $E_F$ | Fermi level |
| $f(E)$ | Fermi distribution function |
| $F_i$ | Fermi-Dirac function (see Eq. 2.12) |
| $G$ | Conductance |
| $g(E)$ | Density of states |
| $h$ | Planck's constant |
| $I$ | Current |
| $k$ | Electron momentum |
| $k_B$ | Boltzman constant |
| $L$ | Length |
| $m^*$ | Effective electron mass |
| $n$ | Quantum energy number |
| $n(E)$ | Energy-dependent electron density |
| $S$ | Seebeck coefficient |
| $T$ | Temperature |
| $t$ | Thickness |

| | |
|---|---|
| $T(E)$ | Energy-dependent conduction |
| $V$ | Voltage |
| $v$ | Phonon group velocity |
| $w$ | Width |
| $ZT$ | Thermoelectric figure of merit |
| K | Thermal conductance |
| L | Length |

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# Chapter 1

# Introduction and Background

Thermoelectric materials are solid-state semiconductors or metals that transform heat into electric voltage and vice versa. They are silent, scalable, and reliable making them ideal for thermal energy harvesting and cooling applications[1]. However, their poor performance relative to other energy harvesting and cooling systems has hampered their adoption. In recent decades, researchers have investigated methods of improving existing thermoelectric materials and developed promising new materials. However, optimizing and developing thermoelectric materials is not simple, with many related material properties at play. As a result, methods of improving one component of performance often hurt another, limiting overall improvement.

While researchers have discovered many promising potential thermoelectric materials, many of the best materials are a combination of rare, expensive, and toxic. Though inconsequential for some applications, they still prevent the widespread commercial application of thermoelectric materials.

This work details a novel method for improving thermoelectric performance in any semiconductor. Silicon, an abundant material with well-defined fabrication processes, is used to experimentally demonstrate the approach's viability.

In this chapter, we outline the operating principles of thermoelectric materials: the

Seebeck, Peltier, and Thomson effects. We also discuss thermoelectric performance and introduce the thermoelectric figure of merit $ZT$. Then, we broadly review recent work on thermoelectric materials in literature. Next, we discuss the shortcomings of CMOS-compatible thermoelectric devices and how they motivate this work. Finally, we provide a brief outline of the organization of the dissertation.

## 1.1 Operating Principles of Thermoelectrics

Three main effects explain the functions of thermoelectric materials: the Seebeck, Peltier, and Thomson effects. The Seebeck effect, detailed in Section 1.1.1, describes the voltage resulting from a temperature gradient in thermoelectric materials. Next, the Peltier effect, discussed in Section 1.1.2, describes how a current induces a temperature gradient in thermoelectric materials. Finally, the Thomson effect, explored in Section 1.1.3, details the absorption and rejection of heat in a single, locally heated conductor when a current passes through it.

### 1.1.1 The Seebeck Effect

The Seebeck effect, reported by Thomas Johann Seebeck in 1821[2], describes the movement of carriers (e.g., electrons and holes) in a thermoelectric material from hot to cold as they seek lower energy states. Because of this, thermoelectric devices produce a voltage in response to a temperature differential. Typically, the voltage is on the order of millivolts but increases proportionally to the difference in temperature. The Seebeck coefficient $S_{ab}$ for two materials $a$ and $b$ joined together is defined in Eq. 1.1[2]:

$$S_{ab} = \lim_{\Delta T \to 0} \frac{\Delta V_{ab}}{\Delta T} \tag{1.1}$$

where $\Delta V_{ab}$ is the voltage across two different connected conductors with an applied temperature gradient of $\Delta T$, as shown in Figure 1.1.

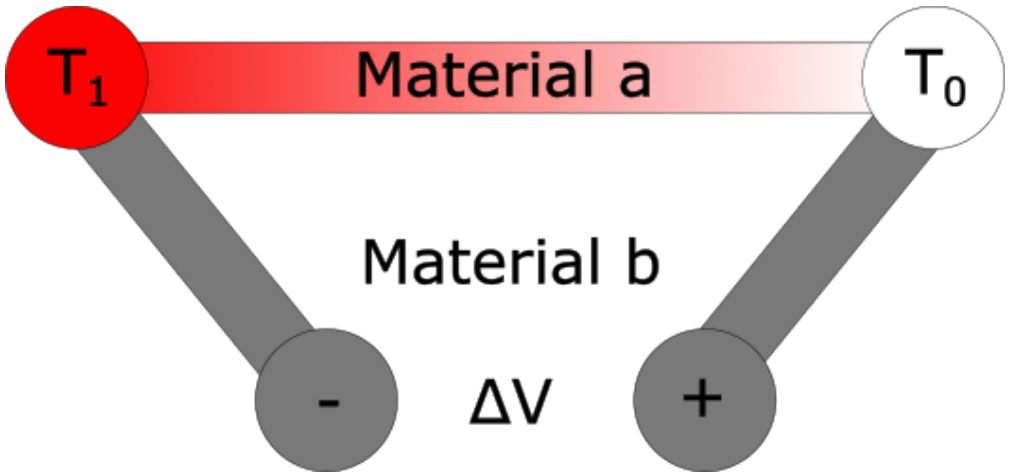


Figure 1.1: Illustration of the Seebeck effect for material $a$ and material $b$ joined at interfaces at temperatures $T_1$ and $T_0$, such that $T_1 > T_0$. Here the temperature gradient is imposed, inducing the voltage.

We can more easily observe the Seebeck coefficient with two different materials because of the asymmetry present in the system. The individual Seebeck coefficient of each material varies, meaning carriers will flow more effectively away from the heat in one material. In a symmetrical system, such as a wire heated in the middle, carriers would flow similarly away from the heated point in both directions, and the effects would cancel.

### 1.1.2 The Peltier Effect

Thermoelectrics also exhibit the Peltier effect, where thermal energy is absorbed or rejected at an Ohmic junction between two dissimilar conductors[3]. The thermal exchange results from a difference in the Fermi energy levels $E_F$ beyond the junction, with carriers absorbing heat when moving to a higher Fermi energy level and carriers rejecting heat when moving to a lower Fermi energy level. Figure 1.2 illustrates the effect.

Eq. 1.2 gives the rate of thermal exchange at the junctions:

$$Q_P = S_{ab} I T = \Pi_{ab} I \tag{1.2}$$

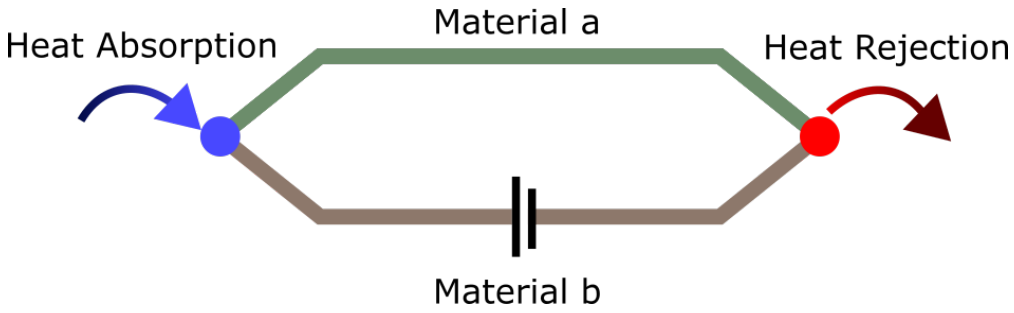


Figure 1.2: Illustration of the Peltier effect between two different materials $a$ and $b$. Current flows from the power source resulting in heat absorption at the left node, where carriers move to a higher Fermi energy level, and heat rejection at the right node, where carriers move to a lower Fermi energy level, leading to a temperature gradient across the device.

where $I$ is the current through the junction at temperature $T$ and $\Pi$ is the Peltier coefficient of the junction.

### 1.1.3 The Thomson Effect

The Thomson effect, discovered by William Thomson in 1856, is the absorption and rejection of heat caused by an electric current in a single conductor[4]. Suppose we heat a wire at a single point and pass current through it. In that case, the carriers absorb heat before the heated point to climb to the higher Fermi energy level and reject it beyond the heating point when returning to a lower Fermi energy level. The result is a cooler section of wire before the heated point and a hotter section after, as shown in Figure 1.3. This phenomenon occurs in addition to the Joule heating typical of conductors.

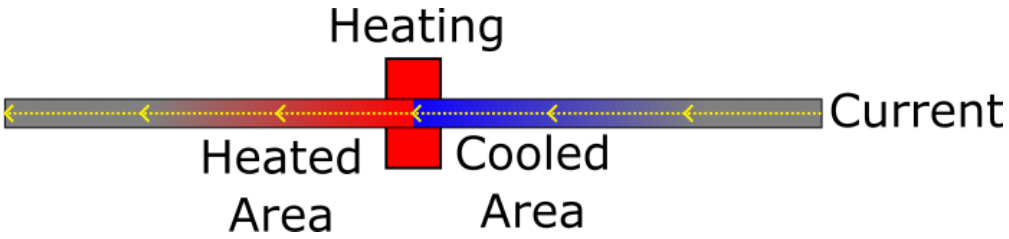


Figure 1.3: Illustration of the Thomson effect. Current flows through a conductor heated at a point, resulting in the cooling of the wire before the heated point as carriers absorb energy to move to higher Fermi energy levels and heating of the wire after as carriers release energy while returning to lower Fermi energy levels.

### 1.1.4 The Superposition of Thermoelectric Effects

Thomson also developed critical relationships, including Eq. 1.2, between the Seebeck, Peltier, and Thomson effects under the assumption that all thermoelectric processes, whether reversible or irreversible, are superimposed on each other and thus separable[4]. The scientific community hotly debated the premise until the advent of new thermodynamics[5–8]. The theory was later experimentally confirmed as a consequence of Onsager's Reciprocal Principle[5].

Perhaps the most critical relation derived by Thomson is given in Eq. 1.3[9]:

$$\overrightarrow{q} = ST\overrightarrow{j} - \kappa\overrightarrow{\Delta}T \tag{1.3}$$

where $\overrightarrow{q}$ is the heat flux vector, $\kappa$ is the thermal conductivity, and $\overrightarrow{j}$ is the current density. The first term $ST\overrightarrow{j}$ contains all contributions from the Seebeck, Peltier, and Thomson effects[1;10;11], which are reversible. The second term $\kappa\overrightarrow{\Delta}T$ gives thermal conduction, which is irreversible.

## 1.2 Thermoelectric Performance

When comparing thermoelectric materials, we look at the thermoelectric figure of merit $ZT$. In this section, we describe the formulation and components of the thermoelectric figure of merit. Then, we note several performances achieved in literature. Finally, we relate the thermoelectric figure of merit to efficiency and the coefficient of performance, which measure the performance of more traditional thermal energy harvesting and cooling systems, respectively.

### 1.2.1 Thermoelectric Figure of Merit

We characterize the performance of thermoelectric materials by the thermoelectric figure of merit $ZT$, defined in Eq. 1.4[12]:

$$ZT = \frac{S^2\sigma}{\kappa}T \tag{1.4}$$

where $S$ is the Seebeck coefficient, $\sigma$ is the electrical conductivity, $\kappa$ is the thermal conductivity, and $T$ is the absolute temperature

From Eq. 1.4, we see that we can improve the thermoelectric figure of merit by increasing the Seebeck coefficient, increasing the electrical conductivity, or decreasing the thermal conductivity, which we can further break down into electronic and phononic contributions, as in Eq. 1.5:

$$\kappa = \kappa_e + \kappa_{ph} \tag{1.5}$$

### 1.2.2 Current Performances in Literature

The thermoelectric figure of merit is a widely reported metric for new and promising thermoelectric materials. Table 1.1 displays a selection of recent thermoelectric figures of merit obtained in literature.

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The list shows materials with thermoelectric figures of merit from 0.8 to 2.6, but most

Table 1.1: Selected thermoelectric figures of merit obtained recently in literature.

| Material | Year | Doping | Temperature, K | $ZT$ |
|---|---|---|---|---|
| $Pb_{1+x}Se_{0.8}Te_{0.2}$ [13] | 2022 | n | 600 | 1.20 |
| $Ag_2Te$ Nanoparticles [14] | 2022 | n | 373 | 1.37 |
| Porous Si Nanowires [15] | 2021 | p | 700 | 0.71 |
| Polycrystalline SnSe [16] | 2021 | p | 783 | 3.10 |
| $Ge_{0.9}Mg_{0.04}Bi_{0.06}Te$ [17] | 2021 | n | 700 | 2.50 |
| BiSbTe/Carbon Microfiber [18] | 2021 | p | 375 | 1.40 |
| $Sb_2Si_2Te_6$ [19] | 2021 | p | 823 | 1.30 |
| $Mg_3Sb_2$ [20] | 2020 | p | 750 | 1.50 |
| $CaZrSe_3$ [21] | 2019 | p | 700 | 0.95 |
| $Mg_{3.2}Sb_{1.5}Bi_{0.49}Te_{0.01}$ [22] | 2018 | p | 650 | 1.55 |
| $(Bi,Sb)_2Te_3$ [23] | 2017 | p | 395 | 1.10 |
| PbTe-SrTe [24] | 2016 | p | 923 | 2.50 |
| BiSbTe+Te arrays [25] | 2015 | p | 320 | 1.86 |
| PbTe-PbS [26] | 2015 | p | 923 | 2.30 |
| $Na_{2+x}Ga_{2+x}Sn_{4-x}$ [27] | 2015 | n | 340 | 1.28 |
| GeTe-$Bi_2Te_3$ [28] | 2014 | p | 773 | 1.90 |
| Pb(Te,Se,S) [29] | 2014 | p | 800 | 2.00 |
| PbS-CdS [30] | 2014 | p | 923 | 1.30 |
| SnSe [31] | 2014 | p | 923 | 2.60 |
| $Cu_{2-x}S$ [32] | 2014 | p | 1000 | 1.70 |
| SnTe-CdS [33] | 2014 | p | 923 | 1.40 |
| $Pb_{1-x}Sb_xSe$ [33] | 2014 | n | 800 | 1.50 |
| MgAgSb [34] | 2014 | p | 475 | 1.40 |
| $Cu_x$BiTeSe [35] | 2013 | n | 340 | 1.15 |
| PbTe-SrTe [36] | 2012 | p | 915 | 2.20 |
| $Mg_2Si_{0.3}Sn_{0.7}$ [37] | 2012 | n | 700 | 1.30 |
| $Cu_{2-s}Se$ [38] | 2012 | p | 1000 | 1.50 |
| $(BaLaYb)_xCo_4Sb_{12}$ [39] | 2011 | n | 850 | 1.70 |
| $In_4Se_3$ [40] | 2009 | n | 705 | 1.48 |
| BiSbTe [41] | 2008 | p | 300 | 1.20 |
| Tl-PbTe [42] | 2008 | p | 773 | 1.50 |
| $Ba_8Ga_{16}Ge_{13}$ [43] | 2006 | n | 1163 | 1.63 |
| $AgPb_mSbTe_{2+m}$ [44] | 2004 | n | 800 | 2.20 |

materials listed are a combination of exotic, hard to fabricate, and toxic. Only one of these obtain their highest thermoelectric figures of merit around room temperature: BiSbTe [41] with a $ZT$ of 1.20 at 300K. Several of these materials employ strategies for improving the thermoelectric figure of merit, which we will discuss in Section 1.3.

Narrowing in on silicon and CMOS-compatible devices, similar to what this work studies, Table 1.2 shows thermoelectric figures of merit for silicon and CMOS-compatible based devices.

Table 1.2: Selected thermoelectric figures of merit of silicon and CMOS-compatible devices obtained recently in literature.

| Material | Year | Doping | Temperature, K | $ZT$ |
|---|---|---|---|---|
| Silicon nanowires[45] | 2020 | p | 300K | 0.02 |
| Silicon nanowires[46] | 2021 | p | 300+K | 0.0035 |
| Polysilicon[47] | 2014 | n | 373K | 0.03 |
| Polysilicon[47] | 2014 | p | 373K | 0.05 |
| CMOS Polysilicon films[48] | 2009 | n | 300K | 0.014 |
| CMOS Polysilicon films[48] | 2009 | p | 300K | 0.012 |

Silicon's performance as a thermoelectric material is generally poor due to its high thermal conductivity. However, silicon is the material of choice for microelectronics. Therefore, using it as a thermoelectric material in these systems is much easier than using the materials in Table 1.1. Because of this, we focus on improving silicon's thermoelectric figure of merit using a CMOS-compatible method.

### 1.2.4 Efficiency and Coefficient of Performance

Furthermore, the conversion efficiency of a thermoelectric device may be written in terms of the thermoelectric figure of merit both when acting as a thermoelectric generator (TEG) and as a thermoelectric cooler (TEC). Equations 1.6 and 1.7 describe the efficiency $\eta$ for a TEG and the coefficient of performance $COP$ for a TEC, respectively[49]:

$$\eta = \frac{T_h - T_c}{T_h}\left(\frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+T_c/T_h}\right) \tag{1.6}$$

$$COP = \frac{T_c}{T_h - T_c}\left(\frac{\sqrt{1+ZT}-T_h/T_c}{\sqrt{1+ZT}+1}\right) \tag{1.7}$$

where $T_h$ and $T_c$ are the hot and cold temperatures, respectively. These relations allow the comparison of thermoelectric materials to commercial systems whose performance is generally measured using efficiency and the coefficient of performance.

For thermoelectric materials to have competitive efficiency for commercial applications, a thermoelectric figure of merit of 4 is estimated to be required[49]. Table 1.1 has a maximum thermoelectric figure of merit of 2.6. We can see the differences in efficiency in Figure 1.4, which plots Eq. 1.6 for a selection of thermoelectric figures of merit, showing the relationship between the thermoelectric figure of merit $ZT$, temperature differential $\Delta T$, and efficiency for TEGs, and Figure 1.5 plots Eq. 1.7 for a selection of thermoelectric figures of merit, showing the relationship between the thermoelectric figure of meri, temperature differential $\Delta T$, and coefficient of performance for TECs.

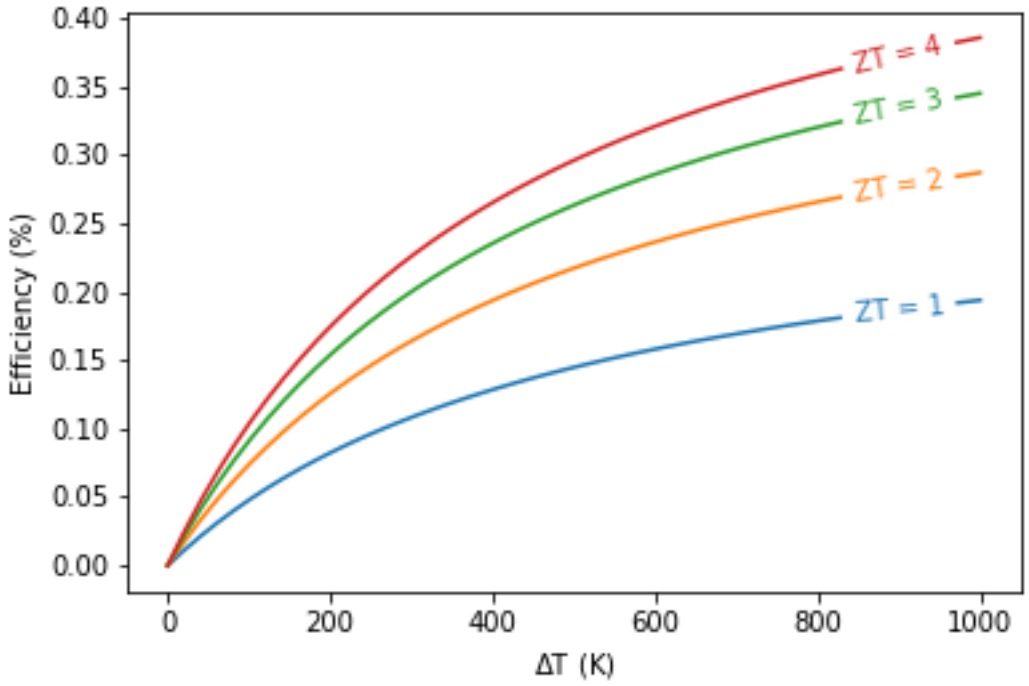


Figure 1.4: Efficiency $\eta$ of a thermoelectric generator (TEG) for a given temperature difference $\Delta T$ for a selection of thermoelectric figures of merit $ZT$. Eq. 1.6 is solved assuming the cold side temperature $T_c$ to be 300 K.

In these, we see that an improved thermoelectric figure of merit results in increased

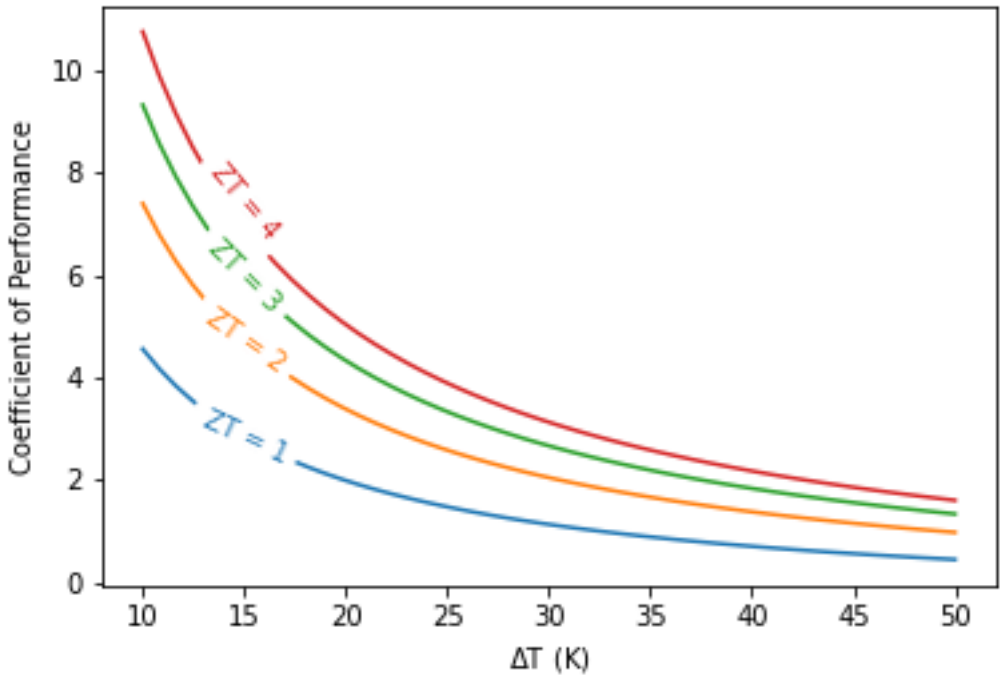


Figure 1.5: Coefficient of performance $COP$ of a thermoelectric cooler (TEC) for a given temperature difference $\Delta T$ for a selection of thermoelectric figure of merit $ZT$ values. Eq. 1.7 is solved assuming the hot side temperature $T_h$ to be 300 K.

efficiency or coefficient of performance.

## 1.3 Thermoelectric Performance Improvement Methods

Historically, low thermoelectric figures of merit, meaning poor efficiency, have kept thermoelectric materials from becoming used in applications where efficiency is essential[50]. Naturally, this has led to extensive research on improving the thermoelectric figure of merit in thermoelectric materials. However, because of the interdependence of the Seebeck coefficient $S$, electrical conductivity $\sigma$, and thermal conductivity $\kappa$, improving the thermoelectric figure of merit $ZT$ is difficult.

The main paths for improving the thermoelectric figure of merit focus on reducing the phonon contribution to thermal conductivity, which reduces the denominator in Eq. 1.4, or

electronic band manipulation, which increases the numerator in Eq. 1.4, commonly referred to as the power factor. The following sections detail the methods employed and their disadvantages.

### 1.3.1 Phonon Engineering

For nonmetallic thermoelectric materials, phonons are the dominant heat carriers[51]. Many recent attempts at improving the thermoelectric figure of merit focus on scattering phonons[52–54] to reduce the phonon contribution to thermal conductivity $\kappa_{ph}$ defined by the Boltzmann transport equation, shown in Eq. 1.8[55]:

$$k_{ph} = \frac{1}{3} C v^2 \tau \tag{1.8}$$

where $C$ is the specific heat, $v$ is the phonon group velocity, and $\tau$ is the phonon relaxation time. Methods that reduce the phononic contribution to thermal conductivity typically use incoherent mechanisms to reduce phonon relaxation time through increased grain boundary scattering, impurity scattering, and rough surface scattering.

From Table 1.1, $Cu_{2-s}Se$[38] and SnSe[31] employ phonon scattering to reduce thermal conductivity, achieving thermoelectric figures of merit of 1.5 at 1000K and 2.6 at 923K, respectively. Effective phonon scattering optimization can also improve performance in traditional thermoelectric materials, such as skutterudites[39;56–58].

The following sections detail the importance of measuring phonon coherence, how phonon coherence affects thermal conductance, and specific methods used to reduce the phonon contribution to thermal conductivity.

#### 1.3.1.1 Phonon Coherence

The coherent transport of energy characters (e.g., electrons, photons, and phonons) is crucial to understanding material properties. However, unambiguous observation of phonon coherence

is challenging relative to the observation of electron and photon coherence due to the short coherence length of phonons and its significant reduction in the presence of imperfections and increased temperature. Recent studies[59;60] have shown that phonons can remain coherent through many layers of superlattices, making them ideal systems for observing phonon coherence and providing strong evidence of the wave behavior of phonons in coherent phonon heat conduction. Moreover, a femtosecond pump-probe has been developed to directly measure the oscillation of coherent phonons[61–64]. Studies have found that phonon coherence plays a sizable role in the reduction of thermal conductance in silicon nitride membranes[65], silicon nanomeshes[66;67], silicon[65;67;68], and $Bi_2Te_3/Sb_2Te_3$[69].

#### 1.3.1.2 Nanoscale Local Resonators

A strategy to reduce thermal conductivity is the introduction of nanoscale resonators, enabling the emergence of unique subwavelength properties. We can alter phonon dispersion relations by engineering nanopillars, reducing the phonon group velocities for dominant heat carriers. Davis and Hussein[70] applied this to thin silicon films, showing a 52% reduction in thermal conductivity compared to a uniform silicon film.

For bulk materials, such as clathrates and skutterudites, filling atoms into them has been shown to induce a rattling effect[39;71]. This rattling effect significantly reduces thermal conductivity and improves thermoelectric performance. This strategy does not alter the electronic band structure, leaving electrical conductivity unchanged. Qiu et al.[72] and Shi et al.[73] achieved high thermoelectric figures of merit in skutterudites using this method.

#### 1.3.1.3 Disadvantages

While phonon engineering can reduce the phonon contribution to thermal conductivity, it also can have the undesired effect of decreasing the electrical conductivity, mitigating any gains in the thermoelectric figure of merit. Additionally, electrons still contribute to the overall thermal conductivity. These methods are also material-dependent and require substantial

work to adapt to new materials.

### 1.3.2 Electronic Band Manipulation

In addition to reducing the thermal conductivity, we can also enhance the thermoelectric figure of merit by increasing the power factor $S^2\sigma$. We can achieve this by manipulating the electric band, typically done by changing the carrier concentration. Unfortunately, the Seebeck coefficient and electrical conductivity depend on the carrier concentration and improving one harms the other. Figure 1.6 illustrates this inverse relationship[49].

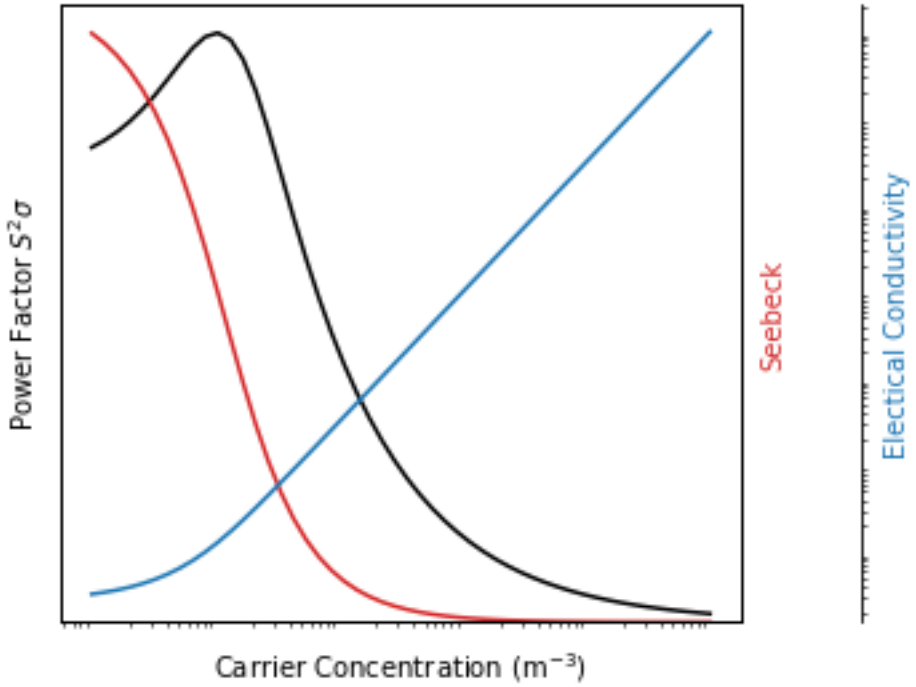


Figure 1.6: Plot showing the qualitative relationships of power factor (black), Seebeck coefficient (red), and electrical conductivity (blue) to carrier concentration. The carrier concentration and electrical conductivity are on a log scale.

At decreased carrier concentrations, the Seebeck coefficient increases, but electrical conductivity decreases. Conversely, the Seebeck coefficient decreases to zero at increased carrier concentrations while electrical conductivity increases. Because of this, we quickly find an optimal carrier concentration where movement in either direction decreases the power

factor. Thus, we see that attempts at manipulating the electronic band are severely limited.

### 1.3.3 Novel Materials and Structures for Thermoelectrics

Finally, researchers have attempted to design and fabricate several new thermoelectric materials. We can see several examples in literature of different hybrid materials synthesized and shaped to produce a high thermoelectric figure of merit. This material engineering ranges from fabricating novel materials to creating low-dimensional versions of commercial materials that exhibit non-bulk characteristics. Researchers often apply this low dimensional technique to the more widely used thermoelectric materials: $Bi_2Te_3$[74], $Bi_2Se_3$[75], and their alloys with Sb and Se, because, for these traditional materials, the relationship of the Seebeck coefficient, electrical conductivity, and thermal conductivity limits the thermoelectric figure of merit.

Development in physical and chemical nanofabrication technologies has made structures such as thin films, nanowires, superlattices, and quantum dots easier to fabricate. While early studies relied on physical fabrication methods like mechanical exfoliation[76], ball milling[77], high-pressure synthesis[78], and vacuum condensation[79], chemical methods have recently become more effective nanomaterial fabrication methods. Solution-phase and spark plasma sintering methods have been used to fabricate $(Si,Bi)_2(Te,Se)_3$ nanoparticles[80;81] and $Te/Bi_2Te_3$core/shell nanowires[82]. Chemical vapor deposition (CVD)[83;84], epitaxial film growth[85], and hydrothermal methods[86] have successfully fabricated two-dimensional thermoelectric materials and superlattices.

#### 1.3.3.1 Nanowires

Nanowires have gained attention as thermoelectric materials because of their low thermal conductivity. The primary cause for the reduction in thermal conductivity is phonon-boundary scattering at the nanowire's roughened surface; the surface-to-volume ratio in any nanowire increases phonon-boundary scattering compared to bulk materials[87]. Silicon nanowires have thermal conductivity approximately two orders of magnitude smaller than bulk silicon while

maintaining a similar power factor[88]. Then, the power factor can be further optimized through doping[89].

#### 1.3.3.2 Two-dimensional Materials

Two-dimensional materials, like nanowires, also exhibit unique properties, making them interesting to research. Several two-dimensional materials, such as transition metal dichalcogenides (TMDs)[90], black phosphorus (BP)[91–93], hexagonal boron nitride (BN)[94], germanane[95], borophene[96–98], InSe[99], silicene[100], and stanene[85], have received attention as thermoelectric materials. Group IV-VI layered compounds, such as GeS[101], GeSe[101], SnS[102], and SnSe[31;103;104], have also been studied.

In particular, $MoS_2$, a TMD, is one material thought to have potential as a thermoelectric material due to its low thermal conductivity[105–107] and high Seebeck coefficient[108–110]. With p-doped bilayer $MoS_2$, Wickramaratne et al.[111] achieved a thermoelectric figure of merit $ZT$ of 1.2. In a nanoribbon structure, Fan et al.[112] achieved a ZT of 3.4 at room temperature. The thermoelectric figure of merit of $MoS_2$ can be further improved by introducing strain, which tunes the electric and thermal properties[113–115].

Another interesting two-dimensional material is single or several-layer black phosphorus (BP), which was first fabricated in 2014[91–93] and garnered interest because of its anisotropic properties[116–118]. Even as a bulk material, Qin et al.[119] demonstrated a $ZT$ value of 0.7 at 800 K with BP. The band gap can also be continuously tuned by altering the number of layers. These results and the tunable bandgap indicate that BP could be a desirable thermoelectric material at intermediate temperatures.

#### 1.3.3.3 Drawbacks of Novel Materials

While these novel materials show promise, many have complex and relatively new fabrication processes[76–79;93]. Furthermore, these processes are generally unique to each material, and many of these materials are a combination of complicated to process, toxic, naturally scarce,

mechanically rigid, and expensive[120–124]. Finally, tuning and material engineering must consider the unique properties of each material, making a fair amount of work to explore a particular method's use with a different material.

### 1.3.4 Quantum Confinement to Enhance Seebeck Coefficient

The work of Hicks and Dresselhaus[125–127] showed that in low-dimensional materials, the physical dimensions affect the thermoelectric properties, providing an alternative way to tune them. However, rather than inducing quantum confinement using the traditional path of low-dimensional materials (e.g., superlattices[52;53;124;128;129] and nanowires[128;130–132]), quantum confinement is generated through the creation of a two-dimensional electron or hole gas (2DEG or 2DHG, respectively) in a metal-oxide-semiconductor field-effect transistor (MOSFET) under strong inversion. This act separates the dominant thermal path (the MOSFET body) from the dominant electrical path (the MOSFET channel), allowing these to be tuned separately. Additionally, the Seebeck coefficient in the 2DEG or 2DHG saturates at high carrier concentrations, allowing for the continued increase in electrical conductivity without the Seebeck coefficient going to zero. Because of this, the method used in this work can decouple the thermoelectric properties.

MOSFET fabrication follows the complementary metal-oxide-semiconductor (CMOS) fabrication guidelines, which are well-established and repeatable. MOSFETs are the backbone of modern computer chips and thus have had extensive work done to ensure their reliability. While we use silicon for devices in this work, we can straightforwardly reproduce the results in MOSFETs fabricated on other semiconductors. We provide in-depth details on the theory behind this in Chapter 2.

## 1.4 Motivation

While thermoelectric materials are widely studied, the literature on CMOS-compatible thermoelectrics is more sparse. This sparseness is partly due to the strict list of materials allowed in CMOS fabrication, which, partnered with the favored approach of novel materials, prevents the application of the bulk of thermoelectric research from applying to CMOS devices.

While sparse, results have been published on CMOS-compatible thermoelectrics[133–136]. Strasser et al.[133] micromachined CMOS thermoelectric generators for powering on-chip electronics. Their approach requires fabrication steps in addition to those in the CMOS process, adding time and expense to fabrication. The devices are also relatively large compared to CMOS structures, making them unsuitable for smaller-scale thermal management applications.

Xie et al.[134] proposed a MEMs-based design, which uses a membrane-like structure. Bah et al.[135] also fabricated a crystalline silicon membrane with the addition of nanopores in a CMOS-compatible process. Li et al.[136] used a CMOS-compatible top-down technique to fabricate silicon nanowire-based thermoelectric generators.

The studies mentioned above do little to improve the thermoelectric performance of the polysilicon forming their devices, aside from thermal conductivity suppression from phonon scattering. While Seebeck coefficients are given, none of them report a thermoelectric figure of merit. While the thermoelectric figure of merit is difficult to measure, it is an essential characteristic of these systems.

This work addresses the shortcomings of current work on CMOS-compatible thermoelectrics by

1. Reporting the first use of electrically-induced quantum confinement to improve the thermoelectric performance of devices. Quantum confinement is a novel approach for CMOS-compatible thermoelectric devices.

2. Inducing said quantum confinement using MOSFETs, which are readily and easily fabricated in the CMOS process, requiring no external tooling or materials. The devices are also on the scale of other microelectronics structures, allowing for more localized thermal management applications. Several current CMOS-compatible thermoelectric materials are "add-ons" and, unlike our devices, cannot be tuned by adjusting gate voltage. Additionally, our approach has the advantage of pumping heat in-plane rather than vertically, which is advantageous in three-dimensional circuit applications.

3. Introducing a novel characterization method that allows for the accurate measurement of the thermoelectric figure of merit and its constitutive properties. This method uses control devices with bulk silicon properties to normalize the results and eliminate systemic measurement errors.

## 1.5 Dissertation Organization

With this background knowledge, we proceed to a more detailed discussion of theory, device design, experiment, and results.

First, in Chapter 2, we discuss the underlying theory behind the methods used in this work to enhance thermoelectric materials using metal-oxide-semiconductor field-effect transistors (MOSFETs). We discuss the relationship between the density of states and the Seebeck coefficient and how this applies to low-dimensional systems, such as quantum wells. In detail, we discuss quantum well induced by MOSFETs and the effects on the thermoelectric properties.

Next, in Chapter 3, we detail the design of the different devices studied in this work, including n-type and p-type MOSFET structures and n-doped and p-doped control devices. We describe how MOSFETs are chained together to achieve greater length and the thought process behind selecting resistors for on-device temperature induction and measurement. We also briefly discuss the fabrication of the devices used in this work.

After, in Chapter 4, we detail the experimental setup used to measure the thermoelectric characteristics of the devices. We outline the device's temperature-resistor calibration to ensure accurate temperature readings. We discuss the current-voltages curves needed to obtain electrical conductivity. Finally, we discuss the thermoelectric characterization used to determine the Seebeck coefficient and thermal conductivity. We also outline the minimal processing for obtaining the Seebeck coefficient, electrical conductivity, and thermal conductivity from the direct measurements.

In Chapter 5, we report the findings of the experiments discussed in Chapter 4. Here, we show approximately an order of magnitude improvement of the thermoelectric figure of merit of MOSFET devices compared to the control diffusion devices. We show the saturation of the Seebeck coefficient predicted at gate voltages (and thus high carrier concentrations). This saturation then allows increasing electrical conductivity to improve the thermoelectric figure of merit.

Finally, in Chapter 6, we summarize the findings of this dissertation. We reiterate the importance of the work and the key findings before proposing additional work.

# Chapter 2

# Theory

This chapter discusses the theory behind using quantum confinement to enhance thermoelectric materials introduced in Section 1.3.4. We discuss the Seebeck dependence on the density of states and how that applies in quantum well systems as predicted by Hicks and Dresselhaus [126], and how it affects thermoelectric performance characterized by the thermoelectric figure of merit $ZT$ shown in Eq. 2.1:

$$ZT = \frac{S^2\sigma}{\kappa_e + \kappa_{ph}}T \tag{2.1}$$

where $S$ is the Seebeck coefficient, $\sigma$ is electrical conductivity, and $\kappa_e$ and $\kappa_{ph}$ are the electron and phonon contributions to thermal conductivity.

As we use metal-oxide-semiconductor field-effect transistors (MOSFETs) to induce quantum wells, we also provide a basic overview of the nomenclature and function of MOSFETs.

## 2.1 Seebeck Dependence on Density of States

First, we establish the dependence of the Seebeck coefficient on the density of states. A conductor has an energy-dependent conductivity $\sigma(E)$ that is associated with the electrons of density $n(E)$ filling the energy states at $E$ as described by Eq. 2.2:

$$\sigma(E) = en(E)\mu(E) \tag{2.2}$$

where $e$ is the free electron charge and $\mu$ is the electron mobility. From this, Ziman derived the expression for the total conductivity shown in Eq. 2.3[137]:

$$\sigma = G\frac{L}{A} = \int \sigma(E)\left(-\frac{\delta f(E)}{\delta E}\right) dE \tag{2.3}$$

where $f(E)$ is the Fermi distribution function, $G$ is the conductance, $L$ is the length, and $A$ is the cross-sectional area of the conductor. However, for small-scale conductors, it may be more appropriate to consider the conductance formulated in the Landauer formalism in terms of energy-dependent transmission $T(E)$ as shown in Eq. 2.4:

$$G = \frac{2e^2}{h}\int T(E)\left(-\frac{\delta f(E)}{\delta E}\right) dE \tag{2.4}$$

where $h$ is Planck's constant. From Eq. 2.3, Cutler and Mott derived the Mott relation form of the Seebeck coefficient[138] as seen in Eq. 2.5:

$$S = \frac{1}{\sigma}\frac{k_B}{e}\int \sigma(E)\left(\frac{E - E_f}{k_B T}\right)\left(-\frac{\delta f(E)}{\delta E}\right) dE \tag{2.5}$$

where $k_B$ is the Boltzman constant.

For a degeneratively doped system, Equation 2.5 further simplifies to Eq. 2.6:

$$S = \frac{\pi^2}{3}\frac{k_B}{e}k_B T\left[\frac{d\ln(\sigma(E))}{dE}\right]_{E=E_F} \tag{2.6}$$

where $E_F$ is the Fermi energy level.

Equation 2.6 shows that enhancing the energy dependence of the conductivity $d\sigma(E)/dE$, which is related to the energy-dependent electron density through Eq.2.2, increases the Seebeck coefficient. Equation 2.2 shows that the energy dependence of the conductivity $d\sigma(E)/dE$ is related to the energy-dependent electron density. Because energy-dependent electron density is related to the density of states, we can improve the Seebeck coefficient by manipulating the density of states $g(E)$. While three-dimensional systems generally have a square root energy dependence for the density of states, lower-dimensional systems can provide a much higher density of states and, in turn, a higher Seebeck coefficient.

## 2.2 Seebeck Coefficient in Quantum-Wells

Knowing that the density of states impacts the Seebeck coefficient, we turn to a method of enhancing the density of states. Hicks and Dresselhaus[126] showed that the density of states near the Fermi level could be enhanced through quantum confinement, enhancing the Seebeck coefficient. This section will discuss the electron dispersion relations and the derivation of equations for the Seebeck coefficient, electrical conductivity, and thermal conductivity in two-dimensional and three-dimensional cases. Additionally, we will combine these relations to show how to calculate the thermoelectric figure of merit.

### 2.2.1 Electron Dispersion Relations

The electronic states of a three-dimensional bulk system are commonly approximated as parabolic bands, leading to the electron dispersion relation given in Eq. 2.7:

$$\epsilon_{3D}(k_x, k_y, k_z) = \frac{\hbar^2 k_x^2}{2m_x^*} + \frac{\hbar^2 k_y^2}{2m_y^*} + \frac{\hbar^2 k_z^2}{2m_z^*} \tag{2.7}$$

where $k$ is electron momentum in the subscript direction, $m^*$ is the effective electron mass in the subscript direction, and $\hbar$ is the reduced Planck's constant[126].

However, in two-dimensional systems, electrons are confined to a quantum well in the z-dimension. In this case, the third term of Eq. 2.7 reduces to that of a particle in a quantum well, as shown in Eq. 2.8:

$$\epsilon_{2D}(k_x, k_y, k_z) = \frac{\hbar^2 k_x^2}{2m_x^*} + \frac{\hbar^2 k_y^2}{2m_y^*} + \frac{n^2 \hbar^2 \pi^2}{2m_z^* a^2} \tag{2.8}$$

where $a$ is the quantum well depth and $n = 1, 2, ...$ is the quantum energy number.

The change in the last term results from the quantization of energy in the z-direction, which prevents electrons from occupying some low-energy states. Electrons are then forced to higher energy states near the Fermi level, enhancing the density of states. As suggested in Section 2.1, this enhancement leads to an enhanced Seebeck coefficient, as shown in Section 2.2.3.

### 2.2.2 Thermoelectric Properties in Three-Dimensional Materials

The process for deriving relations for the Seebeck coefficient, electrical conductivity, and thermal conductivity (and thus the thermoelectric figure of merit) based on electronic dispersion relations is well defined[139;140]. From this process and the bulk electronic dispersion relation in Eq. 2.7, relations for the Seebeck coefficient, electrical conductivity $\sigma$, and thermal conductivity $\kappa$, respectively, for conduction in a bulk material in the x-direction are shown in Eqs. 2.9, 2.10, and 2.11[126]:

$$S_{3D} = -\frac{k_B}{e}\left(\frac{5F_{3/2}(\zeta^*)}{3F_{1/2}(\zeta^*)} - \frac{\zeta}{k_BT}\right) \tag{2.9}$$

$$\sigma_{3D} = \frac{1}{2\pi^2}\left(\frac{2k_BT}{\hbar^2}\right)^{3/2}(m_xm_ym_z)^{1/2}F_{1/2}(\zeta^*)e\mu_x \tag{2.10}$$

$$\kappa_{e,3D} = \frac{\tau\hbar^2}{6\pi^2}\left(\frac{k_BT}{\hbar^2}\right)^{5/2}\left(\frac{m_ym_z}{m_x}\right)^{1/2}k_B\left(\frac{7}{2}F_{5/2}(\zeta^*) - \frac{25F_{3/2}^2(\zeta^*)}{6F_{1/2}(\zeta^*}\right) \tag{2.11}$$

where $k_B$ is the Boltzman constant, $\zeta$ is the chemical potential, $\tau$ is the relaxation time, $m_x$, $m_y$, and $m_z$ are the effective mass components in the $x$, $y$, and $z$-directions, respectively, $\kappa_e$ is the electronic thermal conductivity, and the Fermi-Dirac function $F_i$ is given by Eq. 2.12:

$$F_i(\zeta^*) = \int_0^\infty \frac{x^i dx}{\exp x - \zeta^* + 1} \tag{2.12}$$

where $\zeta^*$ is the reduced chemical potential defined in Eq. 2.13:

$$\zeta^* = \frac{\zeta}{k_BT} \tag{2.13}$$

### 2.2.3 Thermoelectric Properties in Two-Dimensional Materials

Similarly, relations for the Seebeck coefficient, electrical conductivity, and thermal conductivity, respectively, are obtained for a two-dimensional system conducting in the x-direction and shown in Eqs. 2.14, 2.15, and 2.16[126].

$$S_{2D} = -\frac{k_B}{e}\left(\frac{2F_1(\zeta^*)}{F_0(\zeta^*)} - \frac{\zeta}{k_BT} + \frac{n^2\hbar^2\pi^2}{2m_z^*a^2k_BT}\right) \tag{2.14}$$

$$\sigma_{2D} = \frac{1}{2\pi a}\left(\frac{2k_BT}{\hbar^2}\right)(m_x m_y)^{1/2} F_0(\zeta^*) e\mu_x \tag{2.15}$$

$$\kappa_{e,2D} = \frac{\tau\hbar^2}{4\pi a}\left(\frac{k_BT}{\hbar^2}\right)^2\left(\frac{m_y}{m_x}\right)^{1/2} k_B\left(3F_2(\zeta^*) - \frac{4F_1^2(\zeta^*)}{F_0(\zeta^*}\right) \tag{2.16}$$

Comparing Eq. 2.9 and Eq. 2.14, we can see that for all physically possible values of $a$ $S_{2D} \geq S_{3D}$ with the two being equal as quantum well depth approaches infinity. However, it is essential to note that Eq. 2.14 only holds for cases of quantum confinement, meaning $a$ must be on the order of the de Broglie wavelength of an electron ($\sim$10nm). The difference made by this additional term is visualized in Figure 2.1, which compares the results of each equation over a range of chemical potentials.

The three-dimensional case in Figure 2.1a shows an optimal value for the chemical potential that maximizes the power factor $S^2\sigma$. If we recall from Section 1.3.2, this occurs because of the inversely proportional relationship between the Seebeck coefficient and electrical conductivity. In the three-dimensional case, the Seebeck coefficient $S$ drives the power factor to zero at higher chemical potentials, limiting the improvement of the thermoelectric figure of merit.

Figure 2.1b shows the Seebeck value $S$ saturating to a non-zero value, because the last term in Eq. 2.14, $(n^2\hbar^2\pi^2)/(2m_z^* a^2 k_B T)$, is a constant. Whereas the first two terms from Eq. 2.14 cancel out as in the three-dimensional case, this constant value results in the Seebeck coefficient saturating to a non-zero value. Since the Seebeck coefficient saturates to a non-zero value, the power factor increases with rising conductivity.

### 2.2.4 Thermoelectric Figure of Merit Relations

To find the derived thermoelectric figure of merit, Eqs. 2.9, 2.10, and 2.11 for the three-dimensional, bulk case and Eqs. 2.14, 2.15, and 2.16 are plugged into Eq. 2.1. For the

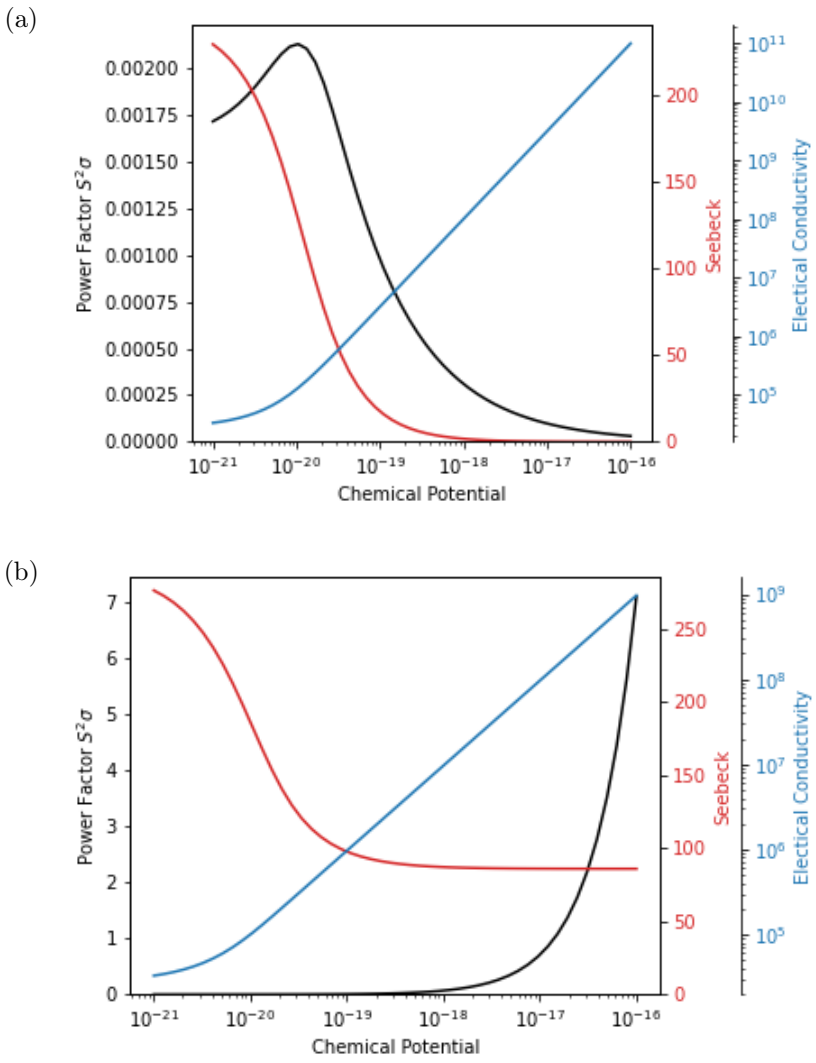


Figure 2.1: Theoretical plots of the Seebeck coefficient $S$ (red), electrical conductivity $\sigma$ (blue), and power factor $S^2\sigma$ (black) in a) a 3D semiconductor and b) a 2D semiconductor with respect to chemical potential based on equations derived by Hicks and Dresselhaus [126].

three-dimensional case, we obtain Eq. 2.17 [126]:

$$Z_{3D}T = \frac{\frac{3}{2}\left(\frac{5F_{3/2}(\zeta^*)}{2F_{1/2}(\zeta^*)} - \frac{\zeta}{k_BT}\right)^2 F_{1/2}(\zeta^*)}{\frac{1}{B} + \frac{7}{2}F_{5/2}(\zeta^*) - \frac{25F_{3/2}^2(\zeta^*)}{6F_{1/2}(\zeta^*)}} \tag{2.17}$$

where $B$ is defined in Eq. 2.18:

$$B = \frac{1}{3\pi^2}\left(\frac{2k_BT}{\hbar^2}\right)^{3/2}(m_xm_ym_z)^{1/2}\frac{k_B^2T\mu_x}{e\kappa_{ph}} \tag{2.18}$$

For the two-dimensional case, we obtain Eq. 2.19[126]:

$$Z_{2D}T = \frac{\left(\frac{2F_1(\zeta^*)}{F_0(\zeta^*)} - \frac{\zeta}{k_BT}\right)^2 F_0(\zeta^*)}{\frac{1}{B'} + 3F_2(\zeta^*) - \frac{4F_1^2(\zeta^*)}{F_0(\zeta^*)}} \tag{2.19}$$

where $B'$ is defined in Eq. 2.20:

$$B' = \frac{1}{2\pi a}\left(\frac{2k_BT}{\hbar^2}\right)(m_xm_y)^{1/2}\frac{k_B^2T\mu_x}{e\kappa_p} \tag{2.20}$$

Again, Eqs. 2.19 and 2.20 show that the effects of the quantum confinement will enhance the thermoelectric figure of merit $ZT$ compared to the three-dimensional case in Eqs. 2.17 and 2.18.

### 2.2.5 Section Summary

This section introduces the electron dispersion relations for bulk and two-dimensional systems. From these relations, we derived equations for both systems' Seebeck coefficient, electrical conductivity, and thermal conductivity. From these equations, we saw a saturation of the Seebeck coefficient to a non-zero value that was unique to the two-dimensional system. This saturation results in an improved thermoelectric figure of merit, which we also described.

## 2.3 Quantum-Confined Systems in MOSFETs

Most quantum-confined systems are physically small materials (superlattices[52;53;124;128;129] and nanowires[128;130–132]). However, this work uses the electrically isolated two-dimensional electron or hole gases (2DEGs or 2DHGs, respectively) in metal-oxide-semiconductor field-effect transistors (MOSFETs) to produce a low-dimensional system. MOSFETs are a good option because they have a well-characterized fabrication process and have been heavily engineered for reliability. The system also decouples the dominant electrical and thermal pathways, allowing for independent manipulation of the thermal conductivity and power factor. Furthermore, the Seebeck coefficient's saturation described in Section 2.2.3 somewhat decouples the components of the power factor (e.g., the Seebeck coefficient and electrical conductivity).

In this section, we outline the nomenclature and basic principles of MOSFETs. We discuss the standard voltages and currents that characterize MOSFET behavior before discussing the threshold voltage in depth. Finally, we discuss the drain-source saturation of the devices. We will limit discussion to enhancement-mode ("normally off") MOSFETs as they a predominately used, and depletion-mode ("normally on") MOSFETs will not be discussed.

### 2.3.1 MOSFET Nomenclature

Figure 2.2 shows how voltages and currents are defined in MOSFETs. Figure 2.2a shows the gate voltage $V_{gs}$, drain-source voltage $V_{ds}$, and the drain current $I_d$ in an n-type MOSFET, while Figure 2.2b shows the gate voltage $V_{sg}$, drain-source voltage $V_{sd}$, and the drain current $I_d$ in a p-type MOSFET. By these diagrams, all voltages and currents are positive, but it is common to refer to the gate voltage $V_{sg}$ in a p-type MOSFET as $V_{gs}$ with the operating voltage being negative.

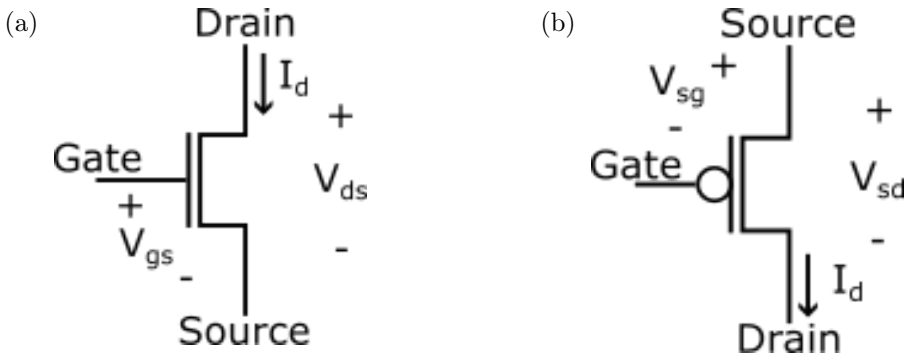


Figure 2.2: Schematics of (a) n-type and (b) p-type MOSFETs. Schematic shows the naming conventions of key voltages and currents.

### 2.3.2 MOSFET Operating Principles

When discussing MOSFET operation, visualization is helpful. To this end, we provide a cross-sectional view of a typical p-type MOSFET operating under strong inversion in Figure 2.3.

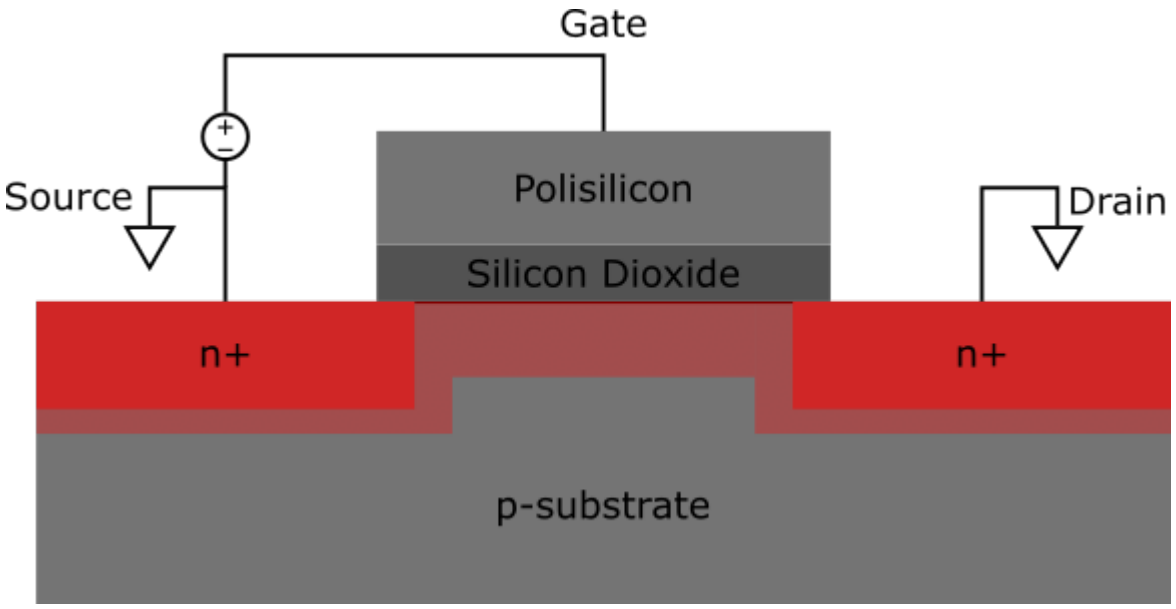


Figure 2.3: Diagram of an n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) operating under strong inversion.

The source and drain regions are the red n-doped wells underneath the source and drain terminals, typically doped around $10^{18}$ cm$^{-}3$. Most modern MOSFETs have polysilicon gates on a silicon dioxide ($SiO_2$) layer. The gate, oxide, and silicon form a MOS capacitor,

the "switch" to turn on the MOSFET. We also note that the body is predominately p-type, and the n-type channel, or depletion region, in transparent red underneath the gate is only present when a gate voltage above a threshold is applied. The gate voltage attracts the source and drain majority carriers (electrons in this n-type MOSFET) toward the gate and pushes away the substrate majority carriers (holes in this case)[141]. At equilibrium, with no gate voltage applied, the p-type substrate extends to the $SiO_2$ layer under the gate, leaving the p-type wells disconnected and the MOSFET off.

Typical values of interest for MOSFETs are the threshold voltage and saturation current, discussed in Sections 2.3.2.1 and 2.3.2.2, respectively.

#### 2.3.2.1 MOSFET Threshold Voltage

The threshold voltage is the minimum gate voltage required to form a conducting channel in a MOSFET. For most modern devices, the threshold value ranges from 0.5 V to 1 V. Mathematically, this threshold voltage $V_{th}$ can be determined using Eqs. 2.21 and 2.22 for n-type and p-type MOSFETs respectively[141;142]:

$$\text{For n-type MOSFET: } V_{th} = V_{fb} + 2|\phi_B| + \frac{\sqrt{2\epsilon_{Si} q N_A |2\phi_B|}}{C'_{ox}} \tag{2.21}$$

$$\text{For p-type MOSFET: } V_{th} = V_{fb} - 2|\phi_B| - \frac{\sqrt{2\epsilon_{Si} q N_D |2\phi_B|}}{C'_{ox}} \tag{2.22}$$

where $V_{fb}$ is the flatband voltage, $\epsilon_{Si}$ is the permittivity of silicon, $N_A$ and $N_D$ are the carrier concentration of acceptors and donors, respectively, $C'_{ox}$ is the gate-oxide capacitance, and $\phi_B$ is the bulk potential, defined in Eqs. 2.23 and 2.24:

$$\text{For n-type MOSFET: } \phi_B = \frac{k_B T}{q} \ln \frac{N_A}{N_i} \tag{2.23}$$

$$\text{For p-type MOSFET: } \phi_B = \frac{k_B T}{q} \ln \frac{N_D}{N_i} \tag{2.24}$$

where $k_B$ is the Boltzman constant, $T$ is the temperature, $q$ is the elementary charge, and $N_i$ is the intrinsic carrier concentration.

The gate-oxide capacitance surface density, typically measured in F/cm$^2$ is defined in Eq. 2.25:

$$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{2.25}$$

where $\epsilon_{ox}$ is the permittivity of the oxide and $t_{ox}$ is the thickness of the oxide.

#### 2.3.2.2 Drain-Source Current Saturation

For gate voltages above the threshold voltage, the MOSFET switches on, and electrons flow through the channel from the source to the drain under the influence of the drain-source voltage. For a constant gate-source voltage, increasing the drain-source voltage also increases the current when in the triode region.

Eventually, the drain-source voltage reaches a saturation voltage, which can be approximated by Eq. 2.26:

$$V_{ds,SAT} = V_{gs} - V_{th} \tag{2.26}$$

At and above this saturation voltage, the MOSFET is in the saturation region. In this region, the drain current saturates as the channel forms a pinch-off point, restricting the

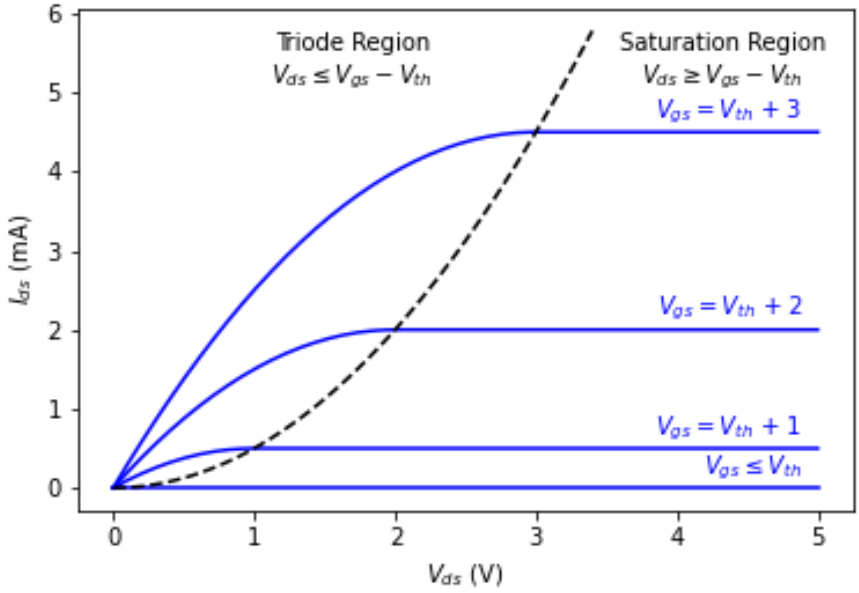


Figure 2.4: IV curve for an n-type MOSFET at several gate-source voltages.

flow of carriers. To visualize the relation between drain current and drain-source voltage, we reference Figure 2.4, which shows a standard IV curve for a MOSFET.

In the figure, we see the linear and saturation regions for the current for a MOSFET for a variety of gate voltages. As the MOSFET is off, we see no drain current for a gate voltage below the threshold voltage. As the gate voltage increases, we see the saturation value of the drain current increase. The dotted black line indicates the region where saturation begins. Equation 2.26 accurately predicts where this line intersects a given gate voltage.

### 2.3.3 Section Summary

In this section, we discussed the operation of MOSFETs. After beginning by defining the terminology, we discussed the operating principles. We introduced the threshold voltage as the voltage where a MOSFET turns on and provided equations for it in both p-type and n-type MOSFETs. We discussed the current saturation in the MOSFET channels and defined the saturation region where this occurs and the triode region where it does not. We also provided equations for approximating the saturation voltage of a MOSFET.

## 2.4 Chapter Summary

In this chapter, we introduced the electron dispersion relations for bulk and two-dimensional systems and derived equations for the thermoelectric properties in both systems. In these relations, we noted a saturation of the Seebeck coefficient to a non-zero value unique to the two-dimensional system. This results in an improved thermoelectric figure of merit.

We also discussed the operation of MOSFETs, as we use them to create our two-dimensional systems. We introduced basic concepts such as threshold voltage and saturation current. We also described how the gate voltage alters the MOSFET channel, creating a two-dimensional electron or hole gas (2DEG or 2DHG, respectively).

# Chapter 3

# Device Design and Fabrication

In this chapter, we discuss the design of the MOSFET and diffusion devices and their design considerations. To this end, we discuss the busFET structure used in MOSFET devices and the resistor selection and placement. We then discuss the diffused substrate of the diffusion devices and their resistors. Finally, we discuss the fabrication processes of the devices. While we use complementary metal-oxide-semiconductor (CMOS) guidelines, we give specifics on the release of the cantilevers of test devices.

## 3.1 MOSFET Device Design

We designed devices for experiments according to CMOS guidelines[141] to ensure compatibility with existing processes and the reliability of devices. We used MOSFETs, which would create the quantum-confined, two-dimensional electron and hole gases (2DEGs and 2DHGs, respectively) as the building blocks of our devices. For testing, we added heating and temperature-sensing resistors to devices. Figure 3.1 shows the final layout of the device. Probe landing pads are located out of the image to the right.

Information in this chapter is also disseminated in another publication by the author[143]

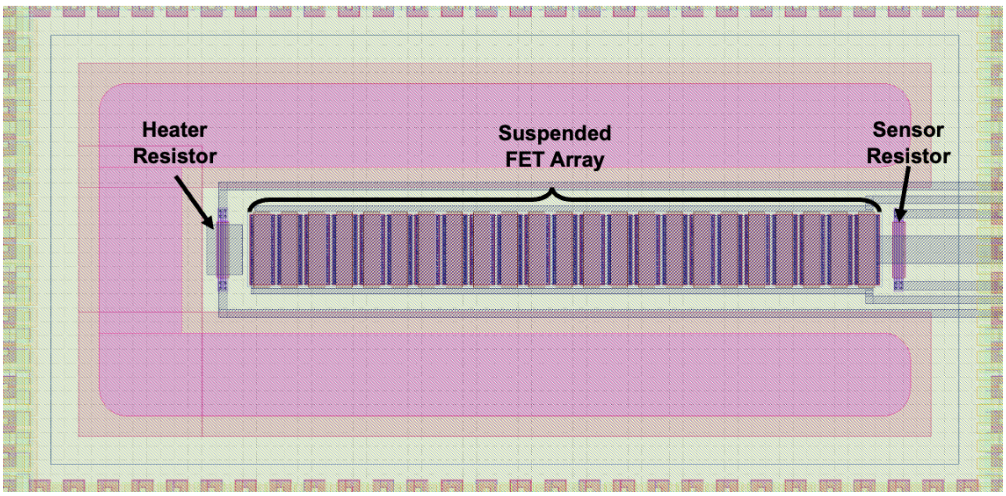


Figure 3.1: Schematic of device layout illustrating placement of the heater and sensor resistors and busFET array in MOSFET devices.

### 3.1.1 busFET Structure

We desired a longer-length device because it would allow a more significant temperature differential between ends and, thus, a more measurable thermoelectric voltage. However, CMOS guidelines limit the dimensions of MOSFETs. To overcome these limitations, we used a busFET structure. To form the busFET, we linked adjacent MOSFETs' source and drain terminals. All MOSFETs shared a gate. The busFET uses twenty-three transistors with a single channel length of 5.95$\mu$m and a width of 25$\mu$m, resulting in a W/L ratio of approximately 4.2. Each MOSFET has a unit cell length of 10$\mu$m, yielding a busFET 230$\mu$m long, as shown in Figure 3.1.

### 3.1.2 Heating and Temperature Measurement Resistors

To induce a temperature gradient and measure the local temperature on the device, we placed resistors at the ends of each device to establish the local temperatures. We used 30$\mu$m by 5$\mu$m polysilicon single event upset (SEU) resistors because they are highly sensitive to temperature making them ideal for measuring it. While polysilicon resistors are very predictable, SEU polysilicon resistors have relatively inconsistent resistance values because of the variance in the additional processing steps. However, we mitigate the inconsistent resistance values by

calibrating device resistors individually.

## 3.2 Diffusion Device Design

Like the MOSFET devices, we fabricated the diffusion devices to CMOS guidelines[141] to ensure compatibility with existing microfabrication processes. In diffusion devices, we dope the substrate and can measure bulk silicon properties. These devices form a control group for the MOSFET devices. Like the MOSFET devices, they also have heating and temperature-sensing resistors. The layout and dimensions are the same as in Figure 3.1 except the suspended FET array is replaced with doped silicon.

### 3.2.1 Doped Substrate

In the place of the suspended FET array of the MOSFET devices, the diffusion devices have a doped silicon substrate. Here, we dope the silicon to the same level as the MOSFET channel under strong inversion. These diffusion devices essentially function as resistors rather than transistors, with the "source" and "drain" regions having the same polarity as the body. With no field effects, these devices are a means to measure the bulk properties of our device for comparison against the MOSFET devices. In addition to measuring bulk properties, the devices allow us the advantage of normalizing away systemic errors in the measurements to easily see the difference quantum confinement makes in our MOSFET devices.

### 3.2.2 Heating and Temperature Measurement Resistors

Like the MOSFET devices, we placed resistors at each end of the device to establish the local temperatures. For uniformity, we used identical SEU resistors in both types of devices. These SEU resistors are highly sensitive to temperature, making them ideal for our purpose. As in the MOSFET device, the diffusion device resistors are $30\mu$m by $5\mu$m.

## 3.3 Fabrication

Using a shared wafer program, we fabricated the MOSFET and diffusion devices to CMOS guidelines. We then had them released to reduce the overall thermal conductivity. We describe the release and justification in more detail in Section 3.3.1. Figure 3.2 shows a scanning electron microscope image of a fabricated device. (SEM).

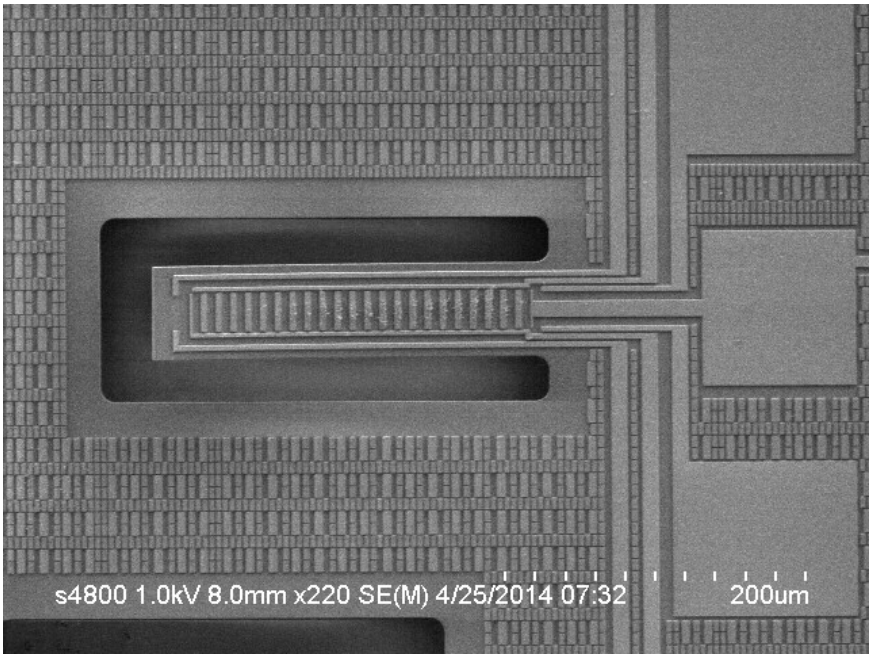


Figure 3.2: Scanning electron microscope (SEM) images of fabricated MOSFET devices.

We see the etched area around the cantilever, as well as a few of the probe landing pads. Resistors can be seen at the ends of the busFET.

### 3.3.1 Release of Devices

To reduce the thermal pathway cross-section, we released both MOSFET and diffusion devices to form cantilevers by etching the buried-oxide (BOX) layer under the device. This etching isolated the device layer from the BOX layer and handle layer of the wafer, achieving the desired elimination of their thermal contribution by reducing the overall cross-sectional area of the devices. The process is outlined as follows:

1. We spin a protective layer on top of the devices and pattern it with windows open to the area surrounding the devices.

2. We wet etch the device layer silicon exposed in the windows using TetraMethylAmmonium Hydroxide (TMAH).

3. We then etch the exposed BOX layer using diluted hydrofluoric acid, separating the device layer from the handle of the wafer.

4. We then remove the protective layer.

## 3.4 Chapter Summary

This chapter discussed the device design, touching on the busFET structure used. We outlined the resistor type selection and placement on MOSFET devices. We discussed the design of the diffusion devices, including the doped substrate and resistors. Finally, we discussed the device fabrication process, which followed CMOS guidelines. Finally, we gave specifics on the release of the cantilevers of test devices.

# Chapter 4

# Experiment and Measurement Setup

In this chapter, we show the novel methodology used to study CMOS-compatible thermoelectrics and reliably obtain the thermoelectric figure of merit. Whereas most studies of CMOS-compatible thermoelectric materials only report the Seebeck coefficient [133–136], here we provide a path to measuring all constitutive parts of the thermoelectric figure of merit allowing for its calculation. The normalization methodology is particularly important, helping to negate systemic measurement errors.

We performed three separate measurement processes on devices to determine the thermoelectric properties. First, we use a temperature-resistance calibration (TRC) procedure to produce the calibration curves used to determine local temperatures on devices. Then, to determine electrical conductivity, we perform a current-voltage (IV) characterization. Next, we perform a thermoelectric characterization to determine the Seebeck coefficient and thermal conductivity. Following, we discussed the error propagation in data processing. Finally, we discussed the automation of the experiments and data acquisition process.

We performed these experiments on metal-oxide-semiconductor field-effect transistor (MOSFET) and diffusion devices. However, each procedure varies slightly because of the lack

Information in this chapter is also disseminated in another publication by the author [143]

of a gate on the diffusion devices. This chapter outlines each device type's processes and data processing to determine the thermoelectric properties.

## 4.1 Temperature-Resistance Calibration

We perform a temperature-resistance calibration (TRC) to calibrate the resistors used to determine the temperature in later experiments. The devices are set on a probe station with a thermocouple and the Kapton heater, as shown in Figure 4.1.

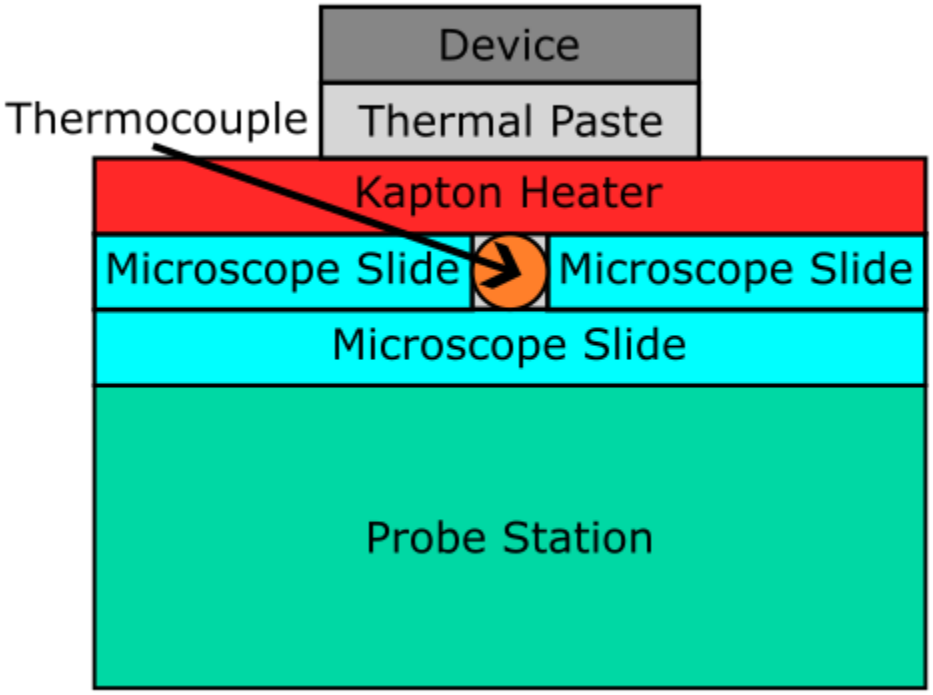


Figure 4.1: Cross-sectional view of temperature resistor calibration (TRC) measurement. Thermal paste ensures good contact between the device and the Kapton heater. The thermocouple is placed next to the Kapton heater between microscope slides to prevent an uneven surface. The gap between the thermocouple and Kapton heater is filled with thermal paste. The whole setup rests on a probe station.

### 4.1.1 Instrumentation and General Procedure

We placed a thermocouple below the Kapton heater for both MOSFET and diffusion devices. We surrounded the thermocouple with microscope slides to provide a flat surface for the Kapton heater and device. We place the device on the Kapton heater with a thermal paste to ensure good thermal conduction between the two. Figure 4.2 shows the TRC instrumentation for MOSFET devices.

In the experiment, we used a Kapton heater, a thermocouple, two digital multimeters (DMMs), a source meter (SM), and a power supply (PS). The power supply powers the Kapton heater and heats the device at each of the values shown in Table 4.1. A DMM measures the thermocouple output used to determine the system's temperature. The remaining DMM and the source meter measure the resistances. While we could replace the source meter with a simple DMM for this experiment, it is necessary to apply current to the heater resistor in later characterizations. Rather than switching instrumentation between experiments, we simply use the source meter as a DMM would be for the TRCs.

Table 4.1: Parameters for temperature resistance calibration of MOSFET and diffusion devices.

| Parameter | Start | Stop | Step Size |
|---|---|---|---|
| Kapton Heater Voltage | 0.0 V | 5.5 V | 0.5 V |

We measure the thermocouple voltage, heater resistance, and sensor resistance for various Kapton heater voltages, allowing us to calibrate the resistors over a temperature range. We use the same procedure for the diffusion devices. Figure 4.3 shows the setup.

### 4.1.2 Transient Temperature Response

Because thermal energy transfer is relatively slow, we did preliminary testing to determine the time taken to reach thermal equilibrium. To do so, we measured the transient response of the resistors and the thermocouple in response to a step input in heater power. Figure 4.4 shows the results.

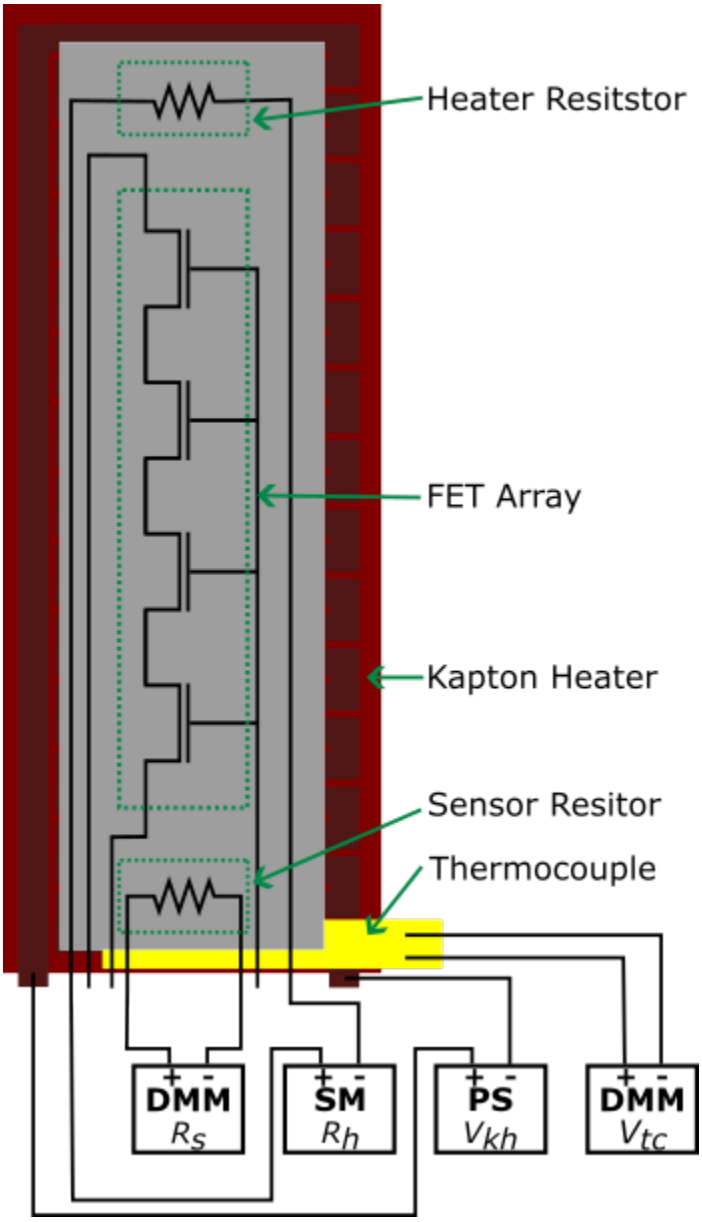


Figure 4.2: Schematic of the experimental setup for a MOSFET device's temperature-resistance calibration (TRC) measurement. The device sits on a Kapton heater. A digital multimeter (DMM) measures the resistance of the sensor resistor $R_s$. A source meter (SM) measures the resistance of the heater resistor $R_h$. A power supply (PS) supplies voltage $V_{kh}$ to the Kapton heater. Finally, a DMM measures the output voltage $V_{tc}$ of the thermocouple.

We see that the resistance values track the system temperature change well, and we selected a time of fifteen minutes for the system to get up to temperature. While not entirely at steady state, the resistors track well enough, and the time allows for adequate temperature change.

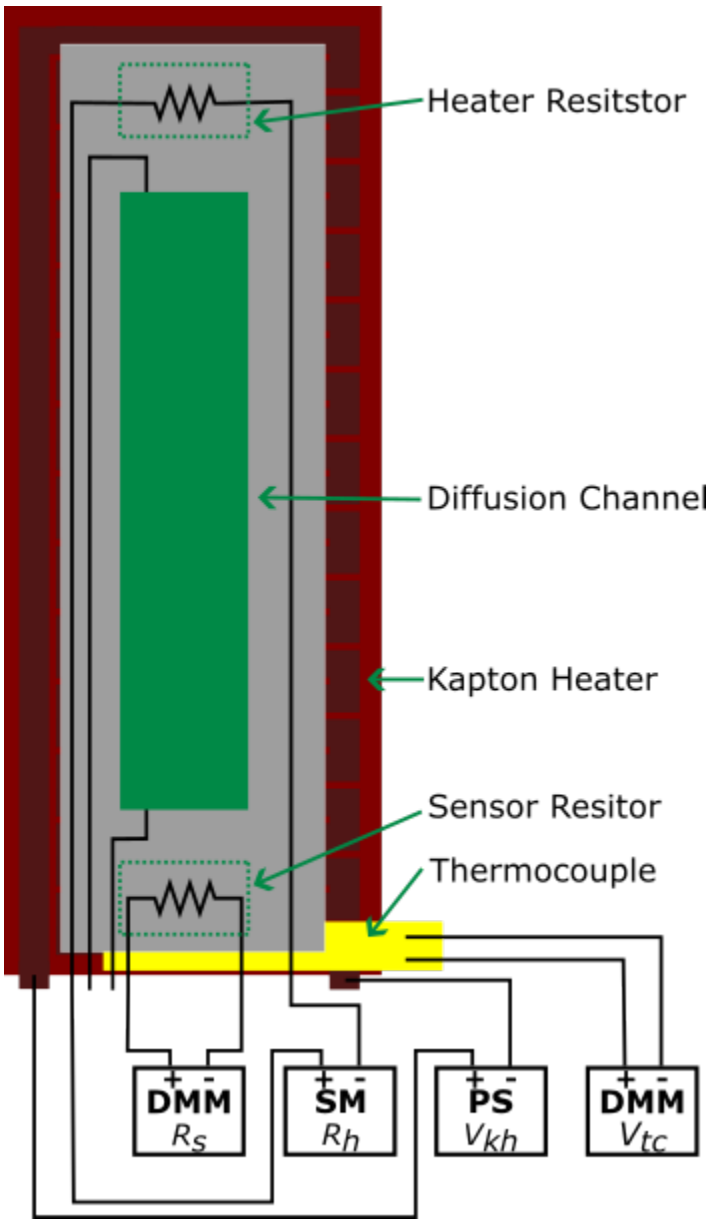


Figure 4.3: Schematic of the experimental setup for a MOSFET device's temperature-resistance calibration (TRC) measurement. The device sits on a Kapton heater. A digital multimeter (DMM) measures the sensor resistance $R_s$. A source meter (SM) measures the heater resistance $R_h$. A power supply (PS) supplies voltage $V_{kh}$ to the Kapton heater. Finally, a DMM measures the output voltage $V_{tc}$ of the thermocouple.

## 4.2 Current Voltage Characterization

We perform the current-voltage characterization to characterize the electrical conductivity of the MOSFET channel and the diffusion devices. We characterize each device with several

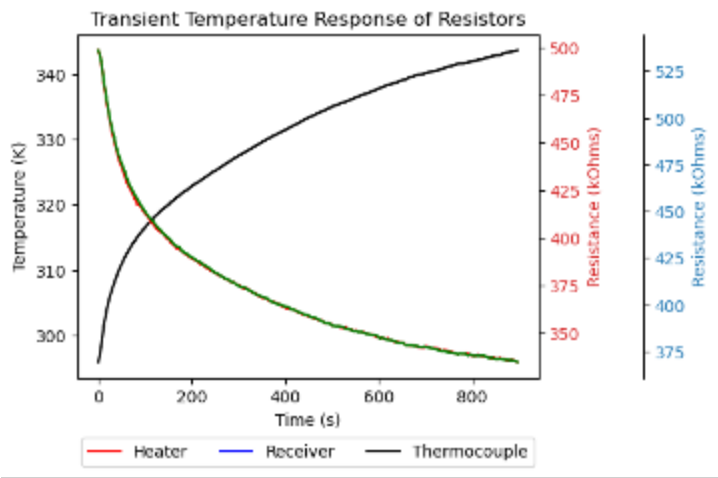


Figure 4.4: Transient response of resistors to a step change in temperature. Results show that temperatures across the device track well and without delay during TRC measurements.

induced temperature gradients, though results suggest the effects of temperature are minimal.

### 4.2.1 Instrumentation and General Procedure

For the current-voltage characterization, we use slightly different procedures for MOSFET and diffusion devices due to the additional gate voltage variable in the MOSFET case. We outline the procedures for each device in the following sections.

#### 4.2.1.1 MOSFET Devices

Figure 4.5 shows the instrument setup for the MOSFET devices.

The measurement uses a digital multimeter (DMM), two source meters (SMs), and a power supply (PS). The DMM measures the resistance of the sensor resistor. We use this resistance and the TRC to determine the local temperature. The first source meter applies a drain-source voltage while measuring the current. The power supply varies the gate voltage. Finally, the second source meter applies a current to the heater resistor, heating the device, and also measures the resistance of the heater resistor. We use this resistance and the TRC to determine the local temperature.

Figure 4.6 shows a flow chart of the current-voltage measurement procedure for MOSFET

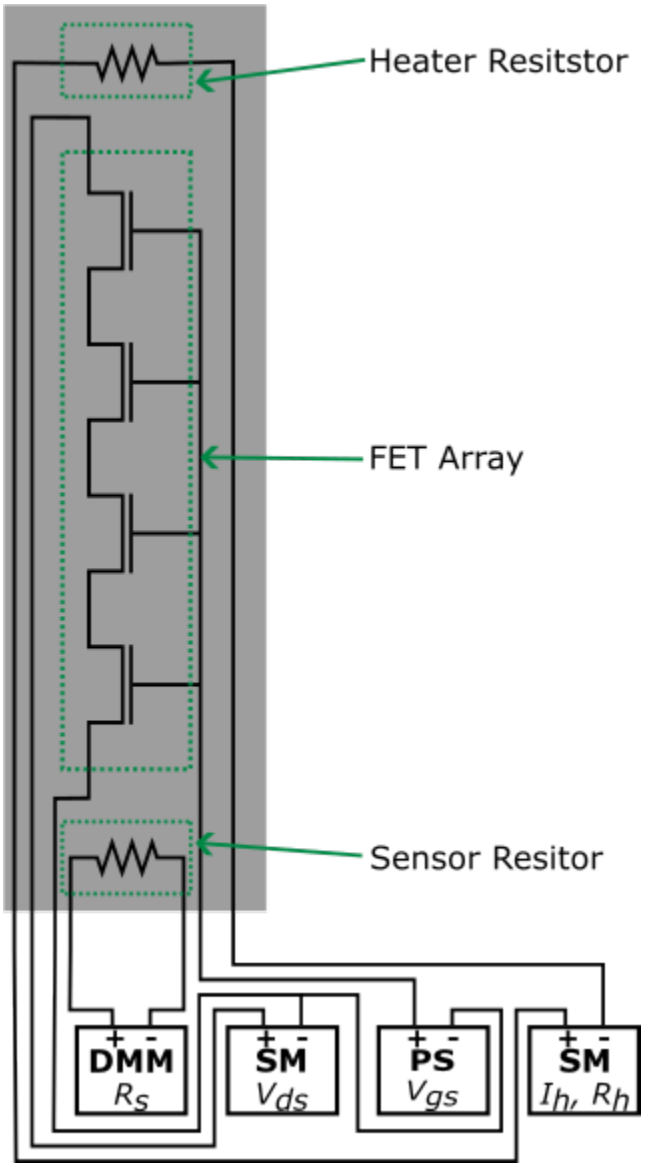


Figure 4.5: Schematic of the experimental setup for the current-voltage (IV) and thermoelectric measurements of a MOSFET device. A digital multimeter (DMM) measures the sensor resistance $R_s$. A source meter (SM) applies the drain-source voltage $V_{ds}$ and measures the drain current $I_d$. A power supply (PS) supplies the gate-source voltage $V_{gs}$. A final source meter applies the heater resistor current $I_h$ and measures the resistance of the heater resistor $R_h$ during the experiment.

devices.

To start, we apply a current to the heater resistor to heat the device. Then, after the device reaches thermal equilibrium, we measure the heater and sensor resistances. These will be used with the TRC to determine local temperatures and the temperature gradient

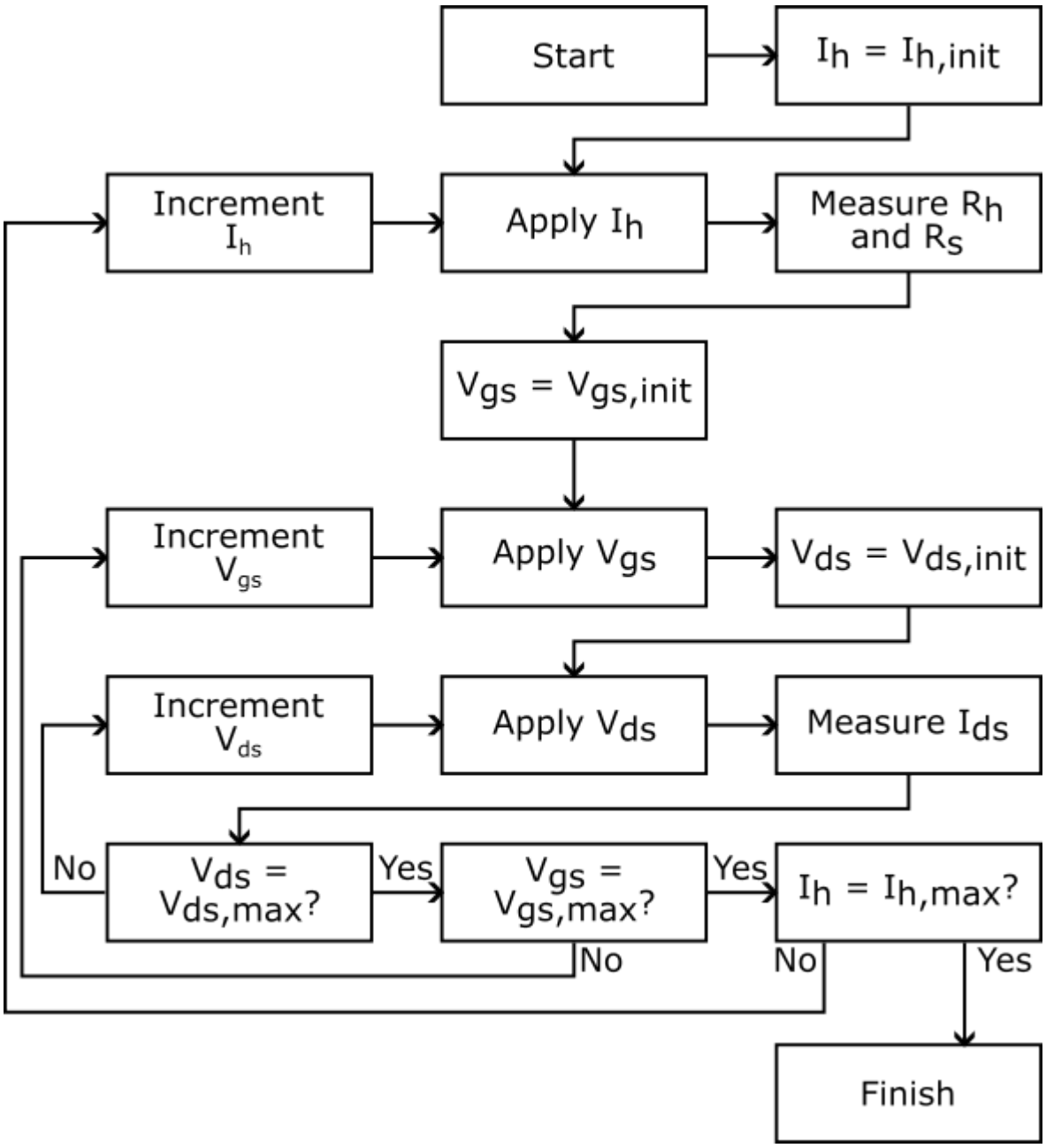


Figure 4.6: Flow chart detailing the current-voltage characterization of a MOSFET device. Heater current $I_h$, gate voltage $V_{gs}$, and drain-source voltage $V_{ds}$ are swept while heater resistance $R_h$, sensor resistance $R_s$, and drain-source current $I_{ds}$ are measured.

across the device. After the resistance measurements, we cycle through the gate voltages of interest, applying a range of drain-source voltages. For each drain-source voltage, we measure the drain-source current. We repeat this process, measuring the drain current for each drain-source voltage at each gate voltage. Once characterized for every gate voltage

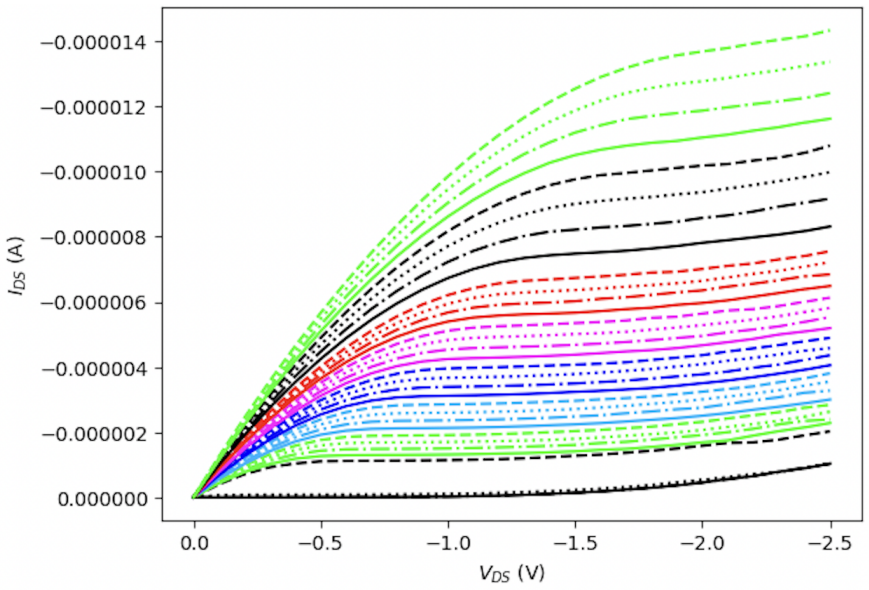


Figure 4.7: Example IV curve from a p-type MOSFET device for gate voltages from 0 V to 5 V in 0.1 V increments.

at that heater current, we increment the heater current and repeat the process. Figure 4.7 shows results for a p-type MOSFET device at a single heater current with drain-source and gate-source voltages from Table 4.2.

Table 4.2: Parameters for current voltage characterization of MOSFET and diffusion devices.

| Parameter | Start | Stop | Step Size |
|---|---|---|---|
| Heater Current | 0.0 $\mu$A | 70 $\mu$A | 3.5 $\mu$A |
| Drain Source Voltage | 0.0 V | 2.5 V | 0.1 V |
| Gate Source Voltage[a] | 0.0 V | 5.0 V | 0.1 V |

[a]MOSFET devices only.

#### 4.2.1.2 Diffusion Devices

Because there is no gate, the measurement simplifies for diffusion devices. Figure 4.8 shows the instrument setup for the diffusion devices.

We use a digital multimeter (DMM) and two source meters (SMs) for the measurement. The DMM measures the sensor resistance. We use this resistance and the TRC curves to determine the local temperature. The first source meter applies a drain-source voltage while

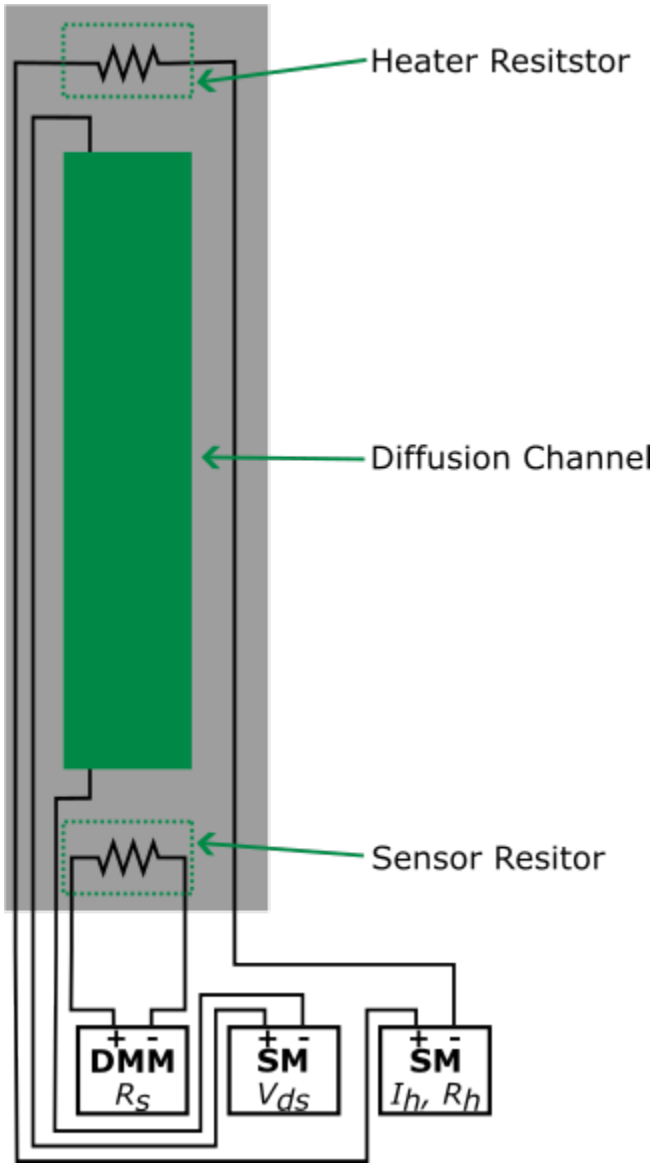


Figure 4.8: Schematic of the experimental setup for the current-voltage (IV) and thermoelectric measurements of a MOSFET device. A digital multimeter (DMM) measures the sensor resistance. A source meter (SM) applies the drain-source voltage $V_{ds}$ and measures the drain current $I_d$. A final source meter applies the heater resistor current $I_h$ and measures the heater resistance $R_h$ during the experiment.

measuring the drain current. Finally, the second source meter applies a current to the heater resistor, heating the device. The second source meter also measures the heater resistance. We use this resistance and the TRC curves to determine the local temperature.

Figure 4.9 shows a flow chart of the current-voltage measurement procedure for diffusion devices.

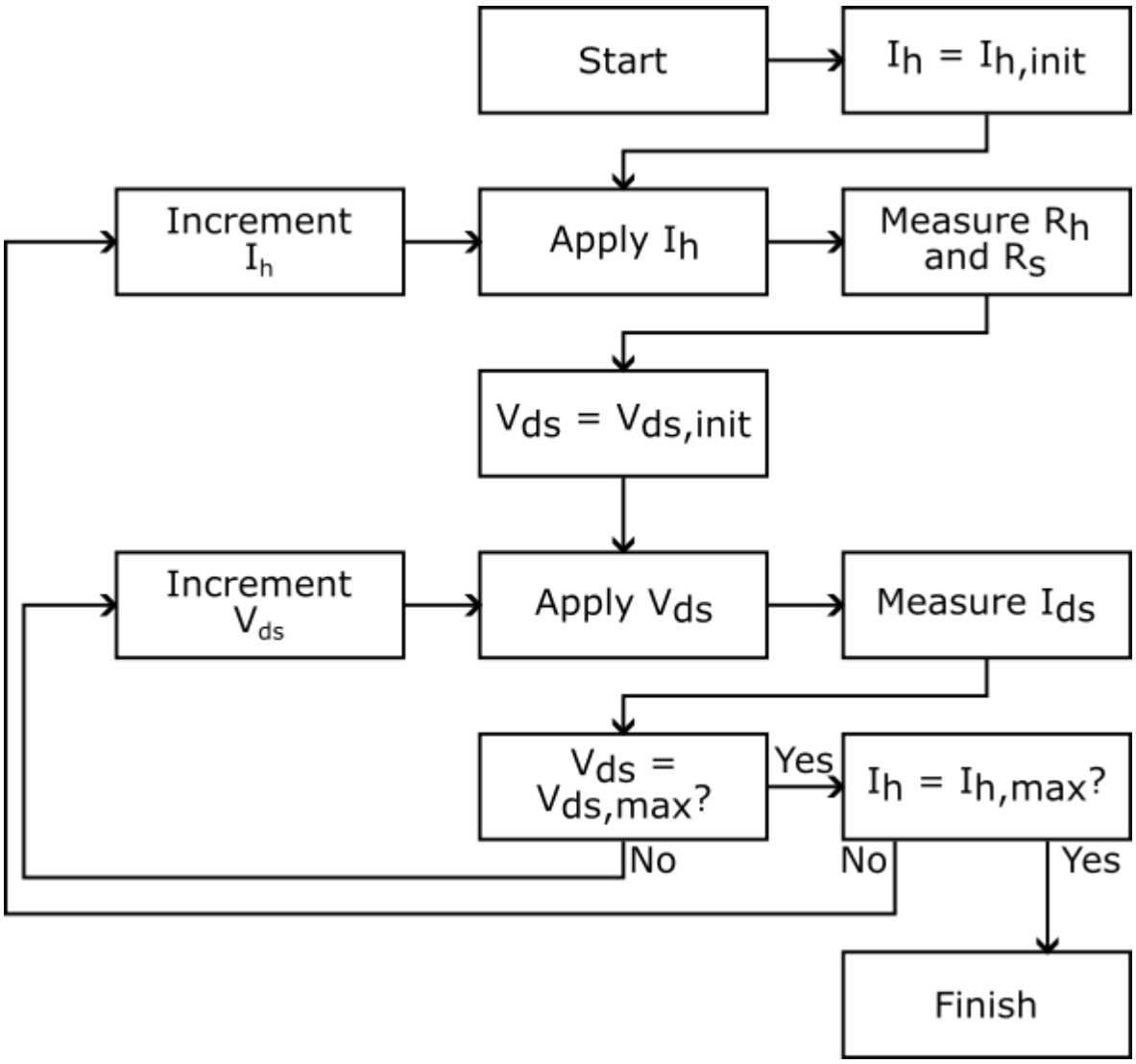


Figure 4.9: Flow chart detailing the current-voltage characterization of a diffusion device. Heater current $I_h$ and drain-source voltage $V_{ds}$ are swept while heater resistance $R_h$, sensor resistance $R_s$, and drain-source current $I_{ds}$ are measured. There is no gate voltage $V_{gs}$ to sweep.

To start, we apply a current to the heater resistor to heat the device. Then, after the device reaches thermal equilibrium, we measure the resistances of the heater and sensor resistors. We use these with the TRC to determine local temperatures and the temperature gradient across the device. Once we establish the temperature, we apply a range of drain-source voltages. For each drain-source voltage, we measure the drain current. Once characterized for every drain-source voltage $V_{ds}$, we move to the following heater current. Again, we use the parameters in Table 4.2, except for the gate voltage, which is not needed for diffusion devices.

## 4.3 Thermoelectric Characterization

We perform the thermoelectric characterization to obtain the Seebeck coefficient and thermal conductivity. We characterize each device for various temperature differentials and the MOSFET devices for several gate voltages.

### 4.3.1 Instrumentation and General Procedure

Because the MOSFET devices have gates, both devices undergo slightly different thermoelectric characterization processes. We detail the procedures for each in the following sections.

#### 4.3.1.1 MOSFET Devices

The MOSFET devices use the same thermoelectric characterization setup as the current-voltage characterization shown in Figure 4.5. Again, this setup uses a digital multimeter (DMM), two source meters (SMs), and a power supply (PS). The DMM measures the sensor resistance. We use this resistance and the TRC curve to determine the local temperature. The first source meter measures the drain-source voltage, and the power supply varies the gate voltage. Finally, the second source meter applies a current to the heater resistor, heating the device. The second source meter also measures its resistance. We use this resistance and the TRC curve to determine the local temperature.

Figure 4.10 shows a flow chart of the thermoelectric measurement procedure for MOSFET devices.

To start, we apply a heater current and wait for the device to reach thermal equilibrium. Then, we measure heater resistance and sensor resistance so we can determine temperature can with the TRC curves. Next, we apply a gate voltage and measure the drain-source voltage. Here, the drain-source voltage is the Seebeck voltage, and we will use it with the temperature differential to determine the Seebeck coefficient. We then increment the gate

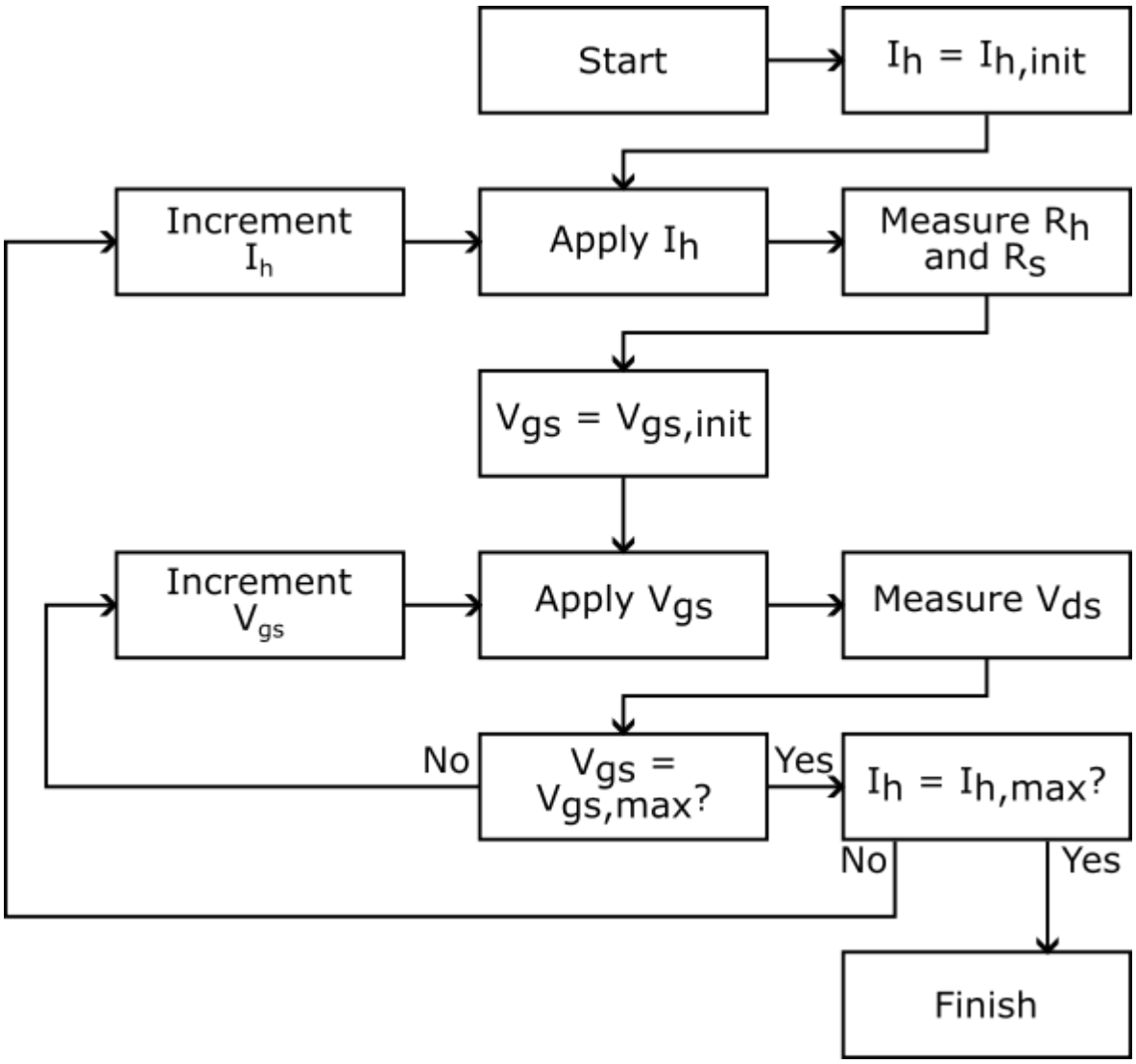


Figure 4.10: Flow chart detailing the thermoelectric characterization of a MOSFET device. Heater current $I_h$ and gate voltage $V_{gs}$ are swept while heater resistance $R_h$, sensor resistance $R_s$, and drain-source voltage $V_{ds}$ are measured.

voltage and repeat the measurement at the same heater current until we reach the maximum gate voltage. After this, we increment the heater current and cycle through the gate voltages again for all of the parameters listed in Table 4.3.

#### 4.3.1.2 Diffusion Devices

For diffusion devices, the measurement simplifies because of the lack of a gate. Again, we use the same setup as the current-voltage characterization shown for the diffusion devices in

Table 4.3: Parameters for thermoelectric characterization of MOSFET and diffusion devices.

| Parameter | Start | Stop | Step Size |
|---|---|---|---|
| Heater Current | 0.0 $\mu$A | 70 $\mu$A | 3.5 $\mu$A |
| Gate Source Voltage[a] | 0.0 V | 5.0 V | 0.1 V |

[a]MOSFET devices only.

Figure 4.8.

This setup uses a digital multimeter (DMM) and two source meters (SMs). The DMM measures the resistance of the sensor resistor. We use this resistance and the TRC curves to determine the local temperature. The first source meter measures the drain-source voltage. Finally, the remaining source meter applies a current to the heater resistor, heating the device. The remaining source meter also measures its resistance. We use this resistance and the TRC curves to determine the local temperature.

Figure 4.11 shows a flow chart of the thermoelectric measurement procedure for diffusion devices.

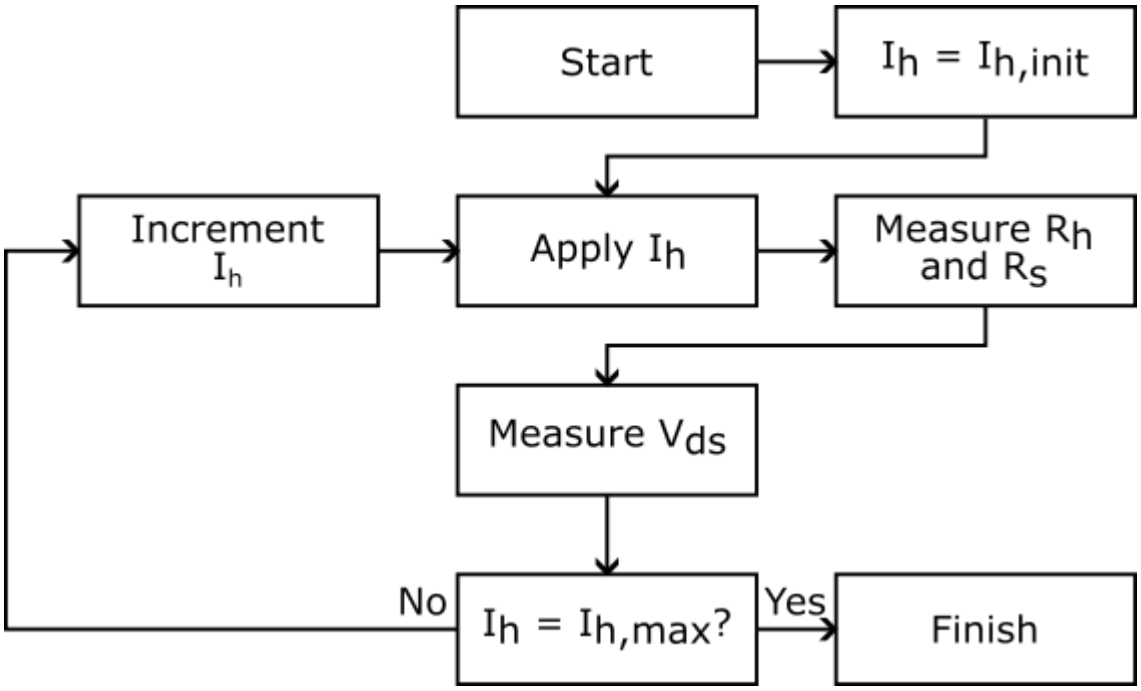


Figure 4.11: Flow chart detailing the thermoelectric characterization of a diffusion device. Heater current $I_h$ is swept while heater resistance $R_h$, sensor resistance $R_s$, and drain-source voltage $V_{ds}$ are measured. There is no gate voltage $V_{gs}$ to sweep.

To start, we apply a heater current and wait for the device to reach thermal equilibrium. Next, we measure heater and sensor resistance are measured so we can determine local temperature with the TRC curves. Then, we measure the drain-source voltage. Here, the drain-source voltage is the Seebeck voltage, and we will use it with the temperature differential to determine the Seebeck coefficient. After this, we increment the heater current and measure the drain-source voltage until reaching the maximum heater current. Again, we use the parameters in Table 4.3, except for the gate voltage, which is not needed for diffusion devices.

## 4.4 Data Processing

In the conducted experiments, we directly measured several values. We take resistance values at various temperatures in the temperature resistance calibration (TRC). During the IV characterizations, we measure the drain-source currents and resistances at various heater currents, drain-source voltages, and (in the case of MOSFET devices) gate voltages. Finally, the thermoelectric characterizations measure the drain-source voltage and resistances at various heater currents and (in the case of MOSFET devices) gate voltages. In the following sections, we outline the processing of this directly measured data to determine the Seebeck coefficient, electrical conductivity, and thermal conductivity and the normalization methods used to isolate the quantum confinement effect in the MOSFET devices.

### 4.4.1 Temperature Resistance Calibration

The TRC produces the calibration curves we use to calculate local device temperature based on the resistances we measure during the IV and thermoelectric characterizations. Because single-event upset (SEU) resistors have a second-order relationship with temperature, we fit the data to a second-order polynomial $R(T)$. Figure 4.12 shows the results and fit for the heater and sensor resistors on a single device.

Note that even on the same device, resistors have different characteristics. As discussed

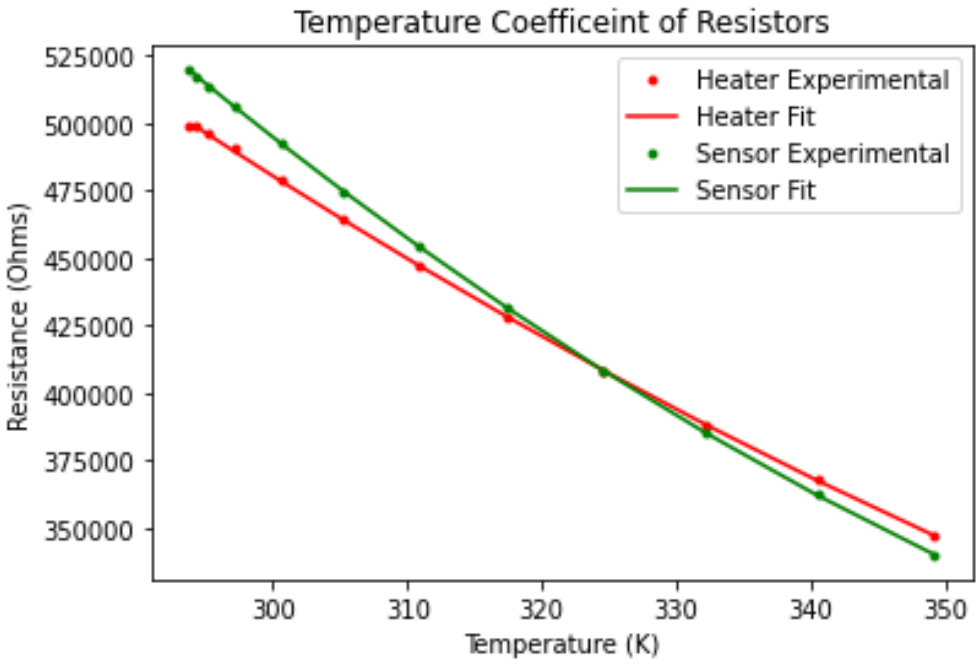


Figure 4.12: A plot of temperature resistance calibration measurement and second-order fit to data of a single device.

in Section 3.1.2, we expect a significant variation between resistors because of the SEU design. In Figure 4.12, we also see the upside of having significant fluctuation with temperature change, which allows small temperature changes to be easily measured.

We later use the fitted second-order polynomial to determine the temperature from resistance. However, as the polynomial defines resistance as a function of temperature, we use iterative solving methods. Further, the results are constrained to prevent any extrapolation from the measured data, ensuring that the solution found correctly represents the physical system.

### 4.4.2 Extracting Electrical Conductivity

To extract the electrical conductivity, we use the data from the IV characterization and device geometry. First, we use the drain-source current and voltage to determine conductance, the inverse of resistance, with Ohms law, seen in Eq. 4.1[141]:

$$G = \frac{1}{R} = \frac{I}{V} \tag{4.1}$$

where $G$ is conductance, $R$ is resistance, $I$ is current, and $V$ is voltage. The conductance value is essentially the slope of the triode region of the IV curves for MOSFETs. The triode region is also where the devices function as the thermoelectric voltage is typically low. Diffusion devices exhibit no saturation, and we use a linear fit to the IV curve.

We then convert the extrinsic property conductance to the intrinsic property electrical conductivity using Eq. 4.2:

$$\sigma = G\frac{L}{A} \tag{4.2}$$

where $L$ is the device length and $A$ is the cross-sectional area, which we define for our devices in Eq. 4.3:

$$A = wd \tag{4.3}$$

where $w$ is the width and $d$ is the depth of the conductance area.

### 4.4.3 Extracting Seebeck Coefficient

We calculate the Seebeck coefficient from the thermoelectric characterization data and the temperature calibration curves from the TRC. Using the TRC curves, we convert the resistances from the thermoelectric characterization to temperatures. We then use these temperatures to determine the temperature across the device $\Delta T_{ds}$. Finally, with the measured drain-source voltages $V_{ds}$, we determine the Seebeck coefficient using Eq 4.4[131]:

$$S = -\frac{\Delta V_{ds}}{\Delta T_{ds}} \tag{4.4}$$

### 4.4.4 Extracting Thermal Conductivity

We extract the thermal conductivity from the thermoelectric characterization data and the temperature calibration curves from the TRC. Using the TRC curves, we convert the resistances from the thermoelectric characterization to temperatures. We then determine the temperature across the device $\Delta T_{ds}$. We also determine the power across the heater using the heater current and heater resistance through Eq. 4.5:

$$P_h = I_h^2 R_h \tag{4.5}$$

We assume that Joule heating converts all of this power to thermal energy and that losses via convection are negligible. Furthermore, heat can only be conducted across the device since the device is on a cantilever. Therefore the power to the heater is analogous to the heat flux across the device ($P_h = q$). Under these assumptions, we calculate thermal conductance $K$ using the heat equation shown in Eq. 4.6:

$$K = \frac{P_h}{\Delta T} \tag{4.6}$$

Finally, we convert the extrinsic property thermal conductance to the intrinsic property thermal conductivity using Eq. 4.7:

$$\kappa = K\frac{L}{A} \tag{4.7}$$

where cross-sectional area $A$ is given by Eq. 4.3. This time, however, the thermal path,

which is the whole device layer, determines the depth.

To verify our early assumptions, we compare the calculated thermal conductivity of our diffusion devices to the value of similarly doped silicon[144]. Our assumptions are validated by finding both values to be 48 W/mK at 300 K. Our assumptions are further validated by matching the thermal conductivities of the MOSFETs to those found in literature[145].

### 4.4.5 Normalization Methodology

After extracting the components of the thermoelectric figure of merit $ZT$, MOSFET devices are normalized to diffusion devices to isolate the effects of quantum confinement. Because of the difference in dominant thermal and electrical pathways, we take special care in the normalization process, normalizing devices to those fabricated on the same die to minimize any differences do to processing or spatial dependencies of properties.

In addition to isolating the effects of quantum confinement, normalization also eliminates any system error in the measurements. For instance, because the device resistors are some distance from the ends of the actual thermoelectric devices and the temperature profile is not strictly linear between the resistors, as shown in Figure 4.13, the temperature gradient is almost certainly overestimated equally for both devices. However, we overcome this error by normalizing, which cancels out and correction factor needed to adjust the temperature differential.

Because our MOSFETs and diffusion devices are identical, aside from the doping of the substrate, the thermal profiles of both will be the same. Furthermore, the diffusion devices are essentially bulk silicon, which has well-known thermoelectric properties. Since the properties are well-known, it provides an additional point to verify the finding on our MOSFET devices. This method is an improvement over current methodologies[131], which rely on correction factors.

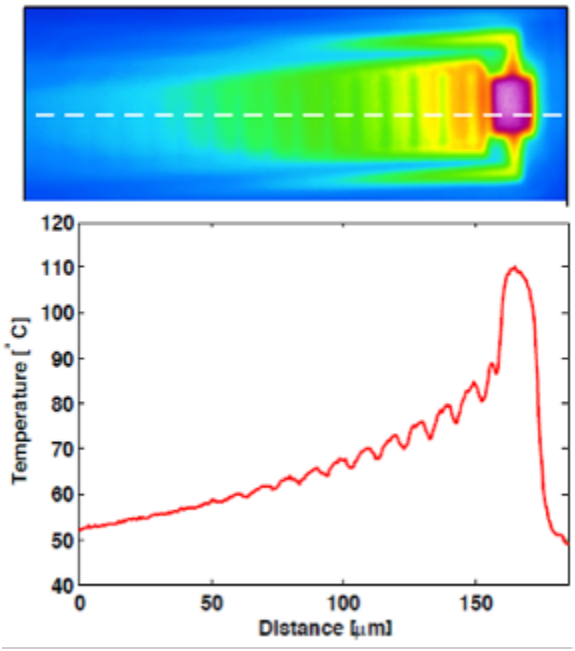


Figure 4.13: The temperature profile of a device heated using the heater resistor measured using infrared thermography.

#### 4.4.5.1 Normalization of Electric Properties

The shape and carrier concentration of the electrical pathway determines the Seebeck coefficient and electrical conductivity. When isolating the effects of quantum confinement in the MOSFET devices, we should look to compare similar electrical pathways. Figure 4.14 shows the electrical pathway of MOSFET and diffusion devices.

In Figure 4.14a, we see a p-type MOSFET under strong inversion. In the channel and wells, holes are the majority carriers and are confined to the green region. Figure 4.14b shows a p-type diffusion device, which has holes as the majority carrier. These holes are free to move about the doped silicon and not confined. Because of the common carrier type, we normalize the electrical properties of the p-type MOSFET in Figure 4.14a by the p-type diffusion device in Figure 4.14b. Similarly, we normalize the n-type MOSFETs to n-type diffusion devices.

Equation 4.8 shows the formula for normalization of the Seebeck coefficient:

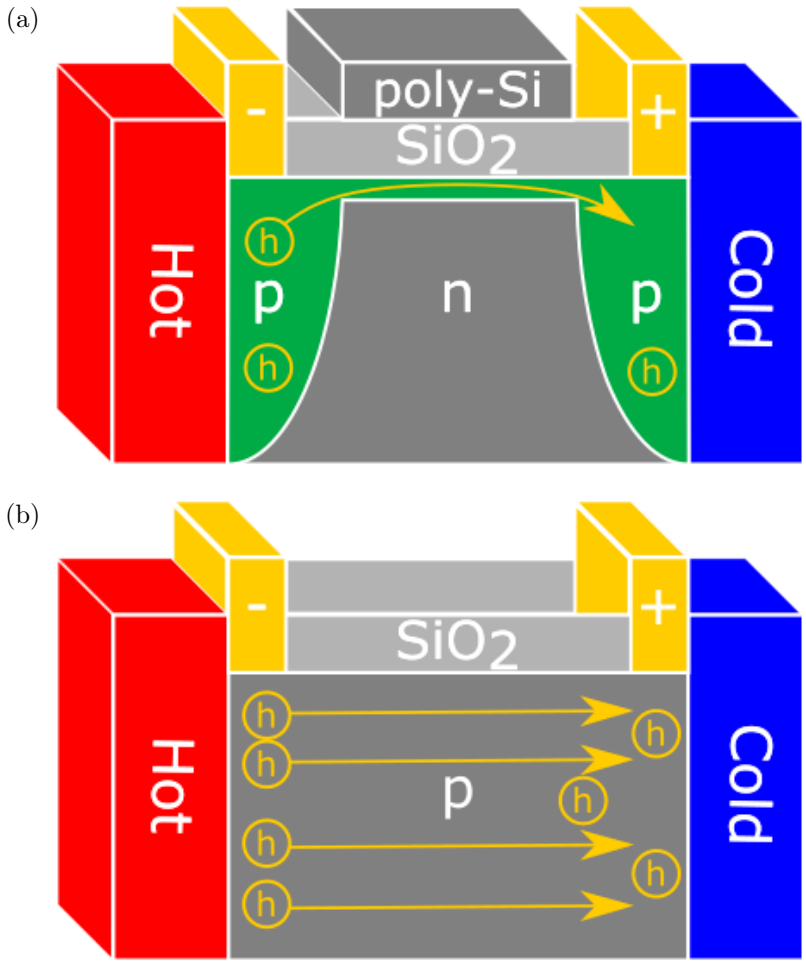


Figure 4.14: Diagrams of (a) the electrical pathway in a pFET and (b) the electrical pathway in a p-type diffusion device.

$$S_{\text{norm}} = \frac{S_{\text{FET}}}{S_{\text{diff}}} \tag{4.8}$$

where $S_{\text{norm}}$ is the normalized Seebeck coefficient, $S_{\text{FET}}$ is the Seebeck coefficient of the MOSFET device, and $S_{\text{diff}}$ is the Seebeck coefficient of the diffusion device.

Equation 4.9 shows the formula for normalization of the electrical conductivity:

$$\sigma_{\text{norm}} = \frac{\sigma_{\text{FET}}}{\sigma_{\text{diff}}} \tag{4.9}$$

where $\sigma_{\text{norm}}$ is the normalized electrical conductivity, $\sigma_{\text{FET}}$ is the electrical conductivity of the MOSFET device, and $\sigma_{\text{diff}}$ is the electrical conductivity of the diffusion device.

#### 4.4.5.2 Normalization of Thermal Properties

When normalizing devices' thermal properties, we should compare similar thermal pathways. Figure 4.15 shows the thermal pathway of MOSFET and diffusion devices.

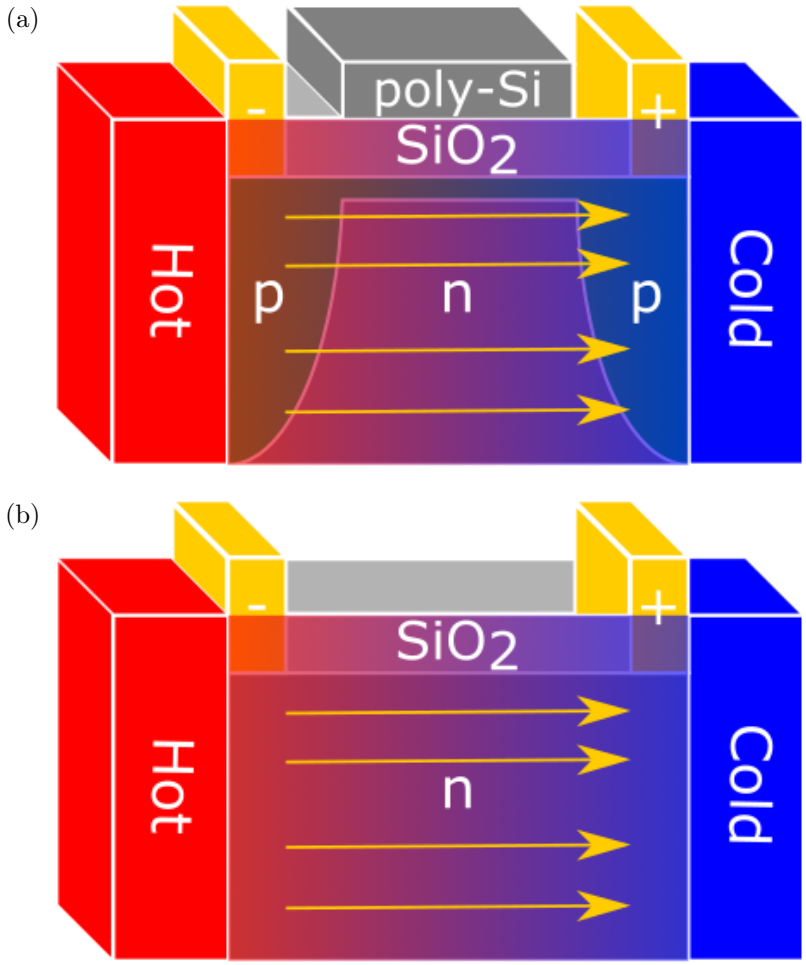


Figure 4.15: Diagrams of (a) the thermal pathway in a pFET and (b) the thermal pathway in an n-type diffusion device.

In Figure 4.15a, a p-type MOSFET under strong inversion is shown. Here, the dominant thermal path is the MOSFET's n-type body. Figure 4.14b shows an n-type diffusion device for which the dominant thermal pathway is the whole diffusion device. For normalization of the thermal property data, because the dominant thermal path is the n-type body, the

p-type MOSFET in Figure 4.15a is normalized by the n-type diffusion device in Figure 4.14b. Similarly, we thermally normalize the n-type MOSFETs to p-type diffusion devices.

Equation 4.10 shows the formula for normalization of the electrical conductivity:

$$\kappa_{\text{norm}} = \frac{\kappa_{\text{FET}}}{\kappa_{\text{diff}}} \tag{4.10}$$

where $\kappa_{\text{norm}}$ is the normalized thermal conductivity, $\kappa_{\text{FET}}$ is the thermal conductivity of the MOSFET device, and $\kappa_{\text{diff}}$ is the thermal conductivity of the diffusion device.

### 4.4.6 Propagation of Error

Because the Seebeck coefficient, electrical conductivity, and thermal conductivity are measured multiple times on multiple devices, each property has its standard error of the mean. When we combine them to calculate the thermoelectric figure of merit, we must propagate the error. Recalling Eq. 1.4, we see that errors will propagate across multiplication/division and powers in the case of the Seebeck coefficient. Equation 4.11 shows the formula for error propagation across powers for $Q = x^n$:

$$\frac{\delta_Q}{|Q|} = |n|\frac{\delta_x}{|x|} \tag{4.11}$$

Likewise, Eq 4.12 shows the formula for error propagation across multiplication and division where $Q = (ab...c)/(xy...z)$:

$$\frac{\delta_Q}{|Q|} = \sqrt{\left(\frac{\delta_a}{a}\right)^2 + \left(\frac{\delta_b}{b}\right)^2 + ... + \left(\frac{\delta_c}{c}\right)^2 + \left(\frac{\delta_x}{x}\right)^2 + \left(\frac{\delta_y}{y}\right)^2 + ... + \left(\frac{\delta_z}{z}\right)^2} \tag{4.12}$$

We see the equation for the error for the $S^2$ term in Eq. 4.13 after some simplification:

$$\delta_S = 2S\delta_S \tag{4.13}$$

Using Eqs. 4.13 and 4.12, we arrive at the equation for the error of the calculated thermoelectric figure of merit in Eq. 4.14:

$$\frac{\delta_{ZT}}{|ZT|} = \sqrt{(2\delta_S)^2 + \left(\frac{\delta_\sigma}{\sigma}\right)^2 + \left(\frac{\delta_\kappa}{\kappa}\right)^2} \tag{4.14}$$

Negligible compared to the variation between devices is the instrument error. We used Keysight 34410A digital multimeters, which have a basic accuracy of 0.0030%. For resistances on the order of hundreds of kOhms, this results in a discrepancy of Ohms. When resistances are converted into temperatures using the temperature resistance calibration curves, 1Ohm changes the temperature by less than 0.001K. We used Keithly 2400 source meters with resolutions of 1pA and 100nV in the usage range. This work measures the order of $\mu$A and mV on the low end, resulting in errors of 1e-6% and 1e-4% for current and voltage, respectively. The error range for the type-K thermocouple is -0.02K to 0.04K, which is minuscule over the 70K+ temperature range studied. Given these values, we can see that these errors are negligible compared to the variation between devices.

## 4.5 Experiment and Data Acquisition Automation

For both efficiency and repeatability, we automated the experiments. We connected a laptop to the various instruments for each experiment using GPIB connections. These connections allow us to control multiple instruments from one program on the laptop.

We developed classes for each instrument needed for the experiments. We use instances of these classes to control each instrument individually, passing commands to the required functions (e.g., measuring resistance, applying a voltage, etc.). These classes streamlined

the development of procedure classes, allowing for the readability and maintainability of the complete code base.

We developed classes for the temperature resistance calibration, current-voltage characterization, and thermoelectric characterization. Each of these classes initialized the equipment for its experiment based on the device type. Figures 4.2 and 4.3 show the procedure followed by the temperature resistance calibration class for MOSFET and diffusion devices, respectively. For the current-voltage characterization, Figs. 4.6 and 4.9 show the procedure the class follows for MOSFET and diffusion devices, respectively. Figures 4.10 and 4.11 show the procedure followed by the thermoelectric characterization class for MOSFET and diffusion devices, respectively. The classes also saved the data for each experiment and shut down all instrumentation at the conclusion.

We also developed a class to process the data from each experiment. The class reads the data for a given experiment and calculates the thermoelectric properties and the thermoelectric figure of merit.

Finally, we developed a class to combine the data from all conducted experiments and calculate the standard error of the mean of the results. This class also produces the final results figures used in this work.

## 4.6 Chapter Summary

This chapter outlined the measurement processes we used to study devices. First, we described a temperature-resistance calibration (TRC) procedure to produce the calibration curves used to determine local temperatures. Then, we outlined a current-voltage (IV) characterization used to determine the electrical conductivity of devices. Next, we discussed a thermoelectric characterization used to determine the Seebeck coefficient and thermal conductivity. Following, we discussed the error propagation in data processing. Finally, we discussed the automation of the experiments and data acquisition process.

We discussed these experiments for metal-oxide-semiconductor field-effect transistor

(MOSFET) and diffusion devices, highlighting the differences between procedures due to the gate on the MOSFET devices. Finally, we showed how we used direct measurements to determine the properties of interest.

# Chapter 5

# Experiment Results and Discussion

In this chapter, the results from the experiment, done at room temperature ( 300K), are examined, with attention paid to the Seebeck coefficient, electrical conductivity, power factor, and thermoelectric figure of merit. The non-zero saturation of the Seebeck coefficient is shown along with increasing electrical conductivity, resulting in an increased power factor. Coupled with effectively no change in thermal conductivity, we see a similar increase in the thermoelectric figure of merit over bulk silicon properties. We also present projections for further improvements from wafer thinning to reduce thermal conductivity.

## 5.1 Power Factor Improvement

Figure 5.1 plots the average normalized power factor, Seebeck coefficient, and electrical conductivity of the MOSFET devices studied as a function of gate voltage. We use diffusion device values, which represent bulk silicon, for normalization. Figure 5.1a shows the results for the p-type MOSFETs while Figure 5.1b shows the results for the n-type MOSFETs.

Figure 5.1aand Figure 5.1b show the normalized Seebeck coefficient exhibiting behavior

Information in this chapter is also disseminated in another publication by the author [143]

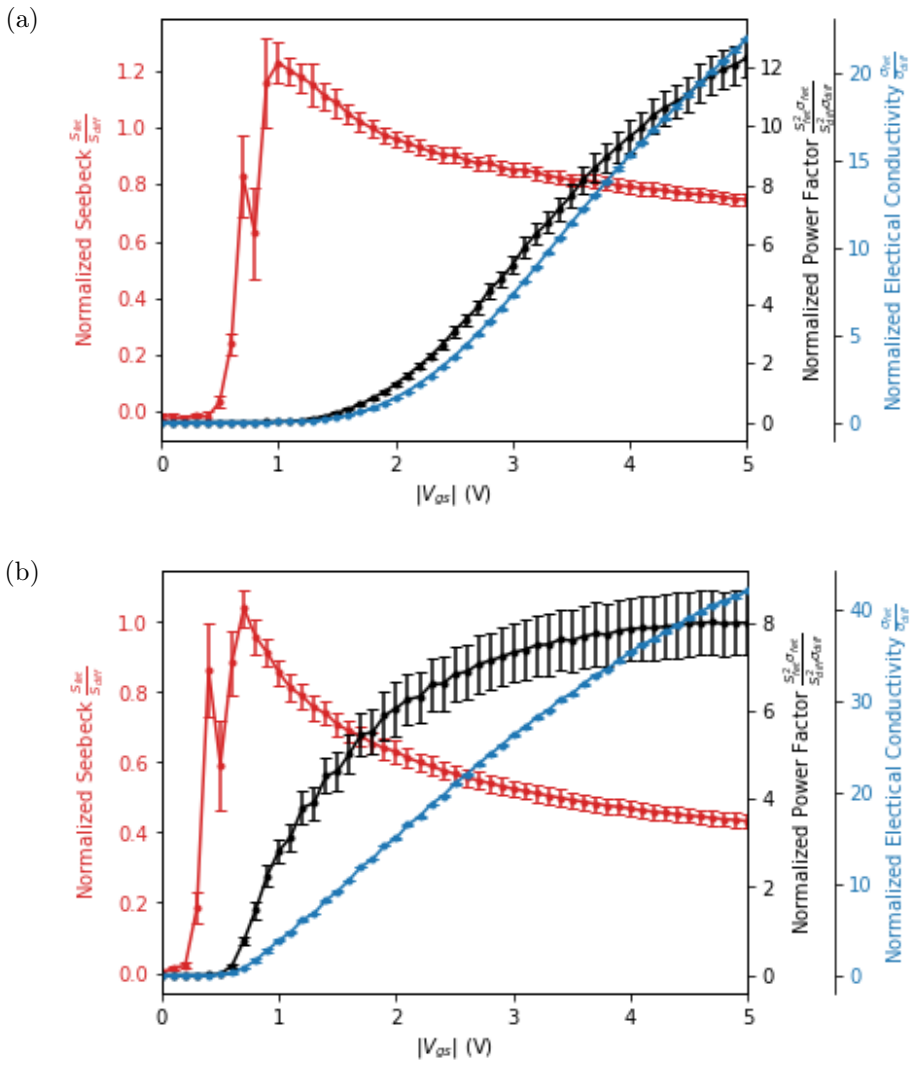


Figure 5.1: Plot showing average normalized power factor, Seebeck coefficient, and electrical conductivity at 300K of ten (a) p-type MOSFET devices and (b) n-type MOSFET devices with standard error of mean error bars.

characteristic of a quantum-confined system at gate voltages above 1 V. Rather than decreasing to zero, the Seebeck coefficient saturates to a non-zero value at high gate voltages. At gate voltages less than 1 V, the MOSFET is off, accounting for the erratic behavior of the Seebeck coefficient.

As expected, the electrical conductivity increases as gate voltage increases in Figure 5.1a and Figure 5.1b due to the higher carrier concentration in the channel. Together with the saturated Seebeck coefficient, this allows the power factor to continue increasing rather than

peaking, as shown previously in bulk thermoelectrics in Figure 2.1a.

Figure 5.1a and Figure 5.1b show trends like the two-dimensional theoretical case seen previously in Figure 2.1b. However, the theoretical and experimental results have some differences resulting from the complexity of the MOSFET channel. It is important to note that the theoretical plot isolates chemical potential as the independent variable. In the experimental case, varying the gate voltage affects not only the chemical potential but the depth of the channel, which profoundly impacts the Seebeck coefficient.

## 5.2 Thermoelectric Figure of Merit Improvement

Figure 5.2 plots the average normalized thermoelectric figure of merit of the MOSFET devices using diffusion device values for normalization. Figure 5.2a shows the results for the p-type MOSFETs while Figure 5.2b shows the results for the n-type MOSFETs.

In both p-type and n-type MOSFETs, we see an increase in the thermoelectric figure of merit at higher gate voltages compared to bulk silicon, represented by diffusion devices. For p-type MOSFETs, we observe approximately a 12-factor improvement over the bulk silicon value measured on the diffusion devices at 300K. For n-type MOSFETs, we observe approximately an 8-factor improvement over the bulk silicon value measured on the diffusion devices at 300K.

These results give us an enhanced thermoelectric figure of merit of 0.12 and 0.08 for p- and n-type MOSFET devices, respectively, working backward from our normalized values and the bulk thermoelectric figure of merit of silicon: 0.01. While this seems low compared to the values in Table 1.1, we must recall that many of those values were measured at well above room temperature and use materials that are not CMOS-compatible. In Table 5.1, we will focus on comparing our results to other silicon-based or CMOS-compatible devices.

In silicon nanowires, Díez et al.[45] measured a thermoelectric figure of merit of 0.02 at 300K. Prete et al.[46] showed thermoelectric values of 0.0033-0.0038 in top-down fabricated silicon-based nanowires at room temperature and above. Zhou et al.[47] showed figure of merits

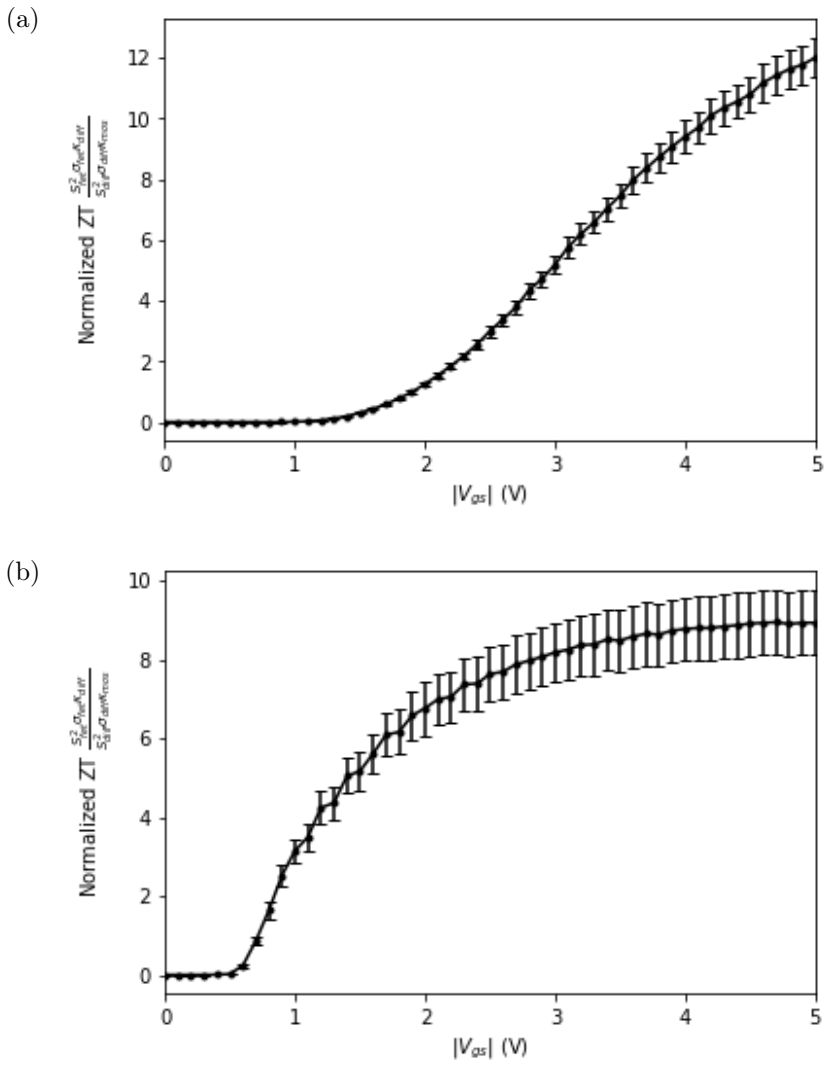


Figure 5.2: Plot showing average normalized ZT at 300K of ten (a) p-type MOSFET devices and (b) n-type MOSFET devices with standard error of mean error bars.

Table 5.1: Selected thermoelectric figures of merit in silicon and CMOS-compatible materials recently obtained recently in literature.

| Material | Year | Temperature, K | $ZT$ |
|---|---|---|---|
| This Work | 2022 | 300 | 0.12 |
| Silicon Nanowires[45] | 2020 | 300 | 0.02 |
| Silicon-based Nanowires[46] | 2021 | 300 | 0.0038 |
| Polysilicon film[48] | 2009 | 300 | 0.014 |

of 0.03 and 0.05 for n- and p-type polysilicon at 373K. Studying polysilicon films for use in CMOS-MEMs thermoelectric power generators, Xie et al.[48] reports figures of merit for p-

and n-type polysilicon as 0.012 and 0.014, respectively.

This work improves upon the measured values of silicon devices in literature while circumventing many fabrication challenges. While silicon is not an impressive thermoelectric material, and our figure of merit is not competitive with those of materials engineered, we should note again that this method can be used for any CMOS-compatible material. Were these structures replicated in $Bi_2Te_3$, which has a room temperature bulk figure of merit of 1, with similar performance enhancement, we would see a figure of merit of 8-12 would.

## 5.3 Further Improvement via Wafer Thinning

Reducing thermal conductivity would further improve the thermoelectric figure of merit. Because the MOSFETs only confine the system electrically, we do not see the benefits in thermal conductivity. However, we can reduce thermal conductivity by thinning the wafer, as shown in Figure 5.3.

Based on this data, we could achieve over 50-factor improvement for p-type MOSFETs and over 30-factor improvement for n-type MOSFETs, respectively, over the control devices studied.

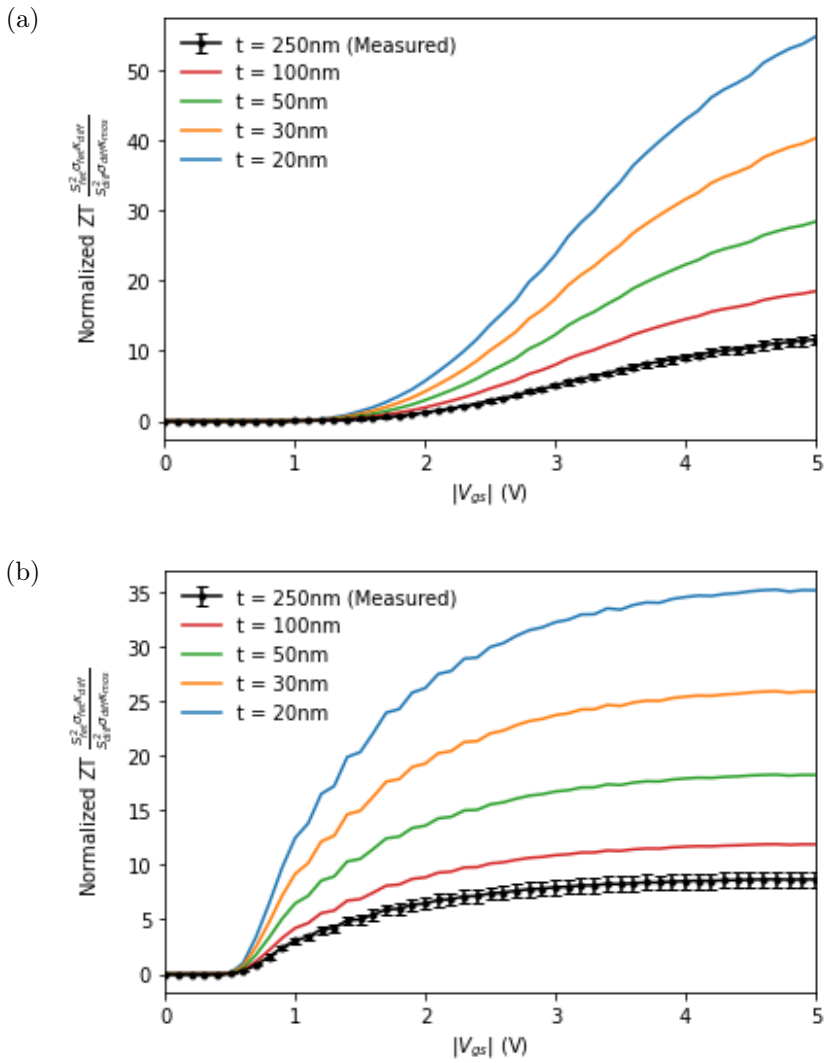


Figure 5.3: Plot showing average normalized ZT and projected normalized ZT after wafer thinning of (a) p-type MOSFET devices and (b) n-type MOSFET devices. Projected thermal conductivity values are taken from Zhang et al. [145].

# Chapter 6

# Conclusion and Future Work

This dissertation discussed the theory behind Seebeck coefficient enhancement using quantum wells. Then, we described the design of complementary metal-oxide-semiconductor (CMOS) metal-oxide-semiconductor field-effect transistors. We designed an experiment to test these devices and demonstrated, for the first time, the enhancement of the Seebeck coefficient of thermoelectric devices through electrical quantum well confinement.

Much of the underlying theory is based on the critical work of Hicks and Dresselhaus[125–127]. First, we showed that the Seebeck coefficient $S$ has a proportional relationship with the density of states near the Fermi level. Through this relationship, low-dimensional devices, such as the two-dimensional electron and hole gases (2DEGs and 2DHGs, respectively), can enhance the Seebeck coefficient because of the enhanced density of states.

This enhanced density of states is brought on by the quantized energy levels caused by the reduced dimension(s) of the material. These quantized energy levels then prevent electrons from occupying some of the low-level states available in large-dimension materials, forcing them to higher energy states near the Fermi level. The result is an increased density of states and an enhanced Seebeck coefficient.

In this work, rather than pursue physically small devices where quantum confinement would occur, we used electrical isolation to induce quantum confinement and the enhanced

density of states needed to enhance the Seebeck coefficient. For this purpose, we used MOSFETs. Under high-inversion operation, the conducting channel in a MOSFET is small enough to induce the quantum effects required for enhancement, decoupling the Seebeck coefficient, electrical conductivity, and thermal conductivity. Additionally, the fabrication process of these devices is well defined, and devices function reliably over time due to their widespread use in computer chip manufacturing. These are advantages over other systems with physically reduced dimension(s), such as superlattices and nanowires.

The devices used in this study were fabricated with a busFET architecture to overcome the CMOS guideline limitations on MOSFET size and fabricate longer thermoelectric devices. The longer devices allowed a greater temperature differential to be induced across the devices, resulting in a higher and more easily measurable Seebeck voltage.

At the ends of the busFET structure, we placed resistors to induce the temperature differential and measure the temperature. The resistors were designed to be sensitive to temperature at the expense of precision in the absolute resistance value. Since these devices are manufactured according to CMOS guidelines, they are also readily compatible with today's computer chips.

We then characterized devices in temperature resistance calibration (TRC), current-voltage (IV) curve, and thermoelectric measurement tests. The TCR measurements characterized resistors on a per-device basis to overcome any fabrication-induced differences in resistance. The calibration for each resistor allows the temperature measurement locally on the devices for later measurements.

We then measured the device's IV curves at a variety of temperature differentials and gate voltages. We determined the temperature from the resistor measurements and the TCR curves. From the data, we pull the electrical conductivity for each temperature differential and gate voltage to calculate the power factor and thermoelectric figure of merit.

We then measure the Seebeck voltage of the device for the same range of temperature differentials and gate voltages as the IV curves. From this data, we determine the Seebeck coefficient.

The results from these experiments show that thermoelectric performance is enhanced in the MOSFET devices under high inversion, with a 12-factor and 8-factor improvement over bulk silicon in the thermoelectric figure of merit for p-type and n-type FETs, respectively. This increase is caused by the saturation of the Seebeck coefficient to a non-zero value induced using quantum confinement. This saturation allows the power factor to continue to climb as the Seebeck coefficient does not go to zero as the electrical conductivity climbs. This work is the first demonstration of the quantum enhancement of the Seebeck coefficient in an electrically defined channel and lays the foundation for microelectronics-based, chip-scale thermoelectric cooling and energy-scavenging applications.

In addition to this novel approach to increasing the thermoelectric figure of merit with CMOS-compatible devices, this work also lays the foundation for an improved methodology for measuring the thermoelectric performance of on-chip devices. Rather than only reporting the Seebeck coefficient, we reported the thermoelectric figure of merit and all of its constitutive properties by using bulk properties as a baseline and normalizing to control devices with those properties. Through this normalization, we were able to mitigate systemic risk stemming from systemic inaccuracies.

## 6.1 Summary of Author Contributions

The author designed, set up, automated, and performed all device characterizations. The most consequential impact of the method in this work is using control devices with bulk properties, mitigating the systemic measurement errors that arise. This approach is an improvement over the previous methodology, which used a correction factor in case of such errors. For example, using resistors to measure temperature at the ends of the devices has a level of inaccuracy because the resistors are located some distance from the actual device ends. Where previous methods would estimate the actual temperature, this method normalizes by a control device which will have the same error, removing any guesswork.

The author also established the methods used to measure the thermoelectric properties

of the test devices. These methods are critical to reporting the final device performance. In addition, the author collaborated in the design of the devices studied.

## 6.2 Future Work

Further improvement to the thermoelectric figure of merit can be made through the reduction of thermal conductivity. Because the MOSFETs only confine the system electrically, we do not see the benefits in thermal conductivity. However, by thinning the wafer used for the MOSFETs, thermal conductivity can be reduced, as shown in Figure 5.3. This data shows over 50-factor and 30-factor improvements for p-type and n-type FETs, respectively, over the control devices studied. Further improvements could be done by heterogeneous integration of $Bi_2Te_3$, which has better bulk properties than silicon.

In addition to further work improving the thermoelectric figure of merit, work can also be done on optimizing arrays of these devices for on-chip cooling, temperature regulation, and heat-pump designs. Optimizing such designs will help the technology be realized in real-world applications where it can have an impact.

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