THE DESIGN OF AN INTEGRATION AND QUANTIZATION UNIT FOR A RADAR PROCESSOR

by

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CHAPTER I

INTRODUCTION

The weather radar has become an increasingly important tool to the Meteorologist. With it, it is possible to study storm development, precipitation patterns, and severe atmospheric disturbances, such as tornadoes. In principle, weather radar data can be applied to such diverse activities as flood forecasting and crop management. Such data has been of limited value in the past due to a lack of an accurate and convenient storage system.

The obvious answer to a storage format is the digital computer. Data from the radar can be digitized and stored in a computer data bank indefinitely. Kansas State has become involved in implementing such a system. The basic scope of the project is to interface a APS-81 radar to a NOVA 1200 minicomputer. The interface itself is to be designed to quantize and digitize the radar data (the video signal) and store it in the NOVA disc system.

Design of the actual interface breaks down into two parts. First, the radar returns from a specified area, called a range bin, are summed together. This analog value is then converted to a digial word. This part of the interface is called the "Integration and Quantization Circuit" (I & Q Circuit). The second half of the interface is called the "Processor". Its function is to take the digital word from the first unit, along with synchronization signals, and place it in the NOVA disc system.

At the present time, the Processor part of the interface has been designed and built. A series of computer programs have been written to handle the data acquisition sequence. This is described in Reference (2).

It is the purpose of this Report to describe the design and testing of the I & Q Circuit. Due to monetary restrictions, it is not possible to implement the entire system at this time. However, the design of the I & Q system is based on a modular concept. This facilitates expansion of the system at a later time.

CHAPTER II

SYSTEM CONSTRAINTS

2.1 Introductory Remarks

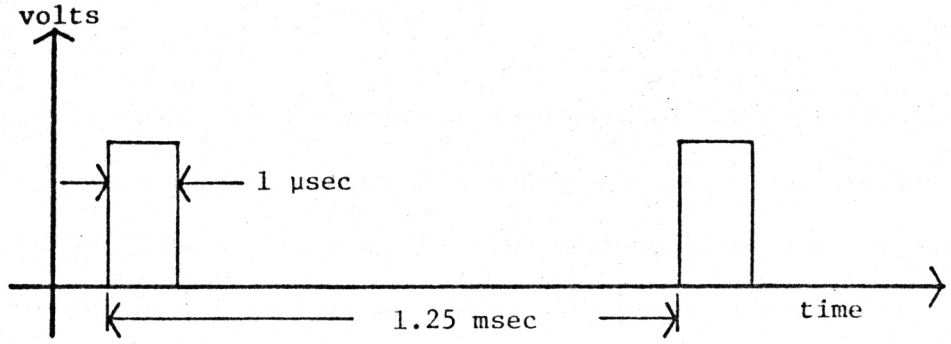
The purpose of this chapter is to define in some detail the overall constraints that are placed on the interface. General background information on radar will be presented, along with a description of what the interface is trying to accomplish. The radar specifications will then be given, and interface parameters will be calculated from these. Finally, an overall scheme for the interface will be unveiled.

2.2 Background Information

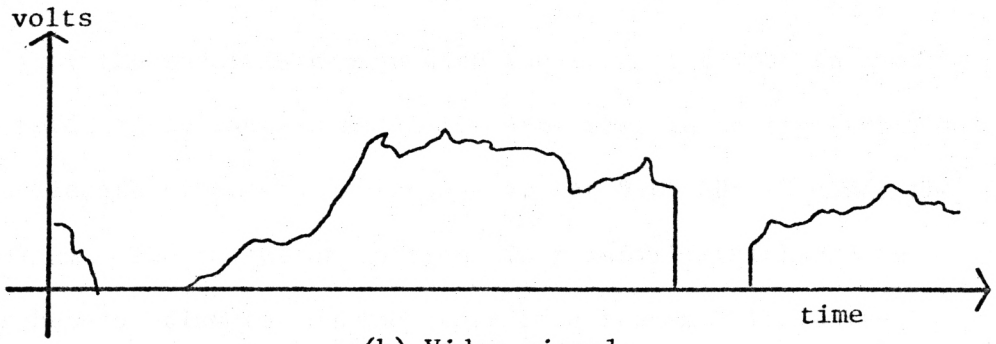
The basic principle behind radar involves sending a known signal in a known direction and measuring the return, or echo. Most radars are pulse radars. By this it is meant that bursts of an RF signal are sent out. During the off period, the radar "listens" for incoming echoes. The rate at which these bursts are sent out is called the pulse repetition frequency (prf). The radar signal and the video return are shown in Figure 2.2-1. The prf is determined primarily by the maximum range at which targets are expected. If the prf is made too fast, there is an increased probability of receiving echoes from the wrong pulse transmission. These echoes are called "multiple-time-around" echoes. They can result in erroneous range measurements. This is demonstrated in Figure 2.2-2. Maximum unambiguous range is given by equation 2.2-1.

$$R_{unamb} = \frac{c}{2f_r} \; ; \; c = 3 \times 10^8 \text{ m/s} \; , \; f_r = \text{prf Hz} \qquad (2.2\text{-}1)$$

It is important to note that the maximum unambiguous range calculated from equation 2.2-1 is not the actual range of the radar. Useful radar range



(a) Unmodulated Radar Output.



(b) Video signal.

Figure 2.2-1 Radar Signals

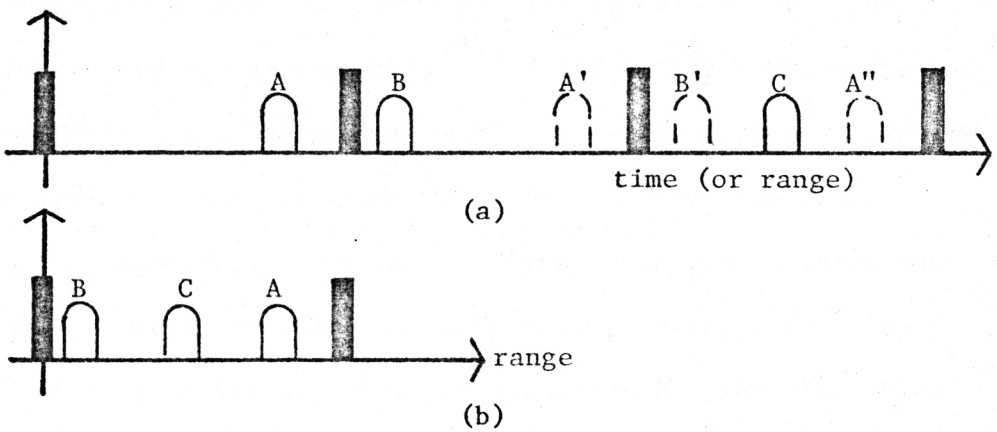


Figure 2.2-2 Multiple-time-around Echoes.

(a) Three targets A, B and C, where A is within R_{unamb} and B and C are multiple-time-around targets.
(b) Appearance of the three targets on A-scope.

SOURCE: M. I. Skolnik, Introduction to Radar Systems New York: McGraw-Hill Book Company, 1962.

is, in general, a very complicated expression depending on, in part, receiver sensitivity, antenna gain, atmospheric conditions, etc. For reliable operation, the prf should be set so that the maximum unambiguous range is slightly greater than the actual radar range. The prf of the APS-81 radar used by Kansas State is 800 Hz, which allows a maximum unambiguous range of 116 miles.

The frequency of the radar is chosen with the type of target in mind. For an object to reflect the radar signal, its size must be on the order of magnitude of a wavelength of the radar frequency. At 9.03 GHz (X-Band) the wavelength is 3.32 cm. The target of interest is rainfall, which can be thought of as a sphere of diameter on the order of a few mm. The wavelength is chosen to be somewhat larger than the target so that the radar signal will penetrate the clouds to a greater degree. This allows the radar to see more than the front of a storm.

It is desirable to make the radar beam as directional as possible. Antenna beamwidth, denoted θ_b, is the quantity that describes how narrow the beam is. The APS-81 has a fan-shaped beam of width 5 degrees. Azimuth and Elevation are the two parameters that describe the direction of the beam. Azimuth is the distance in degrees from true north, which is defined to be zero degrees. Azimuth increases in the clockwise direction. Elevation is the angle of tilt of the antenna, and runs from 0° (horizontal) to 90° (vertical). Azimuth information is sent by a binary shaft encoder or a synchro system to the display. The APS-81 uses a shaft encoder for the Azimuth, and Elevation is fixed. Elevation need not be varied, since a fan-shaped beam is used. Maximum width of the beam is in the vertical direction.

2.3 Data Encoding Scheme

The analog data from the radar is in the form of a I.F. signal. This I.F. signal must be run through a combination logarithmic amplifier and envelope detector, such as the ICLT-3010, manufactured by RHG Electronics Laboratory, to produce the interface video. Logarithmic detection is used to compress the wide dynamic range of the radar signal into a more manageable spread.

The PPI (Planned Position Indicator) display of the radar is shown in Figure 2.3-1. This display plots radar echo intensity as a function of range and azimuth. It is desired that the information on this graph be digitized and stored in the computer. To do this, a series of range bins are set up. The range is split into 200 half mile intervals and the azimuth is split into sixty-four 5.625^{o} increments. The 5.625^{o} value chosen is the value of the second least significant bit of the shaft encoder. All radar returns within each range increment and azimuth increment are summed together. After the azimuth interval is complete, each of the 200 range bins will have an analog voltage proportional to the log of the intensity of return within that area. These range bin values are then run through an analog-to-digital converter and stored in the NOVA computer. After the values are converted, the range bins are dumped in preparation for summing (or integrating) over the next azimuth increment. This sums up the data acquisition scheme. A sample range bin can be seen on Figure 2.3-1. The balance of this Report is concerned with implementation of this scheme.

2.4 Interface Specifications

Pertinent specifications for Kansas State's weather radar are summarized in Table 2.4-1. From these parameters, it is possible to calculate

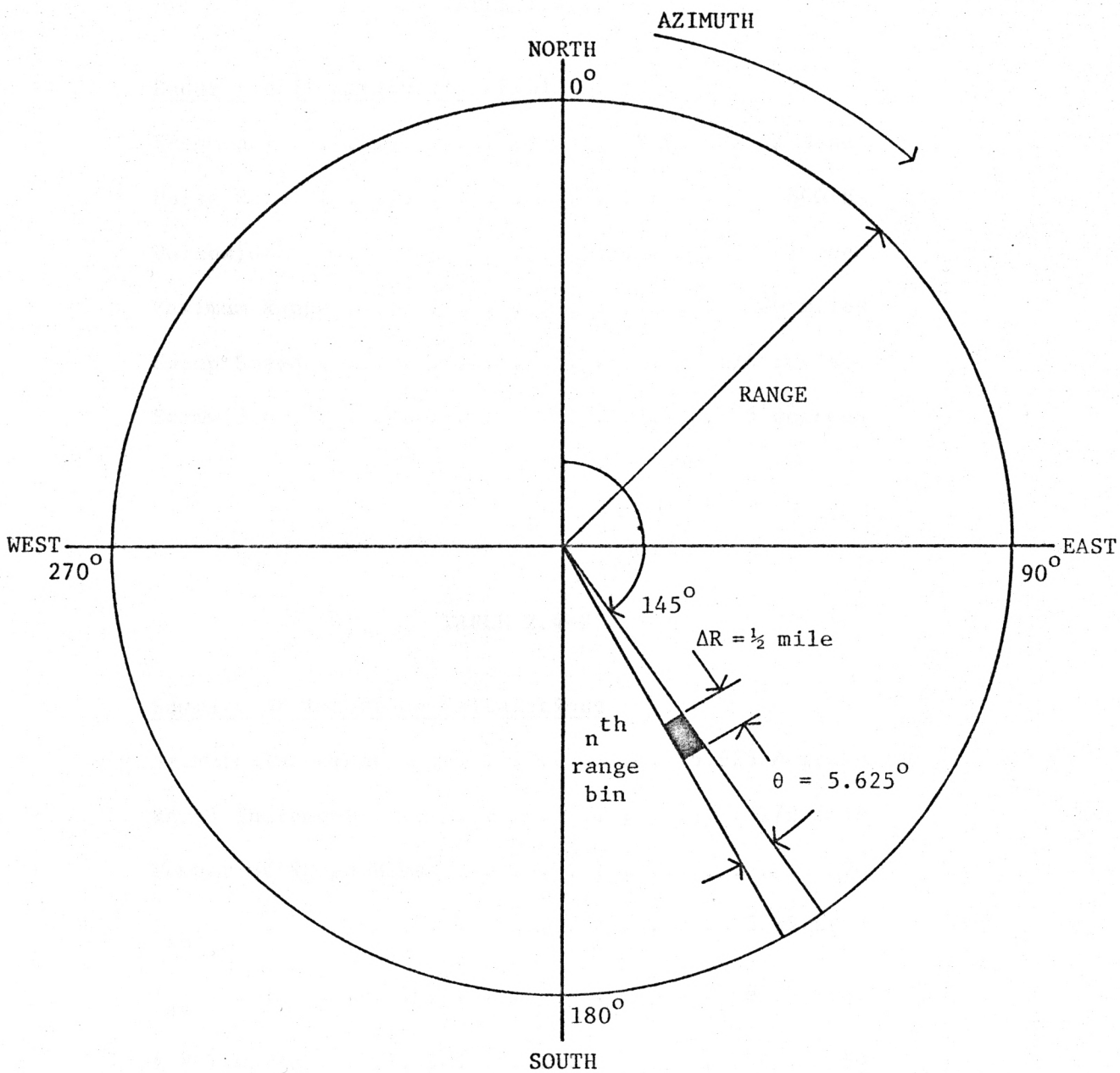


Figure 2.3-1 PPI Display of Radar.

TABLE 2.4-1

Radar Specifications: APS-81

Frequency	9.03 GHz (X-Band)
Pulse Rate	800 Hz
Pulsewidth	1 μsec
Maximum Range	100 miles
Sweep Speed	1/4 rev/sec
Beamwidth	5 degrees

TABLE 2.4-2

Summary of Interface Calculations

Azimuth Increment	5.625 degrees
Range Increment	1/2 mile
Number of Range Bins	200
T_{rb}	5.38 μsec
T_{az}	62.5 msec
# Pulses/Az	50
T_{on}	269 μsec
Time Between Pulses	1.25 msec
T_{d}	174 μsec

the interface constraints. These calculations are as follows:

1) Integration time per range bin per pulse

$$T_{rb} = \frac{2\Delta R}{c} = \frac{2(.5 \text{ mi})}{1.86 \text{ X } 10^5 \text{ mi/sec}} = 5.38 \text{ μsec}$$

2) Time per azimuth increment

$$T_{az} = (\# \text{ degrees/azimuth increment})(\text{time/degree})$$

$$T_{dg} = \text{time/degree} = \frac{1}{(\text{sweep speed})(360)}$$

$$T_{az} = \frac{5.625 \text{ degrees/az}}{(.25 \text{ rev/sec})(360 \text{ degrees/rev})} = 62.5 \text{ msec}$$

3) Number of pulses per azimuth increment

$$\# \text{ pulses} = T_{az} \text{ X prf} = 62.5 \text{ msec X } 800 \text{ Hz} = 50$$

4) Total on time for n^{th} range bin (before dump)

$$T_{on} = \# \text{ pulses X } T_{rb} = 50 \text{ X } 5.38 \text{ μsec} = 269 \text{ μsec}$$

5) Dump time

$$T_d = 1/\text{prf} - T_{rb}(200) = 1/800 \text{ Hz} - (200)5.38 \text{ μsec}$$

$$T_d = 174 \text{ μsec}$$

2.5 Operation of System

Figure 2.5-1 shows the entire radar-computer system in block diagram form. The interface has three inputs from the radar: the radar video, the radar trigger, which is basically the modulating pulse train, and the shaft encoder. The output of the interface consists of a four-bit binary intensity value and encoded azimuth information for each range bin. Necessary control signals are also placed on the NOVA bus by the interface.

The overall interface block diagram is shown in Figure 2.5-2. The interface breaks down into two functional sections. The first, which this Report deals with, is the I & Q Circuit. This circuit's inputs are the

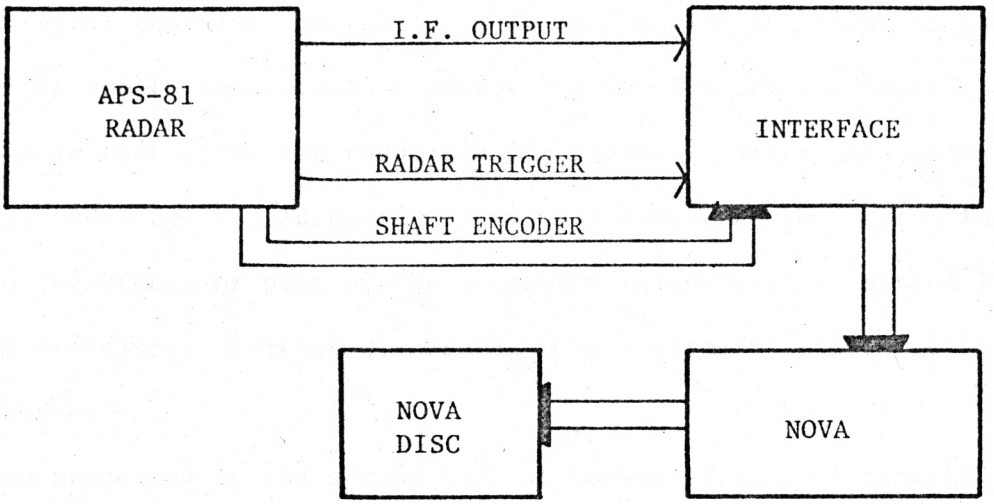


Figure 2.5-1 Entire Radar - Computer System

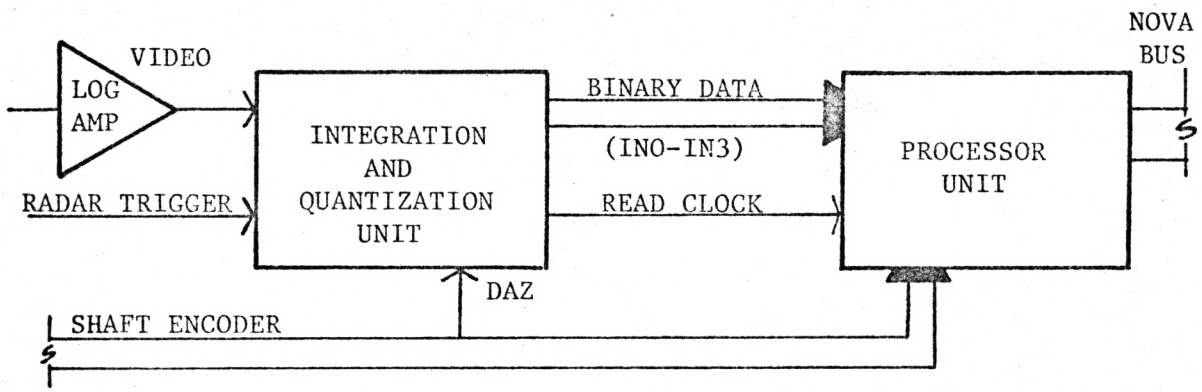


Figure 2.5-2 Interface Block Diagram.

radar video, radar trigger, and the shaft encoder's 5.625 degree bit. The I & Q Circuit contains control logic to synchronize the radar signals to each other and to the interface master clock. The control logic creates the signals that drive the range bin integrators. After each azimuth increment, the range bin intensity values are converted to digital form and sent to the Processor part of the interface, along with a control line to run the Processor. Further discussion of this circuit is defered to the next chapter.

The Processor is the second half of the interface. A detailed description of the Processor is given in Reference (2). Basically, it takes the digital intensity signal and control line from the I & Q, combines it with the azimuth data from the shaft encoder, and places this information on the NOVA bus. Input-output requirements of the NOVA are fulfilled by this half of the interface. Although this is an oversimplified view of the Processor, for the purposes of this Report it is sufficient.

CHAPTER III

THE INTEGRATION AND QUANTIZATION CIRCUIT

3.1 Introductory Remarks

This section describes, on a block diagram level, how the I & Q Circuit operates. Emphasis is placed on subsystems of which there are four: the Digital Control Unit (DCU), the Range Bins Circuit (RBC), the Analog-to-Digital Converter (A/D), and the Translator. Descriptions of the functions of each of these, and how they interrelate, are given. A separate chapter is included later in the Report on each of these subsystems. These deal with actual circuit analysis and implementation.

3.2 Requirements

To re-iterate slightly from the previous chapter, the function of the I & Q Circuit is to take the radar video and timing signals, integrate the video over 200 range bins during one azimuth increment, and convert these range bin intensities into digital words. This process continues until the entire PPI display is stored in the computer. A block diagram is shown in Figure 3.2-1. All control signal mnemonics are explained in Table 3.2-1.

The function of the Digital Control Unit is to synchronize the RADAR TRIGGER and DAZ (5.625^{o} bit) to the master clock. It also provides the system control signals that run the range bins, the Analog-to-Digital Converter, and the Processor. For reasons that will be explained later, the DCU operates on 5 volt TTL, while the rest of the system operates on 15 volt CMOS. It is therfore necessary to level shift the various digital signals. This is the function of the Translator.

The Analog-to-Digital Converter is a 4-bit binary encoder. It must have a very fast conversion time, since the range bin values must be

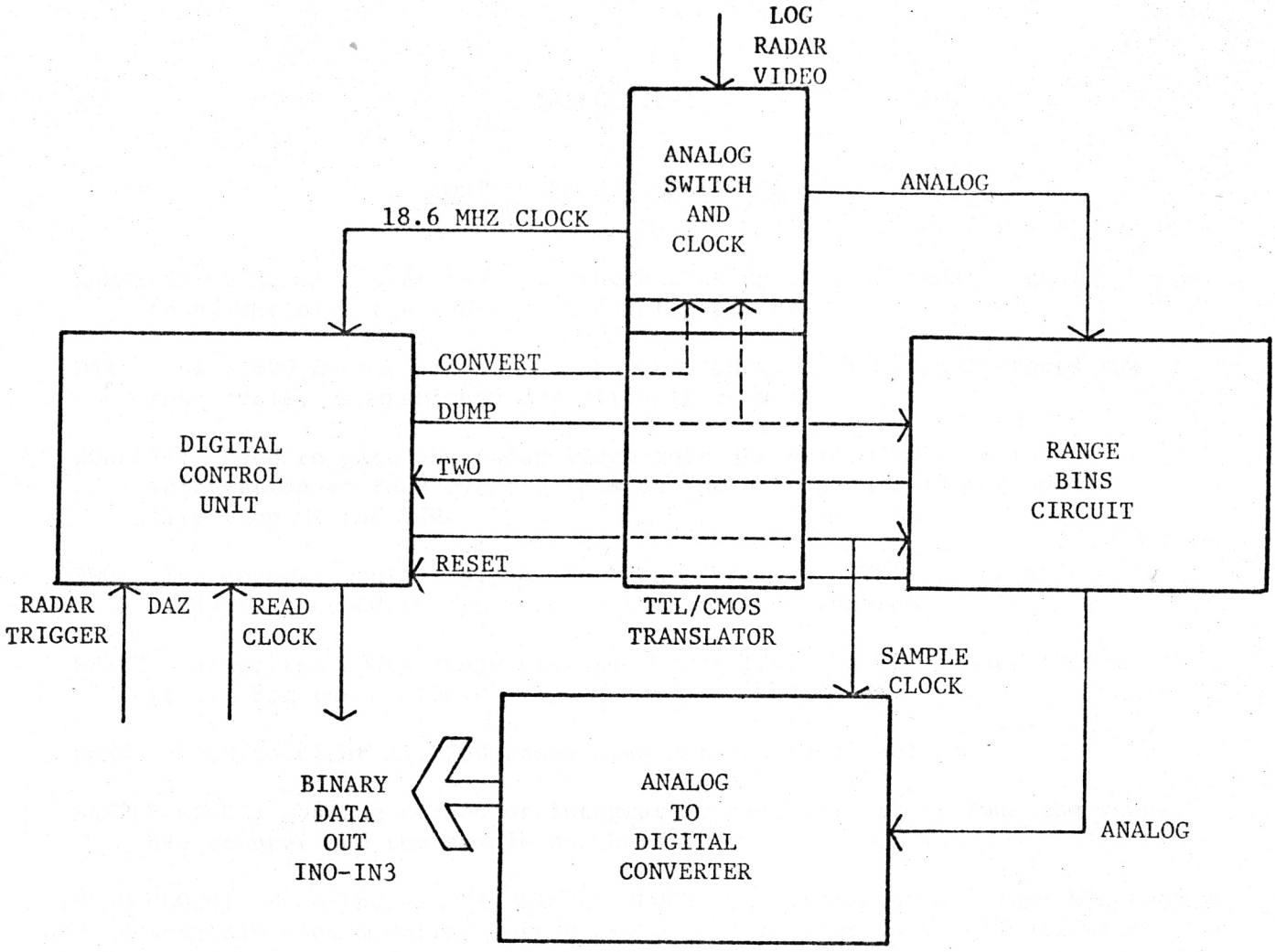


Figure 3.2-1 Integration and Quantization Unit Block Diagram.

TABLE 3.2-1

CONTROL SIGNAL MNEMONICS

RADAR TRIGGER: A 1 μsec pulse at the beginning of each radar signal. Used to synchronize the start of the integrate cycle.

DAZ: The 5.625 degree bit of the shaft encoder. This signal starts the read cycle, as an azimuth deviation is complete.

CONVERT: Used to gate the radar video into the system only during an integration or read cycle. This is the same signal as the COUNT flip-flop in the DCU.

TWO: The decoded control signal for range bin two. This is used internally in the DCU to synchronize the start of the read cycle.

RESET: After the 200th range bin has integrated, the RBC counter resets itself and the system.

DUMP: Used to clear all 200 range bins after a read cycle.

SAMPLE CLOCK: During a read or integrate cycle, this clock runs the range bin counter and the sample and hold.

READ CLOCK: Much the same as SAMPLE CLOCK, but it begins on range bin two and only occurs during a read cycle. It is used to clock data into the Processor.

RADAR VIDEO: Unsampled log video straight from radar.

ANALOG: Analog signal present on range bin capacitors main bus.

converted every 5.38 μsec during a Read cycle. The Range Bins Circuit consists of 200 R-C integrators. A Johnson counter steps down the integrators, using FET switches to switch in and out range bins. Gating is also provided to dump all range bins at once.

3.3 Operation

Perhaps the best way to understand how the system operates is to follow through a cycle on the timing diagram (Figure 3.3-1). Note that this Figure is also used in the next chapter, and therefore contains more information than is needed here. Also note that the COUNT and READ signals represent the SAMPLE CLOCK and READ CLOCK respectively, as COUNT gates the SAMPLE CLOCK and READ gates the READ CLOCK. The first thing that happens after a radar trigger is received is that the DCU outputs the SAMPLE CLOCK, a 186 KHZ clock synchronized with the radar trigger. The SAMPLE CLOCK drives the range bin counters which in turn drive the range bins. Every 5.38 μsec the counter switches to the next range bin. After the 200th range bin has been integrated, the range bin counters reset, resetting the system. Approximately 50 radar pulses are so integrated in one azimuth increment. The above is called an integrate cycle. At any time in the above cycle, a DAZ pulse can arrive. This means it is time to read out the intensities and then dump them. It is up to the DCU to synchronize this read signal with the next radar trigger. At the next radar trigger, the READ CLOCK is used to clock the digital output of the I & Q into the Processor. This READ CLOCK is the so called "control signal" referred to in the last chapter. At the end of the Read cycle, the DUMP signal goes high, discharging the capacitors until the receipt of the next radar trigger.

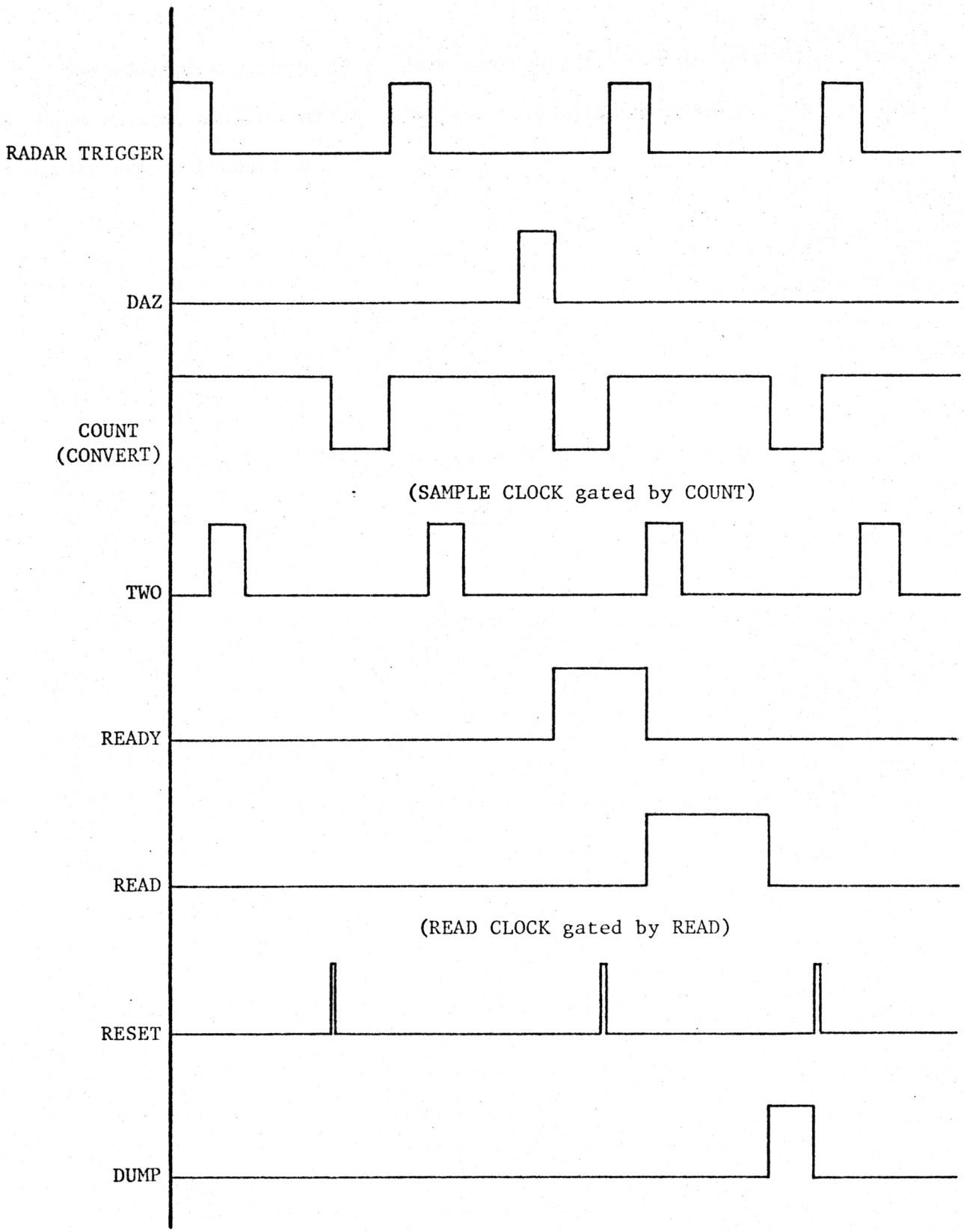


Figure 3.3-1 I & Q Timing Diagram.

The above description is by no means complete. It is intended to give a rough idea of how the system operates. Detailed analysis is reserved for the chapters on circuit analysis.

CHAPTER IV

THE DIGITAL CONTROL UNIT

4.1 Introductory Remarks

The DCU is the heart of the radar interface. It controls all functions of the interface on command of the radar unit. The Range Bins Circuit is used to sum radar information over a certain range and azimuth. The DCU defines the magnitude and precise timing for these quantites. There is a close interrelation between the RBC and the DCU. It was therefore necessary to design a dummy RBC to simulate the full 200 range bin implementation. This is discussed later. A complete functional analysis will be presented with a discussion of the implementation to follow.

4.2 DCU Function

The general function of the control unit is to synchronize all the control signals to the radar trigger. This is extremely important as the incoming video signal is referenced to the radar trigger. For example, for 5.38 μsec after the trigger, any incoming video signal is caused by a target in the 0-1/2 mile range. Without proper synchronization, there is no way to tell range information.

The radar trigger is the most important signal. Next in importance is DAZ, signifying that an azimuth increment of 5.625 degrees has occured. This signal is used to tell the control unit that it is time to read the values stored in the range bins, then dump them out. Since approximately 50 radar pulses occur in each range bin, and the signals are only quantized to 16 levels, each range bin can have ±1 radar pulse.

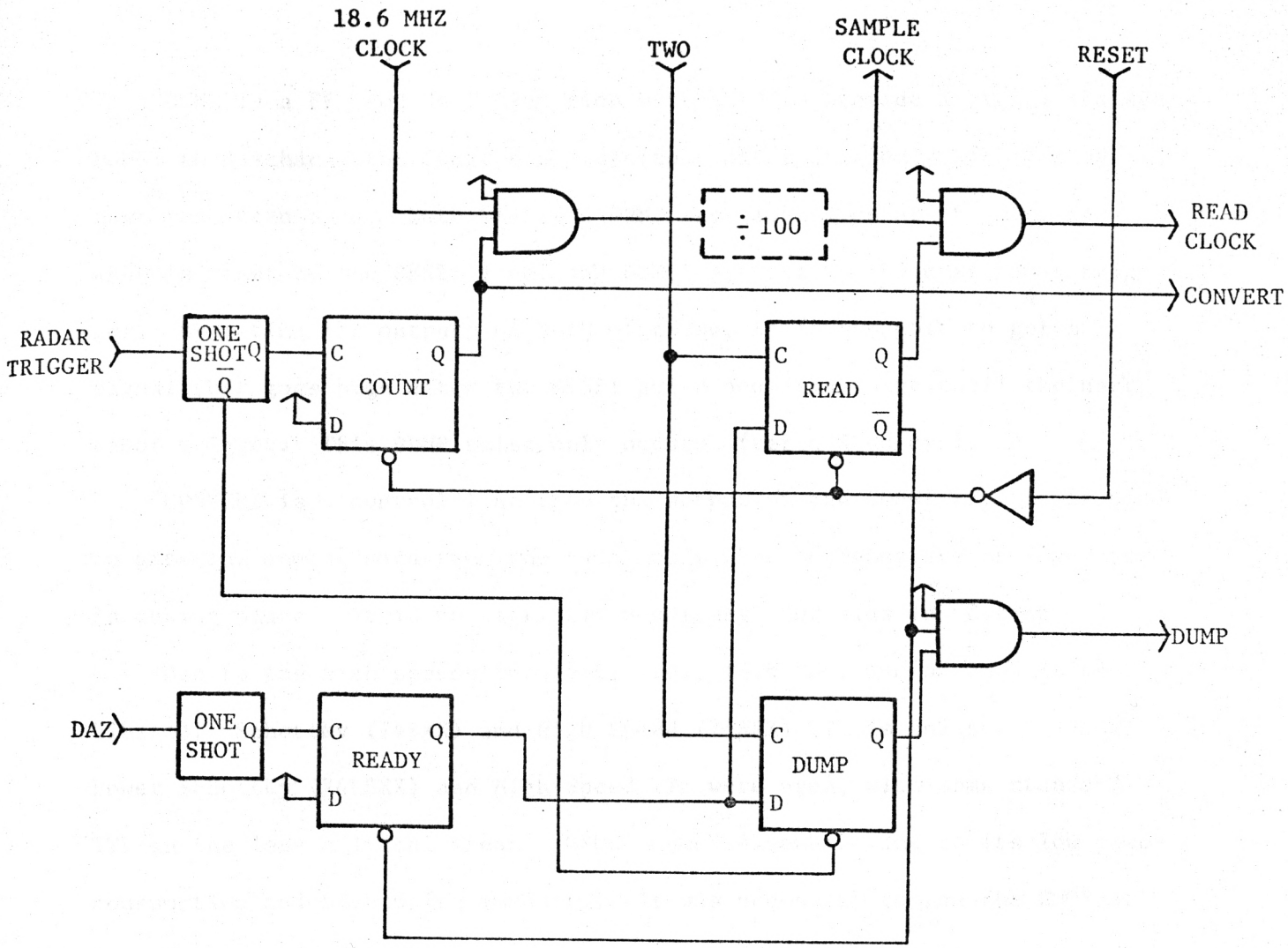
4.3 Implementation

The system timing diagram (Figure 3.3-1) is applicable to this discussion. Figure 4.3-1 shows a schematic of the DCU.

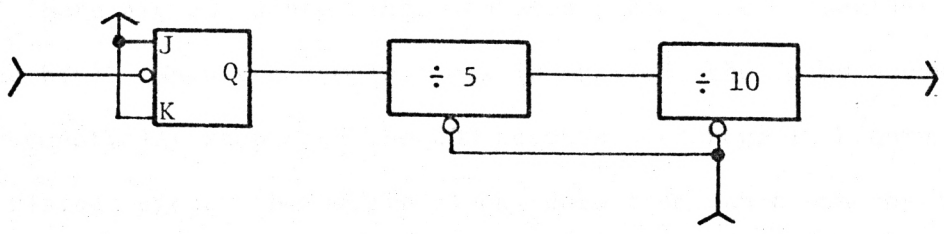
Both DAZ and RADAR TRIGGER are run through one-shots set up for a 1 μsec pulse. This is to clean up the input signal and to keep the clock inputs to the COUNT and READY flip-flops (denoted FF) low. This is necessary as these FF (edge triggered D-type) cannot reset if the clock is held high.

The first sync function that takes place is to synchronize the radar trigger to the sample clock. This is done by taking a very fast clock (18.6 MHZ) and gating it to a divide by 100 chain whenever the COUNT FF (clocked by RADAR TRIGGER) goes high. Therefore, the maximum out-of-sync time is 100th of a clock period, or 53.8 nsec, which is acceptable. The COUNT FF enables the SAMPLE CLOCK, which drives the range bins. After the 200th range bin, a short reset pulse from the RBC resets the COUNT FF.

At any time in the above sequence, a DAZ pulse can arrive. It must be synchronized to the next radar trigger. This is the function of the READY and READ FF's. When the DAZ pulse arrives, it sets READY. READY being high signifies the fact that the Processor wants to read the range bin data at the beginning of the next radar trigger. READ is a FF that gates the sample clock to the Processor and tells it to start transferring data to the NOVA. DAZ signals the start of the READ cycle. Read is clocked by the control line from range bin two (the TWO signal). This is done so that the read clock will start on the transfer from range bin one to range bin two. (For an explanation of the difference between READ CLOCK and SAMPLE CLOCK, see section 4.4). At any rate, both COUNT and READ are reset by the RESET line from the RBC.



(a) Overall schematic.



(b) Divide by 100 circuit.

Figure 4.3-1 Digital Control Unit Schematic.

DUMP is a FF used in conjunction with READ to provide a signal (called DUMP) to discharge the range bin capacitors after (but only after) they have just been read. Both READ and DUMP are clocked on at the same time. READ is reset by the RESET line, and DUMP is reset by the next radar trigger. By gating the outputs of both of these, it is possible to get a signal that goes high after the RESET pulse and stays high until the next radar trigger. This DUMP pulse only occurs after a Read cycle.

CONVERT is a control line from the output of the COUNT FF. It is used to gate the analog data from the radar only when an Integrate or Read cycle is taking place. It is not strictly necessary, but aids in testing.

Due to the high speeds involved, i.e., 18.6 MHZ, use of CMOS is prohibited. Schottky (74SXX) and High Speed (74HXX) TTL is indicated. Low Power Schottky (74LSXX) and High Speed TTL were used, with some standard TTL in the less critical areas. CMOS is used elsewhere due to its low power consumption and high noise immunity. It was necessary to run the CMOS at 15 volts to get maximum speed capability. The DCU is all TTL, with the rest of the I & Q Circuit using CMOS.

4.4 Timing of READ CLOCK and SAMPLE CLOCK

There are 200 range bins, numbered 1-200. Zero count is blank (no range bin). When the sample clock is applied, the Johnson counters begin to sequentially step down the 200 outputs, as shown in Figure 4.4-1. On the rising edge of the sample clock, data from range bin one is fed to the A/D converter. After one clock period, data is stable on the digital output and is ready to be read. The next rising edge of the clock steps the Johnson counter to range bin two, clocking on READ and DUMP. READ enables the read clock, which latches the data in the Processor intensity register. The Read cycle proceeds in this manner until the range bin counter attempts

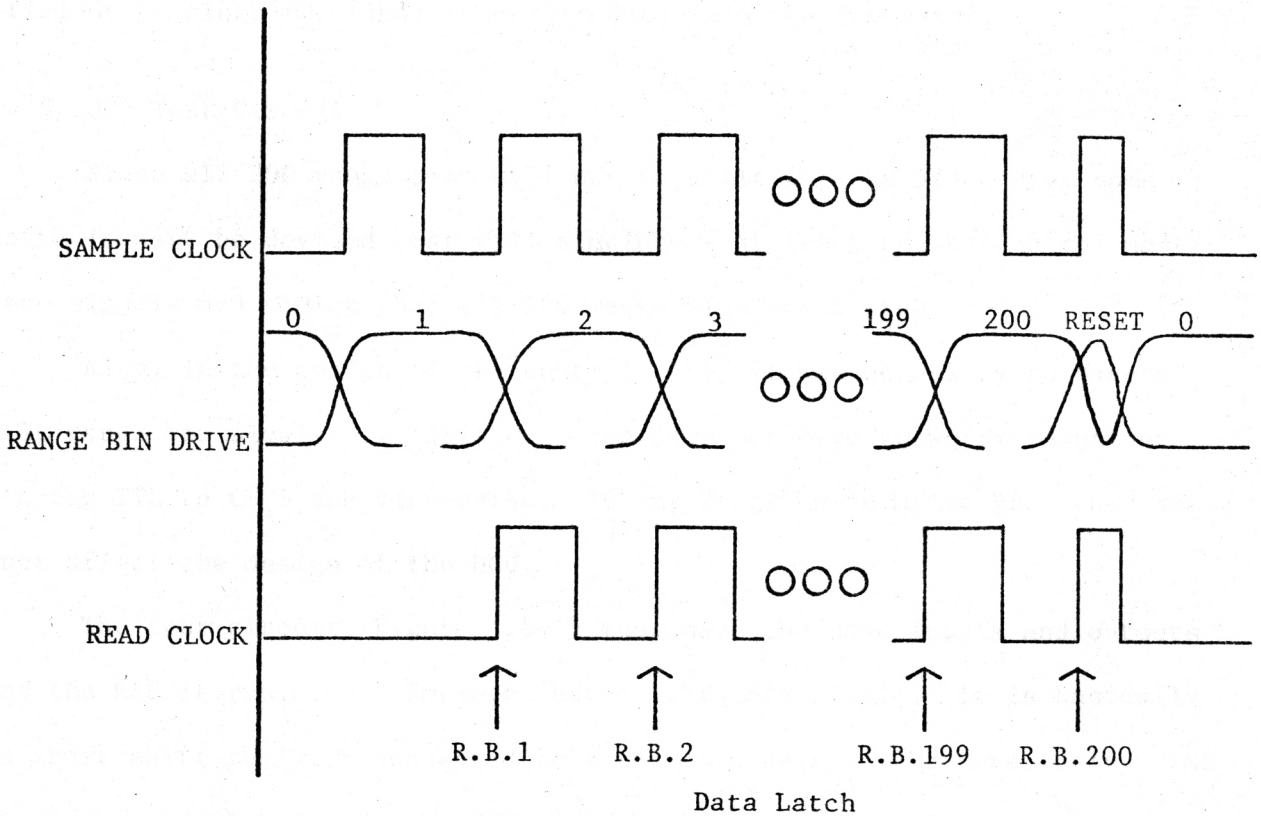


Figure 4.4-1 Timing of READ and SAMPLE CLOCK

to step to the 201st range bin. This initiates the RESET pulse. Note that the sample clock's rising edge triggered the reset. Immediately afterwards, the sample clock is shut off, causing a small glitch. This glitch is sufficient to clock the final range bin data into the Processor.

4.5 DCU Test Circuit

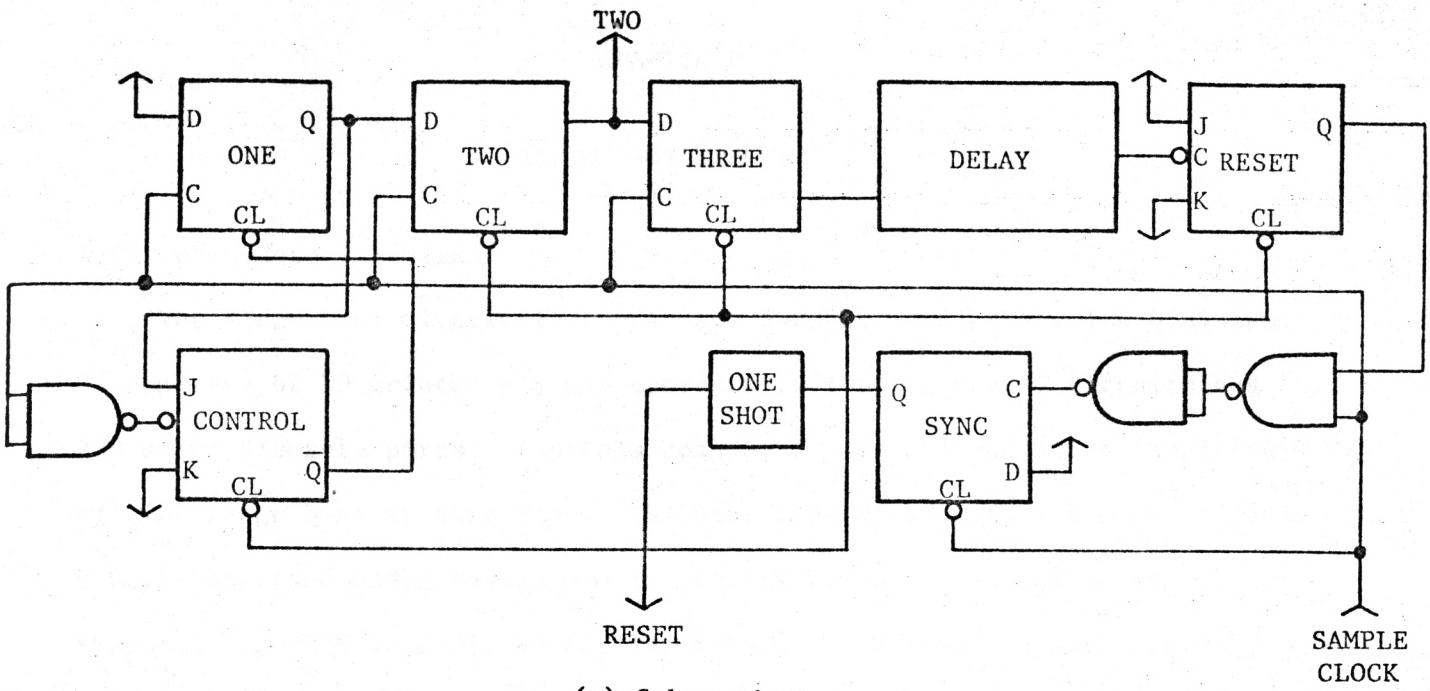
Since all 200 range bins will not be built for the prototype, some circuit must be devised that will simulate - at least to the control unit - the signals and timing that all 200 range bins would give.

Also, in the design of the control unit, it was necessary to have a TTL range bin simulator. This way, one does not have to worry about interfacing TTL to CMOS and vice-versa. If any "bugs" were in the RBC, they would not affect the design of the DCU.

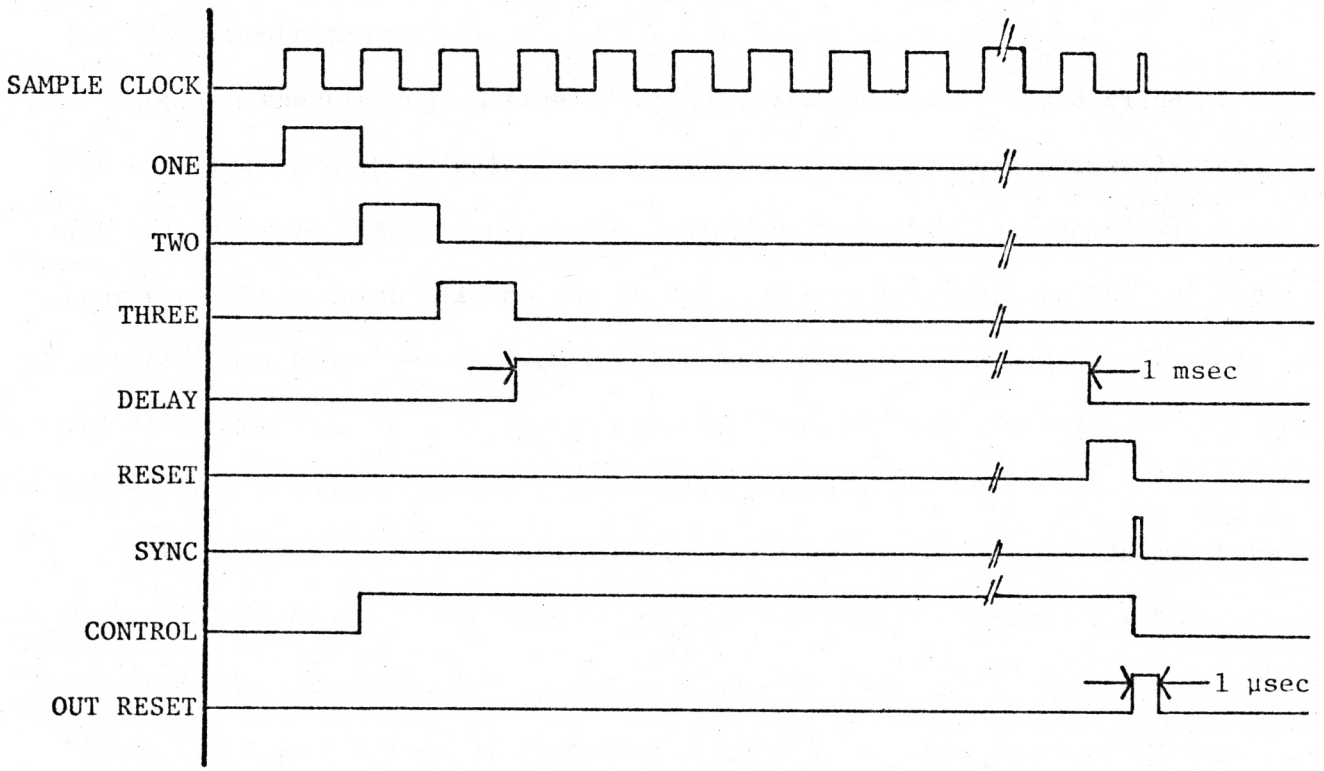
The test circuit (Figure 4.5-1) must have the same inputs and outputs as the RBC it replaces. Implementation is fairly simple. It is basically a short shift register connected to a variable delay. The total delay time is set to be the same as the 200 range bins. The only difficulty encountered is due to the asynchronous nature of the delay. This is taken care of by the SYNC FF and a few gates.

4.6 Test Results

All testing indicated that the DCU is functioning normally. The only thing that one must be careful of is proper filtering and grounding of the 5 volt logic supply. The 18.6 MHZ clock tends to appear on the control signals if proper shielding is not observed.



(a) Schematic.



(b) Timing diagram.

Figure 4.5-1 Test Circuit.

CHAPTER V

RANGE BINS CIRCUIT

5.1 Introductory Remarks

The Range Bins Circuit is by far the largest part of the I & Q system. It consists of 13 printed circuit boards with 175 integrated circuits and 338 other discrete parts. For this reason, it was decided not to implement all 200 range bins at this time. The prototype works with a RBC of 16 range bins. This is a small enough number to work with, yet is sufficient for testing. The RBC is designed for later modular expansion. One merely plugs in additional boards.

5.2 Implementation

Due to the tremendous size of the proposed system, it was decided at the outset to use CMOS logic. This logic family was chosen primarily for its extremely low power consumption. Sixteen range bins per board was chosen as the modular size as the 16 range bin capacitors, the FET switches, counters, and other necessary gates fit on a reasonably sized board. This means 12 ½ boards will be needed in the final version. Some circuitry common to all boards goes on the Translator board.

The counters are CMOS 4017 Johnson counters. These are decade counters with decoded outputs. The Johnson counter basically consists of a BCD counter and a demultiplexer in one package. The configuration shown in Figure 5.2-1 is a method of cascading counters. In this interconnection, the 25 separate counters act as one 200 step counter. Two of the outputs, 0 and 9, on each chip are used to control the cascade. Therefore, each chip can drive 8 range bins. For modular expansion, three signals must be transferred from board to board to control the counters:

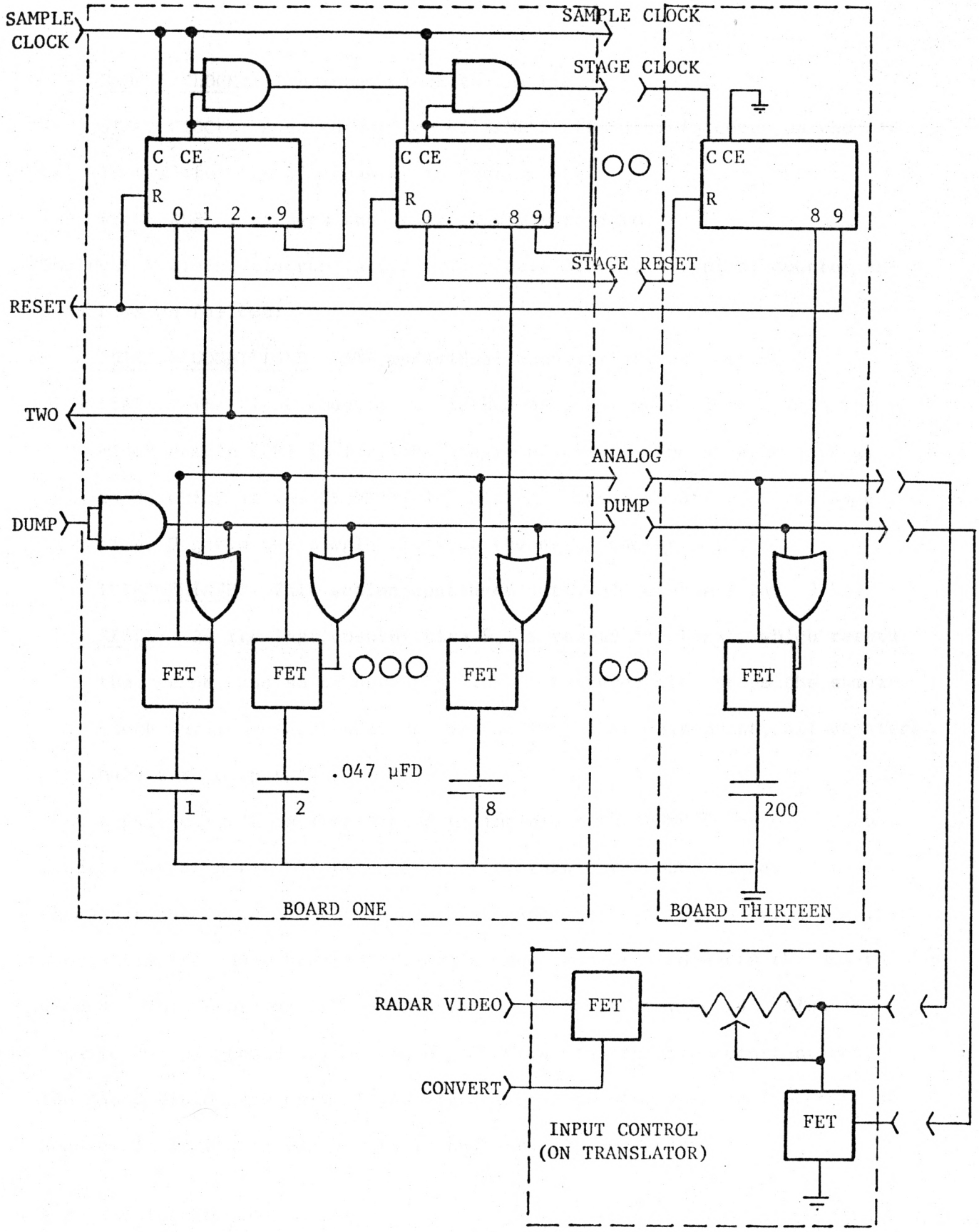


Figure 5.2-1 Range Bins Circuit.

SAMPLE CLOCK: The input clock to the RBC.

STAGE CLOCK: A gated version of SAMPLE CLOCK. This comes on when it is time for the n^{th} counter to start.

STAGE RESET: Resets the stage counters to zero.

The system timing diagram is shown in Figure 5.2-2. A typical counter sequence is as follows:

INITIAL CONDITIONS: All individual counters are on zero.

START: The first counter is clocked by the sample clock. When the clock enable (CE) is low, the stage can count. The stage counts up to 9, which drives CE high, inhibiting further counts. At the same time, 9 gates the sample clock to the next counter.

INTERMEDIATE: This action continues until all counters have 9 high.

RESET: As the last counter hits 9, it resets the first, which resets the second, and so on down the line. The reset also stops the sample clock until another radar trigger arrives. At this point, all counters have zero outputs.

A gate circuit is also needed to implement the DUMP function. Each control input to the FET switches is an OR gate. The DUMP signal is tied through these gates to every range bin. When the DUMP signal goes high, it shorts all the range bins to the analog bus, and then connects the bus to ground. This shorting FET is located on the Translator board. Also located on this board is the RADAR VIDEO gate and the time constant pot. The RADAR VIDEO gate only allows video signal to pass when an Integrate or Read cycle is taking place. It is not strictly necessary.

5.3 R-C Integration

The process called "range bin integration" is in fact not really integration. Figure 5.3-1 (a) shows the response of a R-C integrator to

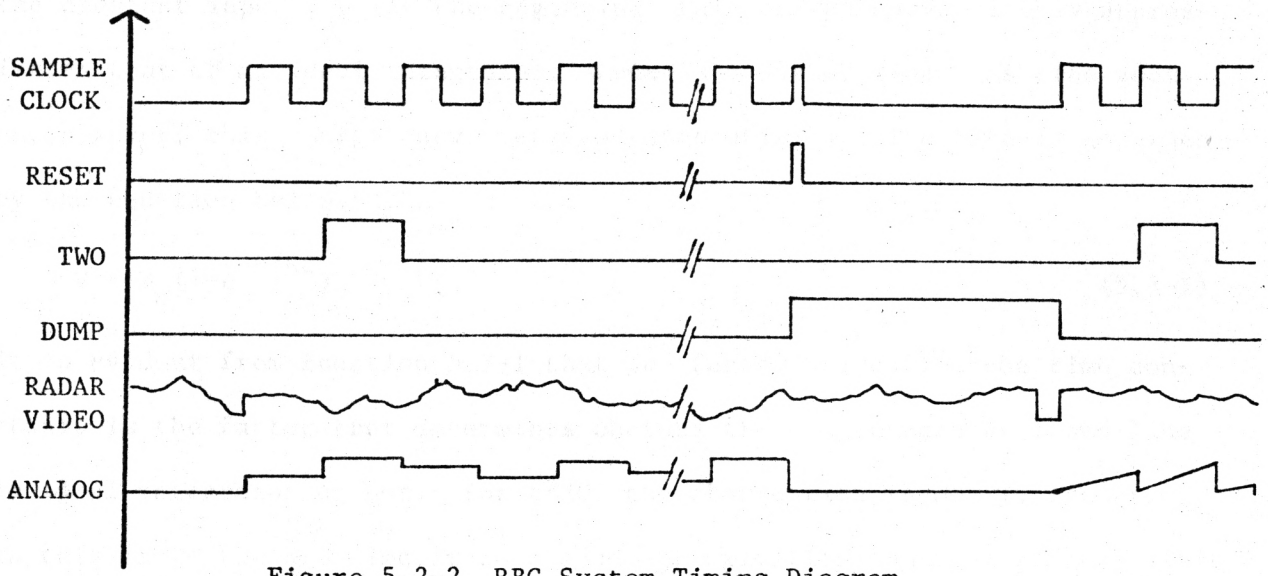
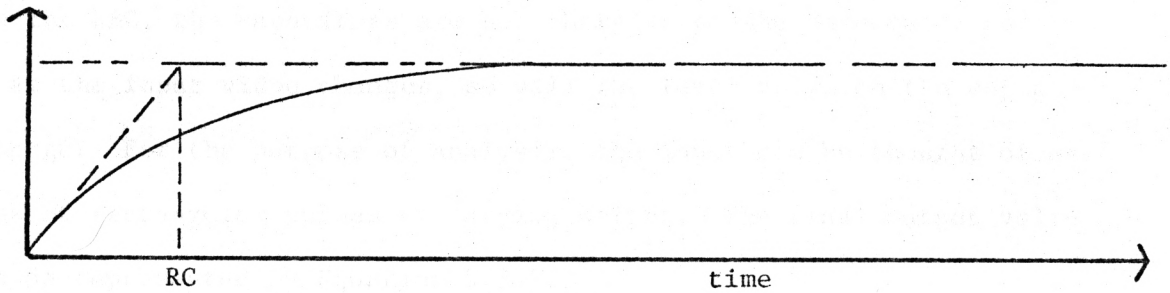
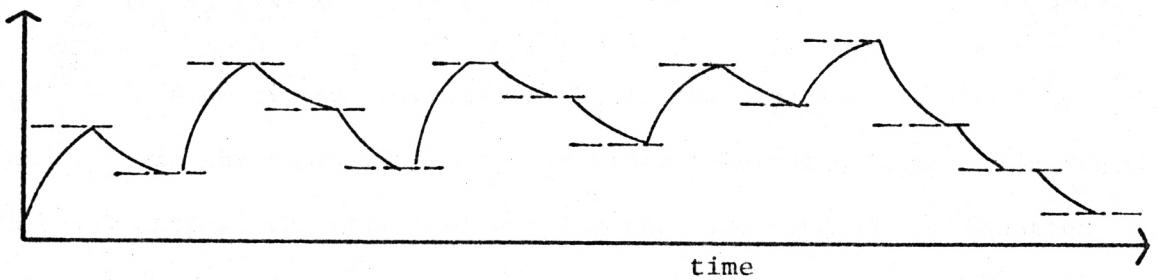


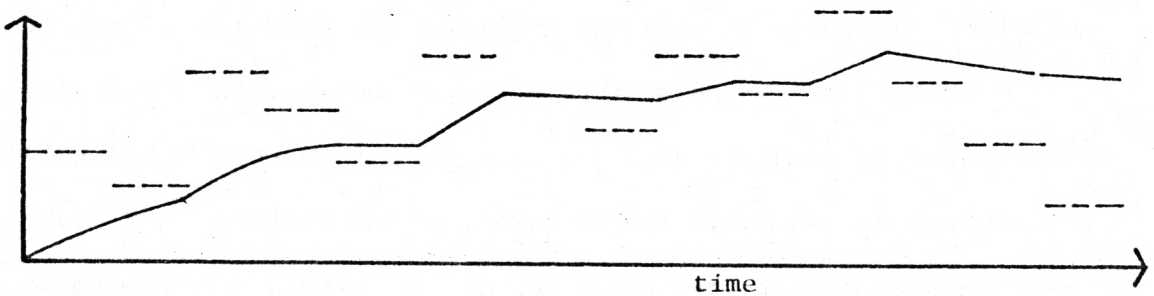
Figure 5.2-2 RBC System Timing Diagram



(a) Charge of capacitor.



(b) RC small.



(c) RC large.

Figure 5.3-1 R-C Integration.

the constant input V_o. At the beginning, this charge curve closely approximates that of an ideal integrator, shown as a dashed line. As time goes on, however, this charge curve behaves exponentially. The rate is governed by the equation below.

$$V = V_o(1-e^{-t/RC}) \tag{5.3-1}$$

It is evident from Equation 5.3-1 that the factor RC, called the time constant, is the factor that determines whether the R-C integrator looks like an ideal integrator or not. For $t<RC$, the charge time is nearly linear. In this range the R-C circuit is a good approximation to an integrator. This result does not hold for $t>RC$.

In the RBC, the capacitors are not charging to the same value each time. As the input video changes, so will the level to which the capacitors charge. For the purpose of analysis, the input can be thought of as a series of rectangular pulses of varying height. The final output voltage can be represented by Equation 5.3-2.

$$V_f = \sum_{i=1}^{n} (V_i - V_{f-1})(1-e^{-t/RC}) \tag{5.3-2}$$

V_f is the final value of the integration, V_i is the amplitude of the i^{th} pulse, and V_{f-1} is the amplitude of the previous integrated value. Figures 5.3-1 (b), (c) explore the effect of varying the time constant on Equation 5.3-2. In (b), the time constant is less than τ, the integration time per pulse. It can be seen that the capacitor has time to charge or discharge fully to the input pulse. The output is therefore the level of the n^{th} pulse. Clearly, this is wrong. In (c), the time constant is much greater than τ. Here the capacitor cannot charge so quickly. The integration is seen to be more nearly linear than in (b). However, neither case is true integration. If it were, the value would monotonically increase. RC has

been chosen to be about ten times greater than τ. This value allows fairly good results.

5.4 Test Results

No problem was encountered with any of the control logic. The range bin capacitors will charge up to some slight extent if the ANALOG line is left floating. This noise charge is not enough to cause problems; moreover, a floating ANALOG line is never allowed anyway. The Range Bins Circuits are operational as designed.

CHAPTER VI

THE ANALOG-TO-DIGITAL CONVERTER

6.1 Introductory Remarks

The A/D Converter is the quantizer portion of the interface. It is designed to distinguish 16 discrete voltage levels, which implies a 4-bit binary word. Sign information is not needed as the video information is not allowed to go negative. The A/D Converter subsystem had two main sections: the Sample and Hold, and the actual A/D Converter.

6.2 Sample and Hold

It is desirable that the voltage that the A/D Converter is attempting to digitize be held constant during the conversion process. Therfore, a sample and hold (S/H) is indicated. The most rudimentary form of a sample/hold is a FET switch and a capacitor. The capacitor charges to the input voltage and tracks it until the FET switch shuts off during the Hold state. This form of a S/H has several disadvantages. Any attempt to load the capacitor during the Hold state will discharge it. A buffer amplifier placed on the output of the S/H solves this problem. The amplifier is a 8007C FET input op-amp. A FET input type op-amp is needed to minimize the input bias current of the op-amp. Since the source of the ANALOG signal is the output of a R-C integrator, it is necessary to buffer it also. To see why this is necessary, consider the case where range bin one has a large voltage, and range bin two has a small voltage. The S/H will charge up until the voltage on the two capacitors is the same. Note that this voltage is not the original voltage, but somewhat less, since $C = Q/V$. When range bin two is sampled, the S/H capacitor will actually charge up range bin two's capacitor. Clearly, another buffer amplifier is needed. The

sample signal is the SAMPLE CLOCK. Thus, the S/H samples for 2.69 μsec and holds for 2.69 μsec. A diode is included to clamp the input voltage to prevent it from ever going negative, which would destroy the FET switch. In normal operation, the diode never turns on.

6.3 A/D Converter

The A/D circuit shown in Figure 6.3-1 is a variation of a circuit described in Electronics[3]. A stable reference voltage is compared against the input on IC1a. The output of IC1a is A, the most significant bit of the digital output. The value of bit A sets up the reference for IC1b in the manner shown in Figure 6.3-2. Since the outputs of the LM339 comparators are open collector, the output voltage at A is either V_{ref} or ground. The two cases lead to a comparator reference of $V_{ref}/4$ or $3V_{ref}/4$, since the input resistors behave like a voltage divider. The other comparators have weighted inputs from the more significant bits. Bit D, the least significant bit, has inputs from bits A, B, and C of weights ±1/4, ±1/8, and ±1/16, respectively. After a time solely dependent upon the comparator speed, the digital output is formed. The second bank of comparators (IC2) is used to buffer the output. In doing so, the outputs are inverted. It is therefore necessary to re-invert these with a 7404 hex inverter. Hysteresis is used to prevent switching on noise.

6.4 Test Circuit

Figure 6.4-1 shows the manner in which the A/D Converter can be tested up to speed. A full conversion must be made in 5.38 μsec, the SAMPLE CLOCK period. To test this, the SAMPLE CLOCK is divided by two. The non-inverted output is used as the analog input to the A/D. By changing the scaling pot of the A/D, a transition between zero and any of the sixteen possible levels

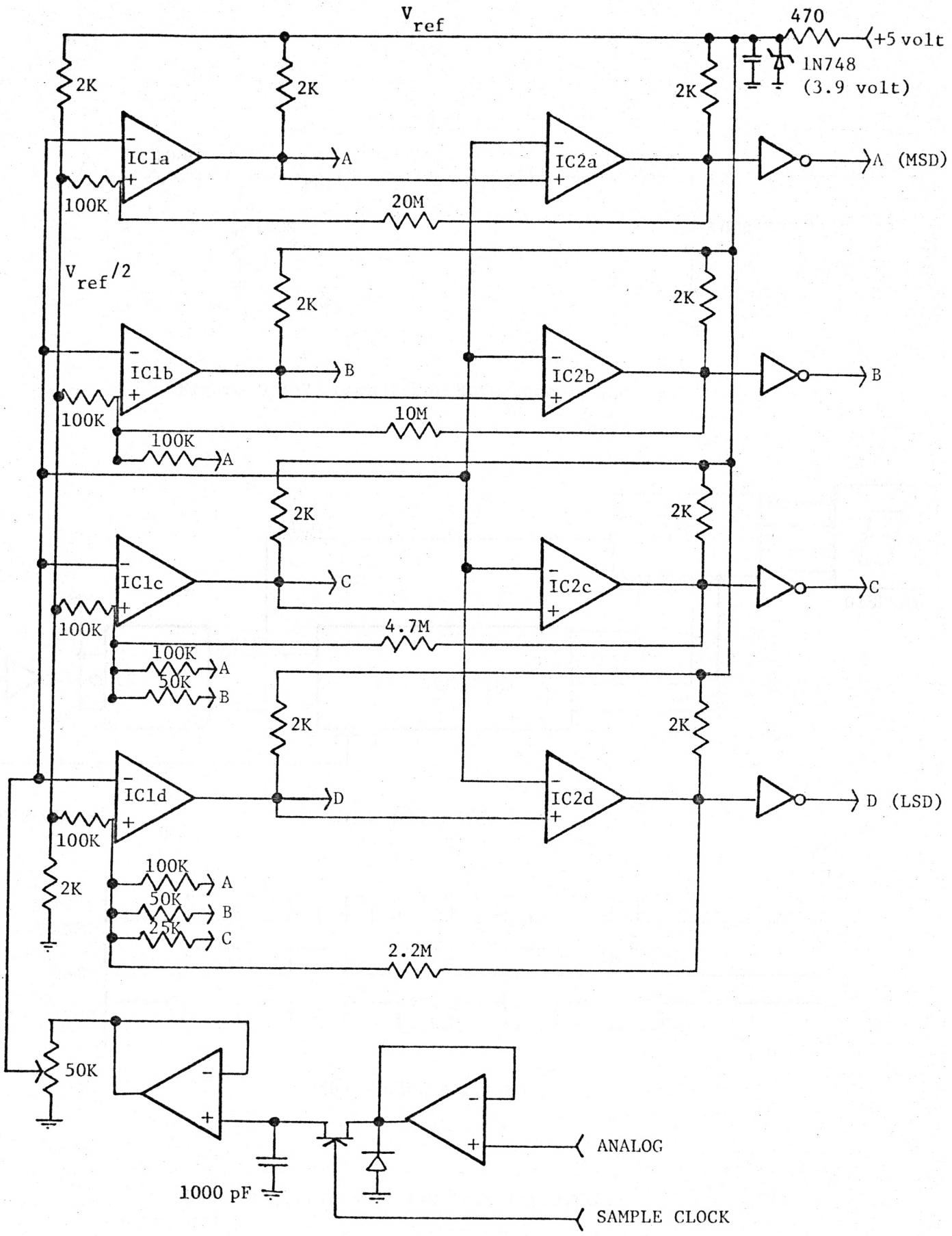


Figure 6.3-1 Analog-to-Digital Converter

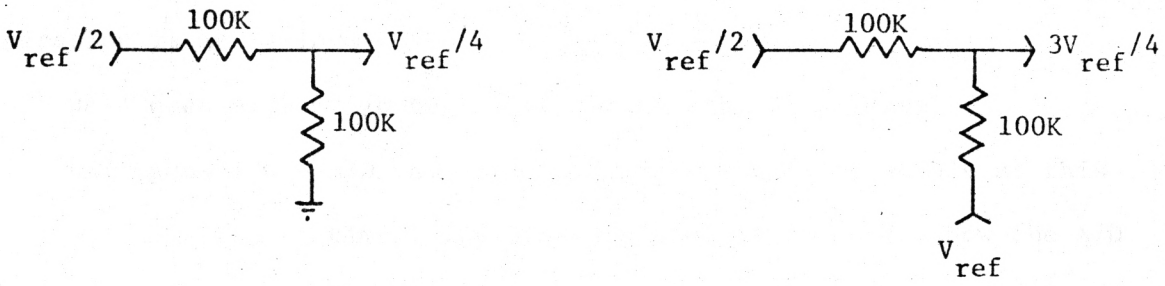
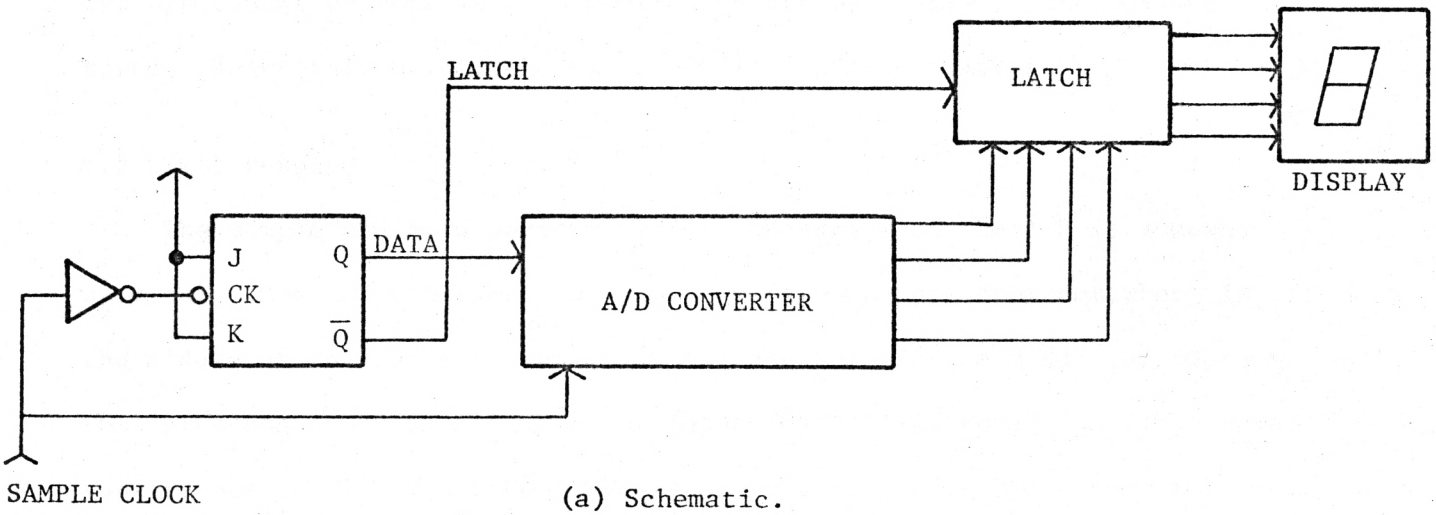
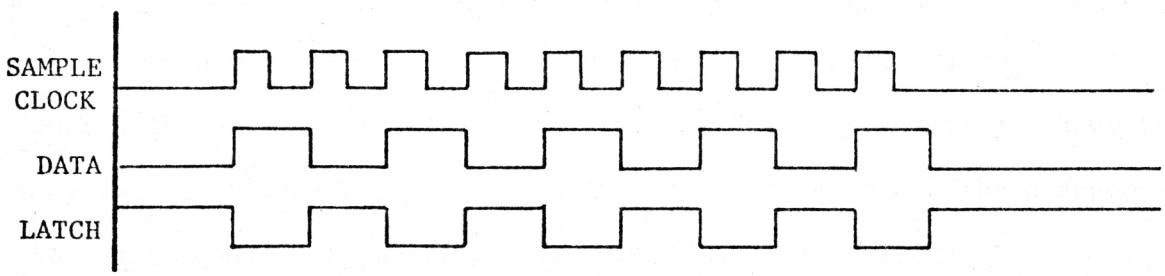


Figure 6.3-2 Comparator Reference Weighting.



(a) Schematic.



(b) Timing diagram.

Figure 6.4-1 A/D Test Circuit.

can be made. An uninverted form of this signal is fed to a positive edge triggered latch, which drives a seven segment display. The sequence of operation is as follows:

DATA goes high - A/D begins to convert the high level

DATA goes low - A/D value for high DATA should be stable at this time. The binary output is latched. Now the A/D begins to convert the DATA low input.

DATA goes high - A/D converts. Binary is not latched.

As the input clock frequency is increased, a point will be reached where the A/D cannot convert in the input clock period. This is the maximum speed. Above this point, the display will begin to flicker.

6.5 Test Results

The sample and hold performs well. Operation of the A/D is somewhat marginal. Most of the time, the input voltage changes from somewhere in the middle of one quantization level to somewhere in the middle of another. This presents no problem. When the input level jumps to a transition point between one level and another, things are not defined. The output may oscillate between one level and the other. This is still legitimate operation, as the processor will pick one value or the other, and either is correct. The only major glitch occurs on the 7 to 8 transition. Here the binary output changes from 0111 to 1000. All bits change. There appears to be a intermediate transition (e.g., 0111 to 1011 to 1000).

This glitch is caused by speed limiting in the LM339 comparators. A faster comparator will solve this problem. It is probable that by the time the full system is implemented, a fast 4-bit A/D will be available at a reasonable cost. This would be worth considering. At the present time,

the only commercially available A/D that comes close to meeting specifications is the Analog Devices ADC 1103-001 8-bit A/D. It sells for $473.

CHAPTER VII

THE TRANSLATOR

7.1 Introductory Remarks

This subsystem derives its name from its function - that of translating 15 volt CMOS to 5 volt TTL levels. The input gating of the Range Bins Circuit has also been placed in this section for convenience.

7.2 Circuit Analysis

The range bin gating is discussed in Chapter V and will not be repeated here. Level shifting is particularly easy using the LM319 dual comparator. It is possible to convert two ways on one chip (see Figure 7.2-1). The LM319 has an uncommitted collector output which can be tied through a load resistor to a logic voltage. One merely sets the input reference at the input logic threshold and the load resistor at the desired output level. Capacitors are placed on the reference resistors to insure against noise problems.

Figure 7.2-2 shows a block diagram of all functions on the Transistor. There are 4 CMOS/TTL converters and 4 TTL/CMOS converters. Not all of these are used, however. Spares are provided in the event that they might be needed due to future modification of the system.

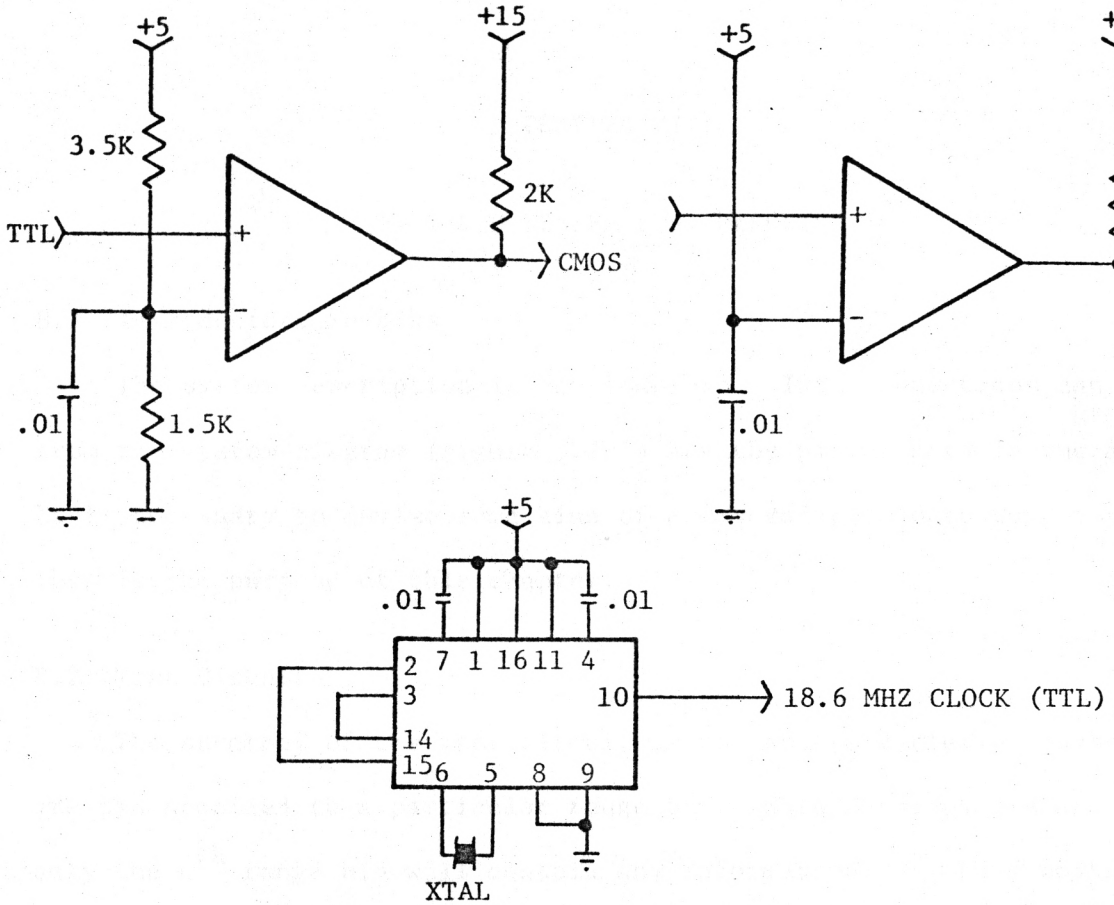


Figure 7.2-1 Translator Circuitry.

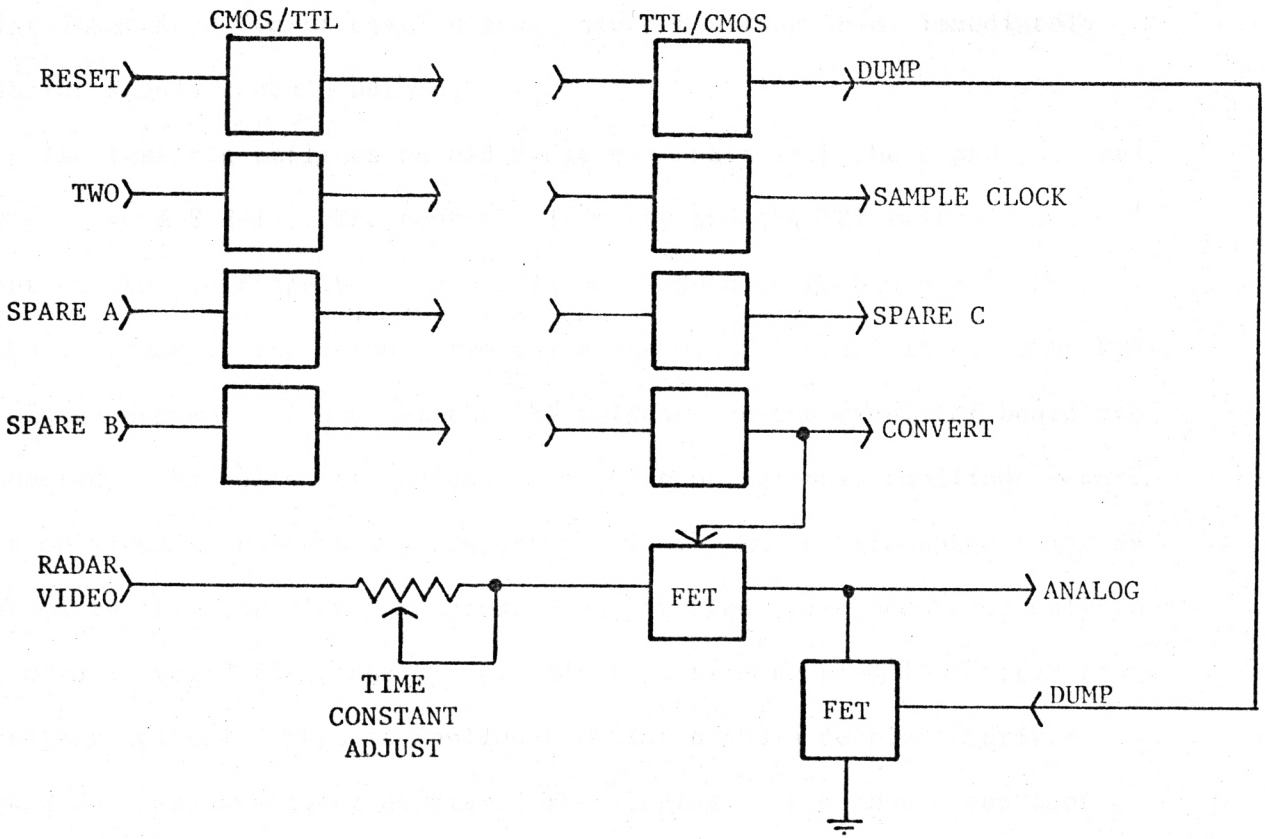


Figure 7.2-2 Translator Block Diagram.

CHAPTER VIII

I & Q SYSTEM TEST RESULTS

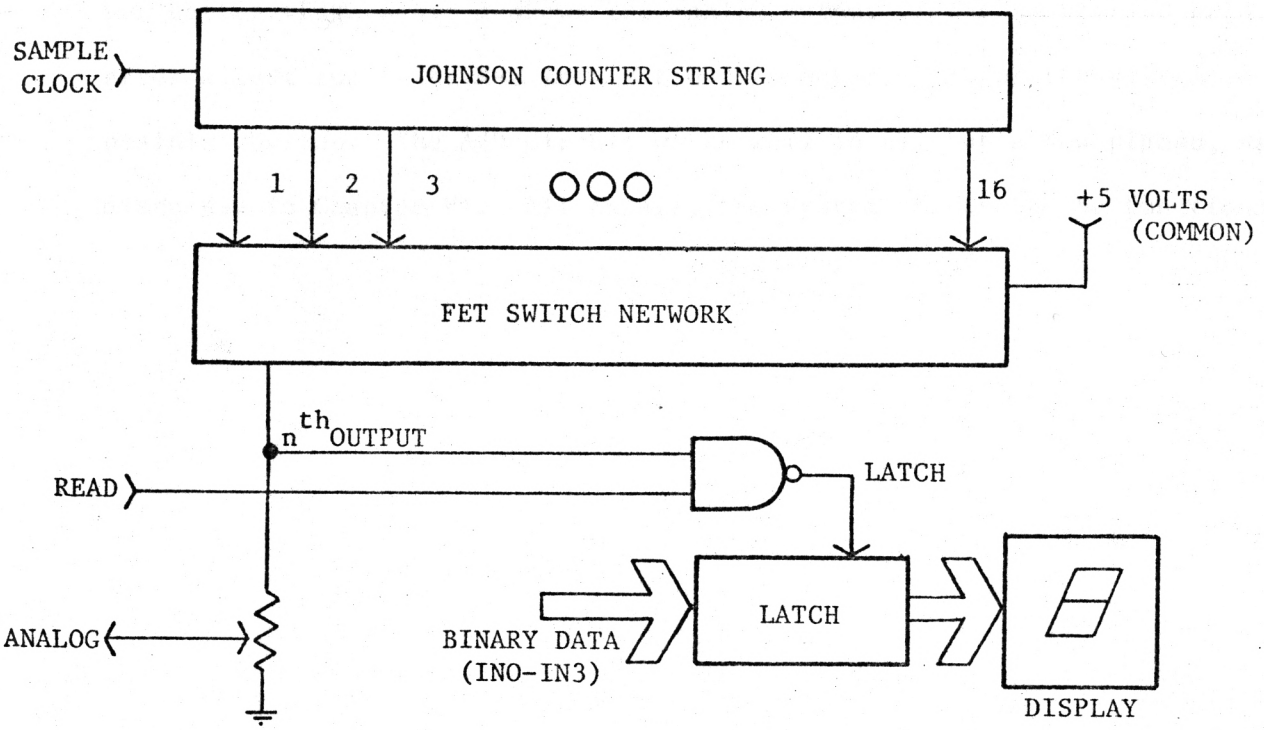
8.1 Introductory Remarks

The system description is now complete. Interconnections can be made from the system diagram (Figure 3.2-1) and the pinout data in the appendix. It is necessary to devise some kind of dummy radar load to test the system. This is the purpose of this chapter.

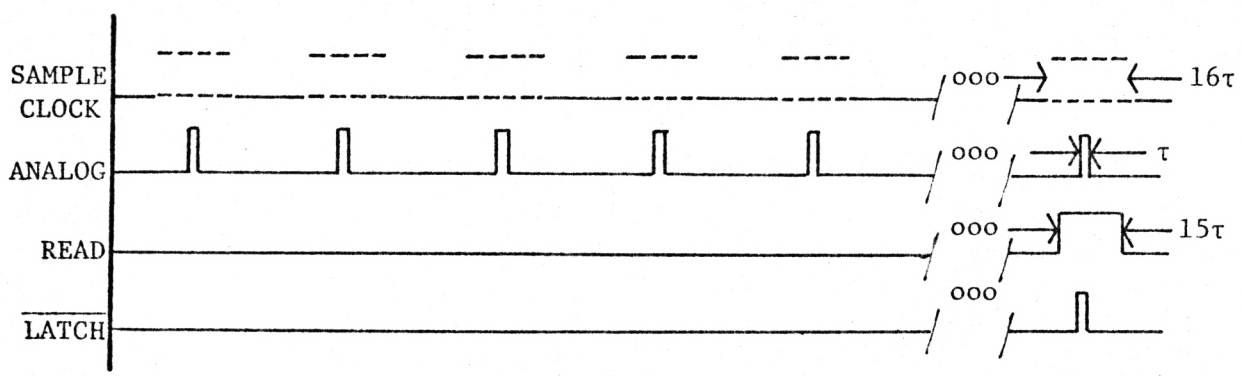
8.2 Test Circuit

The strategy of the test circuit is to input a series of pulses that are synchronized to a particular range bin. When these pulses are fed in, only the n^{th} range bin will contain any information. If this works, it should indicate that radar video data will also integrate correctly. The pulse input is a "worst case" signal, since the range bins immediately adjacent should contain nothing.

The test rig utilizes an old range bin board with the capacitors removed (Figure 8.2-1). The control circuitry and the FET switches are identical to the range bin circuit in use. Both range bin boards are wired in tandem. The output from any range bin FET (call it n) is hooked to a grounded pot. Since all the FET switches on the simulator board are connected to +5 volts, the output is a pulse of variable amplitude occurring only during range bin n's aperture time. The unattenuated pulse is Anded with the READ signal to produce an inverted pulse occurring only when the data is valid for range bin n, and it is time to read (50 integrations have taken place). This is applied to a latch and a decoder - driver hooked to a seven-segment display. The display should show a constant number at all times.



(a) Block Diagram



(b) Timing Diagram

Figure 8.2-1 Test Circuit for I & Q System.

8.3 Test Results

All control and range bin circuitry works as well as designed, if not better. Figure 8.3-1 shows the analog output of the sample and hold after a test run. The R-C integration characteristics of the system is plainly obvious. The A/D Circuit works well in all but a few places, as discussed in Chapter VI. All in all, the system appears to be functional.

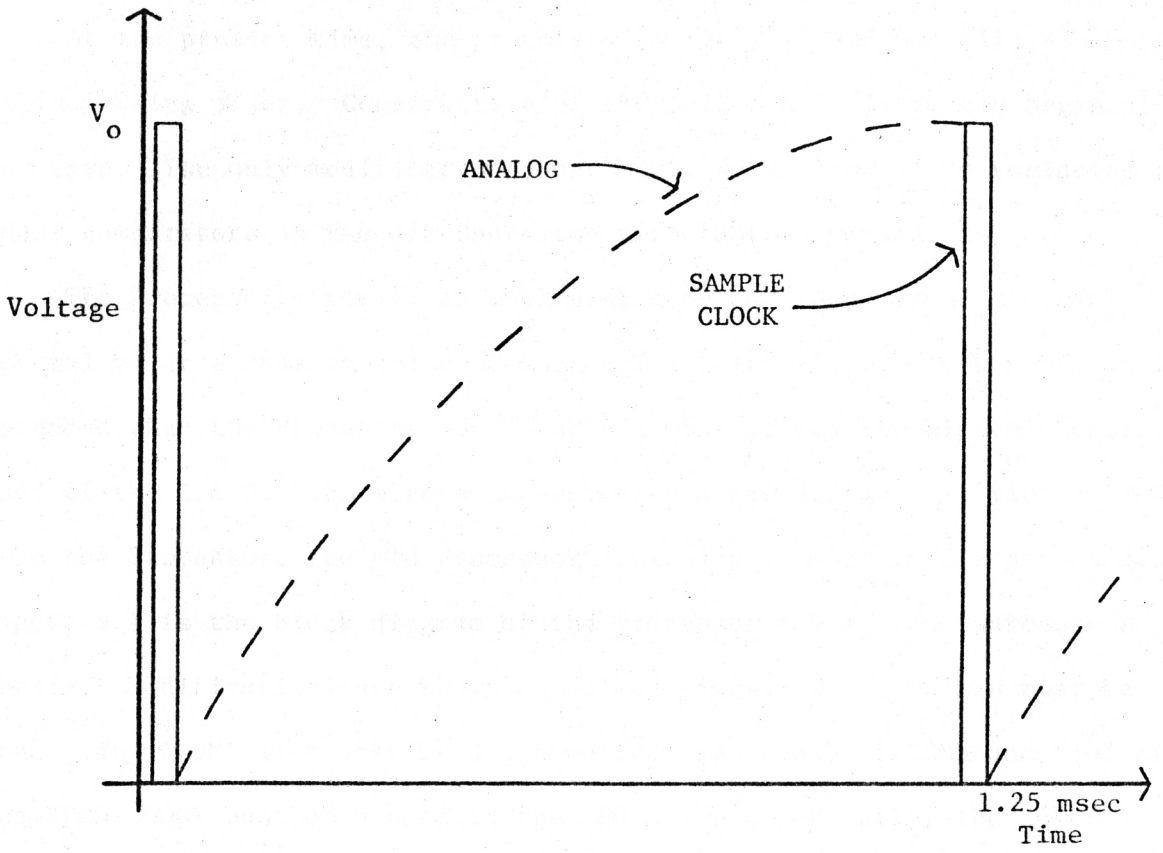


Figure 8.3-1 I & Q System Test Results.

CHAPTER IX

CONCLUSION

At the present time, the prototype Integration and Quantization Unit is in working order. Construction of the full scale system can begin at any time. The only modifications that might be advisable are replacing the LM339 comparators in the A/D Converter with faster comparators.

The Processor circuit, as implemented by Carl Andreasen, contains several major errors in the Processor - I & Q interface. It was originally intended that the Processor would include what is now the Digital Control Unit of the I & Q. The errors necessitated a new design. To tie the I & Q to the Processor, the old Processor control unit must be disconnected. Figure 9.1 is the block diagram of the Processor taken from Andreasen's thesis. Modifications are shown as dashed lines. Three things must be done: The COUNT line must be disconnected from pin 9 of ICMM and tied high. The READ CLOCK must be placed in the SHOLD input. Finally, the internal control line DEVAZDONE is run to the I & Q. It becomes the DAZ signal. The Processor signals $\overline{\text{ONE}}$, $\overline{\text{ZERO}}$, READY, $\overline{\text{DUMP}}$, AND DUMP are now ignored.

With the completion of this Report, all portions of the interface are designed and in working order with the exception of the logarithmic amplifier. This is the next design step. To complete the interface, a person must be found to construct the remaining range bin boards, design the logarithmic amplifier, and tie the system together. A major overhaul of the existing radar is essential if reliable operation is desired.

This Report has attempted to document the design and actual construction of the Integration and Quantization Unit. The Appendix contains circuit board layouts, parts lists, and edge connector pinout data. It is hoped that this Report can also function as a manual for maintenance.

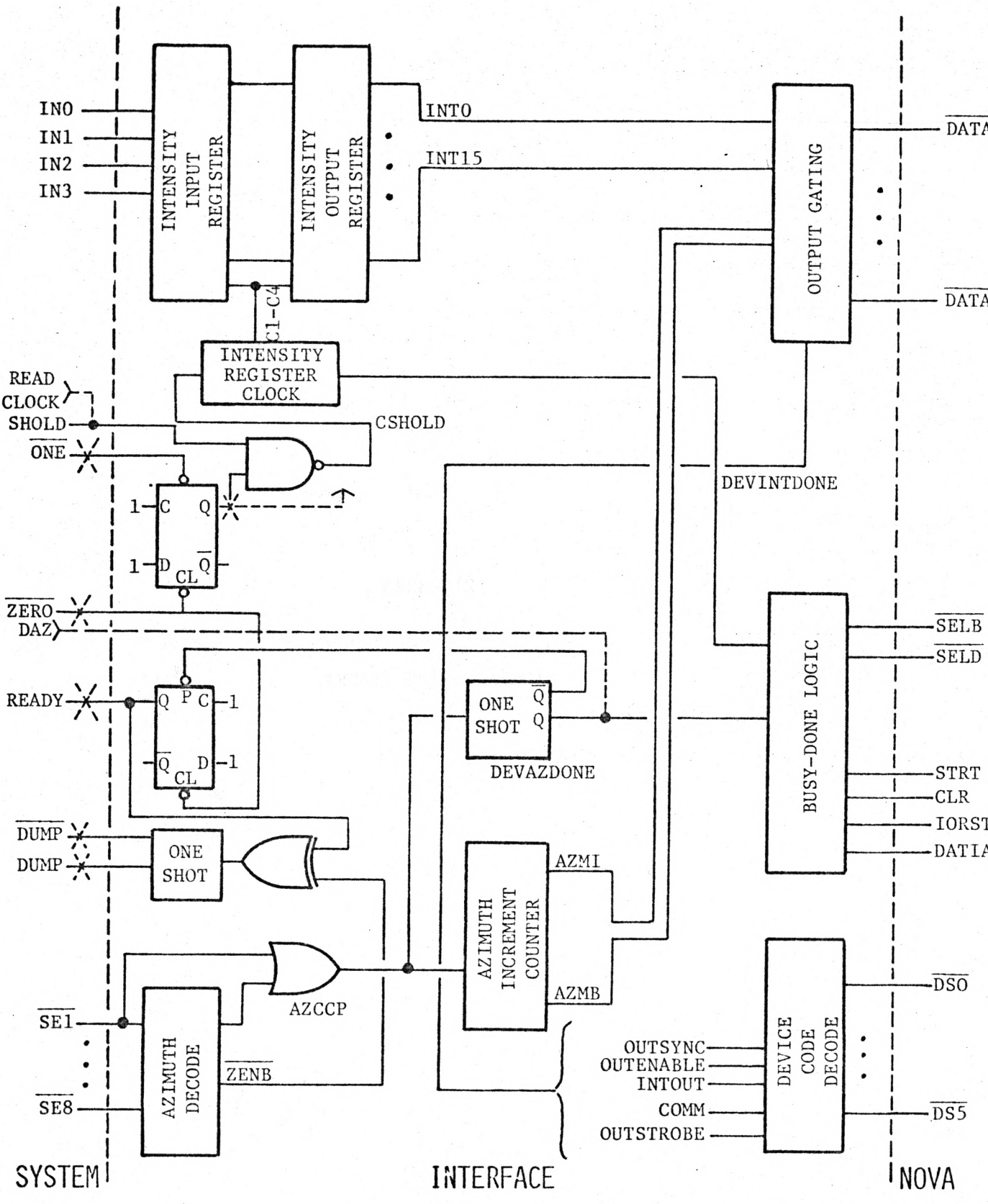


Figure 9.1 Modifications to Existing Processor.

SOURCE: Carl C. Andreasen, "The Design of a Computer Interface for a Radar Processor" (Master's Thesis, Kansas State University, 1976)

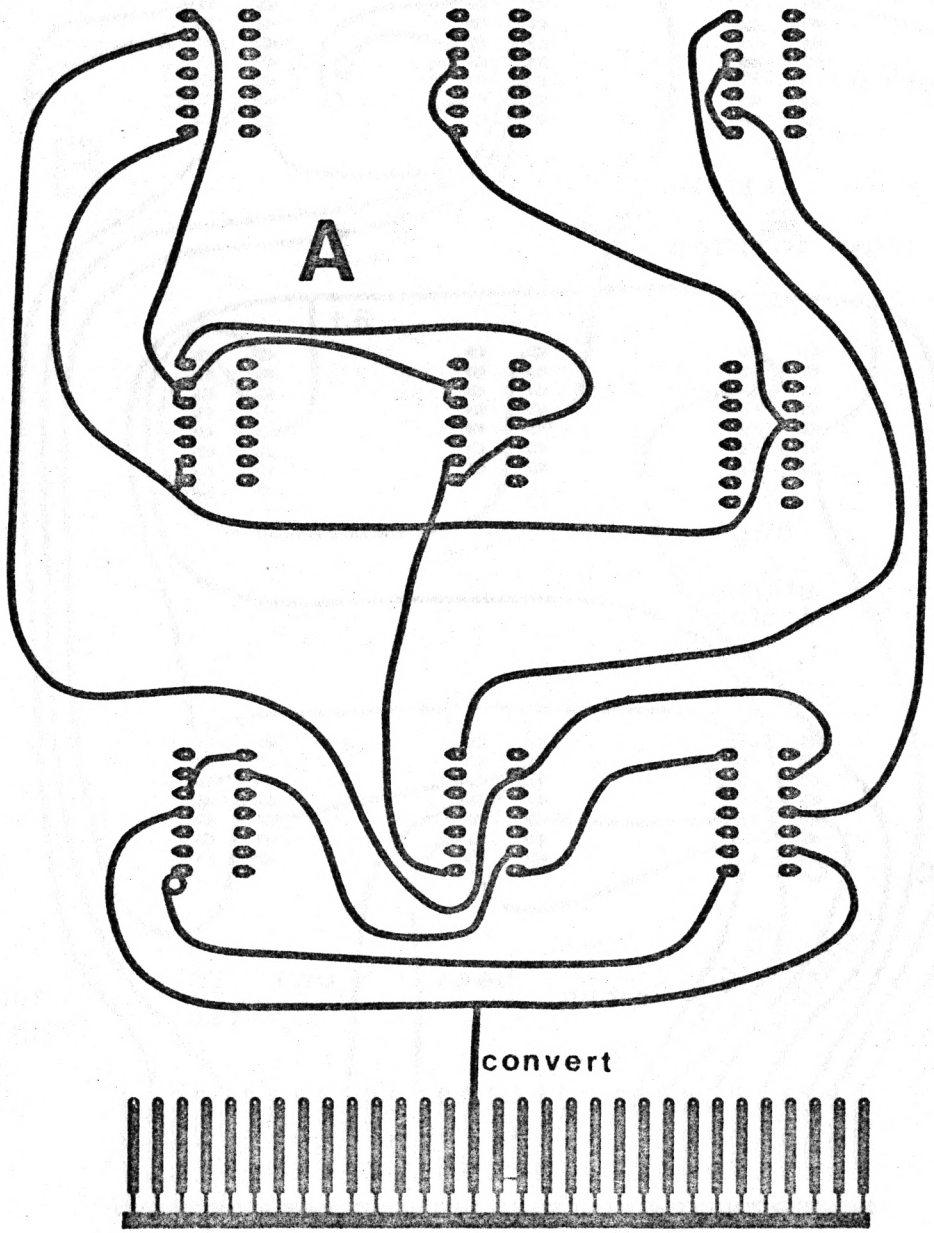
APPENDIX

CIRCUIT BOARD LAYOUTS

PARTS LISTS

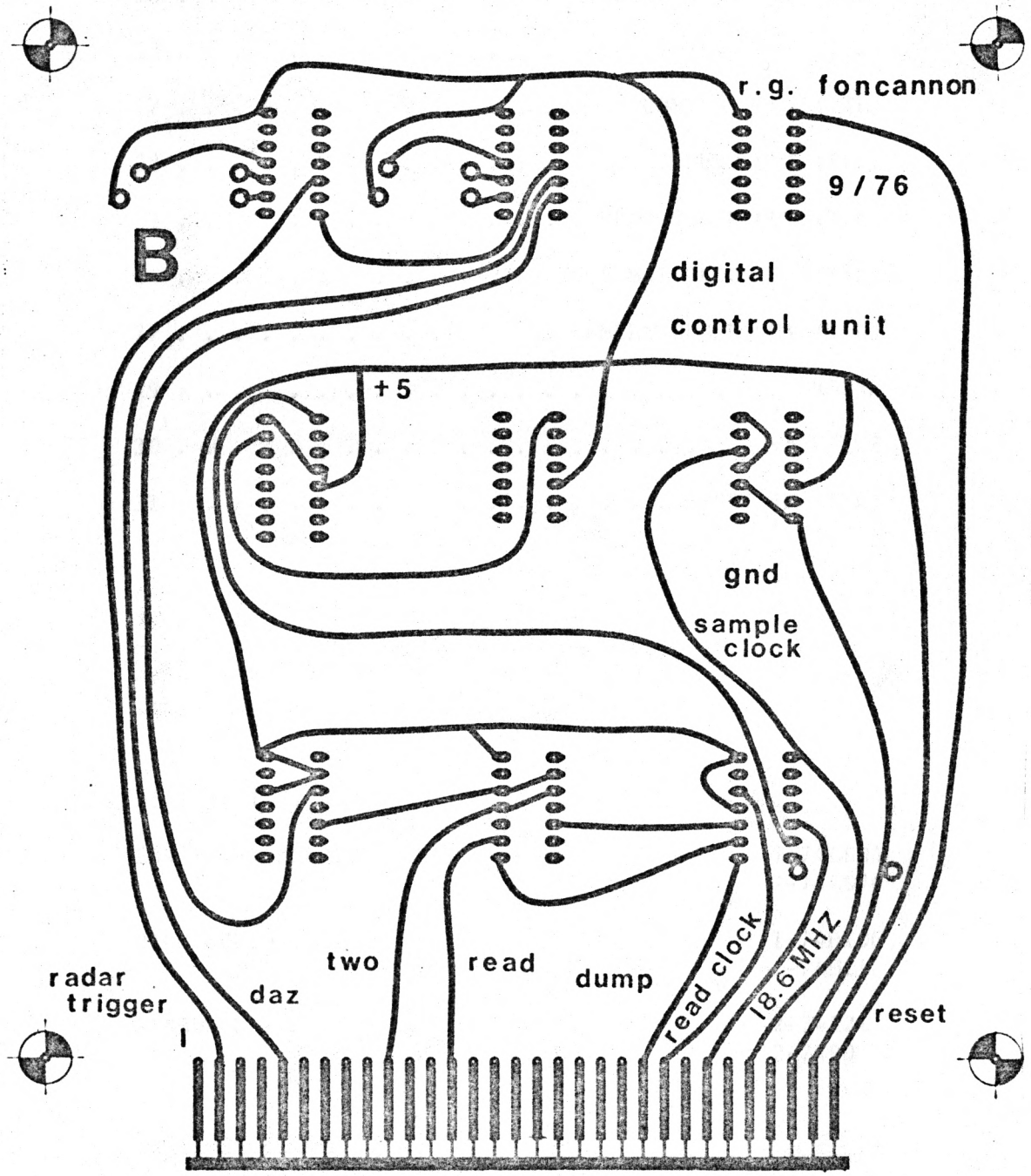
DIGITAL CONTROL UNIT

TOP FOIL



DIGITAL CONTROL UNIT

BOTTOM FOIL



DIGITAL CONTROL UNIT

Pinout

2 . . . . . RADAR TRIGGER IN (TTL)

5 . . . . . DAZ IN (TTL)

10 . . . . . TWO IN (TTL)

13 . . . . . READ OUT (TTL)

17 . . . . . CONVERT OUT (TTL)

22 . . . . . DUMP OUT (TTL)

23 . . . . . READ CLOCK OUT (TTL)

25 . . . . . 18.6 MHZ CLOCK IN (TTL)

27 . . . . . SAMPLE CLOCK OUT (TTL)

29 . . . . . GROUND

30 . . . . . +5 VOLTS

31 . . . . . RESET IN (TTL)

PARTS LIST

Digital I.C.'s

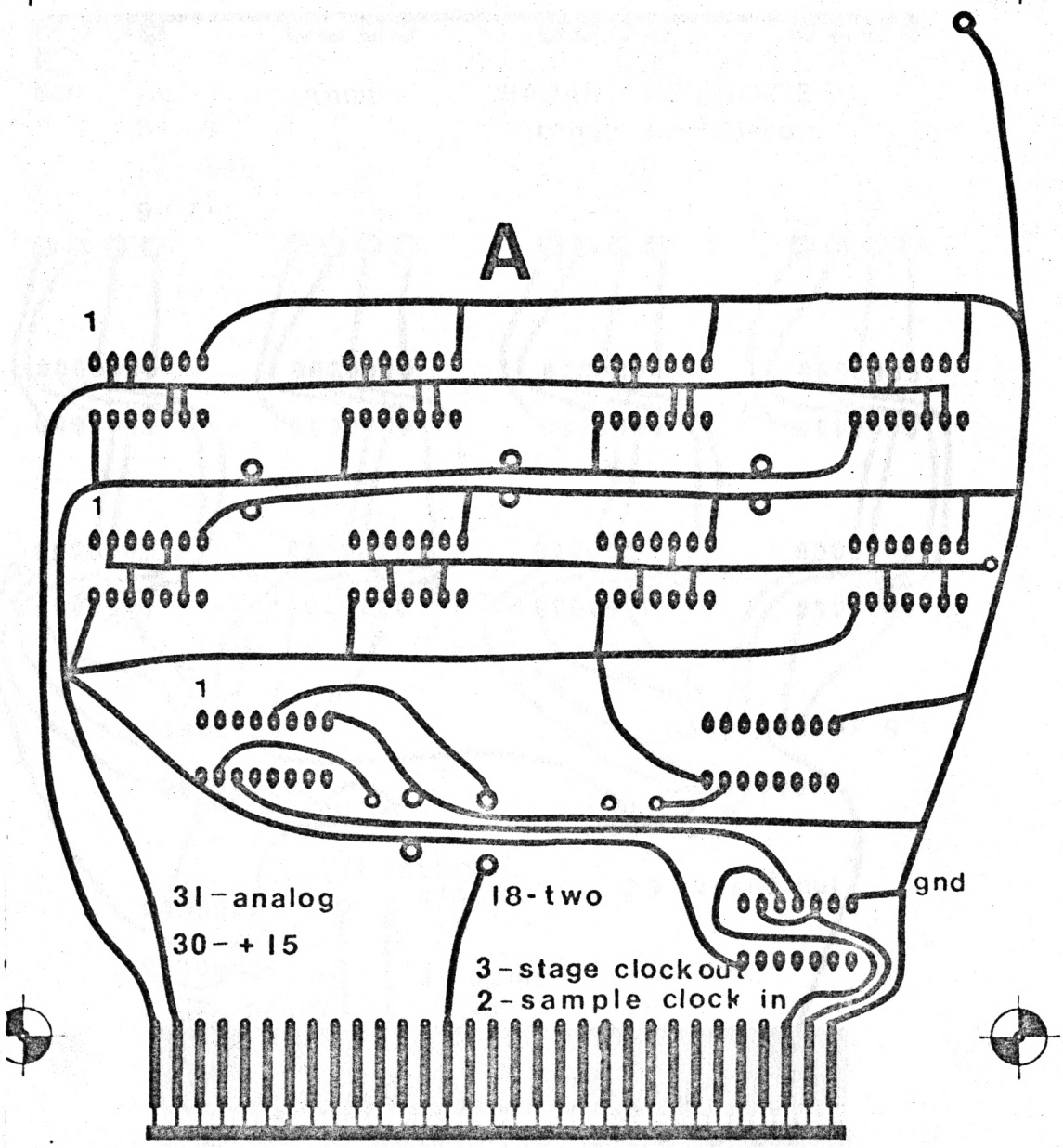
LOW POWER SCHOTTKY TTL:	1-74LS04 2-74LS74
HIGH SPEED TTL:	1-74H106 1-74H11
STANDARD TTL:	2-74121 2-7490

Discrete Parts

2-100pf capacitors
2-11K resistors

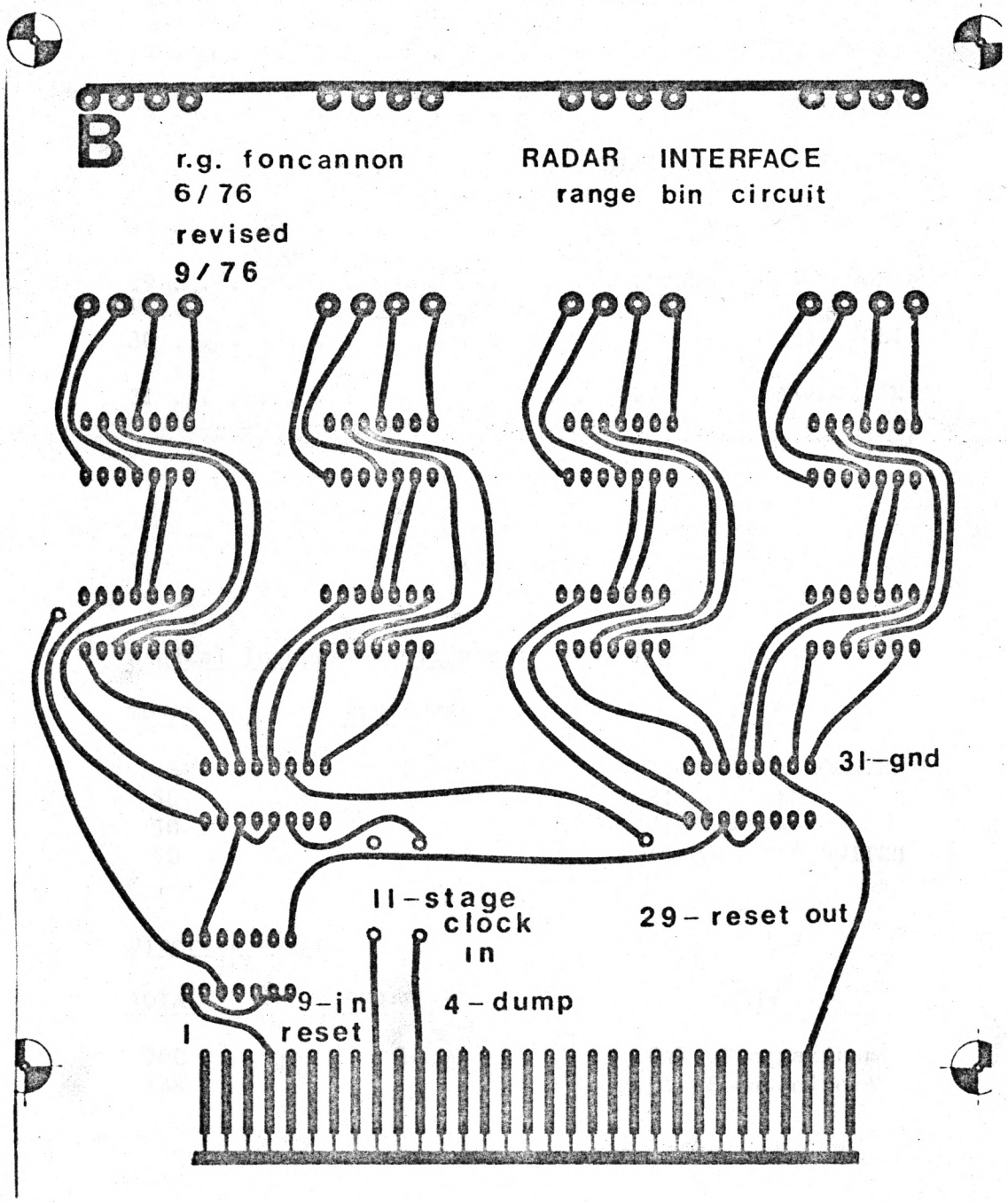
RANGE BINS CIRCUIT

TOP FOIL



RANGE BINS CIRCUIT

BOTTOM FOIL



RANGE BINS CIRCUIT

Pinout

1 . . . . . GROUND

2 . . . . . SAMPLE CLOCK IN (CMOS)

3 . . . . . STAGE CLOCK OUT (CMOS)

4 . . . . . DUMP IN (CMOS)

9 . . . . . RESET IN (CMOS)

11 . . . . . STAGE CLOCK IN (CMOS)

18 . . . . . TWO OUT (CMOS)

29 . . . . . .RESET OUT (CMOS)

30 . . . . . +15 VOLT

31 . . . . . ANALOG IN

PARTS LIST

Digital Integrated Circuits: CMOS

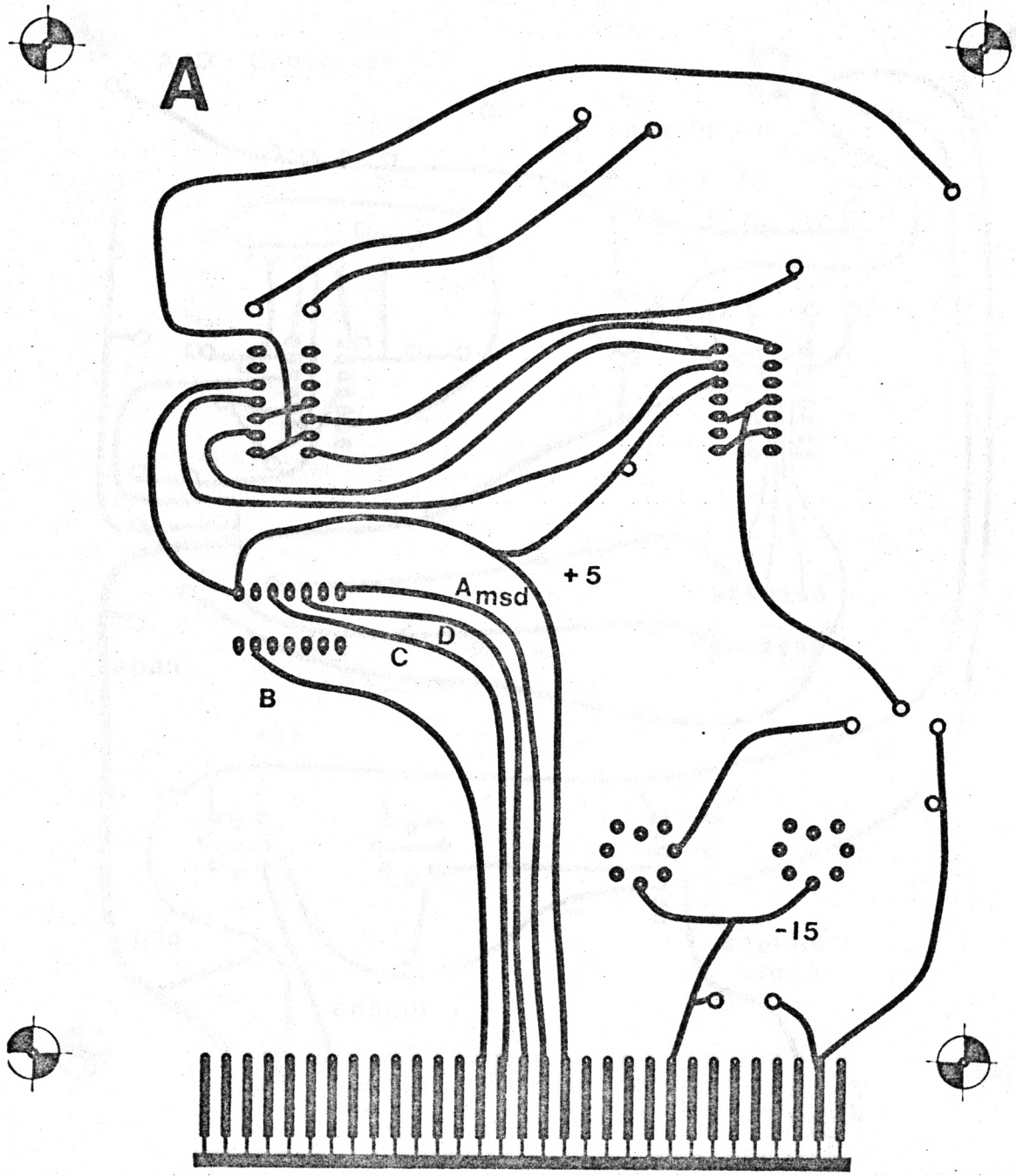
TOTAL	PER BOARD	TYPE
25	2	4017 JOHNSON COUNTER
50	4	4081 QUAD AND
50	4	4071 QUAD OR
50	4	4016 QUAD FET SWITCH

Discrete Parts

TOTAL	PER BOARD	TYPE
200	16	.047 µF capacitor
138	11	.01 µF capacitor

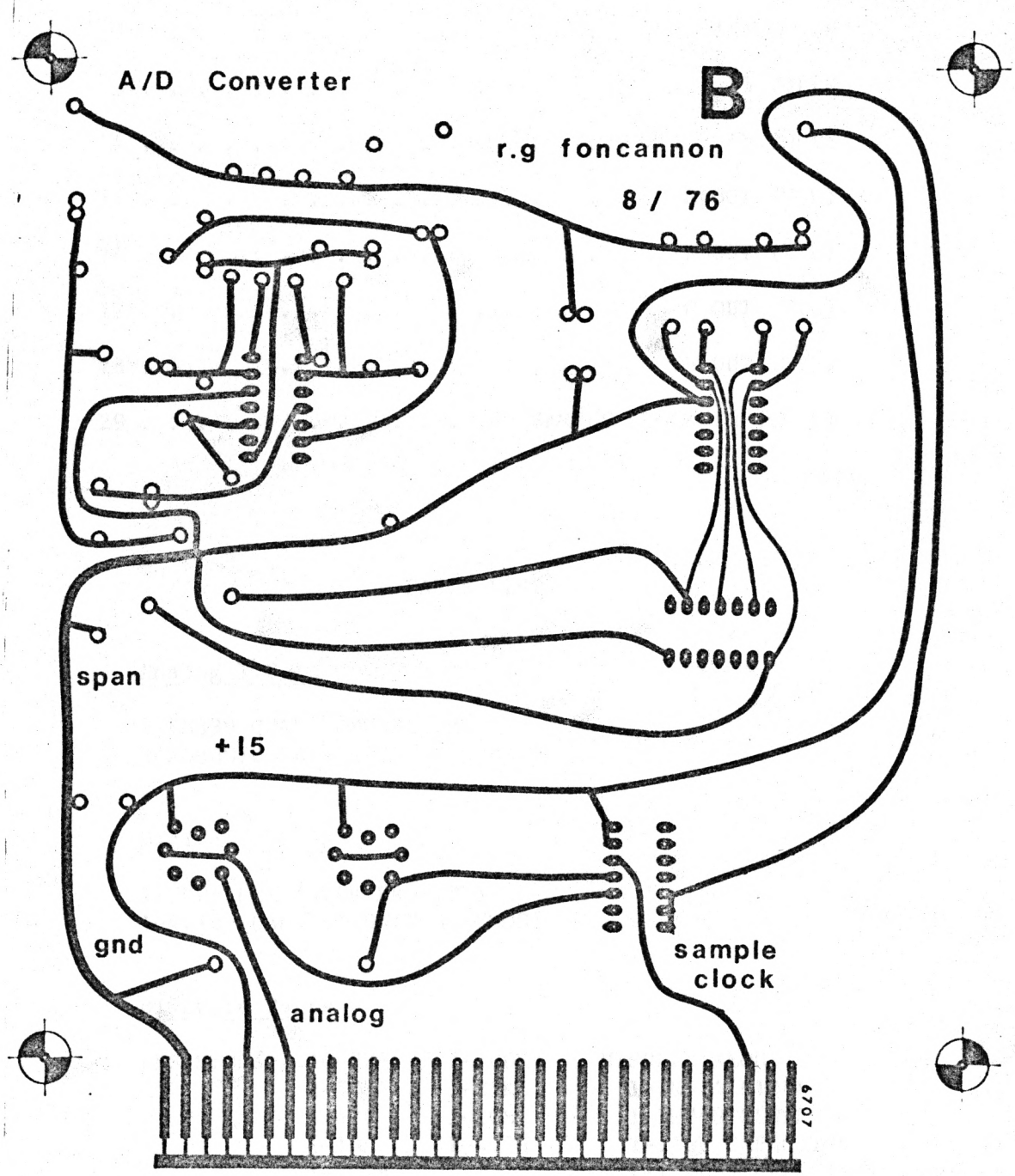
ANALOG/DIGITAL CONVERTER

TOP FOIL



ANALOG/DIGITAL CONVERTER

BOTTOM FOIL



ANALOG/DIGITAL CONVERTER

Pinout

2	GROUND
5	+15 VOLTS
7	ANALOG IN
9	15 VOLTS
14	+5 VOLTS
15	A OUT (TTL)
16	D OUT (TTL)
17	C OUT (TTL)
18	B OUT (TTL)
29	SAMPLE CLOCK IN (CMOS)

PARTS LIST

Analog I.C.'s

2-LM339 QUAD COMPARATORS
2-AD8007C FET-INPUT OP-AMPS

Digital I.C.'s

1-7404 HEX INVERTER (TTL)
1-4016 QUAD FET SWITCH (CMOS)

Discrete Parts

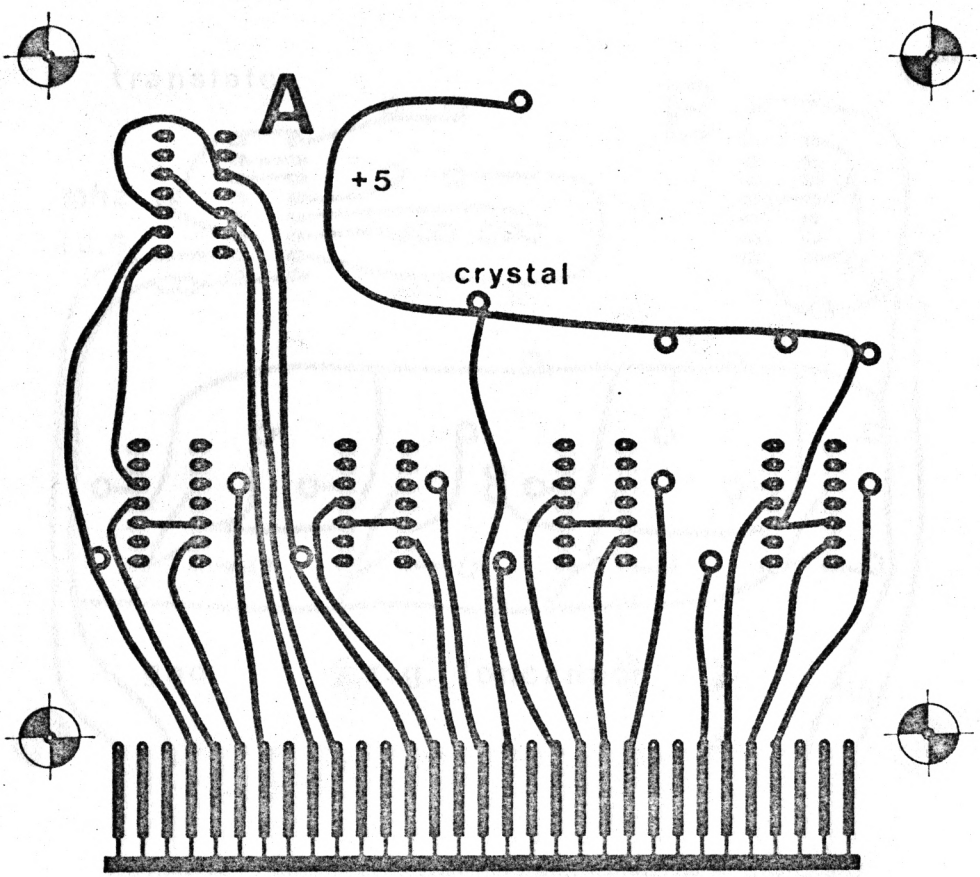
RESISTORS:
10-2K*
2-50K*
1-470
1-10M
1-2.2M
7-100K*
1-25K*
1-20M
1-4.7M

MISCELLANEOUS:
1-1N914 DIODE
1-1N748 ZENER
1-.1µF CAPACITOR
1-1000pF CAPACITOR
1-50K TEN TURN POT

* 1% precision resistors

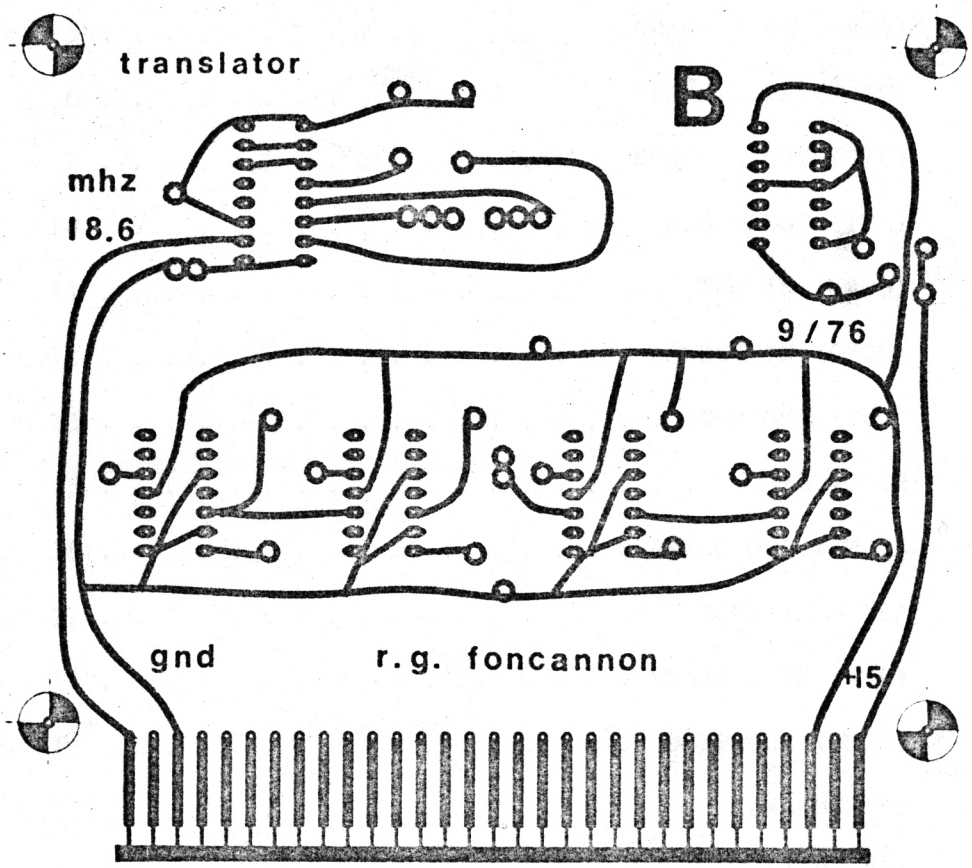
TRANSLATOR

TOP FOIL



TRANSLATOR

BOTTOM FOIL



TRANSLATOR

Pinout

1	18.6 MHZ CLOCK OUT (TTL)
3	GROUND
4	SPARE A OUT (TTL)
5	SPARE B IN (CMOS)
6	SPARE A IN (CMOS)
7	SPARE B OUT (TTL)
10	RESET OUT (TTL)
11	TWO IN (CMOS)
12	RESET IN (CMOS)
13	TWO OUT (TTL)
15	+5 VOLTS
16	SPARE C OUT (CMOS)
17	DUMP IN (TTL)
18	SPARE C IN (TTL)
19	DUMP OUT (CMOS)
22	ANALOG OUT
23	ANALOG OUT
25	SAMPLE CLOCK OUT (CMOS)
26	CONVERT IN (TTL)
27	SAMPLE CLOCK IN (TTL)
28	CONVERT OUT (CMOS)
29	+15 VOLTS
31	RADAR VIDEO IN

PARTS LIST

Linear I.C.'s

1-MC12061 CLOCK CHIP
4-LM319 DUAL COMPARATOR
1-4016 QUAD FET SWITCH

Discrete Parts

1-3.5K*
8-2K
1-1.5K*
4-.1 F CAPACITORS
1-18.6 MHZ SERIES RESONANT FUNDAMENTAL CRYSTAL
1-5K TEN TURN POT

* 1% precision resistors

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THE DESIGN OF AN INTEGRATION AND QUANTIZATION UNIT FOR A RADAR PROCESSOR

by

ROBERT G. FONCANNON
B.S., Kansas State University, 1975

A MASTER'S REPORT

submitted in partial fulfillment of the

requirements for the degree

MASTER OF SCIENCE

Department of Electrical Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

1977

ABSTRACT

In attempting to use weather radar data for storm pattern recognition, precipitation monitoring, etc. it is necessary to have a convenient and accurate method of storing and manipulating the data. The digital computer is such a method. This Report explores the construction of part of the interface necessary to implement this storage process. The Integration and Quantization Circuit sums up the radar returns for incremental areas and azimuth angles and then converts them to a digital intensity word. It is hoped that the system developed here will be a valuable tool in weather analysis.