AN INVESTIGATION OF

INTEGRATED INJECTION LOGIC

by

PETER JOHN CONNOR

B.Sc., University of Auckland, New Zealand, 1966
B.E., University of Auckland, New Zealand, 1969

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Department of Electrical Engineering

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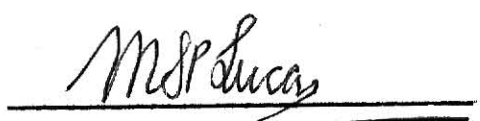
Approved by:



Major Professor

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Chapter 1

INTRODUCTION

Integrated circuit technology started with the invention of the planar process in 1960 by Hoerni, working at Fairchild (1). It was this process which enabled circuit elements - transistors, resistors and capacitors - to be built on a silicon wafer, electrically isolated from each other and with all contacts to the circuit elements made on the one surface of the wafer. Complete circuits could thus be constructed on a silicon wafer by appropriate interconnection.

The technology grew with incredible rapidity. The reasons for this are obvious when one considers the advantages integrated circuits gave over circuit design using discrete transistors. These advantages included compactness, light weight, low power consumption, improved circuit performance, design simplification, higher speed, increased reliability, stability, and many other factors.

A number of different integrated circuit fabrication and isolation processes have been developed, each having its own advantages and disadvantages. The processes can be divided into two broad categories - bipolar and MOS. Some of the more important bipolar methods are the standard buried collector, collector diffusion isolation, double diffused epitaxial, triple diffused, isoplanar and dielectric isolation processes. Principal MOS techniques include the n-channel, p-channel, complementary-MOS and silicon gate processes.

The motivations for developing new processing methods have been

to produce circuits with improved performance (higher speed, lower power consumption, more complex circuit function per package, etc) and to produce circuits at lower cost.

Bipolar processes have generally been dominant for analog circuits and for the simpler digital circuits (small and medium scale integration). Because bipolar circuits are capable of considerably higher speed operation than MOS circuits, they are used for high speed logic. On the other hand, the compactness and low power consumption of MOS structures caused them to be used almost exclusively for producing LSI (large scale integration) circuits.

In 1972 integrated injection logic (I^2L) was developed. This is a bipolar process, but significantly different in concept from other bipolar fabrication methods. It was immediately apparent that it would be a serious competitor of the MOS techniques for LSI applications. It had the basic requirements for LSI of being very compact and having very low power consumption. In addition it could be fabricated by a simple process leading potentially to low production cost. It had the added advantage of being compatible with analog fabrication techniques to the extent that combined digital and analog circuitry could be fabricated on the same chip.

In the experimental work described in this thesis, an investigation was made into the various processes involved in fabricating integrated circuits, using a variation of I^2L known as substrate fed logic.

Starting from a wafer supplied complete with deposited epitaxial layers, all processing steps were carried out in the laboratory in order that the techniques and problems associated with each could be studied in detail. Every attempt was made to keep the processing and

equipment requirements as simple as possible. It was hoped in this way to be able to make processing recommendations which could be successfully followed in laboratories having the minimum of equipment.

THIS BOOK CONTAINS NUMEROUS PAGES WITH DIAGRAMS THAT ARE CROOKED COMPARED TO THE REST OF THE INFORMATION ON THE PAGE.

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Chapter 2

A REVIEW OF I^2L TECHNOLOGY

Integrated Injection Logic (I^2L) is an integrated circuit logic fabrication technique which was developed in 1972 by Hart and Slob (2,3) of Philips in Holland and by Berger and Wiedmann (4) of I.B.M. in Germany. These latter workers called the logic structure Merged Transistor Logic (MTL), and this name is now used synonymously for I^2L.

2.1 The I^2L Structure

The configurations developed by each group were essentially the same. The basic logic unit consisted of a multiple-collector inverter, shown in Figure 2-1. This looks like a conventional n-p-n multi-emitter

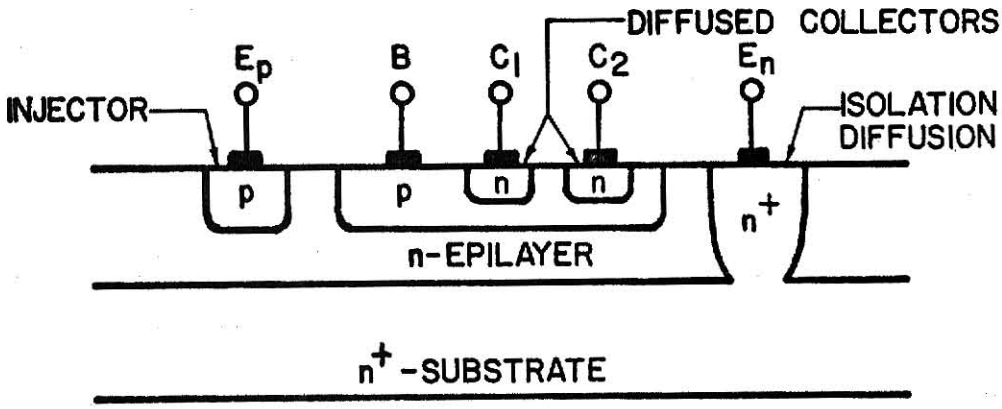


Figure 2-1. I^2L Gate Structure

transistor but is in fact operated in the inverse mode, so that what would normally be the emitters become collectors.

The other unusual features of the structure were that there are no resistors and no connection to a power supply, in the normal sense. In fact, Hart and Slob demonstrated that it was quite possible to operate the logic without a power supply at all, but to use light to provide the necessary carriers to activate the circuit. More conventionally, however, carrier injection was provided by a forward biassed p-n junction called the injector adjacent to the gates. This provided the necessary drive into the base of the switching transistor.

The injection source can effectively be represented by a current source at the base of a multi-collector inverter, as shown in Figure 2-2.

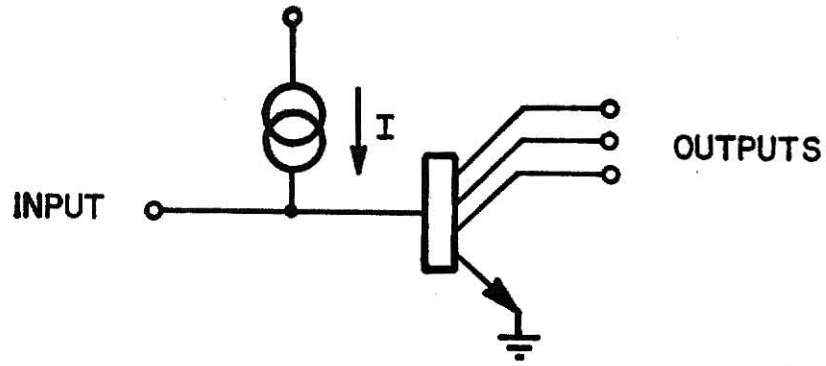


Figure 2-2. Basic I^2L Gate

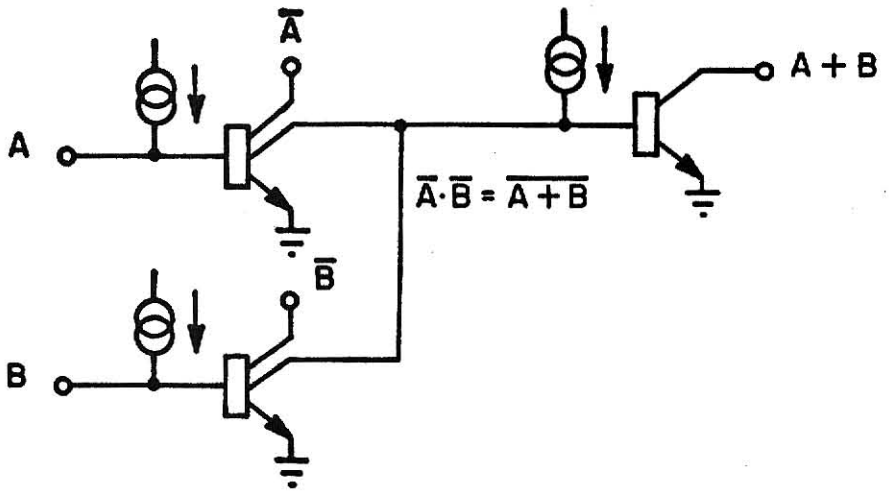


Figure 2-3. Example of I^2L Logic Interconnection

A signal applied at the base appears inverted at each of the collectors. Logic functions can be achieved as shown in Figure 2-3 by connecting the outputs from two or more such inverters.

From a circuit viewpoint, the basic I^2L element looks like the structure shown in Figure 2-4. It consists of a p-n-p transistor which

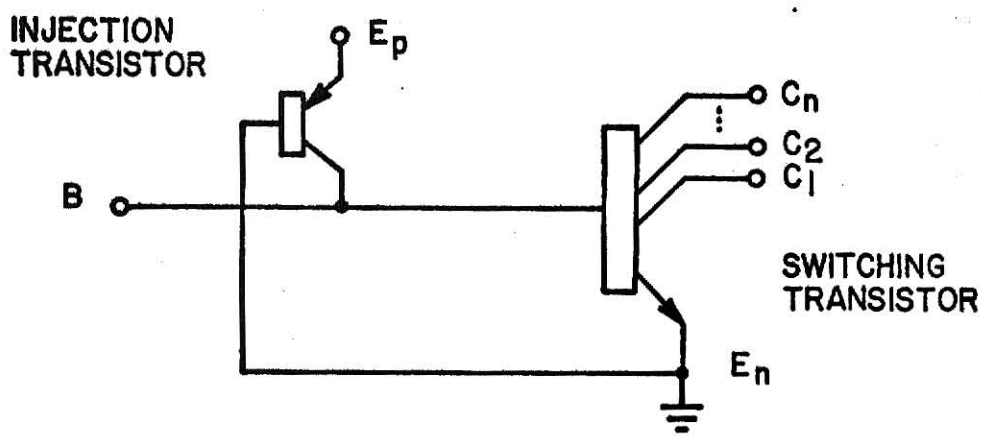


Figure 2-4. Equivalent Circuit of an I^2L Gate

acts as a source of carriers injected into the base region of the n-p-n switching transistor. Though there are no resistors, the structure looks quite complicated for a simple inverter. However a number of simplifications occur when it is implemented because of a merging of various structures (hence the name Merged Transistor Logic). For example, the same p-region acts as base of the multi-collector n-p-n transistor and collector of the p-n-p injection source transistor. An n-region common to all gates in the circuit acts as the emitter of the n-p-n transistor and base of the p-n-p transistor. The emitter of the p-n-p transistor can also be made common to a large number of gates.

The merging of various regions and lack of resistors gives a resulting gate structure which is very simple and which occupies a very small area on the silicon wafer.

A typical layout and cross-section of the I^2L structure is shown in Figure 2-5.

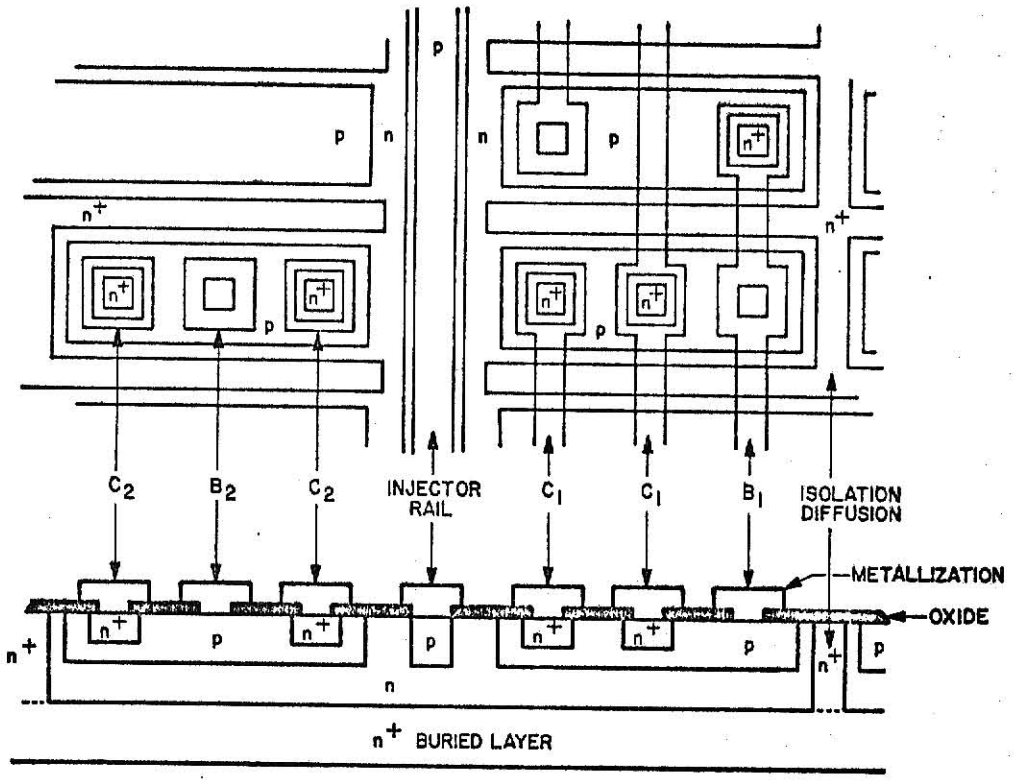


Figure 2-5. I^2L Chip Construction (after Hart et.al.(18))

2.2 Modelling of I^2L Operation

The principle of operation of I^2L can be most simply explained by using the Band Theory model (5).

Consider initially the n-p-n switching transistor in equilibrium condition without carrier injection, and with both base and collector contacts floating. Assume the emitter region to be tied to ground potential. Figure 2-6 shows the band structure for this situation.

When the nearby injection junction is forward biassed, holes are injected into the base region. This reduces the barrier height between base and emitter and between base and collector, as shown in Figure 2-7

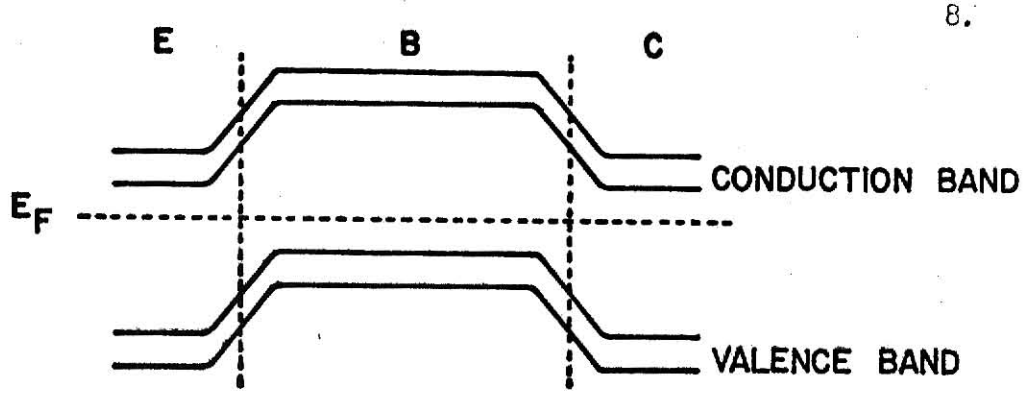


Figure 2-6. Equilibrium Band Structure of n-p-n Transistor Without Injection

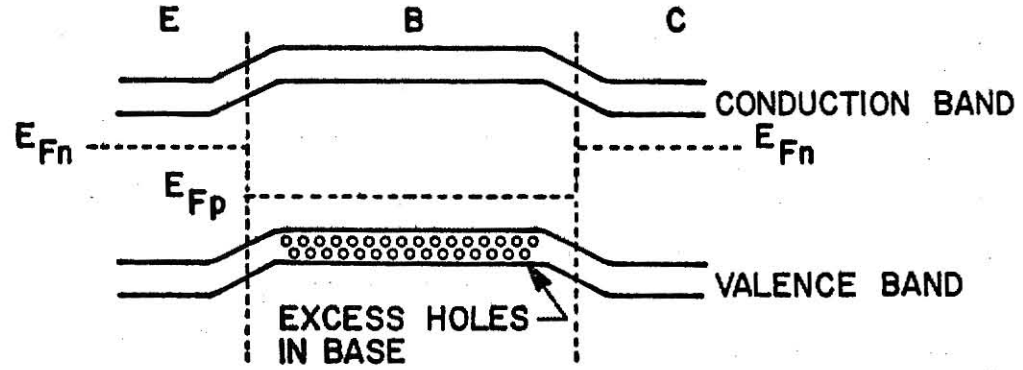


Figure 2-7. Equilibrium Band Structure of n-p-n Transistor With Injection

i.e: the base-emitter and base-collector junctions become forward biassed, and the collector is held at a low potential, close to ground.

Now considering the case when a collector in the 'low' state is connected to the base of a second transistor. This draws off the carriers being injected into the base region, and the band state of the second transistor becomes essentially the same as that shown in Figure 2-6, which is the equilibrium state without injection.

Figure 2-8 shows how this switching action works in a circuit configuration. If the base of transistor T_1 is connected to a 'high' level, then the base-emitter junction of this transistor will be

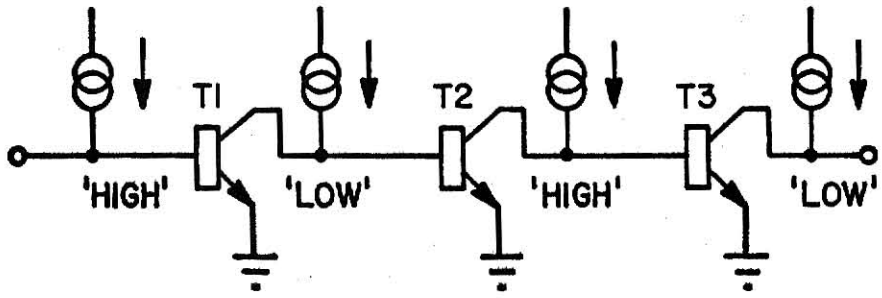


Figure 2-8. Switching Action of I^2L Circuit

forward biassed, and its collector will be held to a low potential (0v) and will drain off the injection current from the base of T_2. Transistor T_2 will thus not be turned on, since it does not receive the injected carriers, and the collector of T_2 will be in a high impedance state. Carrier injection at the base of T_3 will forward bias the base-emitter junction of this transistor, and the base of T_3 will rise to approximately 0.7v above ground. The collector of T_2, being tied to the base, will follow this potential. Transistor T_3 being turned on will drain the injection current from the base of the next transistor, and so on. The logic swing is thus between approximately +0.7v and ground.

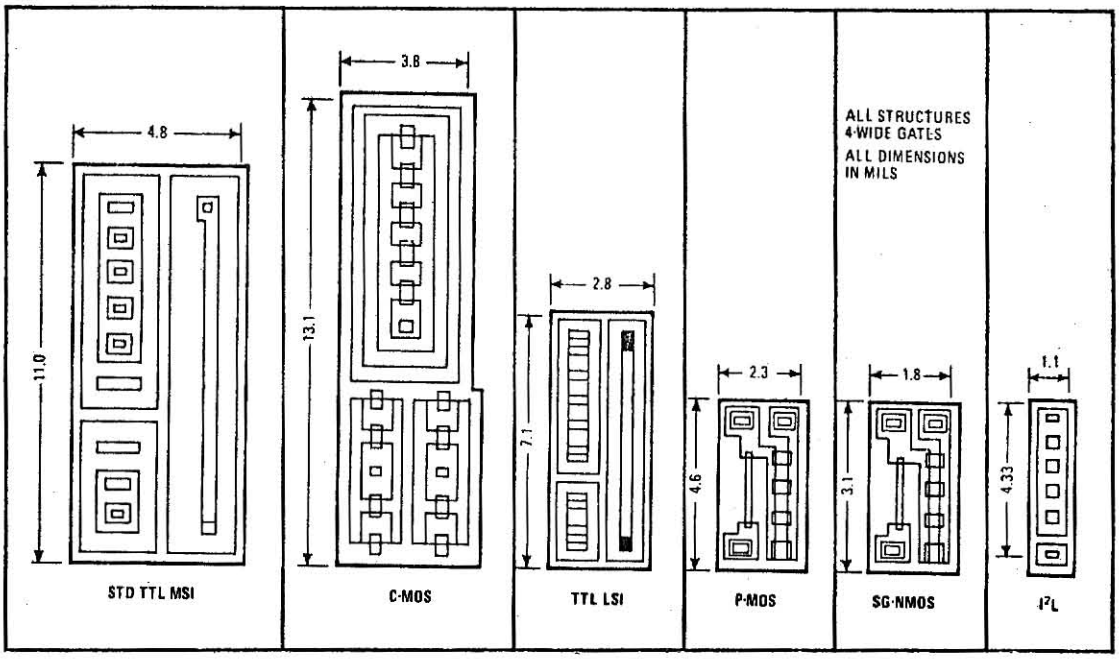
A great deal of other work has been carried out on I^2L modelling (6-16) in an attempt to obtain a better understanding of the physics of the structure, and to predict its behavior under certain conditions.

2.3 Manufacturing Considerations

In addition to its design simplicity and compactness, I^2L is attractive because of its manufacturing simplicity. For the structure shown in Figure 2-5, five masking steps and three diffusions are required. Though it does give some speed advantage, the deep n^+ isolation diffusion is not strictly necessary and is often not used for dense LSI circuits. This simplifies the process to just four masking

steps and two diffusions. Non-isolated I^2L is thus the simplest of the current processing technologies except for p-MOS, but the latters circuit performance is considerably inferior to that of I^2L (17).

Figure 2-9 demonstrates the simplicity and compactness of non-



	TTL/MSI	C-MOS	TTL/LSI	P-MOS	SG-NMOS	I^2L
Area (mil^2)	52.8	49.8	19.9	10.6	5.6	4.8
Components	3	3	3	2	2	1
Masks	7	6	7	4	7	4
Diffusions	4	3	4	1	3	2

Figure 2-9. Comparison of 4-wide Gates Fabricated in Various Technologies (after Horton et.al. (17))

isolated I^2L compared with other current fabrication technologies.

Another major advantage of the technology is that all processing steps are compatible with the Standard Buried Collector (SBC) process used for analog circuit fabrication (18). It is thus possible to fabricate a combined analog and digital circuit on the one chip without increasing manufacturing complexity over the normal seven-mask analog fabrication sequence (2, 3, 18, 19). Several such designs are already in commercial production for applications such as digital panel meter circuitry (20).

2.4 I^2L Performance

Despite its simplicity and compactness the performance of I^2L compares extremely favorably with that of competitive technologies. I^2L is fast and has very low power consumption. These two factors are interdependent, being related through the delay-power product. For I^2L this parameter is constant over a wide range, as shown in Figure 2-10. This graph also indicates the advantages given by I^2L in terms

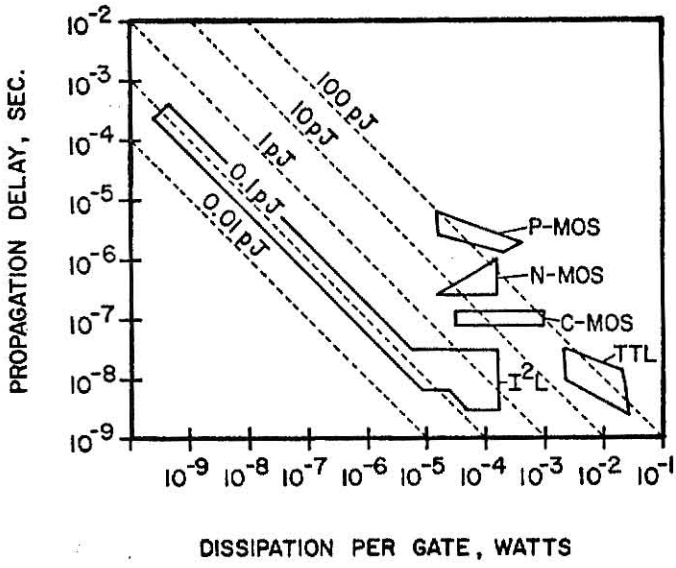


Figure 2-10. Delay-Power Product Comparison of Several Logic Families

of speed and dissipation compared with other logic families.

Production I^2L has not yet achieved the speed of Schottky TTL but comparable speeds have been achieved in laboratory circuits, and with much lower power dissipation than is possible with Schottky TTL (2, 21, 22).

One of the interesting features of I^2L is that the same circuit can be made to operate over a very wide range of speeds, simply by varying the injector supply current. For high speed operation a relatively high injection current is required, but for applications such as digital watch circuitry where speed is unimportant the circuit can operate at extremely low power levels. It is not necessary to have all regions on the same I^2L chip operating at the same speed. By controlling the injector current supplied to various regions of the chip, only those parts of the circuit which need to operate at a very high speed do so. The rest of the circuit can operate at lower speed with consequent saving in the total power consumption of the chip, and giving greater layout flexibility (23).

While the factors which enable control of switching speed by controlling injection current are useful in some situations, they are undesirable in others. Gates at some distance from the injector rail will operate more slowly than gates close to the rail. In addition there is the problem of voltage drops and current drain along the injector rail, so that a lower injection current and hence lower circuit speed is obtained from gates near the end of the injection rail remote from the power supply input.

This problem is usually minimized by placing a metallization track along the injector. However, this solution leads to further problems

since this additional metallization places constraints on the interconnect metallization layout, and may require the increased complexity of two-layer metallization.

2.5 Advanced I^2L Fabrication Techniques

Since I^2L was first introduced considerable effort has been put into attempts to devise improved forms of the logic structure, having higher packing densities and shorter gate delays without degrading the very low delay-power product and other desirable characteristics possessed by I^2L logic. In addition to forming complex logic functions, I^2L has also been successfully used for building large memories (24, 25).

Currently, experimental I^2L structures can give gate propogation delays as low as 2.5ns and delay-power products below 0.05pJ (21, 22, 26-30). Production I^2L, based on simpler manufacturing processes, is achieving delays of about 20ns at 0.3pJ delay-power product. Packing density is also greatly increased by the use of some of the advanced techniques, and densities of nearly 800 gates/mm^2 have been achieved with standard layout dimensions and tolerances (22).

Approaches at improving I^2L performance have fallen into two main categories:

i) improved, or more complex, processing techniques, while still retaining the basic I^2L structure

ii) modifications to the structure, with or without more elaborate processing techniques.

Work in the first category has generally involved applying advanced processing techniques such as the Isoplanar and similar processes to forming I^2L structures (26, 28, 31). Ion implantation

has also been used extensively. The manufacturing simplicity has completely gone, but improvements in circuit performance as a consequence of the improved device isolation and smaller structure justify the change for many applications.

2.6 Schottky I^2L

A structural modification which shows a number of advantages is the use of Schottky diodes in series with each collector (19, 22, 30, 32-35) as shown in Figure 2-11. These diodes reduce the signal swing,

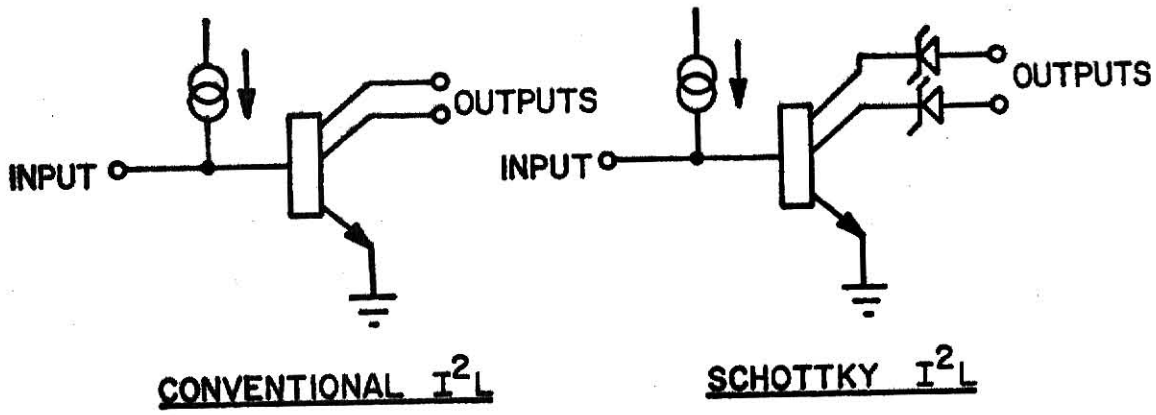


Figure 2-11. Schottky I^2L

thus improving the delay-power product and also improving the maximum switching speed.

Use of Schottky diodes on the outputs does not in itself improve the packing density which can be achieved, though the process is often used in conjunction with advanced fabrication techniques which may enable a more compact structure to be realized. In any case, Schottky I^2L requires greater processing complexity than is required for conventional I^2L, and very tight control over process variables is needed if good Schottky contacts are to be formed.

A logical extension of the use of Schottky contacts is to form Schottky diodes at the gate inputs (22, 25, 30, 35) as shown in Figure 2-12. This enables the basic inverter to be transformed from a single-

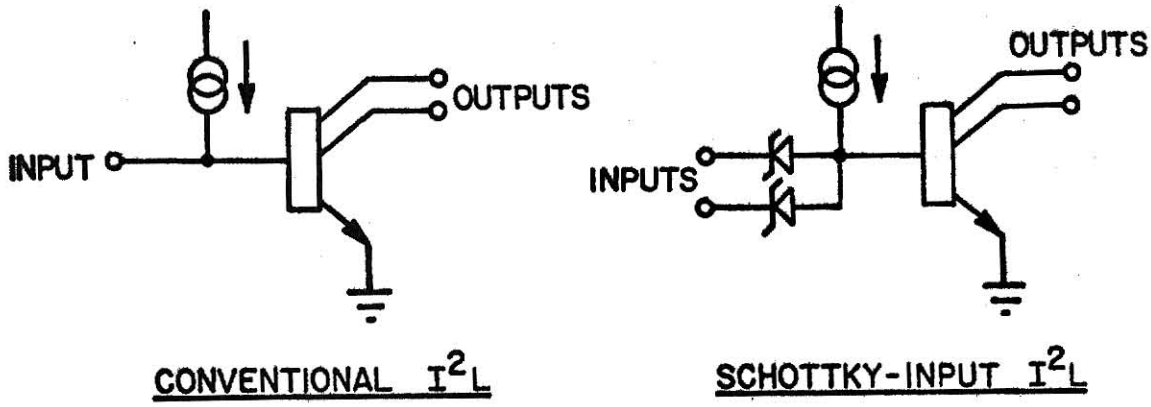


Figure 2-12. Schottky-Input I^2L

input, multiple-output structure into a multiple-input, multiple-output structure. In effect this is achieved by forming a Schottky diode AND-gate at the inverter input.

This modification gives the circuit designer considerably greater layout flexibility. It has been found that typically 20% to 50% fewer gates, and also fewer interconnection tracks, are required when a layout is designed using Schottky-input I^2L, rather than conventional I^2L (30).

2.7 Other Modified Structures

A few of the structural modifications to I^2L give improved performance while still maintaining a simple structure. An example is the 'folded collector' structure (26, 36). In this arrangement, a simple feedback connection between a collector and the base of the switching transistor, as shown in Figure 2-13, controls the saturation of this transistor, significantly reducing the gate delay.

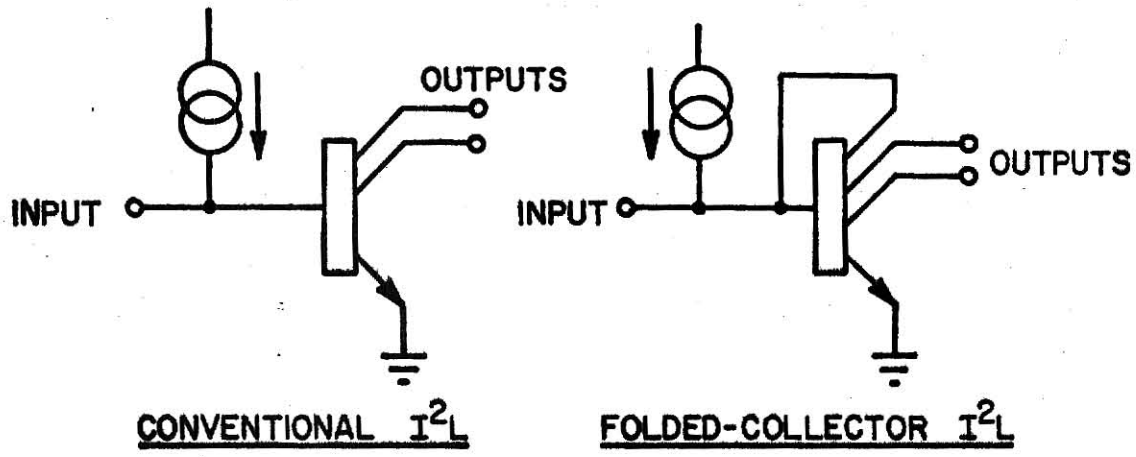


Figure 2-13. Folded-Collector Structure For Saturation Control

Another approach to modifying the structure to give improved performance has been to use buried-layer diffusions or deep implanted layers, particularly to help improve injection efficiency and give a vertical, rather than lateral, injector (29). Others have extended this approach and formed a buried layer which is later upward-diffused into the overlying epilayer (21). This approach gives impurity profiles which correspond better to those needed for speed and high gain in the switching transistor.

The buried layer process helps overcome the problem of switching speed being dependent on layout, and on the distance of a gate from the injector. However, another approach which appears quite successful at overcoming this problem is to form the injector junction within the n^+ isolation diffusion surrounding each gate (27).

2.8 Substrate Fed Logic (SFL)

SFL is a very elegant approach combining the benefits of several of the above techniques (22, 30, 35). This form of I^2L was developed by Blatt and others working at Plessey in England. They argued that

while I^2L could be fabricated using essentially a conventional bipolar process, better results would be obtained using a process specifically designed for I^2L.

Their solution was to start with a p-type wafer, which acts as the emitter of the p-n-p device. N-type and then p-type epitaxial layers are deposited on the substrate and act as base and collector of the p-n-p transistor. These same layers form the emitter and base of the n-p-n transistor, while the collectors are diffused n-type regions as shown in Figure 2-14.

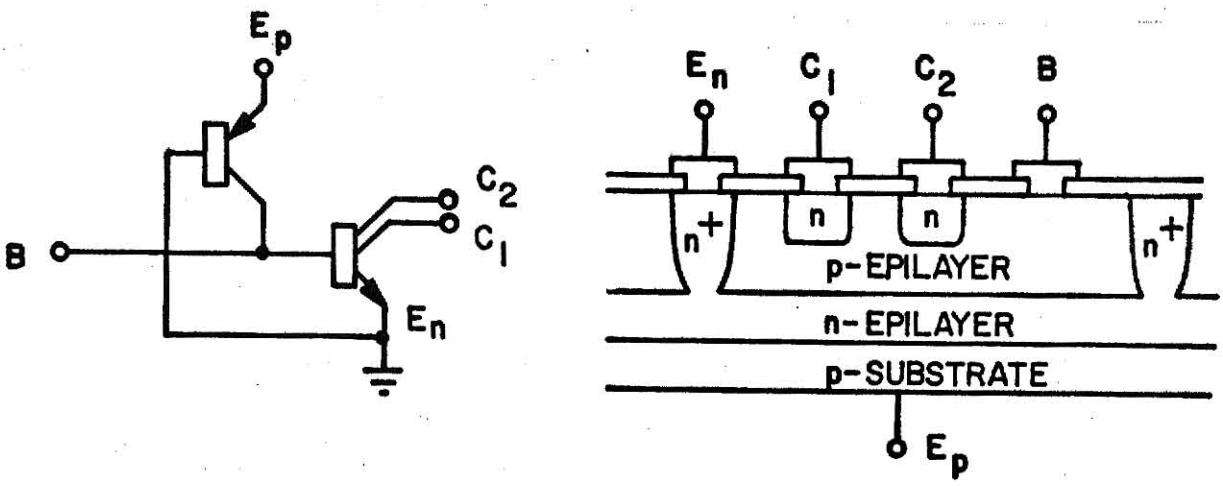


Figure 2-14. Substrate Fed Logic Structure

Blatt and his co-workers took the process further and formed multiple-input gates by using Schottky diode base contacts.

The resulting structure, even if the Schottky inputs are not implemented, is very compact yet still simple. The principal advantages of this technique can be summarized as follows:

i) Since the positive supply is applied to the substrate, and the negative supply to the low resistance isolation diffusion contacting the n-epilayer, there is no need for

metal power supply rails. This greatly simplifies the metallization layout.

ii) Transistors are well isolated from each other by the deep n-diffusion which defines them.

iii) The injecting p-n junction occupies no surface area, since it is beneath the switching transistor.

iv) All transistors are automatically equidistant from the injector, so can be placed in whatever orientation gives the most compact structure.

v) Since separate p-regions are used for the p-n-p transistor emitter and for the p-n-p collector/n-p-n base regions, rather than regions formed during the same p-diffusion as in conventional I^2L, more optimum doping levels can be used, helping to improve the transistor gain.

vi) Because the structure gives uniform injection across the base it is insensitive to base resistance. Higher fan-outs can thus be achieved than with conventional I^2L.

vii) When the Schottky diode multiple-input structure is implemented there is a large reduction in the number of gates required to perform a given logic function.

Disadvantages of SFL include somewhat increased processing complexity. The Schottky diode input structure is a six-mask process, though two of these maskings are for ion implantation and require photoresist definition only without subsequent etching. The process complexity is also increased somewhat by the need to form a double epilayer.

Another disadvantage of SFL is that it is not possible to form

analog circuitry on the same chip, but this is probably not a restriction for most applications of I^2L.

Chapter 3

OXIDATION

The formation of an amorphous layer of silicon dioxide on the wafer surface is an important processing step in integrated circuit fabrication. The oxide layer has the property of being able to mask against doping impurities and permits these impurities to enter the wafer only at the desired locations, where windows have been etched in the oxide.

This same property of the oxide layer is important for helping protect the finished circuit from contamination, as it helps prevent impurities from reaching the silicon surface and degrading the characteristics of the circuit.

Because silicon dioxide is a good dielectric, it permits evaporated metal interconnection patterns to be formed over the wafer surface, making contact with the silicon only where windows have been etched in the oxide layer for this purpose.

3.1 Oxidation Techniques

There are a number of different methods for producing an oxide layer on silicon. These have been described in considerable detail elsewhere (37, 38). The methods in common use are:

i) thermal oxidation (37)

The silicon wafer is heated to a high temperature (typically around 1000°C) in an atmosphere of water vapor or oxygen. The silicon is oxidized according to the reactions

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

$$Si + O_2 \rightarrow SiO_2$$

ii) chemical vapor deposition (37)

A layer of oxide is deposited on the silicon wafer by the pyrolytic decomposition of a silicon compound.

A typical process involves the reaction between silane and oxygen

$$SiH_4 + 2O_2 \longrightarrow SiO_2 + 2H_2O$$

Though heat is not required for the reaction to occur, it is usual to heat the wafer to above 300°C to give a more uniform oxide layer which adheres well to the silicon.

3.2 Open Tube Steam Oxidation

The formation of an oxide layer on silicon by heating the wafer in water vapor at atmospheric pressure is the most important method of oxide growth, and was the only oxidation technique investigated in the laboratory (37, 39).

The process was carried out in a diffusion furnace, as shown in Figure 3-1. Ultra-pure water was heated in a quartz flask, and the

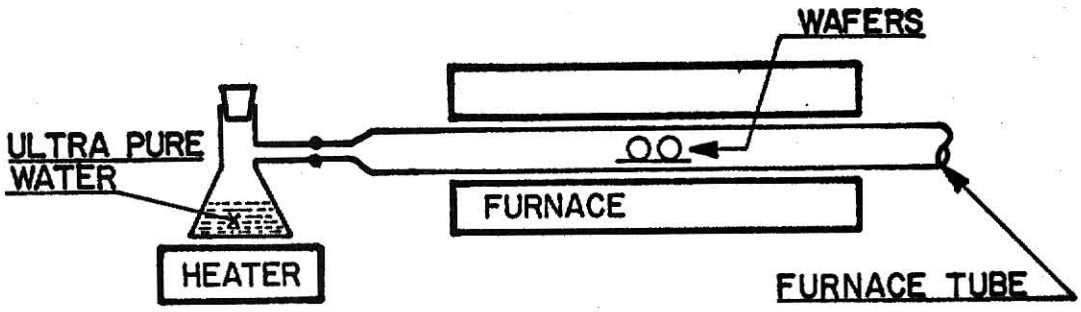


Figure 3-1. Open Tube Steam Oxidation of Silicon

vapor introduced into the furnace containing the heated silicon wafers. The exact temperature of the water was not critical, provided it was high enough to give a water vapor partial pressure of about 1 atmosphere

at the silicon. Power supplied to the water heater was kept at a level to barely maintain boiling. This helped minimise water depletion, and also resulted in a better oxide film than one grown in the presence of excess steam (40).

High purity water does not readily form bubbles when boiling, so the water flask contained several teflon beads to provide boiling nuclei. These prevented the occasional explosive release of vapor observed if the beads were not used.

Precautions were taken to avoid all sources of contamination which could cause impurities to become trapped in the oxide layer, degrading its characteristics.

A large number of oxidations were carried out at 1000°C. The thickness of the resulting oxide layer was measured optically, as discussed below in Section 3.6.

The results of the oxidation tests are shown in Figure 3-2, along with theoretical oxide growth curves for a range of temperatures (37,39).

It can be seen that the experimentally derived values for oxide thickness agree well with the theoretical predictions.

The rate of oxide growth is somewhat dependent on crystal orientation and doping level of the silicon (37). These factors were not taken into account when obtaining the experimental results shown in Figure 3-2, and the wafers used for the tests represented a mixture of conductivity types, doping levels and crystal orientation.

At high temperatures and for long oxidation times the rate of oxide growth is determined by the rate at which water molecules can diffuse through the existing oxide to reach the silicon surface, where the

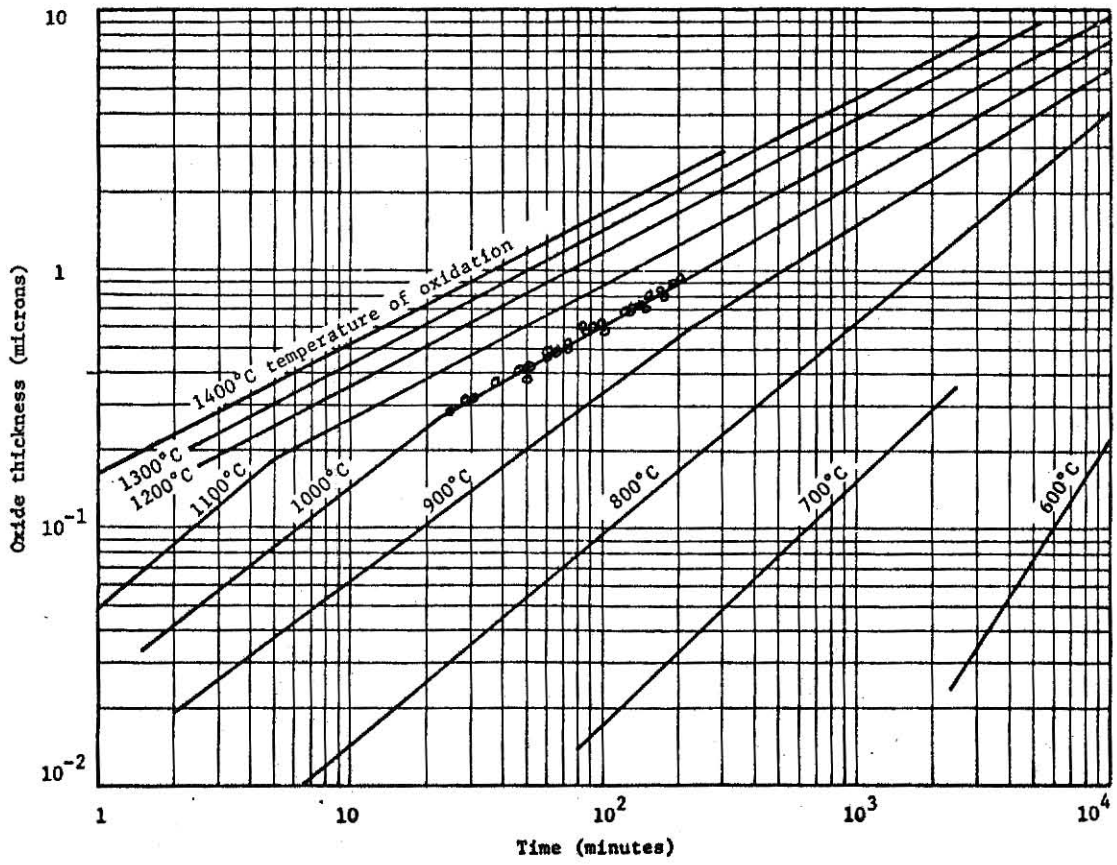


Figure 3-2. Oxide Growth in Atmospheric Steam (after Burger & Donovan (37))

reaction occurs (37, 40, 41). This leads to a parabolic growth characteristic

$$x^2 = ct$$

x = oxide thickness

t = time

c = constant

At lower temperatures, and for short oxidation times (i.e.: when the oxide film is thin) the oxide growth rate is limited by the chemical reaction rate, and the growth characteristic is better described by a linear relationship

$$x = ct$$

The thickness of the silicon wafer is reduced by thermal oxidation, since the surface layers of silicon go to form the oxide. The depth of silicon consumed in growing an oxide layer of thickness x is 0.46x.

3.3 Required Thickness of Oxide Film

When the oxide film is to be used for masking during a diffusion process, the thickness of oxide required will obviously depend on the impurity being diffused into the wafer, and on the duration and temperature of the diffusion cycle (37, 40).

Unlike the impurity diffusion boundary in silicon, the diffusion boundary in the oxide is very sharp, and the masking properties of the oxide layer are excellent until the boundary extends down to the oxide-silicon interface.

The oxide thickness required for effective masking against boron and phosphorus at various temperatures is shown in Figure 3.3.

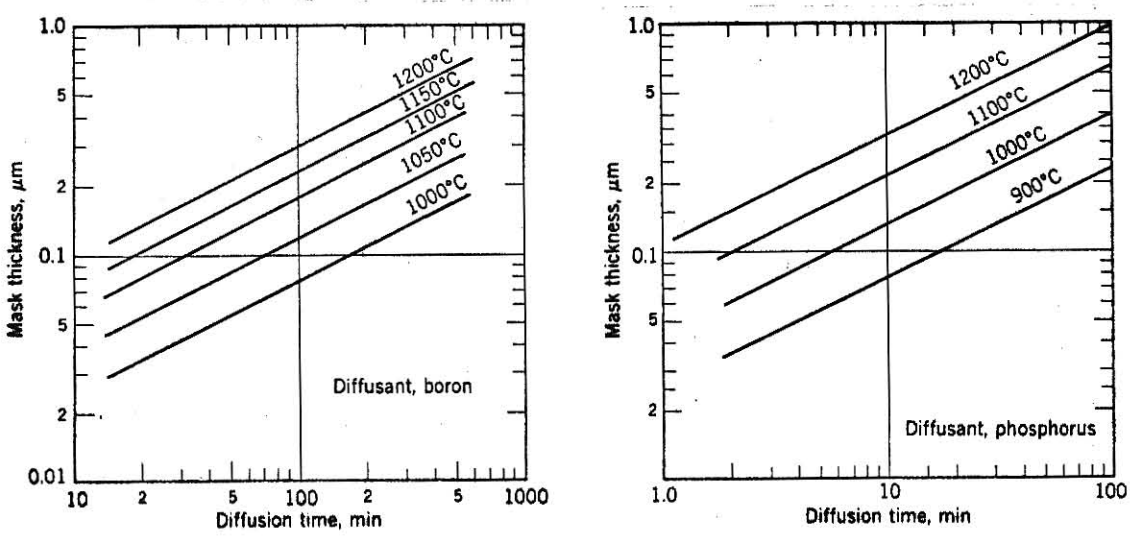


Figure 3-3. Oxide Thickness for Masking Against Boron and Phosphorus (after Ghandi (40))

3.4 Wafer Cleaning

Before growing an oxide layer on the silicon, it is essential that the wafer surface is highly polished and extremely clean if an oxide layer of the necessary high quality is to be obtained. Without a smooth, clean surface there is a liklihood that the oxide grown or deposited on the wafer will not be amorphous but will be of a crystalline form which does not act as an effective mask for diffusion operations.

Any contamination present will degrade the properties of the oxide layer. It is also possible for impurity ions to become trapped in the oxide, giving rise to effects which can very seriously alter the electrical properties of the surface layers of silicon.

To obtain adequate cleanliness, the wafer must be subjected to an elaborate cleaning procedure prior to oxidation. The cleaning process below is typical of cleaning processes used in industry (42). This procedure was followed in the laboratory, and seemed to give very satisfactory results.

i) degreasing step - the wafer is ultrasonically agitated for 5 minutes in hot trichloroethylene followed by rinsing in methanol, and then in deionized water.

ii) sulfuric acid step, the wafers are placed in hot ($85^{\circ}C$) sulfuric acid for 15 minutes. Still in the acid, they are then transferred to the ultrasonic cleaner for a further 10 minutes. This is followed by a thorough rinsing in deionized water.

iii) first mixed acid step - the wafers are placed in a mixture of equal proportions of nitric and sulfuric acids at $85^{\circ}C$ for 15 minutes, then transferred to the ultrasonic cleaner

for 10 minutes, still in the acid. They are then rinsed very thoroughly in deionized water.

iv) hydrofluoric acid step - the wafers are immersed in strong (48%) hydrofluoric acid at room temperature for 1 minute, followed by a thorough deionized water rinse.

v) Second mixed acid step - the mixed acid step (iii above) is repeated, using fresh acid.

vi) drying - this should be done in a very clean environment, preferably using hot nitrogen in a drying tunnel. Since drying equipment was not available in the K.S.U. laboratory, wafers were dried using a heat-lamp in a laminar flow hood.

vii) visual inspection - the wafers are carefully inspected for stains, streaks, films, etc. If any defects are observed, the entire cleaning cycle is repeated.

Extreme precautions should be taken when handling the chemicals used for the cleaning process. All operations should be carried out under a vented hood. In particular

i) hydrofluoric acid is extremely dangerous, especially as its effects on the skin do not become evident until considerable damage has occurred.

ii) mixed acid (nitric and sulfuric) must not come in contact with methanol, or any other alcohol.

During cleaning the wafers should be preferably held in quartz containers. Plastic handling equipment is also satisfactory, in general. Glass containers and handling equipment should be avoided because of sodium contamination.

The equipment used for growing the oxide layer - the boiling flask

and furnace tube - should also be made of quartz to avoid contamination, and the water used for steam generation should be ultra-pure.

The wafers should be oxidized as soon as possible after cleaning to avoid the liklihood of recontamination.

When any defects were observed in wafer cleanliness, they could generally be traced to inadequate rinsing. A good supply of ultra-pure water (resistivity of 18 megohms-cm) and a cascade rinse tank were available. This equipment certainly helped minimize contamination problems, but it was still found desirable to leave wafers to rinse for at least 10 minutes after each cleaning step to ensure thorough rinsing had occurred.

3.5 Detection of Pinholes in Oxide Film

Poor cleaning and oxidation processing can lead to the presence of minute pinholes and cracks in the oxide film. These defects are too small to be seen under an optical microscope. but they can be revealed by various decorating methods (43, 44).

To investigate this technique, an electrolytic cell was set up, using methanol as the electrolyte, as shown in Figure 3-4.

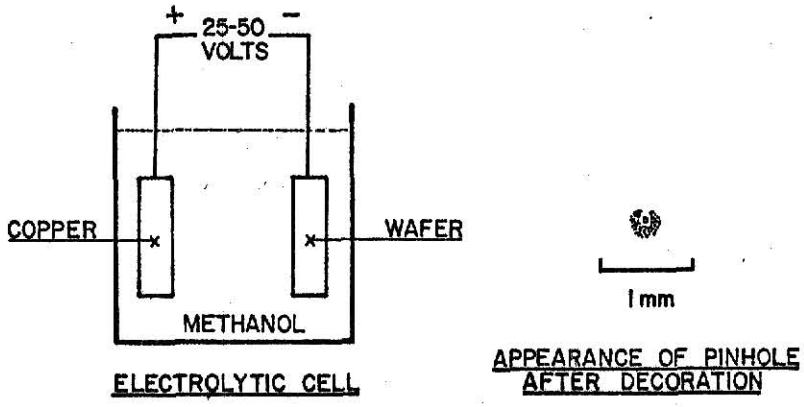


Figure 3-4. Copper Decoration For Oxide Pinhole Detection

The wafer being tested formed the cathode, while the anode was a strip of copper. Applying 40 volts across the cell, the pinhole locations became obvious as a stream of small bubbles arose from each. After about 30 minutes, examination of the wafer showed the pinholes to be very easy to observe due to the presence of the copper halo, which appeared around each defect as shown in Figure 3-4.

3.6 Measurement of Oxide Thickness (37, 43)

Several methods of measuring the thickness of the oxide layer were investigated. These were all optical methods which, because of the small dimensions involved, offer the simplest and most accurate measurements.

3.6.1 Color Method (43, 45)

When an oxidized wafer is viewed in white light, destructive interference between light reflected from the oxide surface and light transmitted through the oxide and reflected from the silicon surface causes the oxide film to appear colored. The color observed is that produced by uniform white light minus the color corresponding to the wavelength(s) removed by destructive interference.

Destructive interference occurs whenever the difference in optical pathlength between light reflected from the oxide and the silicon surfaces equals an odd number of half wavelengths. For normal incidence

$$d = \frac{(2m - 1)\lambda}{4n}$$

d = thickness of oxide film

n = refractive index of oxide = 1.45

m = 1, 2, 3, ...

λ = wavelength of light

The oxide colors are not unique, but can occur repeatedly for different oxide thicknesses, corresponding to different values of the integer m. It is thus necessary to have an approximate idea of the oxide thickness. An accurate measurement can then be made from its color, by using one of the several available charts of color sequence for increasing oxide thickness (37, 43). This procedure demands some care and experience, as many of the color changes are very subtle, particularly for thick oxide films.

This measurement procedure was investigated more fully. The oxide was removed from one half of several wafers by mounting the wafers vertically in a beaker of buffered hydroflouric acid, so that the etch same only part-way up the wafers. This resulted in the formation of a very shallow wedge of oxide increasing from nothing to full oxide thickness over about 2mm. By illuminating the wafer with white light and observing the wedge through a microscope the full color sequence with increasing oxide thickness could be observed.

After some experience, it was found possible to confidently estimate the oxide thickness on an unetched wafer to within a few percent using the color technique provided the approximate thickness was known. This was quite accurate enough for our applications.

3.6.2 Monochromatic-light Fringes This method is similar in principle to the color method. A wedge is etched in the oxide film, and the wafer is now illuminated with monochromatic light rather than white light. A series of light and dark fringes is seen, parallel to the wedge-front. The spacing between fringes (light-light or dark-dark) corresponds to a change in optical path length of one wavelength. A

wedge showing 'm' fringes thus corresponds to an oxide thickness 'd' of

$$d = \frac{m\lambda}{2n}$$

This method was investigated using sodium illumination of wavelength of 589.2nm. It was found possible in practice to estimate the value of m to about $\frac{1}{4}$ fringe, corresponding to a resolution of about 50nm in the oxide thickness measurement. This is considerably worse than the resolution which could be obtained from the color method (typically 20nm). Also, the monochromatic fringe method could only be used where an etched oxide wedge was available, whereas the color method could be used equally well on an unetched wafer, provided the approximate oxide thickness was known.

3.6.3 Fizeau Fringe Method (37, 46) The color and the monochromatic fringe methods both require a value to be assumed for the refractive index of the oxide film. The value of this parameter can vary quite widely, (typically 1.43-1.47) depending on the method and conditions under which the oxide was formed.

The Fizeau fringe method is much superior to the color method if precise measurements are required. Investigation of this method showed it gave very good results, but that it is considerably more complicated than the color method.

i) The oxide is etched away from part of the wafer to leave a wedge-shaped step at the oxide edge.

ii) The surface of this specimen, including the etched step, is coated with aluminum by vacuum evaporation to give a totally reflecting surface.

(iii) A thin film of aluminum was evaporated onto a microscope slide to form a partially transmitting mirror. A special jig was constructed to hold this mirror over the wafer, with provision to adjust the position of the mirror to form a small wedge-shaped airspace between mirror and wafer. The assembly was then viewed through a microscope using sodium monochromatic illumination, as shown in Figure 3-5.

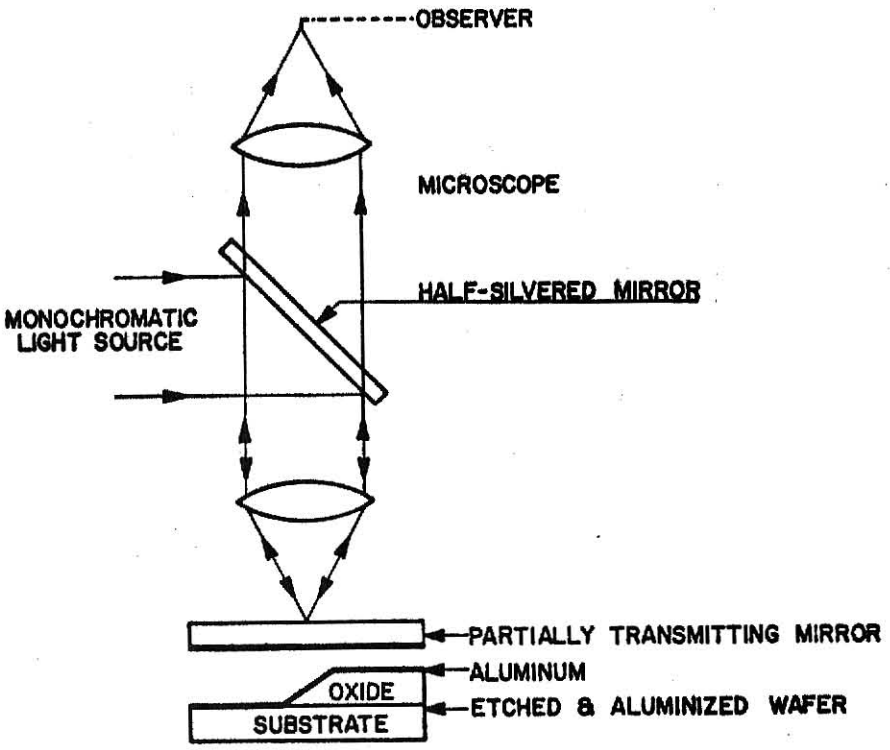


Figure 3-5. Fizeau Fringe Method For Oxide Thickness Measurement

When the mirror and wafer were correctly positioned, a set of fringes similar to those shown in Figure 3-6 could be observed. Because of the multiple reflections between the aluminized wafer and partially transmitting mirror, the dark fringes observed are very thin and

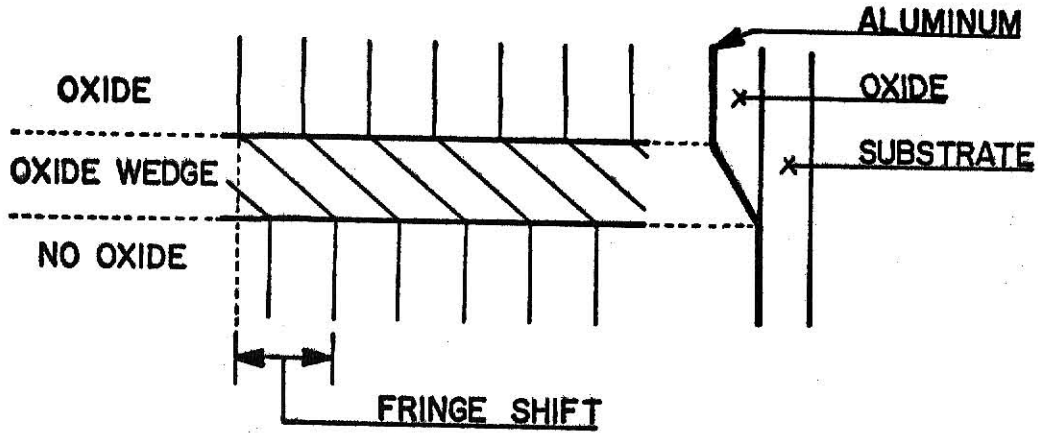


Figure 3-6. Appearance of Fringes

sharp (46). It was thus possible to use an eyepiece micrometer on the microscope and measure the fringe-shift quite precisely.

For this situation, the oxide layer thickness is

$$x = \frac{m\lambda}{2}$$

where m is the fringe-shift observed, measured in terms of fringe-spacing.

It was found that for this method to work satisfactorily, the angle of the oxide wedge step was quite critical. Too steep an angle made fringe-counting difficult, as all fringes tended to run together in the wedge. Too shallow an angle made it difficult to line up with fringes on both sides of the wedge.

The wedge forming technique described above for the color method gave much too shallow a wedge, while photoresist coating, followed by etching in buffered hydrofluoric acid gave too steep a wedge. Best results were obtained by dipping the sample part-way into melted paraffin wax, then etching with either buffered or strong hydrofluoric acid,

using the paraffin wax as resist. This resulted in an oxide wedge of about the right angle.

This method of oxide thickness determination was found to be very precise and repeatable. However, because the much simpler color method gave sufficient accuracy for our purposes the Fizeau-fringe method was not normally used.

3.7 Oxide Etching (37, 45)

For diffusion masking and other processing steps it is necessary to etch windows in the oxide, down to the silicon surface. Etching is done with buffered hydrofluoric acid, and it is important to know the etching rate in order that sufficient etching time be given to completely remove the oxide layer from the windows, without giving an excessive etch time which would result in undercutting of the photoresist.

Tests were carried out in the K.S.U. laboratory using "Transene Buffer-HF Improved" etchant at 23°C, with no agitation. A number of oxidized wafers were etched for measured times, and the thickness of the oxide layer measured by the color method before and after etching.

The etch rate was found to be very constant over a wide range of times. The mean etching rate was 107.5nm/min.

In practice, a value of 100nm/min was used for calculation of etching times. This was considered a safe figure since it gave a small tolerance to ensure complete etching had occurred, without risk of significant undercutting.

Confirmation of complete oxide removal by the etch was obtained by observation of the surface properties of the wafer. A surface with oxide remaining on it is hydrophilic, while a silicon surface which has been freshly exposed by hydrofluoric acid etching is hydrophobic.

Chapter 4

PHOTOLITHOGRAPHY

Integrated circuit photolithography is the process by which circuit features are defined on the surface of the wafer. Two major areas can be considered; preparation of the photographic masks and photoresist technology.

4.1 Preparation of Photographic Masks

The masks used for defining circuit structures in a photoresist layer, prior to etching, consist most commonly of a layer of photographic emulsion on a glass plate. An alternative form of mask, used quite often for its better abrasion resistance, has an opaque film of hard metal such as chromium in place of the emulsion.

The masks are made by photographically reducing artwork drawn several hundred times the final size of the circuit, and at the same time producing multiple images of the circuit in a large array. Normally a number of different masks are required for processing a wafer, and of course the details on each mask must align perfectly with the details defined on the wafer by the previous masks.

A detailed investigation was made to see if it would be possible to make satisfactory photographic masks in the K.S.U. laboratory, and if so to determine the minimum size of details that could be reliably transferred to the wafer.

To help in evaluating the results, the resolution test pattern shown in Figure 4-1 was designed. This consisted of an array of line groups of various widths. The original artwork was cut in Rubylith,

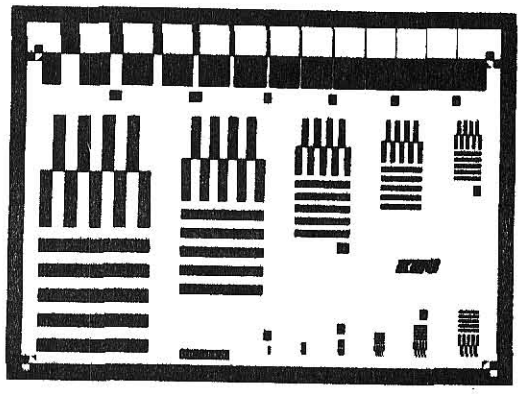


Figure 4-1. Resolution Test Pattern

and the image shown in Figure 4-1 is reduced 5X from this. It was intended that the original pattern be reduced by a total of 250X to form the test photographic mask, giving line widths and spacings on the photomask ranging from 1 micron to 32 microns.

The interlaced line pattern was chosen as it gives a very quick and simple yet accurate indication as to whether the exposure and development times were correct. Incorrect exposure is shown by corresponding broadening or narrowing of the lines as shown in Figure 4-2.

Figure 4-2. Exposure Evaluation from Test Pattern

The overall 250X reduction was made in three stages; two 5X reductions then a final 10X reduction. It is strongly recommended that before attempting any extreme photoreduction and microphotography work the relevant chapters of "Microphotography" by Stevens (47) be read. The Kodak publication number P-52 "Techniques of Microphotography" (48) is also useful.

4.1.1 Cutting Rubylith Artwork The artwork was cut on 'Rubylith' film (Ulano Company, Inc.) at 250 times the final desired image size. This enabled the layout to be produced easily to very close tolerance.

4.1.2 Initial Reduction (5X) The initial reduction of 5X was made using a Calumet 4 X 5 camera with a Schneider Repro-Claron f/9, 210 mm copy lens.

The camera was set to give approximately the desired reduction, using the formula

$$D = \frac{f(R + 1)^2}{R}$$

D = distance between artwork and film

f = focal length of lens

R = reduction factor desired.

The exact reduction factor was set by measuring the image size on the camera focussing screen.

Focussing of the camera was achieved by observing the image on the ground-glass focussing screen; using a mangifer to help locate the setting which gave the sharpest image.

The Rubylith artwork was photographed with transmitted illumination using a lightbox.

The film used was Kodak 'Kodalith' ortho film, type 3 with 0.004"

thick estar base (Kodak no.2556).

A number of exposures were made at various apertures and exposure times. Initially Kodak D-11 developer was used. This gave very high contrast, but fine lines were poorly defined. Subsequent development was carried out using the two-part Kodalith developer. This proved to give greatly superior results with much sharper line edges than were obtained using D-11 developer, though somewhat lower contrast.

The best exposure was judged by comparing details on the test pattern, looking in particular for line broadening or narrowing as shown in Figure 4-2. For the illumination source used, and other conditions applying, the best exposure was judged to be 4 sec. at f/16. When studied very critically, it was found that exposures made at the same aperture and time showed significant differences. These were traced to slight differences in the development process, such as slight change in temperature, developer exhaustion, etc.

To obtain adequately consistent results it was found necessary to standardise the development process as much as possible. The same number of sheets of film were developed in each batch, and the same quantity of fresh developer used for each. Development time and developer temperature were carefully controlled at $2\frac{3}{4}$ min. and $20^{\circ}C$ respectively (the values recommended by Kodak) and the agitation procedure standardised. Completely consistent results were obtained after this process standardisation was implemented.

Following development, the film was placed in a stop bath (Kodak Indicator Stop Bath) for 15 seconds, then fixed for 2 minutes using Kodak Fixer. Finally the film was washed in running water for about ten minutes.

This procedure gave an image on the film which reproduced fine details in the artwork very well, and was considered completely satisfactory for the application.

4.1.3 Second Reduction (5X) An array of first-reduction images was mounted on the lightbox screen and a 5X reduction made of them.

The same camera and lens used for the first reduction were used for the second reduction also. Other lenses investigated for this application were a Wollensak 8¼" f/4.5 Raptar Copy Lens and a Rank Taylor Hobson 8¼" f/4.5 Xerox Lens. Both these lenses gave inferior results to those obtained with the Schneider Lens.

Initial tests using Kodalith type 3 film showed this to have too coarse a grain to satisfactorily reproduce the fine details of the second-reduction image.

Much better results were obtained using Kodak High Resolution Film (Type SO-343). This has an extremely fine grain emulsion, and no grain structure was detectable in the images produced. It is a very slow film, requiring an exposure approximately 75 times longer than that required by Kodalith type 3.

This film was developed according to Kodak's recommendations, using Kodak D-19 developer. Development time was 5 minutes at 20°C, followed by immersion in a water stop bath for 30 seconds. The film was fixed with Kodak Fixer for 2 minutes, then washed for 10 minutes in running water. The emulsion on this film appears to be very delicate, and easily scratched, so care was taken to avoid damage to the emulsion during processing. As with the first reduction, development was standardised as much as possible to give consistent results.

A number of tests were conducted to determine the correct exposure,

and the best exposure was judged to be 105 seconds at f/11, for the light source used.

Because of the very fine details in the image, visual focussing was found to be inadequate. The best focus was determined using the procedure recommended by Stevens (47).

i) A microscope was used to examine the image formed on the camera's focussing screen. This enabled the point of 'best visual focus' to be determined quite accurately.

ii) A series of identical exposures was made with the object to lens distance changed by 2mm between each. The lens to film distance was not changed. This procedure has the effect of changing the focus (the lens-film distance) by X/R^2 mm with each step where R is the reduction factor being used (R = 5 in this case) and X is the step size (X = 2mm). The range of camera positions is chosen to straddle the point of best visual focus.

iii) The sequence of exposures is examined to see which gives the sharpest focus.

Using this procedure, the best focus (which may differ significantly from the best visual focus) can be determined very precisely.

The images produced on the film in these tests were judged to be completely satisfactory for the application. Even the finest details (10μ lines and spacings) were resolved over a reasonable area.

4.1.4 Final Reduction (10X) As expected, the final 10X reduction proved the most difficult. The finest details on the image are now only 1μ wide, which is getting very close to the limit of resolution for any lens. (The wavelength of green light is about 0.5μ.)

One of the problems was that the lens was required to form a high resolution image over the entire area of the mask (approximately 15mm diameter). The normal mask-making procedure is to use a lens to form the image of a single mask element (cell) then move the photographic plate and make a second exposure, and so on, to build up the complete mask array. This step and repeat procedure gives much superior results to forming an entire mask array in one exposure. It requires a lens which gives high resolution only over the area of one mask cell. However, it does need a high precision X-Y table and unfortunately such a table was not available.

A number of different lenses were investigated to see which would give the best results for the application. Lenses investigated were:

Wollensak	25mm	f/1.5	Cine-Raptar (16mm movie camera lens)
Schneider	210mm	f/9	Repro-Claron (copy lens)
Wollensak	209mm	f/4.5	Raptar Copy Lens
Schneider	105mm	f/5.6	Componon (Enlarger lens)
Schneider	150mm	f/5.6	Comparon (Enlarger lens)
Asahi	55mm	f/1.8	Super-Takumar (35mm camera lens)

Because of the wide range in focal length, various cameras had to be used to mount these different lenses. The Wollensak Cine-Raptar was mounted in a special camera body made for the purpose. The Schneider lenses and the Wollensak copy lens were mounted in the Calumet 4 X 5 camera body. The Asahi lens was mounted in an Asahi Pentax 35 mm camera body.

These tests were made using Kodak High Resolution Plates, since these were to be the final photographic masks for transferring the image to the wafer. Glass plates, rather than film, are necessary to give

the required dimensional stability. The emulsion on these plates is essentially identical to that on the High Resolution Film used for the second reduction.

For tests on these lenses, an array of second-reduction images was mounted on the lightbox screen. A number of exposures at 10X reduction and using a range of apertures and exposure times were made with each lens.

Development and processing of the High Resolution Plates was the same as used for the High Resolution Film in the second-reduction stage except that a final rinse in deionized water was given to avoid water marks on the emulsion.

Focussing of the camera to record the very fine details of the image posed some special problems. Ground glass focussing screens were much too coarse to give more than an approximate indication of the correct focus position. An old photographic plate which had been developed without being exposed (i.e.: has a clear emulsion surface on it) was mounted in the plate holder on the camera to act as a focussing screen. A number of very fine scratches were made in the emulsion on this plate to define the focus plane. A high-power microscope (200X) was mounted behind the camera and focussed on these scratches, then the camera was focussed until the image and emulsion surface (scratches) were simultaneously in sharp focus when viewed through the microscope. This determined the point of best visual focus. Finally, the best photographic focus was determined by taking a series of exposures while moving the position of the camera in small increments (approximately 1% of the focal length of the lens) as described for the focussing procedure used for the second reduction process.

This focussing procedure was quite involved, but essential if satisfactory results were to be obtained.

Comparing the results of the exposures made with each of the above lenses, it was found that the Wollensak Cine-Raptar gave the image with highest resolution, but only over an area about 2-3mm in diameter. At an aperture of f/2.8, this lens clearly resolved patterns with 2μ lines and spacings, and marginally resolved the 1μ patterns. However, the quality of the image deteriorated very rapidly away from the center of the field, with bad flare and distortion evident. At smaller apertures, the resolution in the center of the field deteriorated while that towards the edge of the field improved, but not sufficiently to make this lens suitable for the requirements of the final reduction. The lens would probably be suitable, however, for use in a step and repeat camera since it gave very fine resolution in the center of its field.

The other five lenses tested were all rather similar in their characteristics, and gave a much more uniform image over a wide field than was given by the Wollensak Cine-Raptar. Over the required field diameter of about 15mm the Asahi Super Takumar lens gave the best results. Used at f/5.6, this lens gave good resolution of 8μ patterns over the whole field. The three Schneider lenses gave good results which would probably be acceptable, but their resolving power was apparently limited by their smaller apertures.

4.2 Photoresist Processing

The photoresist used in the laboratory was Hunts 'Waycoat' IC Resist. This is a negative-acting photoresist i.e.: where the resist

is exposed to ultraviolet light it remains on the wafer after development.

Wafers were coated with photoresist on a spinner where rotation speed could be varied up to 10,000rpm, the wafer being held on the spinner by a vacuum-chuck.

Coated wafers were exposed using a mask aligner. This equipment had provision for translating or rotating the mask relative to the wafer while viewing them through a microscope. When the mask was correctly aligned with features already on the wafer, the mask and wafer were brought into intimate contact and exposed to a u.v. light source.

There were several main parameters in the photoresist processing sequence which could be varied:

photoresist viscosity

r.p.m. of spinner

exposure time

development time

To minimise the number of variables, it was decided to keep the development process fixed at Hunt's recommendations (see below).

After investigating a large number of combinations of resist viscosity, spin speed and exposure time, it was found that the most consistent results were obtained using a very thick photoresist coating. This was given by using the resist undiluted (viscosity 59cps) applied by spinning at 2000 r.p.m. An exposure of 4 minutes was required for best results with the u.v. source available. However, when the photoresist was applied on an aluminum metallization layer, rather than on oxide, an exposure of about 8 minutes was needed for acceptable results.

4.2.1. Photoresist Filtration To avoid particulate

contamination in the photoresist, it was found very desirable to filter the photoresist as it was applied. The photoresist was dispensed from a hypodermic syringe, and a filter element which fitted between the syringe and needle was used. The filter element used was a Millipore Type AAWP-02500, having a 0.8μ pore size, plus a Type AP25-02200 prefilter.

Some care had to be taken when filling the syringe with photoresist. It was found that if resist was drawn up into the syringe through a needle, the low pressure in the syringe could apparently cause minute bubbles to form in the resist which could later pass through the filters and cause pinholes in the resist coating on the wafer. This problem was not experienced if the syringe was filled by dipping the syringe itself into resist, and drawing resist into it without using a needle.

4.2.2 Photoresist Processing Sequence The following sequence of processing steps based on Hunt's recommendations was found to give satisfactory images in the photoresist.

i) unless it had just come from a furnace processing step (oxide growth or diffusion) the wafer was baked at 200°C for at least 30 minutes immediately prior to coating with photoresist

ii) the wafer was placed on the spinner and spun at about 5000 r.p.m. to throw off any loose contamination particles

iii) the wafer was flooded with undiluted photoresist (viscosity 59 cps) then spun at 2000 r.p.m. for 1 minute

iv) immediately before exposure the wafer was baked at 85°C for 15 minutes, in an oven. The wafer was contained in a glass Petri dish covered with aluminum foil to exclude light.

v) the wafer was aligned with the mask on the mask aligner, then exposed to u.v. light for 4 minutes (8 minutes if the wafer is coated with a metallization layer)

vi) the wafer was immersed in Waycoat I.C. Developer for 90 seconds, without agitation

vii) the wafer was transferred to Waycoat I.C. Thinner for 15 seconds with vigorous agitation.

viii) the wafer was immersed in methanol for 15 seconds with vigorous agitation

ix) the wafer was rinsed in deionized water. This step is not in Hunt's recommendations, but was found to reduce the incidence of streaking and scumming on the wafer. Additional rinses in methanol may also have worked, but were not tried.

x) the wafer was dried under a heatlamp. The wafer should now be examined with a microscope to confirm that a good image has been formed in the photoresist

xi) immediately before etching, the wafer was baked in the oven at 140°C for 25 minutes

xii) the wafer was now etched in buffered HF (or Aluminum etch) for an appropriate time

xiii) the photoresist coating was now stripped from the wafer using Hunt's Microstrip. No recommendations were available for using the Microstrip, but good results were obtained by immersing the wafer in Microstrip at 85°C for 5 minutes. The wafer was then transferred to the ultrasonic cleaner, still in the Microstrip, for a further 5 minutes, followed by a thorough rinse in water, and deionized water.

xiv) in general, it was considered desirable to give the wafer a final cleaning step in hot mixed (nitric and sulfuric) acids for 10 minutes, plus a further 5 minutes in the ultrasonic cleaner, followed by a very thorough rinse in deionized water.

The photoresist processing cycle is now complete, and the details on the photographic mask should have been faithfully transferred to the wafer surface.

Chapter 5

DIFFUSION

Diffusion is the most important method used for introducing impurity atoms into a silicon wafer to give the desired electrical characteristics.

5.1 Diffusion Techniques

The wafer is heated in a diffusion furnace to a temperature usually in the range 950°-1300°C. Atoms of the doping impurity are introduced into the vicinity of the silicon wafer, and diffuse into the wafer at locations where its surface is not protected by an oxide mask. For a particular impurity, the number of atoms that enter the wafer and the depth to which they penetrate depend on their concentration at the wafer surface and on the temperature and duration of the diffusion process.

There are a number of different methods of carrying out the diffusion and for introducing the impurity. These have been described in considerable detail elsewhere (37).

By far the most common diffusion technique is the open tube method, in which the wafers are contained in a furnace tube which is open to the atmosphere, or at atmospheric pressure inside.

The diffusion source used is generally a compound of the doping impurity, and may be a solid, liquid or gas. With gaseous sources, the impurity gas is mixed with a carrier gas in precise proportions and allowed to flow through the furnace tube. Liquid diffusion sources act in a similar way, except that the carrier gas is bubbled through

the liquid impurity compound which is held at constant temperature to control its vapor pressure.

Solid diffusion sources are commonly in the form of discs of the same diameter as the wafers being diffused which are stacked between each wafer in the furnace.

The diffusion sources used in the K.S.U. laboratory were spin-on sources obtained from Emulsitone Company. These consist of compounds of the doping impurity, dissolved in an organic solvent. Using a photoresist spinner, the wafer is coated with a thin film of the diffusion source material. When the solvent evaporates, it leaves a layer of silicon dioxide doped with the impurity on the wafer surface. The impurity diffuses into the wafer when heated in the furnace.

Spin-on diffusion sources have the advantage of being cheap and simple to use. They do not require the precise metering systems needed when using gaseous or liquid diffusion sources. For each of the common impurities, spin-on sources are available in a range of formulations designed to give various surface impurity concentrations or other particular characteristics for specific applications. This makes spin-on sources simple to use, especially for experimental work.

5.2 Diffusion Theory

Diffusion in semiconductors is the movement of impurities along a concentration gradient. The process can be described by Fick's law (41, 49)

$$f(x,t) = -D. \frac{\partial N}{\partial x}$$

$f(x,t)$ is the rate of flow of impurity atoms through a plane at distance x below the surface, and N is the impurity concentration in atoms per unit volume. D is the diffusion coefficient, and is a strong function

of temperature.

In the solution of Fick's law, two special cases can be considered, corresponding to two diffusion situations

i) diffusion from an infinite source.

It is assumed that an infinite quantity of the impurity is present at the wafer surface, so the diffusion does not decrease the surface impurity concentration.

This leads to a solution in which the impurity concentration profile is characterised by the complementary error function

$$N_x = \frac{N_o}{2} \cdot \text{erfc} \frac{x}{2\sqrt{Dt}}$$

N_x is the impurity concentration at depth x, after a diffusion of duration t. N_o is the surface impurity concentration, and will generally be set by the solid solubility limit of the impurity in silicon.

ii) diffusion from a limited source.

When the quantity of impurity available is limited, diffusion of impurity into the wafer will lower the surface impurity concentration. The impurity concentration profile which results is characterised by the Gaussian distribution

$$N_x = \frac{Q}{\sqrt{\pi Dt}} \cdot e^{-x^2/4Dt}$$

Q is the number of impurity atoms present in the wafer (assumed initially to all be in a very thin surface layer).

A typical diffusion cycle would consist of an initial infinite source diffusion at a relatively low temperature, called a predeposit diffusion, to deposit a desired number of impurity atoms per unit area into the surface layer of the wafer. The impurity source is then removed, and a second diffusion called a drive-in diffusion is carried

out to redistribute these impurities to give the desired profile.

5.3 Measurement of Junction Depth (43)

The position of the p-n junction at the interface between a diffused region and the background silicon is considered to be the point where the impurity concentration from the diffusion equals the background impurity concentration.

It is frequently desirable to measure the position of this junction. This is normally done by lapping the wafer at an angle to the surface until the junction is exposed. The p and n regions can then be differentiated by appropriate staining, and hence the junction depth measured.

An angle-lapping tool, shown in Figure 5-1, was constructed. The

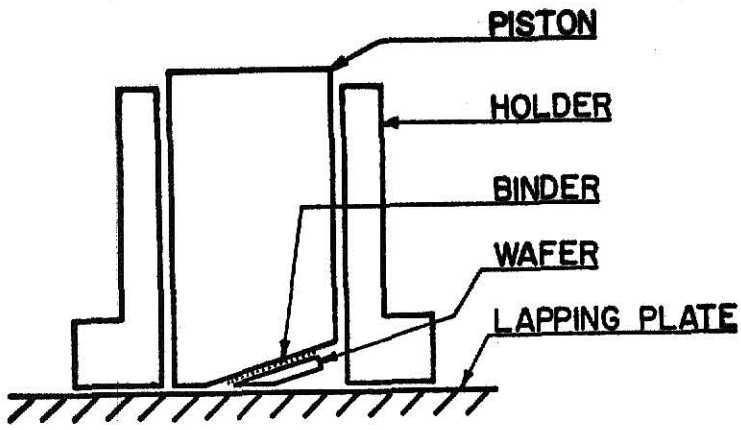


Figure 5-1. Angle Lapping Tool

tool consists of a cylindrical holder into which fits a piston constructed of hexagonal section brass stock. The lower face of the piston is ground at an angle of approximately 4° from perpendicular.

The sample of wafer was attached to the face of the piston with hard wax. The wafer was lapped on a sheet of Pexiglass, using Linde A

polishing compound (0.3μ alumina). Typically 10 minutes lapping was required to produce an adequate depth of cut.

After lapping, junction delineation was achieved by staining with '50-6' etch. This consists of

50 ml HF (4%)

6 drops HNO_3 (70%)

A few drops of the etch were put on the lapped wafer, and the region illuminated with a bright light source. The illumination apparently helps the staining reaction to occur, and it also makes it easier to see how the reaction is proceeding. The p-region stains dark, while the n-region and depletion layer remain unstained. When the specimen is judged to be adequately stained (usually 30 seconds to 1 minute) the specimen is washed and dried, then viewed with a microscope. If the staining is allowed to proceed for too long, the whole of the specimen can become stained and the junction can no-longer be distinguished. A number of junction delineations were made using this technique. It was found that with practice, satisfactory junction delineation could be achieved by this method in most cases.

The lapped surface intersects the p-n junction at a shallow angle. This effectively magnifies the junction depth, as shown in Figure 5-2.

The horizontal distance can be measured accurately using a micrometer eye-piece on the microscope, then the junction depth can easily be determined from a knowledge of the tool angle. The angle lapping tool built in the laboratory gave a bevel of approximately 4° which resulted in a horizontal magnification of junction depth of about 15x.

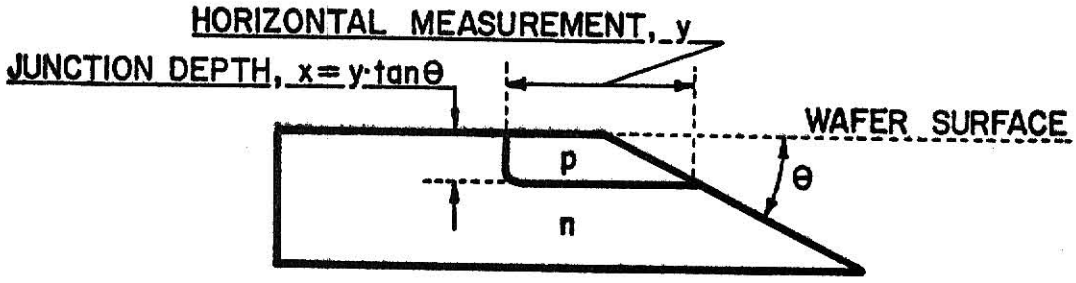


Figure 5-2. Junction Depth Measurement

A number of infinite source diffusions were carried out at various temperatures and for various times. With each, the junction depth was measured by lapping and staining, and compared with the expected value of junction depth obtained by calculation. These results showed a fair amount of variability between experimental and calculated values. However, it was later discovered that the spin-on diffusion source used had deteriorated, which probably accounted for the variability in the results.

5.4 Impurity Redistribution During Diffusion (41)

During each diffusion or oxidation, impurities already present in the wafer will diffuse further. In calculating final junction positions, account has to be taken of the entire sequence of thermal processing steps to which the wafer is subjected. This effect will, of course, cause movement not only of junctions formed by diffusion, but also of epilayer boundaries.

To minimize redistribution, impurities having relatively low

diffusion coefficients (e.g. arsenic and antimony) can often be used for doping in the early wafer processing steps, such as for epilayer doping.

5.5 Conductivity Type Determination

It is frequently desirable to be able to check the conductivity type of a wafer. Several methods exist for doing this (43), one of the simplest being the thermal emf method.

A simple instrument for measuring conductivity type was constructed. This consisted of two probes, spaced about 1 cm apart. One of the probes had a small heater attached to it. The heat caused carriers to migrate away from the hot probe, which thus became positive with respect to the cold probe for n-type material, or negative for p-type material. The polarity of the probes was detected using a galvanometer.

This method was found in general to give a simple and sensitive check on conductivity type. Some difficulty was occasionally experienced with high resistivity material, as this gave a very small deflection, and sometimes surface effects which masked the thermal e.m.f.

5.6 Resistivity Measurement

The resistivity of various wafer samples was measured with a linear 4-point probe. This consists of four equally spaced probe points. A current is passed between the outer two, and the voltage between the inner two probes is measured.

For a semi-infinite specimen, the resistivity is

$$\rho = 2\pi s \cdot \frac{V}{I}$$

s is the probe spacing which, for the probe used, was 0.159 cm. This gives a value for $2\pi s$ of 1 cm, so the resistivity ρ in ohm-cm is

given numerically by the value of V/I.

For thin specimens such as wafers a geometry correction has to be applied, and other corrections have to be used if measurements are made near the wafer edge (43, 49, 50).

For the case where the wafer thickness x is much less than the probe spacing s, and the probe is a long way from the edge of the specimen, the resistivity reduces to

$$\rho = 4.53 \frac{V}{I} \cdot x$$

This formula can also be used for measurements of the resistivity of an epilayer on the wafer of the opposite conductivity type.

In practice, considerable difficulty was found making accurate, repeatable measurements with the 4-point probe.

Chapter 6

METALLIZATION

The final major wafer processing steps required for integrated circuit manufacturing involve coating the wafer with a film of metal, usually aluminum, then selectively etching away the metal to leave the interconnection pattern which appropriately connects the various elements of the circuit.

6.1 Deposition of Metal Layer (41, 45)

The metal most commonly used for forming the interconnection pattern on integrated circuits is aluminum. It is normally applied by vacuum evaporation.

The wafers are placed in a vacuum chamber with the side to be coated facing the metallization source. The pressure in the chamber is reduced to below 10^{-5} torr in order that nearly all the aluminum atoms evaporated from the source will reach the wafers without colliding with residual air molecules. If the pressure in the chamber is too high, the quality of the resulting aluminum film will be poor.

The evaporation source can take several forms, but most commonly a tungsten filament is used. Electron-beam furnace sources are also used quite often. The aluminum is heated to a temperature of 800°-1000°C by passing a heavy current through the filament. At this temperature the vapor pressure of aluminum increases sharply and the metal rapidly evaporates from the source. The aluminum atoms condense on any object with which they come into contact, so in this way the wafers become coated with a film of the metal.

A number of wafers were coated with aluminum in the K.S.U. laboratory, using a length of high purity aluminum wire held in a tungsten filament as the evaporation source. The pressure in the vacuum chamber could not be brought below about 2×10^{-5} torr with the vacuum system available, but apparently satisfactory evaporations were achieved at this pressure.

It was not found necessary to heat the wafers during evaporation. This is sometimes done to improve adhesion and thus prevent undercutting of the metal during etching (38, 45), but in practice this did not prove to be a problem.

To give reasonably consistent results, the evaporation process was standardized as much as possible. With the filament located 6 cm below the wafer, a 15 mm length of aluminum wire 1.7 mm in diameter gave a satisfactory metal film, approximately 600 nm thick. The evaporation was made with a filament current of about 50 A. It was found that better quality films resulted from relatively slow evaporations, though it was not easy to reliably control the evaporation rate. It was found helpful to be able to view the filament while the evaporation was occurring, so that the melting of the aluminum followed by wetting of the filament could be observed. There was no significant evaporation until after the aluminum had wetted the filament, and until this occurred a shutter was used to shield the wafer from the source. This protected the wafer from a certain amount of spattering of aluminum which occurred during melting.

The desired thickness of the aluminum film on the wafer was about 500-600 nm. Thinner films than this (down to 150 nm) are commonly used for wafer metallization, but some trouble was experienced with breaks in the metallization over oxide steps when films of this thickness were

used. The principal objection to having too thick a film is that it obscures details on the wafer underneath the metallization, making mask alignment difficult. No alignment problems were experienced with 600 nm films.

The expected aluminum film thickness was calculated, assuming the evaporation to occur equally in all directions from the source. The sample of aluminum to be evaporated was weighed, then its volume calculated from a knowledge of the specific gravity of aluminum. Assuming that after evaporation this volume of aluminum is in a spherical shell of radius equal to the separation between filament and wafers, the expected film thickness is easily calculated.

The most common method of monitoring aluminum film thickness is to use a quartz crystal located in the plane of the wafers being coated. The metal deposited on the crystal will change its resonant frequency by an amount proportional to the film thickness. Unfortunately, a film thickness monitor of this type was not available, so it was necessary to use a less convenient technique.

The thickness of deposited films was measured using the Fizeau fringe method (section 3.6.3). A step was produced in the film by shading with a microscope slide during the evaporation. The measured film thickness corresponded quite closely to the expected film thickness calculated.

6.2 Etching the Aluminum Film

Immediately after removing the metal coated wafer from the vacuum chamber it was coated with photoresist, applied undiluted (59 cps) by spinning at 2000 rpm. No bake step was given prior to photoresist coating.

The standard process was used to define the interconnection image in the photoresist, except that it was found necessary to expose the resist for about 8 minutes, rather than the 4 minutes used when defining patterns over oxide.

The composition of the etch used to remove the excess aluminum is

70 ml phosphoric acid (conc.)

3 ml nitric acid (conc.)

27 ml water

This etch was used hot (approximately 80°C) with ultrasonic agitation. Etching was very rapid, taking only 30 seconds for a 600 nm thick aluminum film. The wafer was then rinsed in dionized water, and the resist stripped using 'Microstrip'.

6.3 Contact Sintering (41)

To form good contacts, it is necessary to sinter the aluminum metallization to the silicon. The eutectic temperature for aluminum and silicon is 577°C. Care must be taken not to exceed, or even approach, this temperature during sintering as the aluminum will rapidly penetrate the silicon and destroy the devices on the wafer. Contact sintering in the laboratory was carried out at 500°C for 5 minutes. On some wafers apparent over-sintering was evident, and a lower sintering temperature may be preferable.

A problem with using aluminum for interconnections is that aluminum is an acceptor impurity in silicon, so some precautions have to be taken if the contacts are to be ohmic rather than rectifying. Clearly there is no difficulty about making contacts to p-type regions. The problems arise when making contact to lightly doped n-type regions. Fortunately, the solid solubility of aluminum in silicon is only $6 \times 10^{18} cm^{-3}$.

Provided the contact is made to an n-region more heavily doped than this the contact will be ohmic. Standard practice is to make a shallow, heavily doped n diffusion at the location of all contacts between the metal and n-type regions.

Chapter 7

CIRCUIT DESIGN AND FABRICATION

The design and fabrication of a 'D' flip-flop and a separate gate using substrate-fed I^2L technology was carried out in the K.S.U. laboratory. Design parameters were based on those used by Blatt et. al. (30).

7.1 Circuit Design

The circuit of a 'D' flip-flop implemented using conventional TTL-NAND gates is shown in figure 7-1. This circuit was converted to a design suitable for implementation in I^2L by appropriately taking account of the differences between the gate characteristics. The principal differences are:

i) The TTL-NAND gate is essentially a multiple input, single output structure, while the I^2L gate is a single input, multiple output structure.

ii) NAND gate inputs may be tied together but I^2L gate inputs may not.

iii) NAND gate outputs must not be tied together but I^2L outputs can be.

The resulting 'D' flip-flop implemented in I^2L is shown in Figure 7-2. Comparison of this circuit with the NAND gate implementation of Figure 7-1 shows how the above rules affect the design. A separate buffer to give two isolated clock signals for different points in the circuit is required for the I^2L layout. The corresponding buffer at the clock input is not required by the TTL-NAND gate design, but has

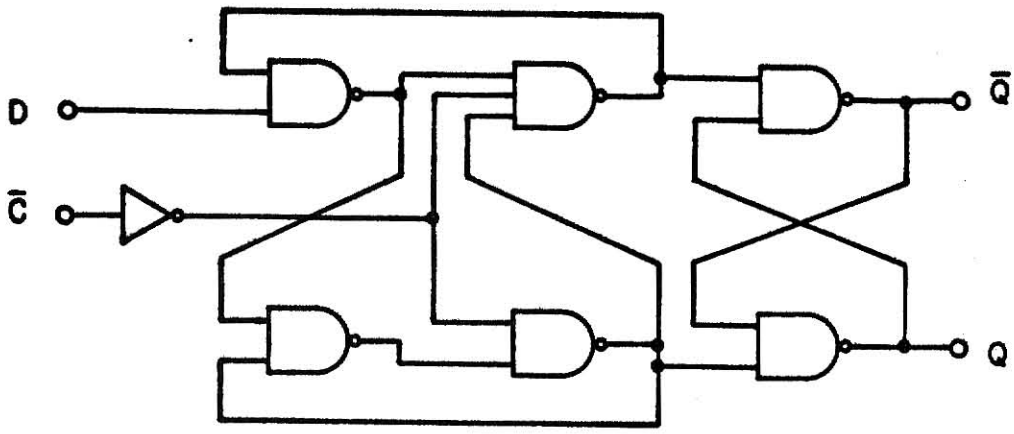


Figure 7-1. Implementation of 'D' Flip-Flop with NAND Gates

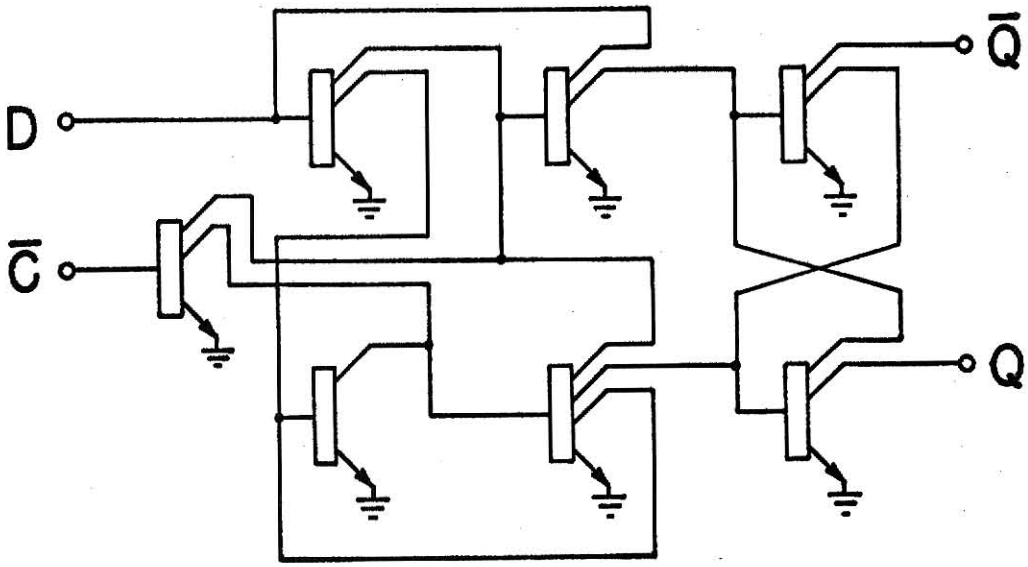


Figure 7-2. I^2L 'D' Flip-Flop

been included only to make the two circuit layouts completely equivalent.

7.2 Wafer Specifications

Wafers on which to construct the substrate-fed I^2L circuit were obtained from Transitron Electronics Corp.

The wafers are a p-substrate, with n and p epilayers formed on them.

The manufacturer's specification of the wafers is:

<100> substrate, 2" diameter, p-type

resistivity 0.02 ohm-cm, boron doped

n-epilayer 2.9μ thick

resistivity 0.09 ohm-cm, arsenic doped

p-epilayer 3.5μ thick

resistivity 4.4 ohm-cm, boron doped

The above specification applies to wafers from run number H/C 27313. Wafers from run number H/C 27329 have the same specification except for the p-epilayer which is 3.8μ thick, and of 3.4 ohm-cm resistivity.

7.3 Circuit Layout

A circuit layout for the 'D' flip-flop was developed, based on using the substrate fed I^2L structure shown in Figure 7-3.

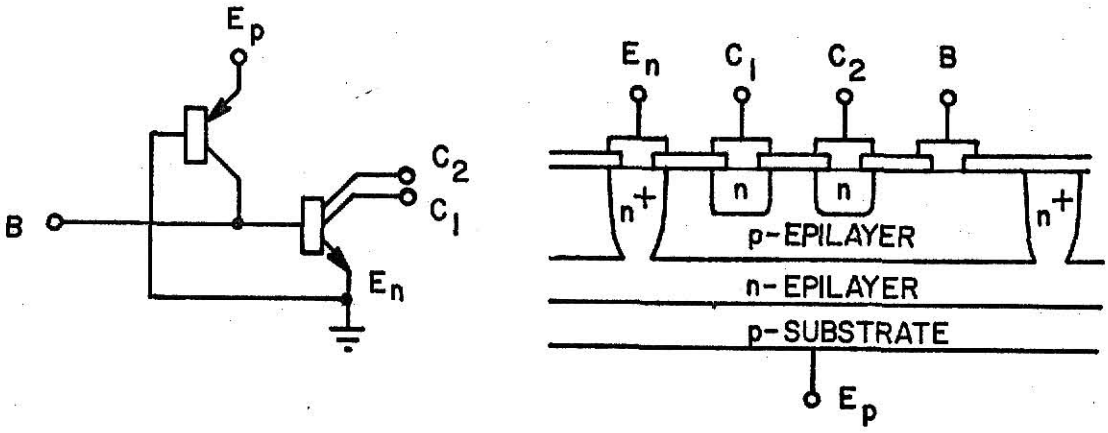


Figure 7-3. Substrate Fed Logic Structure

The layout of the basic gate cell was as shown in Figure 7-4.

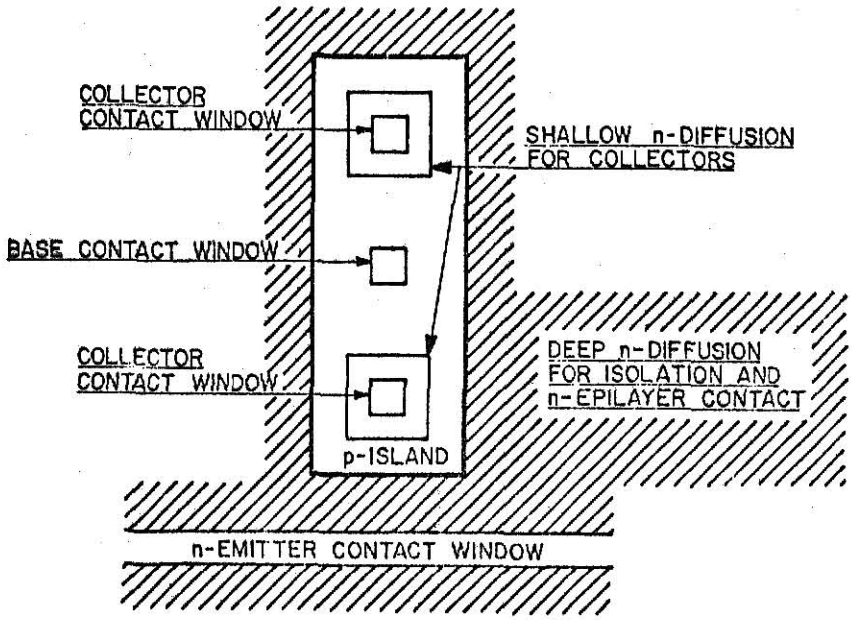


Figure 7-4. Basic Gate Layout

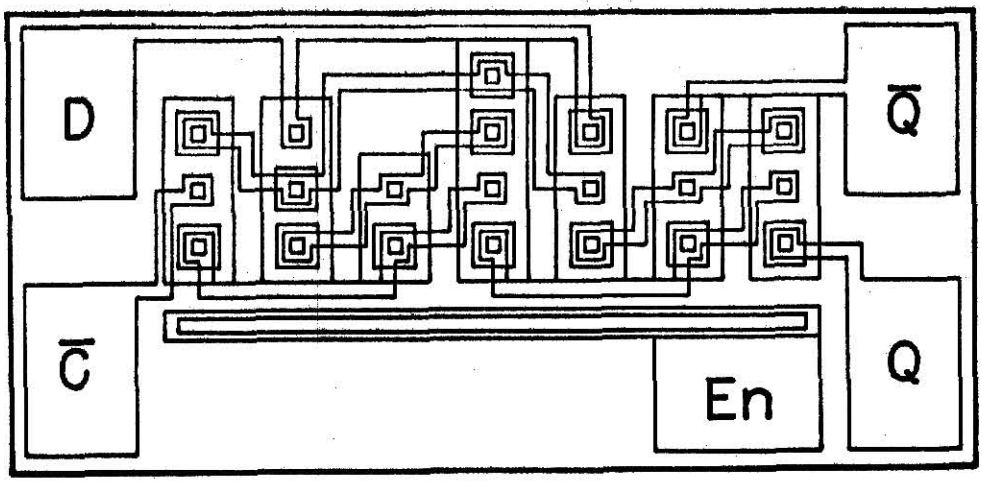
The photoreduction tests discussed in Chapter 4 indicated that the production of masks with a minimum detail size of 12 microns should be possible with the equipment available. It was considered that the mask aligner available was suitable for handling masks with this detail size, provided some care was taken. The motivation for working with a fairly small-geometry structure is that this gives a circuit which corresponds reasonably well to current industry standards, and which is thus more realistic in terms of its performance and problems than a circuit built with larger geometries might be.

The design rules used for the layout are:

i) minimum line widths, apertures and alignment tolerances to be 12

ii) no metallization crossovers permitted. (i.e.: will use only a single layer of metallization.)

iii) minimization of the separation between the base contact and the most distant collector contact in the gate. The importance of this constraint was not fully known, but it was felt intuitively that



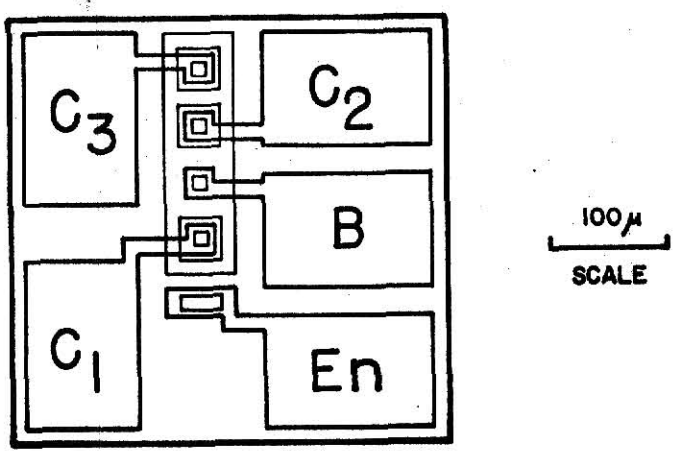


Figure 7-5. Layout Design of Flip-Flop and Gate

an excessively large separation between base and collector must be undesirable for best performance.

Using these design rules, a layout diagram of the flip-flop was prepared at a scale of 250x final size. This is shown in Figure 7-5. In addition, a layout for an isolated I^2L gate with three collector contacts was designed, and is also shown in Figure 7-5.

7.4 Preparation of Photographic Masks

Four masks were required for processing the circuit.

Mask 01 - first diffusion. This mask defines the deep n-diffusion for isolating the p-islands and making contact to the n-epilayer.

Mask 02 - second diffusion. The second mask defines the shallow collector diffusion.

Mask 03 - metallization contact windows. This mask opens windows in the oxide layer where the metallization is to make contact with the circuit.

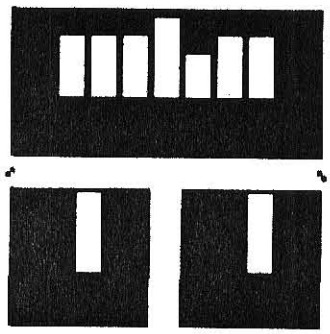
Mask 04 - interconnection mask. This mask defines the metal interconnection pattern.

7.4.1 Cutting of Rubylith master layout

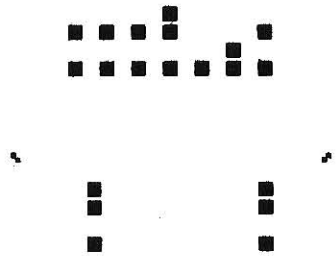
Using the circuit layouts (Figure 7-5) as a guide, Rubylith masters were cut for each of these masks. The mask patterns are shown reduced 5x in Figure 7-6.

The patterns show the basic element of the mask, which is a cell consisting of a 'D' flip-flop and two isolated gates.

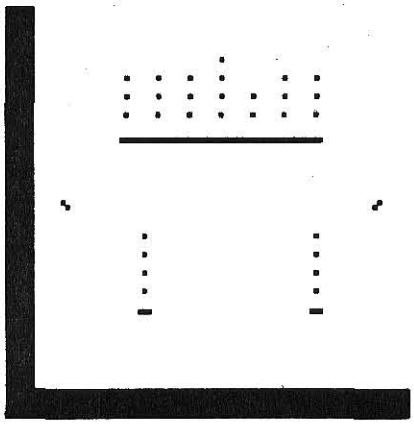
The Rubylith layouts were cut in the form which required minimum stripping. For the first three masks, this gave the correct image in the



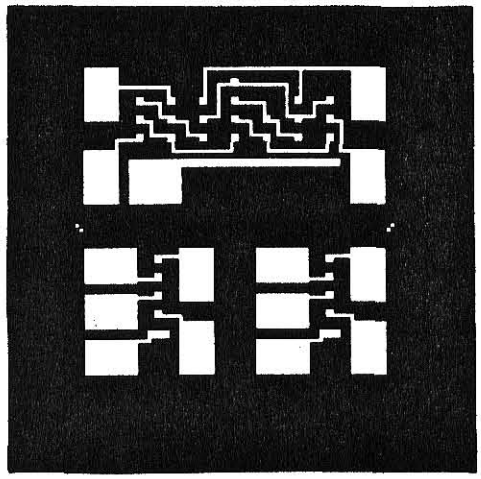
Mask O1
First Diffusion



Mask O2
Second Diffusion



Mask O3
Contact Windows



Mask O4
Interconnect Metallization

Figure 7-6. Mask Layouts After First Reduction

final mask (i.e.: the correct regions were opaque). However, the interconnection mask required an additional photographic reversal to give the correct final mask. This was achieved by making a contact negative of the first reduction image. Stripping the Rubylith for this mask to give the correct final image without reversal would have been very difficult.

During diffusion, the impurity not only diffuses downwards, but laterally under the oxide as well. The lateral diffusion extends approximately as far under the mask edges as the depth of the diffusion. The first diffusion was to be approximately 4μ deep. Accordingly, an allowance for lateral diffusion was made when cutting the pattern for mask 01 by locating the edges of all windows in from the desired diffusion boundary by a distance equivalent to 4μ in the final mask.

Since the second diffusion was much shallower, it was not considered necessary to allow for lateral diffusion when cutting its mask pattern.

On the metallization contact mask (mask 03) a 75μ wide scribing grid was drawn around the chip, so that scribing of the wafer could be done on bare silicon rather than on oxide.

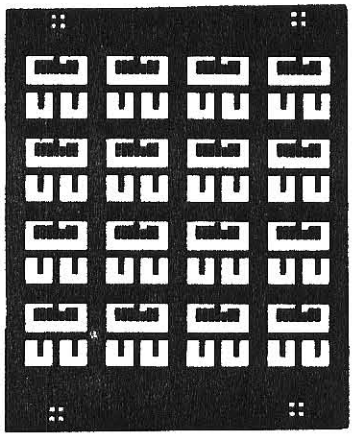
Alignment marks were included on each mask pattern to assist in laying out the pattern array.

7.4.2 First reduction

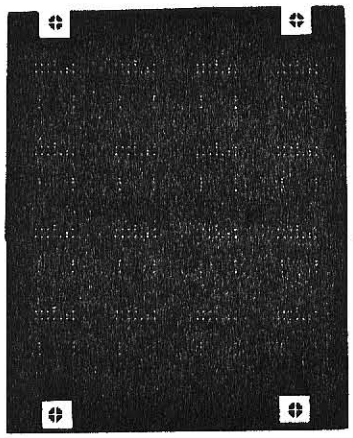
A 5 x reduction was made of each mask, using the procedures recommended in Section 4.1.2. A contact negative of mask 04 was made to give the required image reversal. First reductions of each mask are shown in Figure 7-6.

7.4.3 Second reduction

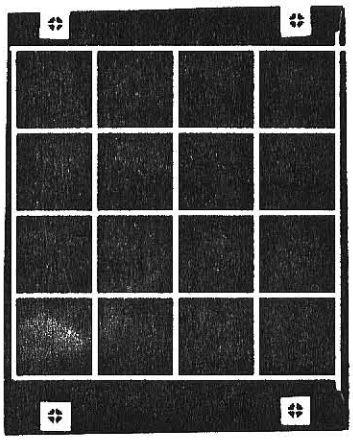
For each mask, sixteen first reduction prints were laid out in a



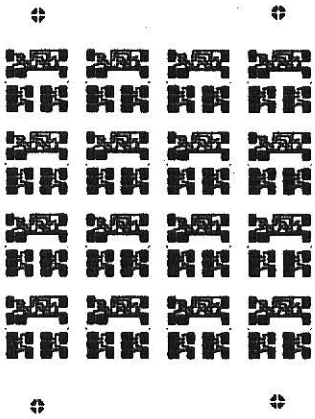
Mask 01
First Diffusion



Mask 02
Second Diffusion



Mask 03
Contact Windows



Mask 04
Interconnect Metallization

Figure 7-7. Second Reduction Layout

4 x 4 array, by taping down on transparent mylar film. When laying out the arrays for masks 02, 03 and 04, each element of these arrays was very carefully aligned with the corresponding element of mask 01. Additional alignment marks were inserted to assist in the next layout.

The arrays for each mask were then photographed at 5 x reduction, using the procedures recommended in section 4.1.3. The resulting prints are shown in Figure 7-7. When making these exposures, the effects of any distortion in the camera system were minimized by placing each layout in the same position on the lightbox screen, and at the same orientation.

7.4.4 Third reduction

Four second reduction prints for each mask were formed into an array. This array contains 64 identical cells consisting of the 'D' flip-flop and two isolated gates. As before, each print in the array for masks 02, 03 and 04 was carefully aligned with the corresponding print of the mask 01 array. A further set of alignment masks was placed on the array to assist in aligning the final photographic masks with details on the wafer.

The final layout for mask 04 (interconnection mask) is shown in Figure 7-8. Similar arrays were of course produced for the other three masks.

A 10x reduction of each layout was made onto Kodak High Resolution Plates, using the procedure described in section 4.1.4. The Asahi Super-Takumar 55mm, f/1.8 lens was used mounted in an Asahi Pentax 35mm camera. To fit the plates into the camera without extensively modifying the camera body, it was found convenient to cut the $2\frac{1}{2}$ inch square photographic plates in half. These half-plates then could be easily mounted in the camera body. The plates were cut using a

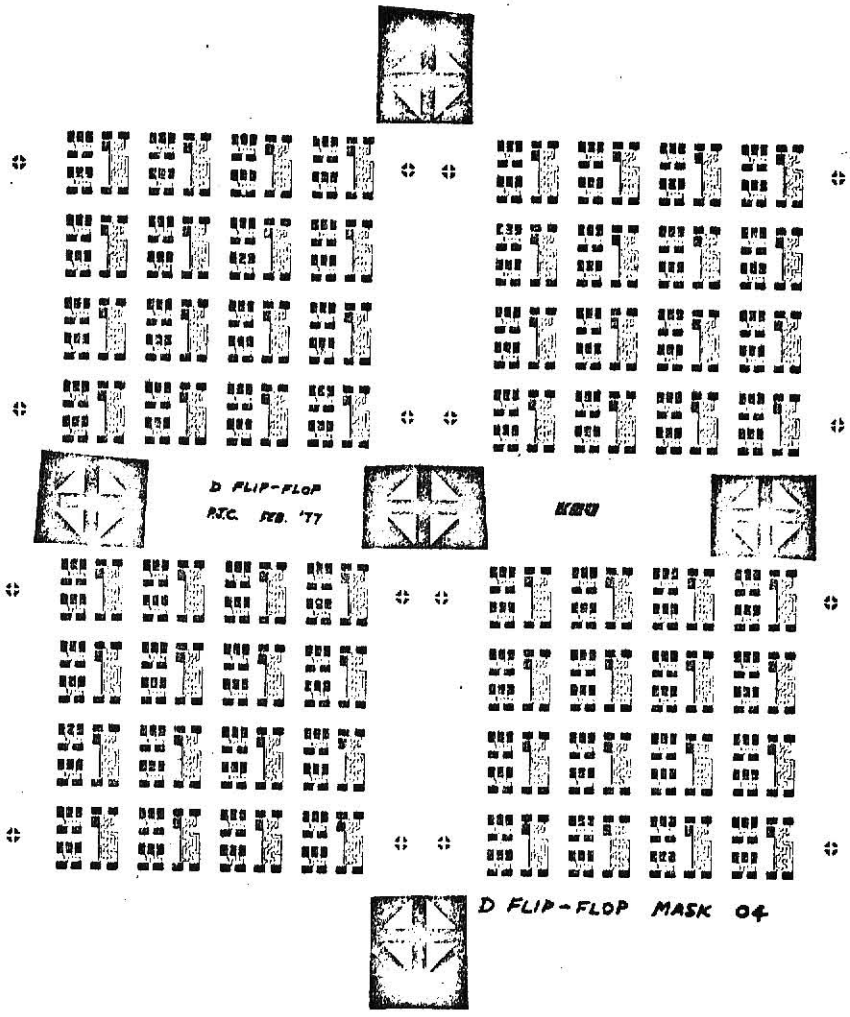


Figure 7-8. Layout of Mask 04 Before Final Reduction

conventional glass cutter. Extreme care was taken to avoid contaminating the plates with glass fragments or dirt while cutting them.

Very careful examination of the masks produced showed the quality of the images to be completely satisfactory for the application.

The layout procedure described above for producing an array of circuit cells on the mask was extremely tedious, but it did produce a very satisfactory set of masks. However, a step and repeat camera, if available, would have saved a great deal of time.

7.5 Wafer Processing Calculations

A number of calculations need to be made to determine the parameters for the wafer processing steps.

7.5.1 Required oxide thickness

An estimate of the first diffusion parameters is needed before this and other processing calculations can be made.

From the results of diffusion tests made previously, and checked by angle lapping and staining (section 5.3) it is estimated that a phosphorus diffusion of 20 minutes at 1200°C will be appropriate for the first diffusion, to make contact to the n-epilayer.

Figure 3-3 indicates that an oxide layer at least 600 nm thick is needed to mask this diffusion. It was decided to use an oxide layer about 700 nm thick to give a margin of safety.

Figure 3-2 indicates that this thickness of oxide can be grown in approximately 120 minutes at 1000°C.

7.5.2 Silicon removed during oxidation

During oxidation, a layer of silicon 0.46 times the oxide layer thickness goes to form the oxide.

For an oxide thickness of 700 nm, 320 nm of silicon will be removed from the top epilayer.

7.5.3 Epilayer movement during diffusion

During each high temperature process, impurities already present in the wafer will become redistributed. In particular, there will be p-type material diffused from the substrate into the more lightly doped n-epilayer, and there will be diffusion of impurity from the n-epilayer into the p-epilayer.

In determining the final epilayer boundaries, the total thermal

cycle should be considered, though the initial diffusion will be the dominant step, since this occurs at higher temperature and the diffusion coefficient is a very strong function of temperature.

Assume the thermal cycle to be

initial oxidation	120 minutes	1000°C
first diffusion	20 minutes	1200°C
oxidation	60 minutes	1000°C
second diffusion	10 minutes	1000°C
oxidation	30 minutes	1000°C

i.e.: a total of 20 minutes at 1200°C plus 220 minutes at 1000°C.

The diffusion is assumed to be from an infinite source, (see section 5.2). The impurity profile is thus given by

$$N_x = N_o . \text{erfc} \frac{x}{2\sqrt{Dt}}$$

An equivalent diffusion can be considered, by assuming $Dt = D_1 t_1 + D_2 t_2$ where D_1 and t_1 are the diffusion coefficient and time at temperature T_1, and D_2, t_2 apply to temperature T_2.

The parameter $\sqrt{Dt}$ is known as the 'diffusion length' of the diffusion process.

i) diffusion of the n-epilayer into the p-epilayer. The n-epilayer dopant is arsenic. From Burger and Donovan (37) the diffusion coefficients for arsenic are

$1200°C$: $D_1 = 2.3 \times 10^{-13} cm^2\ sec^{-1}$, $t_1 = 20$ min

$1000°C$: $D_2 = 1.2 \times 10^{-15} cm^2\ sec^{-1}$, $t_2 = 220$ min

$$Dt = D_1 t_1 + D_2 t_2$$
$$\simeq 2.76 \times 10^{-10} + 1.73 \times 10^{-11}$$
$$= 2.93 \times 10^{-10}\ cm^2$$

N_x is taken as the background concentration in the p-epilayer, and N_o

is the impurity concentration in the n-epilayer

$$N_x = 4 \times 10^{15} \text{ cm}^{-3}$$

$$N_o = 1 \times 10^{17} \text{ cm}^{-3}$$

$$\therefore N_x/N_o = 4 \times 10^{-2}$$

The value of $\frac{x}{2\sqrt{Dt}}$ can be found from tables or graphed values of the erfc function (41, 45)

$$\therefore \frac{x}{2\sqrt{Dt}} = 1.40$$

Substituting for Dt gives a value for the movement of the epilayer boundary of 0.48μ.

ii) diffusion of the substrate into the n-epilayer. A similar calculation can be made for the movement of this boundary. The substrate dopant is boron, giving

$$1200^{\circ}\text{C} : \quad D_1 = 1.3 \times 10^{-12} \text{ cm}^2 \text{ sec}^{-1}$$

$$1000^{\circ}\text{C} : \quad D_2 = 1.9 \times 10^{-14} \text{ cm}^2 \text{ sec}^{-1}$$

The source concentration N_o is the substrate concentration of 5×10^{18} cm^{-3}, while N_x is the n-epilayer concentration of 1×10^{17} cm^{-3}.

Substituting these values, and performing a similar calculation to that above, indicates that the boundary between the substrate and n-epilayer will move by 1.4μ during the thermal cycle.

It can be seen from the above figures that nearly all the movement occurs during the short but high temperature first diffusion.

7.5.4 First diffusion parameters

The thickness of the p-epilayer after oxidation, and after account has been taken of the movement of the epilayer boundary caused by the diffusion will be 3.0μ. This layer is doped to give a resistivity of 3.4 ohm-cm, which corresponds to a doping level of 4×10^{15}cm^{-3}.

The diffusion is to be made using as a source 'phosphorosilicafilm'

spin-on dopant (Emulsitone Co.), designed to give a surface concentration of $5 \times 10^{20} cm^{-3}$.

The diffusion will be an infinite source diffusion. The diffusion profile is thus given by (see section 5.2)

$$N_x = N_o . \text{erfc} \frac{x}{2\sqrt{Dt}}$$

At 1200°C, the diffusion coefficient for phosphorus is $3.7 \times 10^{-12} cm^2 . sec^{-1}$.

Taking

$$N_o = 5 \times 10^{20} \ cm^{-3}$$

$$N_x = 4 \times 10^{15} \ cm^{-3}$$

i.e.: the junction position is where the concentration of diffused impurity equals the background doping level.

$$N_x / N_o = 8 \times 10^{-6}$$

$$\therefore \quad \frac{x}{2\sqrt{Dt}} = 3.15$$

(from graphical tabulation of the erfc function (41, 45)).

We require the diffusion depth x to be at least 3.0μ. Substituting the above values gives a diffusion time of 11 minutes for a 3μ diffusion.

It was decided that it would be desirable to use a somewhat deeper diffusion than the absolute minimum required to ensure good ohmic contact to the n-epilayer. A diffusion time of 20 minutes at 1200°C gives a diffusion depth of approximately 4μ, so this diffusion time was chosen.

7.5.5 Second diffusion parameters

The second diffusion is much shallower, and is consequently made at a lower temperature than the first diffusion. However, for this diffusion significant junction movement will occur during the oxidation step

after the diffusion, since this oxidation is made at the same temperature as was used for the diffusion. For the first diffusion, the subsequent oxidation and second diffusion steps did not significantly alter the junction position, as the diffusion length for the first diffusion was much greater than the combined diffusion lengths of subsequent processing steps.

This condition does not apply for the second diffusion, and the equivalent diffusion time is taken to be the duration of the diffusion itself plus the duration of the subsequent oxidation at the same temperature.

For this diffusion, the same surface and background impurity concentration values apply as for the first diffusion. However, the diffusion coefficient is now $1.5 \times 10^{-13} cm^2 sec^{-1}$.

It was considered that a diffusion depth of 1μ would be sufficient for the first attempt, though this would leave a base width (separation between the junction formed by the second diffusion, and the boundary between the p and n-epilayers) of about 2μ which is rather wide.

Performing a calculation similar to that made for the first diffusion gives a total diffusion time required of 28 minutes (diffusion plus subsequent oxidation) for a junction depth of 1μ.

It was considered that a diffusion of less than 10 minutes duration would be difficult to make with any accuracy, and that the oxide growth during a 20 minute oxidation at 1000°C (250nm) was probably a little thin. Accordingly, it was decided to make a 10 minute diffusion, followed by a 30 minute oxidation step. This would increase the junction depth to 1.2μ, which was considered acceptable.

The above calculations are included to demonstrate the design

procedure. However, the processing steps are clearly interdependent, and consequently an iterative series of calculations is required to fully determine the optimum processing sequence.

7.6 Details of Wafer Processing Steps

The sequence of operations described below was used for producing the substrate fed I^2L flip-flop circuit.

During cleaning, and for subsequent processing steps as appropriate, the wafer was held in a polypropylene basket. This avoided the need to touch the wafer when transferring it from one reagent or processing step to another. When the wafer had to be removed from the basket, special stainless steel wafer-tweezers were used. Whenever possible, processing steps were conducted in a laminar flow hood to reduce contamination risk.

At each stage in the processing, the wafer was carefully examined with a microscope to check that the processing had been completed satisfactorily. If not, the process step was repeated.

Though not always mentioned specifically, thorough rinsing in deionized water was carried out between each processing step.

1) A wafer from batch H/C27329 was thoroughly cleaned, using the standard procedure described in section 3.4.

2) The wafer was oxidized using the open tube steam process at 1000°C for 140 minutes. This gave an oxide layer approximately 750 nm thick.

3) Using the standard photoresist process described in section 4.2.2, the details of mask 01 were transferred to the photoresist.

4) The wafer was etched in buffered HF for 8 minutes. The resist was then stripped using 'Microstrip' and the wafer rinsed in deionized water.

5) The wafer was cleaned in hot mixed (nitric plus sulfuric) acid for 5 minutes, followed by 5 minutes ultrasonic agitation then a thorough rinse in dionized water.

6) The wafer was coated with phosphosilicafilm, $C_o = 5 \times 10^{20}$, by spinning at 3000 rpm for 1 minute.

7) The wafer was diffused at 1200°C for 20 minutes.

8) Immediately on removal from the furnace, the wafer was placed in boiling deionized water for 5 minutes. It was found that if this step was omitted, a phosphorus glass film which was hard to etch developed on the wafer surface.

9) The wafer was immersed in buffered HF for $1\frac{1}{2}$ minutes to remove the phosphorus glass layer, followed by a thorough deionized water rinse.

10) A new layer of oxide was grown in steam at 1000°C for 75 minutes.

11) Using the standard photoresist procedure, the details of mask 02 were defined on the wafer. This required alignment of the mask with the details from mask 01 already on the wafer. Some problem was experienced in finding a satisfactory illumination system for viewing the wafer during the alignment process. The problem was solved reasonably adequately by shining a beam of light down one barrel (with eyepiece removed) of the stereo viewing microscope on the mask aligner. A red filter was included to avoid risk of exposing the photoresist. The wafer and mask were viewed through the other barrel of the microscope. This gave suitable illumination to enable the wafer and mask to be aligned to the required accuracy.

12) The wafer was etched in buffered HF for 8 minutes, followed

by stripping of the photoresist and a hot mixed acid cleaning step.

13) A layer of phosphorosilicafilm $C_o = 5 \times 10^{20}$ was applied by spinning at 3000 rpm.

14) The second diffusion was carried out at 1000°C for 10 minutes.

15) Without removing the wafer from the furnace after the previous diffusion step, an oxide layer was grown on the wafer. This was achieved by simply connecting the source of steam to the furnace at the completion of the 10 minute diffusion. The oxidation was for 30 minutes at 1000°C.

16) Using the standard photoresist process, the wafer was exposed to mask 03 and the contact windows opened in the wafer by etching in buffered HF for 8 minutes.

17) Following resist-stripping and acid cleaning steps, a film of aluminum approximately 500 nm thick was evaporated on the wafer.

18) The interconnection pattern (mask 04) was defined in photoresist on the metallization layer, and the excess metal removed with aluminum etch as detailed in section 6.2. This was followed by stripping of the resist, and thorough rinsing in deionized water.

19) A layer of aluminum was evaporated onto the back of the wafer to enable contact to be made to the substrate. During this step, the front of the wafer was shielded with a glass slide to avoid any contamination of the circuit.

20) As the final processing step, the wafers were sintered at 500°C for 5 minutes to form good ohmic contacts.

This completed the wafer processing sequence, and the circuits on the wafer are now ready for testing.

7.7 Wafer Testing

Contact to the wafer for testing was made using a manual probe station. This had four probes which could be moved by micropositioner controls. To provide a fifth probe needed for some of the testing, a simple micropositioner was constructed from a small x-y table mechanism.

Attempts to construct a probe-card with a probe array fixed in the correct positions for testing a single circuit proved only partially successful, and were not pursued.

Reliable contact to the back of the wafer proved to be somewhat of a problem. This was finally overcome by attaching a wire to the aluminized surface, using indium metal as a solder.

Chapter 8

RESULTS AND CONCLUSIONS

The fabrication procedure described in the previous chapter resulted in the production of circuits which, at least to visual inspection, appeared completely satisfactory. A microphotograph of a completed circuit on the wafer is shown in Figure 8-1.

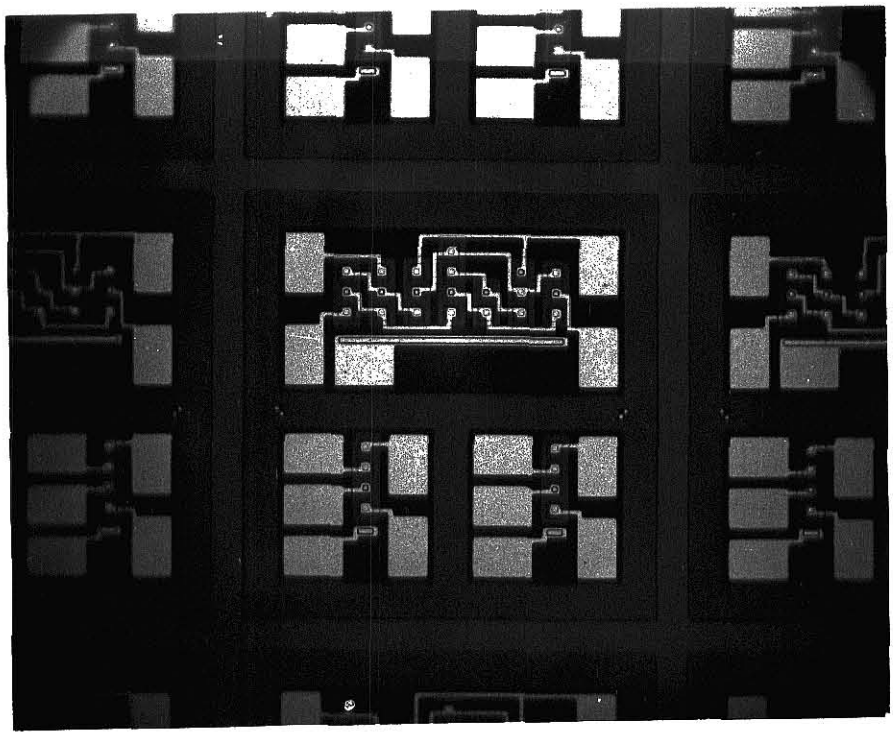


Figure 8-1. Microphotograph of Completed Wafer (100X)

The greatest alignment problem was experienced with the interconnection mask (mask 04). It would have been desirable to use larger metal pads for making contact to the circuit through the oxide windows. Slight misalignment did occur in some cases, but not sufficient to

cause the metallization to fail to make contact with the circuit elements.

The majority of the testing was made using a Tektronix Model 576 Curve Tracer, since this showed the device characteristics in a very convenient form.

On account of their simplicity, most of the initial testing was carried out on the isolated inverter-gates.

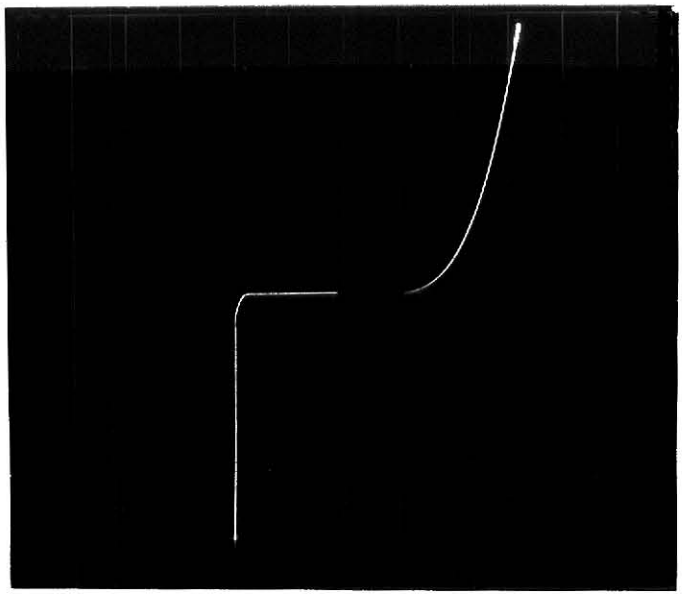
8.1 Circuit Characteristics

The diode characteristics of the various junctions within the inverter were examined, and are shown in Figure 8-2. Contact labelling conforms to that of Figure 7-3.

The characteristics of the diodes formed between the base and the collector diffusion regions, and between the base and the emitter E_n are quite satisfactory. The diodes show a clean reverse breakdown at about 100 volts for the base-collector junctions, and a similar result for the base-E_n junction. These breakdown voltages are close to the expected values for the doping levels involved (50). Forward characteristics are also reasonably typical. The characteristic of the base-collector diodes in particular shows a fairly high impedance as would be expected from the high resistivity of the base region.

The characteristics of the junction between E_p and E_n (substrate to n-epilayer) are less satisfactory. This shows very high leakage and no true avalanche breakdown is observable. The reasons for this poor characteristic are not clear.

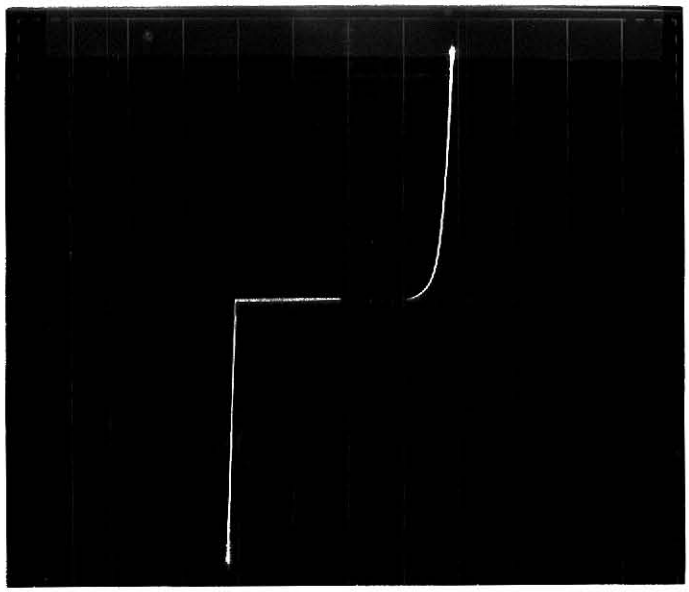
The characteristics measured between two collector-regions are also different from expected. The structure shows high leakage, and no clean avalanche breakdown was observable.



VERT: 100μA/div

HOR:
V+ve 500mV/div
V-ve 50V/div

Base to Collector Junction



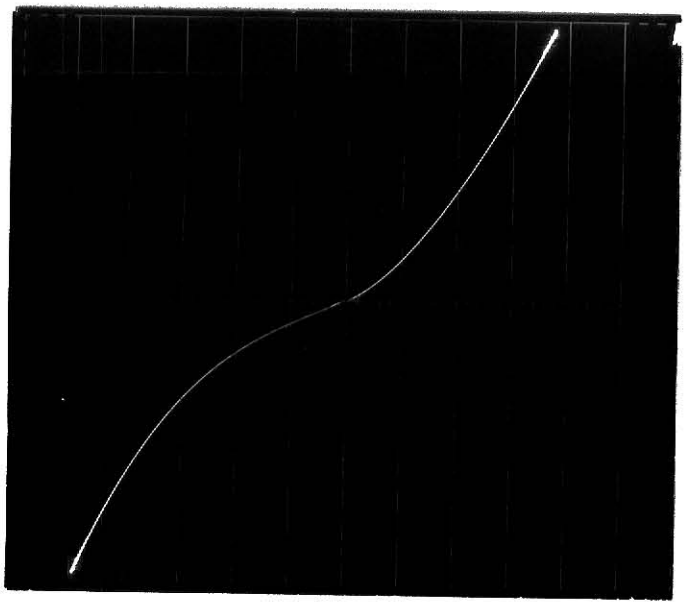
VERT: 100μA/div

HOR:
V+ve 500mV/div
V-ve 50V/div

Base to n-p-n Emitter (En) Junction

Figure 8-2. Characteristics of Circuit Junctions

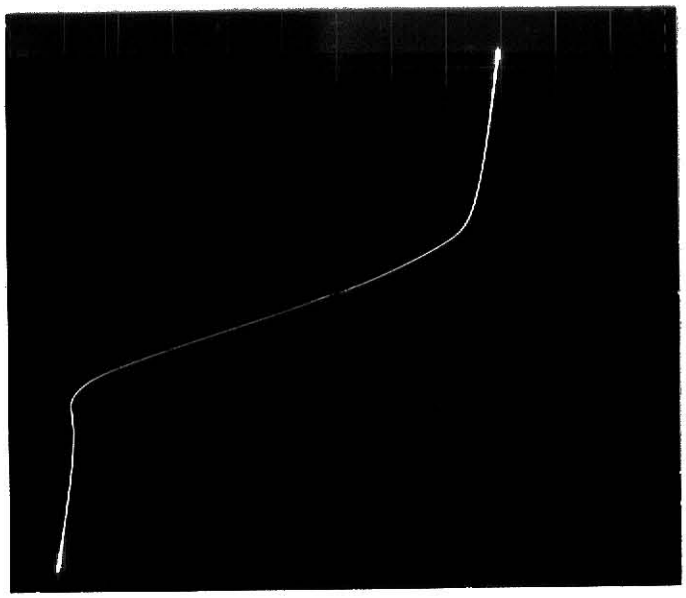
(continued over)



VERT: 100μA/div

HOR: 200mV/div

p-n-p Emitter (E_p) to n-p-n Emitter (E_n) Junction
(substrate to n-epilayer)



VERT: 100μA/div

HOR: 500mV/div

Collector to Collector Characteristic

Figure 8-2 (cont): Characteristics of Circuit Junctions

Tests were made on the characteristics of the n-p-n switching transistor. This showed poor characteristics, with high leakage and very low β. The reverse characteristics, formed by connecting this transistor with the E_n terminal as collector, and a collector as emitter, were better (as would be expected) though still very poor.

Tests were made on the 'D' flip-flop, operated in the I^2L mode. Current was supplied to the circuit through the E_p (substrate) terminal. No observable functioning of this circuit could be detected. Injection currents used ranged from 100 nA to 100 mA. Attempts were also made to operate the circuit using light to supply the necessary carriers, but without success.

It was strongly suspected that the problems related to the very poor characteristics observed for the E_n-E_p junction (Figure 8-2).

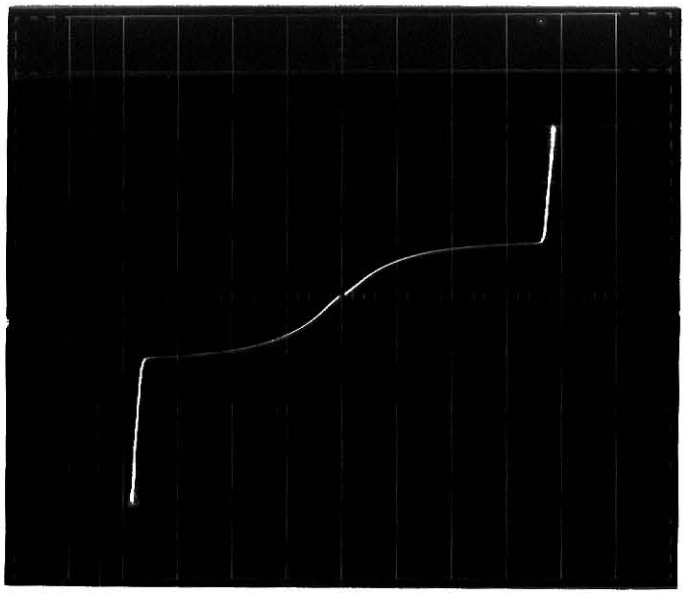
The pnp injection transistor could not be made to show any transistor characteristics at all, unless an extremely high base drive was used (about 50 mA). However, the resulting β for the transistor was less than 0.01!

8.2 Diffusion Tests

Examination of the possible causes of poor characteristics from this device lead to the conclusion that the first diffusion cycle may be too long, or at too high a temperature.

Tests were made to determine the minimum diffusion required to obtain the desired electrical characteristics from this diffusion. The requirements for the diffusion is that it should make ohmic contact with the n-epilayer.

Accordingly, a series of diffusions were made, using mask 01, at various temperatures and for various times. The impedance characteristics



VERT: 1mA/div

HOR: 5V/div

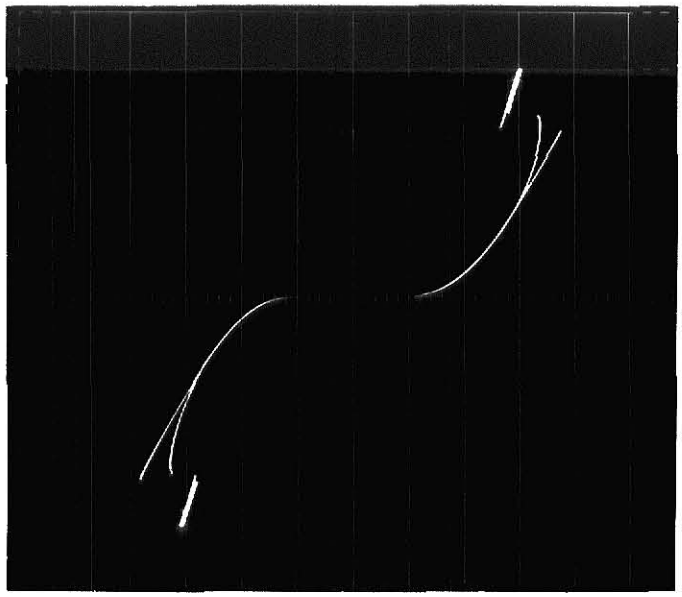
8 minutes, 1050°C

VERT: 1mA/div

HOR: 1V/div

32 minutes, 1050°C

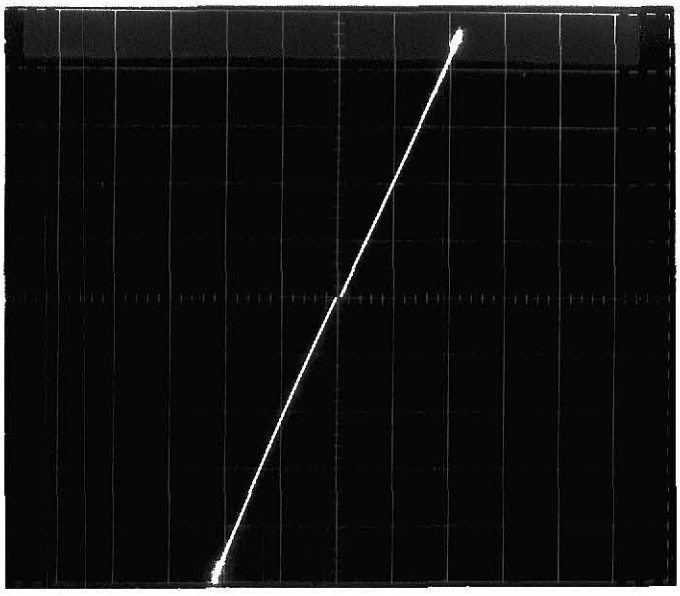
Figure 8-3. Diffusion Tests on Wafer - Characteristics Between Diffused Regions (cont. over)



VERT: 1mA/div

HOR: 1V/div

50 minutes, 1050°C



VERT: 1mA/div

HOR: 1V/div

72 minutes, 1050°C

Figure 8-3 cont: Diffusion Tests on Wafer

between two separate n-diffused regions were then examined.

It was found that even with a diffusion of only 10 minutes at 1200°C, the characteristic between two n-regions was linear.

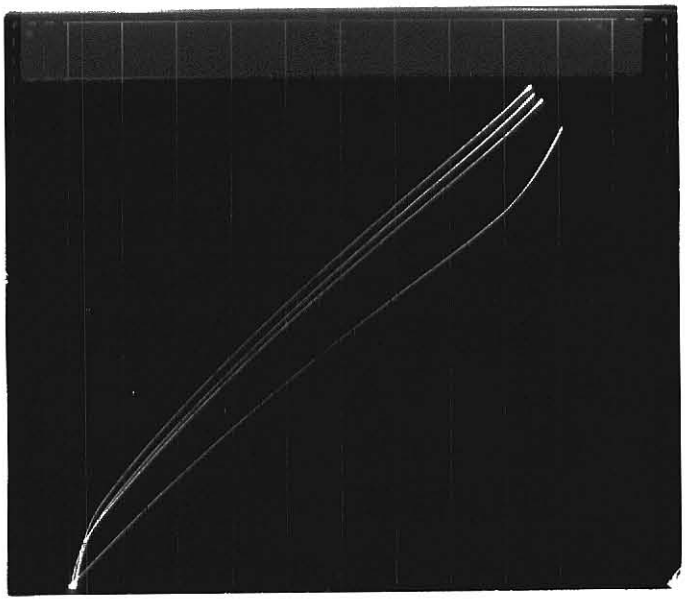
Further tests were made at a diffusion temperature of 1050°C. For diffusion times up to 50 minutes, a non-ohmic characteristic was obtained. However, at the 72 minute diffusion a very clear transition to ohmic characteristics between two n-regions was shown. This can be seen in Figure 8-3. This very short diffusion to give contact with the n-epilayer is puzzling in view of the results of the diffusion calculations carried out earlier (section 7.5.4). From theoretical considerations, this diffusion should give a junction depth between 2.0 and 2.5 microns, which is considerably less than would be expected to be required from the wafer specification.

8.3 Improved Wafer Fabrication Processes

More circuits were fabricated using the same processing sequence as described in section 7.6, except that the first diffusion was now 72 minutes at 1050°C, followed by an oxide growth of 20 minutes at the same temperature. This oxide was grown without removing the wafer from the furnace after the diffusion step, but simply by introducing water vapor into the furnace at the completion of the diffusion step.

Tests on completed circuits showed diode characteristics similar to those discussed for the earlier device (section 8-1). The diode characteristic between the E_n and E_p terminals still looked extremely poor.

Reasonable transistor characteristics were now obtained for both the forward and reverse characteristics of the switching transistor, (figure 8-4) except that a high resistive leakage path was evident.

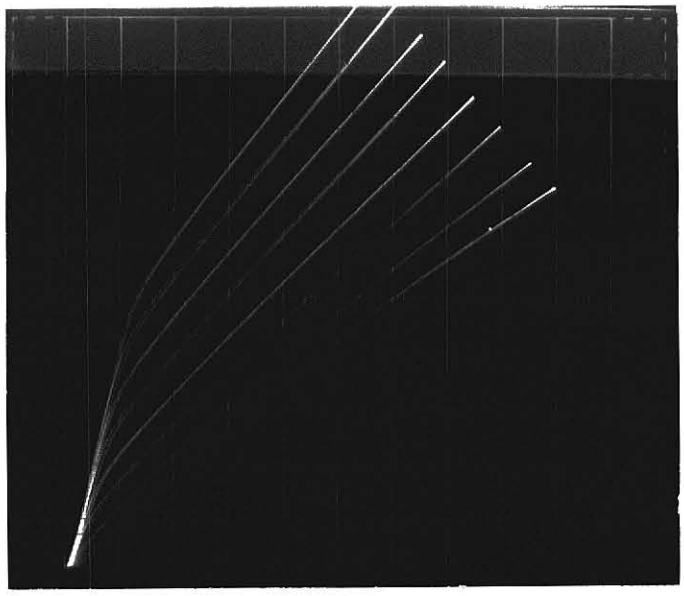


VERT: 500μA/div

HOR: 500mV/div

BASE: 500μA/step

Forward Characteristics



VERT: 500μA/div

HOR: 500mV/div

BASE: 2μA/step

Reverse Characteristics

Figure 8-4. Transistor Characteristics Showing Inversion Channelling

It was considered likely that this leakage could be caused by the formation of an inversion layer in the surface of the p-epilayer, effectively providing a resistive path between collector and emitter of this transistor.

No success was obtained with attempts to get the 'D' flip-flop circuit to operate.

A further series of fabrications were made with the process modified to reduce the liklihood of an inversion layer being formed. This was done by making an initial unmasked p-type diffusion into the wafer surface, with the objective of increasing the doping in the p-epilayer. This would greatly reduce the possibility of inversion layer formation.

The diffusion source used for the p-type diffusion was Borosilicafilm II (Emulsitone Co.). This was applied by spinning at 3000 rpm, followed by a 15 minute predeposit diffusion at 950°C. Drive in diffusion occurred during the oxidation step which followed, and the first n-diffusion step.

The dopant was designed to give a surface concentration of $5 \times 10^{19} cm^{-3}$, while the background concentration in the p-epilayer was $4 \times 10^{15} cm^{-3}$. The diffusion coefficient for boron at 950°C is $5.6 \times 10^{-15} cm^2/sec$. Following the standard infinite source diffusion calculation, this leads to a junction depth of 0.11μ.

The number of impurity atoms predeposited per unit area is given by

$$\frac{Q}{A} = \frac{2N_o}{\sqrt{\pi}} \cdot \sqrt{Dt}$$

Substituting the above values gives a density of 1.13×10^{14} atoms/cm^2.

The total drive-in cycle is that given by the initial oxidation

step plus that given by the first n-diffusion

$$Dt = D_1 t_1 + D_2 t_2$$
$$= (1.44 \times 10^{-14} \times 120 \times 60) + (4.72 \times 10^{-14} \times 92 \times 60)$$
$$= 3.64 \times 10^{-10} \text{ cm}^2$$

diffusion depth

$$x = 2\sqrt{Dt \cdot \ln \frac{Q/A}{N_x \sqrt{\pi Dt}}}$$

Substituting in this expression gives

$$x = 0.99\mu$$

The impurity concentration at the wafer surface after completion of the drive-in is

$$N_o = \frac{Q}{\sqrt{\pi Dt}} = 3.3 \times 10^{18} \text{ cm}^{-3}$$

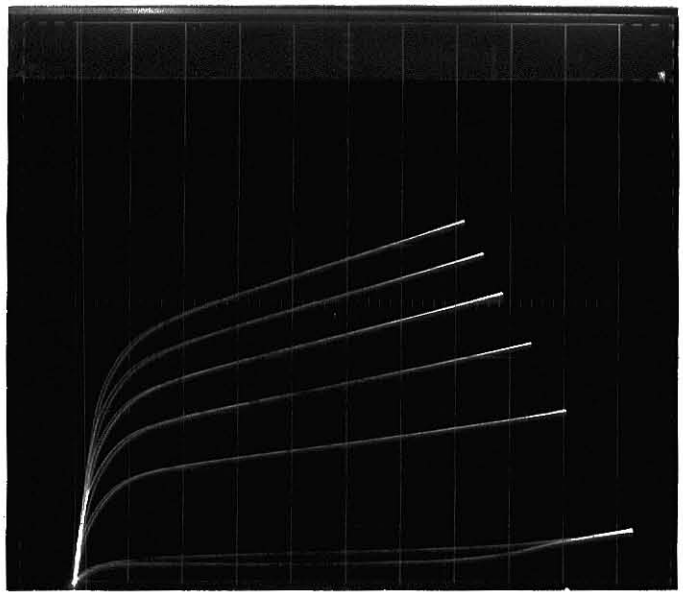
After the boron predeposit step, remaining diffusion source material on the wafer surface was stripped by immersing the wafer in HF for 1 minute. This was followed by a hot mixed acid step and thorough rinsing in dionized water. Processing of the wafer then proceeded exactly as for the previous wafer, with the first n-diffusion being of 72 minutes at 1050°C.

Tests on these circuits showed that good diode characteristics were still obtained from the base-collector and base-E_n diodes, though the reverse breakdown voltage had reduced to the range 15-20 volts.

The E_p-E_n junction still gave very poor characteristics, and the p-n-p injection transistor could not be made to show transistor behaviour.

The 'D' flip-flop still could not be made to function, even though a very wide range of injection currents, and illumination, were tried.

It was concluded that for some reason, either the injector emitter

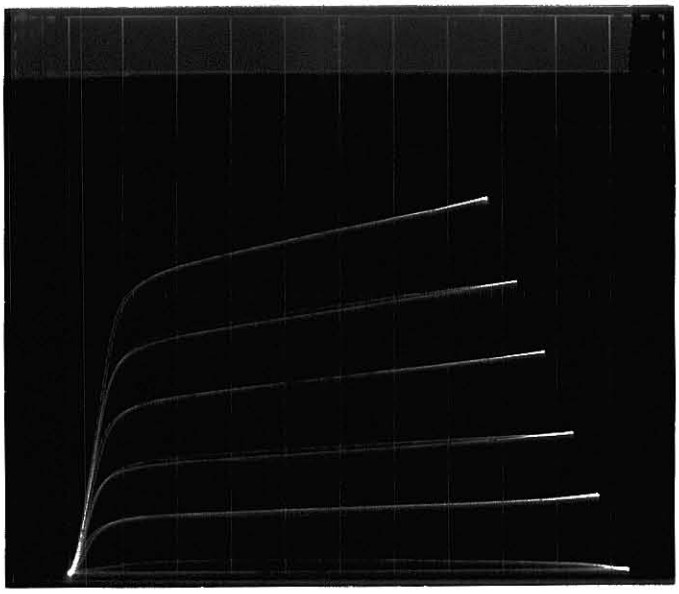


VERT: 50μA/div

HOR: 500mV/div

BASE: 20μA/step

Forward Characteristics



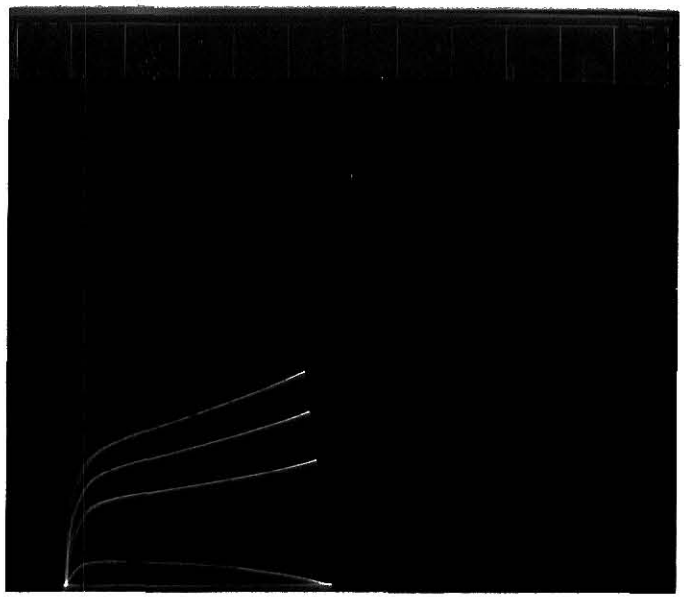
VERT: 200μA/div

HOR: 500mV/div

BASE: 2μA/step

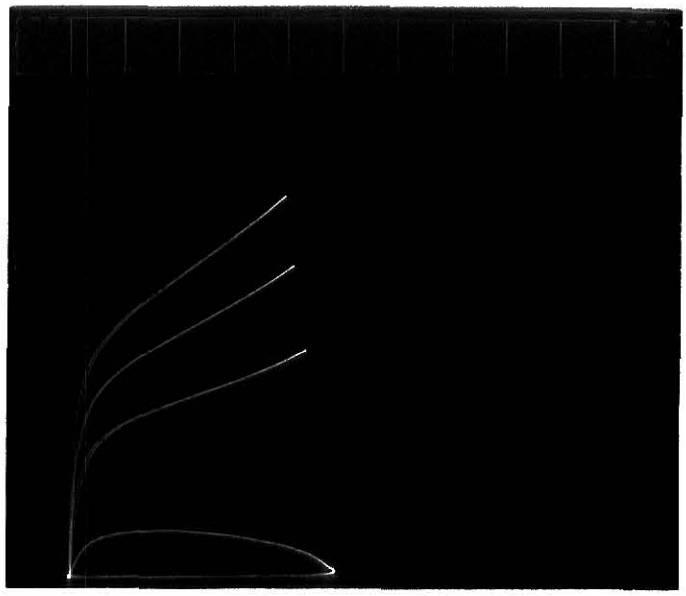
Reverse Characteristics

Figure 8-5. Transistor Characteristics



VERT: 50μA/div
HOR: 1V/div
BASE: 10μA/step

Single Collector Region Connected



VERT: 50μA/div
HOR: 1V/div
BASE: 10μA/step

Two collectors Connected Together

Figure 8-6. Dependence of Transistor Gain on Collector Area

efficiency or the base transport factor (or both) of the p-n-p transistor is very low, and very few carriers are being injected into the base regions of the n-p-n switching transistors. These transistors are thus not being turned on, and so cannot operate in the I^2L mode.

The n-p-n transistor treated as a conventional transistor showed very good characteristics in both the forward and reverse modes, as shown in Figure 8-5. Inversion channelling is no longer present, so evidently the boron diffusion was successful at overcoming this problem. Though its leakage is a little high, it gives a β of about 5 or 6 per collector in the forward mode, which is comparable to what other workers have obtained (30). The curve-tracer photographs in Figure 8-6 show how the β is directly dependent on collector area. By coupling two collectors together, approximately twice the current gain is obtained.

This transistor when operated in the inverse mode shows very good characteristics, with a β of about 150.

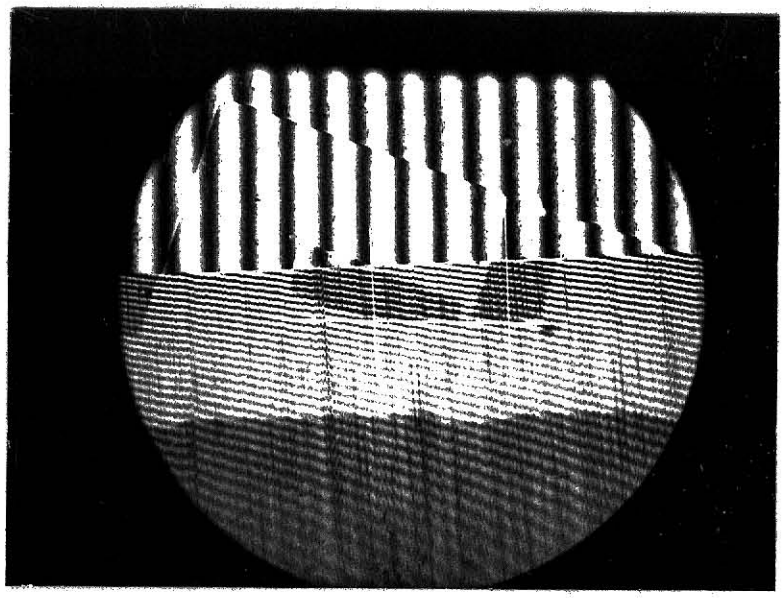
Because the n-p-n switching transistors built work well in both the forward and reverse modes, it is felt that failure of the I^2L flip-flop to work is related not to them, but rather to the very poor characteristics of the p-n-p injection transistor.

8.4 Evaluation of Wafer

In view of the unexpected nature of some of the results obtained, particularly those relating to the poor characteristics of the junction between the substrate and n-epilayer, assistance was sought on evaluation of the wafers supplied. Detailed testing of these was beyond the capabilities of the equipment available in the K.S.U. laboratory.

Evaluation of the wafers was undertaken by Mr R. Brockman of Delco

Grooved and Stained Wafer
(p-regions appear dark)



Same specimen with interference
fringes for junction depth measurement

Figure 8-7. Junction Depth Measurement by Grooving and Staining

Electronics. Several significant points emerged from his investigation.

The characteristics of the epilayers differed significantly from their specification. The p-epilayer was much thinner than the 3.8μ specified. By grooving and staining (similar to the technique discussed in section 5.3) the p-epilayer thickness was measured as 1.9μ. One of the specimens used for this measurement is shown in Figure 8-7. An optical interference technique was used for the depth measurement, rather than calculation based on the geometry of the specimen.

The results of a spreading resistance measurement are shown in Figure 8-8. This technique enables a resistivity profile of the wafer to be constructed. The p and n regions are not differentiated, but the junctions are shown as a point of inflection. By this method, the p-epilayer thickness is measured as 1.5μ. Another aspect of the p-epilayer shown by this test is that severe autodoping is evident. (Autodoping is undesired doping of an epilayer which occurs when the epilayer is being deposited, due to diffusion up from the layer on which the epilayer is being grown.) While the resistivity of the p-epilayer was specified as 3.4 ohm-cm, in fact its resistivity is dropping steadily from the epilayer boundary, but reaches only 20 ohm-cm at the wafer surface. The effect of such a graded and very thin epilayer is hard to assess, but it can be safely assumed that this characteristic is undesirable for the intended application. The very thin p-epilayer explains, of course, why the first diffusion needed to be much shorter than expected from calculation.

The n-epilayer corresponds reasonably to its specified thickness, but its resistivity is 0.35 ohm-cm, rather than the 0.09 ohm-cm specified. Some autodoping is evident in the n-epilayer, but no more

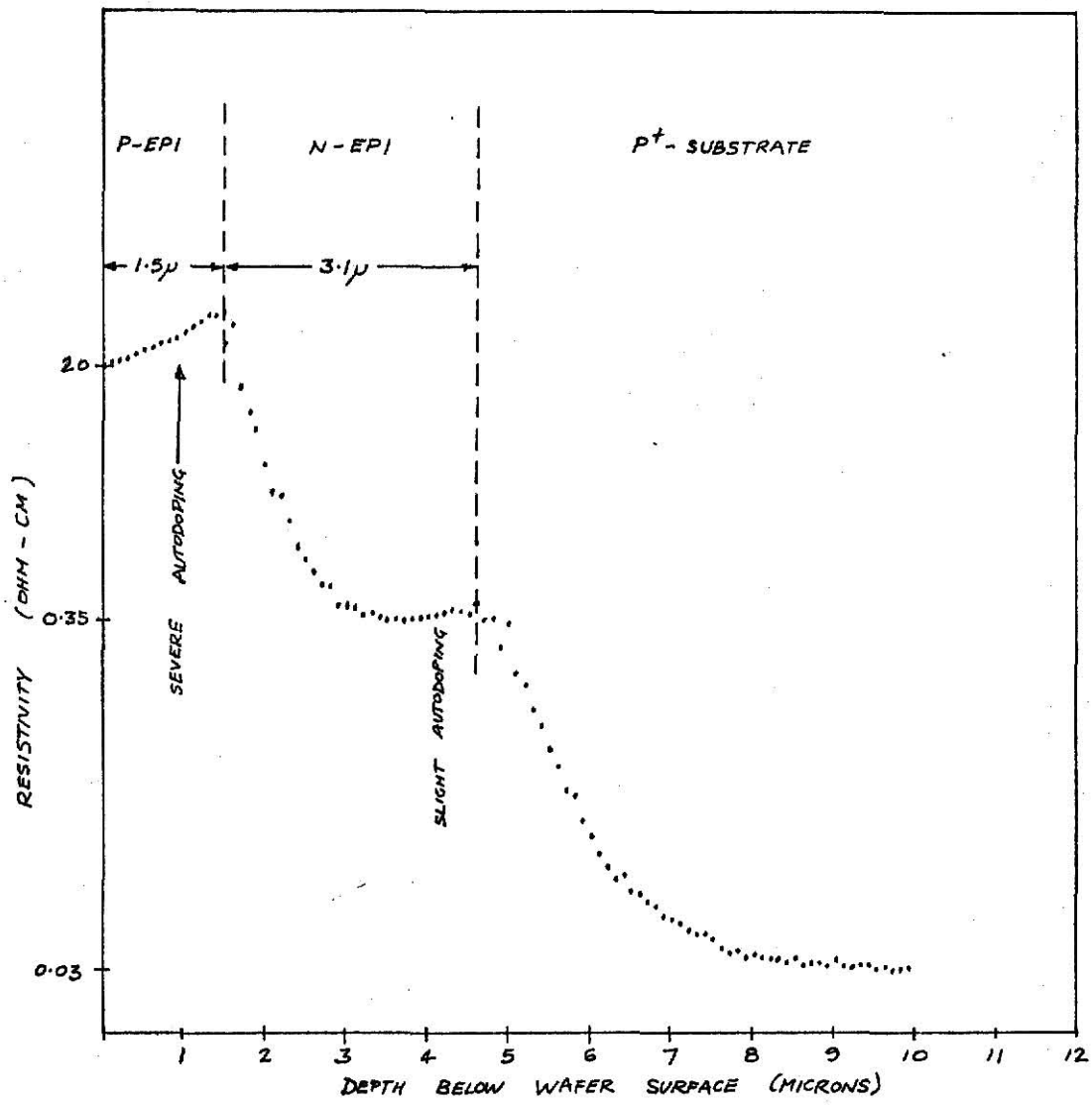


Figure 8-8. Spreading Resistance Profile of Wafer

than might be reasonably expected.

The poor characteristics of the substrate to n-epilayer junction were confirmed, but the reason for them was not determined. The possibility of crystal damage exists, but could not be confirmed.

A specimen on which the deep first diffusion had been made was examined. This specimen showed damage to the crystal structure at the

surface caused by excessive phosphorus doping. This damage is shown in Figure 8-9, enhanced by Sirtl etching (43) and the use of interference

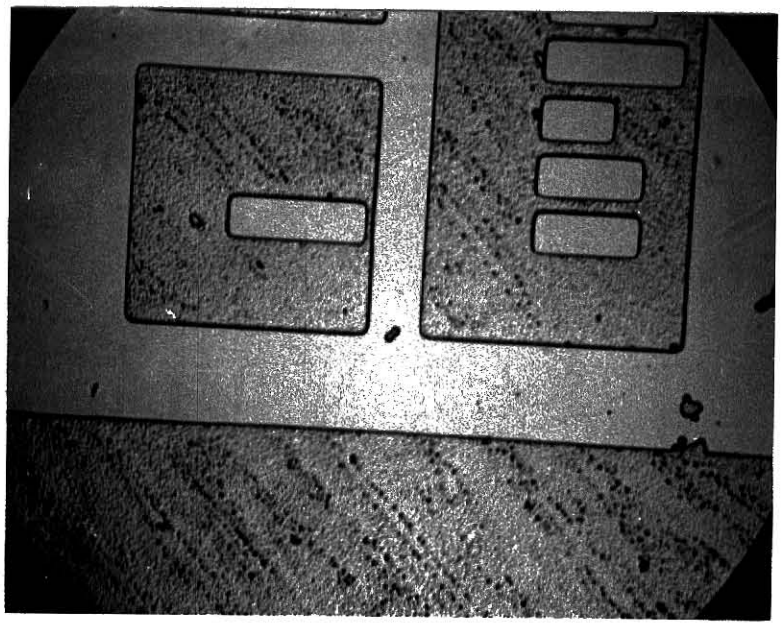


Figure 8-9. Phosphorus Damage on Diffused Wafer

contrast microscopy. While the damage could affect surface characteristics, it is not considered at all likely that the damage would extend down far enough to influence the behavior of the substrate to n-epilayer junction.

8.5 Conclusions

From this research project a great deal of experience was obtained of the techniques and problems involved in integrated circuit fabrication, and it was possible to make detailed recommendations on all of the

design and fabrication techniques used. The failure of the 'D' flip-flop circuit to work was disappointing, but hardly surprising in view of the poor characteristics of the wafers supplied.

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AN INVESTIGATION OF

INTEGRATED INJECTION LOGIC

by

PETER JOHN CONNOR

B.Sc., University of Auckland, New Zealand, 1966
B.E., University of Auckland, New Zealand, 1969

AN ABSTRACT OF A MASTER'S THESIS

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Manhattan, Kansas

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ABSTRACT

A review of the design theory and fabrication technology of Integrated Injection Logic (I^2L), and a detailed description of the design and fabrication of an I^2L 'D' flip-flop are presented. Starting from a wafer supplied complete with deposited epitaxial layers, all processes involved in fabricating I^2L circuits were studied in depth. The processing and equipment requirements were kept as simple as possible, and detailed processing recommendations are included. Results of experimental investigations into the oxidation, photolithography, diffusion and metallization processes are discussed in considerable detail, together with the results of the attempt to fabricate the 'D' flip-flop.