Corrective schemes for internal and external abnormalities in cascaded multilevel inverters

by

Jacob Lamb

B.S., Northern Arizona University, 2013
B.S.E., Northern Arizona University, 2013

AN ABSTRACT OF A DISSERTATION

submitted in partial fulfillment of the requirements for the degree

DOCTOR OF PHILOSOPHY

Department of Electrical and Computer Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2017

Abstract

Corrective schemes for facilitating continued operation of dc-ac converters during internal and external abnormalities are presented in this dissertation. While some of the developed techniques are suited for any dc-ac converter topology, most of the presented methodologies are designed specifically for cascaded H-bridge (CHB) multilevel converters. While CHB provide increased scalability and efficiency compared to traditional topologies, these converters are more likely to experience internal faults due to the additional components required. Realizing the full potential of CHB converters requires fault tolerant techniques, such as those demonstrated in this dissertation. Adaptive sinusoidal pulse width modulation (ASPWM) is introduced in this dissertation as a method which enables CHB to directly utilize time-variant dc sources, increasing CHB flexibility when compared to traditional pulse width modulation (PWM) methods which require dc sources with equal magnitudes or with magnitudes existing in specific ratios. Two alternative algorithms are presented to enable ASPWM implementation, providing a trade off between system performance and required sensor circuitry. This dissertation also introduces a load independent analytical approach for identifying discordant operating points, i.e. operating points where some cells in an asymmetric CHB leg regenerate power while the overall leg delivers power, or vice-versa. Identification of these points is essential due to the deleterious effects which can result from extended discordant operation, for instance overcharging of batteries leading to lifespan degrada-

tion or even catastrophic failures such as fires or explosions. Additionally, a method for rapidly identifying, isolating, and verifying internal IGBT open-circuit and gate-driver faults is presented in this dissertation to address the increased probability of switch failures occurring within CHB. The proposed approach enables converter operation to continue in the event of gate-driver or open-circuit faults, but avoids unnecessary converter reconfiguration due to gate-misfiring faults. For a CHB leg with M cells, the proposed technique identifies and isolates open-circuit switch faults in less than $2M$ measurement (sampling) cycles, and verification is completed in less than one full fundamental cycle. Furthermore, this dissertation introduces a real-time implementable atypical PWM technique which enables increased dc bus utilization under a wide range of non-ideal operating conditions. While this approach is suitable for a wide range of converters operating under external abnormalities, for instance maximizing dc bus utilization for converters providing auxiliary services such as negative-sequence compensation, this approach also facilitates operation of CHB with faulty cells. The proposed method can be used with any control technique and any carrier-based PWM method, enabling its implementation in both symmetric and asymmetric CHB. In addition to these fault tolerant techniques, a novel approach for analyzing the active- and reactive-power deliverable by grid-interactive converters is proposed. This method facilitates performance comparisons for various converter configurations, simplifying the process for selecting filter components, dc bus voltages, and other system parameters. This analytical approach also enables converter performance to be analyzed during internal and external fault events, allowing assessment of converter robustness. The efficacy of the developed techniques are supported by MATLAB/Simulink simulations as well as experimental data obtained using a laboratory-scale cascaded H-bridge multilevel converter.

Corrective schemes for internal and external abnormalities in cascaded multilevel inverters

by

Jacob Lamb

B.S., Northern Arizona University, 2013
B.S.E., Northern Arizona University, 2013

A DISSERTATION

submitted in partial fulfillment of the requirements for the degree

DOCTOR OF PHILOSOPHY

Department of Electrical and Computer Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2017

Approved by:

Major Professor
Dr. Behrooz Mirafzal

Copyright

Abstract

Corrective schemes for facilitating continued operation of dc-ac converters during internal and external abnormalities are presented in this dissertation. While some of the developed techniques are suited for any dc-ac converter topology, most of the presented methodologies are designed specifically for cascaded H-bridge (CHB) multilevel converters. While CHB provide increased scalability and efficiency compared to traditional topologies, these converters are more likely to experience internal faults due to the additional components required. Realizing the full potential of CHB converters requires fault tolerant techniques, such as those demonstrated in this dissertation. Adaptive sinusoidal pulse width modulation (ASPWM) is introduced in this dissertation as a method which enables CHB to directly utilize time-variant dc sources, increasing CHB flexibility when compared to traditional pulse width modulation (PWM) methods which require dc sources with equal magnitudes or with magnitudes existing in specific ratios. Two alternative algorithms are presented to enable ASPWM implementation, providing a trade off between system performance and required sensor circuitry. This dissertation also introduces a load independent analytical approach for identifying discordant operating points, i.e. operating points where some cells in an asymmetric CHB leg regenerate power while the overall leg delivers power, or vice-versa. Identification of these points is essential due to the deleterious effects which can result from extended discordant operation, for instance overcharging of batteries leading to lifespan degrada-

tion or even catastrophic failures such as fires or explosions. Additionally, a method for rapidly identifying, isolating, and verifying internal IGBT open-circuit and gate-driver faults is presented in this dissertation to address the increased probability of switch failures occurring within CHB. The proposed approach enables converter operation to continue in the event of gate-driver or open-circuit faults, but avoids unnecessary converter reconfiguration due to gate-misfiring faults. For a CHB leg with M cells, the proposed technique identifies and isolates open-circuit switch faults in less than $2M$ measurement (sampling) cycles, and verification is completed in less than one full fundamental cycle. Furthermore, this dissertation introduces a real-time implementable atypical PWM technique which enables increased dc bus utilization under a wide range of non-ideal operating conditions. While this approach is suitable for a wide range of converters operating under external abnormalities, for instance maximizing dc bus utilization for converters providing auxiliary services such as negative-sequence compensation, this approach also facilitates operation of CHB with faulty cells. The proposed method can be used with any control technique and any carrier-based PWM method, enabling its implementation in both symmetric and asymmetric CHB. In addition to these fault tolerant techniques, a novel approach for analyzing the active- and reactive-power deliverable by grid-interactive converters is proposed. This method facilitates performance comparisons for various converter configurations, simplifying the process for selecting filter components, dc bus voltages, and other system parameters. This analytical approach also enables converter performance to be analyzed during internal and external fault events, allowing assessment of converter robustness. The efficacy of the developed techniques are supported by MATLAB/Simulink simulations as well as experimental data obtained using a laboratory-scale cascaded H-bridge multilevel converter.

Table of Contents

List of Figures

List of Tables

Acknowledgments

First, I would like to thank my parents and my brothers for their encouragement during my studies. This dissertation would not exist without their support.

A big thanks to my advisor Dr. Behrooz Mirafzal. My experience as a graduate student would have been very different without his guidance, and the insight he provided has undoubtedly made me a better researcher. Also, I don't know how he is able to see the difference between font sizes or tell when letters appear pixelated, but my work would be much less visually appealing without his hawk-like vision.

I'd like to extend my gratitude to Dr. Dwight Day, Dr. Anil Pahwa, and Dr. Suresh Gopalakrishnan for the constructive input they all provided as members of my supervisory committee.

A tremendous thanks to Steve Booth for all of the insight he provided while I was building my converter, as well as for helping to improve my gardening capabilities by sharing his extensive horticultural knowledge.

My time in Manhattan would not have been as enjoyable without Mr. Aswad Adib's considerable abilities and professional attire, Mr. Joseph Benzaquen's insight and recognition of the mafia with which we've all become acquainted, or Mr. Mohsen Pilehvar's extremely thorough and extremely silent editing services. Additionally, I suppose I should also extend my gratitude to my *former* lab mate Dr. Akanksha Singh, even though she abandoned the lab and took her exceptional capabilities with

her. I appreciate the thought they have all given to my often pointless questions, as well as the enthusiasm of everyone's periodic rants against certain word processing software and laboratory equipment.

Finally, none of this would have been possible without the unconditional love and support of my wife, Caitlin. Because of everything she has done, she doesn't have to read the rest of this dissertation.

Dedication

To Caitlin, of course.

Chapter 1

Introduction

The foundations of this dissertation, which introduces corrective schemes for internal and external abnormalities in cascaded multilevel converters, are laid in this introductory chapter. The motivation and objectives of the research presented herein are detailed in Section 1.1, and a literature review is presented in Section 1.2 to introduce relevant state-of-the-art fault tolerant techniques. The contributions of this dissertation are presented in Section 1.3, and Section 1.4 concludes this chapter with an outline of this dissertation's organization.

1.1 Motivation and Objectives

Solid-state based dc-ac power converters are ubiquitous, essential for the efficient generation and utilization of electrical energy. These converters are utilized in everything from traction vehicles to manufacturing facilities to traditional and renewable energy generators and, given the diverse range of applications, ensuring their functionality is paramount [1–16]. At a minimum, converter failure is an inconvenience often necessitating costly repairs [4, 14–17], and in critical applications converter failures can

be hazardous. For instance, a converter failure occurring in a transportation vehicle during operation can adversely affect vehicle stability, thereby endangering passengers [4, 12, 14, 17]. As such, ensuring the reliable operation of converters, though the introduction of fault tolerant hardware and control, has become an important goal for the electrical engineering community [1–7, 10–23]. This dissertation continues pursuing this goal of increased reliability, with a focus on identifying and resolving abnormal operating conditions encountered by a particular dc-ac power converter topology.

Traditionally, three-phase dc-ac converters utilized in industry have a two-level line-to-neutral voltage output. The three legs of a traditional two-level voltage source inverter (2L-VSI) each require two solid-state switches, such as IGBTs with anti-parallel diodes, as shown in Fig. 1.1. This minimalistic topology provides few opportunities for enabling fault tolerant operation, with continued post-fault operation achieved for instance through the utilization of redundant converter legs [24–26]. Due to the limited options for implementing fault tolerance in 2L-VSI, alternative converter topologies may be preferred when continued converter operation is essential. In particular, a relatively new class of converter topologies, called multilevel converters, have the potential to be used for fault tolerant applications.

Multilevel topologies have several advantages compared with traditional two-level converters, such as high efficiency due to lower switching frequencies and low electromagnetic emission due to low dv/dt [1–7, 16, 18–20, 27–29]. Several multilevel topologies

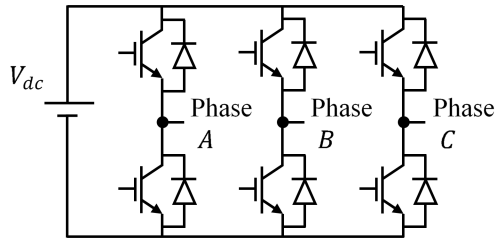


Fig. 1.1: Conventional three-phase, two-level voltage source inverter topology.

exist [1, 4, 5, 16, 24, 27, 29–32], but three of the most established are the neutral point clamped, the flying capacitor, and the cascaded H-bridge (CHB) multilevel converters [3–7, 16, 18–20, 24, 27, 29, 32, 33]. The CHB topology, as shown in Fig. 1.2, has been identified as particularly promising for medium-voltage, high-power applications due in part to its inherent modularity and fault tolerance [3, 16, 24, 29, 34–37]. As such, this dissertation focuses on the CHB multilevel converter, which has been implemented and proposed for use in a wide range of applications, including active filters, renewable energy conversion systems, and traction motor applications [3–5, 8, 9, 16, 29, 35, 36, 38].

Despite the benefits offered by the CHB converter, this topology requires many more switches and input sources than traditional 2L-VSI. These additional components increase the probability for internal fault events and other abnormal operating conditions, and the CHB's complexity increases the difficulty of isolating internal abnormalities. In addition to these internal abnormalities, application specific external nonidealities should also be accounted for when considering converter fault tolerance. However, due to the wide range of internal and external abnormalities which can occur during CHB

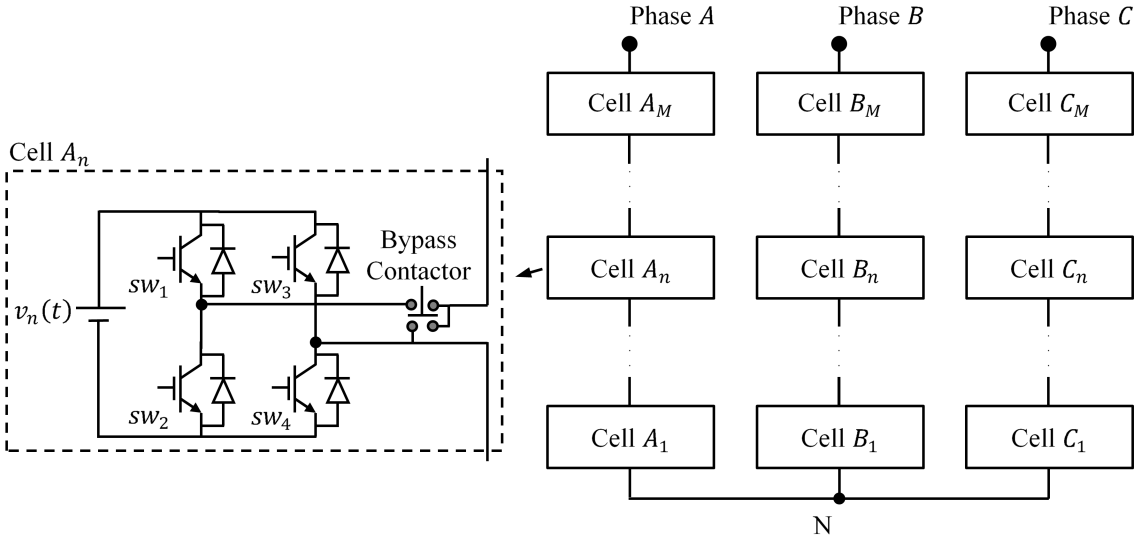


Fig. 1.2: Three-phase cascaded H-bridge multilevel topology with M cells per leg.

operation, it is not feasible to address all non-ideal operating conditions in one work. As such, the internal and external abnormalities investigated in this dissertation, outlined in the following subsections, were selected based on topology specific needs, i.e. the additional switches and sources required, as well as the promising prospective of using CHB to provide power in microgrid systems.

1.1.1 Switch Faults

Solid-state semiconductor switches are known to be one of the most vulnerable parts of a power converter [4, 13–15, 17, 21, 23, 39–41]. Compared to traditional two-level voltage source inverters which utilize six switches, the probability of an IGBT fault is increased when using CHB converters due to the high number of semiconductor switches these topologies require [2, 4, 8, 19, 20, 24, 41]. These additional switches make the CHB topology inherently reconfigurable, however, allowing continued converter operation in the event of one or more faults [2–4, 24, 42].

Thermomechanical fatigue is the main cause of IGBT failures [15, 18, 21, 39], and due to the inherent power and thermal cycling in some applications, e.g. electric vehicle motor drives [43], this thermomechanical fatigue is difficult to avoid. Switch failures can be roughly classified as open- or short-circuit faults [1, 13–15, 17, 24, 41, 44, 45]. Although short-circuit failures can cause nearly immediate damage to a CHB cell [13, 14, 17, 20, 22, 41], the dangers of open-circuit faults cannot be neglected as extended operation with open-circuit failures can cause extensive damage to an entire system [1, 6, 9, 13, 14, 17, 41, 46]. Ultimately, the probability and consequences of an open-circuit fault event, e.g. due to thermomechanical fatigue, are non-negligible and must be addressed [13, 14, 17, 41, 46].

1.1.2 Utilization of Time-Variant DC Source Inputs

The CHB topology is unique because it requires several isolated dc sources. While these sources may be obtained using phase shifting transformers in grid-tied applications [2, 4, 5, 16, 33], the CHB is particularly suited for applications where isolated sources are inherently available, such as in applications utilizing batteries [27–29,31,37,47–49]. Batteries, as would be used in an electric or hybrid electric vehicle application [27–29, 37,47,49,50] or a grid-tied energy storage application [31,37,48,51–53] are time-variant sources, since a battery's terminal voltage is dependent upon battery chemistry, state of charge, temperature, current magnitude, and other factors [50, 54–56]. This time-variance, combined with discrepancies in battery construction, unbalanced aging, or unequal discharging may cause input sources of a battery powered CHB to become unequal [37, 47, 49, 50, 57], negatively impacting the performance of typically utilized PWM schemes.

A further difficulty when using sources with unequal magnitudes in a CHB is that, under certain conditions, some sources receive an average regenerative power flow even when the overall converter is providing power [4, 33]. Note that a load-independent analytical method for identifying conditions which cause this discordant behavior is presented in this dissertation. Regardless, if a CHB cell source is a near fully charged battery, then an extended period of average regenerative power flow can lead to cell overcharging. This overcharging degrades the battery's cycle life and, depending on the battery chemistry, could cause battery overheating or a catastrophic failure such as ignition or explosion [47,50,57–59]. Nonetheless, the direct use of time-variant sources may be a desirable operating feature, depending on the application, and therefore the development of enabling methods is necessary.

1.1.3 Unbalanced Grid-Interactive Operation

In addition to stand-alone applications, cascaded H-bridge multilevel converters have a significant role as grid interfaces for renewable energy sources (RES) and battery energy sources (BES). This is particularly true in microgrids, which are seen as a key concept in smart-grid development [51,52,60]. Designed to operate in grid-connected and islanded modes [51–53, 60–63], microgrids are a holonic means of facilitating RES integration into the power grid [51–53,62,63]. In addition to RES, the utilization of which has been increasing due to a wide range of factors including renewable portfolio standards arising from growing concerns about global climate change [34, 64, 65], microgrids typically incorporate BES to provide operating reserves [31, 51–53, 61, 66], as well as traditional sources such as diesel generators [52, 61, 66]. Due to their utilization of independent sources, CHB converters are well suited to the interconnection of both BES and RES, particularly PV [29, 31, 34–36, 48, 51–53, 61, 66].

Irrespective of the input dc sources used, microgrid-interactive converters may be expected to provide auxiliary services, such as negative-sequence compensation [52, 60, 63], since harmonic- or negative-sequence currents drawn from traditional rotating generators can cause deleterious effects. This issue is particularly acute in microgrids, where smaller rotating generators can be used and loads may be unbalanced or contain nonlinear loads [52, 60, 63, 67]. When providing auxiliary services, however, converter reference waveforms required by carrier-based pulse width modulation (PWM) techniques may become distorted, i.e. nonsinusoidal, and unbalanced. Therefore, the maximum positive-sequence component of these waveforms must be reduced, since PWM references cannot exceed limits defined by a converter's dc bus voltages without causing overmodulation. Accordingly, the active- and reactive-power which a converter can supply are diminished when providing auxiliary services, and methods for maximizing dc bus utilization under these operating conditions must be developed.

1.2 Literature Review

In this section, a review of state-of-the-art fault tolerant approaches for addressing the challenges outlined in the Section 1.1 is presented.

1.2.1 Switch Faults

Identification and isolation of open-circuit faults can be approached using algorithmic solutions, whereas short-circuit protection is often provided by hardware solutions [11, 12,14,17,18,41], such as the desaturation [20] or di/dt feedback methods [22]. Hardware is used for short-circuit protection largely due to the speed that these faults must be detected and corrected, often cited as $10\,\mu s$, in order to prevent damage to the complementary switch within a leg [11, 14, 18, 24, 41]. Furthermore, industrial drives typically include short-circuit protection [13,18,41], whereas protection is not included as a standard feature for open-circuit faults [23]. Accordingly, there is still an industry need for further advancements which protect against open-circuit faults [23, 41], as presented in this dissertation, characterized by loss of IGBT control but continued operation of the faulty switch's anti-parallel diode [8, 12, 18]. Such faults are due, for instance, to wire bond liftoff or failure in gate-drive circuitry [6, 17, 18, 44]. These open-circuit faults create deleterious effects which can cause further system damage if no remedial action is taken [1, 6, 9, 13, 14, 18]. However, prior to any corrective reconfiguration, e.g. [8, 42], the fault location must be pinpointed [16, 19].

Various techniques for fault identification have been proposed [11, 12, 17, 18, 23, 24, 44], but are targeted toward implementation in two-level voltage source inverters and therefore do not aim to identify the exact location of a faulty switch in a multilevel converter. Other methods have been proposed for multilevel converters [6, 7, 13, 18, 19], but are not specifically intended for implementation in CHB converters.

One method designed for the identification of faulty switches in CHB multilevel converters is output voltage frequency analysis [8], where implementation requires a voltage sampling frequency $f_m = Mf_s$ for a CHB with M cells per phase and a pulse width modulation (PWM) switching frequency f_s. The sampling requirement precludes the use of lower sampling frequencies, e.g. if M or f_s are large, or higher sampling frequencies, e.g. if high-speed instrumentation is available.

Artificial intelligence based techniques, employing e.g. artificial neural networks and genetic algorithms [9], can also be used to identify faulty switches in multilevel converters. This approach requires significant computational effort [6, 12], as well as application specific data or expert knowledge for training.

Techniques in [1] are also suitable for fault identification in CHB multilevel converters. The proposed approach analyzes current flow deviations caused by improperly operating zero-states in CHB cells. This method requires a diagnosis time of M fundamental cycles for an M cell CHB.

The fault detection techniques presented in [1,8,9] require utilization of symmetric input sources and specific PWM methods, potentially limiting their applicability. As such, there is a need for an open-circuit fault-detection technique which: *(i)* can be applied to symmetric and asymmetric converters, *(ii)* is independent of the PWM scheme utilized, *(iii)* identifies faults quickly, and *(iv)* does not have a significant computational burden.

1.2.2 Maintaining Balanced Input Sources

The isolated input sources required by CHB can be inherently supplied by sources such as batteries, but the time-variant nature of these sources can cause undesirable complications. Accordingly, many of the developed techniques utilized to modulate CHB require sources with equal magnitudes [4,16,68,69]. If sources with unequal magnitudes

are used, the sources are assumed to be time-invariant with known magnitudes existing in specific ratios [4, 28, 68] or cells are required to switch at low frequencies [29, 49].

Since multilevel PWM methods typically cannot effectively utilize time-variant sources with unequal voltage magnitudes in CHB, many applications utilizing battery sources instead employ techniques intended to ensure the magnitudes of these sources stay equal. For instance, converter topologies have been proposed for their potential to be used to balance batteries voltages, such as the double-star connected converter proposed in [47] or the boost inverter topology presented in [70, 71]. These alternative topologies, however, can introduce further complications into systems. For instance, the topology proposed in [70, 71] requires the use of floating capacitors which necessitate complex balancing schemes [72]. Furthermore, the possibility of directly utilizing time-variant sources should be explored for the CHB topology, due to the other benefits of this converter as well as its wide range of applications.

In some systems, such as hybrid and electric vehicles, the time-variant nature of batteries can be resolved by using dc-dc converters to regulate the available dc voltage [37, 47, 70, 73]. While this approach may enable the utilization of CHB converters and traditional modulation schemes, the inductor required by the dc-dc converters naturally increases the weight, size, cost and loss of the overall system [47, 70, 73]. Further, extending this solution to a battery powered CHB would require a dc-dc converter for each cell, increasing control complexity and device component count. Accordingly, approaches which can directly utilize batteries directly are valuable.

Unbalanced cell voltages caused the time-variant nature of battery sources can be mitigated via the use of battery balancing methods. Passive, also called dissipative, balancing techniques act by discharging high voltage cells, for instance through a resistive load, until all cell voltages are equal. While inexpensive and simply implemented, passive approaches are rarely implemented due to their inefficiency and

slow operation [37, 47, 50, 74]. Active balancing methods are more attractive than passive solutions, operating for instance by transferring charge between cells using flying capacitors. These approaches are more efficient and provide balanced voltages more quickly than passive techniques, but they require additional components and control systems, thereby increasing system cost and introduce additional points of failure [29, 37, 47, 50, 74, 75]. Moreover, some balancing techniques require connections between dc sources, eliminating the isolation between sources required by CHB converters [29, 37, 50].

An alternative to battery balancing methods may provide a new path for utilizing time-variant sources. However, if sources are not balanced, then existing PWM techniques cannot be utilized without causing decreased system performance. Accordingly, a novel multilevel PWM technique must be developed to enable the direct utilization of time-variant dc sources.

1.2.3 Effective Utilization of DC Sources

Modulation strategies used to generate converter outputs often aim to maximize dc bus utilization, regardless of the converter topology being controlled. For three-phase, three-wire converters, maximal dc bus utilization requires line-to-neutral output voltages to contain a common-mode component, which can be added without affecting converter currents [8, 24, 31, 36, 48, 76–81]. Several techniques for creating appropriate common-mode components have been developed and are suitable for implementation in a wide range of converter topologies [42, 77–81]. One commonly implemented method for generating a common-mode line-to-neutral component is third-harmonic injection, an approach detailed in Chapter 2. Space vector PWM (SVPWM) and other PWM techniques can also be used to create common-mode components which maximize dc bus utilization. While these techniques can be utilized to modulate CHB, they were not

specifically designed for the modular CHB structure and therefore can only be directly applied under certain circumstances, for instance when all CHB cells are functioning properly, precluding their use in fault tolerant applications. Nonetheless, many techniques for maximizing dc bus utilization have been developed to facilitate continued CHB operation after internal fault events [8, 24, 77, 78].

One prominent method for enabling CHB operation under internal fault conditions is introduced in [77]. This technique enables balanced line-to-line voltages to be produced by adjusting the phase shifts between PWM references, with phase shift angles obtained by solving a system of transcendental equations. Ultimately this approach adds a fundamental frequency common-mode component, and is therefore referred to as fundamental phase shift compensation (FPSC). The FPSC method is extended in [8], improving the flexibility and allowing increased line-to-line voltages under specific fault conditions. Due to their ubiquity, the FPSC and extended FPSC methods are reviewed in Chapter 2. Nonetheless, the FPSC techniques proposed in [77] and [8] have been developed only for balanced operating conditions for implementation in grid-tied applications.

The FPSC technique has also been modified in [80] for implementation in SVPWM modulated converter. The method proposed in [80], however, requires at least two of the CHB phases to have an equal number of operative cells, necessitating healthy cells to be bypassed if this condition is not met. The authors of [80] also extended the FPSC technique to a different PWM strategy in [81], though the proposed method can only be implemented if one CHB cell is faulty. Moreover, implementation in unbalanced systems was not considered in either [80] or [81].

In [78], the set of common-mode components which ensure linear-modulation is determined, and the injected common-mode component is computed as the mean value of set elements. The process for obtaining a suitable common-mode component using this

approach is complex [26], and analysis presented in [78] only considered implementation in balanced systems.

While these techniques for maximizing dc bus utilization enable continued CHB converter operation after internal faults, analysis has only been presented for converters operating under balanced conditions. As such, there is still a need for a technique which can be be implemented during unbalanced operating conditions, for instance when a converter supplies auxiliary services such as negative-sequence compensation.

1.3 Contribution of Dissertation

Cascaded H-bridge multilevel converters are a promising topology for dc-ac conversion, but more work is needed to increase their reliability as well as their capacity to adequately operate during external non-idealities. This dissertation presents corrective schemes which enable continued CHB operation under internal and external abnormalities, with the following primary contributions:

- An analytical technique for identifying the active- and reactive-power which a grid-interactive converter can provide. This method enables a converter's operating region to be analyzed for varying converter parameters under nominal and abnormal conditions, facilitating the converter design process.

- A load-independent approach for identifying discordant operating conditions, i.e. conditions which cause some cells within a leg to provide power to other cells within a leg. Identifying the conditions which cause discordant operation is essential for determining whether hardware or control modifications are necessary to mitigate or eliminate this behavior.

- An atypical PWM technique for maximizing converter dc bus utilization. This

method can be implemented in real-time for a wide range of dc-ac converter topology operating under a ideal and abnormal conditions.

- Adaptive carrier-based PWM techniques which enable CHB to directly utilize time-variant sources. These methods adjust the amplitude and offset of carriers used for PWM generation, enabling symmetric output waveforms to be generated when cells utilize non-ideal inputs.

- A method for open-circuit IGBT fault detection in cascaded H-bridge (CHB) multilevel converters. Once potential fault locations have been identified using this approach, the fault location is systematically isolated and then verified, reducing the possibility of unnecessary corrective actions due to fault misidentification, e.g. an intermittent gate misfiring fault being classified as an open-circuit fault.

The efficacy of the developed techniques are supported by MATLAB/Simulink simulations as well as experimental data obtained using a laboratory-scale cascaded H-bridge multilevel converter.

1.4 Organization of Dissertation

The remainder of this dissertation is organized as follows:

An introduction to the cascaded H-bridge topology is provided in Chapter 2. Level-shifted and hybrid PWM, techniques typically utilized to generate gate signals for symmetric and asymmetric CHB, are also presented. Moreover fundamental phase shift compensation, a common approach for enabling CHB operation to continue after internal fault events, is reviewed.

An approach for identifying the operating region of grid-interactive CHB is presented in Chapter 3. The output region, defined by the linear modulation region and

the filter coupling the converter to the grid, is analyzed first. The converter's operational region, a subset of the converter's output region, is then identified, with restrictions imposed by component VA limits, THD limitations, and the requirement that active-power is delivered by the converter. Finally, an analytical technique is presented for identifying discordant operating points, where some cells in a CHB regenerate power while the leg delivers power, or vice-versa.

A technique for maximizing dc bus utilization is presented in Chapter 4. This technique, compatible with carrier-based PWM methods and all voltage source converter topologies, injects references with the minimum zero-sequence component required to enable linear modulation. This method does not rely upon synchronization of waveforms, as third-harmonic injection does, nor does it require the use of lookup tables, as fundamental phase-shift compensation does. Moreover, this technique is easy to implement, and can be used when converter supplies auxiliary services such as negative-sequence compensation.

In Chapter 5, adaptive algorithms are developed to modify level-shifted PWM to allow CHB to directly utilize time-variant dc sources. The sensor-per-source algorithm is able to immediately respond to varying input sources by utilizing M voltage sensors and a current sensor. The sensor-per-leg algorithm is presented next, enabling direct utilization of time-variant dc sources with a single sensor, though a recalculation period is required when cell voltages are changed.

A technique developed for open-circuit fault identification and isolation in CHB is presented in Chapter 6. First, the effects of uncorrected open-circuit faults are identified. Next, the foundation is laid for the technique for detecting open-circuit faults utilizing a single voltage and current sensor. Due to sensor placement, this technique is well suited to work in tandem with the sensor-per-leg algorithm presented in Chapter 5. However, this open-circuit fault identification technique is implemented

as a subroutine, making it compatible with any switching pattern.

Finally, a summary of the presented research and this dissertation's contribution to state-of-the-art converters is presented in Chapter 7. Suggestions for future work to increase converter flexibility are also proposed in this concluding chapter.

Chapter 2

The Cascaded H-Bridge Multilevel Converter

The cascaded H-bridge multilevel converter is the dc-ac converter topology at the center of many of the techniques presented in this dissertation, and therefore the working principles of this converter are foundational for the work presented in future chapters. To that end, an overview of the CHB is provided in this chapter, beginning with an introduction to the CHB topology in Section 2.1. The level-shifted and hybrid PWM techniques, as well as a method for improving dc bus utilization during healthy converter operation, are presented in Section 2.2. In Section 2.3, a technique for enabling fault tolerance in CHB is introduced.

2.1 System Topology

In this section, the symmetric and asymmetric CHB converter topologies are presented. Each CHB converter leg, as shown in Fig. 2.1 for a grid-interactive CHB, is used to generate a single electrical phase. Each leg consists of M series connected cells, or

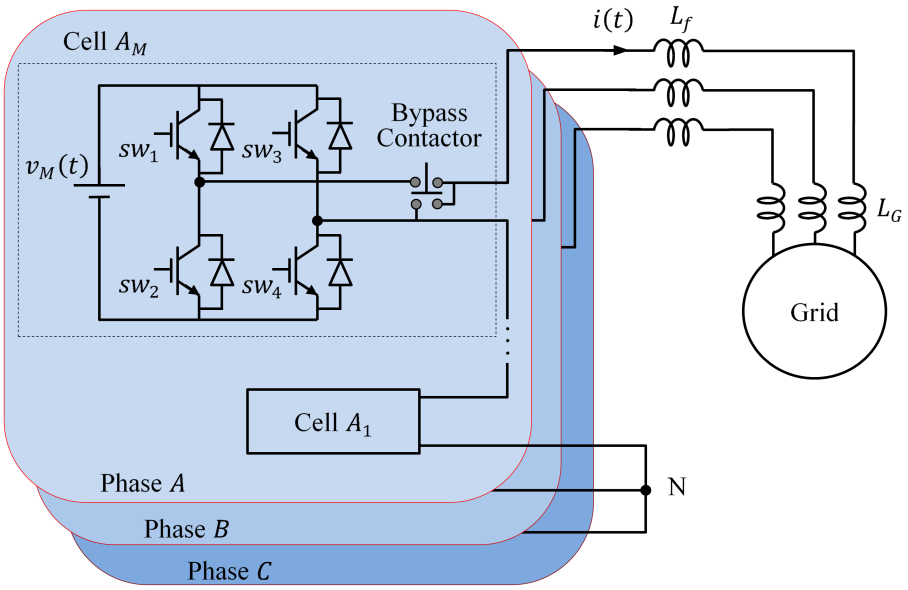


Fig. 2.1: A grid-interactive cascaded H-bridge multilevel converter.

modules, with each cell generally including: *(i)* an H-bridge configuration of four IGBTs with anti-parallel diodes, *(ii)* a bypass contactor used to completely bypass the cell, e.g. in the event of a fault [3, 24], and *(iii)* an isolated dc source input, such as batteries, fuel cells, or PV arrays. For PV applications, additional hardware is typically required in order to implement maximum power point tracking algorithms and to isolate the PV modules from the grid [35, 36, 64, 65].

For both grid-interactive and stand-alone CHB, passive filters are generally utilized to attenuate high frequency harmonics. The multilevel waveforms generated by CHB converters allow for the use of simpler inductive filters [34–36, 64, 65, 82], compared to the LCL filters typically used by traditional two-level inverters [82–84]. However, depending on the converter's switching frequency and the number of cells in each leg, utilization of an LCL filter may be advantageous. For grid-interactive CHB, system operators may also need consider the inherent grid impedance, Z_G, in addition to the impedance of the filtering impedance, Z_f. The magnitude of Z_G varies from one region

to the next, and can vary throughout the lifetime of an installed converter [83].

A CHB is said to be symmetric if all cell sources have equal magnitude, otherwise the CHB is asymmetric [3, 4, 33]. A symmetric CHB has many redundant switching states whereas an asymmetric CHB eliminates some or all redundant states to increase the number of unique voltage levels which the converter can generate [3–5]. Asymmetry may be intentionally introduced for a system [4], but it can also occur due to external factors. For instance, partial shading may cause asymmetry when using PV sources [34–36, 64, 65]. One difficulty when operating an asymmetric CHB is the existence of discordant output points, where power is transferred between cells within a leg, for instance causing one cell to have a net regenerative power flow when the overall converter leg is providing power [3, 4]. Depending on the input dc sources utilized by a CHB, discordant converter output points may be undesirable. For instance, if a CHB utilizes asymmetric batteries as input dc sources, then extended operation at a discordant output point can lead to battery overcharging even when the converter operates in motoring mode. The battery's cycle life can be negatively impacted by this overcharging and, depending on the battery chemistry, overcharging could even cause battery overheating or a catastrophic failure such as ignition or explosion [3, 47, 57].

A CHB leg's line-to-neutral voltage is equal to the sum of the output voltages of all cells within that leg, where cell A_n can be made to provide an output voltage of v_n, 0, or $-v_n$ by appropriately controlling switches sw_1, sw_2, sw_3, and sw_4 [3, 27]. Notation is simplified by noting that sw_1 and sw_2 act in a complimentary manner, as do sw_3 and sw_4, allowing the four available cell states to be uniquely identified according to the configuration of sw_1 and sw_3. The four allowable cell switch configurations each correspond to a unique cell state, $s_n(t)$, as shown in Table 2.1. With the exception of Chapter 6, the two zero cell states are treated interchangeably throughout this dissertation, i.e. $0_U = 0_L = 0$.

Table 2.1: Cell A_n Switch Configurations, Output Voltages, and States

$[sw_1, sw_3]$	Cell Output Voltage	Cell State $s_n(t)$
$[0, 0]$	0	0_L
$[0, 1]$	$-v_n(t)$	-1
$[1, 0]$	$v_n(t)$	1
$[1, 1]$	0	0_U

2.2 PWM Methods

A wide range of multilevel PWM techniques have been created to modulate the output of CHB converters. This section provides an overview of the two techniques used in this dissertation, level-shifted PWM (LSPWM), and hybrid PWM. Moreover, this section also introduces third-harmonic injection a commonly utilized method for modifying these PWM techniques to increase dc bus utilization. Numerous works, e.g. [4, 16, 33, 85–88], provide overviews of other multilevel PWM schemes, including space vector PWM [69, 80, 89], selective harmonic elimination PWM [90, 91], and selective harmonic mitigation PWM [92, 93].

2.2.1 Level-Shifted Pulse Width Modulation

Level-shifted PWM for multilevel converters is one of the natural extensions of sinusoidal PWM, a carrier-based technique commonly used for two-level converters. For this method, and all carrier-based PWM schemes, gate signals for cells in each leg are generated by comparing carrier (triangular) waveforms and a reference waveform. When used to modulate symmetric CHB, where $v_M(t) = V_{dc}\ \forall M$, two carriers are required for each CHB cell, as shown in Fig. 2.2 for a three-cell CHB.

When utilizing symmetric CHB, it is typically desirable to have each cell provide equal power provided by each cell. Accordingly, strategies to achieve even power distribution have been developed when using LSPWM to modulate CHB [88, 94, 95]. One

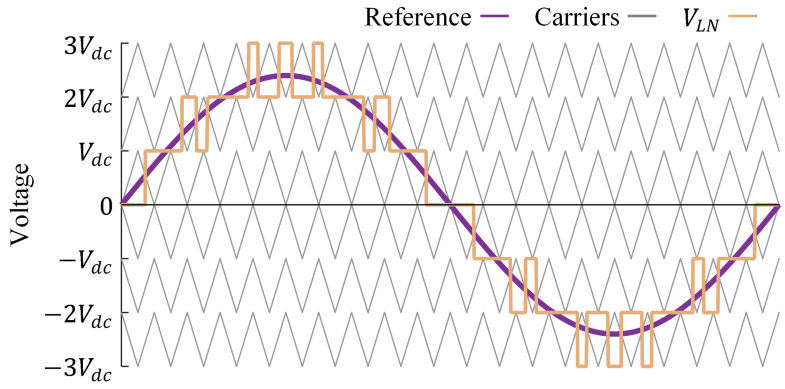


Fig. 2.2: Reference, carriers, and the unfiltered line-to-neutral output when using level-shifted PWM to modulate a symmetric three-cell CHB. Carriers are in the phase opposition disposition configuration.

such approach is the first-on, first-off strategy [3, 27–29, 96]. Using this method, cells in a CHB leg are switched in a rotating pattern using an ordered cyclic cell list with a turn-on and turn-off position. Initially the turn-on and turn-off position are the same, i.e. both markers are placed at cell x. When the magnitude of the leg's line-to-neutral output voltage is to be increased, the cell indicated by the turn-on marker is activated and the turn-on marker advances to the next cell in the cycle. Similarly, when the magnitude of the leg's line-to-neutral output voltage is to be decreased the cell indicated by the turn-off marker is deactivated and the turn-off marker advances to the next cell in the cycle.

The LSPWM method can be extended for use by asymmetric CHB by placing carriers between each attainable converter output [3, 96], as shown in Fig. 2.3 for a two-cell CHB with $v_2 > v_1 > v_2 - v_1$. This approach utilizes all available converter outputs, providing a waveform with more output levels than a symmetric CHB with an equivalent number of cells. However, cells may not deliver equal power using this modulation method, and switching between adjacent levels may require multiple cells to change their output state simultaneously.

When implementing LSPWM, carriers can be arranged in several configurations,

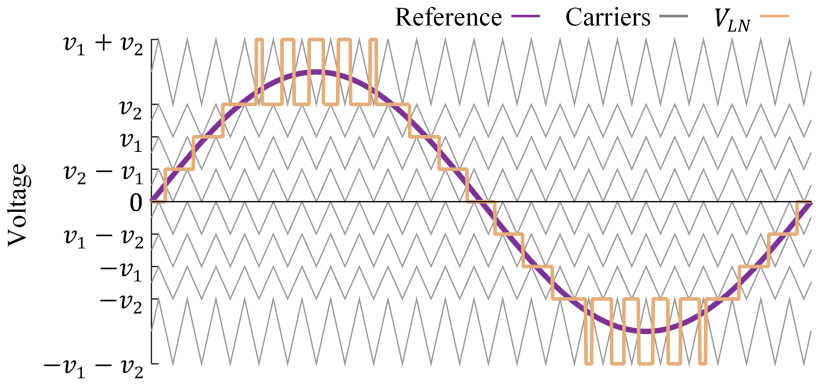


Fig. 2.3: Reference, carriers, and the unfilitered line-to-neutral output when using level-shifted PWM to modulate an asymmetric two-cell asymmetric CHB with $v_2 > v_1 > v_2 - v_1$. Carriers are in the phase disposition configuration.

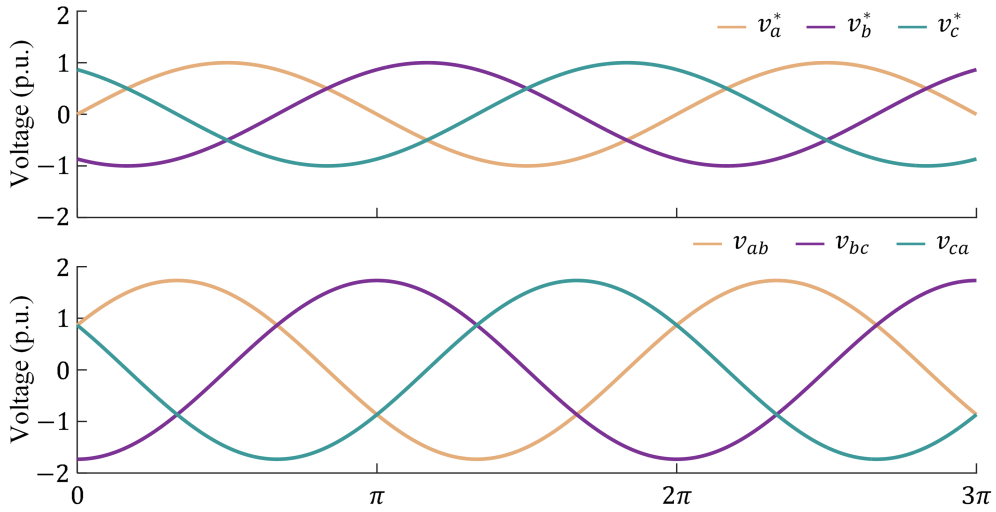


Fig. 2.4: Maximum references (top) and resulting ideal line-to-line voltages (bottom) when using purely sinusoidal references in a balanced three-phase system. Waveforms are normalized by the sum of dc bus voltages within a leg.

though there are only three commonly used arrangements [68, 97]. Carriers are in-phase for the phase disposition (PD) configuration; adjacent carriers are 180° out of phase for the alternative phase opposition disposition (APOD) configuration; and positive carriers are 180° out of phase with negative carriers for the phase opposition disposition (POD) method. Carriers shown in Fig. 2.2 are arranged according to the POD method, and carriers shown in Fig. 2.3 are in the PD configuration. While the

PD strategy is shown to produce a slightly improved harmonic profile in three-phase systems [68], the minor differences in high frequency content may be negligible due to the attenuation of high frequency content achieved using passive filtering techniques [4].

For carrier-based PWM methods such as LSPWM, reference waveforms define the ideal line-to-neutral voltage to be generated by a CHB leg, and therefore each leg requires its own reference waveform. A wide range of control schemes can be used to generate references, depending on system goals [4, 52, 85, 87, 98–102]. In order to be accurately recreated, PWM references cannot exceed the maximum voltage the CHB leg can produce. Accordingly, the magnitude of a leg's reference is typically less than or equal to the sum of the dc voltages within the leg, denoted as $V_{dc,x}$ for each $x \in \{a, b, c\}$. Equivalently, references normalized according to $V_{dc,x}$, denoted as v_x^*, typically have magnitudes less than or equal to one. Defining the modulation index, m, as the peak value of v_x^*, a converter is said to operate in the linear modulation region if $m \leq 1$. When using purely sinusoidal references in a balanced three-phase system, the normalized line-to-line peak voltage is $\sqrt{3}$ at the limit of the linear modulation region, i.e. when $m = 1$, as shown in Fig. 2.4.

A converter is said to operate in the overmodulation region if $m > 1$, and the line-to-neutral voltage waveforms generated during overmodulation can be distinctively flat for several switching cycles, as shown in Fig. 2.5. The flat regions of the voltages generated by an overmodulated converter introduce difficult-to-filter low order harmonics into a system. Accordingly, overmodulation behavior may be undesirable, particularly for grid-interactive inverters where regulations limit the maximum permissible waveform distortion [103]. However, overmodulation is utilized in some applications to increase the fundamental component of the waveform generated. For instance, the reference waveforms in Fig. 2.6 have a normalized magnitude of 1.25, and the resulting line-to-line voltages have a normalized fundamental component of 1.94, which is 12%

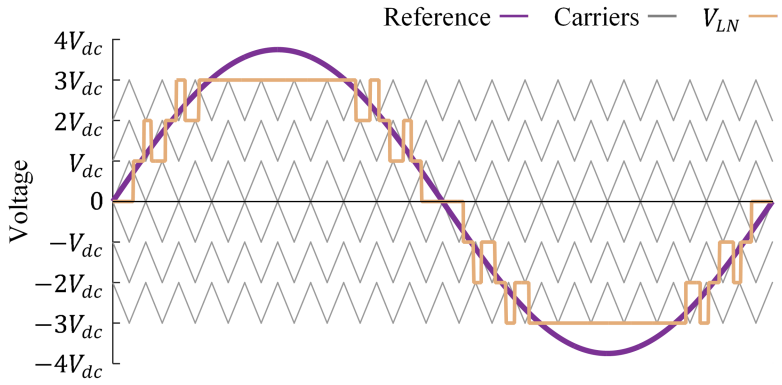


Fig. 2.5: Reference, carriers, and the unfilitered line-to-neutral output when using level-shifted PWM to modulate a symmetric three-cell CHB. Since the reference exceeds the maximum line-to-neutral output voltage, the converter is overmodulated.

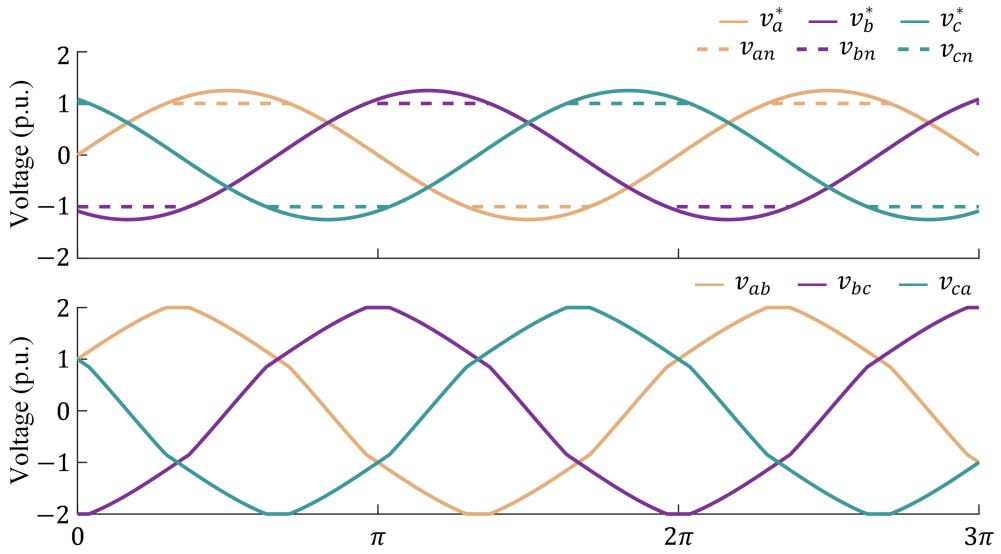


Fig. 2.6: Overmodulated references and ideal line-to-neutral voltages (top) as well as the resulting ideal line-to-line voltages (bottom) when using purely sinusoidal references in a balanced three-phase system. Waveforms are normalized by the sum of dc bus voltages within a leg.

greater than the maximum attainable voltage in the linear PWM region. However, the generated line-to-line voltages are distorted, as shown in Fig. 2.6. While the normalized reference waveforms in Fig. 2.6 have magnitudes greater than unity, the resulting ideal line-to-neutral voltages cannot exceed unity. For the maximum overmodulation case, the resulting line-to-line voltages have a normalized fundamental component of $4\sqrt{3}/\pi$,

a 27% increase over the maximum value obtained via linear modulation. Again, however, this boost comes with a cost, with significant harmonic content in the generated line-to-line voltage.

2.2.2 Reference Modifications

For Y-connected systems, such as the CHB in Fig. 2.1, there is no path for common-mode current, i.e. $i_a(t) + i_b(t) + i_c(t) = 0$, and line-to-neutral voltages can therefore contain a non-zero common-mode component without inducing current flow. Accordingly, the PWM references which define a converter's line-to-neutral voltages can be made to include a common-mode component, v_{cm}, often selected to increase a converter's linear PWM region, enabling line-to-line voltages generated by a converter to include a larger maximum fundamental component than would otherwise be possible for a given dc bus voltage. One of the most ubiquitous methods for increasing dc bus utilization is third-harmonic injection, an approach where v_{cm} is selected such that

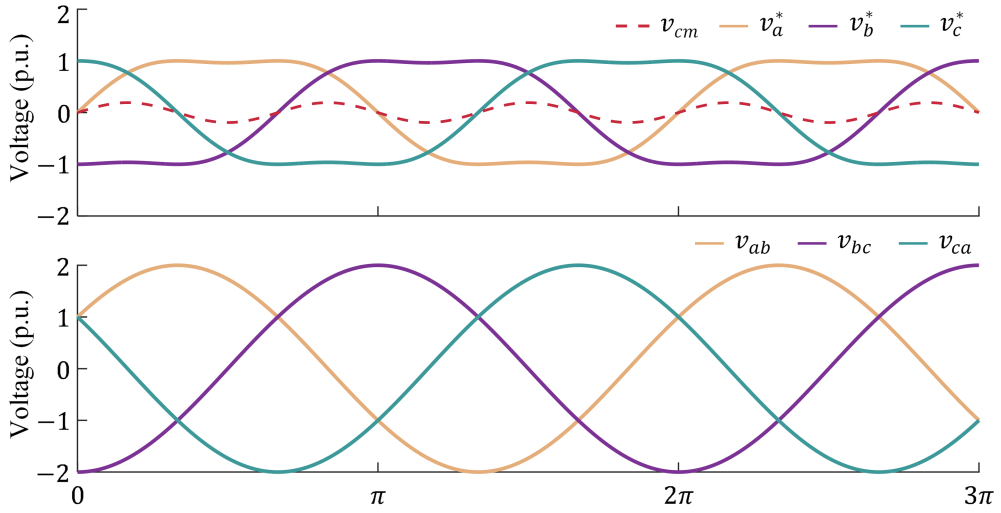


Fig. 2.7: References and common-mode component (top) and resulting ideal line-to-line voltages (bottom) when using third-harmonic injection in a balanced three-phase system. Waveforms are normalized by the sum of dc bus voltages within a leg.

references include a third harmonic component which reduces references' peak values. Since all line-to-neutral components are injected with the same third harmonic component, the third harmonic cancels when computing line-to-line voltages leaving only the fundamental component, as shown Fig. 2.7.

Define the fundamental modulation index, m_1, of leg x as the ratio of the fundamental component of the leg's reference, $v^*_{x,1}$, to the sum of dc voltages within a leg, $V_{dc,x}$. That is,

$$m_1 = \frac{v^*_{x,1}}{V_{dc,x}}.$$

Selecting v_{cm} to have approximately one-sixth the amplitude of the fundamental, the linear PWM region of a converter is increased from $m_1 = 1$, obtained when purely sinusoidal references are used, to $m_1 = 2/\sqrt{3}$, resulting in line-to-line peak voltages of $2MV_{dc}$. Overmodulation still occurs if m_1 is increased beyond $2/\sqrt{3}$ when using

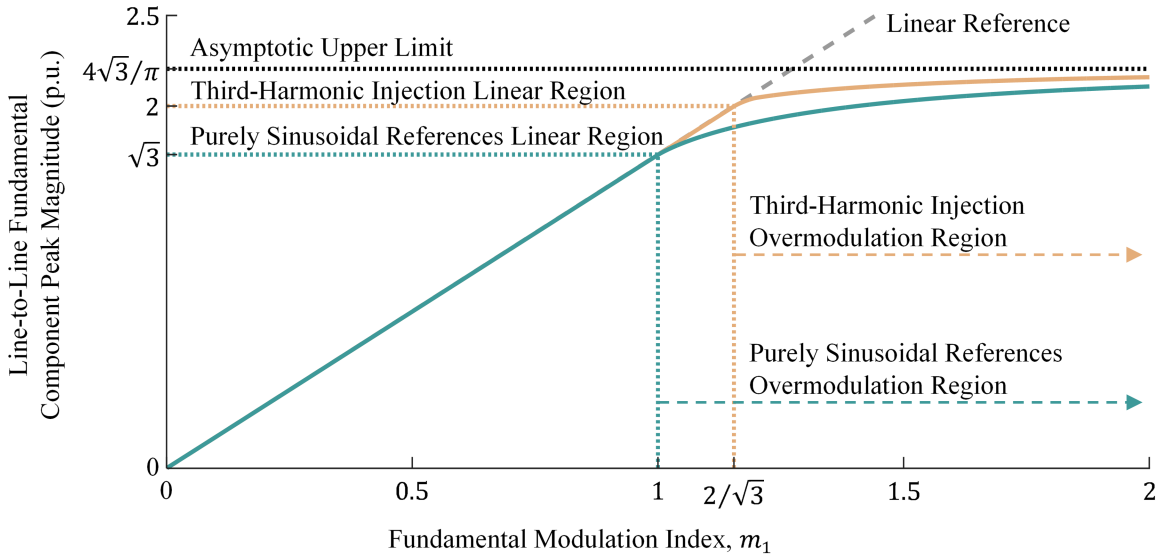


Fig. 2.8: Compared to purely sinusoidal references, the linear PWM range of a CHB is increased by utilizing third-harmonic injection. Regardless of the method utilized, operation in the overmodulation causes difficult to filter low order harmonics. Voltage magnitudes are normalized by the sum of dc bus voltages within a leg.

third-harmonic injection, but this approach increases the linear modulation region, as shown in Fig. 2.8, enabling more effective use of available dc bus voltages.

2.2.3 Hybrid Pulse Width Modulation

For asymmetric CHB with voltages in specific ratios, hybrid PWM is a carrier-based modulation technique which can be used as an alternative to LSPWM [4, 104]. Unlike LSPWM, hybrid PWM requires only the lowest voltage cell to switch at PWM frequencies, enabling other cells to switch more slowly. However, this technique can only be implemented if cell voltages specially related, with the maximum number of evenly spaced leg output voltages attainable if cell voltages are in a $[1 : 2 : 6 : ... : 2\Sigma(\text{previous voltages})]$ ratio. As shown in the block diagram in Fig. 2.9 for an asymmetric three-cell CHB leg with $v_3 > v_2 > v_1$, the output of each cell is determined by cell references which are defined by a leg reference as well as the output of any higher voltage cells within the leg. The leg reference and unfiltered line-to-neutral output, as well as individual cell references and outputs, are shown in Fig. 2.10 for a three-cell CHB with cell voltages in the $[1 : 2 : 6]$ ratio. Hybrid PWM is a carrier-based technique, even though only the lowest voltage cell is modulated using a carrier, and therefore third-harmonic injection

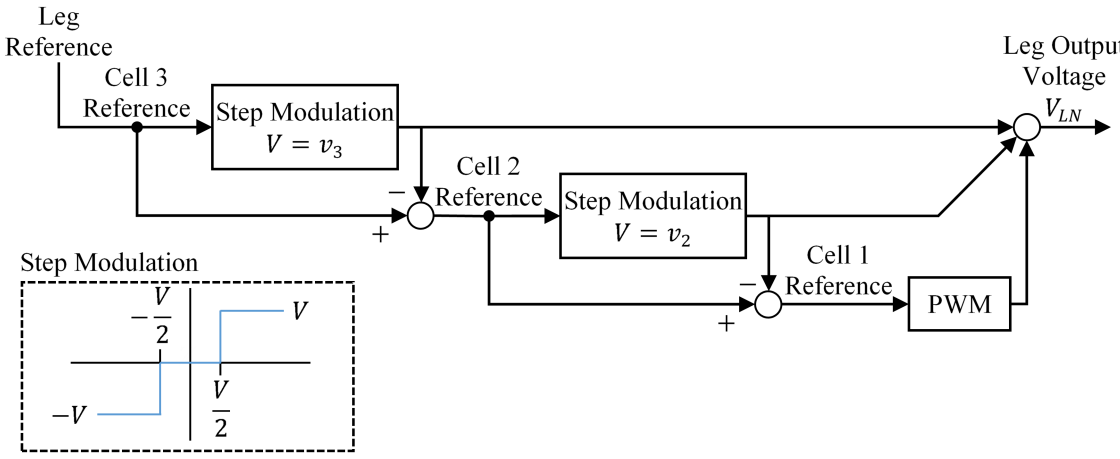


Fig. 2.9: Block diagram for implementing hybrid PWM in a three-cell CHB leg.

can still be utilized when hybrid PWM is used to modulate a three-phase converter.

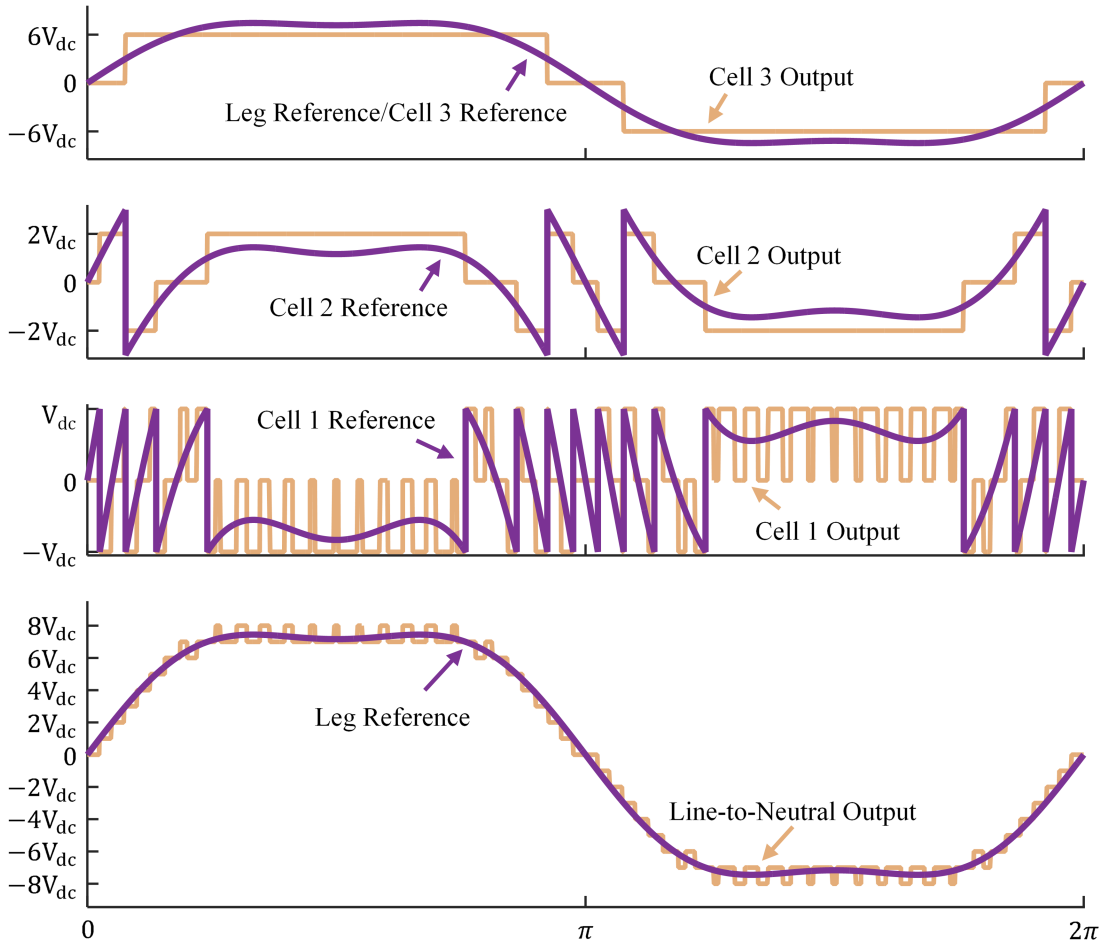


Fig. 2.10: Individual cell references and outputs, as well as the overall leg reference and unfilitered line-to-neutral output, when hybrid PWM is used to modulate a three-cell CHB leg with $[v_1 : v_2 : v_3] = [1 : 2 : 6]$. Assuming this is one leg of a three-phase system, third-harmonic injection can be used to increase dc bus utilization since this is a carrier-based technique.

2.3 Continued Post-Fault Operation

A three-phase cascaded H-bridge multilevel converter with M cells per leg is comprised of $12M$ solid-state switches. Due to this increased switch count, compared to the six solid-state switches utilized by traditional two-level voltage sources converters, CHB

have a higher probability of a switch fault occurring. However, CHB are fault tolerant due to their modular structure and techniques developed to enable their continued operation in the event of one or more faults. One of the most prominent techniques [24, 35,42,45,77,78,80,105] for enabling continued operation after a fault event, fundamental phase shift compensation (FPSC), is reviewed in this section. Before introducing FPSC, however, a less effective method is considered.

Define an $[a, b, c]$ CHB as a symmetric CHB with a healthy cells in leg A, b healthy cells in leg B, and c healthy cells in leg C. As shown in Fig. 2.11.a, continued operation of a $[5, 5, 2]$ CHB results in unbalanced line-to-line voltages if references fully utilize each leg's remaining healthy cells and 120° phase shifts between references are maintained. As shown in Fig. 2.11.b, however, balanced line-to-line voltages can be generated if only 40% of the voltage available in the healthy legs is utilized, effectively causing an equal number of cells in each leg to be bypassed. While this approach produces in balanced line-to-line voltages, the resulting voltage magnitudes may be decreased more than necessary due to healthy cells being bypassed. Healthy CHB cells can be more effectively utilized by implementing FPSC.

Balanced line-to-line voltages are generated via FPSC by adjusting the phase shift between references. Since references with specially selected phase shifts allow balanced operation when legs have an unequal number of healthy cells, the maximum producible line-to-line voltage may be increased compared to the case where an equal number of cells are bypassed in each CHB leg. However, this technique can only be implemented in CHB with a floating neutral point, since FPSC generated references have a non-zero common-mode component.

Angles between references which result in balanced line-to-line voltages are found by solving the system of equations,

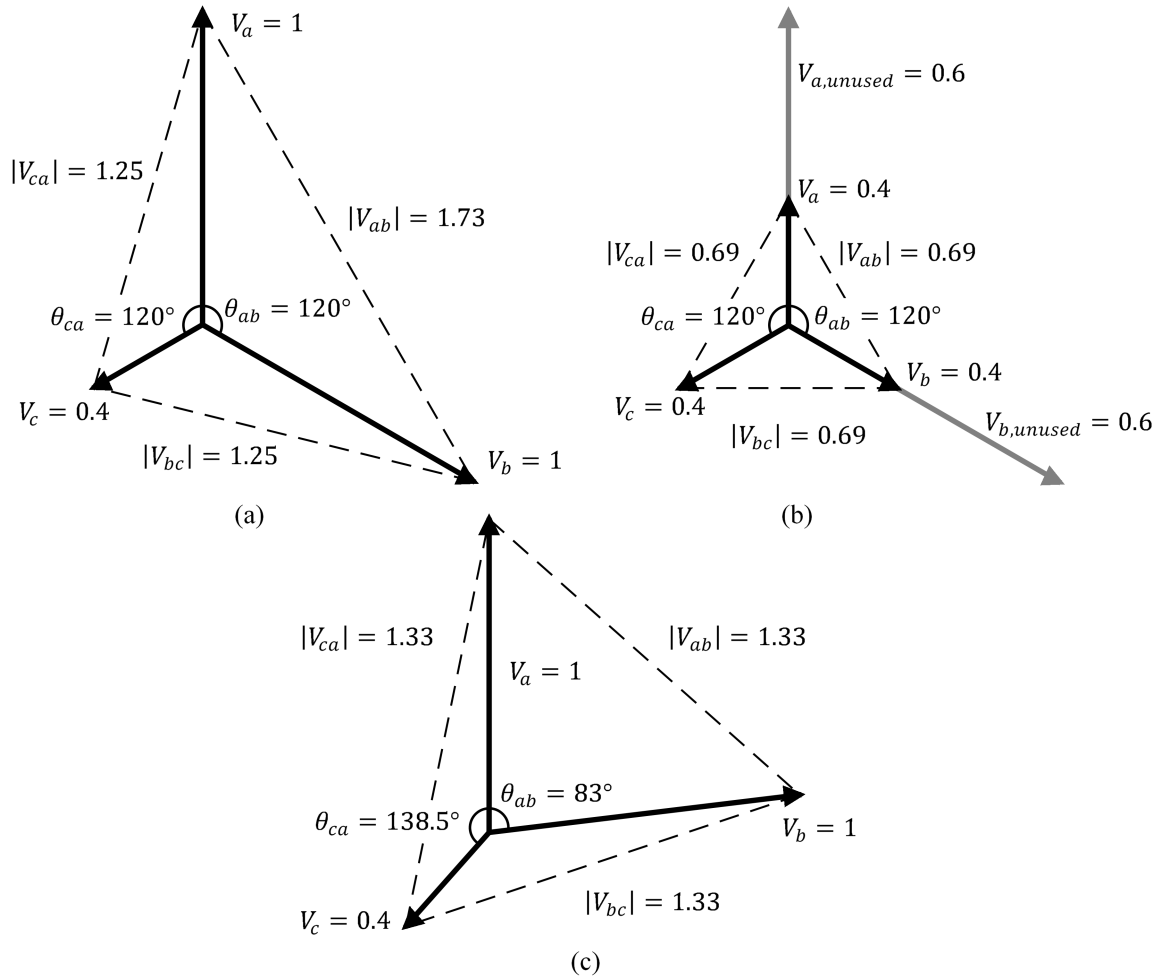


Fig. 2.11: Unbalanced line-to-line voltages generated by a $[5, 5, 2]$ CHB if references fully utilize the available leg voltages and maintain 120° phase shifts (a), balanced line-to-line voltages generated by utilizing only some of the cells in healthy legs (b), and balanced line-to-line voltages generated by applying FPSC to adjust phase shifts between references (c). All voltage magnitudes are normalized by $5V_{dc}$, the sum of dc bus voltages in a healthy leg.

$$V_{dc,a}^2 + V_{dc,b}^2 - V_{dc,a}V_{dc,b}\cos(\theta_{ab}) = V_{dc,b}^2 + V_{dc,c}^2 - 2V_{dc,b}V_{dc,c}\cos(\theta_{bc}) \tag{2.1}$$

$$V_{dc,a}^2 + V_{dc,b}^2 - V_{dc,a}V_{dc,b}\cos(\theta_{ab}) = V_{dc,c}^2 + V_{dc,a}^2 - 2V_{dc,c}V_{dc,a}\cos(\theta_{ca}) \tag{2.2}$$

$$\theta_{ab} + \theta_{bc} + \theta_{ca} = 360°, \tag{2.3}$$

where θ_{xy} is the angle between references x and y, and $V_{dc,x}$ is the sum of dc source

magnitudes of the healthy cells in leg x. Assuming the use purely sinusoidal references in the linear modulation region, applying FPSC to a $[5, 5, 2]$ CHB results in maximum line-to-line voltage magnitudes which are 91% larger than the maximum voltages producible if balanced voltages are obtained by bypassing healthy cells, as shown in Fig. 2.11.c, and FPSC obtained voltage magnitudes for a $[5, 5, 2]$ CHB are only 23% smaller than the voltages obtained by a healthy $[5, 5, 5]$ CHB. FPSC generated references and resulting ideal line-to-line voltages for a $[5, 5, 2]$ CHB are shown in Fig. 2.12, where all values are normalized by $5V_{dc}$, i.e. the total dc bus voltage of a healthy leg. Note that references' common-mode component, also shown in Fig. 2.12 for a $[5, 5, 2]$ CHB, is a sinusoid with the same frequency as the generated references. Note that solutions to the non-linear set of equations (2.1), (2.2), and (2.3) are generally stored in a lookup table and used when a fault event occurs, precluding the use of this technique to systems utilizing time-invariant, and typically symmetric, dc sources.

Under some conditions, there is no solution set to (2.1), (2.2), and (2.3). Moreoever, some solutions require a phase shift greater than 180° between references, resulting in

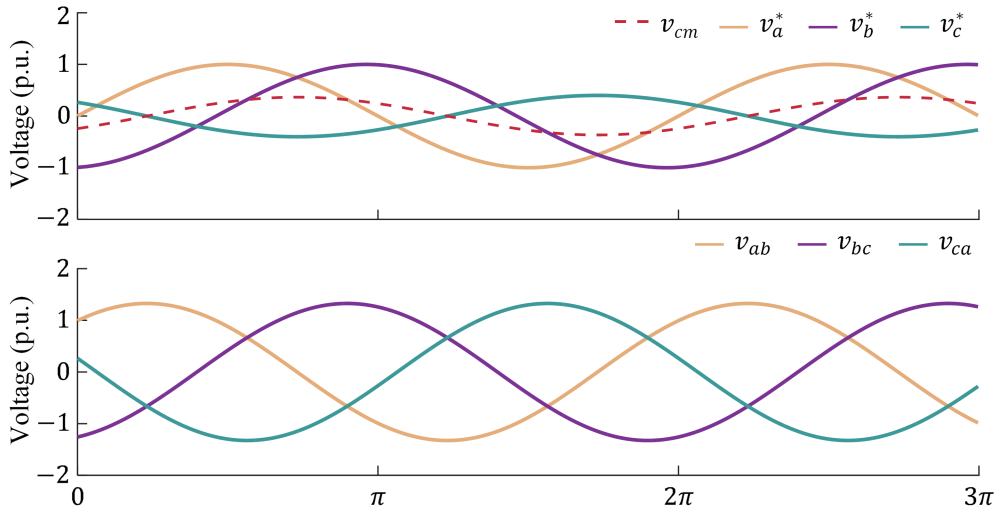


Fig. 2.12: FPSC generated references and their common-mode component (top) and ideal resultant line-to-line voltages (bottom) for a $[5, 5, 2]$ CHB. All waveforms are normalized by $5V_{dc}$.

line-to-line voltages which are smaller than those obtained using a 180° phase shift between references and decreasing utilization of the leg with the most healthy cells. These shortcomings are addressed [42] with the introduction of an extended FPSC method. Assuming $V_{dc,A} > V_{dc,B} \geq V_{dc,C}$ extended FPSC computes references using,

$$V_a^{new} = \sqrt{V_b^2 + V_b V_c + V_c^2} \tag{2.4}$$

$$\theta_{ab} = \sin^{-1}\left(\frac{\sqrt{3}}{2}\frac{V_b + V_c}{V_a^{new}}\right). \tag{2.5}$$

As an example, a $[5, 3, 2]$ CHB is considered. Under this configuration, as shown in Fig. 2.13, normalized line-to line voltage magnitudes of 0.87 can be generated using $\theta_{ac} = 60°$ and $\theta_{bc} = 240°$, calculated via (2.1), (2.2), and (2.3). Using (2.4) and (2.5), however, normalized line-to line voltage magnitudes of 1 can be generated using $\theta_{ab} = 83°$ and reducing the utilized magnitude of the normalized V_a from 1 to

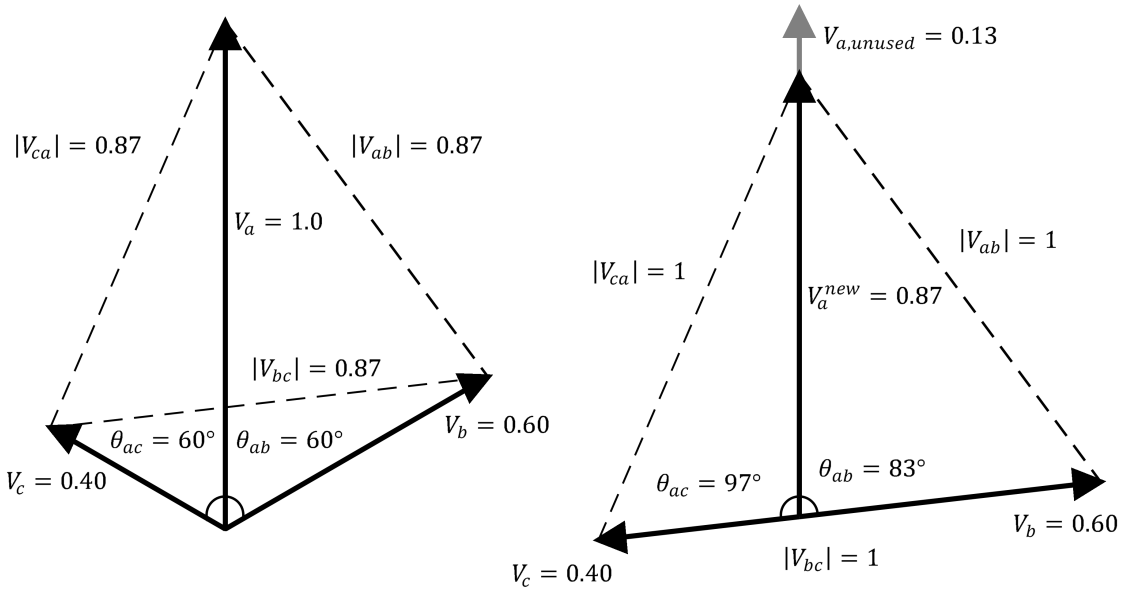


Fig. 2.13: Solutions to (2.1), (2.2), and (2.3) enable balanced voltages to be produced for a $[5, 3, 2]$ CHB (left), but larger voltage magnitudes can be obtained using extended FPSC, i.e. (2.4) and (2.5) (right). All voltage magnitudes are normalized by $5V_{dc}$.

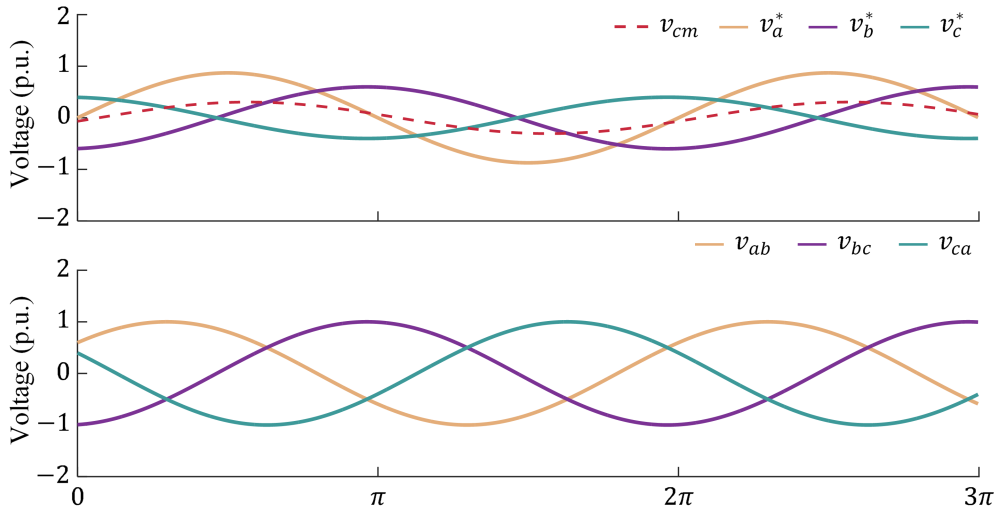


Fig. 2.14: FPSC references and common-mode component (top) and resulting ideal line-to-line voltages for a $[5, 3, 2]$ CHB. All waveforms are normalized by $5V_{dc}$.

0.87. Extended FPSC generated references and resulting ideal line-to-line voltages for a $[5, 3, 2]$ CHB are shown in Fig. 2.14, where all values are again normalized by $5V_{dc}$, i.e. the total dc bus voltage of a healthy leg. Similar to unextended FPSC, the common-mode component of references generated via extended FPSC, also shown in Fig. 2.14, is a sinusoid with the same frequency as the generated references.

Finally, note that third-harmonic injection may no longer be utilized to increase dc bus utilization when implementing FPSC or extended FPSC, since phase shifts between references are no longer 120° and reference magnitudes are no longer equal.

2.4 Conclusion

The cascaded H-bridge multilevel converter topology has been reviewed in this chapter. The LSPWM and hybrid PWM techniques have been presented, and third-harmonic injection for increasing dc bus utilization in three-phase CHB has been introduced. Finally, fundamental phase-shift compensation has been presented as an approach for enabling continued converter operation in the event of cell level faults.

Chapter 3

PQ Plane Operating Analysis

In this chapter, the operating points in the PQ plane which are available when using symmetric and asymmetric CHB converters are identified. Moreover, this chapter aims to explain why other converter output points must be avoided due to undesirable features, e.g. poor quality of the resultant current waveforms. Asymmetric CHB converters in particular, as described in Section 2.1, may have operating regions which are significantly restricted due to discordant output points, i.e. output points which cause power transfer between a leg's cells. This potentially undesirable behavior of asymmetric CHB converters is well known [3, 4], but the conditions which cause discordant output points have not been explicitly identified. To address this deficiency, a load-independent technique which allows these discordant output points to be identified is proposed in this chapter. Overall, the work presented in this chapter aims to provide distribution engineers with information regarding the feasible active and reactive-power which can be injected by grid-tied CHB converters, and to create a framework for assessing operating point trajectories when altering the steady-state operation of grid-tied CHB converters. The presented analysis also provides a basis for selecting and modifying steady-state PWM generation techniques in order to meet de-

sired performance criteria. Moreover, the techniques presented provide a foundation which can be built upon to facilitate the analysis of grid-interactive CHB under a wide range of conditions, such as continued operation after CHB cell faults or when when grid voltages contain negative-sequence or harmonic components.

This chapter contains four sections. In Section 3.1, grid-tied symmetric CHB converter output points are analyzed in order to identify the converter's operational region. In Section 3.2, the results presented in Section 3.1 are extended to include discordant output points, allowing the operating region for grid-interactive asymmetric CHB converters to be determined. Numerical test cases are presented in Section 3.3 to verify the methods presented, and concluding remarks are provided in Section 3.4.

3.1 Symmetric CHB Converter Operating Region

In this section, the PQ plane operational region of a symmetric CHB converter is identified. While the analytical approach presented in this chapter is not restricted to any particular PWM scheme, for all simulation results presented in this section, first-on-first-off level-shifted PWM (LSPWM) as described in Chapter 2 was used to individually control CHB legs. Since this PWM technique utilizes a reference waveform, converter output points in the PQ plane are selected by adjusting the reference's modulation index, m, and the phase angle, δ, between the reference and the grid voltage. Only one phase angle needs to be defined for a balanced three-phase converter, as the remaining angles are found as $\delta + 2\pi/3$ and $\delta - 2\pi/3$. While a desired PQ output point is generally produced using closed-loop control, in this chapter the parameters used for PWM generation are directly varied in order to facilitate analysis of a converter's operational region. It is worth noting that the implementation of a control scheme does not alter a converter's operational region, it only automates the

selection of PWM parameters in order to meet specific goals. As such, understanding a converter's operational region is important for control systems design, filter design, component selection, etc.

An equation which describes the PQ plane behavior of a grid-interactive CHB can be derived by considering apparent power, S. Measured from the grid-perspective,

$$S = V_G \left(\frac{V_I - V_G}{Z_{eq}} \right)^* = \frac{|V_I|\,|V_G|\,e^{-j\delta}}{Z_{eq}^*} - \frac{|V_G|^2}{Z_{eq}^*}, \tag{3.1}$$

where $|V_I|$ and $|V_G|$ respectively correspond to the rms line-to-line converter and grid voltages, and Z_{eq} is the equivalent impedance coupling the converter and grid. Note that $|V_I|$ is proportional to m and the converter's dc bus voltages, but an explicit relationship is dependent upon the PWM scheme utilized. To prevent low order harmonics, it is assumed that the converter operates in the linear region.

The output region of a CHB is defined by (3.1), and each point within the region is a converter output point. Assuming $|V_G|$, Z_{eq}, and the converter's dc bus voltages are constant, for m in the linear modulation range and $0 \leq \delta < 2\pi$, equation (3.1) describes a disk in the PQ plane with radius

$$R = \frac{|V_I|\,|V_I|}{|Z_{eq}|} \tag{3.2}$$

centered at

$$\text{Point } O = \frac{-|V_G|^2}{Z_{eq}^*} \tag{3.3}$$

Point O is the converter's output origin, as this is the output point when $m = 0$ is used for PWM generation.

Using (3.2) and (3.3), grid-interactive symmetric CHB output points in the PQ plane can be identified for various values of m and δ. As shown in Fig. 3.1, varying δ from 0 to 2π for fixed values of m traces circles of output points centered at Point O in the PQ plane, with larger values of m tracing circles with larger radii. On the other hand, radial lines extending from Point O are traced by PQ plane output points by varying m for fixed values of δ. If the converter and the grid are completely in phase then there exists a converter voltage magnitude such that the grid does not provide or absorb any active or reactive-power. Accordingly, when there is no phase-shift between the grid and converter, i.e. $\delta = 0$, output point's trajectory of departure from Point O passes through the origin of the PQ plane, as shown in Fig. 3.1. If the converter

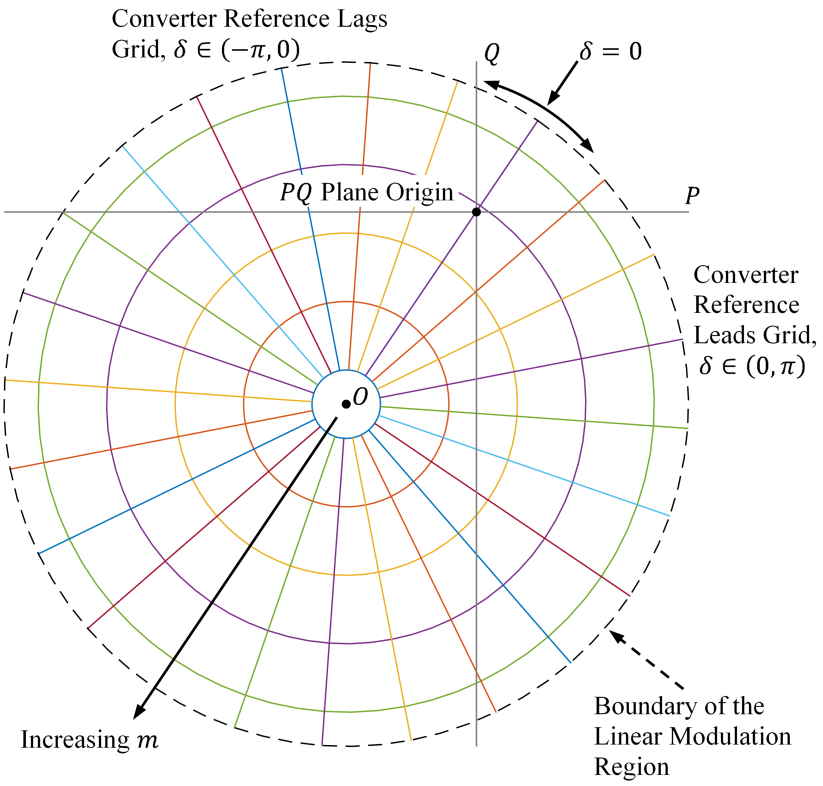


Fig. 3.1: The boundary of the linear modulation region defines the output region for a grid-interactive CHB. Converter output points for fixed m and variable δ trace circles in the PQ plane, while output points trace radial lines for fixed δ and variable m.

reference leads the grid, i.e. $\delta \in (0, \pi)$, then the radial line of output points extending from the converter's output origin may cross the $j\omega$ axis at a negative value (as for an inductive load), whereas if the converter reference lags the grid, i.e. $\delta \in (-\pi, 0)$, then the radial line of output points may cross the $j\omega$ axis at a positive value (as for a capacitive load).

Equations (3.2) and (3.3) show that the output region of a grid-interactive CHB is dependent upon the impedance coupling the converter and grid, Z_{eq}. Assuming an inductive filter is used, the impact of varying a nominal Z_{eq} by ten percent is shown in Fig. 3.2. As Z_{eq} increases, the size of the resulting output region decreases. Further, output regions defined by larger Z_{eq} are subsets of the output regions defined by smaller Z_{eq}, as shown in Fig. 3.2, illustrating that an oversized filter will limit the maximum

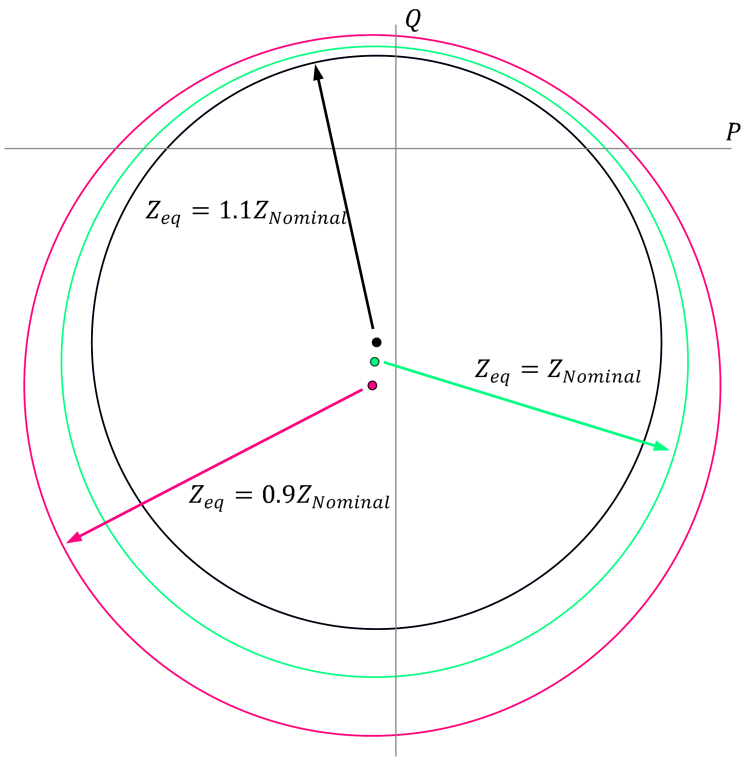


Fig. 3.2: Alterations of the converter's output region due to ten percent deviations of a nominal impedance used coupling the converter and grid.

active and reactive-power which a converter can provide using a fixed voltage.

Once a CHB converter's output region has been identified, the current generated by each output point within that region must be analyzed to ensure grid standards, e.g. IEEE 519 [103], are met, and those output points which do not meet grid standards must be excluded from the converter's operating region. The quantifier of waveform quality discussed here is total harmonic distortion (THD), defined for a current waveform as,

$$\text{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{3.4}$$

where I_h is the rms magnitude of the h^{th} harmonic. To ensure that a given output point produces a current waveform which meets THD limitations, the numerator and denominator of (3.4) are analyzed independently as follows:

- When considering the numerator of (3.4), i.e. the 2-norm of the injected current harmonics, it is noted that harmonic currents are the result of harmonic voltages generated by the converter. Since the grid-side harmonic voltages are assumed to be zero, phase shifts between grid and converter harmonic voltages are irrelevant, thus the numerator of (3.4) is independent of δ and is therefore symmetric about the converter's output origin, Point O.

- The denominator of (3.4), i.e. the fundamental component of the injected current, is proportional to $|S|$, and is therefore symmetric about the origin of the PQ plane if the grid voltage is assumed to be ideal, as $S = \sqrt{3}V_G I^*$. Thus, near the origin of the PQ plane the denominator of (3.4) approaches zero and so the THD increases dramatically. Accordingly, converter output points near the origin of the PQ plane do not meet THD standards and therefore cannot be utilized as operating points.

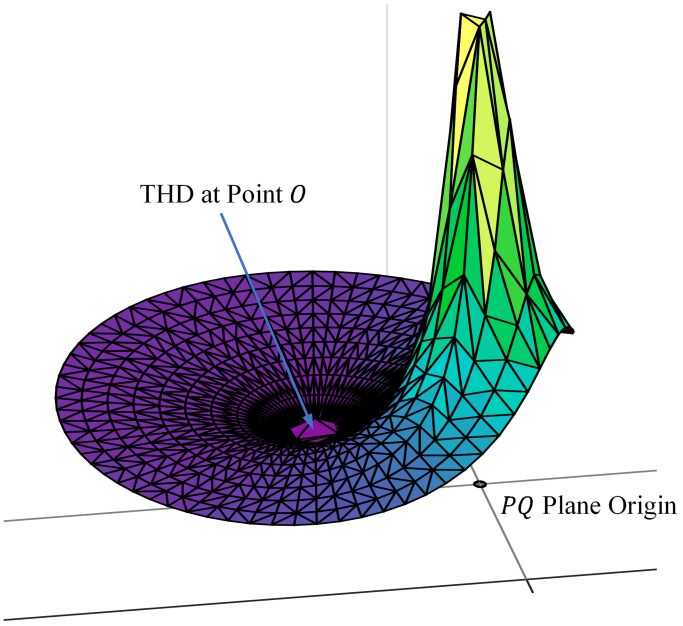


Fig. 3.3: Line current THD for the PQ plane output region of a grid-interactive CHB. Distortion increases dramatically near the origin of the PQ plane, and values of THD are asymmetric about the PQ plane's origin.

The THD produced by output points of a symmetric grid-interactive CHB converter is shown in Fig. 3.3, clearly illustrating that a converter's operating region must be restricted to exclude output points near the PQ plane origin which cause high THD. It should be noted that the numerator and denominator of (3.4) have different points of symmetry, and therefore the excluded output points are not symmetric about the origin. Because output region THD is asymmetric around the origin of the PQ plane, ensuring that THD restrictions are met for a given $|S|$ requires testing a specific, worst case THD output point. If the 2-norm of the injected current harmonics are assumed to increase monotonically with m, then for a given value of $|S|$ the output point with the highest THD is the output point farthest from Point O. Thus, the output point which maximizes THD for a fixed $|S|$ lies on the trajectory defined by $\delta = 0$. If no output point is available at $\delta = 0$ for a given $|S|$, then the smallest magnitude of δ for which an output point exists will define the highest THD value.

Another operating region restriction introduced when constructing a grid-interactive CHB converter is caused by real-world components with limited VA ratings, thereby defining an $|S_{max}|$ which cannot be exceeded. Determining a desirable value of $|S_{max}|$ for a given CHB output region, and choosing components accordingly, may not be a straight-forward process. As described by (3.1), a grid-interactive converter's output region is centered about Point O, and therefore, as shown in Fig. 3.2, $|S|$ corresponding to the Quadrant I output point with maximum P is not necessarily equal to the $|S|$ corresponding to the Quadrant I output point with maximum Q, and thus desirable VA ratings can be defined in many ways. Two possible methods for defining a desirable $|S_{max}|$ are shown in Fig. 3.4. One possibility is to define $|S_{max}|$ based on the largest disk in the PQ plane which is a subset of the converter's output region. However, components selected using this definition cannot support the maximum active and reactive-power which the converter could otherwise supply. Another possibility is to select $|S_{max}|$ based on the smallest disk in the PQ plane which contains all Quadrant I converter output points. Components selected based on this definition, however, are fully utilized only at a few select output points. Regardless of which $|S_{max}|$ is used to select components, many output points of a grid-tied CHB cannot be considered as operating points due to the large values of $|S|$ associated with them.

The operational region of a grid-interactive symmetric CHB is shown in Fig. 3.5, where it is assumed that the converter is meant to supply power. This operating region is defined by *(i)* the converter output region defined according to (3.1) for a fixed filter, *(ii)* grid-interconnection standards for maximum THD, *(iii)* VA limitations imposed by converter components, and *(iv)* the assumption that power is to be delivered to the grid. Note that the operational region shown in Fig. 3.5 is asymmetric, partially due to component VA ratings selected such that the converter output point in Quadrant I with maximum Q is enclosed.

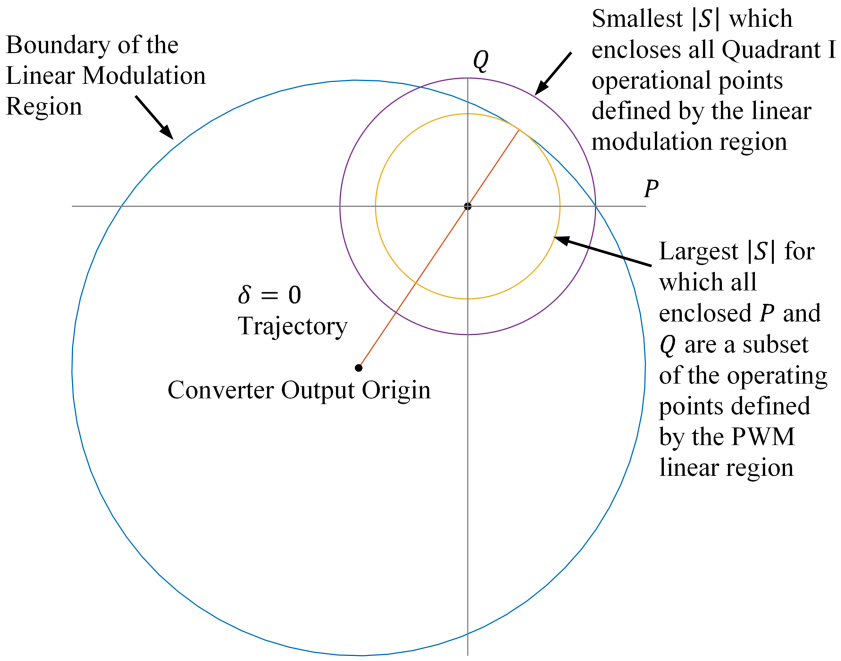


Fig. 3.4: Two potentially desirable $|S_{max}|$ values, used for component selection, based on the disk defined by the linear modulation region.

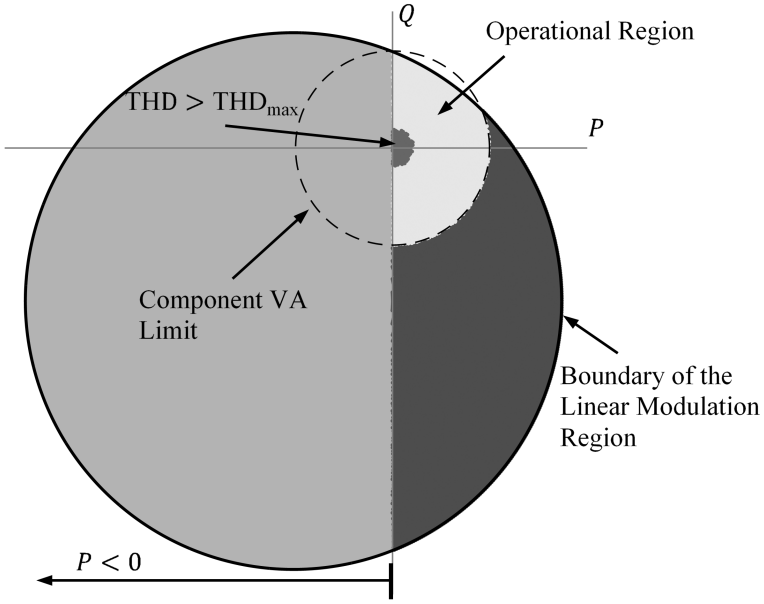


Fig. 3.5: PQ plane operational region for a grid-tied symmetric CHB converter operating in the linear PWM region.

The operational region shown in Fig. 3.5 is similar to the operational region for a grid-interactive traditional two-level inverter, as presented in [84]. Further, the analysis presented in this section is general and therefore may be applicable to wide range of grid-interactive converter topologies. However additional factors may act to restrict the operational region for some topologies, such as the asymmetric CHB analyzed in the next section.

3.2 Asymmetric CHB Converter Operational Region

In this section, the PQ plane operational region for asymmetric CHB converters is identified. For all simulation results presented in this section, LSPWM for asymmetric CHB, detailed in Chapter 2, was used to individually control CHB legs. Similar to the previous section, converter output points are selected by varying m and δ of the reference waveform used for PWM generation.

Initially, the analysis for an asymmetric CHB is very similar to the analysis for the symmetric CHB. That is, (3.1) still applies, filter variation effects are still observed, and restrictions based on THD and component ratings must be considered. When utilizing asymmetric sources, however, under certain conditions power transfer between CHB cells may occur, e.g. some CHB cells may receive a net regenerative power flow even if the overall converter is supplying power. This behavior is generally undesirable, and therefore these discordant output points may need to be identified and excluded from the converter's operation region.

While the power delivered by each CHB cell can be analyzed on a case-by-case basis to identify discordant output points, analysis using a load-independent method would be more convenient. Thus, instead of determining the power delivered by each cell in

a CHB leg, it may be beneficial to instead compute the ratio of power delivered by cell n, P_n, to the total power delivered by the leg containing that cell, P_L. Thus,

$$\frac{P_n}{P_L} = \frac{\left(V_n/\sqrt{2}\right) I \cos\left(\theta_n\right)}{\left(\sum_k V_k/\sqrt{2}\right) I \cos\left(\theta_k\right)} = \frac{V_n}{V_L} \tag{3.5}$$

where V_n and V_L are, respectively, the fundamental voltage component generated by cell n and the CHB leg, and it is assumed that cell voltages are in-phase, i.e. $\theta_x = \theta$ $\forall x$. An output point is cell n discordant if $V_n/V_L < 0$, indicating cell n absorbs power while the leg delivers power, or vice-versa.

The reference used for PWM generation can be used to determine V_L directly. The ideal voltage generated by cell n, i.e. the PWM reference as seen by cell n, is analyzed in order to determine V_n. Typically however, a PWM reference, $r\left(\theta\right)$, is only provided for a CHB leg, and so references seen by individual cells are not immediately available. As such, the reference seen by a cell must be constructed for the purpose of this analysis. When using LSPWM for gate signal generation, cell references can be obtained by adjusting the amplitude and bias of the leg reference waveform based on cell voltages and utilized leg output voltages. For instance, Fig. 3.6 shows the PWM references seen by each cell of a two-cell CHB leg when $v_1 = 100\,\mathrm{V}$, $v_2 = 150\,\mathrm{V}$, and $r\left(\theta\right) = 200\sin\left(\theta\right)$, assuming all available leg output voltages are used. It is emphasized that cell references are used for analysis only and are not required for PWM generation.

Once the cell n reference, $r_n\left(\theta\right)$, is known, the fundamental reference component is computed using the Fourier series as,

$$V_n = \frac{1}{\pi}\int_0^{2\pi} r_n\left(\theta\right)\sin\left(\theta\right)\mathrm{d}\theta \tag{3.6}$$

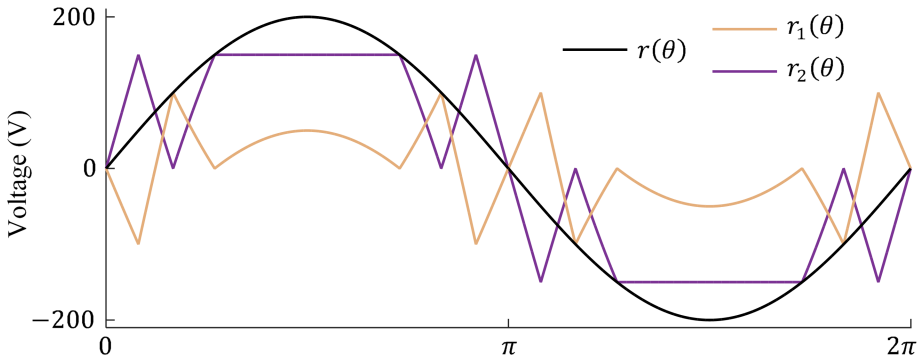


Fig. 3.6: LSPWM and cell references for an $M = 2$ cell CHB with $v_1 = 100\,\text{V}$, $v_2 = 150\,\text{V}$, and $r\,(\theta) = 200\sin\,(\theta)$. Cell references $r_1\,(\theta)$ and $r_2\,(\theta)$ are not typically available, but are constructed for analysis.

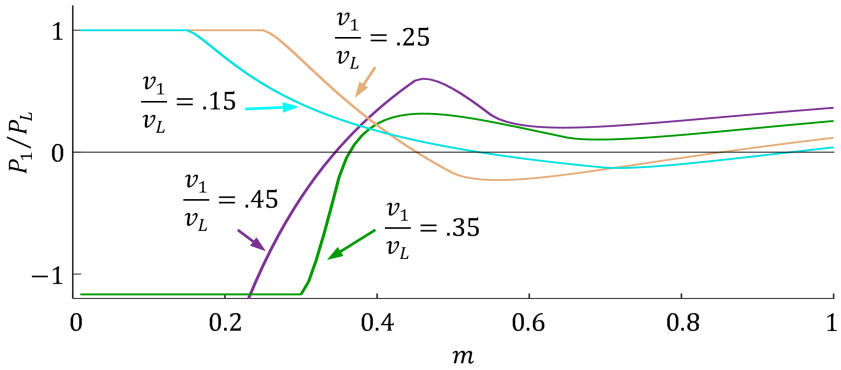


Fig. 3.7: Power ratio for the low voltage cell, cell 1, of a two-cell CHB for varying ratios of $v_1/\,(v_1 + v_2) = v_1/v_L$, *assuming all available voltage outputs are used for PWM generation.* A given value of m results in a cell 1 discordant output point if $P_1/P_L < 0$.

The value obtained using (3.6) can then be compared to the fundamental component of the leg reference as in (3.5) to determine the power contribution of cell n.

For a two-cell CHB with $v_1 < v_2$, Fig. 3.7 shows P_1/P_L within the converter's output region for varying $v_1/\,(v_1 + v_2) = v_1/v_L$ ratios, assuming all available converter voltages are utilized. When $P_1/P_L < 0$, cell 1 is discordant, and thus discordant output points are identified. A dramatic change occurs in the P_1/P_L function when $v_1/v_L = 1/3$, since the lowest available voltage magnitude is v_1 when $v_1/v_L < 1/3$, and $v_2 - v_1$ when $v_1/v_L > 1/3$. As shown in Fig. 3.7, discordant output points occur at

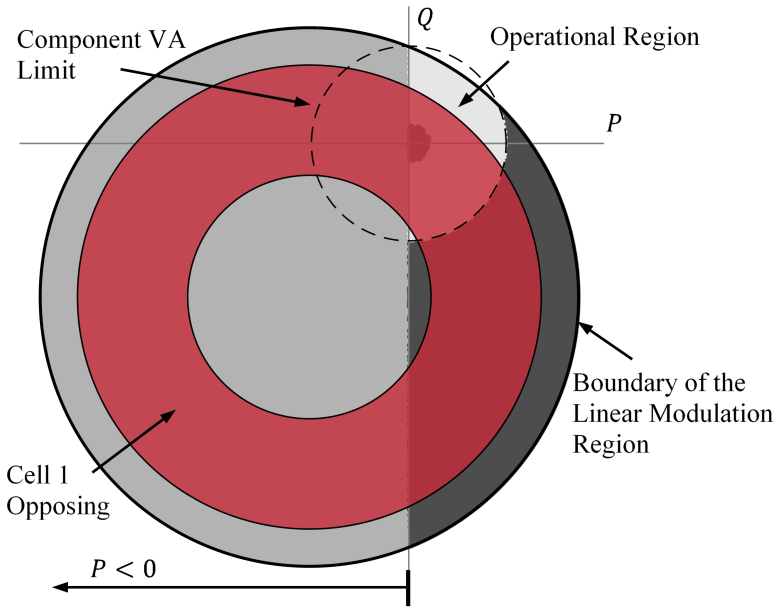


Fig. 3.8: PQ plane operational region for a two-cell grid-tied asymmetric CHB converter operating in the linear region, with all available output voltages utilized. Voltage ratios are in the trinary configuration, $v_1 : v_2 = 1 : 3$.

higher values of m when $v_1/v_L < 1/3$, and therefore these voltage ratios are most likely to have the most significant impact on the operational region of an asymmetric CHB.

The operational region for a two-cell asymmetric CHB converter, with $v_1/v_L = 0.25$, is shown in Fig. 3.8. This trinary configuration, where $v_1 : v_2 = 1 : 3$, provides the greatest number of evenly spaced converter output voltages when using a two-cell CHB [4, 100]. However, this configuration results in cell 1 discordant output points which restrict the operational region if discordant behavior is to be prevented. Alternatively, the location of discordant output points in the PQ plane may be modified if some available converter output voltages are not utilized during PWM generation. For instance, all discordant output points can be eliminated when using a two-cell asymmetric CHB, as shown in Fig. 3.9, if the output voltages $\pm(v_1 - v_2)$ are not utilized during PWM generation.

The behavior of discordant output points can be more complex for asymmetric

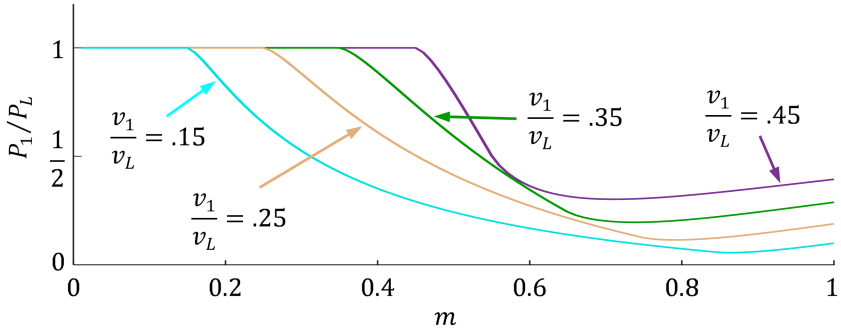


Fig. 3.9: Power ratio P_1/P_L for the low voltage cell of a two-cell CHB for varying ratios of $v_1/(v_1+v_2) = v_1/v_L$, *assuming converter voltages* $v_1 - v_2$ *and* $-v_1 + v_2$ *are not used for PWM generation.*

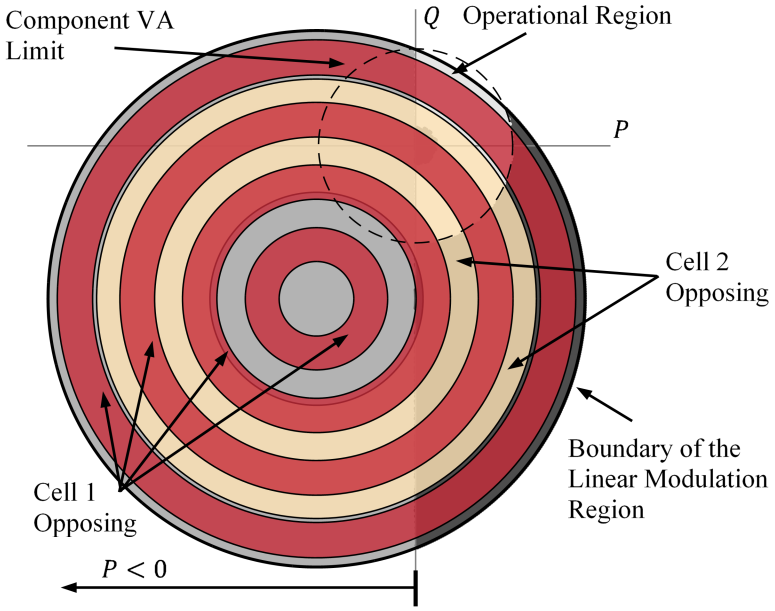


Fig. 3.10: PQ plane operational region for a three-cell grid-tied asymmetric CHB converter operating in the linear region, *with all available output voltages utilized.* Voltage ratios are in the trinary configuration, $v_1 : v_2 : v_3 = 1 : 3 : 9$.

CHB converters with more than two cells. For instance, Fig. 3.10 shows the available operational region for a three-cell CHB, if voltage ratios are again selected such that the greatest number of evenly spaced converter output voltages are available, i.e. in the trinary configuration where $v_1 : v_2 : v_3 = 1 : 3 : 9$. The operational region shown in Fig. 3.10 must be heavily restricted if discordant output points are not permitted.

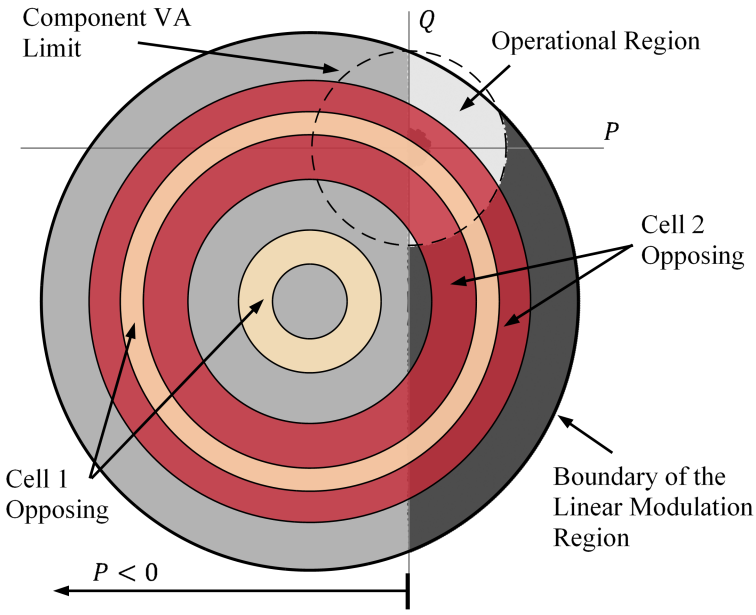


Fig. 3.11: PQ plane operational region for a three-cell grid-tied asymmetric CHB converter operating in the linear region, *with some output voltages unused*. Voltage ratios are in the trinary configuration.

However, by eliminating the use of some voltage levels, the converter's operational region is modified. For instance, $\pm(-v_1 + v_2 + v_3)$ and $\pm(-v_1 - v_2 + v_3)$ are not used, the resulting operational region is as shown in Fig. 3.11. In this way, (3.5) may be used to identify a converter's discordant operating regions, and can also facilitate the selection and modification of steady-state PWM generation techniques in order to meet desired performance criteria.

3.3 Numerical Test Cases

In this section, two numerical test cases are provided to demonstrate the validity of the presented models for analyzing a grid-interactive converter's output region and for identifying discordant operating points for asymmetric CHB. Since laboratory scale equipment may only enable a small portion of the converter's operating region to be

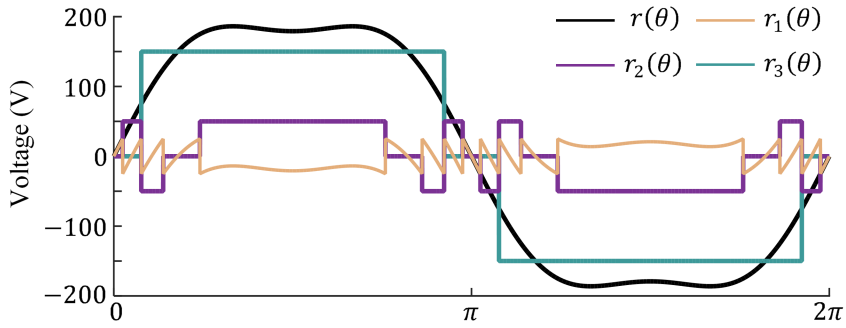


Fig. 3.12: PWM and cell references for an $M = 3$ cell CHB with $v_1 = 25\,\text{V}$, $v_2 = 50\,\text{V}$, $v_3 = 150\,\text{V}$, and $r(\theta) = 215\,(\sin(\theta) + \sin(3\theta)/6)$. Using hybrid PWM, only the low voltage cell switches at PWM frequency.

validated, e.g. [84], data were collected using MATLAB/Simulink simulation software to enable validation of the entire CHB output region.

For both numerical test cases, a grid with negligible impedance and line-to-line rms voltage $|V_G| = 208\,\text{V}$ was connected to an $M = 3$ cell CHB with dc bus voltages $v_1 = 25\,\text{V}$, $v_2 = 50\,\text{V}$, and $v_3 = 150\,\text{V}$. This $1:2:6$ ratio enables hybrid PWM to be applied with the maximum number of converter output voltages, as explained in Chapter 2. Hybrid PWM was used to generate gate signals, with switching frequency $f_s = 6.12\,\text{kHz}$ applied to the low voltage cell. PWM references were injected with a third-harmonic component equal to one-sixth of the fundamental component, enabling the CHB to produce a maximum line-to-line rms voltage $|V_I| = \sqrt{2}\,(v_1 + v_2 + v_3)$. Typical hybrid PWM and cell references are shown in Fig. 3.12.

The two numerical test cases differed only in the filter used to couple the converter to the grid. For the first test case, the converter filter was purely inductive, with $L_f = 5\,\text{mH}$ and non-ideal resistance $R_f = 0.5\,\Omega$, whereas an LCL filter was used for the second test case, with inverter-side inductance $L_{fI} = 1\,\text{mH}$, grid-side inductance $L_{fG} = .5\,\text{mH}$, $C = 5\,\mu\text{F}$ (Y-connected), with non-ideal resistances $R_{LI} = 0.1\,\Omega$, $R_{LG} = 0.05\,\Omega$, and $R_C = 0.1\,\Omega$. Both test cases were analyzed for 16560 m and δ combinations, with m varied in the linear PWM range in steps of 0.01 from 0.01 to 1.15, and δ varied

Table 3.1: Numerical Test Case Results

	Test Case 1	Test Case 2
Z_{eq} (Ω)	$0.5 + j1.8850$	$0.1501 + j0.5657$
Point O (kW, kVAR)	$(-5.69, -21.44)$	$(-18.96, -71.44)$
Output Region Radius (kVA)	33.9	113.1
Max $P > 0$ for $Q = 0$ (kW)	20.5	68.7
Max $Q > 0$ for $P = 0$ (kVAR)	11.9	40.1
	$(4.4, 7.9)$	$(14.7, 26.5)$
Cell 1 Discordant Regions	$(12.0, 15.6)$	$(40.2, 51.9)$
(inner, outer) radii (KVA)	$(19.7, 23.2)$	$(65.6, 77.4)$
	$(27.3, 30.8)$	$(91.1, 102.8)$
Cell 2 Discordant Region	$(12.0, 26.1)$	$(40.2, 87.2)$

in 2.5° steps from 0° to 357.5°.

The converter output regions obtained for both test cases were similar the output region shown in Fig. 3.10. That is, the output regions for both test cases include four annular regions for which cell 1 is discordant, and one annular region for which cell 2 is discordant. The inner and outer radii of these annular regions, as well as Z_{eq}, the output origins, and the output region radii, are summarized in Table 3.1 for both test cases. Also, similar to Fig. 3.10, output points for both test cases produced currents with THD ≥ 5 near the PQ plane origin. Due to LCL filter resonance, this increased THD was found for 25 output points in the second test case, compared to two output points in the first test case. The range of outputs which result in high THD when using an LCL filter could be attenuated via passive or active damping techniques [82, 83].

The data in Table 3.1 show the CHB analyzed for the second test case was able to supply a higher maximum active-power than the CHB in the first test case, despite both setups utilizing the same dc bus voltages. Via (3.1), the dc bus voltages for the first test case would need to increase more than two-fold for the resulting converter output region to include the same maximum output point available using the second test case, $P = 68.7\,\text{kW}$ $Q = 0$. These considerations may be useful when selecting

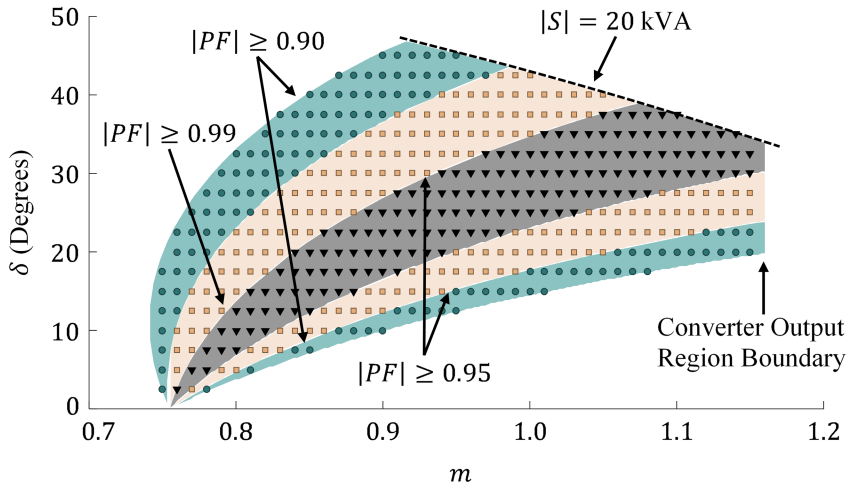


Fig. 3.13: Simulated data (markers) from test case 1 compared to results (shaded areas) obtained via (3.1), showing regions in the $m\delta$ plane corresponding to power factors greater than 0.9, 0.95, and 0.99 when power is delivered to the grid and components have an artificially imposed VA limit of 20 kVA.

filters and dc bus voltages for a grid-interactive CHB.

For the first test case, m and δ values which caused the converter to deliver active-power to the grid with power factors greater than 0.9, 0.95, and 0.99 were identified. The identified values were then restricted to identify m and δ which resulted in PQ output points with apparent power less than 20 kVA, an artificial component limit selected based on the maximum active-power deliverable by the converter. In Fig. 3.13, this set of m and δ values are compared to results obtained via (3.1), with a close match between the two data sets observed. The narrow range of m and δ which result in desirable converter behavior, as shown in Fig. 3.13, can be useful when designing and analyzing the performance of controllers for grid-interactive CHB.

To determine the validity of the technique proposed in Section 3.2 for identifying discordant output points, for both test cases the mean value of P_x/P_L at each m was computed and then compared results obtained via (3.5). To avoid outliers caused by dividing by small P_L, 64 data points for which $|P_L| < 10W$ were omitted when computing mean values of P_x/P_L. Since the method presented in Section 3.2 is load

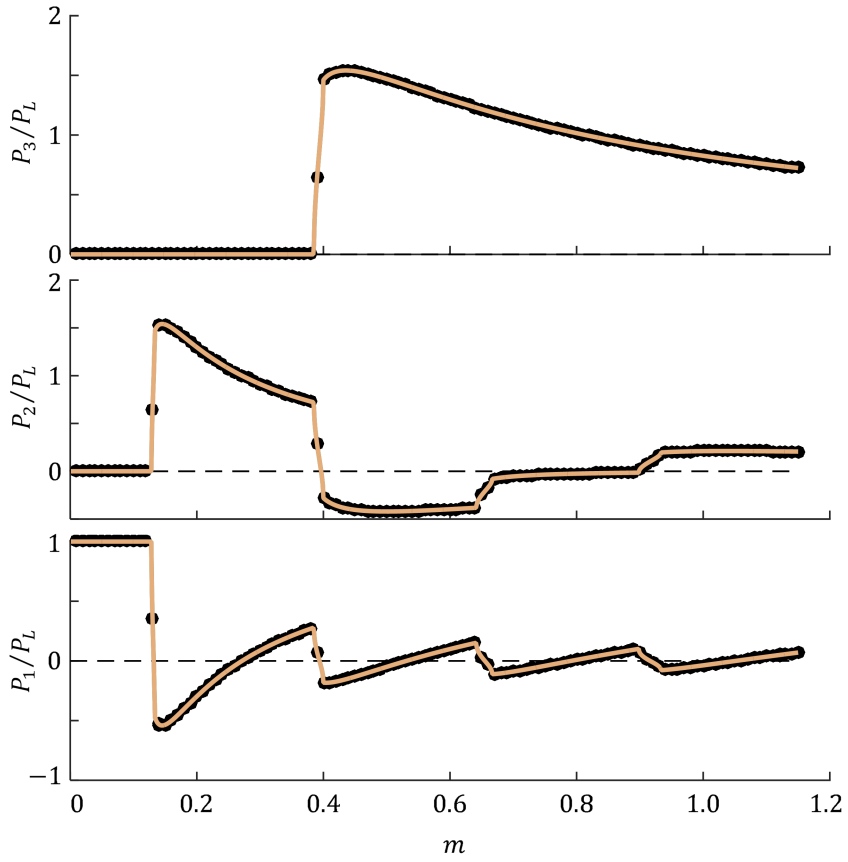


Fig. 3.14: Simulated data (black markers) from both test cases compared to data (gold) obtained via (3.5), showing the ratio P_x/P_L is only dependent upon m.

independent, Fig. 3.14 shows results from (3.5) compared to data obtained for both test cases. As shown in Fig. 3.14, there is close agreement between the proposed technique and the data collected for all three leg cells, verifying the presented load-independent approach for identifying discordant operating points.

Finally, as per the analysis presented in Section 3.1, the converter output origin and output region radius provided in Table 3.1 for the first test case can be used to approximate results for the second test case using the multiplicative factor $Z_{eq,1}/Z_{eq,2}$, where $Z_{eq,y}$ is Z_{eq} for test case y. Moreover, discordant behavior for both test cases is caused by the same values of m, and hence the same values of $|V_I|$. Accordingly, since (3.2) allows computation of radii for given $|V_I|$, the radii of the discordant regions

presented in Table 3.1 can be related using the same $Z_{eq,1}/Z_{eq,2}$ factor.

3.4 Conclusion

In this chapter, the PQ plane operational region for grid-interactive symmetric and asymmetric CHB converters have been identified. The operational region for symmetric CHB converters has been shown to be defined by *(i)* the boundary of the linear modulation region, influenced by the equivalent impedance coupling the converter and grid, *(ii)* VA ratings of system components, and *(iii)* a region of high THD near the origin of the PQ plane. In addition to these three factors, it has also been shown that the operational region for asymmetric CHB converters is also shaped by discordant operating regions, which are determined by *(iv)* the PWM generation technique used as well as *(v)* the asymmetries of the available cell voltages. Understanding the operational region for these CHB converter topologies provides distribution engineers with information regarding the feasible active and reactive-power which can be generated by grid-tied converters. It has also been demonstrated that the results presented in this chapter can also be used as the basis for investigating the trajectories of operating points in the PQ plane when altering the steady-state behavior of grid-tied CHB converters. Finally, the presented techniques form a foundation which can facilitate the analysis of grid-interactive CHB under conditions such as grid voltage imbalance or continued operation after cell faults.

Chapter 4

Atypical PWM for Maximizing DC Bus Utilization

In this chapter, an atypical technique for modifying PWM references by injecting a common-mode component is proposed for microgrid-interactive cascaded H-bridge multilevel converters operating under balanced and unbalanced conditions. The proposed technique *(i)* can be implemented in real-time without utilization of lookup tables, *(ii)* enables continued operation under internal fault conditions, *(iii)* is implemented independently from any converter controllers, and *(iv)* is compatible with any carrier-based PWM methods used for gate signal generation, enabling its use for symmetric and asymmetric converters. The proposed approach is analyzed for use during balanced and unbalanced conditions under both healthy and faulty converter operation.

This chapter contains for sections. The PQ plane analysis technique introduced in Chapter 3 is expanded in Section 4.1 to enable analysis when grid-interactive converters provide negative-sequence compensation. In Section 4.2 the proposed common-mode reference adjustment technique is presented and analyzed. Experimental data are presented in Section 4.3, and concluding remarks are provided in Section 4.4. Note

that while the atypical PWM technique introduced in this chapter can also be applied to stand alone operation, the presented analysis focuses on grid-interactive performance to highlight the performance of this method during unbalanced grid operation.

4.1 PQ Plane Output Region Under Unbalanced Conditions

As presented in Chapter 3, the apparent power, S, delivered by a grid-interactive CHB measured from the grid-perspective is computed as,

$$S = \frac{|V_I|\,|V_G|\,e^{-j\delta}}{Z_{eq}^*} - \frac{|V_G|^2}{Z_{eq}^*}, \tag{4.1}$$

where $|V_I|$ and $|V_G|$ respectively correspond to the positive-sequence rms line-to-line converter and grid voltage components, δ is the phase shift between positive-sequence grid and converter voltages, and Z_{eq}^* is the complex conjugate of the equivalent impedance coupling the converter and grid. Once again, note that $|V_I|$ is proportional to the converter's dc bus voltages and the modulation index, m, defining the PWM references' positive-sequence component, but an explicit relationship is dependent upon the PWM scheme utilized.

As detailed in Chapter 3, the PQ output points which a converter is able to supply can be determined by evaluating (4.1) for all possible m and δ. The theoretical PQ plane output region of a converter is defined as the collection of these output points. Practically, the operating region of a grid-interactive CHB is the portion of the output region which satisfies total harmonic distortion (THD) standards and does not exceed component-specific apparent power restrictions [106]. If the CHB is asymmetric, further restrictions may be imposed to prevent operation at discordant operating points,

i.e. output points where some cells in a leg have a net regenerative power flow when the overall leg is providing power, or vice-versa. However, analyzing a converter's entire output region gives insight into converter behavior, particularly when the converter provides auxiliary services.

Assuming operation is restricted to the linear PWM region, the output region of a grid-interactive CHB can be defined by the converter's output origin, obtained by evaluating (4.1) for $|V_I| = 0$, as well as the output region boundary identified by evaluating (4.1) for the maximum m which results in linear PWM operation for each $\delta \in [-\pi, \pi]$. When no auxiliary services are being supplied, the maximum m, and hence the upper limit of $|V_I|$, is independent of the phase shift between grid and converter voltages. Accordingly, the output region of a healthy microgrid-interactive CHB defines a disk in the PQ plane, as shown in Fig. 4.1. As auxiliary services are provided, however, the maximum m which ensures linear-region PWM may decrease, and become δ dependent, causing the converter's output region to shrink, become distorted, and no longer define a disk. For instance, Fig. 4.1 also shows converter output region boundaries when PWM references must include a fixed negative-sequence component. Fig. 4.1 further shows that altering the angle of the negative-sequence component, with respect to the positive-sequence component of the grid, causes the converter's output region to rotate about the output origin.

The output region boundary of a grid-interactive CHB can be expanded by implementing techniques for increasing dc bus utilization, such as the third-harmonic injection technique presented in Chapter 2, since these approaches increase the linear PWM region and therefore allow converters to produce higher $|V_I|$ than they otherwise could. However, these approaches are typically intended for balanced converter operation, and therefore may no longer be simply implemented when a converter supplies auxiliary services, since the magnitude, angle, and frequency of the injected component

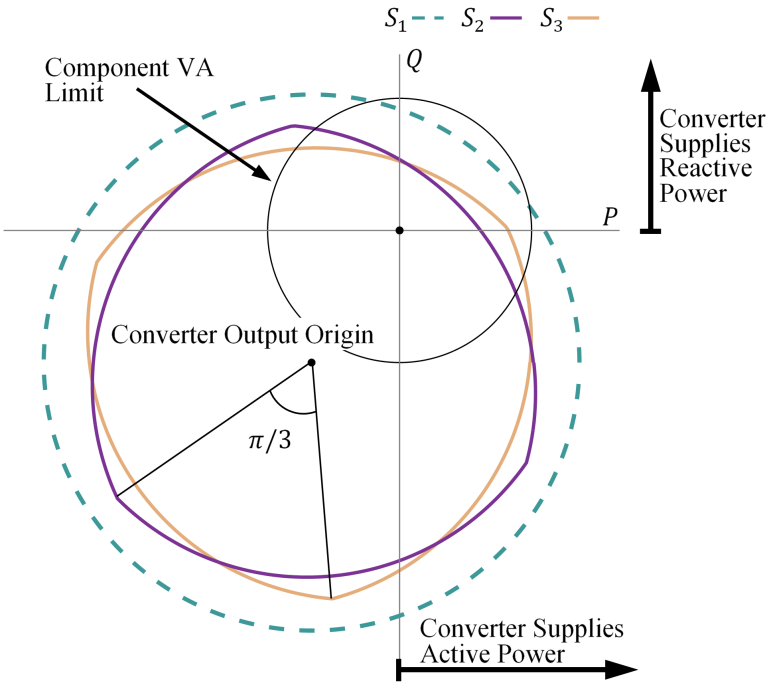


Fig. 4.1: PQ plane output region boundary for: no negative-sequence component (S_1); negative-sequence component $V_2\angle\theta$ (S_2); and negative-sequence component $V_2\angle(\theta+\pi/3)$ (S_3). An ideal component VA limit is included as a typical, though arbitrary, reference.

may need to be continually adjusted to ensure references stay within the linear PWM region. Accordingly, there is a need for a simple to implement technique which can maximize dc bus utilization regardless of any auxiliary services provided.

4.2 Common-Mode Component Generation

In this section, the proposed method for maximizing dc bus utilization by injecting PWM references with a common-mode component is explained in Subsection A. The PQ plane output region for CHB utilizing the proposed technique when providing negative-sequence compensation is presented in Subsection B.

4.2.1 Common-Mode Generation and Injection

Define $V_{dc,x}$ as the sum of isolated dc-input voltages for the healthy cells in leg $x \in \boldsymbol{P} = \{a, b, c\}$. Since the PWM reference, $v_x(t)$, defines the leg x line-to-neutral output for both symmetric and asymmetric CHB, linear-range modulation is ensured if $|v_x(t)| \leq V_{dc,x}$. Accordingly, references only need to be adjusted if there exists a voltage difference $u_x(t) = |v_x(t)| - V_{dc,x} > 0$ for $x \in \boldsymbol{P}$. Defining, at each time instant,

$$k = \underset{x \in \boldsymbol{P}}{\operatorname{argmax}} \left(u_x(t) \right), \tag{4.2}$$

the minimum magnitude common-mode voltage which ensures $|v_k(t)| \leq V_{dc,k}$ is computed as,

$$v_0(t) = \begin{cases} \operatorname{sign}\left(v_k(t)\right) u_k(t) & u_k(t) > 0 \\ 0 & \text{otherwise.} \end{cases} \tag{4.3}$$

The common-mode component computed via (4.3) is then used to generate modified PWM references as,

$$v_x^*(t) = v_x(t) - v_0(t), \quad x \in \boldsymbol{P}. \tag{4.4}$$

All $v_x^*(t)$ are guaranteed to be within the linear modulation range provided $|v_x(t) - v_y(t)| \leq V_{dc,x} + V_{dc,y}$ for all $x, y \in \boldsymbol{P}$. Extending the proposed method to the overmodulation region is not considered here.

Defining an $[a, b, c]$ CHB as having a healthy cells in Leg A, b healthy cells in Leg B, and c healthy cells in Leg C, a typical set of references containing positive- and negative-sequence components are shown in Fig. 4.2 before and after being adjusted for a $[3, 3, 3]$ CHB and a $[3, 2, 3]$ CHB. The adjusted references shown in Fig. 4.2 are clamped at each leg's maximum available dc bus voltage, thereby ensuring linear-range

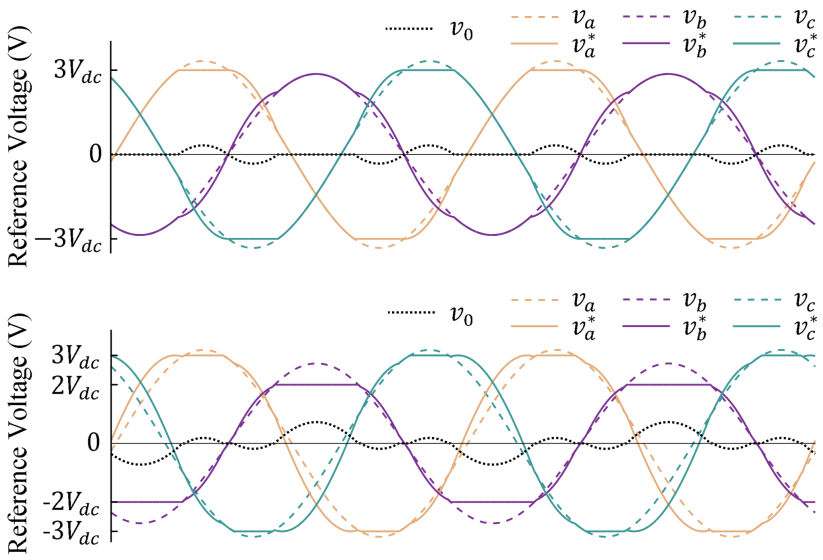


Fig. 4.2: Unadjusted PWM references containing a negative-sequence component, v_x, compared to Atypical PWM references, $v_x^* = v_x - v_0$, for a healthy [3,3,3] CHB (top), and a [3,2,3] CHB (bottom).

modulation. Note that the $v_o\,(t)$ waveform used to adjust references, also shown in Fig. 4.2, are significantly different from the waveforms typically used. That is, $v_o\,(t)$ is not a third harmonic component, as is typically used for balanced operation, nor is it a fundamental frequency component, as obtained using FPSC for CHB operation under internal fault conditions.

Since the proposed method is independent of the PWM technique utilized, this technique can be applied to symmetric and asymmetric CHBs with any number of faulty cells, provided $V_{dc,x}$ values are appropriately adjusted. Moreover, the proposed method does not directly produce references or gate signals, instead acting as an intermediary step between the creation of references and the generation of gate signals. Accordingly, the proposed method can be implemented using any reference generation, i.e. controller, technique and can be used with any carrier-based PWM scheme.

Since the positive-sequence component of references can be increased when a common-mode component is injected using the proposed technique, the maximum apparent

power the converter can supply is increased, neglecting the component VA limitations. Accordingly, utilization of this method modifies a converter's PQ plane output region, as discussed in the next subsection.

4.2.2 Modified PQ Plane Output Region

The proposed technique can be implemented for converters providing a wide range of auxiliary services, as well as for converters providing no auxiliary services at all. However, this subsection focuses on the case where the PWM references must contain a negative-sequence component, for instance to ensure balanced currents are drawn from traditional sources. Analysis of the converter's PQ plane output region is presented to demonstrate the efficacy of the proposed technique, since this representation provides a visualization of the range of $|V_I|$ a CHB can provide for all δ values. For all presented analyses the phase angle of the negative-sequence component is maintained at 0 radians, with respect to the grid's positive-sequence component. This simplification is permissible, without loss of generality, due to the understanding that any non-zero negative-sequence phase angle will predictably change the converter's PQ plane output region, causing the region to rotate about the converter's output origin as shown in Fig. 4.1.

Before examining the case where the converter supplies the negative-sequence compensation, the case where PWM references only contain positive-sequence content is considered. As explained in Section 4.1, the converter's output region always defines a disk in the PQ plane when references only contain positive-sequence content. To ensure a balanced three-phase system, the maximum line-to-line peak voltage attainable when using the proposed technique is equal to the sum of the two smallest leg voltages, i.e.

$$\hat{V}_{LL,max} = \sum_{x \in \boldsymbol{P}} V_{dc,x} - \max\left(V_{dc,a}, V_{dc,b}, V_{dc,c}\right). \tag{4.5}$$

Therefore, $\hat{V}_{LL,max} = 6$ for $[3,3,3]$ CHB, $\hat{V}_{LL,max} = 5$ for $[3,3,2]$ CHB, $\hat{V}_{LL,max} = 4$ for $[3,2,2]$ and $[2,2,2]$ CHB, and so on. The proposed atypical PWM technique enables these maximum line-to-line peak voltages to be obtained, since $v_o(t)$ can be produced to generate linear-range modulation provided $|v_x(t) - v_y(t)| = V_{dc,x} + V_{dc,y}$ for all $x, y \in \boldsymbol{P}$. Compared to the attainable line-to-line voltages provided using fundamental phase shift compensation as detailed in Chapter 2, the proposed technique enables greater dc bus utilization, extending the radius of the disk in the PQ plane defining the converter's output region. This extension is due to the fact that FPSC only utilizes a fundamental-frequency common-mode component, whereas the proposed technique does not have this restriction. Furthermore, balanced line-to-line voltages are attainable even if all cells within one leg are completely bypassed, e.g. $\hat{V}_{LL,max} = 3$ for a $[3,3,0]$ CHB.

When PWM references of a microgrid-interactive CHB must contain a negative-sequence component, the maximum line-to-line voltage which the converter can supply becomes dependent upon the angle of the phase shift between the grid and the inverter reference. That is, $\hat{V}_{LL,max}$, and hence the range of $|V_I|$, become dependent upon δ, and therefore the converter's output region may no longer define a disk in the PQ plane. For references containing a fixed negative-sequence component, Fig. 4.3 shows the PQ output region for an $M = 3$ cell CHB under various fault conditions. The PQ output regions in Fig. 4.3 are shown for a CHB utilizing the proposed atypical PWM scheme as well as for a CHB with no common-mode component. In each case, a circle centered at the converter's output origin is also included as a reference.

For the healthy $[3,3,3]$ CHB shown in Fig. 4.3(a), both the adjusted and unadjusted regions have 120° rotational symmetry, and use of the proposed atypical PWM

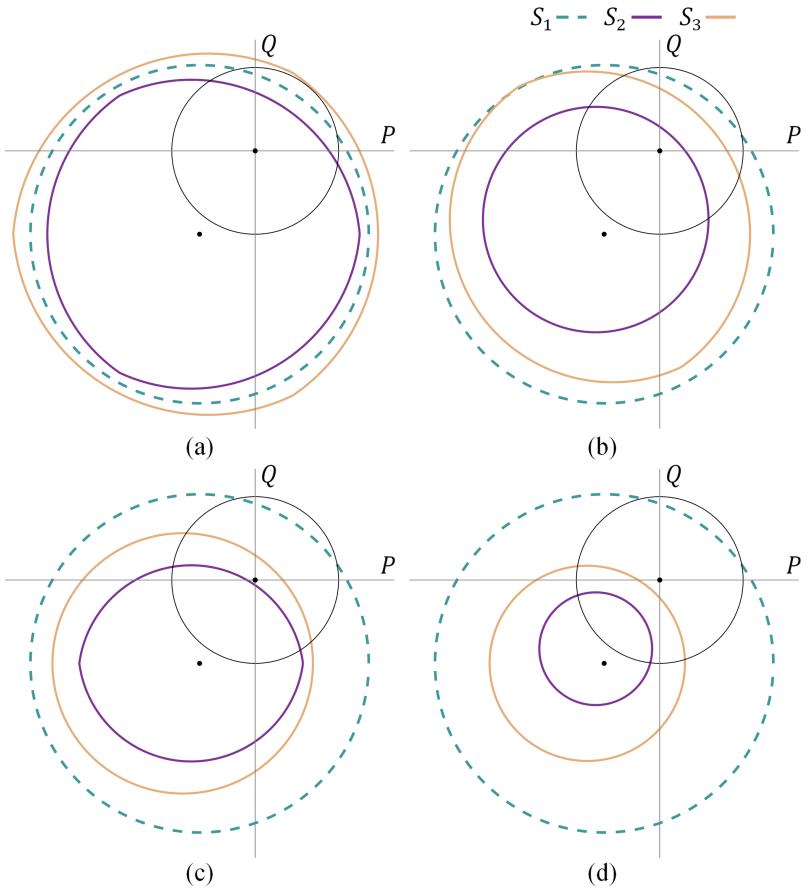


Fig. 4.3: CHB PQ plane output region when PWM references contain negative-sequence component $V_2\angle 0$ without any common-mode component (S_2) and using the proposed atypical PWM method (S_3) for: (a) healthy $[3, 3, 3]$ CHB, (b) $[3, 3, 2]$ CHB, (c) $[3, 2, 2]$ CHB, and (d) $[3, 2, 1]$ CHB. A circle, S_1, centered at the converter's operating origin is included for reference.

technique shows $\hat{V}_{LL,max}$ is increased for all δ, though the increase in $\hat{V}_{LL,max}$ is δ dependent. As faults occur and cells are bypassed in CHB legs, the PQ plane output region of a microgrid-interactive CHB may lose rotational symmetry for PWM references containing a negative-sequence component, though the CHB's PQ plane output region still rotates about the converter's output origin as the angle of the negative-sequence component changes. The regions shown in Fig. 4.3(b), (c), and (d) show that $\hat{V}_{LL,max}$ is increased for all δ when the proposed technique is utilized under cell fault conditions, although once again the increase in $\hat{V}_{LL,max}$ is δ dependent. Under some

circumstances, the CHB is only able to provide active-power at unity power factor if the proposed technique is used, as shown in Fig. 4.3(c). However, there are also some cases, such as shown in Fig. 4.3(d), where the CHB is unable to provide active-power at unity power factor regardless of whether the proposed method is utilized, though active-power may still be provided at a reduced power factor. Accordingly, the CHB becomes more fault tolerant when the proposed technique is used, as it can remain connected to a microgrid under a wider range of faults.

4.3 Experimental Verification

In this section, experimental data are presented to verify the proposed technique. For experimental verification, a CHB with $M = 3$ cells per leg was connected to the grid and an unbalanced 2 kW Y-connected load with $R_a = 24\,\Omega$, $R_b = 24\,\Omega$, and $R_c = 31\,\Omega$. The CHB was connected to the system using an LCL filter, with grid-side inductance L_{fG}, converter-side inductance L_{fI}, and Δ-connected capacitors C_f with series damping resistors R_f. System parameters are provided in Table 4.1. The experimental setup is shown in Fig. 4.4.

The active- and reactive-power delivered by the CHB were controlled via a PI controller in the dq frame, with a phase-locked loop (PLL) used to find ωt required for synchronization. For all data collected, the CHB was set to deliver $P = 500\,\mathrm{W}$

Table 4.1: Experimental Parameters

Line-to-Line Voltage	$208\,\mathrm{V_{rms}}$
Cells per Leg (M)	3
PWM Carrier Frequency	4.2 kHz
L_{fI}	1.5 mH
C_f (Δ)	5 µF
R_f	3.3 Ω
L_{fG}	1.0 mH

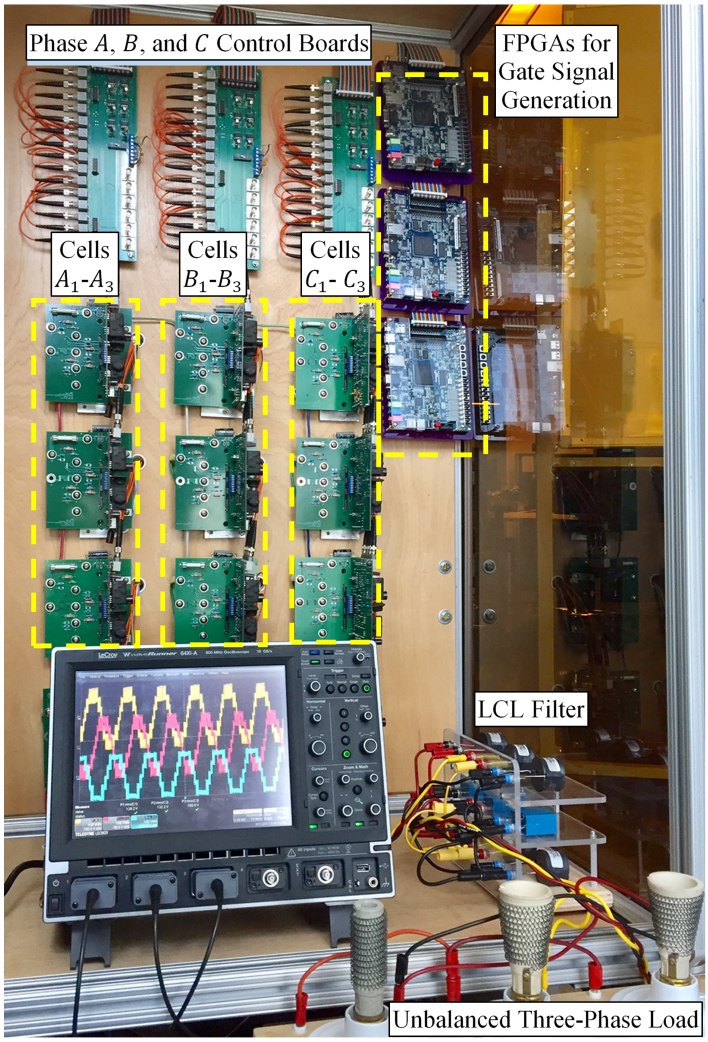


Fig. 4.4: Setup used for experimental verification.

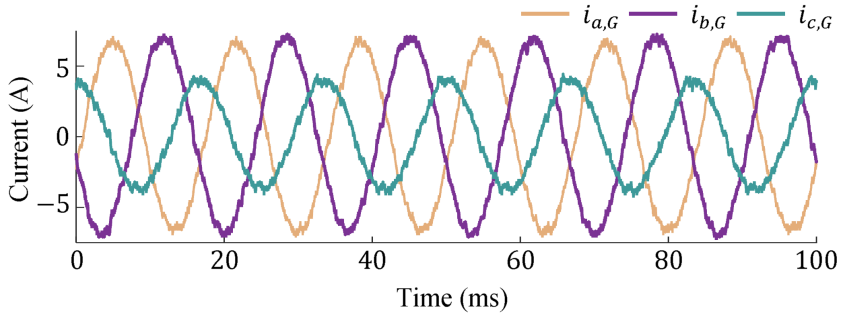


Fig. 4.5: Grid currents drawn by the converter and unbalanced load for $R_a = 24\,\Omega$, $R_b = 24\,\Omega$, and $R_c = 31\,\Omega$, when $V_{LL,rms} = 208\,\text{V}$, $MV_{dc} = 195\,\text{V}$, and the converter does not supply negative-sequence compensation.

and $Q = 0$. A dSPACE CP1103 control board was used to create PWM references, while gate signals were generated using LSPWM implemented via an Altera Cyclone V 5CSEMA5F31C6 FPGA [107]. Using a total leg dc bus voltage $MV_{dc} = 195\,\text{V}$, 65 V per cell, the grid current drawn by the system is shown in Fig. 4.5 when the converter did not provide any negative-sequence compensation. This unbalanced current can deleteriously affect microgrid-scale generators, therefore implementing negative-sequence compensation may be beneficial for the system.

Negative-sequence compensation was achieved by converting currents drawn from the grid into the negative-sequence dq frame, and then driving any negative-sequence component to zero using a PI controller. The signals for active- reactive-power control were added to the negative-sequence compensation controller. The proposed atypical PWM technique was applied to the resultant reference signals and LSPWM was again used for gate signal generation. A block diagram of the experimental setup is shown in Fig. 4.6. Before moving on, however, it is reemphasized that the proposed technique

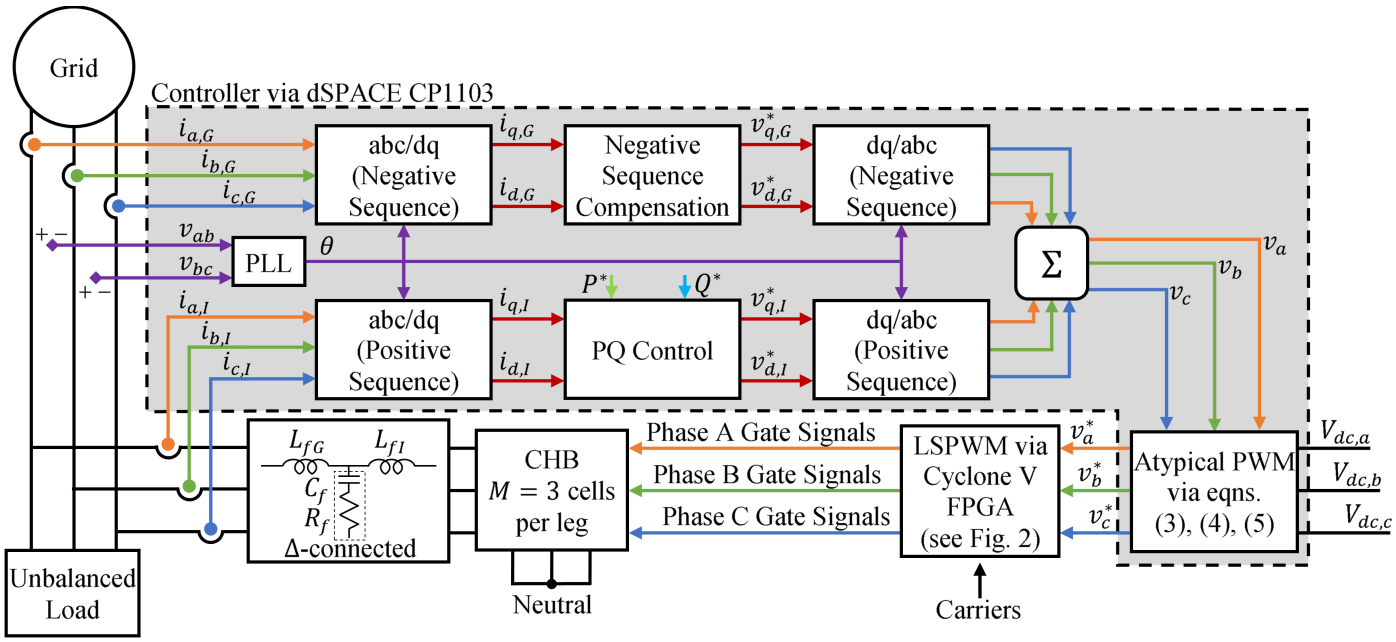


Fig. 4.6: Block diagram of the system used for experimental verification.

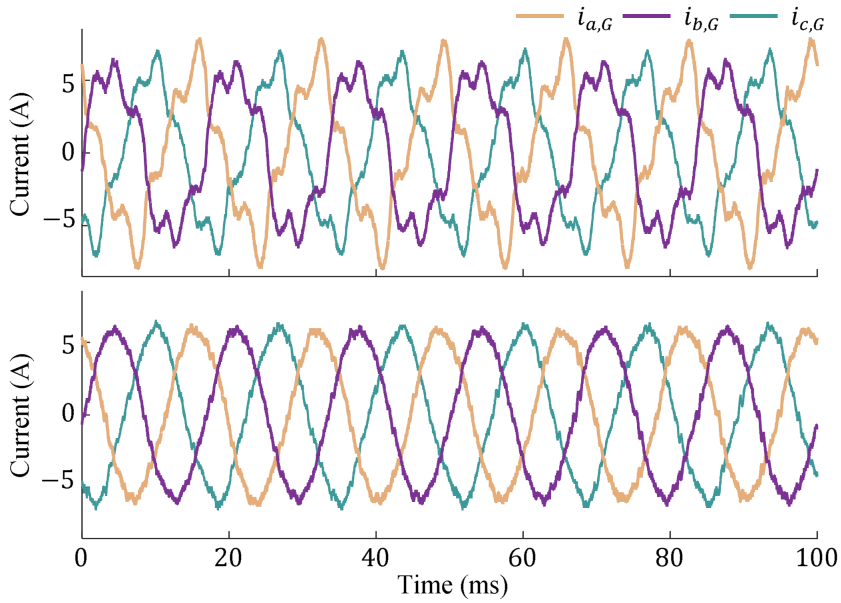


Fig. 4.7: Grid currents using total leg dc bus voltage $MV_{dc} = 160\,\text{V}$, obtained without (top) and with (bottom) the proposed atypical PWM scheme.

is independent of the control method utilized as well as the PWM scheme, provided it is a carrier-based approach.

With the PWM references generated to ensure balanced grid currents were drawn by the system, the total leg dc bus voltage of the converter, initially $MV_{dc} = 195\,\text{V}$, was decreased in 5 V steps until a minimum voltage of 150 V while ensuring cell source magnitudes remained equal. Currents drawn from the grid for $MV_{dc} = 160\,\text{V}$, with and without using the proposed atypical PWM technique, are shown in Fig. 4.7, clearly demonstrating that lower distortion is made possible if the proposed method is used. The results shown in Fig. 4.7 demonstate that if the proposed method is not used for the given conditions, either *(i)* the active-or reactive-power delivered by the converter must be changed, *(ii)* negative-sequence compensation must be removed, and/or *(iii)* the increased harmonic distortion must be accepted. Alternatively, it may be necessary to completely disconnect the converter from the grid if performance goals cannot be met.

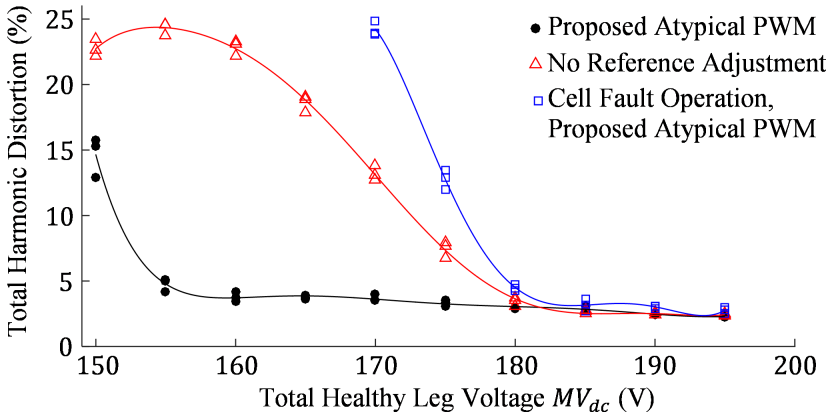


Fig. 4.8: Grid current THD vs. total leg dc bus voltage, MV_{dc}, with each dc bus voltage tested at three different measurement instants. For the case where a cell is faulty, MV_{dc} is the total dc bus voltage of a healthy leg.

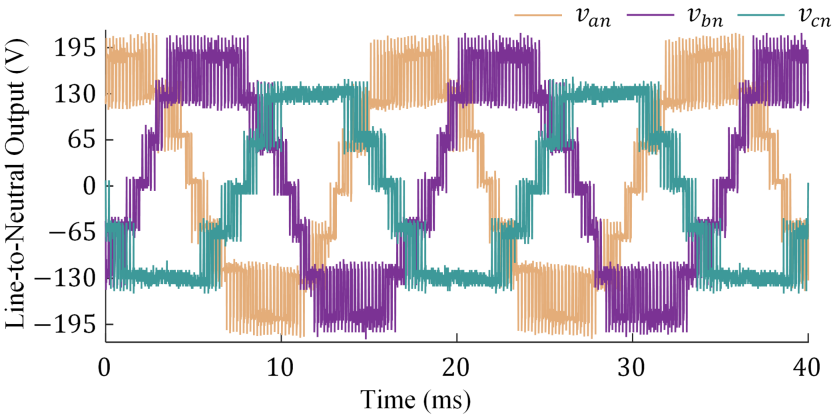


Fig. 4.9: Line-to-neutral PWM waveforms obtained when a leg C cell is bypassed using the proposed technique, and the total dc bus leg voltage of a healthy leg is $MV_{dc} = 195\,\text{V}$.

To analyze the system behavior over a wide range of voltages, the three line currents drawn from the grid for each MV_{dc} value were measured, both with and without utilizing the proposed atypical PWM method. The THD of the three phase currents were then computed and averaged for each MV_{dc}. To account for grid variations, measurements were made at three separate instants. The results, shown in Fig. 4.8, demonstrate that a baseline THD value can be maintained using lower MV_{dc} if the proposed atypical PWM technique is used. Data were also collected to show system performance for a CHB with a phase B cell bypassed, e.g. due to a fault. Under

cell fault conditions, the proposed technique generates line-to-neutral voltages such as shown in Fig. 4.9. The results shown in Fig. 4.8 demonstrate that, provided MV_{dc} is sufficiently large, the proposed atypical PWM technique enables continued converter operation even in the event of a cell fault.

4.4 Conclusion

In this chapter, an atypical PWM technique for maximizing dc bus utilization in microgrid-interactive CHB converters has been presented. The proposed method is implemented independently of any control techniques used, making it suitable for use in a wide range of applications. Moreover, this technique can be applied to any carrier-based PWM scheme, enabling its use for symmetric and asymmetric CHB. Finally, the proposed technique enables continued converter operation in the event of cell faults, provided the fault has been identified. The efficacy of the atypical PWM technique has been demonstrated under healthy and faulty conditions for balanced operation and when the CHB provides negative-sequence compensation, for instance to ensure that balanced currents are drawn from traditional sources. The common-mode component injected into PWM references is based on the available dc bus voltages and enables references to be adjusted in real-time, without requiring lookup tables. Ultimately, it has been demonstrated that the presented technique allows PWM references to contain greater positive-sequence components than they otherwise could and thereby enlarges the converter's PQ plane output region.

Chapter 5

Direct Utilization of Time-Variant DC Sources

Multilevel PWM schemes typically assume CHB cells are powered by time-invariant dc sources with equal magnitudes, or magnitudes existing in specific ratios, as detailed in Chapter 2. In this chapter, an adaptive sinusoidal PWM (ASPWM) technique which increases CHB flexibility by enabling time-variant dc sources to be directly utilized is presented. Two alternative algorithms for implementing the proposed ASPWM scheme are detailed in this chapter, providing system designers with a trade off between system performance and the number of sensors required for implementation. The first algorithm requires all cell input voltages to be measured, while the second algorithm only requires measurement of the leg's line-to-neutral output voltage. Accordingly, the first algorithm is referred to as the sensor-per-source (SPS) algorithm while the second algorithm is referred to as the sensor-per-leg (SPL) algorithm.

This chapter includes seven sections. A modified implementation of the conventional LSPWM technique, providing a foundation for ASPWM, is presented in Section 5.1. The SPS and SPL ASPWM algorithms are presented in Sections 5.2 and 5.3,

respectively. Simulation results which demonstrate the effectiveness of proposed algorithms are then presented in Section 5.4, and experimental verification is presented in Section 5.5. In Section 5.6, potential modifications to the steady-state behavior of both algorithms are proposed. Concluding remarks are given in Section 5.7.

5.1 Conventional Sinusoidal Pulse Width Modulation

Several PWM methods can be used to control the output of a CHB converter [4, 68], but the techniques presented in this chapter are most closely related to the LSPWM method introduced in Chapter 2. A modified method for implementing LSPWM, hereafter called conventional sinusoidal PWM (SPWM), is presented in this section to provide a foundation for the proposed ASPWM algorithms.

Conventional SPWM is used to provide gate signals to an M cell symmetric CHB leg by comparing a sinusoidal reference signal, $r(t) = m\sin(\omega t)$, to several triangular signals (carriers), $c_k(t)$, with fixed frequency f_c. For a CHB leg as shown in Fig.

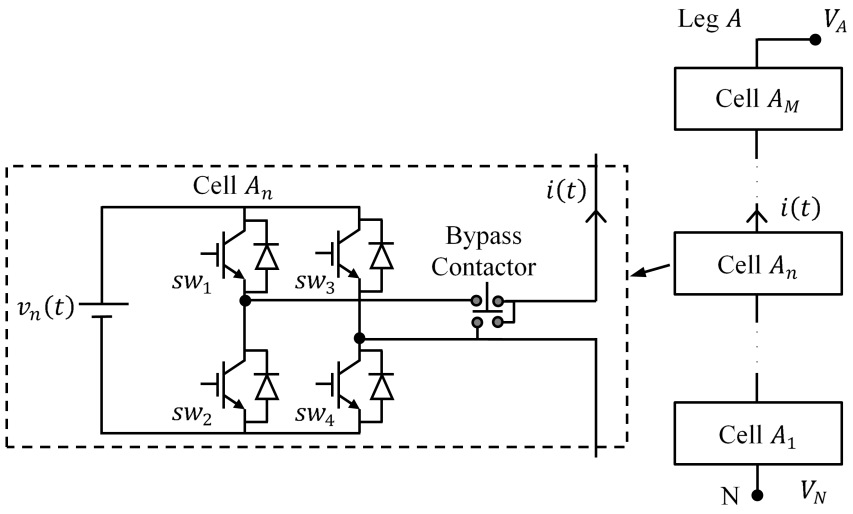


Fig. 5.1: A grid-interactive cascaded H-bridge multilevel converter.

Table 5.1: Cell A_n Switch Configurations, Output Voltages, and States

$[sw_1, sw_3]$	Cell Output Voltage	Cell State $s_n(t)$
$[0,0]$	0	0
$[0,1]$	$-v_n(t)$	-1
$[1,0]$	$v_n(t)$	1
$[1,1]$	0	0

5.1, define the leg-state as the row vector of cell states, $S(t) = [s_1(t), \ldots, s_M(t)]$, where states are defined as shown in Table 5.1. Since each $s_i(t) \in \{1, 0, -1\}$ there are 3^M distinct leg states, i.e. $S(t) \in \{S_1, S_2, \ldots, S_{3^M}\}$. Defining the cell voltage vector as the column vector $\bar{v}(t) = [v_1(t), \ldots, v_M(t)]^{\mathrm{T}}$, the line-to-neutral output voltage of the leg is found as $V_{ph}(t) = S(t)\,\bar{v}(t)$. In conventional SPWM, the modulation index, m, is defined as $m = \hat{v}_{out}/(MV_{dc})$, for a desired peak output voltage, $\hat{v}_{out}$, assuming equal input dc sources, i.e. $v_i(t) = V_{dc}$ for $i \in \{1, 2, \ldots, M\}$. An approach for implementing SPWM with a purely sinusoidal reference is to choose $r(t) = \sin(\omega t)$, and control the range of the carriers using m. This approach provides the base needed for implementing the adaptive SPWM algorithm for time-variant dc sources. In this technique, $M + 1$ carriers are considered such that $c_0(t) = 0$ and for the remaining carriers, range$(c_k(t)) = [\alpha_{k-1}, \alpha_k]$, where $\alpha_k = k/(mM)$. Defined in this way, carriers are non-overlapping, occupy the region between 0 and $1/m$, and have equal magnitudes. Finally, if the set

$$C = \{k \mid c_k(t) \leq |r(t)|\} \tag{5.1}$$

is defined for each time instance, then the number of cells outputting a non-zero voltage at time $t + \Delta t$ is found as $\max(C)$, and sign$(r(t))$ is used to determine whether non-zero cell states are positive or negative. An example showing the references, carriers, and unfiltered line-to-neutral output obtained using this PWM scheme for a two-cell CHB are shown in Fig. (5.2).

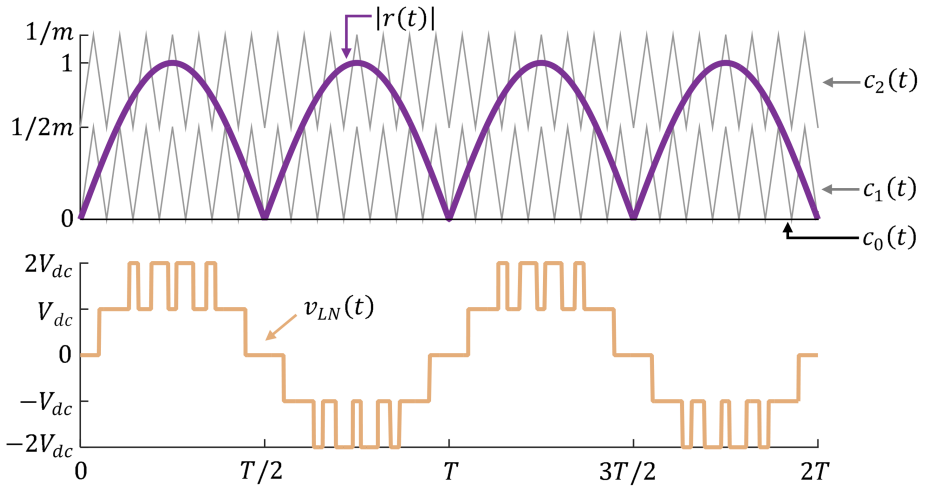


Fig. 5.2: Reference and carrier waveforms (top) and converter line-to-neutral output (bottom) obtained using conventional SPWM, assuming $r\left(t\right) > 0$ for $t \in (0, T/2) \cup (T, 3T/2)$, and $r(t) < 0$ otherwise.

This conventional SPWM technique requires all cell voltage magnitudes to be equal, known in advance, and time-invariant. The adaptive algorithms proposed in Sections 5.2 and 5.3 eliminate these restrictions.

5.2 Sensor-Per-Source Algorithm

The SPS algorithm, outlined in Fig. 5.3, is introduced in this section. For this implementation of adaptive SPWM, every element of the cell voltage vector, $\bar{v}\left(t\right) = \left[v_1\left(t\right), \ldots, v_M\left(t\right)\right]^{\mathrm{T}}$, must be measured in real-time. To simplify the analysis of steady-state behavior it is assumed that all permissible voltages are unique, i.e.

$$\left|S_i\bar{v}\left(t\right) - S_k\bar{v}\left(t\right)\right| > \epsilon > 0 \quad \text{for} \quad i \neq k. \tag{5.2}$$

With this assumption, the SPS algorithm initializes by finding and storing all $(S_k, S_k\bar{v}\left(t\right))$ (leg-state leg-voltage) pairs such that $S_k\bar{v}\left(t\right) \geq 0$. Since (5.2) is satisfied, there will be $N = \left(3^M + 1\right)/2$ such pairs. With the switching states indexed as

$$0 = S_0 \bar{v}\left(t\right) < \cdots < S_{N-1} \bar{v}\left(t\right), \tag{5.3}$$

define the modulation index using the desired peak output voltage and the maximum voltage which can be generated by the converter

$$m = \frac{\hat{v}_{out}}{S_{N-1} \bar{v}\left(t\right)} \tag{5.4}$$

and generate N carriers such that $c_0\left(t\right) = 0$, and for the remaining carriers

$$\text{range}\left(c_k\left(t\right)\right) = \left[\alpha_{k-1}, \alpha_k\right] \tag{5.5}$$

where α_k is given by

$$\alpha_k = \frac{S_k \bar{v}\left(t\right)}{m S_{N-1} \bar{v}\left(t\right)}. \tag{5.6}$$

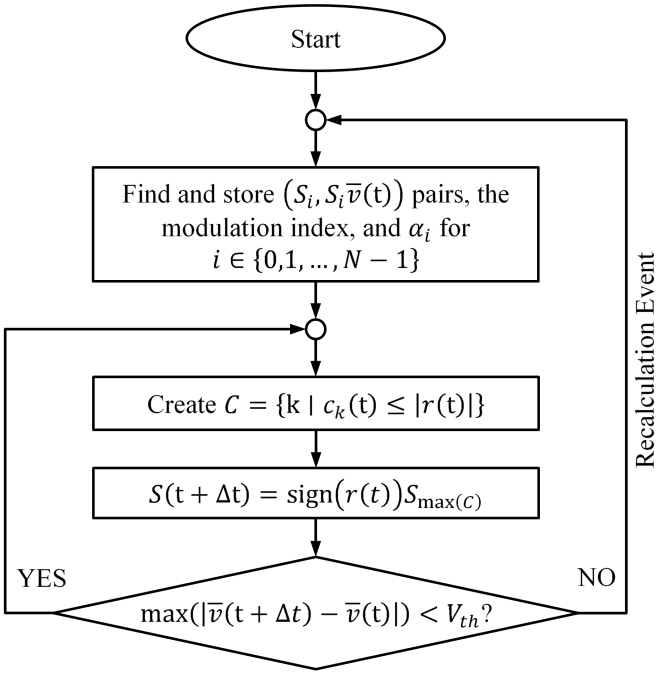


Fig. 5.3: Flowchart of SPS adaptive SPWM.

With these values stored, the initialization event is finished, and the algorithm's steady-state behavior begins. Similar to conventional SPWM, during steady-state behavior SPS adaptive SPWM sets the converter's leg state at time $t + \Delta t$ using the set defined in (5.1) as,

$$S\left(t + \Delta t\right) = \text{sign}\left(r\left(t\right)\right) S_{\max(C)}. \tag{5.7}$$

The algorithm proceeds by determining if

$$\max\left|\bar{v}\left(t + \Delta t\right) - \bar{v}\left(t\right)\right| < V_{th}, \tag{5.8}$$

where V_{th} is a predefined perturbation threshold, with a magnitude set to avoid unnecessary recalculation events while also ensuring an acceptable output. The magnitude of V_{th} is primarily limited by instrumentation used for measurements. If a greater resolution, i.e. a small V_{th}, is desired then either the range of measured voltage must be limited, limiting the range of cell voltage inputs which can be used, or more accurate measurements must be made, which may increase system costs.

If (5.8) is satisfied, then stored values are used to define C for the next time step. If (5.8) is not satisfied, however, then a recalculation event, identical to initialization, is triggered, leading to the recalculation of $(S_k, S_k\bar{v}\left(t\right))$ pairs, the modulation index, and α_k values. This scheme avoids unnecessary recalculations, with recalculation events occurring only if a significant cell voltage deviation is detected.

An example illustrating the SPS algorithm implementation of adaptive SPWM for an asymmetric two-cell ($M = 2$) CHB satisfying (5.2) is shown in Fig. 5.4. Initially in this example $v_1\left(t\right) = v_1$ and $v_2\left(t\right) = v_2$, where $v_1 > v_2$. As such the $N = 5$ ordered leg states are $S_0 = [0, 0]$, $S_1 = [1, -1]$, $S_2 = [0, 1]$, $S_3 = [1, 0]$, and $S_4 = [1, 1]$, and the corresponding leg voltages are 0, $v_1 - v_2$, v_2, v_1, and $v_1 + v_2$. For the desired peak output

voltage $\hat{v}_{out}$, the modulation index is defined via (5.4) as $m = \hat{v}_{out}/(v_1 + v_2)$. Using the modulation index and the $(S_k, S_k\bar{v}(t))$ pairs, N α_i values are calculated via (5.6) as $\alpha_0 = 0$, $\alpha_1 = (v_1 - v_2)/\hat{v}_{out}$, $\alpha_2 = v_2/\hat{v}_{out}$, $\alpha_3 = v_1/\hat{v}_{out}$, and $\alpha_4 = (v_1 + v_2)/\hat{v}_{out}$. Finally, carriers are generated with $c_0 = 0$ and for the remaining carriers the ranges are set according to (5.5). Thus, for a triangular waveform, $T(t)$, with range $(T(t)) = [0, 1]$, the carriers are defined as $c_i(t) = (\alpha_i - \alpha_{i-1})T(t) + \alpha_{i-1}$ for $i \in \{1, 2, 3, 4\}$. Defined in this way carrier signals are non-overlapping, occupy the region between 0 and $1/m$, and the amplitude of each carrier is directly proportional to the difference between adjacent leg voltages. With the carriers defined, the leg state for a given time step is selected using (5.1) and (5.7). The α_i values are stored and used to compute the carriers until, during the third half cycle, the magnitude of $v_1(t)$ abruptly decreases to v_1' such that (5.8) is not satisfied and a recalculation event is triggered. During the recalculation event the leg-state leg-voltage pairs, the modulation index, and the α_i values are recomputed as they were during initialization. Once the new values are stored the recalculation event is executed and steady-state behavior resumes with the carrier signals appropriately adjusted.

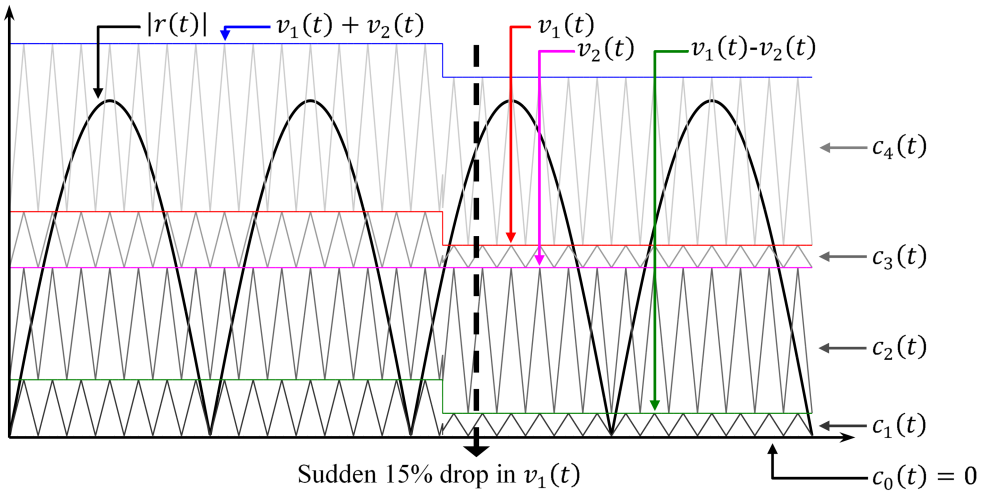


Fig. 5.4: Example showing SPS adaptive SPWM where a recalculation event is triggered during the third half-cycle.

5.3 Sensor-Per-Leg Algorithm

The SPS algorithm requires constant real-time measurement of every cell input voltage, and therefore requires several voltage sensors. These essential sensors increase the number of components used in the converter, negatively impacting the overall reliability [43, 108] and cost. As such, an alternate algorithm which requires fewer sensors may be desirable. Accordingly the SPL algorithm, outlined in Fig. 5.5, is now presented. This method only requires measurement of the converter leg's line-to-neutral voltage, $v_{ph}(t)$, making implementation possible using one voltage sensor per leg.

During SPL algorithm initialization the elements of the cell voltage vector, $\bar{v}(t) = [v_1(t), \ldots, v_M(t)]^{\mathrm{T}}$, are not known. Using a single sensor, $v_{ph}(t)$ is measured and stored for M non-trivial, linearly independent recalculation leg-states $S^{(1)}, \ldots, S^{(M)}$, where $S^{(i)} = [s_1^{(i)}, s_2^{(i)}, \ldots, s_M^{(i)}]$ with $s_k^{(i)} \in \{-1, 0, 1\}$ the state of cell k under recalculation leg-state i.

To expedite the speed with which the recalculation leg-states are applied, a recalculation state period, T_r, is defined. A small value of T_r is desired to reduce the duration of recalculation events, and since this value only plays a role during recalculation events it will be primarily limited by processor speed, analog-to-digital converters, etc. During initialization, the converter's leg state is set as $S^{(k)}$ for a complete recalculation state period, after which $v_{ph}(t)$ is measured and stored in the $M \times 1$ vector V_{ph} and the switching state is changed from $S^{(k)}$ to $S^{(k+1)}$. After M recalculation state periods, the cell voltage vector is calculated as

$$\bar{v}(t) = \begin{bmatrix} s_1^{(1)} & s_2^{(1)} & \cdots & s_M^{(1)} \\ s_1^{(1)} & s_2^{(2)} & \cdots & s_M^{(2)} \\ \vdots & \vdots & \ddots & \vdots \\ s_1^{(1)} & s_2^{(M)} & \cdots & s_M^{(M)} \end{bmatrix}^{-1} \begin{bmatrix} V_{ph}(1) \\ V_{ph}(2) \\ \vdots \\ V_{ph}(M) \end{bmatrix}, \tag{5.9}$$

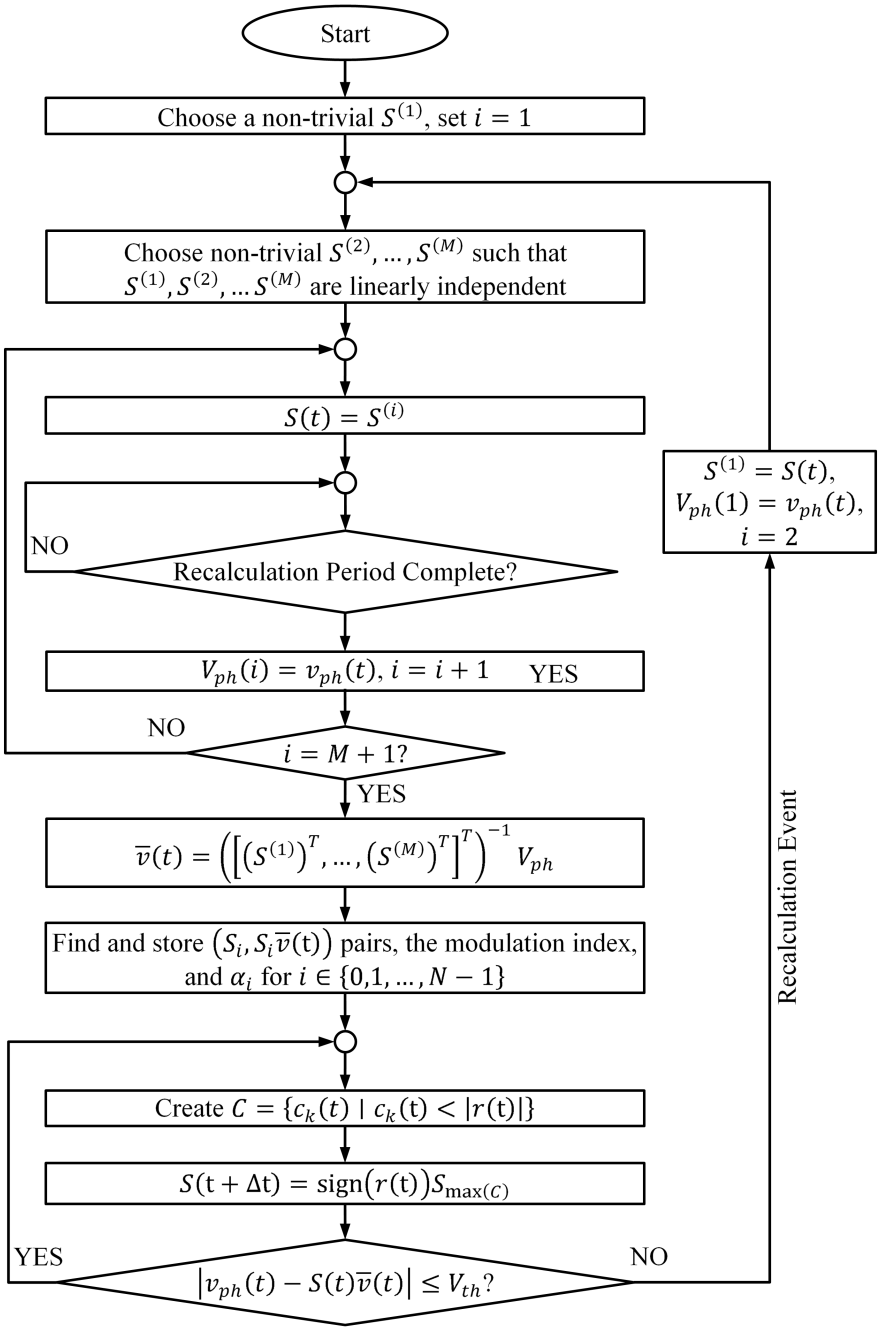


Fig. 5.5: Flowchart of SPL adaptive SPWM.

where the recalculation leg states are chosen to be non-trivial and linearly independent, thereby ensuring the matrix in (5.9) will never be singular. Once the cell voltage vector is calculated the SPL algorithm proceeds similarly to the SPS algorithm. That is, with the cell voltage vector known the algorithm finds $(S_k, S_k\bar{v}(t))$ pairs and sorts them according to (5.3), where (5.2) is again assumed. Using the $(S_k, S_k\bar{v}(t))$ values the modulation index and α_i values are computed according to (5.4) and (5.6). With the computed values stored, the initialization event is finished and the algorithm's steady-state behavior begins.

During steady-state behavior SPL adaptive SPWM behaves identically to the SPS algorithm, with $N = \left(3^M + 1\right)/2$ triangular carriers defined using the α_i values such that $c_0 = 0$ and (5.5) is satisfied for the remaining carriers. Next, the converter's leg-state at time $t + \Delta t$ set according to (5.7) where C is generated as in (5.1). The SPL algorithm proceeds by verifying that the measured leg line-to-neutral output voltage is close to the stored leg voltage corresponding to the current leg-state, i.e.

$$|v_{ph}(t) - S(t)\,\bar{v}(t)| < V_{th}, \tag{5.10}$$

where V_{th} is again a predefined perturbation threshold. As with the SPS algorithm, the magnitude of V_{th} is primarily limited by instrumentation used for measurements. The voltage range required to be measured for the SPL algorithm is larger than the range required to be measured for the SPS algorithm, as the SPL algorithm must measure the range from $-\hat{V}_{ph}$ to $+\hat{V}_{ph}$, where $\hat{V}_{ph}$ is the maximum phase voltage generated by the converter. Accordingly, V_{th} must either be larger for the SPL algorithm than for the SPS algorithm or measurements with higher resolutions must be implemented.

If (5.10) is satisfied, then stored $(S_k, S_k\bar{v}(t))$ are used to define C for the next time step. If (5.10) is not satisfied, however, then a recalculation event is triggered. Recalcu-

lation events are identical to the initialization event except that the first recalculation leg-state and output voltage are set to the leg state and voltage which triggered the recalculation event, i.e. $S^{(1)} = S(t)$, $V_{ph}(1) = v_{ph}(t)$. The remaining $M-1$ non-trivial recalculation leg-states are chosen such that $S^{(1)}, S^{(2)}, \ldots, S^{(M)}$ are linearly independent. After $M-1$ recalculation state periods the cell voltage vector is calculated according to (5.9). With the computed cell voltage vector the $(S_k, S_k\bar{v}(t))$ pairs, the modulation index, and the α_i values are recalculated. With the recalculated values stored the recalculation event is completed and the algorithm's steady-state behavior resumes.

An example illustrating the SPL algorithm implementation of adaptive SPWM for an asymmetric two-cell ($M = 2$) CHB satisfying (5.2) is shown in Fig. 5.6. The behavior of the cell input voltages for this example are the same as in the example presented in Section 5.2. At the start of the example the cell input voltages are unknown, so an initialization event occurs. The non-trivial, linearly independent recalculation leg-states are selected as $S^{(1)} = [-1, 0]$ and $S^{(2)} = [0, 1]$, and the converter's leg-state is immediately set to $S^{(1)}$. After one complete recalculation state period (one sawtooth period in the figure) the output voltage is measured and stored as $V(1) = -v_1$, and the converter's leg-state is changed to $S^{(2)}$. After a second recalculation state period the output voltage is measured and stored as $V(2) = v_2$. With these values, the cell voltage vector is found using (5.9) as

$$\bar{v}(t) = \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix}^{-1} \begin{bmatrix} -v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}.$$

Once the cell voltage vector is known the $N = 5$ $(S_k, S_k\bar{v}(t))$ pairs, the modulation index, and the α_i values are computed as described in example presented in Section 5.2. With these values stored the recalculation event is finished and steady-state behavior

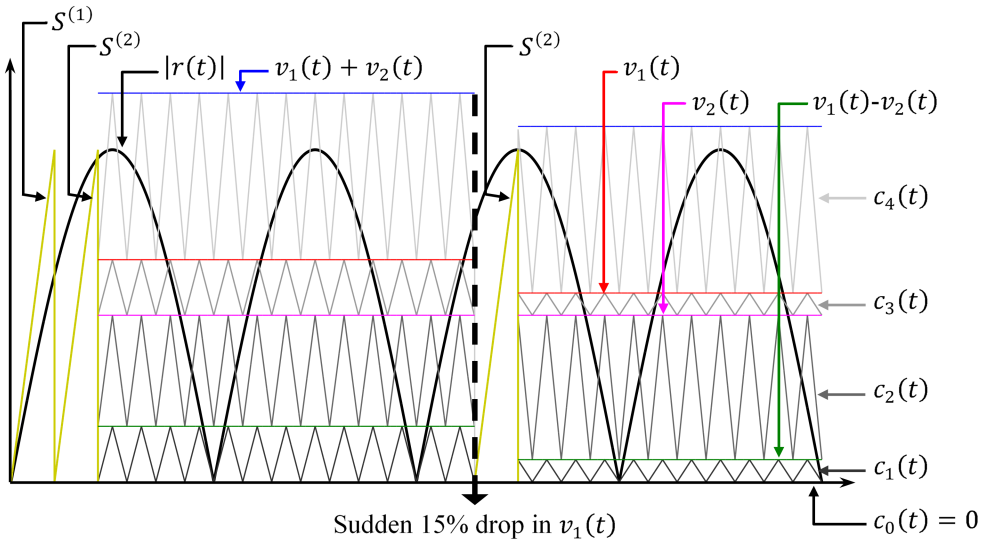


Fig. 5.6: Example showing SPL adaptive SPWM with an initialization event as well as a recalculation event in the third half-cycle, with recalculation periods shown as one period of a sawtooth waveform.

begins.

The stored values are used to generate carriers until, during the third half cycle, the magnitude of $v_1(t)$ abruptly decreases to v_1' such that (5.10) is not satisfied and a recalculation event is triggered. The converter's leg state and leg voltage when the recalculation event is triggered are $S(t) = [1, 0]$ and $v(t) = v_1'$, thus $S^{(1)} = [1, 0]$ and $V(1) = v_1'$. For this recalculation event the remaining recalculation leg-state is chosen as $S^{(2)} = [1, 1]$, and the converter's leg-state is immediately changed to $S^{(2)}$. After a complete recalculation state period the leg's output voltage is stored as $V(2) = v_1' + v_2$. With these values the cell voltage vector is found using (5.9) as

$$\bar{v}(t) = \begin{bmatrix} -1 & 0 \\ 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_1' \\ v_1' + v_2 \end{bmatrix} = \begin{bmatrix} v_1' \\ v_2 \end{bmatrix}.$$

Once the cell voltage vector is known the $N = 5$ $(S_k, S_k\bar{v}(t))$ pairs, the modulation index, and the α_i values are recalculated as described in example presented in Section

5.2. With these values stored the recalculation event is completed and steady-state behavior resumes.

When using SPL adaptive SPWM the $\bar{v}(t)$ calculation will fail, i.e. an incorrect result will be obtained, if the input voltages vary significantly during measurement. Such a failure would cause a second recalculation event as (5.10) would not be satisfied. For instance, suppose during the recalculation event in the previous example that v_1' changed to v_1'' before the end of the recalculation period. Such a variation would change the calculated cell voltage vector as

$$\bar{v}(t) = \begin{bmatrix} -1 & 0 \\ 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_1' \\ v_1'' + v_2 \end{bmatrix} = \begin{bmatrix} v_1' \\ -v_1' + v_1'' + v_2 \end{bmatrix}.$$

This cell voltage vector would be used to compute $(S_k, S_k\bar{v}(t))$ pairs, the modulation index, and the α_i values. However, because the true cell voltage vector is $\bar{v}(t) = [v_1'', v_2]^{\mathrm{T}}$ the output voltages produced by the converter will differ from the stored values. If this difference is large enough then (5.10) will not be satisfied and so a second recalculation event would be triggered.

Finally, note that when using the SPL algorithm as outlined in Fig. 5.5 the output line-to-neutral voltage of a CHB converter leg during a recalculation event is determined only by the recalculation leg-states selected and hence independent of the reference. Accordingly, when selecting $S^{(1)}, \ldots, S^{(M)}$ available information should be used in an effort to minimize the error between the converter's output and the reference. In addition to proper selection of recalculation states when using SPL adaptive SPWM, the impact of recalculation events can be modified by making adjustments to T_r such that the voltage generated during recalculation is made dependent upon the reference. One strategy is to increase T_r for one recalculation state to make the average voltage during recalculation approximately equal to $\hat{v}_{out}r(t)$ at the time the recalculation event

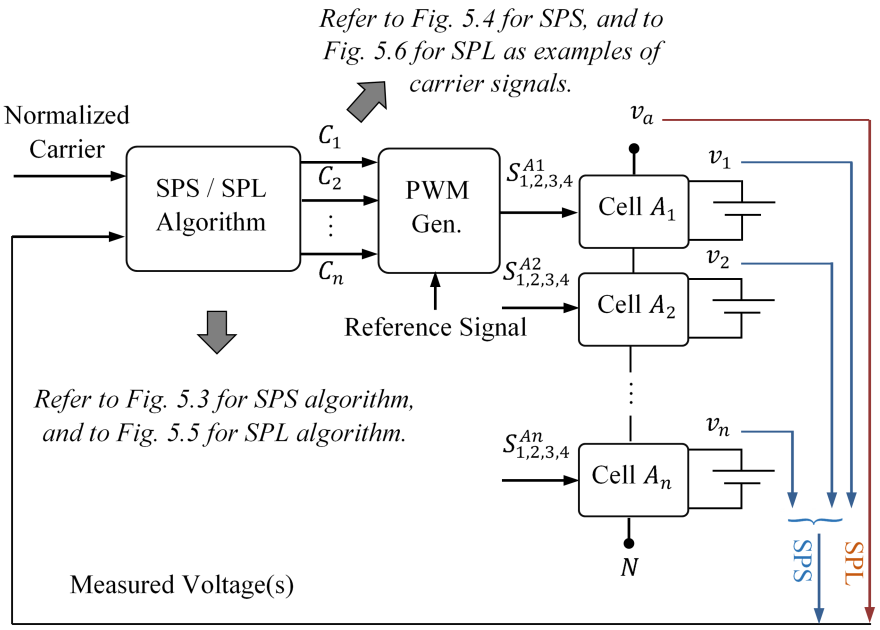


Fig. 5.7: Block diagram representation of the SPS and SPL algorithms, allowing a given reference signal to be more accurately followed using available sources.

is initialized.

A block diagram representation of both the SPS and SPL algorithms is shown in Fig. 5.7. Both proposed adaptive SPWM algorithms require the appropriate measurement voltage(s) and a normalized carrier waveform to generate scaled and shifted carriers $C_1, \ldots C_n$. These generated carriers are then compared with a reference voltage to generate PWM waveforms used to control each cell in a converter. The SPS or SPL algorithms allow a given reference waveform to be accurately followed using the available dc sources even though neither algorithm is used to generate a reference.

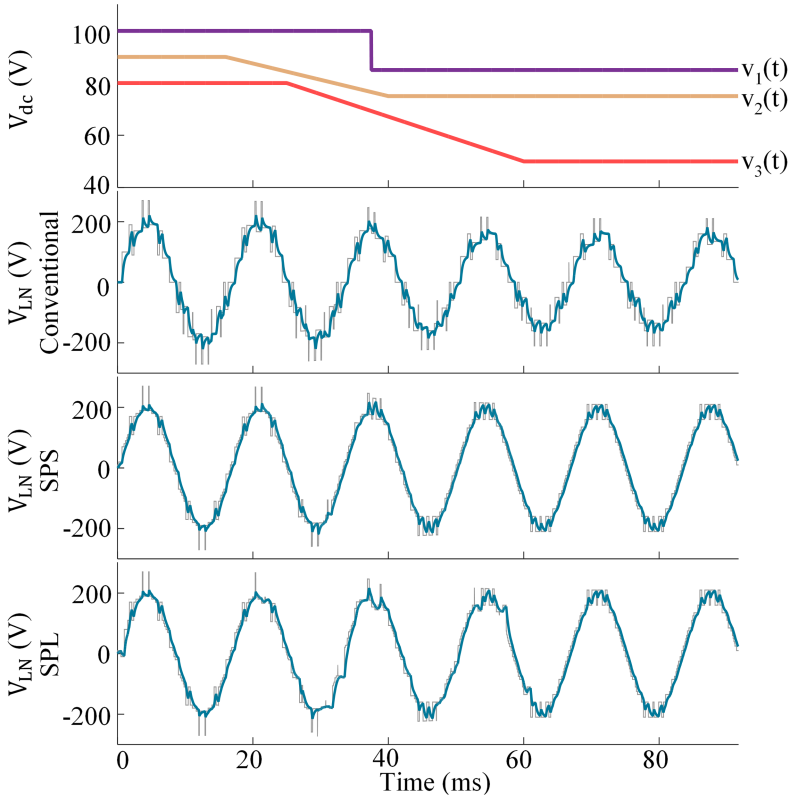
5.4 Performance Analysis with Varying Cell Voltages

In this section, the dynamic and steady-state performances of the SPS and SPL adaptive SPWM algorithms are compared using simulation results. For the first simulation presented, a single-phase CHB converter was considered with model parameters chosen as shown in Table 5.2, where parameters were selected to allow an example to be demonstrated. Note that the inverter's load does not have a significant impact on the behavior of either the SPS or SPL algorithms, as the measurements required for algorithm implementation are load independent thereby making the algorithms load independent as well.

In Fig. 5.8, simulation results showing cell voltages as well as the filtered and unfiltered converter output voltages are given for the SPS and SPL algorithms, and in Table 5.3 the steady-state performance of the algorithms before and after the simulated cell input voltage changes is provided. Further, to provide a reference for performance results obtained using conventional SPWM are also provided in Fig. 5.8 and Table 5.3. For the waveform generated by conventional SPWM, V_{dc} was made equal to the average value of v_1, v_2, and v_3 at initialization. The first-on, first-off strategy, outlined in Chapter 2, was used while implementing conventional SPWM. Using this method, cells in a CHB leg are switched in a rotating pattern using an ordered cyclic cell list

Table 5.2: Simulation Parameters

$\hat{v}_{out}r\,(t)$	$200\sin(2\pi 60t)$ V
M	3
f_P	1.08 kHz
T_r	500 µs
V_{th}	3 V
Load	10 Ω in series with 3 mH



6.1

Fig. 5.8: Cell voltages (top) used to generate converter unfiltered output voltages (gray) and filtered load voltages (blue) for conventional SPWM, SPS adaptive SPWM, and SPL adaptive SPWM algorithms using simulation parameters shown in Table 5.2.

Table 5.3: Analysis of Simulation Steady-State Behavior Before and After Cell Input Voltage Changes Shown in Fig. 5.8

	Conventional		SPS		SPL	
	Before	After	Before	After	Before	After
Line-To-Neutral Output Voltage Fundamental Component (peak)	199	156	198	197	198	197
THD (%)	9.95	12.49	5.08	4.36	5.09	4.36

with a turn-on and turn-off position. Initially the turn-on and turn-off position are the same, i.e. both markers are placed at cell x, but when the magnitude of the leg's line-to-neutral output voltage is to be increased the cell indicated by the turn-on marker is activated and the turn-on marker advances to the next cell in the cycle. Similarly, when the magnitude of the leg's line-to-neutral output voltage is to be decreased the cell

indicated by the turn-off marker is deactivated and the turn-off marker advances to the next cell in the cycle. The results in Fig. 5.8 show the filtered waveform produced using conventional SPWM has significant harmonic content and a peak value which varies with the input voltages, clearly demonstrating the shortcomings of using conventional SPWM with asymmetric, time-variant sources. The results presented in Table 5.3 show that during steady-state, the 20% decrease in cell input voltages produces a 20% decrease in peak measured fundamental voltage, and the increased asymmetry of the cell voltages produces an increased THD.

When using either the SPS or the SPL implementation of adaptive SPWM the output voltage produced remains regulated and harmonic content is reduced, as shown in Fig. 5.8 and Table 5.3. To achieve this behavior, both algorithms required initialization recalculation events. Due to the rapidly varying cell voltages in this example, 12 recalculation events and an initialization event were required when using the SPS algorithm, whereas the SPL algorithm required 13 recalculation events as well as an initialization event. For SPL recalculation events, the leg-states selected as recalculation leg states are those which produced voltages closest to the reference using stored values.

As shown in Fig, 5.8, some SPL recalculation events are accompanied by the waveform produced deviating from the desired waveform. To understand this temporary decline in performance when using the SPL algorithm, the recalculation state period T_r must be considered. Using the parameters detailed in Table 5.2, the simulation results shown in Fig. 5.9 were obtained for the SPL algorithm with $T_r = 500\,\mu s$, $250\,\mu s$, and $125\,\mu s$. Note that the plot for $T_r = 500\,\mu s$ is shown both as the bottom plot of Fig. 5.8 and the top plot of Fig. 5.9. From Fig. 5.9 it is clear that recalculation events are less evident for lower T_r values. This result is due to the fact that the average line-to-neutral leg output voltage during recalculation is independent from the reference, so by

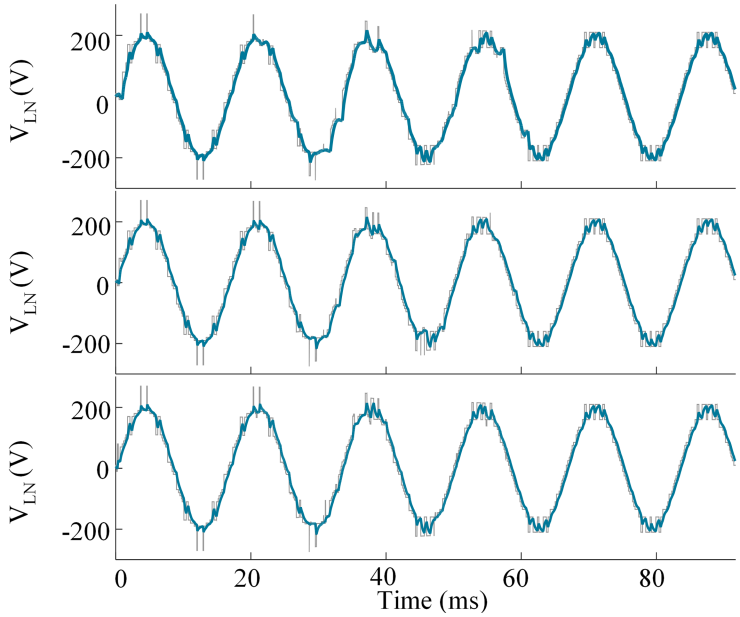


Fig. 5.9: Comparison of unfiltered output voltages (gray) and filtered load voltages (blue) generated via SPL adaptive SPWM for $T_r = 500\,\mu s$ (top), $250\,\mu s$ (middle), and $125\,\mu s$ (bottom) using simulation parameters shown in Table 5.2.

reducing T_r the duration during which this independent voltage is applied is reduced. It is worth reemphasizing that T_r only plays a role during recalculation events, so T_r does not have any impact on switching losses during steady-state. Accordingly, the value of the T_r is restricted by the speed of the processor and other hardware.

5.5 Experimental Verification

In this section, experimental results verifying the proposed algorithms are presented. To provide a reference, experimental results are also presented for conventional SPWM implemented using the first-on, first-off strategy, where both cell voltages are assumed to be 120 V. One leg of the three-phase two-cell CHB shown in Fig. 5.10 was used for experimental verification. An Altera EP3C16F484C6 FPGA was used to implement all algorithms [107]. All voltage measurements were made using sensors consisting

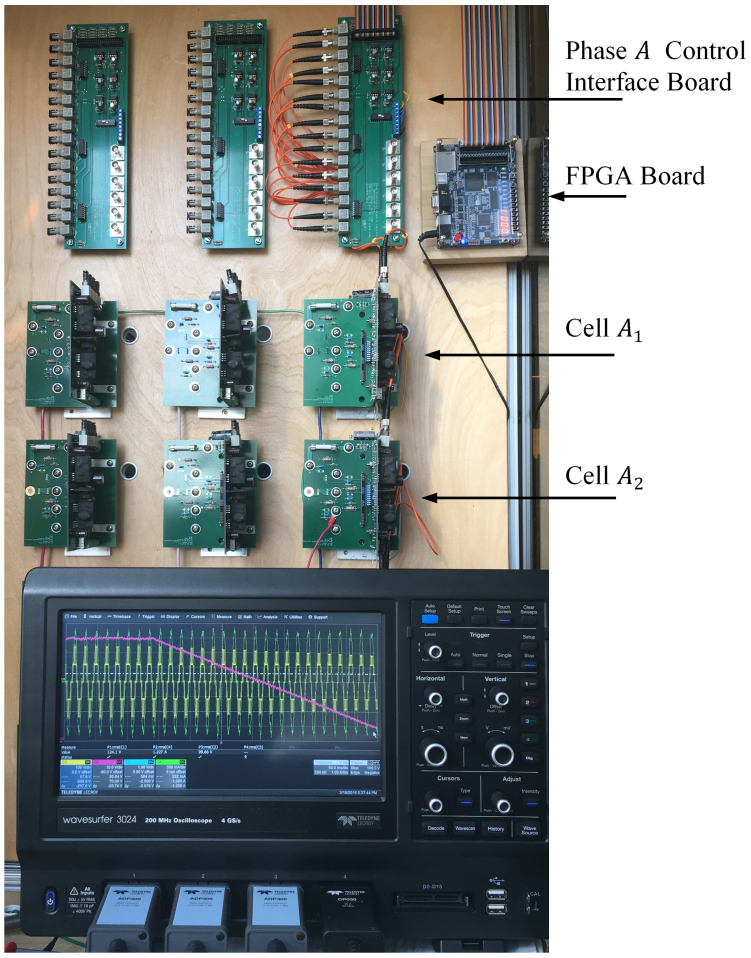


Fig. 5.10: One phase of this experimental setup was used to verify the proposed techniques, as the SPS and SPL algorithms are implemented independently for each CHB leg.

of voltage dividers, AD620AN instrumentation amplifiers, and MAX187 analog-to-digital converters. All other parameters used for experimental verification are shown in Table 5.4. As explained in Section 5.3, the difference in V_{th} between the SPS and SPL algorithms is due to differences in sensor ranges. Finally, for SPL recalculation events, the leg-states selected as recalculation leg-states are those which produced voltages closest to the reference using stored values at the time of recalculation event initialization.

To analyze steady-state performance of the SPS and SPL algorithms, cell voltage v_1 was set and maintained at 120 V while cell voltage v_2 was varied from 120 V to

Table 5.4: Experimental Parameters

	Conventional	SPS	SPL
$\hat{v}_{out}r\,(t)$		$170\sin(2\pi 60t)$ V	
M		2	
f_p		1.2 kHz	
Sensor Range	N/A	$[0, 250]$ V	$[-250, 250]$ V
V_{th}	N/A	4 V	8 V
T_r	N/A	N/A	208 µs
LC Filter		10 mH, 20 µF	
Load		100 Ω	

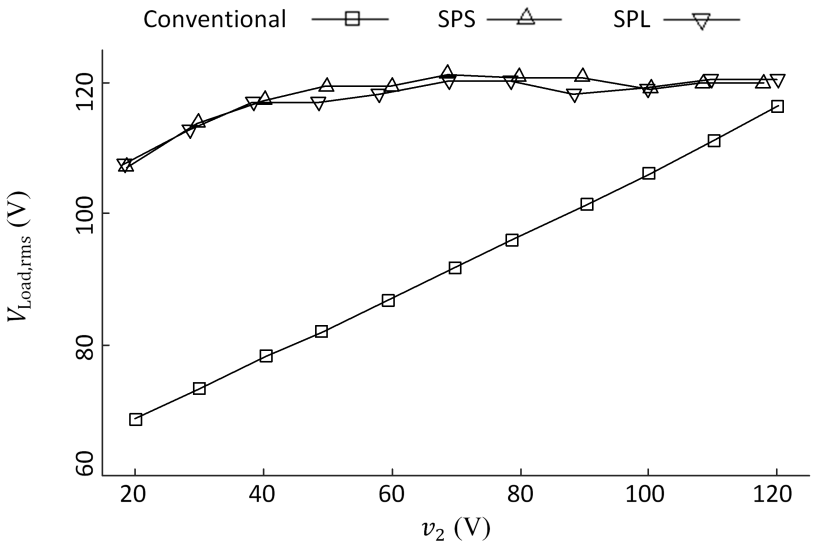


Fig. 5.11: Steady-state fundamental rms voltage for $v_1 = 120\,\text{V}$ and $v_2 \in [20\,\text{V}, 120\,\text{V}]$, obtained using conventional SPWM, SPS adaptive SPWM, and SPL adaptive SPWM.

20 V. For each point analyzed the fundamental component of the load voltage was recorded. When using conventional SPWM the converter's output voltage decreases proportionally with v_2, as shown in Fig. 5.11. The SPS and SPL algorithms, on the other hand, both maintain the desired output voltage over a wide range of v_2 values, with the inverter producing a fundamental component of approximately $120\,\text{V}_{\text{rms}}$ even when $v_2 = 40\,\text{V}$.

To analyze the dynamic performance of the SPS and SPL algorithms, cell voltage v_1 was maintained at 120 V while cell voltage v_2 was decreased from 120 V to 65 V

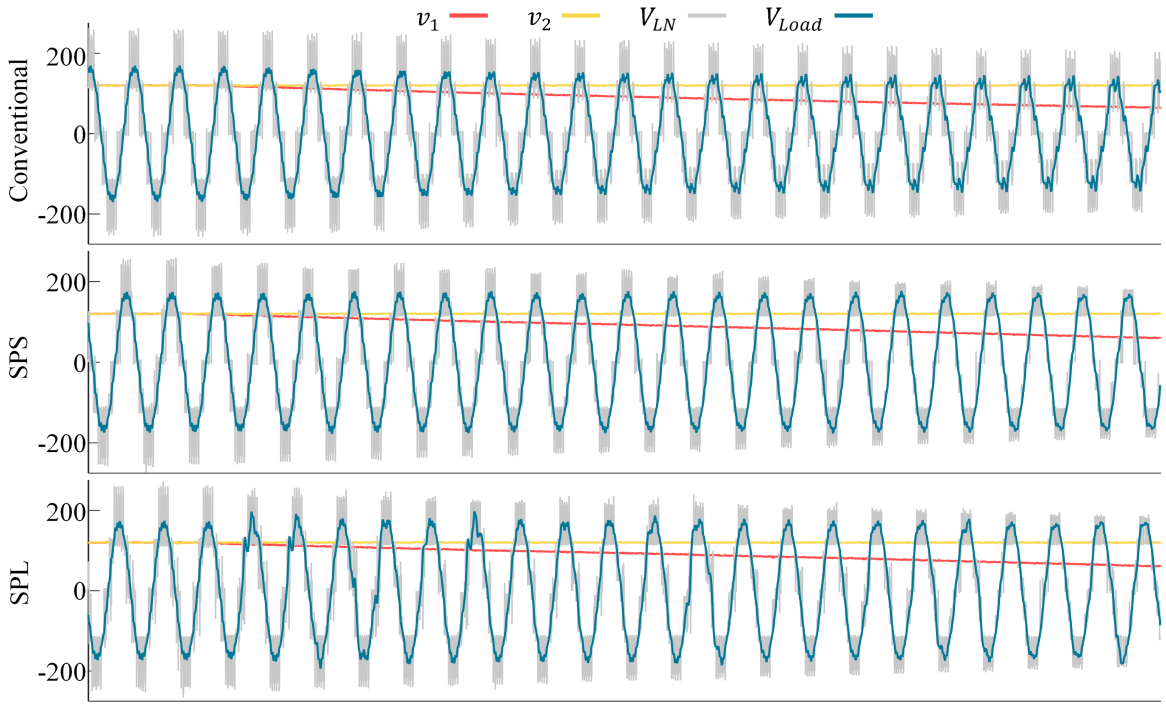


Fig. 5.12: Dynamic performance of the conventional first-on-first-off algorithm, the SPS algorithm, and the SPL algorithm for a rapidly decreasing cell voltage.

at a rate of 160 V/s. The waveforms obtained for conventional SPWM, SPS adaptive SPWM, and SPL adaptive SPWM are shown in Fig. 5.12. The load voltage obtained when using conventional SPWM has a magnitude which decreases as v_2 decreases, and the load voltage waveform becomes noticeably distorted as v_1 and v_2 become unequal. When using SPS or SPL adaptive SPWM the load voltage is maintained as v_2 decreases. When using the SPS algorithm the load voltage waveform generated has little distortion, whereas the load voltage waveform generated when using the SPL algorithm occasionally becomes distorted during recalculation events.

5.6 Steady-State Behavior Modifications

The steady-state PWM output generated using adaptive SPWM is identical whether using the SPS or SPL algorithm, as both algorithms utilize (5.1) and (5.7) to determine

the converter's leg-state. The steady-state behavior of adaptive SPWM as presented in Sections 5.2 and 5.3 results in the utilization of every available switching state, producing a waveform with low THD and minimal dv/dt transitions. In general, however, it may be desirable to alter steady-state behavior based upon other criteria, such as switching losses or power delivered by each cell. While a wide range of criteria can be achieved by changing the steady-state behavior of the proposed algorithms, this section will focus on modifications in a two-cell CHB leg which prevent discordant operation, e.g. average regenerative power flow into a cell while the converter is in motoring mode (Subsection 5.6.1), as well as modifications which minimize switching losses in the higher-voltage cell (Subsection 5.6.2). The proposed alterations focus on preventing certain switching states from being utilized during part of, or an entire, reference period.

5.6.1 Preventing Discordant Operation

As detailed in Chapter 3, it is possible for cells in a CHB leg to receive an average regenerative power even if the leg is providing power under specific circumstances, resulting in a discordant operating point. If the source of the cell receiving power is a near fully charged battery, then an extended period of average regenerative power flow can lead to cell overcharging and potentially deleterious consequences. Thus, measures may be necessary to prevent this average regenerative power flow.

In any multilevel converter with a sinusoidal load current, i.e. $i(\theta) = I\sin(\theta - \phi)$, this regenerative power flow can be prevented by ensuring the generated waveform is quarter-wave-symmetric and utilizes only those switching states where cell voltage outputs have the same sign as the reference. In a two-cell CHB leg this amounts to using $[0,0]$, $[1,0]$, $[0,1]$, and $[1,1]$ when generating pulses for $r(t) > 0$ and using $[0,0]$, $[-1,0]$, $[0,-1]$, and $[-1,-1]$ when generating pulses for $r(t) < 0$. Thus, PWM

generation is the same as in Sections 5.2 and 5.3, except the leg-states $[1,-1]$ and $[-1,1]$ are not used.

To verify that discordant operation will be prevented with these modifications, suppose a cell with $v(t) = v$ provides a pulse between θ_1 and θ_2 where $0 \leq \theta_1 < \theta_2 \leq \pi/2$. Due to quarter wave symmetry a corresponding pulse is provided by the cell between $\pi - \theta_2$ and $\pi - \theta_1$. During one half-cycle the average cell power due to these pulses is found as

$$\begin{aligned} P &= \frac{1}{\pi} \int_0^{\pi} v(\theta)\, i(\theta)\, d\theta \\ &= \frac{1}{\pi} \left(\int_{\theta_1}^{\theta_2} vi(\theta)\, d\theta + \int_{\pi-\theta_2}^{\pi-\theta_1} vi(\theta)\, d\theta \right) \\ &= \frac{2vI\cos(\phi)}{\pi} \left(\cos(\theta_1) - \cos(\theta_2)\right). \end{aligned} \tag{5.11}$$

With the constraints provided, and since $\phi \in (-\pi/2, \pi/2)$ due to the assumption that power is delivered, (5.11) shows $P > 0$. A similar result can be shown for the second half-cycle, proving that the cell generating the pulse is providing power so long as cell outputs have the same sign as the reference voltage. Thus, by avoiding the $[1,-1]$ and $[-1,1]$ leg-states during operation each CHB cell provides power. As explained in Chapter 3, using these leg-states does not necessarily cause a regenerative power flow, but discordant operation is prevented by halting their use.

5.6.2 Minimizing Switching Losses in a High-Voltage Cell

Consider an asymmetric two-cell CHB where $0 < v_1 - v_2 < v_2$, and suppose a switching pattern is to be generated with the primary goal of generating a reference waveform,

$r(\theta)$, while minimizing switching losses in the higher voltage cell (cell 1). For the converter leg described, $0 < v_1 - v_2 < v_2 < v_1 < v_1 + v_2$, so define $L_1 = [0, 0]\,\bar{v}(t)$, $L_2 = [1, -1]\,\bar{v}(t)$, $L_3 = [0, 1]\,\bar{v}(t)$, $L_4 = [1, 0]\,\bar{v}(t)$, and $L_5 = [1, 1]\,\bar{v}(t)$.

In order to minimize cell 1 switching losses without entering cell over-modulation, the converter should switch between ρL_1 and ρL_3 when $|r(\theta)| < v_x$, where $L_2 \leq v_x \leq L_3$ and $\rho = \text{sign}(r(t))$. For $v_x < |r(\theta)| < L_4$ the converter should begin switching between ρL_2 and ρL_4. Finally, for $L_4 < |r(\theta)|$ the converter should switch between ρL_4 and ρL_5. This switching pattern results in cell 1 to switching whenever $|r(\theta)| = v_x$. Assuming $r(\theta) = \hat{v}_{out} \sin(\theta)$, cell 1 will either switch twice every half-cycle ($\hat{v}_{out} > v_x$) or not at all ($\hat{v}_{out} < v_x$).

To achieve the switching pattern described, the interval $[0, \pi]$ must be partitioned into three distinct regions. For $\theta \in [0, \theta_1]$ and $\theta \in [\pi - \theta_1, \pi]$, the set of carriers used should be generated as if S_1 and S_3 are the only available switching states, whereas for $\theta \in [\theta_1, \pi - \theta_1]$ the set of carriers used should be generated as if S_2, S_4, and S_5 are

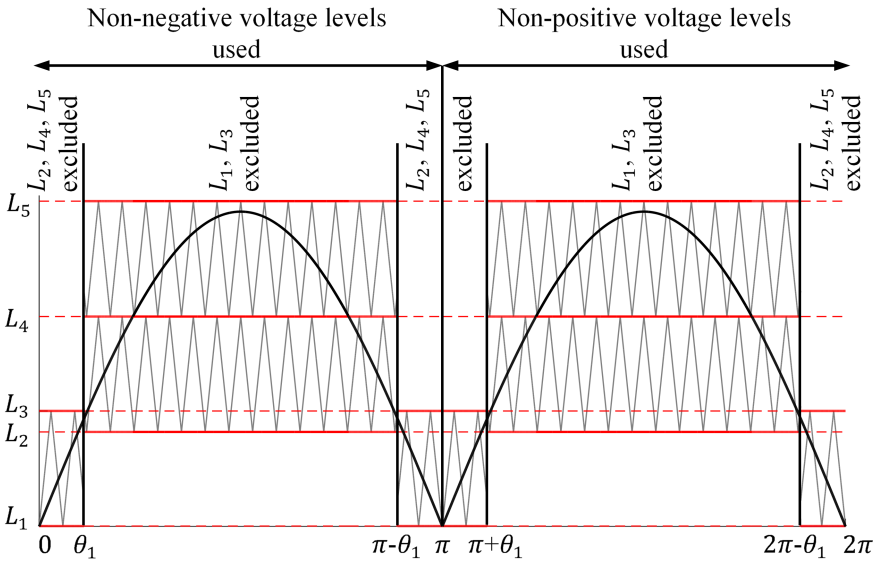


Fig. 5.13: Partitioning of the half-wave region $[0, \pi]$ for a two-cell asymmetric CHB which minimizes the number of switching transitions for the higher voltage cell, where the reference in a region is generated by switching between levels with solid lines.

the only available switching states. Partitioning the positive half cycle in this way the desired switching pattern is implemented. A plot showing this partitioning for $|r(\theta)|$ is shown in Fig. 5.13.

Finally, note that by varying v_x between L_2 and L_3 the ratio of power delivered by cell 1 vs cell 2 can be modified. By making the adjustments suggested in this subsection, the switching pattern generated matches the pattern generated by hybrid PWM as presented in Chapter 2.

5.7 Conclusion

In this chapter, adaptive SPWM has been introduced for use in CHB multilevel inverters to allow a symmetric waveform to be generated even in the presence of time varying input dc-voltage sources. The SPS algorithm, which requires one voltage sensor for each voltage source, and the SPL algorithm, which requires one voltage sensor for each CHB leg, have been presented as alternative methods to implement adaptive SPWM. Simulation software has been utilized to demonstrate the functionality of both algorithms for one leg of a three-cell CHB with rapidly changing input voltages, and experimental verification have been provided for one leg of a two-cell CHB. A modification limiting the states utilized by the SPS and SPL has also been proposed as a method to allow various design criteria to be met during steady-state behavior. Finally, it should be noted that although the algorithms in this chapter described single-phase implementation, the methods can be naturally expanded for use in polyphase systems.

Chapter 6

Open-Circuit Switch Fault Detection and Isolation

In this chapter, an open-circuit fault-detection technique is presented. This technique *(i)* can be applied to symmetric and asymmetric converters, *(ii)* is independent of the PWM scheme utilized, *(iii)* identifies faults quickly, and *(iv)* does not have a significant computational burden. In Section 6.2, the proposed method for fault detection is explained. Simulink simulation results and experimental data, demonstrating the performance of the proposed technique, are provided in Sections 6.3 and 6.4, respectively. Details about choosing a threshold value, and important step of the proposed method, are provided in Section 6.5. In Section 6.6, concluding comments are provided.

6.1 Chapter Notation

The CHB converter notation used throughout this chapter will be introduced in this section. The notation introduced in Chapter 2 is slightly modified in this chapter to provide each switch within a CHB leg with a unique label, as shown in Fig. 6.1. These

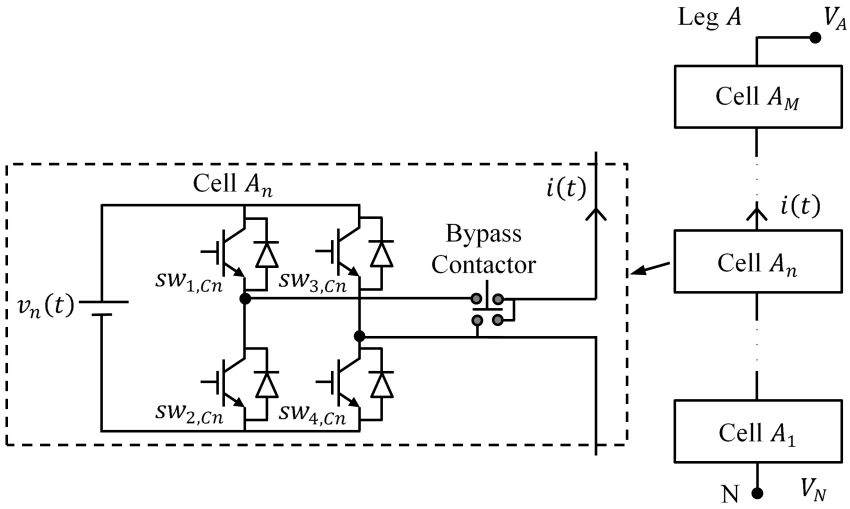


Fig. 6.1: One cascaded H-bridge multilevel converter leg.

Table 6.1: Cell Switch Configurations, Output Voltages, and States

$[sw_{1,Cn}, sw_{3,Cn}]$	Cell Output Voltage	Cell State $s_n(t)$
$[0,0]$	0	0_L
$[0,1]$	$-v_n(t)$	-1
$[1,0]$	$v_n(t)$	1
$[1,1]$	0	0_U

unique labels facilitate the presentation of techniques within this chapter. Using this modified notation, the a cell's output voltage of depends on the cell's switch configuration, as shown in Table 6.1, where it is assumed that $sw_{1,Cn}$ and $sw_{2,Cn}$ act in a complimentary manner, as do $sw_{3,Cn}$ and $sw_{4,Cn}$. The four allowable cell switch configurations each correspond to a unique cell state, $s_n(t)$, as shown in Table 6.1. During healthy operation the two zero-states, denoted as 0_U and 0_L, are treated interchangeably, but the distinction between these states is necessary under fault conditions.

Techniques presented in this chapter require input dc source magnitudes to be known prior to a fault event, thus permitting time-variant or time-invariant input dc sources to be used. To demonstrate the proposed method for fault detection, isolation, and verification, LSPWM is utilized for the symmetric CHB presented in Section 6.3,

whereas ASPWM, introduced in Chapter 5, is used for the asymmetric CHB presented Section 6.4. However, the proposed method is independent of the PWM technique used, enabling the utilization of any PWM scheme.

6.1.1 Open-Circuit Switch Fault Effects

When an open-circuit switch fault occurs in a CHB cell, the faulty cell's state and the direction of current flow through the CHB leg determine whether the cell's output voltage is impacted, since a switch's anti-parallel diode is assumed to be unaffected by the open-circuit switch fault. Table 6.2 shows how the output voltage of cell n is affected for positive and negative current flow under open-circuit fault conditions at each of the four possible fault locations. The data in Table 6.2 show that a given open-circuit fault impacts a cell's output voltage for two cell states, one zero-state and one nonzero-state, and this effect is only seen for one direction of current flow. Further, whenever a cell's output voltage deviates due to an open-circuit fault the direction of current flow determines the deviation of the cell's output voltage, with deviations due to positive current flow producing voltages lower than expected and deviations due to negative current flow producing voltages higher than expected. For instance, as shown

Table 6.2: Cell n Output Voltage Deviation, $\Delta v = v_{expected} - v_{actual}$, Under Open-Circuit Fault Conditions

		$[sw_{1,Cn}, sw_{3,Cn}]$			
Fault Location	Current Direction	$[0,0]$	$[0,1]$	$[1,0]$	$[1,1]$
$sw_{1,Cn}$	$i > 0$	0	0	$v_n(t)$	$v_n(t)$
	$i < 0$	0	0	0	0
$sw_{1,Cn}$	$i > 0$	0	0	0	0
	$i < 0$	$-v_n(t)$	$-v_n(t)$	0	0
$sw_{1,Cn}$	$i > 0$	0	0	0	0
	$i < 0$	0	$-v_n(t)$	0	$-v_n(t)$
$sw_{1,Cn}$	$i > 0$	$v_n(t)$	0	$v_n(t)$	0
	$i < 0$	0	0	0	0

*Current directions are in reference to Fig. 6.1.

in Table 6.2, an open-circuit $sw_{1,Cn}$ fault can only be observed when $s_n(t) \in \{1, 0_U\}$ and $i(t) > 0$ (using the reference direction shown in Fig. 6.1) as current flows through the IGBT of the faulty switch only under these conditions. If $sw_{1,Cn}$ has an open circuit fault and $i(t) > 0$, then the output voltage of cell n is 0 if $s_n(t) = 1$ and $-v_n$ if $s_n(t) = 0_U$, showing the output is lower than expected in both cases. These observations form the basis for the open-circuit fault detection scheme presented in this chapter.

6.2 Open-Circuit Fault Detection

A method for detecting open-circuit switch faults in a CHB converter leg, outlined as a state-machine diagram in Fig. 6.2, is presented in this section. The proposed technique requires a voltage sensor and current sensor to measure a CHB leg's output voltage and the direction of current flow through the leg. Note that the required voltage sensor can also be used for the SPL ASPWM algorithm introduced in Chapter 5. Fault detection consists of three distinct states: A) Identification of Possible Open-Circuit Fault Locations, B) Faulty Switch Isolation, and C) Faulty Switch Verification. These three stages are detailed in the following subsections.

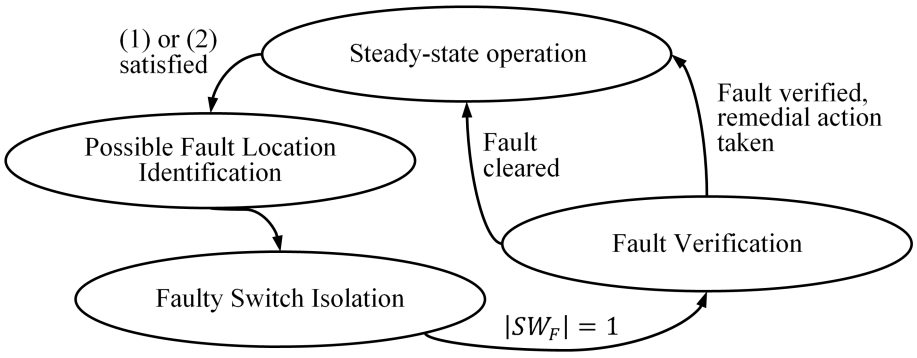


Fig. 6.2: Finite-state machine diagram for the proposed fault-detection method.

6.2.1 Identifying Possible Open-Circuit Fault Locations

The expected output voltage, v_E, for each leg-state of a CHB are defined by stored dc source input magnitudes for each cell, determined e.g. via ASPWM as described in Chapter 5. As shown in Table 6.2, a cell with an open-circuit fault produces predictable output voltage deviations depending on the direction of current flow through the cell and the cell's state. Accordingly, a CHB leg containing a cell with an open-circuit fault generates output line-to-neutral voltages, $v_{LN}(t)$, which predictably deviate from expected values depending on the faulty cell's state and the current flow direction through the leg. An output voltage deviation is symptomatic of an open-circuit switch fault in cell n if:

$$i > 0,\ s_n \in \{1, 0_U, 0_L\},\ \text{and}\ |(v_{LN} - v_E) + v_n| < \epsilon \tag{6.1}$$

or,

$$i < 0,\ s_n \in \{-1, 0_U, 0_L\},\ \text{and}\ |(v_{LN} - v_E) - v_n| < \epsilon \tag{6.2}$$

where $\epsilon > 0$ allows for measurement noise. Details regarding the choice of ϵ are provided in Section 6.5. For symmetric CHB converters, ϵ should be set as a fraction of each cell's input dc voltage, e.g. $V_{dc}/2$. For asymmetric converters, the smallest input dc voltage can be used to set ϵ, though it may be advantageous to instead set ϵ based on the differences between input dc voltages. If either (6.1) or (6.2) are met for cell n then any conducting IGBTs in the cell are possible open-circuit switch fault locations. Thus there are two possible faulty switch locations if $s_n \in \{1, -1\}$ and one possible faulty switch location if $s_n \in \{0_P, 0_N\}$. All possible switch locations are stored in the set SW_F.

As an example, consider a two-cell CHB leg with the known cell voltage vector

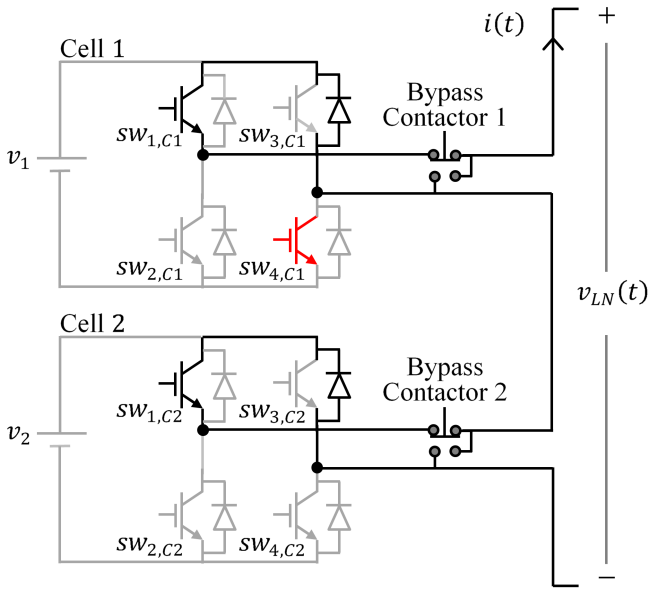


Fig. 6.3: Current path when $i\,(t) > 0$ for a two-cell CHB leg under the $S = [1, 0_U]$ leg-state, with an open-circuit fault in $sw_{4,C1}$. The expected voltage is $v_E = v_1$, but the measured voltage is $v_{LN}(t) = 0$.

$\bar{v}\,(t) = [v_1, v_2]^{\mathrm{T}}$. Suppose an open-circuit $sw_{4,C1}$ switch fault in occurs as shown in Fig. 6.3, when $i > 0$ and the leg-state is $S\,(t) = [1, 0_U]$ (indicating the outputs of cells 1 and 2 are expected tobe v_1 and 0, respectively). An output voltage deviation is detected, as $v_E = v_1$ but $v_{LN}\,(t) = 0$. The possible fault locations identified depend upon the relation between v_1 and v_2 as follows:

Case (i): If $v_1 \neq v_2$, then it is determined that $sw_{1,C1}$ and $sw_{4,C1}$ are possible open-circuit fault locations, since $i\,(t) > 0$, $s_1\,(t) = 1$, and $v_{LN}\,(t) + v_1 = 0 + v_1 = v_E$ and so (6.1) is satisfied. Since cell 2 does not satisfy (6.1) or (6.2) no other potential fault locations exist, so the set of potential fault locations is $SW_F = \{sw_{1,C1}, sw_{4,C1}\}$.

Case (ii): If $v_1 = v_2 = v$, then it is determined that $sw_{1,C1}$ and $sw_{4,C1}$ are possible open-circuit fault locations, since cell 1 satisfies (6.1). Similarly, $sw_{1,C2}$ is identified as a possible fault location since cell 2 satisfies (6.1) and current flows through $sw_{1,C2}$ when $i\,(t) > 0$ and $s_2\,(t) = 0_U$. Thus, $SW_F = \{sw_{1,C1}, sw_{4,C1}, sw_{1,C2}\}$.

6.2.2 Faulty Switch Isolation

Once all possible fault locations have been identified, the switch most likely to be faulty must be isolated, i.e. SW_F must be made to have a single element. Faulty switch isolation is achieved as outlined in Fig. 6.4. Assuming the cardinality of SW_F is greater than 1, the following procedure is used to individually test elements of SW_F:

1) A potentially faulty switch to be tested, sw_T, is selected from the set of potential fault locations, SW_F.

2) A test-state, S_T, is chosen as a leg-state which utilizes all switches from the set $SW_F \backslash sw_T$, i.e. the test-state is selected such that the state uses all potentially faulty switches excluding sw_T.

3) The line-to-neutral voltage corresponding to S_T is measured and compared to the expected voltage, v_E. If the measured voltage is not equal to the expected voltage of S_T then one of the switches in $SW_F \backslash sw_T$ is faulty, therefore sw_T is not faulty and is

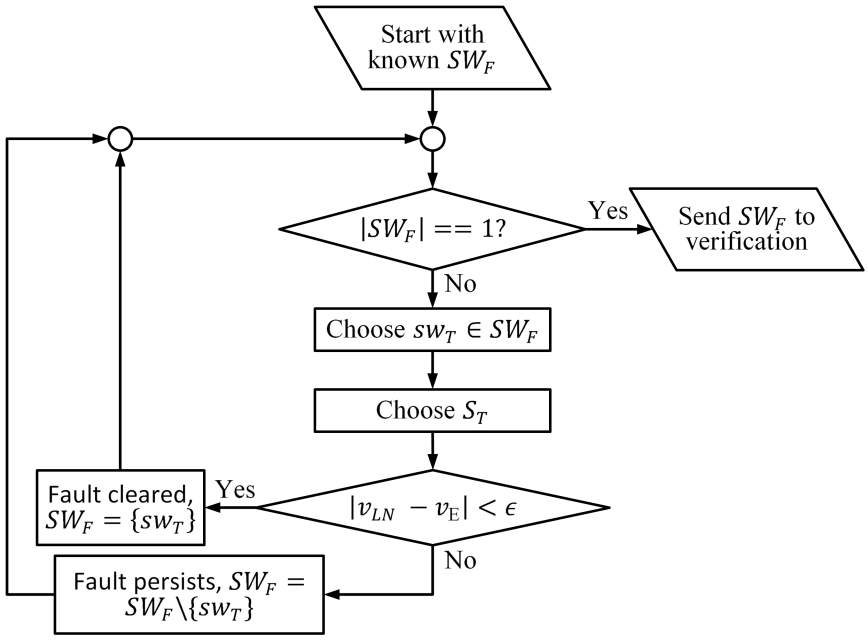


Fig. 6.4: Procedure for fault location isolation using set of possible fault locations, SW_F, identified as explained in Section 6.2.1.

removed from SW_F. On the other hand, if the measured output voltage is equal to the expected output voltage then no fault exists in the switches in $SW_F \backslash sw_T$, therefore sw_T is identified as faulty and all elements except sw_T are removed from SW_F.

4) Steps 1-3 are repeated until $|SW_F| = 1$, i.e. the set contains one element, at which point the fault location has been isolated.

During the isolation procedure the direction of current flow through the leg must be the same as when the fault was initially detected. If the current direction changes during the isolation procedure, the switch being tested cannot be accurately classified as either faulty or non-faulty and retesting is required. However, maintaining current direction during isolation can be facilitated, most notably through high-speed assessment of any required test states. Further adjustments may be desirable, particularly when the current through a leg is nearly zero when a fault is detected. For instance, concerns about current direction can be mitigated by selecting test-states intended to maintain the desired direction of current flow. Alternatively, to avoid current flow reversal, (6.1) and (6.2) can be modified to only allow fault detection if the current magnitude exceeds a minimum value.

For an M cell CHB leg, the largest possible cardinality of SW_F is $2M$, obtained if all elements of $\bar{v}(t)$ are equal and a voltage deviation occurs either when $i(t) > 0$ and the leg-state S only contains elements equal to 1, or when $i(t) < 0$ and the leg-state S only contains elements equal to -1. Using the isolation procedure outlined, if k possible fault locations exist then between 0 and $k-1$ test-states are required for isolation. Thus, faulty switch isolation for an M cell CHB requires between 0 and $2M-1$ test-states. Assuming the converter changes between the required states at a rate equal to the measurement frequency, open-circuit fault identification and isolation can occur in a fraction of a cycle, i.e. in less than 16.7 ms for a 60 Hz fundamental frequency. Briefly adjusting a converter's switching frequency during the isolation procedure, in

order to transition between the required states at a rate equal to the measurement frequency, may be justifiable since the isolation process would require, at most, $2M-1$ measurement cycles. Once a fault has been detected, the PWM strategy utilized during prefault operation is interrupted in order to rapidly apply any test states required for isolation. During the isolation procedure, for less than $2M$ measurement (sampling) cycles the prefault PWM scheme is temporarily suspended, and therefore the proposed method is independent of the PWM scheme utilized.

Continuing the example from the previous subsection:

Case (i): Since $SW_F = \{sw_{1,C1}, sw_{4,C1}\}$ has more than one element, isolation is required. Initially choose $sw_T = sw_{1,C1}$. The test-state $S_T = [0_L, 1]$ is selected to test sw_T since this leg-state uses all elements of $SW_F \backslash \{sw_{1,C1}\} = \{sw_{4,C1}\}$ and does not use $sw_{1,C1}$. This S_T produces an output of $-v_1 + v_2$. Since the expected output is $v_E = v_2$ a fault still exists and so $sw_{1,C1}$ is removed from SW_F. Since $SW_F = \{sw_{4,C1}\}$ contains a single element the faulty switch has been isolated.

Case (ii): Since $SW_F = \{sw_{1,C1}, sw_{4,C1}, sw_{1,C2}\}$ has more than one element, isolation is required. Initially choose $sw_T = sw_{1,C1}$, and proceed as in *Case i* to obtain $SW_F = \{sw_{4,C1}, sw_{1,C2}\}$. The isolation procedure continues by selecting $sw_T = sw_{4,C1}$. The test-state $S_T = [0_U, 1]$ is selected to test sw_T since this leg-state uses all elements of $SW_F \backslash \{sw_{4,C1}\} = \{sw_{1,C2}\}$ and does not use $\{sw_{4,C1}\}$. This S_T produces an output of $v_2 = v$, which is equal to the expected voltage. Since the switches being used for S_T do not produce a fault, all elements except $\{sw_{4,C1}\}$ are removed from SW_F. Since $SW_F = \{sw_{4,C1}\}$ contains a single element the faulty switch has been isolated.

6.2.3 Faulty Switch Verification

Once a single switch, $sw_{x,Cy}$, has been identified as a possible location for an open-circuit switch fault, the fault must be verified. This step prevents unnecessary recon-

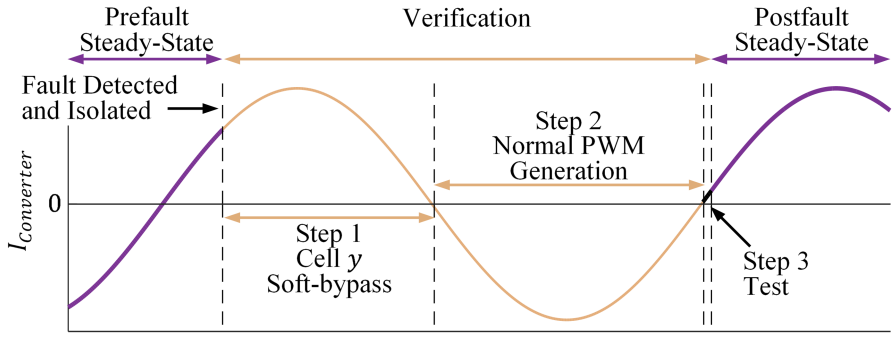


Fig. 6.5: Three-step verification process for a $sw_{x,Cy}$ fault, $x \in \{1, 4\}$. For $x \in \{2, 3\}$ the current direction for each step is reversed.

figuration due to fault misclassification, e.g. intermittent gate misfiring faults being classified as open-circuit faults. The proposed three-step verification process, shown in Fig. 6.5, depends on the location of the isolated switch, $sw_{x,Cy}$, as well as the direction of current flow through the converter. The three-step verification process is as follows:

1) After isolation, cell y is set to the zero-state which doesn't require $sw_{x,Cy}$, i.e. $s_y = 0_U$ if $x \in \{2, 4\}$ and $s_y = 0_L$ if $x \in \{1, 3\}$. This is a soft-bypass for the cell, as opposed to a hard-bypass achieved via the faulty cell's bypass contactor.

2) For $x \in \{1, 4\}$, cell n is again used for PWM generation once the current flow through the converter is negative, as current will flow through the faulty switch's anti-parallel diode. Similarly, if $x \in \{2, 3\}$ then cell n is used for PWM generation once the current flow through the converter is positive.

3) The possibly faulty switch is tested once current flow through the converter reverses, i.e. becomes positive for $x \in \{1, 4\}$ or negative for $x \in \{2, 3\}$. The switch is tested by using either of the cell states affected by the fault location, e.g. $s_n \in \{1, 0_U\}$ if $x = 1$, $s_n \in \{-1, 0_L\}$ if $x = 2$, etc.

Regardless of the PWM strategy utilized by the CHB converter, when using this three-step procedure a suspected open-circuit fault is verified if the expected leg voltage is equal to the measured voltage during steps 1 and 2, but a deviation satisfying (6.1) or

(6.2) occurs during step 3. On the other hand, if a cell operates normally during steps 1, 2, and 3, then the suspected open-circuit fault may have been due to gate misfiring, whereas unexpected output voltages during steps 1 or 2 may indicate time-variant input dc source magnitudes have improbably changed such that (6.1) or (6.2) were coincidentally satisfied. Confirming or clearing $sw_{x,Cy}$ as an open-circuit fault location takes approximately one fundamental cycle of the generated waveform, depending on when the potential fault is first identified.

Concluding the example from the previous subsections:

Cases (i) and (ii): The isolated faulty switch is $sw_{4,C1}$, and so cell 1 is soft-bypassed by setting $s_1(t) = 0_U$ while $i(t) > 0$. When current flow changes direction, i.e. $i(t) < 0$, cell 1 is used for PWM generation as normal. When current flow changes direction again, i.e. $i(t) > 0$ a half-cycle later, the verification process is tested by setting $s_1(t) = 1$. Regardless of the remaining cell states, v_{LN} will deviate from v_E by v_1, and thus the fault in $sw_{4,C1}$ is verified and corrective actions can be implemented. One potential corrective action is to hard-bypass cell 1 using the bypass contactor. If implemented in a three-phase system, the atypical PWM technique presented in Chapter 4 can be used to facilitate increased dc bus utilization during postfault operation.

Finally, it is noted that application of the proposed technique requires consideration of the sensor circuitry necessary. Utilization of high-bandwidth, high-resolution sensors increase the rate at which the system voltage and current can be measured, thereby reducing the time required for fault detection and isolation. However, the proposed technique does not necessitate the use of high-bandwidth sensors, which are costly and potentially susceptible to high-frequency noise. If the bandwidth of the sensor circuitry is decreased then implementation cost is reduced and the system is less vulnerable to high frequency noise, although the measurement rate must be reduced. It is ultimately up to the system designer to decide upon the appropriate sensor circuitry for a system,

as the proposed method does not impose any strict requirements upon the sensor bandwidth.

6.3 Simulation Results

In this section, MATLAB/Simulink simulation results are presented for a symmetric three-cell CHB leg to demonstrate the methods proposed in the previous section. Since the proposed technique is designed to be individually applied to each phase, data collected for a single-phase system allow validation of the detection, isolation, and verification processes. Open-circuit faults were simulated by appropriately modifying the gate signal sent to a given switch. Simulation data are provided for two different simulations to show the behavior of the proposed techniques for: (A) an open-circuit fault, and (B) a gate-misfiring fault. The presented simulations utilize the parameters shown in Table 6.3, with gate signals generated using level-shifted sinusoidal PWM implemented using a first-on-first-off pattern. Due to simulation idealities, selecting ϵ is not an important consideration. However, if measurement noise were a concern, then an epsilon value based on the 40 V input dc voltages could be used since the CHB is symmetric. For instance, $\epsilon = 20$ could be selected to mitigate noise concerns without allowing (6.1) or (6.2) to be satisfied during normal operation. Finally, note that the converter's load does not significantly impact the behavior of the proposed technique, provided that the direction of current flow through the converter can be determined.

Table 6.3: Simulation Parameters

Prefault Reference Voltage	$100\sin(2\pi 60t)$ V
M	3
$[v_1, v_2, v_2]$	$[40\,\text{V}, 40\,\text{V}, 40\,\text{V}]$
Carrier Frequency	1.32 kHz
Measurement Period	500 µs
Load	2.5 Ω in series with 5 mH

6.3.1 Open-Circuit Fault

The simulation data in this subsection, shown in Fig. 6.6, were obtained for an open-circuit $sw_{3,C3}$ fault, where $sw_{3,C3}$ was selected to demonstrate the longest possible isolation process using Table 6.3 parameters. For this simulation, fault detection occurs when the leg-state is $S = [-1, -1, -1]$. Since all input voltages are equal, the maximum number of switches are identified as possible fault locations, i.e. $SW_F = \{sw_{2,C1}, sw_{3,C1}, sw_{2,C2}, sw_{3,C2}, sw_{2,C3}, sw_{3,C3}\}$. These possible locations are checked in the order they appear in the set, thus five measurement cycles, 2.5 ms, elapse between the generation of SW_F and the isolation of $sw_{3,C2}$. For the switch $sw_T = sw_{x,Cy}$ being tested during isolation, the test leg-state used was chosen such that $s_y = 0_U$ if $x \in \{2, 4\}$, $s_y = 0_L$ if $x \in \{1, 3\}$, and $s_n = -1$ if $n \neq y$.

After $sw_{3,C2}$ is isolated, the fault is verified using the three-step method presented in Section 6.2.3, with successful verification completed 11.47 ms after isolation. With the fault verified, a hard-bypass is implemented for cell 3 and the PWM reference waveform is adjusted from a 100 V peak to an 80 V peak, thereby preventing overmodulation. Note that this reference waveform adjustment can be omitted if overmodulation is permitted for the application. For a three-phase system, postfault operation may

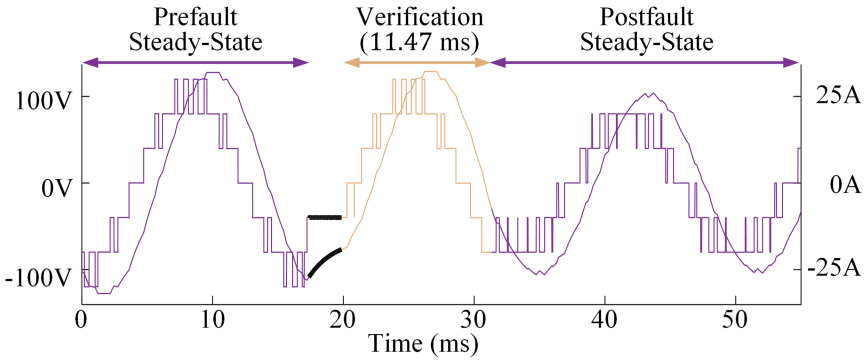


Fig. 6.6: CHB leg line-to-neutral voltage and load current with a $sw_{3,C3}$ open-circuit fault occurring at 17.35 ms. Fault detection and isolation, highlighted in black, occur in the 2.5 ms between prefault steady-state and verification.

require further reconfiguration actions, e.g. the use of the atypical PWM technique introduced in Chapter 4.

6.3.2 Gate Misfiring Fault

Simulation data in this subsection, shown in Fig. 6.7, were obtained for a $sw_{1,C1}$ gate-misfiring fault, where $sw_{1,C1}$ was selected to demonstrate the shortest possible isolation process, for a non-singular SW_F, using Table 6.3 parameters. The simulated gate-misfiring fault causes the affected switch to appear as an open-circuit until its gate signal is cycled, i.e. the gate-misfiring fault is cleared if the gate signal is turned from conducting to non-conducting and back.

For this simulation, the apparent open-circuit fault is detected when $S = [1, 1, 0_U]$, and thus $SW_F = \{sw_{1,C1}, sw_{4,C1}, sw_{1,C2}, sw_{4,C2}, sw_{1,C3}\}$. As before, these possible fault locations are checked in the order they appear in the set, thus one measurement cycle, 500 µs, elapses between the generation of SW_F and the isolation of $sw_{1,C1}$. The three-step verification process is then implemented, and $sw_{1,C1}$ is tested and confirmed to be operating properly 11.20 ms after isolation. The fault is therefore cleared and no corrective action is necessary.

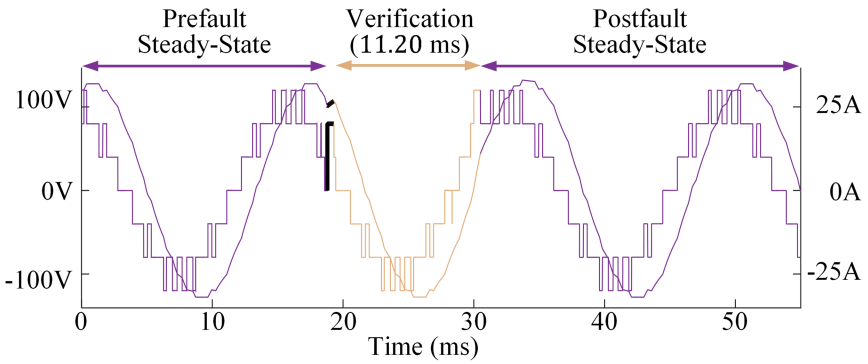


Fig. 6.7: CHB leg line-to-neutral voltage and load current with a $sw_{1,C1}$ gate misfiring fault occurring at 18.8 ms. Fault detection and isolation, highlighted in black, occur in the 0.5 ms between prefault steady-state and verification.

6.4 Experimental Verification

In this section, experimental data are presented for an asymmetric three-cell CHB leg to support the proposed open-circuit fault detection techniques. Open-circuit faults were emulated by appropriately modifying the gate signal sent to a given switch. Using parameters as outlined in Table 6.4, data were collected utilizaing the setup shown in Fig. 6.8. An Altera EP3C16F484C6 FPGA, programmed using techniques outlined in [107], was used to implement the techniques for detection, isolation, and verification proposed in Sections 6.2.1, 6.2.2, and 6.2.3. Steady-state behavior for the CHB leg, also implemented using the FPGA, was achieved using steady-state ASPWM as outlined in Chapter 5. Reconfiguration for verified faults consisted of a soft-bypass for the faulty cell and a reference adjustment to prevent overmodulation. As before, if overmodulation is permitted for an application then the reference waveform adjustment can be omitted. Also, for a three-phase system, postfault operation may require further reconfiguration actions such as utilization of the atypical PWM technique introduced in Chapter 4.

The current and voltage sensor circuitry used in the experimental setup is shown in Fig. 6.9. A MAX187 analog-to-digital converter (ADC) was used to measure the inverter's output voltage, after it had been stepped down by a voltage divider and then shifted using an AD620AN instrumentation amplifier (IA) with 1 MHz bandwidth.

Table 6.4: Experimental Parameters

Prefault Reference Voltage	$170\sin(2\pi 60t)$ V
M	3
$[v_1, v_2, v_2]$	$[60\,\text{V}, 70\,\text{V}, 75\,\text{V}]$
Carrier Frequency	2.52 kHz
Measurement Period	$\approx 110\,\mu\text{s}$
LC Filter	3 mH, 15 µF
Load	50 Ω

The current was measured using a 200 kHz bandwidth LAH25-NP current transducer, a voltage divider, an AD620AN IA, and a MAX187 ADC. Serial peripheral interface communication was used to transfer the 12-bit measurement data from the ADC to the FPGA. The proposed method was implemented with $\epsilon = 2.5\,\mathrm{V}$, selected based on the measurement noise level while also attempting to minimize the number of cells which could satisfy (6.1) or (6.2) in the event of a fault. Finally, to help prevent current flow reversal during the isolation procedure, (6.1) and (6.2) were modified so that fault detection was only permitted for current magnitudes greater than 0.2 A.

To provide a basis for comparison, experimental data, shown in Fig. 6.10, were collected for the case where converter operation continues normally in the event of a

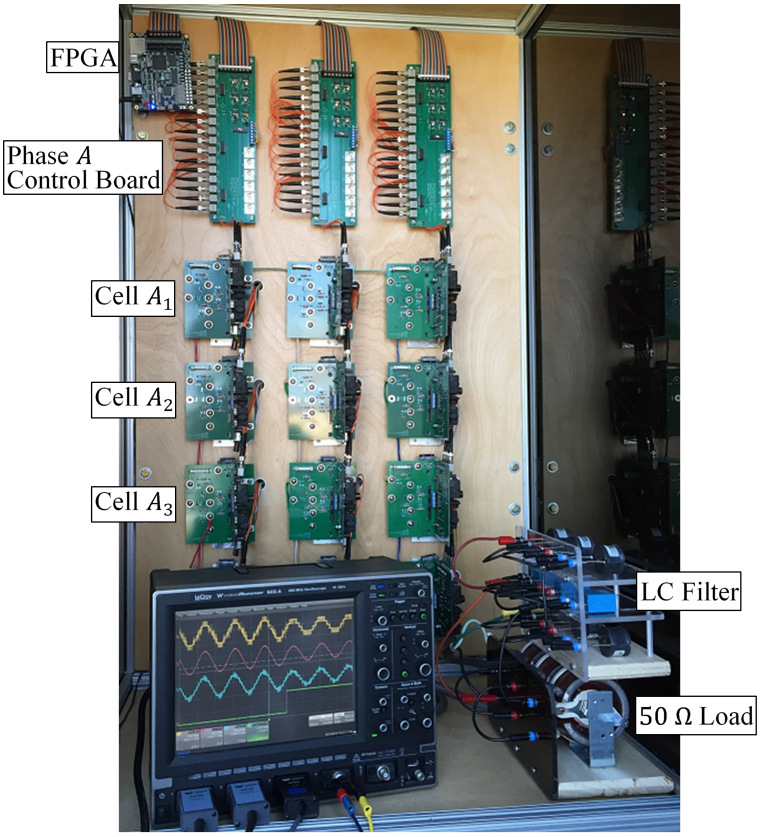


Fig. 6.8: One leg of this laboratory scale CHB was used to verify the proposed technique, as it is designed to be implemented independently for each leg.

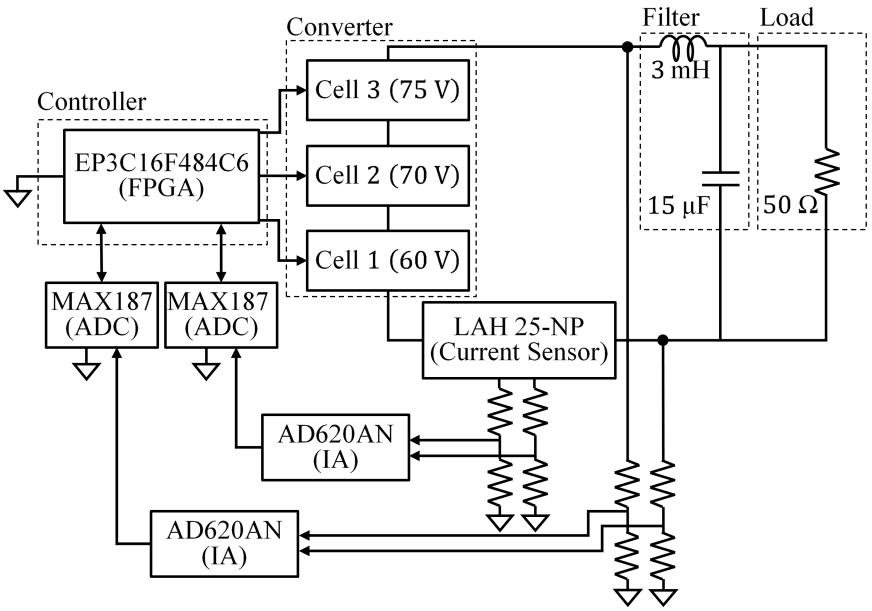


Fig. 6.9: Diagram of experimental setup, detailing the current and voltage sensor circuitry used.

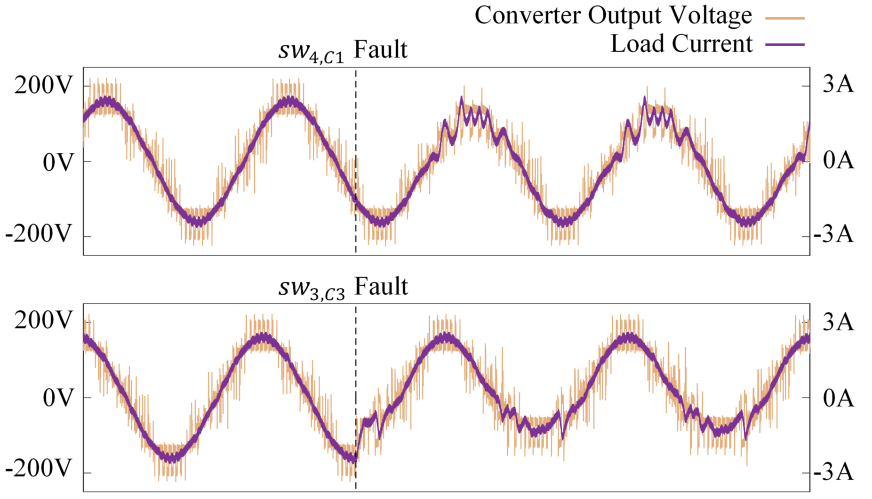


Fig. 6.10: Experimental data collected for an open-circuit fault in $sw_{4,C1}$ (top), and $sw_{3,C3}$ (bottom), if no corrective actions are taken.

fault. Open-circuit faults were created separately for $sw_{4,C1}$ and $sw_{3,C3}$ by forcing the gate driver to make the corresponding IGBT nonconductive. The results, for both locations, show the load current and converter output voltage are both distorted for approximately half of each cycle, matching the analysis presented in Section 6.2.1.

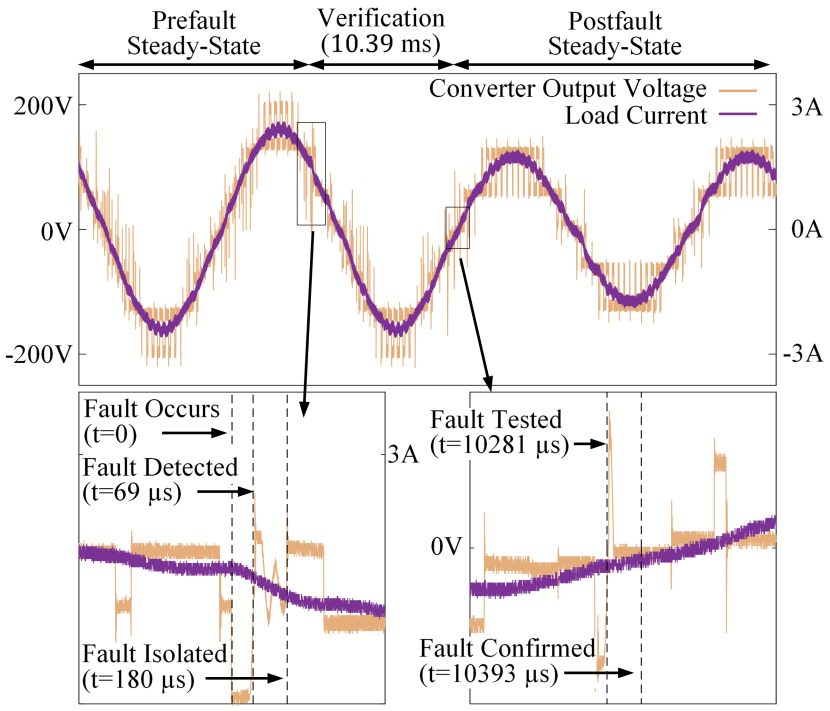


Fig. 6.11: Performance for an open-circuit fault in $sw_{1,C3}$, with behavior shown in detail during detection/isolation and step three of the verification process.

While converter operation continues even without making any corrective action, the resulting current waveform is noticeably distorted and has a dc-offset which can cause severe damage to some loads, e.g. motors. Note that the effects of a fault are only apparent during part of an output cycle, and thus faults may not cause ill-effects immediately after occurring, as shown in Fig. 6.10 for the $sw_{4,C1}$ fault.

Experimental data demonstrating the proposed technique for a fault in $sw_{1,C3}$ are shown in Fig. 6.11. The fault was detected 69 µs after occurring, and $sw_{1,C3}$ is isolated as the fault location one measurement cycle later. The three-step verification process, described in Section 6.2.3, is then carried out, with the faulty switch finally tested using the leg-state $S = [0, 0, 1]$. The fault is ultimately confirmed as a deviation is detected during the test state, since the expected voltage corresponding to the test leg-state is 75 V while the measured voltage is 0 V. Reconfiguration actions are taken

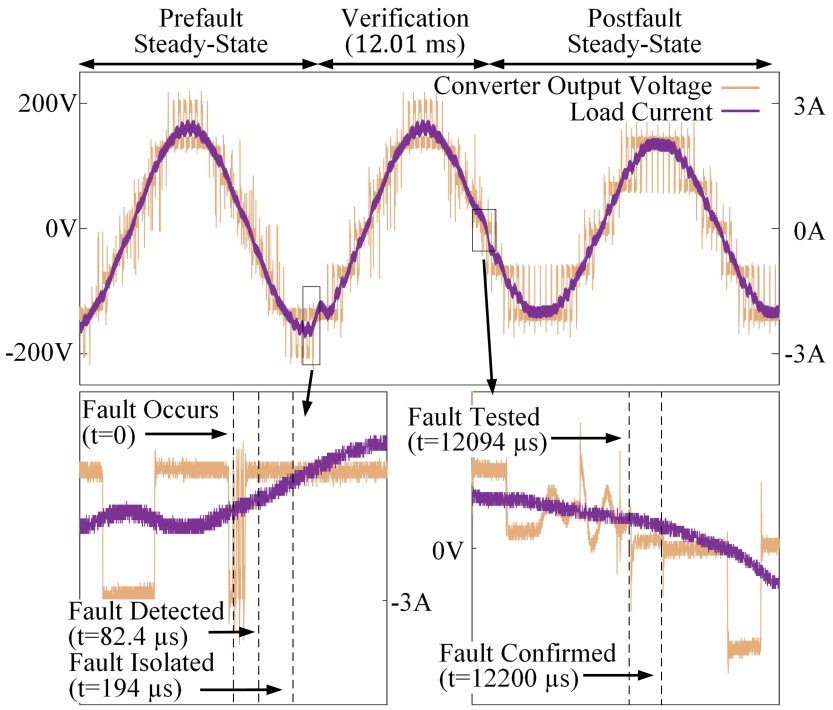


Fig. 6.12: Performance for an open-circuit fault in $sw_{2,C1}$ occurring mid-cycle.

once the fault is verified, with the reference reduced to have a peak value of 140 V, thereby preventing overmodulation.

Experimental data shown in Fig. 6.12 demonstrates a similar fault detection process for a $sw_{2,C1}$ open-circuit fault. The fault is detected and isolated in less than two measurement cycles, and then verified in less than one fundamental cycle. In this case the current delivered to the load was noticeably affected when the fault occurred as the converter briefly operates in the overmodulation region to avoid using the potentially faulty cell. Operation in the overmodulation region is more apparent for the experimental data shown in Fig. 6.13, where a $sw_{2,C1}$ open-circuit fault occurs during the half-cycle where current does not flow through the faulty switch. The fault is not detected until current is supposed to flow through the switch, 4814 µs after the fault occurs. After the fault is isolated, cell 1 is soft-bypassed using the 0_U state as per step-one of the verification process. Because cell 1 is bypassed the maximum converter

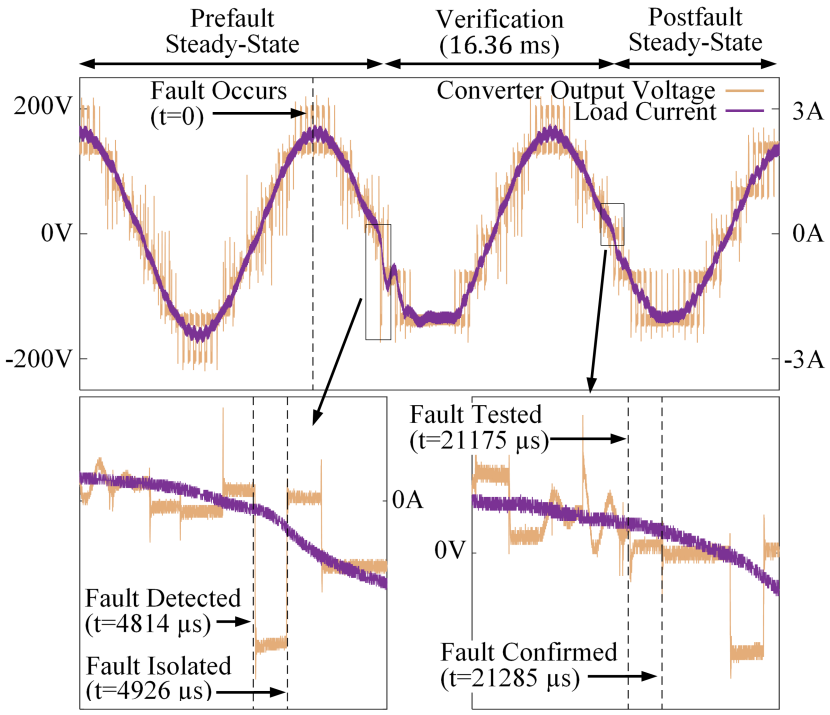


Fig. 6.13: Performance for an open-circuit fault in $sw_{1,C2}$ occurring during a non-affected cycle. Overmodulation is apparent due to the soft-bypass of the faulty cell during step one of the verification process.

output is 145 V and so overmodulation occurs. Once the fault is verified the reference is adjusted to prevent overmodulation.

Experimental data were also collected for simulated gate misfiring faults. As in the previous section, the simulated gate-misfiring fault caused the affected switch to appear as an open-circuit until its gate signal is cycled, i.e. the gate-misfiring fault was cleared once the gate signal was turned from conducting to non-conducting and back. Fig. 6.14 shows data for a $sw_{1,C2}$ gate misfiring fault occurring in the middle of a cycle. The fault occurs and is misidentified as an open-circuit fault within less than two measurement cycles. The suspected fault is then tested and cleared 12.45 ms after being detected, and steady-state operation then resumes with no reconfiguration necessary. Experimental data, shown in Fig. 6.15, were also collected for a $sw_{4,C1}$ gate misfiring fault occurring near the beginning of a cycle. The fault is detected

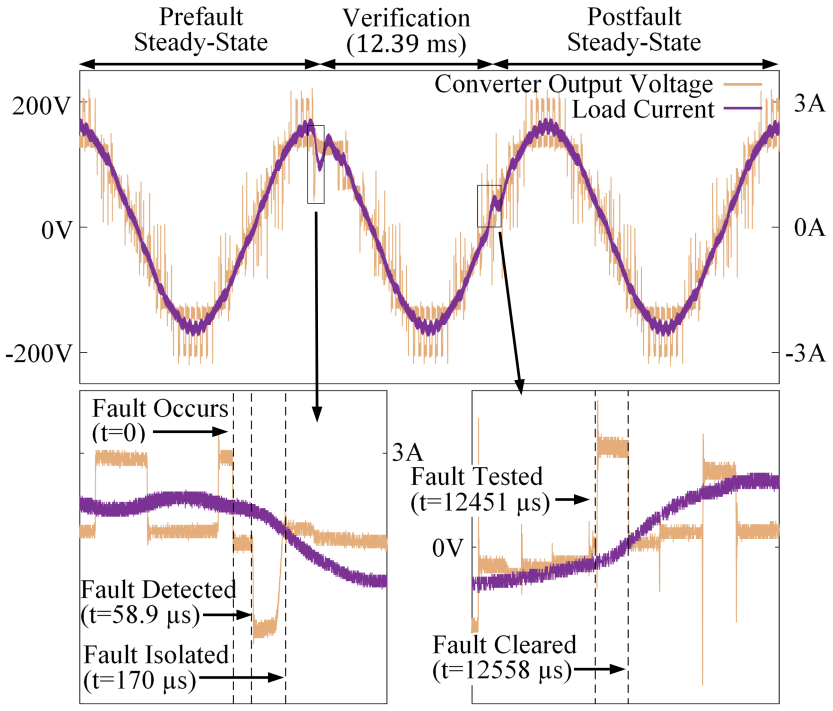


Fig. 6.14: Performance for an open-circuit fault in $sw_{2,C1}$ occurring during a non-affected cycle. Overmodulation is apparent due to the soft-bypass of the faulty cell during step one of the verification process.

and misclassified as an open-circuit fault. The potentially faulty cell is soft-bypassed during step-one of the three-step verification process, and therefore overmodulation briefly occurs. The suspected fault is tested and cleared 15.5 ms after being detected, and then steady-state operation resumes with no reconfiguration action necessary.

As given in Table 6.4, the cell input voltages for the CHB presented in this section were 60 V, 70 V, and 75 V. The CHB is therefore asymmetric, although not with input voltage ratios traditionally utilized in asymmetric CHB converters. Nonetheless, the PWM strategy used to generate gate signals for this asymmetric converter is distinct from the PWM scheme utilized for the symmetric CHB presented in the previous section. The proposed method for fault detection, isolation, and verification is therefore compatible for both symmetric and asymmetric converters. It is emphasized that no modifications to the proposed method are required when applying the proposed method

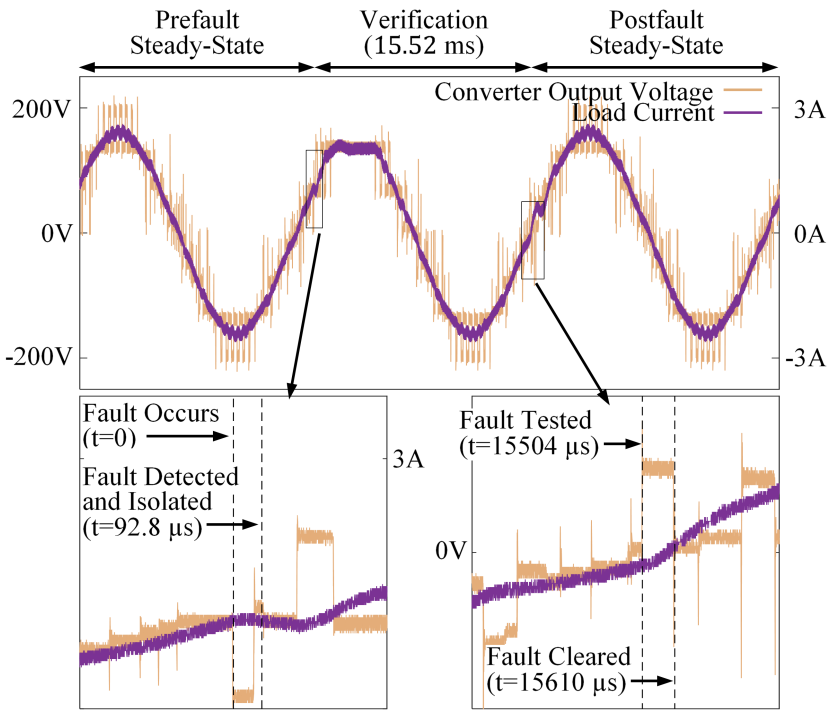


Fig. 6.15: Performance for a gate misfiring fault in $sw_{4,C1}$ occurring during a non-affected cycle. Overmodulation is apparent as the faulty cell is soft-bypassed during step one of the verification process.

to asymmetric CHB converters, as the PWM scheme used during prefault operation is independent of the fault isolation procedure.

6.5 Epsilon Selection

To enable open-circuit fault detection using the proposed technique, even with noise disturbances, ϵ is included in (6.1) and (6.2). Proper ϵ selection is facilitated by determining noise magnitudes which can cause undesirable algorithm performance. This analysis is achieved by adjusting the inequalities of (6.1) and (6.2) to include a noise term, v_N, as,

$$|(v_{LN} - v_E) + v_n + v_N| < \epsilon \tag{6.3}$$

and,

$$|(v_{LN} - v_E) - v_n + v_N| < \epsilon, \tag{6.4}$$

respectively.

Three scenarios where noise affects algorithm performance are described in subsections 6.5.1, 6.5.2, and 6.5.3, and in subsection 6.5.4 the impacts of this analysis on ϵ selection are summarized. Two cells of an asymmetric CHB, with $v_1 > v_2$, are considered here, though the results presented can be naturally extended to include more cells or symmetric voltages.

6.5.1 False Alarms

A false alarm, i.e. a fault detection during healthy converter operation, occurs when $v_{LN} = v_E$ and (6.1) or (6.2) are satisfied. Thus, from (6.3) and (6.4), a false alarm occurs if

$$\pm v_n - \epsilon < v_N < \pm v_n + \epsilon. \tag{6.5}$$

In the event of a false alarm, the fault location suspected will ultimately be classified as fault free during the verification process, though converter operation may be disrupted during the isolation and verification steps of the proposed technique. For two asymmetric CHB cells, the hashed areas of Fig. 6.16(a) show the range of $|v_N|$ satisfying (6.5) for each cell for a given ϵ.

6.5.2 Missed Detection

A missed detection occurs when (6.1) or (6.2) are not satisfied in the event of a fault. Ideally, for a cell n open-circuit fault,

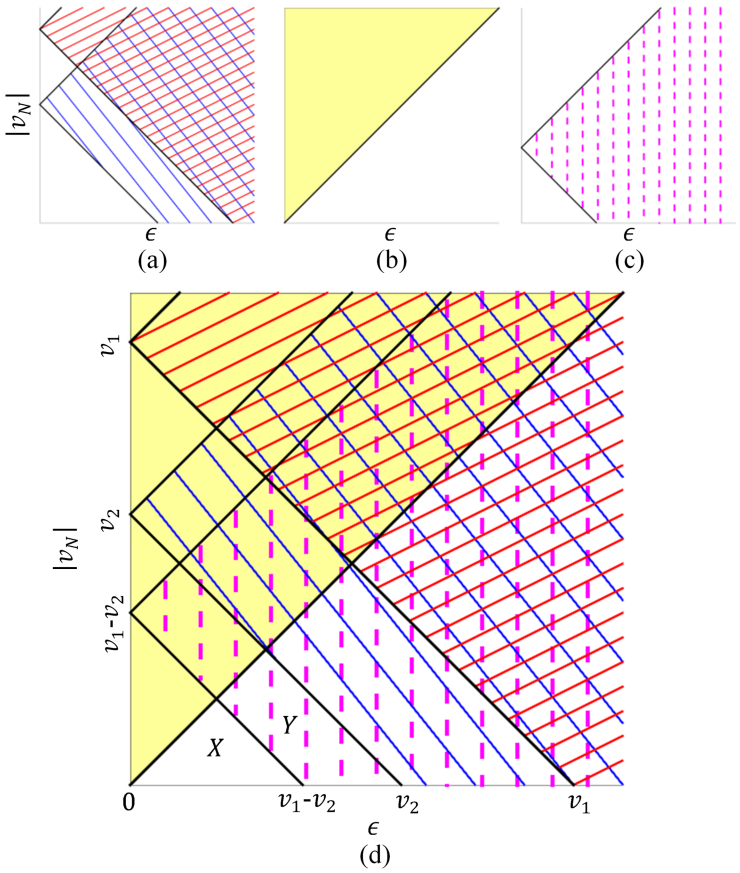


Fig. 6.16: Noise magnitudes, $|v_N|$, satisfying (6.5), (6.7), and (6.10) are shown for fixed ϵ in the shaded and hashed areas of (a), (b), and (c), respectively, for a two-cell asymmetric CHB leg. The union of these areas is shown in (d). When a fault initially occurs $|SW_F|$ is minimized if the system operates in region X of (d), though operation in either region X or region Y ensures no false flags or missed detections will occur.

$$v_{LN} - v_E = \begin{cases} -v_n & i > 0, \\ v_n & i < 0. \end{cases} \tag{6.6}$$

Applying (6.6) to (6.3) and (6.4), a missed detection occurs during a fault event if,

$$|v_N| > \epsilon. \tag{6.7}$$

For any CHB leg, the shaded area of Fig. 6.16(b) shows the range of $|v_N|$ satisfying

(6.7) for a given ϵ, as (6.7) is independent of the dc voltages used.

6.5.3 Minimizing $|SW_F|$

For open-circuit fault events in asymmetric CHBs, $|SW_F|$ can be minimized when the fault is initially detected if only the faulty cell satisfies (6.1) or (6.2). When applying (6.1) and (6.2) to cell m in the event of a cell n open-circuit fault, (6.6) can be applied to (6.3) and (6.4) as,

$$|-v_n + v_m + v_N| < \epsilon \tag{6.8}$$

and,

$$|v_n + v_m + v_N| < \epsilon. \tag{6.9}$$

Accordingly, $|SW_F|$ is not minimized if for any $m \neq n$,

$$\pm\left(v_n - v_m\right) - \epsilon < v_N < \pm(v_n - v_m) + \epsilon. \tag{6.10}$$

While the proposed open-circuit fault detection technique does not necessitate $|SW_F|$ minimization, reduced isolation time is required as $|SW_F|$ decreases. For two asymmetric CHB cells, the hashed area of Fig. 6.16(c) shows the range of $|v_N|$ satisfying (6.10) for a given ϵ.

6.5.4 Selecting ϵ

The shaded and hashed areas of Fig. 6.16(d) show the range of $|v_N|$ satisfying (6.5), (6.7), and (6.10) for a given ϵ when considering two asymmetric CHB cells. Inspecting Fig. 6.16(d), it is clear that false alarms, missed detections, and minimization of $|SW_F|$

can be achieved for the greatest $|v_N|$ by setting $\epsilon = (v_1 - v_2)/2$, as was done for the experimental setup described in Section 6.4. If this value does not provide sufficient noise immunity to missed detections, of if a symmetric CHB is used, then setting $\epsilon = v_2/2$ allows the greatest $|v_N|$ while preventing false alarms and missed detections.

Ultimately, while the presented analysis may facilitate ϵ selection, a system designer may determine it is advantageous to adjust ϵ upon considering the consequences of false alarms and missed detections. That is, since healthy operation is the most frequent operating state for a converter, a system designer may choose to decrease false alarm probability by reducing ϵ. On the other hand, ϵ may be increased by a system designer to reduce the probability of missed detection in the event of an open-circuit fault.

6.6 Conclusion

A method for detecting open-circuit faults in CHB multilevel converters has been presented in this chapter. It has been verified using simulation and experimentally obtained data that the presented procedure for fault detection, isolation, and verification enables open-circuit faults to be identified in less than one fundamental cycle. This method: *(i)* is designed to be implemented independently for each CHB leg, *(ii)* requires one voltage sensor and one current sensor for each leg, *(iii)* identifies and isolates faults in less than $2M$ measurement cycles for an M cell CHB leg, and verifies faults in less than one fundamental cycle, *(iv)* is independent of the PWM strategy used, and *(v)* can be implemented in symmetric and asymmetric CHB converters.

Chapter 7

Conclusions and Suggestions for Future Work

In this chapter, the primary contributions of this dissertation are reviewed in Section 7.1. Suggestions for future investigations, building upon the work presented in this dissertation, are presented in Section 7.2.

7.1 Summary and Conclusions

Methods to facilitate continued dc-ac converter operation during internal and external abnormalities have been presented in this dissertation. Motivation and background information detailing the necessity of fault tolerant methods has been provided as an introduction. Moreover, the introductory chapter presented a literature review which outlined state-of-the-art protection schemes as well as the challenges which must be overcome to increase the fault tolerance of dc-ac converters, with a particular emphasis placed on the cascaded H-bridge multilevel converter topology, which is at the center of many of the techniques presented within this dissertation.

The working principles of multilevel CHB converters have been presented in this dissertation, with the LSPWM and hybrid PWM techniques detailed as two carrier-based schemes for modulating the output of CHB legs. The linear-range and overmodulation behavior of these PWM methods has been reviewed, with third-harmonic injection presented as a commonly used technique to increase dc bus utilization, extending the linear PWM region by approximately 15% during nominal operating conditions. Additionally, an overview of the FPSC method has been provided to demonstrate a commonly utilized approach for enabling continued operation of three-phase CHB after internal fault events, i.e. after CHB cells are bypassed.

This dissertation introduced the concept of PQ plane analysis as an approach to assess converter performance during operation under nominal and fault conditions for varying parameters such as filter values and dc bus voltages. The presented approach evaluates all possible converter outputs, making it a flexible technique which can be implemented for many converter topologies regardless of the control or PWM schemes used. Once all possible outputs are identified, the operating region for a converter can then be identified by eliminating converter output points which are unfeasible due to practical considerations such as component VA limitations. This dissertation also introduced a load-independent technique to identify discordant converter operation for asymmetric CHB converters. Identification of this discordant operation is essential due to the potential for deleterious effects resulting from extended operation at a discordant output point.

Moreover, an atypical PWM technique has been demonstrated in this dissertation as a method to enable dc bus maximization for converters operating under nominal and faulty conditions. While this approach can be implemented in a wide range of dc-ac converter topologies, its application to CHB converters facilitates continued converter operation after cell fault events. This atypical PWM method computes the

common-mode component to be injected into PWM references in real-time by comparing references to the maximum voltages producible by CHB legs. The atypical PWM technique acts as an intermediary step between reference and gate signal generation, making it compatible with any control method and any carrier-based PWM scheme.

This dissertation further introduced adaptive sinusoidal PWM, an approach to enable CHB to directly utilize time-variant dc sources. The sensor-per-source and sensor-per-leg algorithms have been presented as alternative methods to implement ASPWM, providing a trade off between converter performance and the required sensor circuitry. Modifications to this technique have been presented to enable design criteria to be met. The proposed alterations satisfy design criteria by preventing certain switching states from being utilized during part of, or an entire, reference period.

Additionally, a method to identify, isolate, and verify open-circuit IGBT faults in a CHB leg has been presented in this dissertation. This method only requires measurement of a CHB leg's current and output voltage, is compatible with any PWM scheme, and can be applied to symmetric and asymmetric CHB. Measured voltages are compared to expected voltages, and deviations are used to determine open-circuit fault locations based on the deviation's magnitude and current flow direction. For a CHB leg with M cells, the proposed technique identifies and isolates open-circuit switch faults in less than $2M$ measurement (sampling) cycles, and the verification process, which reduces the possibility of unnecessary corrective actions due to fault misidentification, is completed in less than one full fundamental cycle.

All techniques developed and presented in this dissertation have been validated via MATLAB/Simulink simulation results, as well as data obtained experimentally using a laboratory-scale CHB converter.

Ultimately, the methods presented herein provide tools to analyze and enable continued converter operation during non-ideal operating conditions. These techniques

can be jointly integrated into a system to provide fault tolerance for a wide range of fault events. However, since the presented techniques are not necessarily codependent, they can also be implemented individually to provide systems with specific layers of protection.

7.2 Suggestions for Future Work

In this dissertation, new techniques to facilitate converter operation under abnormal conditions have been presented and validated. There are, however, some opportunities to further analyze and build on the work introduced herein.

An analytical technique to analyze the PQ plane behavior of grid-interactive converters has been presented in Chapter 3. The proposed approach could be expanded to enable its application under a wider range of non-ideal conditions, such when a converter is connected to a weak grid.

In Chapter 5, the sensor-per-source and sensor-per-leg algorithms have been introduced. A generalized sensor-per-n-cell approach could be developed to provide system designers the freedom to select a balance between the number of sensors required and the time required for voltage source identification, particularly for CHB with many cells. Moreover, an approach to adjust CHB PWM schemes to modify, or entirely eliminate, discordant points was also introduced. However, optimal techniques to eliminate the discordant operation could be developed.

The method for fault identification, isolation, and verification proposed in Chapter 6 has been designed with the assumption that CHB cells fail separately. However, the proposed approach could be expanded to enable operation during simultaneous fault events, i.e. when destructive conditions cause multiple failures within a CHB leg.

An approach for maximizing dc bus utilization in grid-interactive converters has

been introduced In Chapter 4. This approach could be expanded to enable operation in the overmodulation region. Moreover, the efficiency of converters using the proposed atypical PWM scheme could investigated, as the reduced switching events during the clipped portions of the reference waveforms may increase system efficiency.

Bibliography

[1] H. W. Sim, J. S. Lee, and K. B. Lee, "Detecting open-switch faults: Using asymmetric zero-voltage switching states," *IEEE Ind. Appl. Mag.*, vol. 22, no. 2, pp. 27–37, Mar. 2016.

[2] L. Sun, Z. Wu, F. Xiao, X. Cai, and S. Wang, "Suppression of real power back flow of nonregenerative cascaded h-bridge inverters operating under faulty conditions," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5161–5175, Jul. 2016.

[3] J. Lamb and B. Mirafzal, "An adaptive SPWM technique for cascaded multilevel converters with time-variant dc sources," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4146–4155, Sep. 2016.

[4] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[5] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[6] U. M. Choi, H. G. Jeong, K. B. Lee, and F. Blaabjerg, "Method for detecting an open-switch fault in a grid-connected NPC inverter system," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2726–2739, Jun. 2012.

[7] F. Deng, Y. Tian, R. Zhu, and Z. Chen, "Fault-tolerant approach for modular multilevel converters under submodule faults," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7253–7263, Nov. 2016.

[8] P. Lezana, R. Aguilera, and J. Rodriguez, "Fault detection on multicell converter based on output voltage frequency analysis," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2275–2283, Jun. 2009.

[9] S. Khomfoi and L. M. Tolbert, "Fault diagnosis and reconfiguration for multilevel inverter drive using AI-based techniques," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2954–2968, Dec. 2007.

[10] Y. Song and B. Wang, "Survey on reliability of power electronic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 591–604, Jan. 2013.

[11] U. M. Choi, F. Blaabjerg, and K. B. Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2517–2533, May. 2015.

[12] B. Gou, X. Ge, S. Wang, X. Feng, J. B. Kuo, and T. G. Habetler, "An open-switch fault diagnosis method for single-phase PWM rectifier using a model-based approach in high-speed railway electrical traction drive system," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3816–3826, May 2016.

[13] L. M. A. Caseiro and A. M. S. Mendes, "Real-time IGBT open-circuit fault diagnosis in three-level neutral-point-clamped voltage-source rectifiers based on

instant voltage error," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1669–1678, Mar. 2015.

[14] M. A. Rodríguez-Blanco, A. Vázquez-Pprez, L. Hernández-González, V. Golikov, J. Aguayo-Alquicira, and M. May-Alarcón, "Fault detection for IGBT using adaptive thresholds during the turn-on transient," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1975–1983, Mar. 2015.

[15] P. Garg, S. Essakiappan, H. S. Krishnamoorthy, and P. N. Enjeti, "A fault-tolerant three-phase adjustable speed drive topology with active common-mode voltage suppression," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2828–2839, May 2015.

[16] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. . M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[17] S. M. Jung, J. S. Park, H. W. Kim, K. Y. Cho, and M. J. Youn, "An MRAS-based diagnosis of open-circuit fault in PWM voltage-source inverters for PM synchronous motor drive systems," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2514–2526, May 2013.

[18] Q. Yang, J. Qin, and M. Saeedifard, "Analysis, detection, and location of open-switch submodule failures in a modular multilevel converter," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 155–164, Feb. 2016.

[19] R. Picas, J. Zaragoza, J. Pou, and S. Ceballos, "Reliable modular multilevel converter fault detection with redundant voltage sensor," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 39–51, Jan. 2017.

[20] A. K. Jain and V. T. Ranganathan, "V_{CE} sensing for IGBT protection in NPC three level converters- causes for spurious trippings and their elimination," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 298–307, Jan. 2011.

[21] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May 2011.

[22] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3720–3732, Jul. 2014.

[23] N. M. A. Freire, J. O. Estima, and A. J. M. Cardoso, "A voltage-based approach without extra hardware for open-circuit fault diagnosis in closed-loop PWM AC regenerative drives," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4960–4970, Sep. 2014.

[24] B. Mirafzal, "Survey of fault-tolerance techniques for three-phase voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5192–5202, Oct. 2014.

[25] M. Naidu, S. Gopalakrishnan, and T. W. Nehl, "Fault-tolerant permanent magnet motor drive topologies for automotive x-by-wire systems," *IEEE Trans. Ind. Appl.*, vol. 46, no. 2, pp. 841–848, Mar. 2010.

[26] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014.

[27] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan. 1999.

[28] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 459–469, Mar. 2006.

[29] A. Gholizad and M. Farsadi, "A novel state-of-charge balancing method using improved staircase modulation of multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6107–6114, Oct. 2016.

[30] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[31] G. Wang, G. Konstantinou, C. D. Townsend, J. Pou, S. Vazquez, G. D. Demetriades, and V. G. Agelidis, "A review of power electronics for grid connection of utility-scale battery energy storage systems," *IEEE Trans. Sustain. Energy*, vol. 7, no. 4, pp. 1778–1790, Oct. 2016.

[32] X. Yuan, "Derivation of voltage source multilevel converter topologies," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 966–976, Feb. 2017.

[33] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[34] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded h-bridge multilevel pv inverter with distributed mppt for grid-connected applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, Mar. 2015.

[35] Y. Yu, G. Konstantinou, B. Hredzak, and V. G. Agelidis, "Operation of cascaded h-bridge multilevel converters for large-scale photovoltaic power plants under

bridge failures," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7228–7236, Nov. 2015.

[36] Y. Yu, G. Konstantinou, B. Hredzak, and V. G. Agelidis, "Power balance optimization of cascaded h-bridge multilevel converters for large-scale photovoltaic integration," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1108–1120, Feb. 2016.

[37] C. M. Young, N. Y. Chu, L. R. Chen, Y. C. Hsiao, and C. Z. Li, "A single-phase multilevel inverter with battery balancing," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1972–1978, May 2013.

[38] Y. Yu, G. Konstantinou, B. Hredzak, and V. G. Agelidis, "Power balance of cascaded h-bridge multilevel converters for large-scale photovoltaic integration," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 292–303, Jan. 2016.

[39] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power cycle testing of power switches: A literature survey," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2465–2473, May 2015.

[40] *Military handbook reliability prediction of electronic equipment.* Department of Defense, 1991.

[41] F. Wu and J. Zhao, "Current similarity analysis-based open-circuit fault diagnosis for two-level three-phase PWM rectifier," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3935–3945, May 2017.

[42] P. Lezana and G. Ortiz, "Extended operation of cascade multicell converters under fault condition," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2697–2703, Jul. 2009.

[43] D. Hirschmann, D. Tissen, S. Schroder, and R. W. D. Doncker, "Reliability prediction for inverters in hybrid electrical vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2511–2517, Nov. 2007.

[44] B. Lu and S. K. Sharma, "A literature review of IGBT fault diagnostic and protection methods for power inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1770–1777, Sep. 2009.

[45] J. Lamb and B. Mirafzal, "Open-circuit IGBT fault detection and location isolation for cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4846–4856, Jun. 2017.

[46] B. Li, S. Shi, B. Wang, G. Wang, W. Wang, and D. Xu, "Fault diagnosis and tolerant control of single IGBT open-circuit failure in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3165–3176, Apr. 2016.

[47] M. Quraan, T. Yeo, and P. Tricoli, "Design and control of modular multilevel converters for battery electric vehicles," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 507–517, Jan. 2016.

[48] J. I. Y. Ota, T. Sato, and H. Akagi, "Enhancement of performance, availability, and flexibility of a battery energy storage system based on a modular multilevel cascaded converter (mmcc-ssbc)," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2791–2799, Apr. 2016.

[49] L. A. Tolbert, F. Z. Peng, T. Cunnyngham, and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1058–1064, Oct. 2002.

[50] M. Y. Kim, C. H. Kim, J. H. Kim, and G. W. Moon, "A chain structure of switched capacitor for improved cell balancing speed of lithium-ion batteries," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3989–3999, Aug. 2014.

[51] D. Stimoniaris, D. Tsiamitros, and E. Dialynas, "Improved energy storage management and pv-active power control infrastructure and strategies for microgrids," *IEEE Trans. Power Syst.*, vol. 31, no. 1, pp. 813–820, Jan. 2016.

[52] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, "Control of power converters in ac microgrids," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4734–4749, Nov. 2012.

[53] A. Merabet, K. T. Ahmed, H. Ibrahim, R. Beguenane, and A. M. Y. M. Ghias, "Energy management and control system for laboratory scale microgrid based wind-pv-battery," *IEEE Trans. Sustain. Energy*, vol. 8, no. 1, pp. 145–154, Jan. 2017.

[54] M. Chen and G. A. Rincon-Mora, "Accurate electrical battery model capable of predicting runtime and I-V performance," *IEEE Trans. Energy Convers.*, vol. 21, no. 2, pp. 504–511, Jun. 2006.

[55] A. Hentunen, T. Lehmuspelto, and J. Suomela, "Time-domain parameter extraction method for thévenin-equivalent circuit battery models," *IEEE Trans. Energy Convers.*, vol. 29, no. 3, pp. 558–566, Sep. 2014.

[56] R. C. Kroeze and P. T. Krein, "Electrical battery model for use in dynamic electric vehicle simulations," in *Proc.IEEE Power Electron.Specialists Conf.*, Jun. 2008, pp. 1336–1342.

[57] M. Uno and A. Kukita, "Bidirectional PWM converter integrating cell voltage equalizer using series-resonant voltage multiplier for series-connected energy storage cells," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3077–3090, Jun. 2015.

[58] S. M. Lukic, J. Cao, R. C. Bansal, F. Rodriguez, and A. Emadi, "Energy storage systems for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2258–2267, Jun. 2008.

[59] A. Affanni, A. Bellini, G. Franceschini, P. Guglielmi, and C. Tassoni, "Battery choice and management for new-generation electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1343–1349, Oct. 2005.

[60] M. Hamzeh, S. Emamian, H. Karimi, and J. Mahseredjian, "Robust control of an islanded microgrid under unbalanced and nonlinear load conditions," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 512–520, Jun. 2016.

[61] M. Zachar and P. Daoutidis, "Microgrid/macrogrid energy exchange: A novel market structure and stochastic scheduling," *IEEE Trans. Smart Grid*, vol. 8, no. 1, pp. 178–189, Jan. 2017.

[62] F. Chen, M. Chen, Q. Li, K. Meng, Y. Zheng, J. M. Guerrero, and D. Abbott, "Cost-based droop schemes for economic dispatch in islanded microgrids," *IEEE Trans. Smart Grid*, vol. 8, no. 1, pp. 63–74, Jan. 2017.

[63] Y. Han, P. Shen, X. Zhao, and J. M. Guerrero, "An enhanced power sharing scheme for voltage unbalance and harmonics compensation in an islanded ac microgrid," *IEEE Trans. Energy Convers.*, vol. 31, no. 3, pp. 1037–1050, Sep. 2016.

[64] L. Liu, H. Li, Y. Xue, and W. Liu, "Reactive power compensation and optimization strategy for grid-interactive cascaded photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 188–202, Jan. 2015.

[65] S. Essakiappan, H. S. Krishnamoorthy, P. Enjeti, R. S. Balog, and S. Ahmed, "Multilevel medium-frequency link inverter for utility scale photovoltaic integration," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3674–3684, Jul. 2015.

[66] I. U. Nutkani, P. C. Loh, P. Wang, and F. Blaabjerg, "Decentralized economic dispatch scheme with online power reserve for microgrids," *IEEE Trans. Smart Grid*, vol. 8, no. 1, pp. 139–148, Jan. 2017.

[67] J. He, Y. W. Li, and F. Blaabjerg, "An enhanced islanding microgrid reactive power, imbalance power, and harmonic power sharing scheme," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3389–3401, Jun. 2015.

[68] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[69] I. Ahmed, V. B. Borghate, A. Matsa, P. M. Meshram, H. M. Suryawanshi, and M. A. Chaudhari, "Simplified space vector modulation techniques for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8483–8499, Dec. 2016.

[70] Z. Du, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, "DC-AC cascaded h-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications," *IEEE Trans. Ind. Appl.*, vol. 45, no. 3, pp. 963–970, May 2009.

[71] Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded h-bridge multilevel inverter," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 25–33, Jan. 2009.

[72] J. Pereda and J. Dixon, "23-level inverter for electric vehicles using a single battery pack and series active filters," *IEEE Trans. Veh. Technol.*, vol. 61, no. 3, pp. 1043–1051, Mar. 2012.

[73] W. Qian, H. Cha, F. Z. Peng, and L. M. Tolbert, "55-kW variable 3x dc-dc converter for plug-in hybrid electric vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1668–1678, Apr. 2012.

[74] Y. Chen, X. Liu, Y. Cui, J. Zou, and S. Yang, "A multiwinding transformer cell-to-cell active equalization method for lithium-ion batteries with reduced number of driving circuits," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4916–4929, Jul. 2016.

[75] H. S. Park, C. H. Kim, K. B. Park, G. W. Moon, and J. H. Lee, "Design of a charge equalizer based on battery modularization," *IEEE Trans. Veh. Technol.*, vol. 58, no. 7, pp. 3216–3223, Sep. 2009.

[76] E. Behrouzian and M. Bongiorno, "Investigation of negative-sequence injection capability of cascaded h-bridge converters in star and delta configuration," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1675–1683, Feb. 2017.

[77] J. Rodriguez, P. W. Hammond, J. Pontt, R. Musalem, P. Lezana, and M. J. Escobar, "Operation of a medium-voltage drive under faulty conditions," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1080–1085, Aug. 2005.

[78] F. Carnielutti, H. Pinheiro, and C. Rech, "Generalized carrier-based modulation strategy for cascaded multilevel converters operating under fault conditions," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 679–689, Feb. 2012.

[79] W. Yao, H. Hu, and Z. Lu, "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 45–51, Jan. 2008.

[80] M. Aleenejad, H. Mahmoudi, and R. Ahmadi, "Unbalanced space vector modulation with fundamental phase shift compensation for faulty multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7224–7233, Oct. 2016.

[81] M. Aleenejad, H. Mahmoudi, P. Moamaei, and R. Ahmadi, "A new fault-tolerant strategy based on a modified selective harmonic technique for three-phase multilevel converters with a single faulty cell," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3141–3150, Apr. 2016.

[82] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak, "A review of passive power filters for three-phase grid-connected voltage-source converters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 54–69, Mar. 2016.

[83] Y. Liu, W. Wu, Y. He, Z. Lin, F. Blaabjerg, and H. S. H. Chung, "An efficient and robust hybrid damper for lcl - or llcl -based grid-tied inverter with strong grid-side harmonic voltage effect rejection," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 926–936, Feb. 2016.

[84] J. Lamb and B. Mirafzal, "Active and reactive power operational region for grid-tied inverters," in *Proc. 7th Int. Symp. Power Electron. Distributed Generation Syst. (PEDG)*, Jun. 2016, pp. 1–6.

[85] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[86] A. Edpuganti and A. K. Rathore, "A survey of low switching frequency modulation techniques for medium-voltage multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 4212–4228, Sep. 2015.

[87] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[88] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2688–2701, May 2016.

[89] Y. Deng, Y. Wang, K. H. Teo, and R. G. Harley, "A simplified space vector modulation scheme for multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1873–1886, Mar. 2016.

[90] Z. Du, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, "Reduced switching-frequency active harmonic elimination for multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1761–1770, Apr. 2008.

[91] M. S. A. Dahidah and V. G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1620–1630, Jul. 2008.

[92] M. Najjar, A. Moeini, M. K. Bakhshizadeh, F. Blaabjerg, and S. Farhangi, "Optimal selective harmonic mitigation technique on variable dc link cascaded h-

bridge converter to meet power quality standards," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1107–1116, Sep. 2016.

[93] J. Napoles, A. J. Watson, J. J. Padilla, J. I. Leon, L. G. Franquelo, P. W. Wheeler, and M. A. Aguirre, "Selective harmonic mitigation technique for cascaded h-bridge converters with nonequal dc link voltages," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1963–1971, May 2013.

[94] M. Angulo, P. Lezana, S. Kouro, J. Rodriguez, and B. Wu, "Level-shifted PWM for cascaded multilevel inverters with even power distribution," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Jun. 2007, pp. 2373–2378.

[95] J. I. Leon, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, S. Kouro, and J. Rodriguez, "Two-dimensional modulation technique for multilevel cascaded h-bridge converters," in *Proc. IEEE Int. Conf. Ind. Technol.*, Feb. 2009, pp. 1–6.

[96] J. Lamb and B. Mirafzal, "An adaptive SPWM technique for cascaded multilevel converters," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2015, pp. 703–708.

[97] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.

[98] S. Adhikari, F. Li, and H. Li, "P-Q and P-V control of photovoltaic generators in distribution systems," *IEEE Trans. Smart Grid*, vol. 6, no. 6, pp. 2929–2941, Nov. 2015.

[99] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[100] S. Kouro, R. Bernal, H. Miranda, C. A. Silva, and J. Rodriguez, "High-performance torque and flux control for multilevel inverter fed induction motors," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2116–2123, Nov. 2007.

[101] Y. Wang, X. Wang, Z. Chen, and F. Blaabjerg, "Distributed optimal control of reactive power and voltage in islanded microgrids," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 340–349, Jan. 2017.

[102] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 654–664, Mar. 2009.

[103] "IEEE recommended practices and requirements for harmonic control in electrical power systems," *IEEE Std 519-1992*, pp. 1–112, Apr. 1993.

[104] C. Rech and J. R. Pinheiro, "Impact of hybrid multilevel modulation strategies on input and output harmonic performances," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 967–977, May 2007.

[105] P. Lezana, J. Pou, T. A. Meynard, J. Rodriguez, S. Ceballos, and F. Richardeau, "Survey on fault operation on multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2207–2218, Jul. 2010.

[106] J. Lamb and B. Mirafzal, "Active and reactive power operational region for grid-interactive cascaded h-bridge multilevel converters," in *Proc. of 2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–6.

[107] J. Lamb, A. Singh, and B. Mirafzal, "Rapid implementation of solid-state based converters in power engineering laboratories," *IEEE Trans. Power Syst.*, vol. 31, no. 4, pp. 2957–2964, Jul. 2016.

[108] G. Farivar, B. Hredzak, and V. G. Agelidis, "A dc-side sensorless cascaded h-bridge multilevel converter-based photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4233–4241, Jul. 2016.

Appendix A

FPGA for Rapid Prototyping

Field programmable gate arrays (FPGAs) offer several important benefits when used for prototyping solid-state based power converters. Compared to other commonly used controllers, such as dSPACE, FPGAs cost less, enable increased switching speeds, and offer an increased number of general-purpose input/output (GPIO) ports. For multi-level converters, the increased availability of GPIO ports is especially important due to the increased number gating signals required. However, FPGA programming requires a hardware description language (HDL) such as very high speed integrated circuit HDL (VHDL) or Verilog. Instead of spending time mastering an HDL language, it is possible to utilize MATLAB/Simulink toolboxes to generate HDL code from a compatible Simulink model, thereby allowing control schemes and pulse width modulation (PWM) switching patterns to be rapidly prototyped. In addition to use for power electronics research, the approach of FPGA programming using MATLAB/Simulink software has been identified as an appealing option for use in educational undergraduate laboratories [107].

To program the FPGA using Simulink's HDL coder, a model must be created using only HDL compatible blocks and user written functions. Once such a model has been

developed, the user can attempt to generate HDL code by pressing a button on the Simulink toolbar. If the code generation is unsuccessful then a message describing the error appears, and if the code generation is successful then VHDL code is generated for the overall model, including any subsystems and user made functions. The generated VHDL code can then be loaded and compiled in Quartus II. If compilation is unsuccessful, often the result of a non-compatible data type being used, changes can be made to the Simulink model and HDL code can be generated again. If the compilation is successful, then the FPGA specific input and output pins can be assigned, and the program can be loaded into an FPGA. Finally, the Simulink model must be edited if more modifications are required due to unexpected experimental behavior. A flow diagram outlining this process is shown in Fig. A.1. Going from a compatible Simulink model to a programmed FPGA takes minutes, allowing for rapid prototyping of controller models and switching patterns.

One of the primary difficulties of using the HDL coder is that the data types used in a Simulink model must be carefully chosen in order for the VHDL code generated to be compiled in Quartus II. To overcome this difficulty, the double and single data types must be avoided, a hurdle which can be overcome using the fixed-point data type made available through the Fixed-Point Designer Toolbox. When using the fixed-point data type, the signedness, word length, and fractional length of a variable can be specified, allowing for arbitrary precision.

Many useful Simulink models can be converted to VHDL code using Simulink's HDL coder even though not all Simulink blocks are HDL compatible. A wide array of open-loop control can be implemented using only HDL compatible blocks, and closed-loop control can be realized if an analog-to-digital converter (ADC) is used with the FPGA. Moreover, it is possible to interface FPGA with a more versatile controller, such as dSPACE, enabling desirable features of both devices to be utilized. One method

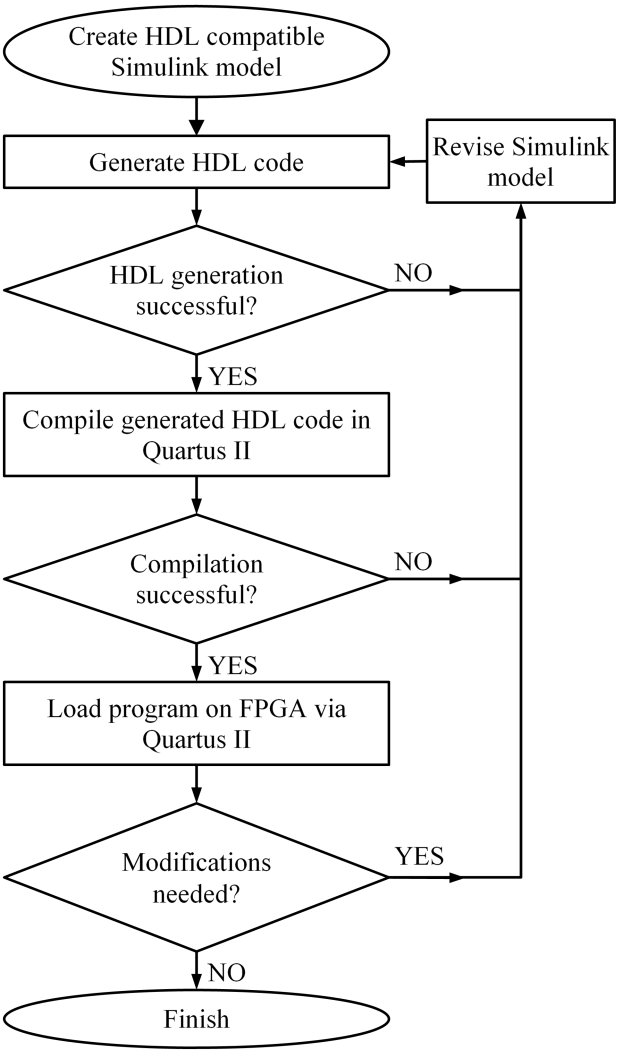


Fig. A.1: Flow diagram for the proposed development process.

to do this is to generate PWM reference waveforms using the versatile controller, e.g. dSPACE, and send the references to the FPGA. A carrier waveform, generated in the FPGA, can then be compared to the received PWM references to generate gate signals. This approach allows complex control algorithms, such as PQ control, to be more easily implemented than if only an FPGA were utilized. When interfacing an FPGA with dSPACE, improper communication between the devices may cause an erroneous reference can be used. One simple approach for interfacing the two devices

is to have the FPGA detect changes sent by dSPACE, and then allow some time, e.g. 10 FPGA clock cycles, to elapse before the received value is treated as finalized.

A.1 Waveform Generation

To demonstrate the HDL coder's functionality, models for generating sawtooth, pulse, triangular, and sinusoidal waveforms are presented in this section.

When using Simulink's HDL coder for waveform generation, the counter block is commonly used. When used in an FPGA, the counter's output, initially zero, increases by one at every rising clock edge, and once a preset limit is reached the counter's output is reset to zero and the process repeats. A sawtooth waveform can be realized by only using a counter. If the upper limit, $P \in \mathbb{N}$, of a counter is known, then the frequency of the sawtooth wave generated is $f = \frac{f_{FPGA}}{P+1}$, where f_{FPGA} is the clock speed of the FPGA used. Alternatively, if the desired waveform frequency is known then the upper limit can be found as $P = \frac{f_{FPGA}}{f} - 1$, rounding as necessary. In many cases $(\frac{f_{FPGA}}{f}) \gg 1$, and so setting $P = \frac{f_{FPGA}}{f}$ is a sufficient approximation. By using available arithmetic blocks, the amplitude and dc offset of the sawtooth wave can be modified as desired.

Experiments involving dc-dc converters or controlled rectifiers often require pulse waveforms, which can be generated by comparing the output of a counter, with upper limit P, against the constant value $D \cdot P \in [0, P]$, as shown in Fig. A.2. Using this model, the pulse wave has frequency $f = \frac{f_{FPGA}}{P+1}$ and duty ratio D. This model can be modified to make the waveform's frequency and duty ratio real-time adjustable using an FPGA's IO ports. At high frequencies the sawtooth waveform generated using a counter has a low number of steps in each period, resulting in readily evident discretization which, depending on the application, must be accounted for. For instance, suppose the model in Fig. A.2 uses a counter with upper limit $P = 3$ and the program

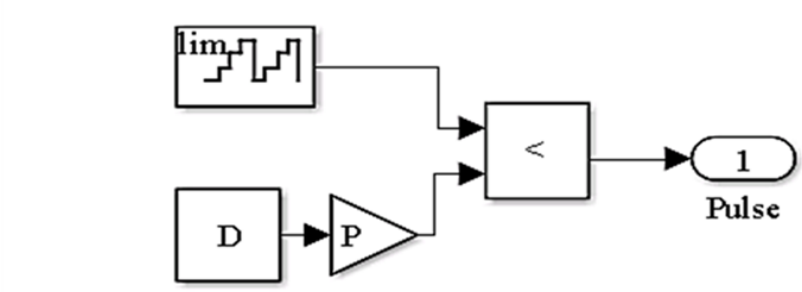


Fig. A.2: Simulink model used to generate a pulse waveform with duty ratio D.

is implemented on an FPGA with 50 MHz clock frequency. The resultant pulse waveform will have a 12.5 MHz frequency, but the only realizable duty ratios will be 0, 0.33, 0.66, and 1, since the sawtooth waveform is made using only four discrete values. The sawtooth wave's frequency must be decreased, or the FPGA clock frequency increased, if more duty ratio options are desired.

When implementing SPWM and other control methods, triangular waveforms with no dc component and unity amplitude are often useful. One approach for generating such a waveform is to use a counter's output for the increasing half of the waveform, and then subtract the counter's output from a constant to generate the decreasing half of the waveform. The waveform can then be shifted and scaled to have a zero average value and unity amplitude. A Simulink model demonstrating this method for generating triangular waveforms is shown in Fig. A.3. If the counter has upper limit P, the triangular wave frequency is obtained as $f = \frac{f_{FPGA}}{P+1}$.

It is also possible to create MATLAB functions which can be used to generate HDL. For instance, as an alternative to the model shown in Fig. A.3, the code in Fig. A.4 can be used to generate a triangular waveform with frequency $f = \frac{f_{FPGA}}{4P}$. Note that P is passed to the function as a parameter in the model shown to simplify the model by decreasing clutter. The triangular output generated using the given code does not have unity amplitude to prevent rounding errors. A gain block can be used, however,

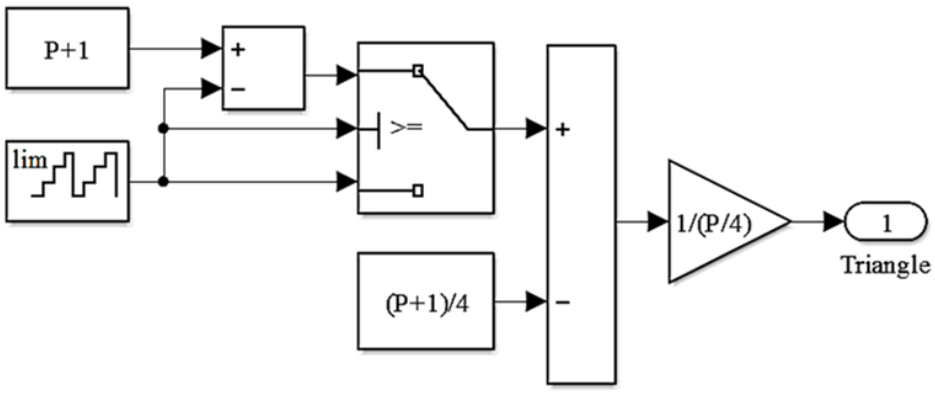


Fig. A.3: Simulink model used to generate a triangular waveform with unity amplitude and zero dc offset.

Fig. A.4: HDL-Compatible MATLAB function used to generate a triangular waveform with no dc component.

to adjust the amplitude of the triangular wave as desired. The following should be noted when writing MATLAB code for use in an FPGA:

1. Data types must be explicitly set. If, for instance, Fig. A.4 was changed from CurrentValue=int16(0) to CurrentValue=0, the CurrentValue variable would be stored as a double data type, which cannot be used in the Quartus II environment.

2. Use of persistent variables, which retain their values between function calls, can be beneficial.

3. User written MATLAB functions may not be HDL compatible, notably when some built-in functions such as **sin**() or **cos**() are utilized.

Finally, lookup tables can be used to make other waveforms of interest. In order to limit the amount of data which must be stored on the FPGA, however, a model must be created for a slow counter, i.e. a counter which changes its output only after K FPGA clock cycles. A slow counter can be implemented by placing a counter with upper limit P in a rising edge triggered subsystem, as shown at the bottom of Fig. A.5. The slow counter subsystem is triggered using a second counter, with upper limit $K-1$, for instance by comparing zero to the second counter's output. Using this model, the frequency of the slow counter is $f = \frac{f_{FPGA}}{K(P+1)}$.

As an example, a zero-order hold discretization of a sinusoidal waveform can be generated using a lookup table and a slow counter. To use a lookup table to generate a periodic waveform, the desired number of evenly spaced samples, n, within one period must be determined. Once n is known the lookup table can be set to output $A\sin\left(\frac{2\pi}{n}\left[0:n-1\right]\right)$, corresponding to slow counter output $m \in \{0, 1, \ldots, n-1\}$. If the slow counter increments every K clock cycles, then the generated sinusoid will have frequency $f = \frac{f_{FPGA}}{Kn}$. A Simulink model showing a slow counter controlled lookup table is shown in Fig. A.5. It is worth emphasizing that any waveform can be made using a lookup table, the process of generating a sinusoid was chosen for demonstration purposes only.

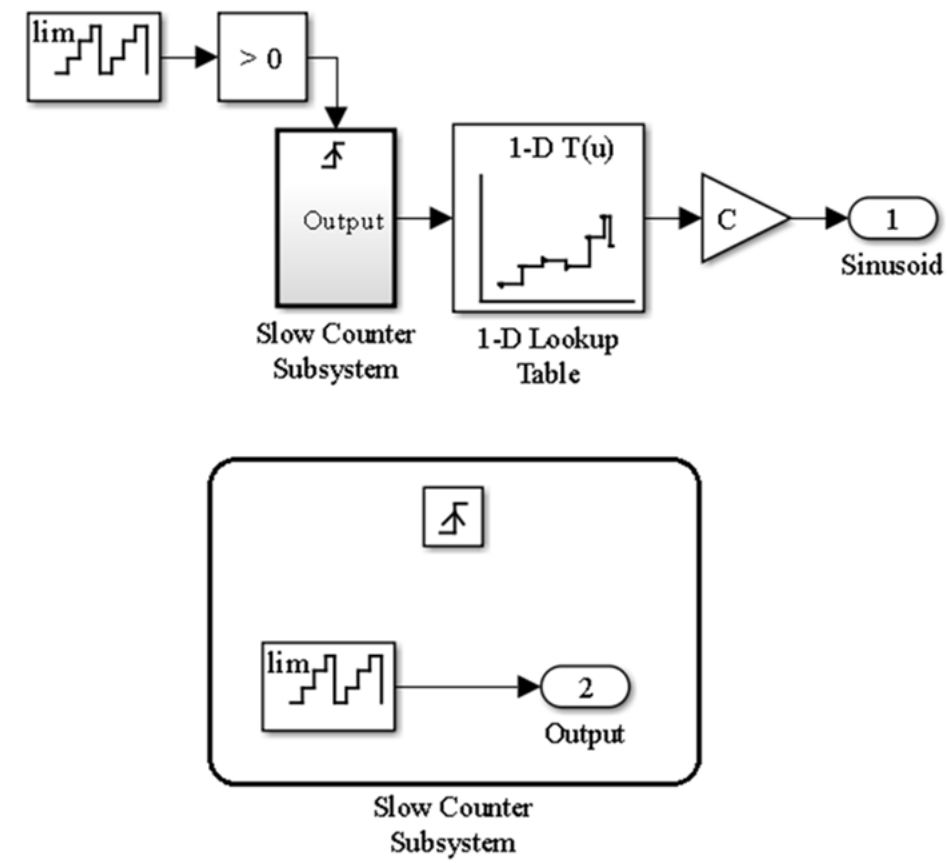


Fig. A.5: Simulink model used to generate a sinusoidal waveform with arbitrary amplitude.

A guide containing further instruction for using an FPGA with Simulink, *A Practical Guide to Using Simulink's HDL Coder with the DE0 Board*, has been prepared for use at Kansas State University.

Appendix B

Developed Hardware

In this appendix, information necessary to use the developed cascaded H-bridge converter are provided. Details are given for the layout of the converter, as well as information required for FPGA interfacing.

B.1 Converter Layout

The legs of the constructed laboratory-scale CHB converter, shown in Fig. B.1, are comprised of two distinct printed circuit board (PCB) designs. Each of the three long upper boards, referred to as brain boards, act as an interface between the CHB cells within a leg and the FPGA used to send gate signals. The remaining 12 boards are the CHB cells, or modules. Cell IGBTs conduct if a "high" signal is sent by the FPGA to the brain board. As shown in Fig. B.1, the right-most leg is Phase A, and cell 4 is the cell closest to the CHB's neutral connection. Phase outputs, as well as the neutral point, can be accessed via the terminal strip at the bottom of the CHB cabinet.

For some tests, it may be necessary to bypass some cells in a CHB leg. While cells can be soft bypassed by setting the unused cells to a zero-state, this approach

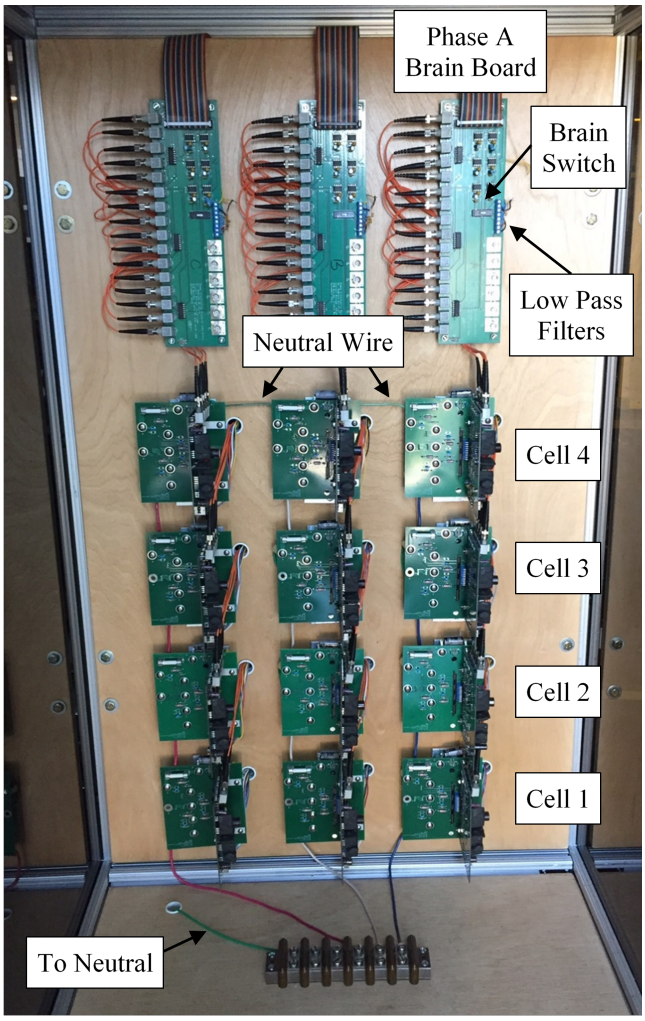


Fig. B.1: Cascaded H-bridge converter.

may cause undesirable diode voltage drops and conduction losses. These voltage drops can be avoided using a hard bypass, i.e. attaching a conductor to completely bypass unused cells. For each leg, the neutral is connected to port U of cell 4, port V of cell 4 is connected to port U of cell 3, and so on. When choosing where to attach a conductor, recognize the neutral is connected to port U of cell 4, port V of cell 4 is connected to port U of cell 3, and so on.

Each CHB cell has a voltage sensor to measure the input dc bus voltage, and cells 2 and 4 in each leg have current sensors oriented such that current flow from the neutral

to the phase output produces a positive measurement. Each voltage and current sensor utilizes an AD620AN instrumentation amplifier (IA), which is placed directly on the cell PCB. Measurements can be made using either dSPACE an analog-to-digital converter (ADCs) on the brain board connected to an FPGA. The gain of the IA need to be adjusted depending on whether the output is going to dSPACE or an ADC. Each cell has a switch to enable IA gains to be changed, with gains made ADC compatible if the switch position is toward the board edge, as shown in Fig. B.2. The single-ended IA output is then connected to the brain board, though low-pass RC filters can be added between the IA output and brain board to attenuate high-frequency noise. Each brain board also has a switch, which enables measurements to either be sent to analog-to-digital converters or to dSPACE. Measurements are sent to the ADCs if the switch position is away from the nearest board edge, as shown in Fig. B.3. Note that the MAX 187 ADCs used in the CHB utilize serial peripheral interfacing (SPI), a common communication technique.

Three terminal strips found on the upper backside of the converter cabinet are used to interface with, and distribute, dc inputs necessary for converter operation. A diagram of these terminal strips is provided in Fig. B.4. In Fig. B.4: Br. X indicates a connection to the phase X brain board; X y,z indicates a connection to cells y and z of phase X; ILL, X is the output of the IA connected to the current sensor in cell 2, phase X; ILU, X is the output of the IA connected to the current sensor in cell 4, phase X; Vmy, X is the output of the output of the IA measuring the input voltage of cell y, phase X; J indicates an input terminal. All control voltage inputs must have a common ground, achieved by connecting power supply terminals appropriately. The function of each terminal strip voltage input is as follows:

GND Black banana plug: control common ground, required return path for all inputs.

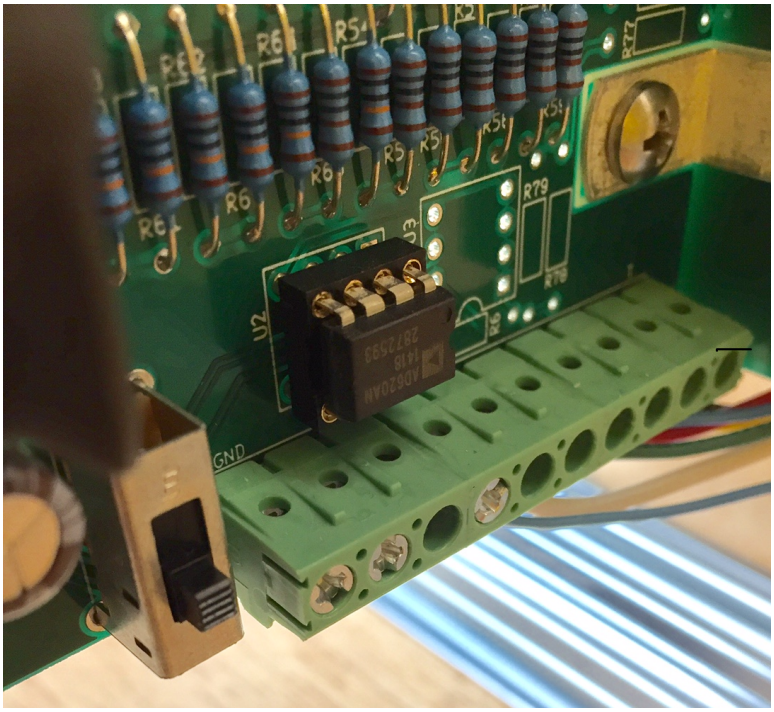


Fig. B.2: Cell switch position to set IA gains for FPGA.

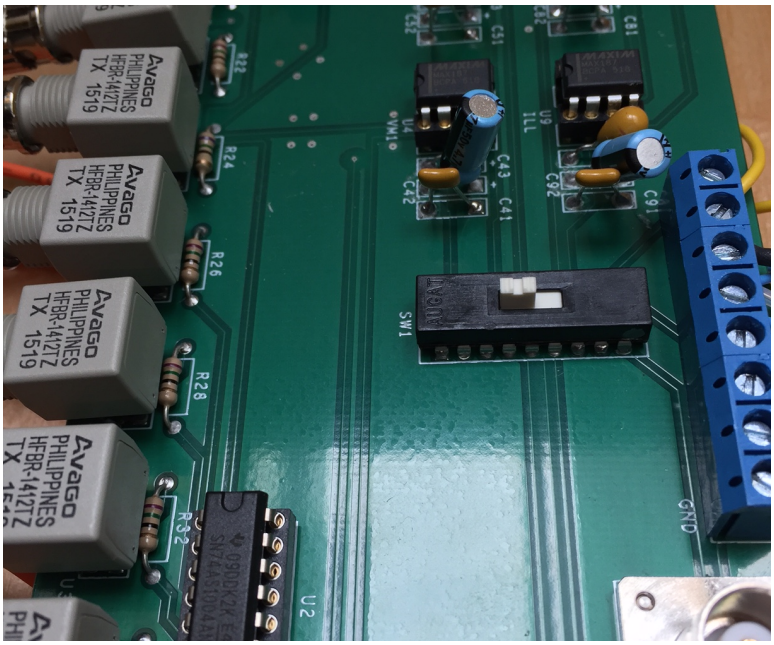


Fig. B.3: Brain board switch position to send measurements to ADCs.

24V Yellow banana plug: required input for dc-dc converters.

10V Blue banana plug: (actual input 11V), required input for instrumentation amplifiers and LAH 25-NP current sensors.

-10V Green banana plug: (actual input -11V), required input for instrumentation amplifiers and LAH 25-NP current sensors.

5V Red banana plug: required input for logic gates and fiber optic transmitters and receivers.

Vref White banana plug: offset used by instrumentation amplifiers measuring cell input voltages.

Cref Orange banana plug: offset used by instrumentation amplifiers measuring leg currents.

Egnd These act as placeholders for an earth ground connection which may be desired at a later time. Each CHB cell also has an available earth ground connection position.

As shown in Fig. B.1, fiber optic cables are used to send gate signals from the brain boards to individual cells. Should a fiber optic cable need to be temporarily removed, or entirely replaced, labels visible from the backside of the converter cabinet can be used to ensure proper removal and reconnection. Fiber optic cables are labeled both ends with tape to designate which cell it runs to, with cell 1 labeled with tie-dye patterned tape, cell 2 with lamb patterned tape, cell 3 with green tape, and cell 4 with blue tape. Each piece of tape is also labeled according to which gate it is connected to, with a "1" label denoting a connection to gate Vp, "2" to Vn, "3" to Up, and "4" to Un.

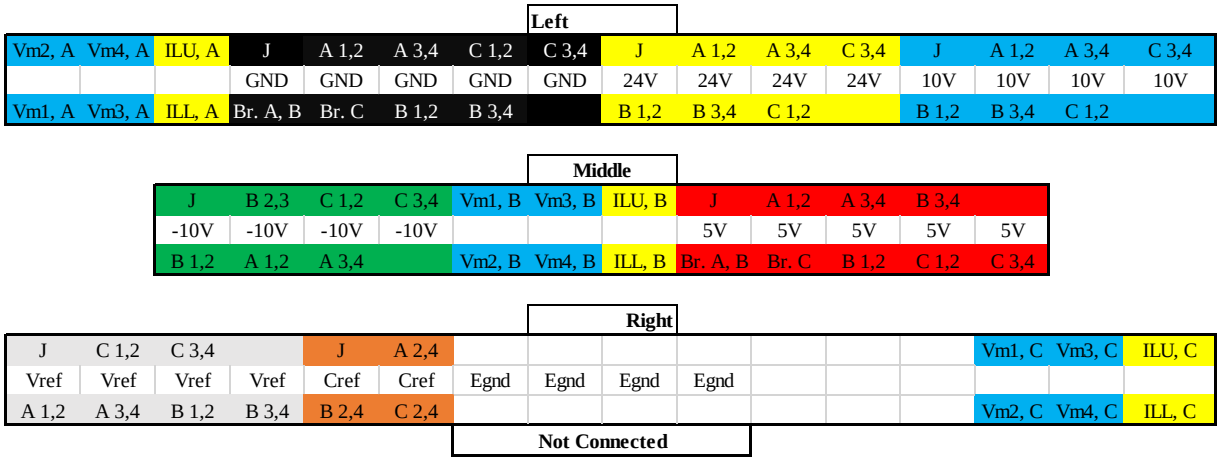


Fig. B.4: Layout of terminal strips on the upper backside of the CHB.

Finally, it should be noted that brain board and cell PCB component identifiers, seen on board silkscreen labels as well as PCB schematics, were selected to facilitate the debugging process. On the brain board, for instance, components numbered with a one in the tens place interact with FPGA gate signals for module 1 gates, denoted I_M1Gx for input–module 1 gate x, where x=1 for gate Vp, 2 for Vn, 3 for Up, and 4 for Un. Similarly, for cells, components numbered with a one in the tens place interact with gate signal Vp, components with a two in the tens place interact with Vn, etc.

B.2 FPGA Interfacing

An FPGA is required to interface with each brain board of the CHB. Table B.1 provides pin assignments utilized when connecting an FPGA to a CHB brain board, using the same notation which is used on the brain board PCB schematic. Note that I_MxGy is the input for module x, gate y, where the gate is made conductive if a high signal is sent from the FPGA into the brain board. Pin assignments for other FPGA features (e.g. Hex display) are available via the user manuals. Note that the pin assignments in Table B.1 are provided assuming pin 1 of the FPGA is tied to pin 1 of the brain

board, where a black arrow indicates the position of pin 1 on all 40-pin headers used. Ribbon cables should be made such that the FPGA and brain board pins are properly interfaced.

Three FPGAs are required to interface with the three CHB brain boards. However, when multiple CHB legs are simultaneously used, slight mismatches between FPGA internal clock frequencies deviations can cause the FPGAs to operate asynchronously. Over time, this may result in carrier phase deviations if FPGAs are being used to implement a carrier-based PWM method. Therefore, instead of using FPGA internal clocks when testing polyphase systems, an external clock can be used to ensure FPGAs remain in phase. Moreover, external switches can be used to simultaneously provide "clock enable" and "reset" signals to multiple FPGAs.

Table B.1: FPGA GPIO Pin Assignments

	DE0		DE1	
Brain Board Label	GPIO0	GPIO1	GPIO0	GPIO1
I_M1G1 (Input, Module 1, Gate 1)	AB16	AA20	Y17	AA21
I_M1G2	AA16	AB20	Y18	AC23
I_M1G3	AA15	AA19	AK16	AD24
I_M1G4	AB15	AB19	AK18	AE23
I_M2G1	AA14	AB18	AK19	AE24
I_M2G2	AB14	AA18	AJ19	AF25
I_M2G3	AB13	AA17	AJ17	AF26
I_M2G4	AA13	AB17	AJ16	AG25
I_M3G1	AB10	Y17	AH18	AG26
I_M3G2	AA10	W17	AH17	AH24
I_M3G3	AB8	U15	AG16	AH27
I_M3G4	AA8	T15	AE16	AJ27
I_M4G1	AB5	W15	AF16	AK29
I_M4G2	AA5	V15	AG17	AK28
I_M4G3	AB4	AB9	AA19	AJ26
I_M4G4	AA4	AA9	AC10	AH25
cs1 (Chip Select 1)	U14	AB7	AJ20	AJ24
sclk1 (Slow Clock 1)	V14	AA7	AH19	AJ25
data1 (VM1) (Module 1 Voltage)	AB12	AB11	AC18	AB17
cs2	W13	R14	AK21	AG23
sclk2	Y13	T14	AH20	AK24
data2 (VM2)	AA12	AA11	AD17	AB21
cs3	V12	T12	AD20	AH23
sclk3	U13	U12	AD19	AK23
data3 (VM3)	R10	R11	AE18	AK22
cs4	Y10	U10	AF20	AH22
sclk4	V11	R12	AE19	AJ22
data4 (VM4)	W10	T10	AF21	AG22
cs5	V8	T9	AG21	AF23
sclk5	T8	U9	AF19	AF24
data5 (ILU) (Module 4 Current)	W7	Y7	AF18	AE22
cs6	V5	V6	AG18	AA20
sclk6	W6	U8	AG20	AD21
data6 (ILL)	U7	V7	AJ21	AC22