Design of ultra-narrowband Q-enhanced LNAs

by

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Abstract

Modern-day radio receivers operate in environments that are becoming increasingly dense with RF signals. As the density of the radio spectrum increases, receivers must be able to maintain successful operation despite these potential interfering signals. Two issues facing modern-day radio receivers are signal blocking issues, and the generation of intermodulation products in the LNA. These issues stem from entire bands reaching the LNA, as the power level of the signals within the service band may differ widely. This can cause the LNA to compress before a desired low-power signal receives the full gain of the LNA or allow two moderate-power signals to mix and generate an intermodulation product that is located at the same frequency of a desired low-power signal.

This thesis focuses on the design, simulation, and testing of a new radio receiver architecture, using an ultra-narrowband Q-enhanced LNA, which aims to address these issues. The design is based on the fundamentals of regenerative receivers, using controlled positive feedback for control of the gain and bandwidth of the filter response. Furthermore, gain, bandwidth, and filter center frequency can be automatically tuned with the addition of an auto-tuning algorithm running on a microcontroller.

Two different designs were realized, one at the board level for FM radio, the other at the chip-level for use with 802.11ax, known as Wi-Fi 6, at 2.4 GHz. This thesis details the design of the core building blocks used in an ultra-narrowband Q-enhanced LNA, including the core amplifiers, buffers, matching networks, feedback networks, and auto-tuning algorithm. The results of both physical testing and simulation are also presented, and are used to verify that the design addresses both signal blocking and intermodulation product issues.

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Dedication

For my parents Roman and MaryBeth as this work, and more, would not have been possible without their love, support, and encouragement.

Chapter 1 - Introduction

This work is focused on the design, testing, and simulation of ultra-narrowband Q-enhanced low noise amplifiers (LNAs). Over the course of this thesis, a complete auto-tunable ultra-narrowband Q-enhanced FM receiver was designed and tested at the board level, while a tunable Q-enhanced LNA was developed in a 45nm RFSOI process at 2.4 GHz. The Q-enhanced LNAs and systems presented were designed with the goal of reducing the impact of high-power interfering signals on the reception of low power signals in a wide variety of applications.

1.1 – Motivation

Modern day radio receivers are expected to work without issue in an increasingly dense spectrum. As the spectrum density increases, radio frequency (RF) receivers must filter out unwanted out of band (OOB) signals with greater rejection, and low noise amplifiers (LNAs) must be capable of amplifying bands of signals ranging widely in power level without compressing. It's not only OOB signals that provide a challenge to these receivers, as it is often in band signals presenting challenges for an LNA. Many different modern receiver architectures include a preselect filter, which is responsible for filtering out signals other than those in the desired service band. In the case of FM radio, this means passing all signals from 88 MHz to 108 MHz. Figure 1.1 shows the crowded FM spectrum in Manhattan, Kansas, while Figure 1.2 shows a generic RF frontend that uses a preselect filter.

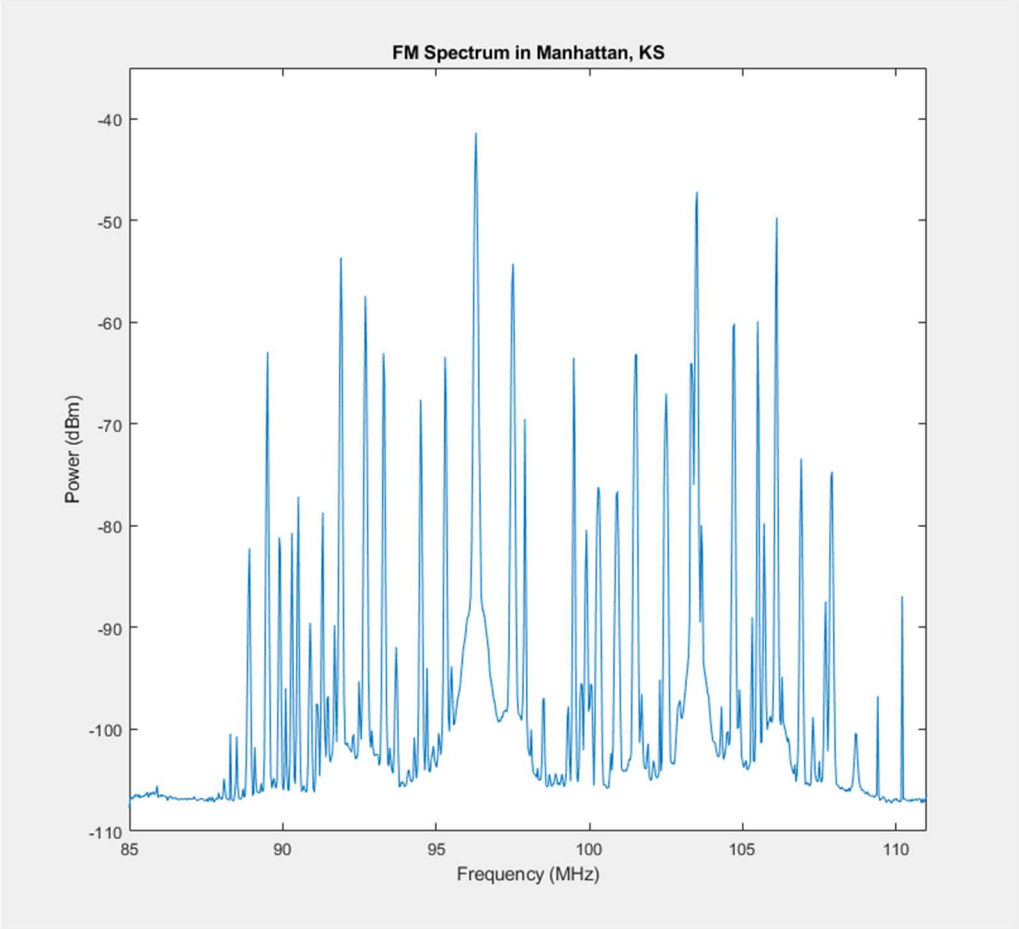

Figure 1.1. FM Spectrum in Manhattan, Kansas, 3 kHz RBW and 0 dB attenuation.

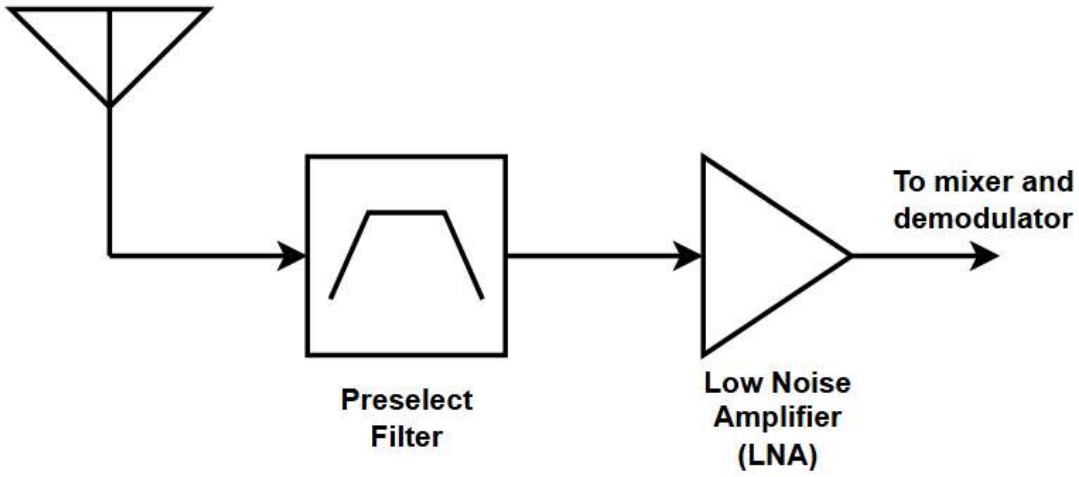

Figure 1.2. Generic RF frontend with preselect filter.

The large variation in power level of the signals in the desired frequency range, as shown in Figure 1.1, causes signal blocking and intermodulation product issues. The signal blocking issue stems from a large in band signal, around -20 dBm to -10 dBm, compressing the LNA before a desired small signal, around -60 dBm to -70 dBm or less, can be fully amplified. As the desired small signal does not receive the full gain of the LNA, it has effectively been blocked by the larger in band signal and may not be received correctly. Figure 1.3 provides a visual representation of the blocking issue.

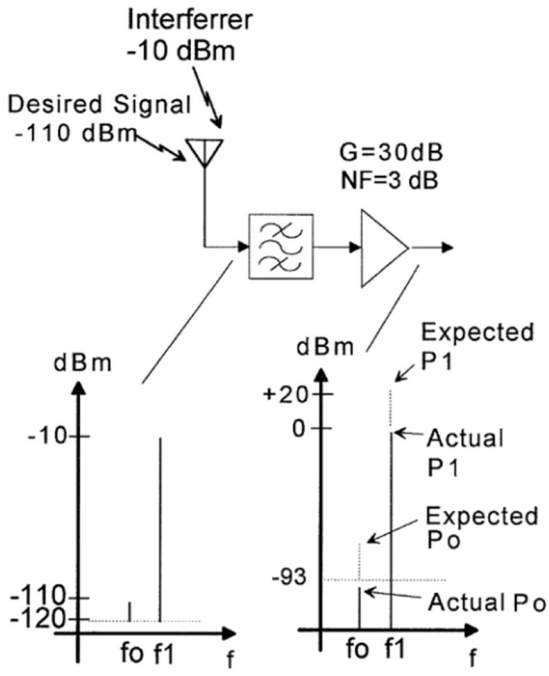

Figure 1.3. Visualization of the blocking problem issue [19].

Intermodulation products stem from the underlying mathematics of non-linearities in circuits [19]. They occur when a signal at frequency f_1 mixes with another signal at frequency f_2 in the third-order Taylor series expansion of the gain function and creates intermodulation products at $2f_2 - f_1$ and $2f_1 - f_2$. These new signals have the potential to fall on the desired signal at frequency f_0, meaning that $2f_2 - f_1 = f_o$ or $2f_1 - f_2 = f_o$. Additionally, these signals

need not be high power, instead they can be much smaller, around -40 dBm. The generated intermodulation product effectively "buries" the desired signal. In the case of FM radio, this means the user would hear a combination of the radio stations at frequency f_1 and f_2 and would not hear the desired signal at f_o [19]. Figure 1.4 provides a visual representation of the generation of third-order intermodulation products. Figure 1.5 provides an example of where an intermodulation product may be generated, based on the spectrum shown in Figure 1.1.

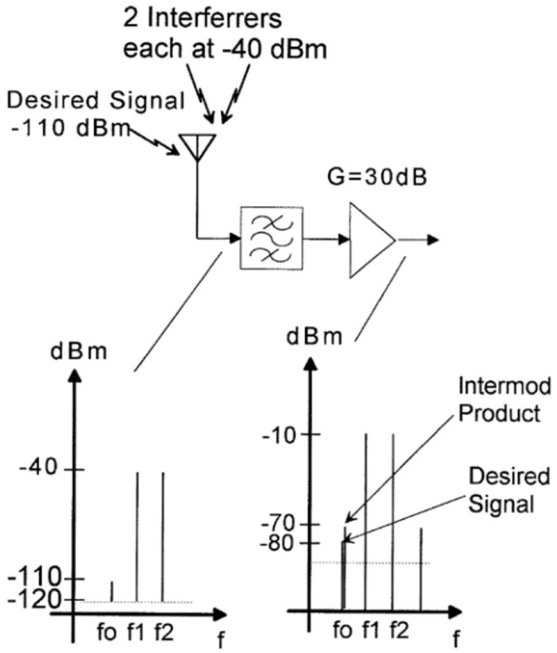

Figure 1.4. Visualization of the generation of intermodulation products [19].

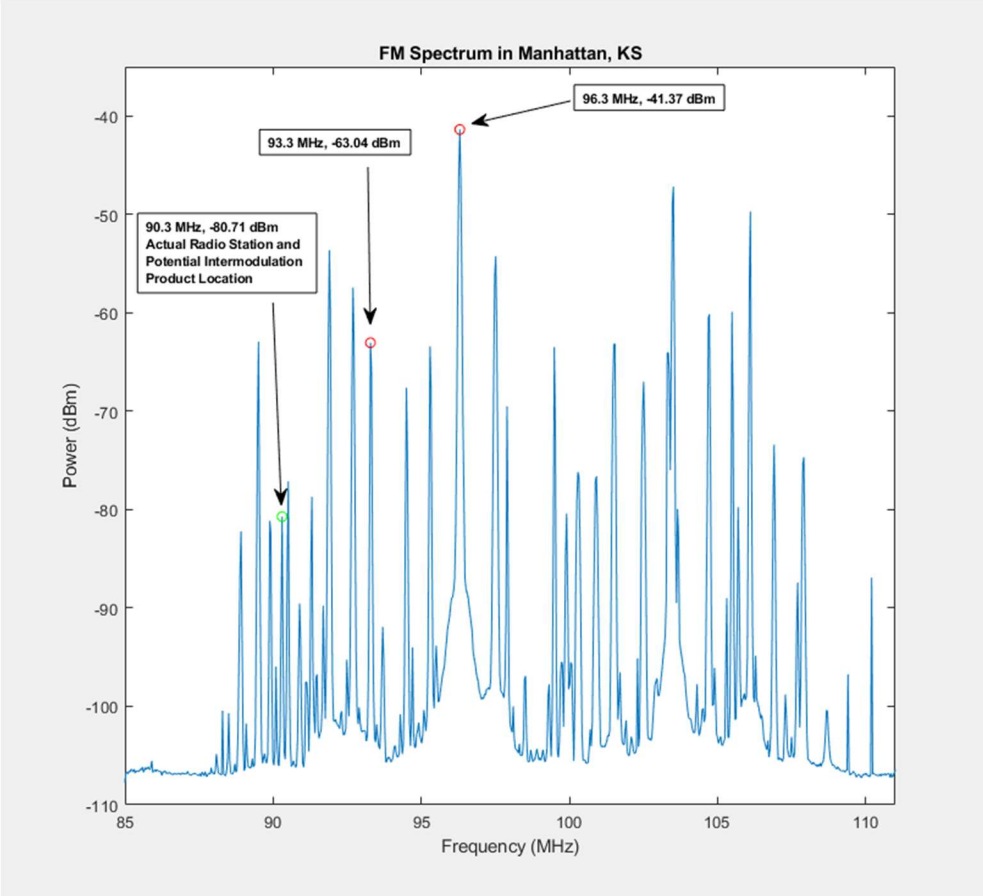

Figure 1.5. Potential intermodulation product location in a real spectrum.

As many service bands are becoming increasingly dense, these issues may become more prevalent as many modern-day receiver architectures use a preselect filter, allowing the entire service band to reach the LNA. This thesis aims to address these issues by using known receiver architectures and improving them, as proposed in [18][19].

1.2 – Prior Work

One of the earliest methods of receiving radio signals was by using regenerative receivers. These receivers excelled in terms of selectivity, only amplifying the desired signal while attenuating large interfering signals. Although these receivers had desirable qualities for a modern-day receiver in a dense spectrum, they did not gain widespread popularity as they proved

to be difficult to tune at the time [22]. The superheterodyne architecture, developed several years after the regenerative receiver architecture, gained widespread popularity as it was much easier to tune and operate [22]. Since then, many different variations of the superheterodyne receiver have been developed.

There have also been some changes in the design of LNAs at the circuit level, such as increasing the power draw of an LNA. By burning more power in the LNA, the 1 dB output compression point can be improved, effectively increasing the input compression point and mitigating the blocking issue. However, burning more power in the LNA may not be practical as many modern-day systems are portable, and try to minimize power consumption to maximize battery lifetime between charging cycles.

Several receiver architectures, as well as the use of high power LNAs, are discussed in depth in this thesis. By knowing the history and the design of these architectures, they can be improved upon to design an ideal receiver architecture as proposed by [19]. Additionally, [1] and [9] further discuss the benefits of Q-enhancement in radio receivers to mitigate the previously discussed issues.

1.3 – Thesis Organization

This thesis spans a total of five chapters. The first chapter covers a brief overview of the issues receivers face as the radio spectrum becomes increasingly dense. A quick look at radio architectures used in both the past and present is also included, as well as how they can be used to mitigate the issues discussed. The second chapter delves into the history of several receiver architectures and how they are impacted by the issues presented in Chapter 1. This chapter also provides a quick look at the use of feedback in circuits, and how it impacts circuit performance. This chapter concludes by presenting a new ideal receiver architecture capable of mitigating the

issues discussed in Chapter 1. The third chapter dives into the design and testing of the ideal receiver architecture described in Chapter 2. The fourth chapter discusses the design and simulation of the ideal receiver architecture on-chip in a 45nm RFSOI process, with heavy emphasis on the design of the feedback network. Finally, the fifth chapter reiterates the practical use of the designed receiver, as well as discussing several areas of interest for future research and development of the proposed receiver architecture.

Chapter 2 - Traditional Solutions and Feedback Systems

2.1 – Traditional Solutions

Having discussed the motivation for this work, this section provides a brief history and overview of different architectures and techniques used in radio receivers throughout the last century. In addition, the fundamental mathematics of feedback are discussed, and a system architecture that innovates on regenerative receivers is presented.

2.1.1 – Regenerative Receivers

Regenerative receivers predate superheterodyne receivers by several years, with both Edwin Armstrong and Lee de Forest discovering the benefits of regeneration at roughly the same time. Although de Forest officially holds the US patent for regenerative receivers, engineers often credit Armstrong with the invention as his patent was issued two years prior to de Forest having his patent issued [8][22]. Figure 2.1 depicts the regenerative receiver architecture.

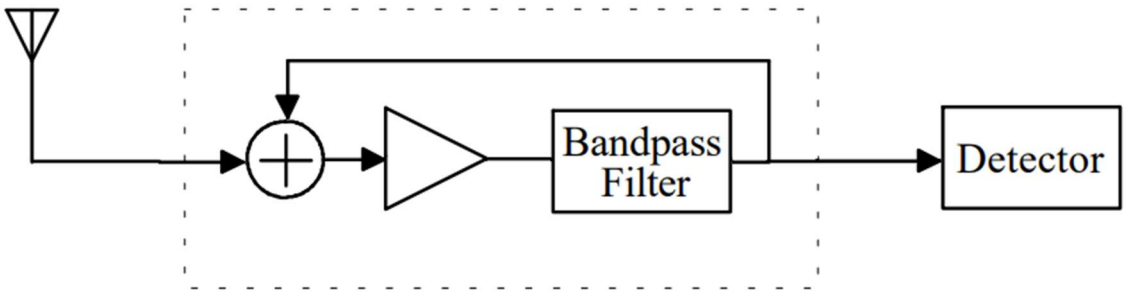

Figure 2.1. Regenerative receiver architecture [7].

What makes the regenerative receiver so special is its use of positive feedback. By feeding back a portion of the amplifier's output signal back into the amplifier's input, gain and selectivity can be significantly increased. By using a highly selective receiver, large interfering signals that may have originally been allowed through by a preselect filter will now be off-

channel. These large signals will now be attenuated significantly, minimizing the risk of the LNA compressing or generating intermodulation products. Effectively, this architecture addresses the issues presented in Section 1.1 by narrowing the filter response and only amplifying the desired signal.

Unfortunately, while the regenerative receiver addresses these issues, this architecture was difficult to tune and control in a practical environment, as discussed in [22]. Fortunately, as technology has developed over the last century there are new potential solutions to the tuning problem faced by regenerative receivers of the past. To understand how feedback can be controlled, and how it impacts circuit performance, Section 2.2 provides a deep dive into the fundamental mathematics of feedback. Additionally, Section 2.2.2 presents a new receiver architecture that improves on the regenerative receivers of the past.

2.1.2 – Superheterodyne Receivers

The superheterodyne receiver is one of the most used architectures in modern day receivers, and was originally developed in 1918 by American engineer, Edwin Armstrong [22]. The superheterodyne architecture addressed some challenges presented by regenerative receivers, namely the ability to easily tune. While there are many different implementations of superheterodyne receivers, Figure 2.2 illustrates the typical single conversion superheterodyne receiver architecture.

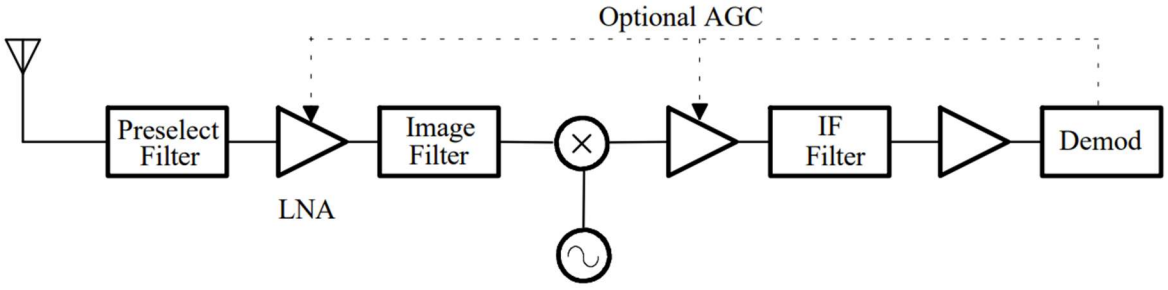

Figure 2.2. Superheterodyne receiver architecture [7].

The superheterodyne receiver architecture contains several notable blocks. First is the preselect filter, which allows the entire desired service band through to the LNA, while rejecting OOB signals. In the case of FM radio, the entire FM spectrum from 88 MHz to 108 MHz is passed. The entire service band then reaches the LNA, providing some amplification and setting the noise figure of the receiver. The amplified RF signal then mixes with a local oscillator (LO) to generate the intermediate frequency (IF) signal. This signal is filtered and amplified again before being demodulated. By downmixing to a predetermined IF, only the LO frequency will need to be tuned, making the superheterodyne receiver easier to tune than the regenerative receivers. Additionally, higher gain amplifiers and narrow filters are more easily achievable at lower frequencies, such as those that would be used in the IF section.

The problems discussed in Section 1.1 really stem from the entire service band being allowed through by the preselect filter and reaching the input of the LNA. To be more specific, it is the potential for large in-band signals reaching the LNA that causes issues. In this regard, the LNA needs to be "protected", and an ideal architecture is presented in Section 2.2.2 that achieves this. The use of a preselect filter is quite widespread, and as such the remainder of the receiver architectures and techniques discussed in this section all use preselect filters making them susceptible to the issues this thesis works to mitigate.

2.1.3 – Direct Conversion Receivers

Direct conversion receivers, or zero-IF receivers, are conceptually simple as they lack the IF stage seen in the superheterodyne architecture. Instead, these receivers directly convert the RF signal down to baseband where further filtering, amplification, and processing can be done. Figure 2.3 depicts the direct conversion receiver architecture for quadrature modulation schemes as outlined by [7].

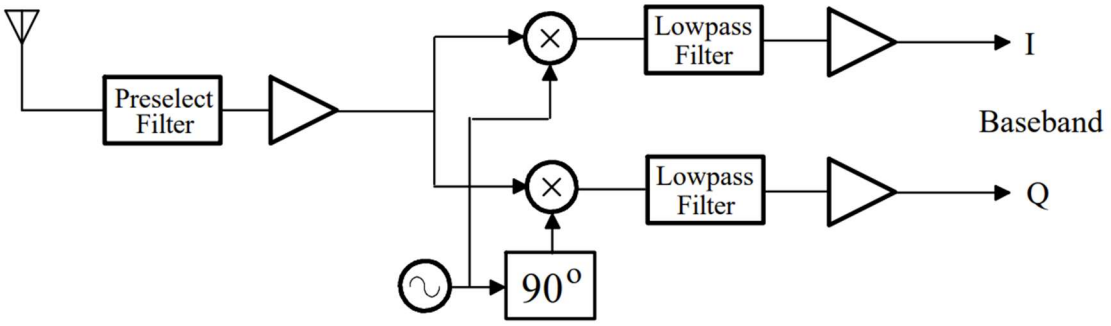

Figure 2.3. Direct conversion receiver architecture [7].

Understanding the benefits and drawbacks of the direct conversion receiver architecture is outside the scope of this thesis, although a brief overview is presented in [7]. What is important to note, however, is that this architecture also includes a relatively wideband preselect filter before the LNA, just as in the superheterodyne architecture, and does not address the issues discussed in Section 1.1.

2.1.4 – Software Defined Radios

Software defined radios (SDRs) are relatively new compared to the architectures that have been mentioned. These radios are designed to replace the hardware responsible for mixing, modulating and demodulating, and provide extended signal processing. This allows the radio to be extremely flexible, as it can be reused for multiple different frequency ranges or modulation techniques, requiring just a software change [7]. Figure 2.4 illustrates the software defined radio architecture.

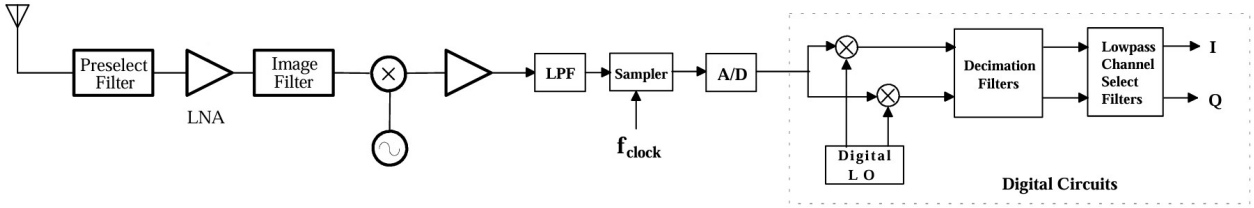

Figure 2.4. Software defined radio architecture [7].

As shown in Figure 2.4, the only analog components in the SDR architecture are a part of a superheterodyne receiver, which is responsible for converting the desired frequency range down to an intermediate frequency that is within the range of the analog-digital-converter (ADC). The remainder of the functions, such as digital signal processing like filtering, further down mixing, and demodulating, are implemented in software [7]. However, just like the superheterodyne receiver and direct conversion receiver architectures, the use of an LNA amplifying the whole desired service band, or more, and the subsequent active/non-linear mixing operation is what causes the issues discussed in Section 1.1.

2.1.5 – High-Power Low Noise Amplifiers

Another technique for mitigating the issues presented in Section 1.1 is the use of high-power LNAs. By simply burning more power in the LNA, such as increasing the bias current, the 1 dB output compression point, and effectively the 1 dB input compression point, as well as the associated third-order intermodulation intercept [19] can be improved. In turn this means that larger signals should not compress the LNA as easily, and low power desired signals should be fully amplified. Unfortunately, additional power consumption may not be feasible for applications requiring minimal power consumption.

2.2 – Feedback Systems

As noted in [22], the ability to adjust the positive feedback quickly and effectively proved to be the largest threat to the widespread use of regenerative receivers. Feedback in itself is a somewhat complicated topic, especially positive feedback. Even in modern-day circuit theory and electronics courses, the use of feedback largely focuses on negative feedback rather than positive feedback. The ability to understand the effects of both types of feedback is essential to

understanding the operation of the proposed Q-enhanced LNA circuit, that is robust against large signal interferers and intermodulation products.

The full mathematical understanding of feedback and its effect on many amplifier and circuit parameters is discussed in depth by [14], while a shortened version is presented in Section 2.2.1. Sections 2.2.2 and 2.2.3 elaborate on the use of positive feedback and the benefits gained by utilizing it, while Section 2.2.4 addresses the sensitive nature of positive feedback systems and outlines the need for designers to be careful when employing positive feedback in an RF receiver.

2.2.1 – Feedback Analysis

The use of feedback is widespread in modern day systems and circuits using operational amplifiers (op-amps), comparators, switch-mode power supplies, and more. In-fact many engineers likely learned about feedback in a university course as a part of the derivation of the op-amp gain equations, although it is unlikely that the use and benefits of feedback were covered in depth. Since understanding feedback is paramount to this work, this section provides a brief overview of the fundamentals of feedback and how they change several circuit and amplifier parameters. The full mathematics and understanding of the effects of feedback are covered in [14]. Figure 2.5 depicts the general feedback amplifier system structure that is commonly used in university courses to understand the mathematics of feedback.

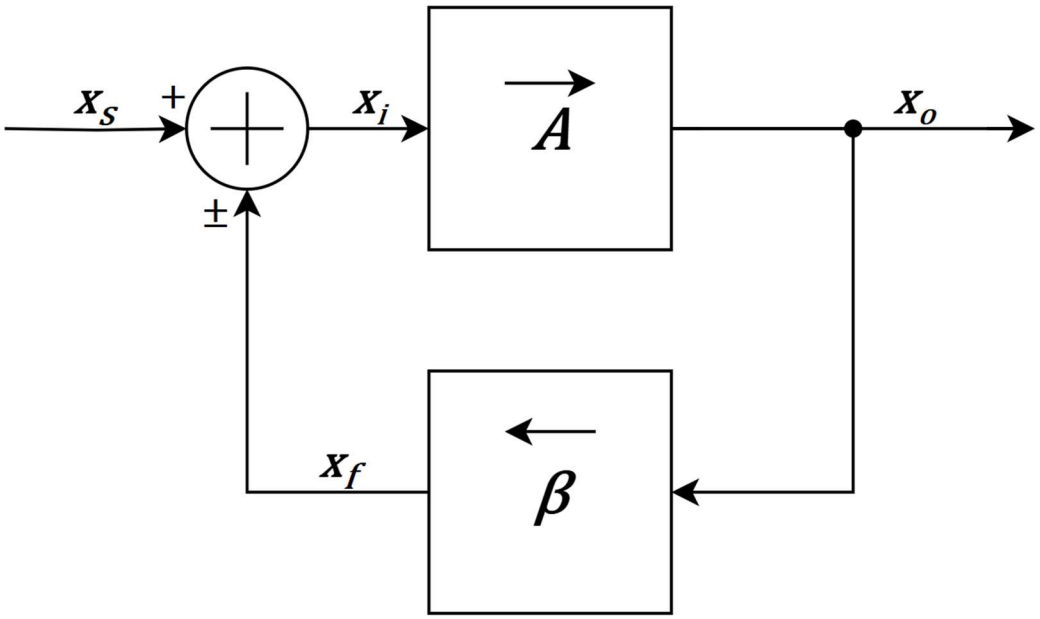

Figure 2.5. General feedback amplifier structure.

The general structure of feedback amplifiers illustrated in Figure 2.5 is simple and contains several blocks used to define its operation. The block labelled A is the main unilateral amplifier with gain A, while the block denoted by β is a unilateral feedback network with feedback network gain β [14]. Of note, it is assumed that the feedback network does not load the output of the amplifier significantly, and the quantities denoted by x can represent either voltage or current as discussed in [14]. From the block diagram, Equation (2.1) can be written.

$$x_o = Ax_i \tag{2.1}$$

The variable A is known as open-loop gain and indicates the amount of gain when the feedback network is not applied, and as such, Equation (2.1) shows the standard relationship between input and output when using an amplifier with gain A. When the feedback network is applied, the feedback signal x_f can be written in terms of the output signal and the feedback network gain β.

$$x_f = \beta x_o \tag{2.2}$$

While Equations (2.1) and (2.2) do not differ between negative or positive feedback, the operation of the summing block, and hence the input signal x_i, changes depending on which type of feedback is being used. In systems employing negative feedback, the amplifier input signal is the difference between the source and feedback signals. In positive feedback systems, the amplifier input signal is the summation of the source and feedback signals. Equations (2.3) and (2.4) [14] show the input signal in terms of the source signal, x_s, and the feedback signal, x_f, for negative and positive feedback systems respectively.

$$x_i = x_s - x_f \tag{2.3}$$

$$x_i = x_s + x_f \tag{2.4}$$

With the equations defined for each signal of the general structure shown in Figure 2.5, the effect of feedback networks can be analyzed. Having already defined the open-loop gain of the circuit, where there is no feedback present, the closed-loop gain can be defined by Equation (2.5) [14].

$$A_f \triangleq \frac{x_o}{x_s} \tag{2.5}$$

Combining Equations (2.1) through (2.5) results in Equations (2.6) and (2.7), which show the closed loop gain for negative and positive feedback systems respectively.

$$A_f = \frac{A}{(1 + A\beta)} \tag{2.6}$$

$$A_f = \frac{A}{(1 - A\beta)} \tag{2.7}$$

The quantity $A\beta$ is known as loop gain, while the quantity $(1 + A\beta)$ is known as the feedback factor. The only difference between Equations (2.6) and (2.7) is the sign of the loop gain, $A\beta$, changing. Due to the sign of the loop gain changing, positive feedback will have the opposite effect of negative feedback on gain. The simple change in loop gain polarity is an

important distinction to note, as the remainder of equations in this section will be presented in the negative feedback form. These equations can then be used to find formulas for the positive feedback case simply by modifying the sign of the loop gain in the expressions.

2.2.2 – Effect of Feedback on Bandwidth and Impedance

While the change in gain is just one effect of using feedback, there are several other effects that are discussed in depth in [14]. As shown in [14], the consequences of using negative feedback are desensitized gain, reduced nonlinear distortion, reduced effect of noise, increase or decrease of input and output impedances, and bandwidth extension. Conversely, positive feedback will have the opposite effect of the previously described effects of negative feedback.

While the effect of feedback on amplifier gain is simple, the change in input and output impedance is more complex. It requires understanding of different 2-port network models for the gain and feedback blocks and how they align with different amplifier types. For feedback networks, the output of the amplifier must be “sensed”, while the output of the feedback network is “mixed” back into the input of the amplifier. There are two types of feedback sensing and mixing that can be used: shunt and series. Shunt sensing or mixing implies that the feedback network is connected in parallel to the output or input respectively, while series sensing or mixing implies that the feedback network is connected in series to the output or input of the amplifier.

The different combinations of shunt and series sensing and mixing create four different topologies of feedback networks, shunt-shunt, shunt-series, series-shunt, and series-series. Each feedback topology subsequently has an appropriate amplifier type: shunt-shunt feedback for transresistance amplifiers; shunt-series feedback for current amplifiers; series-shunt feedback for voltage amplifiers; and series-series feedback for transconductance amplifiers.

The intricacies of each amplifier and feedback topology are outside the scope of this thesis, although understanding the impacts on input and output impedance and bandwidth is crucial to designing an amplifier that is robust against large signal interferers and intermodulation products, which is the core work of this thesis. Following [14], Table 2.1 outlines the effect each feedback topology has on input and output impedance for the case of negative feedback.

Amplifier Type	Feedback Topology	A_f Units	Input Impedance	Output Impedance
Transresistance	Shunt-Shunt	$\frac{V_o}{I_s}$	$R_{if} = \frac{R_i}{(1+A\beta)}$	$R_{of} = \frac{R_o}{(1+A\beta)}$
Current	Shunt-Series	$\frac{I_o}{I_s}$	$R_{if} = \frac{R_i}{(1+A\beta)}$	$R_{of} = R_o(1+A\beta)$
Voltage	Series-Shunt	$\frac{V_o}{V_s}$	$R_{if} = R_i(1+A\beta)$	$R_{of} = \frac{R_o}{(1+A\beta)}$
Transconductance	Series-Series	$\frac{I_o}{V_s}$	$R_{if} = R_i(1+A\beta)$	$R_{of} = R_o(1+A\beta)$

Table 2.1. Input and output impedances for negative feedback topologies.

Using the equations from Table 2.1, designers can select feedback and amplifier types that will provide the desired change in input and output impedance. As previously stated, the equations for positive feedback can be found simply by changing the sign of the loop gain.

While changes in impedance depend on the feedback topology and amplifier type, the change in bandwidth does not. To analyze the change in bandwidth, it is appropriate in this application to use the equation for a second-order bandpass filter that is normally made by an LC tank circuit in the amplifier. Equation (2.8) provides the S domain transfer function of such a filter.

$$H(s) = \frac{s\frac{2\pi f_o}{Q}}{s^2 + s\frac{2\pi f_o}{Q} + (2\pi f_o)^2} \tag{2.8}$$

A crucial component of the bandpass transfer function is the quality factor, shown as the variable Q. Quality factor can be a measure of how "good" an inductor is, where a larger Q indicates a lower series resistance, and a smaller Q indicates a higher series resistance. Quality factor is also a measure of how selective the filter response is, where a higher Q indicates a narrower bandwidth compared to a lower Q, where the bandwidth is larger. For this work, Q is calculated from the 3 dB bandwidth and the center frequency of a bandpass filter, shown in Equation (2.9).

$$BW = \frac{f_o}{Q} \tag{2.9}$$

As previously mentioned, the use of feedback will change the bandwidth in an amplifier. Equations (2.10) and (2.11) show the change in Q and bandwidth when using negative feedback.

$$Q_{fb} = \frac{Q}{1 + A\beta} \tag{2.10}$$

$$BW_{fb} = BW(1 + A\beta) \tag{2.11}$$

As previously discussed, the use of negative feedback decreases the selectivity of the filter, as it increases the bandwidth of the amplifier's filter response. This is the opposite of what is desired in a modern-day receiver, as a more selective amplifier will mitigate the potential for blocking or intermodulation product issues to occur. Understanding the impact on circuit and amplifier performance caused by feedback allows designers to develop creative solutions to problems facing modern day RF receivers.

2.2.3 – Benefits of Positive Feedback for Q-Enhanced Frontends

As discussed in Section 1.1, receiver preselect filters let through entire service bands, which can cause several issues that modern day radio receivers face: blocking and intermodulation products. As a brief reminder, the blocking problem is caused by large signal

interferers compressing the LNA gain before the low-power desired signal can be fully amplified [19]. In the context of signal compression and blocking problems, large signal interferers may mean signals with a power around -20 to -10 dBm or more, depending on the amplifier's gain and power consumption. The intermodulation product issue is caused by two signals mixing in the third-order Taylor series expansion of the gain function of an LNA, creating intermodulation products at $2f_2 - f_1$ and $2f_1 - f_2$.

As outlined in [7] and [22], the regenerative receiver is designed around the use of positive feedback to increase both gain and selectivity of an amplifier's filter response. By using positive feedback to enhance the Q of the filter significantly, it is possible to obtain a filter with channel bandwidth. For example, it is possible to obtain a 200 kHz bandwidth for FM radio at 100 MHz, implying a Q of 500. This greatly exceeds the Q of available inductors or capacitors, hence implying the circuit has been Q-enhanced. By tuning the amplifier's channel-bandwidth filter response to the desired frequency, off-channel interferers should be significantly attenuated and not cause the amplifier to compress easily or generate intermodulation products. While the use of positive feedback alone should provide attenuation to off-channel signals at the amplifier's output, additional attenuation of the input signal can be gained by adding a series resistor before the input of the main amplifier to create a voltage divider. The additional attenuation provides additional overhead to ensure high power signals do not compress the LNA. An L matching network can also be used to scale up the input impedance from the viewpoint of the amplifier input, creating a voltage divider. Figure 2.6 shows the impedances seen at different viewpoints due to the addition of an L matching network to scale up the source impedance.

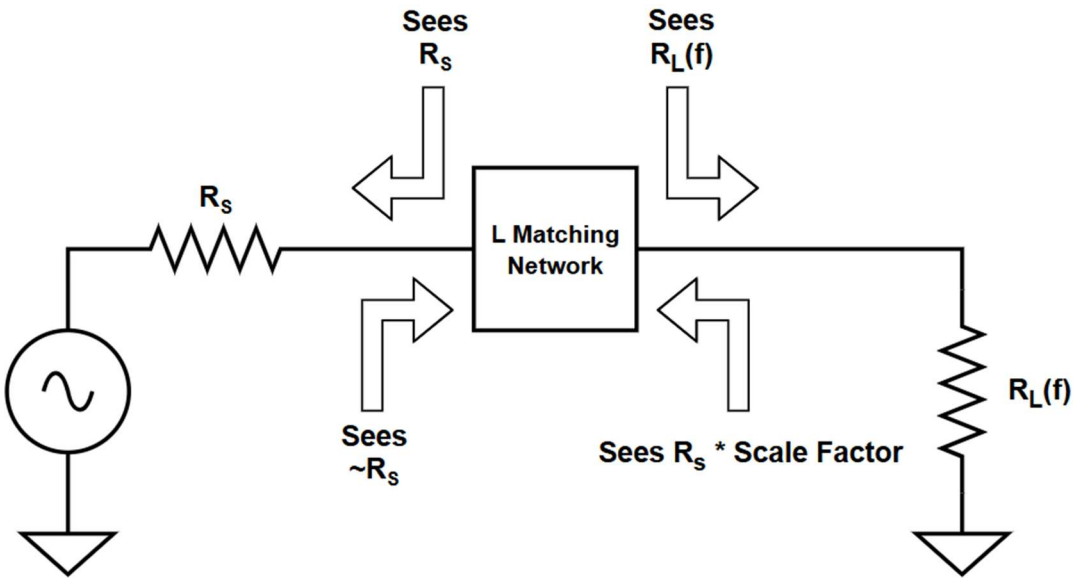

Figure 2.6. Impedances seen due to an L-matching network

Note that with the use of positive feedback the amplifier input impedance, R_L, will become a function of frequency, denoted $R_L(f)$, causing the impedance seen by the signal source to also become a function of frequency. While either method of creating a voltage divider with the input impedance of the main amplifier will work, the L-matching network has the added benefit of being considered lossless, potentially providing a lower noise figure.

By using an L-matching network, a 10 dB or better attenuator can be made with the input impedance of the main amplifier by matching from the signal source impedance to ten times the amplifier input impedance. By using positive feedback and a tunable LC tank in the amplifier, the input impedance becomes a function of frequency, making attenuation frequency dependent. At the center frequency of the amplifier's filter response, the amount of positive feedback will be much larger than the amount of positive feedback at off-channel frequencies. Because of the large amount of positive feedback at the center frequency, the amplifier input impedance can be increased to match the L-matching network or exceed it, resulting in a 0 dB or less attenuation to the desired signal at the input of the main amplifier. Frequencies and signals that are off-channel

will have much less positive feedback, maintaining the nominal 10 dB or better attenuation. This will provide protection from large off-channel interferers that would otherwise result in blocking or generation of intermodulation products.

As there is desire to increase the input impedance using positive feedback, the use of a transresistance or current amplifier is required as input impedance will increase as the loop gain approaches unity, as seen in Table 2.1. While both shunt-shunt or shunt-series feedback will work, the shunt-shunt feedback topology has the added benefit of being much easier to intuitively understand as it sits directly in parallel with the main amplifier.

In conclusion, the core building blocks of the ideal system are starting to take shape, having discussed the tuned primary amplifier, the shunt-shunt positive feedback network, and the L-matching network at the amplifier input. One final note is that it may be desirable to add buffers to the output of the primary amplifier. This is done to present a stable high impedance load to the primary amplifier, and to be able to drive low impedance loads. Furthermore, it may be desirable to use two separate buffers, one for the final system output and one that leads to the feedback network. Figure 2.7 depicts the nominal system architecture, known as a Q-Enhanced LNA, that has been described in both this text and in [18][19].

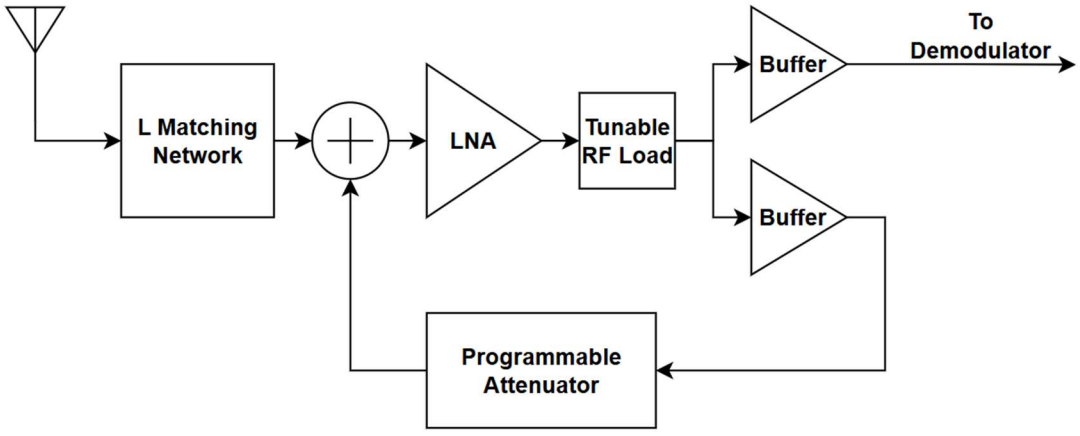

Figure 2.7. Nominal Q-enhanced LNA system architecture.

The Q-Enhanced LNA architecture addresses the issues discussed in Section 1.1 and was implemented in early forms as discussed in [18]. This design was adapted for the filter used in this research and uses an additional control board to provide automated on the fly tuning of both the center frequency and selectivity of the amplifier. The proof-of-concept system based on this architecture is shown in Figure 2.7 and is discussed in depth in Chapter 3. Chapter 4 showcases the complete design and simulation of a Q-enhanced LNA on-chip for Wi-Fi 6, designed in a 45 nm RFSOI process.

2.2.4 – Sensitivity of Positive Feedback Amplifiers

As a final remark, positive feedback based amplifiers are quite sensitive, and designers must be aware of the potential impacts of both process variation at the chip level and component variation at the board level. As will be seen in Section 4.2, small changes in the amount of positive feedback provided by the feedback network may cause the bandwidth of the amplifier's filter response to change significantly. The feedback network should be designed in such a way that the steps in attenuation, and hence bandwidth, are small around the oscillation point of the amplifier, as seen in Section 4.2.

Another note to make is that the tuning algorithm shown in Section 3.3 requires the amplifier to be put into oscillation, so designers must ensure that the oscillation is not large enough to disturb downstream devices. Designers must also ensure that the oscillation does not reach the input antenna and radiate back out of the receiver at levels above regulatory limits. To ensure that the oscillation does not radiate back out, an attenuator may be switched in between the input antenna and the primary amplifier during tuning of the system. Doing so will effectively take the amplifier "offline" and ensure that there is no unintentional radiation from the Q-enhanced receiver, which may violate FCC regulations.

Chapter 3 - BJT FM Band Q-Enhanced System

This chapter discusses the design and testing of a complete BJT-based auto-tuned Q-enhanced frontend for use in the FM band. A broad system level overview is presented first, with the following three subsections detailing the hardware and software utilized by the individual circuit boards that compose the full system. Finally, the relevant electrical characteristics and full system test results are presented.

3.1 – System Overview

The complete FM Band Q-enhanced system is composed of three separate subsystems, with each subsystem being housed on a different printed circuit board (PCB). The three subsystems are: the Q-enhanced filter board, containing the main amplifier, tuned-RF load, and feedback network; the auto-tuning board, responsible for filter measurements and tuning the amplifier core; and the FM receiver board, which provides the audible output of the FM station. Figure 3.1 illustrates this full system architecture.

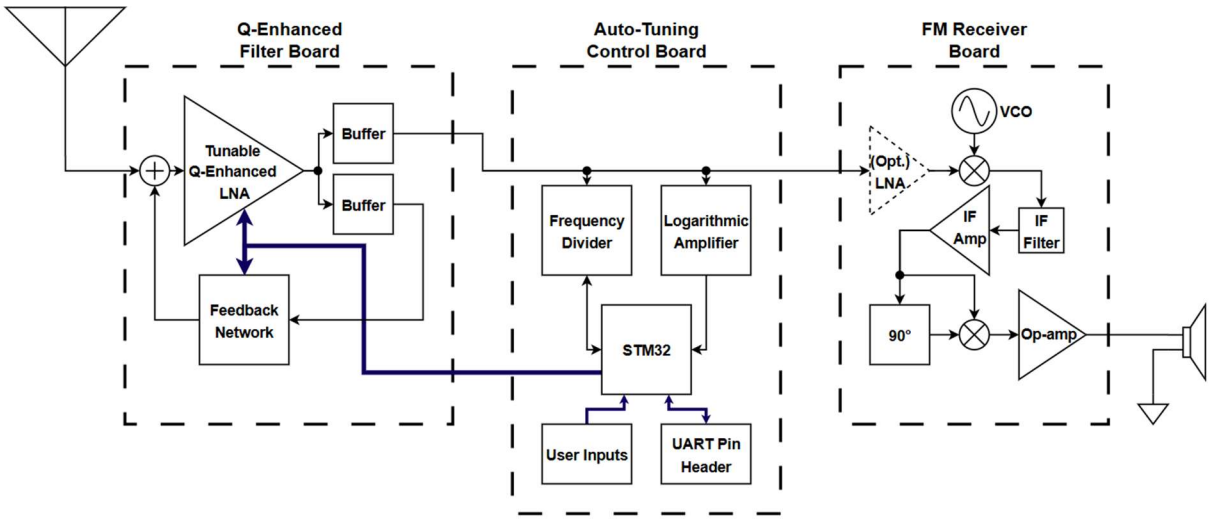

Figure 3.1. FM Q-enhanced system block diagram.

When the system is in operation, the received signal first hits the main Q-enhanced filter block, which serves as a moderate to high gain LNA with a built in ultra-narrow bandwidth preselect and image filter. The tuning of the Q-enhanced LNA and feedback network within this block is controlled by the auto-tuning control board. Upon selection of a desired frequency by the user, the microcontroller (MCU) briefly puts the Q-enhanced filter core block into oscillation by increasing the Q significantly and tunes it to the desired channel. When the center frequency reasonably matches that of the desired frequency, the system incrementally increases the attenuation in the feedback network, taking it out of oscillation and setting the desired bandwidth. Understanding the practical relationship between attenuation in the feedback network and filter bandwidth is described in Section 4.2, while the tuning algorithm is discussed at length in Section 3.3.2.

The amplified and filtered signal from the Q-enhanced core amplifier passes through a pair of buffers, one of which feeds into the feedback network while the other drives the board output. The design of the primary amplifier chain and feedback network is covered in Section 3.2. As previously mentioned, the auto-tuning control board is responsible for taking measurements of both frequency and power to be used in the auto-tuning algorithm that runs when a new desired frequency is selected. When the amplifier has been successfully tuned and the user is not selecting a new desired frequency, the auto-tuning control board sits idle and acts as a pass through with minor loss due to a resistive power splitter at the input of the board.

The final board in the system is a traditional superheterodyne FM receiver, responsible for taking the amplified RF signal, mixing it down to the FM intermediate frequency and demodulating it. This board provides an audible output signal of the FM radio station to an

external speaker. The full design of this board is outside the scope of this thesis, although basic functionality will be discussed in Section 3.4.

3.2 – Q-Enhanced Filter Board

The Q-enhanced filter board is the fundamental board in the full system, and its associated schematic is shown in Figure 3.2. This design is based on prototypes shown in [18].

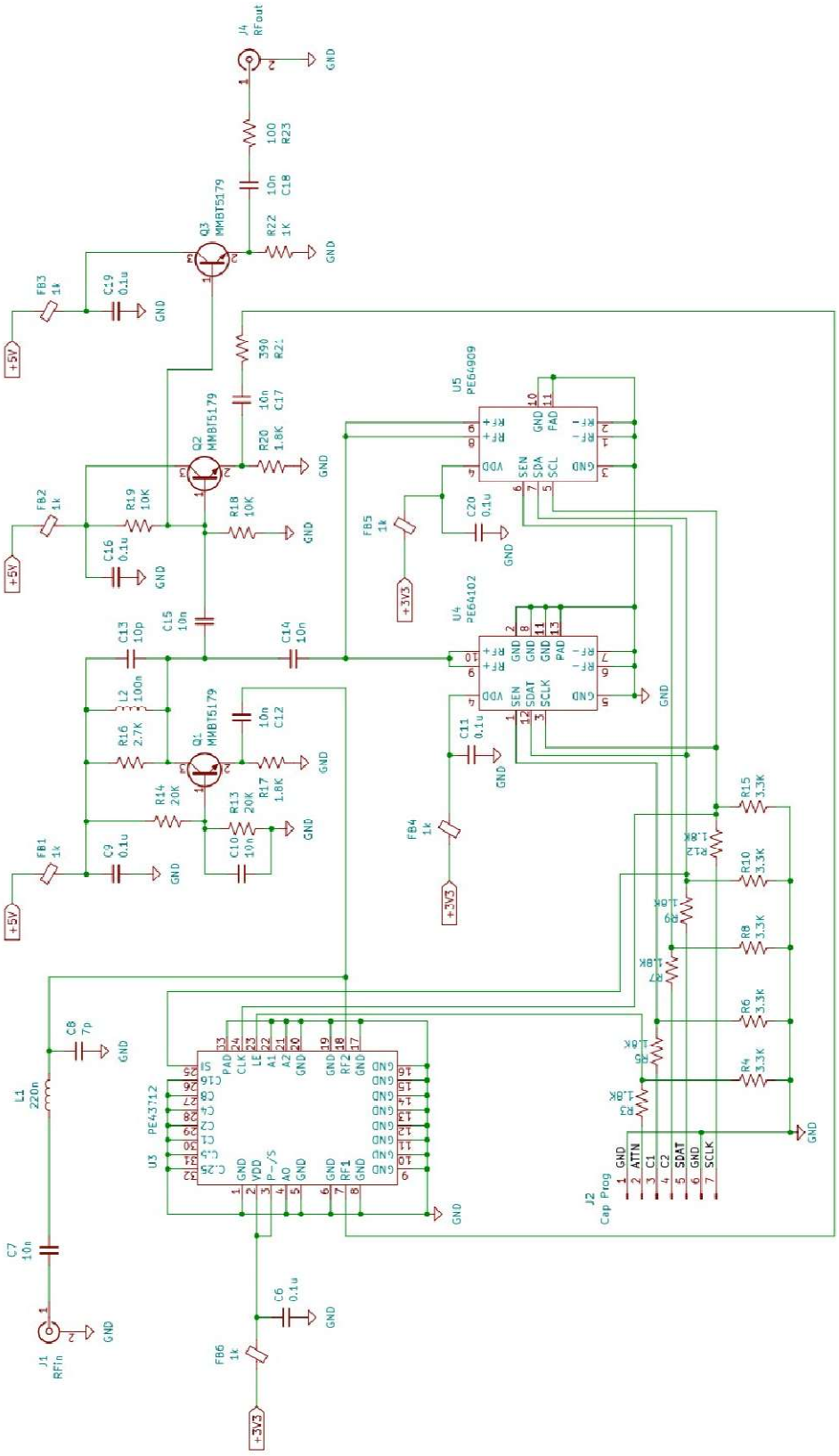

Figure 3.2. Q-Enhanced filter board schematic.

The board was designed as a proof of concept to verify that both the amount of positive feedback as well as the center frequency of the amplifier's filter response could be controlled and easily tuned, creating an auto-tunable ultra-narrowband Q-enhanced LNA. The design of the common-base (CB) core amplifier Q1 and common-collector (CC) amplifiers (buffers) Q2, Q3 follows procedures outlined in a typical undergraduate communication circuits course. The use of additional circuitry is required to achieve the Q-enhancement of the tank circuit formed by R16, L2, C13, as well as allow for tuning of both the positive feedback loop with the programmable attenuator, U3, and center frequency with digitally tunable capacitors (DTCs), U4, U5. Figure 3.3 depicts the board level block diagram of the Q-enhanced amplifier board.

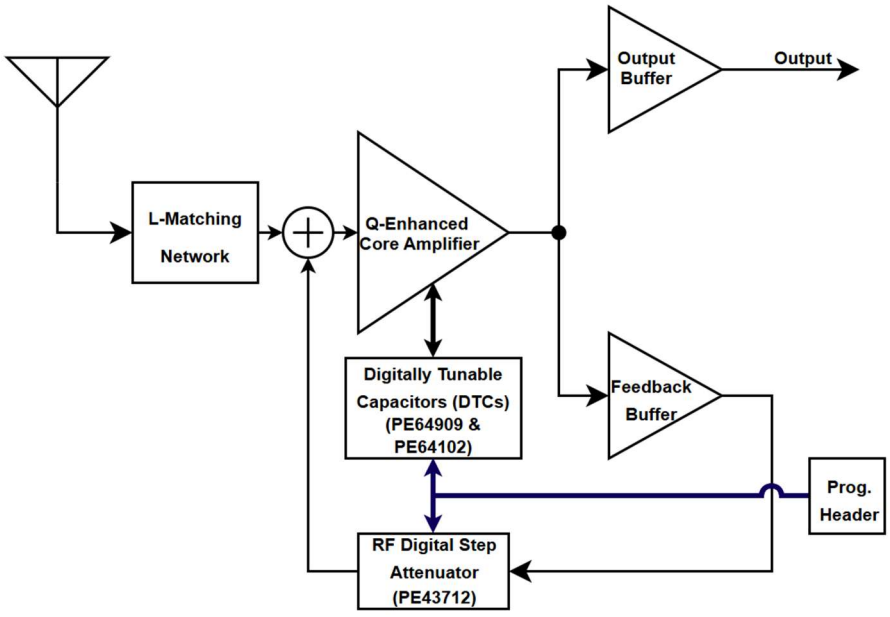

Figure 3.3. BJT Q-enhanced filter board block diagram.

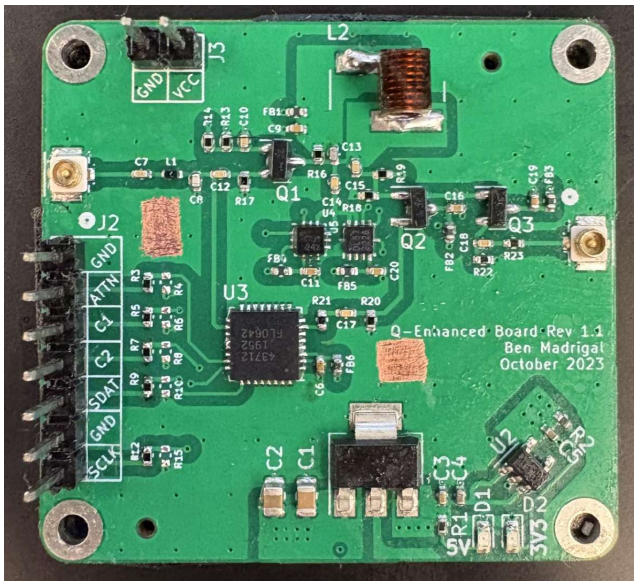

Figure 3.4. Assembled Q-enhanced amplifier board

Figure 3.3, shows the DTCs U4, U5 from Peregrine Semiconductor (pSemi) used for frequency tuning. The DTCs used are the PE64909 and PE64102, which allow for a variable capacitive load to be switched into the LC tank of the core amplifier to tune the filter's center frequency in steps of approximately 200 kHz. The PE64909 allows for 0.6 pF to 2.35 pF of capacitance to be added in 117 fF steps [17], while the PE64102 can switch in 1.88 pF to 14.0 pF of additional capacitance in 391 fF steps [16]. The addition of a combined 2.48 pF to 16.35 pF of capacitance from the DTCs allows the amplifier response to have a range of 40 MHz while maintaining channel bandwidth, allowing for the system to tune to any desired channel in the FM band.

While DTCs or some other form of tunable capacitors are needed for practical system design, they are not essential to the Q-enhancement of the amplifier. As shown in Section 2.2.1, the amount of positive feedback in the system is directly responsible for the increase in gain and selectivity. Additionally, a sufficiently large increase in the amount of positive feedback will put the amplifier into oscillation and allow for the tuning of the center frequency of the amplifier's

filter response. The PE43712 is a digitally programmable RF step attenuator that can step from 0 dB to 31.75 dB of attenuation in 0.25 dB steps [15], allowing for precise control over the gain and selectivity of the amplifier, and is able to take the amplifier in and out of oscillation. For this work, the 0.25 dB steps are crucial as small changes in the amount of positive feedback cause large changes in the gain and selectivity of the amplifier. Additionally, in this design the targeted 200 kHz channel bandwidth is only achievable by adding 0.25 dB of attenuation in the feedback network from the point of oscillation. Section 4.2 provides an in-depth discussion into the design of feedback networks to achieve desirable bandwidths for other applications such as Wi-Fi 6, where several different bandwidths can be used.

3.2.1 – BJT Core Amplifier Design

At the heart of the Q-enhanced filter board shown previously in Figure 3.2 is the singular amplifier Q1 that will be Q-enhanced by the feedback network and act as the main gain and filtering element in the system. This amplifier will be referred to as the core amplifier throughout the thesis, even as the design of this amplifier changes. In the case of the FM band design, the core amplifier is a common-base amplifier using an NPN BJT, depicted in Figure 3.5.

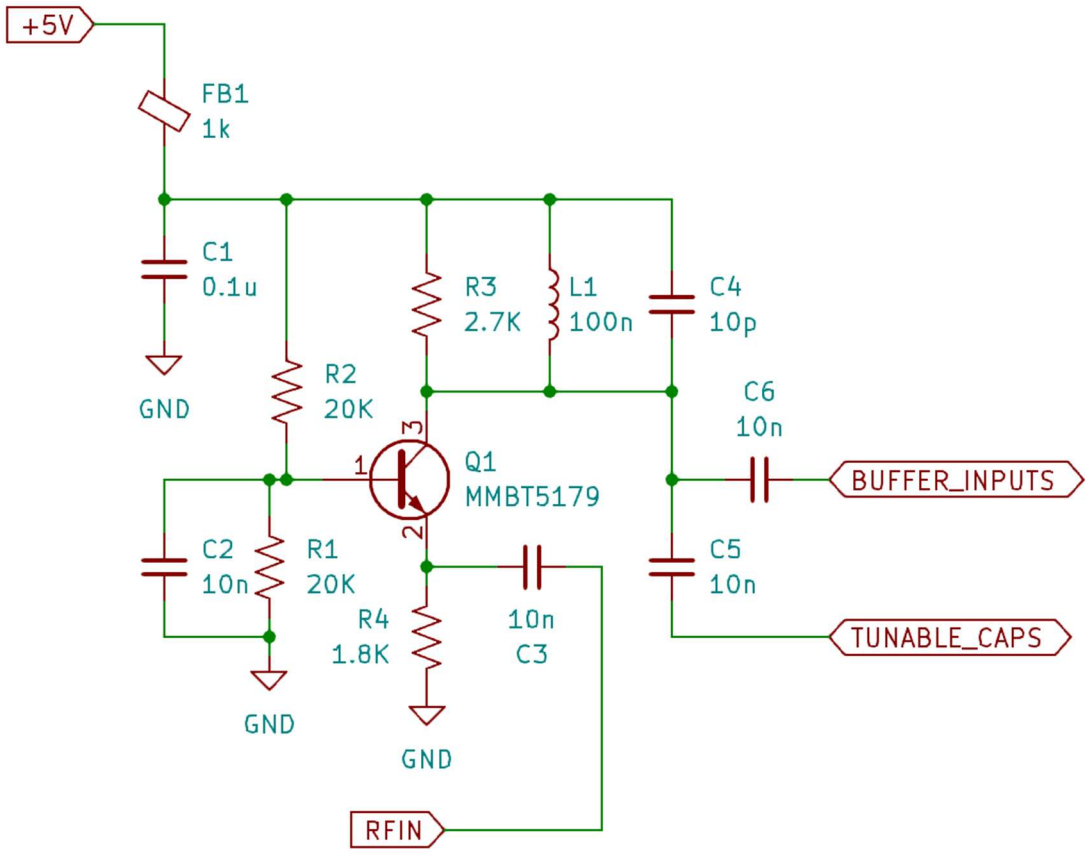

Figure 3.5. Q-Enhanced BJT core amplifier schematic.

The common-base core amplifier formed by Q1 has its base biased to mid-rail to maximize output voltage swing capability and has a nominal 1mA collector current. Knowing both the collector current and input impedance of the amplifier is crucial to the design of the L-matching network in Section 3.2.3. Equations (3.1) and (3.2) show how to calculate the input impedance of a common-base amplifier as shown in [14].

$$R_{IN} = \frac{1}{g_m} \tag{3.1}$$

$$g_m = \frac{I_C}{nV_t} \tag{3.2}$$

The calculation of amplifier transconductance, shown in Equation (3.2), requires use of the ideality factor, n, and thermal voltage, V_t. Thermal voltage itself is a function of temperature

and is roughly 25.8 mV at room temperature. Ideality factor accounts for the imperfect junctions of real transistors and typically ranges from 1-2. Prior classroom experimentation has shown that n is closer to 1.5 for the selected NPN BJT. The combined use of Equations (3.1) and (3.2) show that the input impedance of the core amplifier is 39 Ω.

The core amplifier is primarily loaded by the parallel combination of the collector resistor R3, as well as the input impedance of both the feedback and output buffers. The loaded gain of the core amplifier is roughly 12 dB when there is no positive feedback applied. It should be noted that the gain will change depending on the amount of positive feedback applied, and roughly a 36 dB gain can be achieved at channel bandwidth.

3.2.2 – BJT Buffer Design

The feedback and output buffers were designed to provide a stable load impedance to the output of the common-base core amplifier while being able to drive low impedance outputs. By using two separate buffers, the overall board output impedance will not be affected by positive feedback. The schematics for both the feedback and output buffers are shown in Figures 3.6 and 3.7.

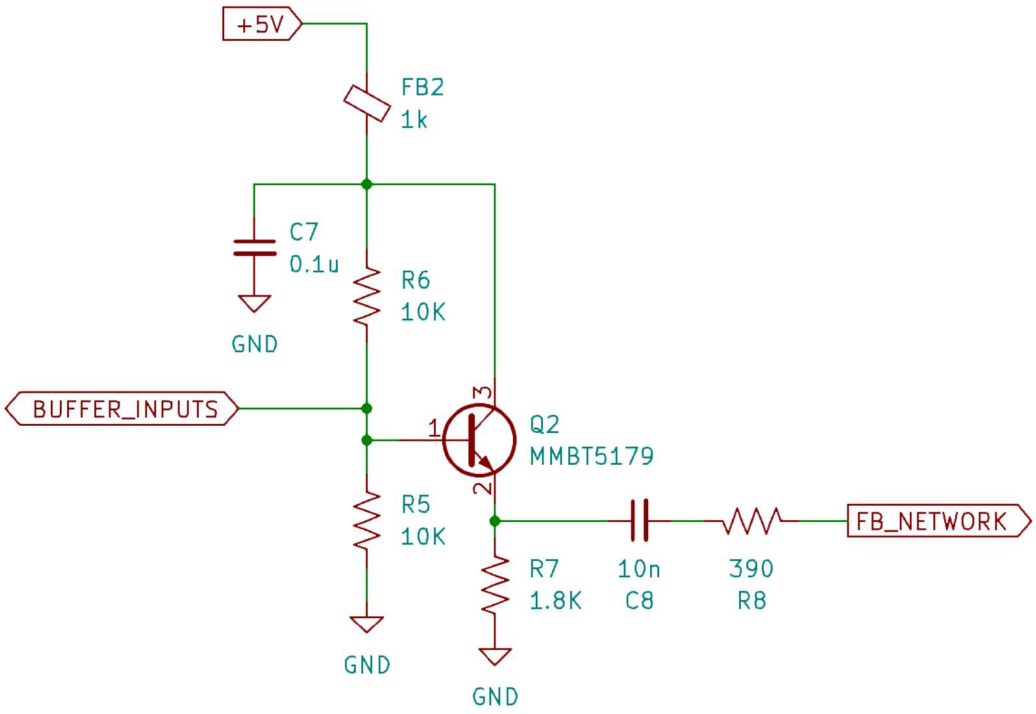

Figure 3.6. Feedback buffer schematic.

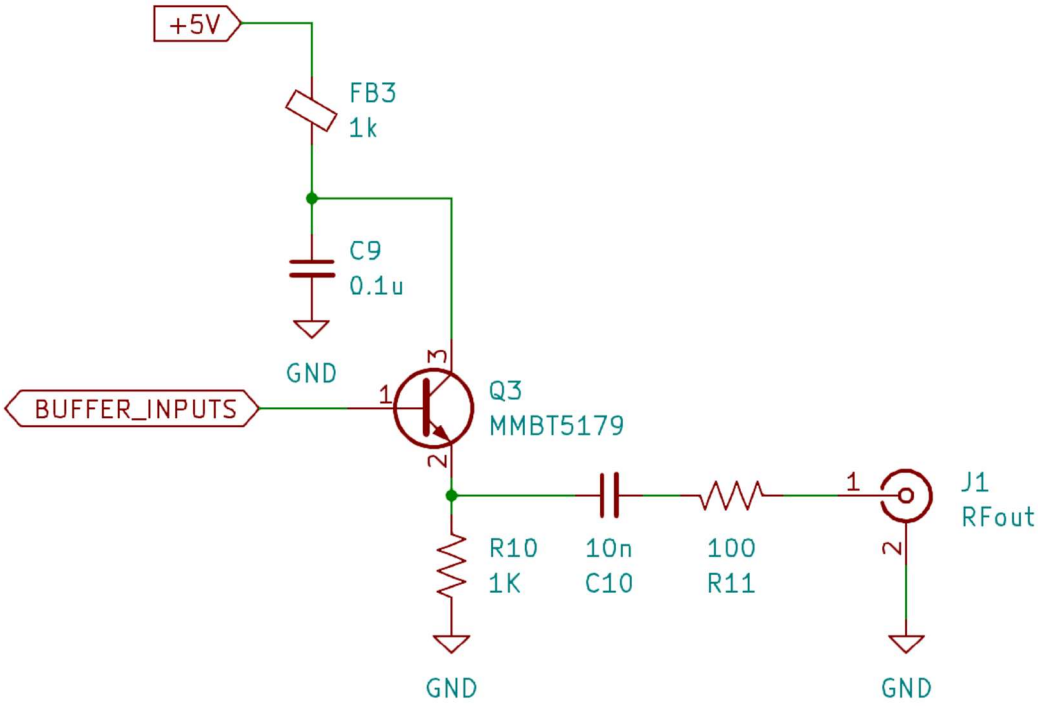

Figure 3.7. Output buffer schematic.

The two buffers pictured share a common base bias voltage at the “BUFFER_INPUTS” connection in Figures 3.6 and 3.7. Additionally, the buffers are nearly identical, differing only in collector current and in output impedance. At the output of the feedback buffer, the 390 Ω resistor R8 combined with the 50 Ω input of the programmable attenuator in the feedback network creates an additional 19 dB of attenuation in the feedback network needed to ensure the common-base core amplifier can exit oscillation. The output buffer is loaded by both the 50 Ω of the output connector, as well as a 100 Ω resistor R11. This additional 100 Ω resistor was added to increase the output compression point of the common-collector buffer.

To note, while the buffer nominally provides unity gain, the use of a 100 Ω resistor at the output of the board causes the signal to be attenuated by roughly 10 dB. This additional attenuation makes it important for the common-base core amplifier to provide sufficient gain, ensuring that the system still acts as an LNA, and not just a filter.

3.2.3 – L Matching Network Design

As discussed in Section 2.2.2 the use of a lumped element L matching network can provide additional attenuation to off-channel signals, making the amplifier more robust against large blocking signals and mitigating the generation of intermodulation products. From the viewpoint of the input of the core amplifier, the signal source impedance can be made to look much larger (e.g. 500 Ω) than the input impedance of the core amplifier itself. This creates a large voltage divider, providing 10 dB of attenuation or more to off-channel signals. As mentioned in Section 2.2.2, this large attenuation only affects off-channel signals, as the amount of positive feedback at the center frequency of the amplifier’s filter response will be much larger causing the core amplifier input impedance to rise drastically. Due to the rise in impedance at the

center frequency the attenuation will be significantly decreased, reaching 0 dB or above, preserving the desired signal while reducing the large off-channel signals.

The core amplifier discussed in Section 3.2.1 presents a nominal input impedance of 39 Ω and by matching the standard 50 Ω signal input to look like 500 Ω, another 10 dB or more of attenuation is applied by the voltage divider created by the now 500 Ω input impedance and the 39 Ω amplifier input impedance. Note, attenuation will not reach the nominal 20 dB expected by the voltage divider formed by a 39 Ω load and a 500 Ω input due to the reactance of the components used in the L matching network. The L matching network can be designed by using equations presented in [20] or visually with the use of the Smith chart. The exact understanding and use of the Smith chart is outside the scope of this work, but it provides an easy visual method of matching normalized impedances. Many programs, such as Advanced Design System from Keysight [3], provide a Smith chart calculator allowing for easy visual impedance matching. Figure 3.8 depicts the designed L matching network, matching 50Ω to 500Ω.

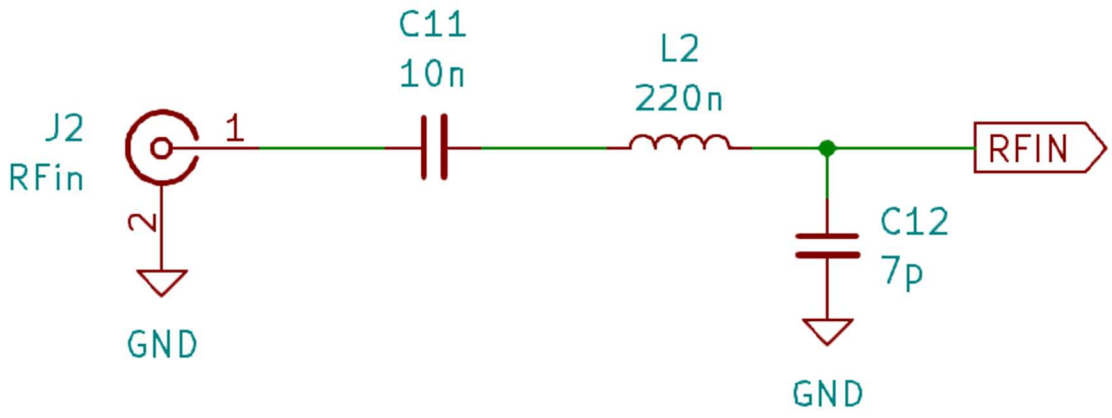

Figure 3.8. Core amplifier input L matching network.

As shown in the full schematic, the output of the L matching network formed by L2 and C12 is tied directly to the input of the core amplifier, as well as the output of the feedback

network. This matching network provides nearly 12 dB of attenuation to off-channel signals, while preserving the signal at the center frequency of the LC tank shown in Figure 3.5.

3.3 – Auto-Tuning Control Board

For the Q-enhanced amplifier to be tuned successfully, the amplifier must be put into oscillation. Although oscillation is normally not desired, it is essential as the oscillating signal is used to locate and change the center frequency of the amplifier, as well as provide indication of how much attenuation needs to be added in the feedback network to achieve a given bandwidth. Being able to control the feedback and center frequency of the amplifier, and hence the gain and bandwidth, is the core principle of an auto-tunable ultra-narrowband Q-enhanced amplifier.

To effectively measure the frequency and power level of the oscillating signal, the auto-tuning control board houses both a logarithmic amplifier and frequency synthesizer, as well as a microcontroller that uses measurements from both devices in the auto-tuning algorithm. Figure 3.9 illustrates the board level block diagram of the auto-tuning control board, while Figure 3.10 shows an assembled auto-tuning control board.

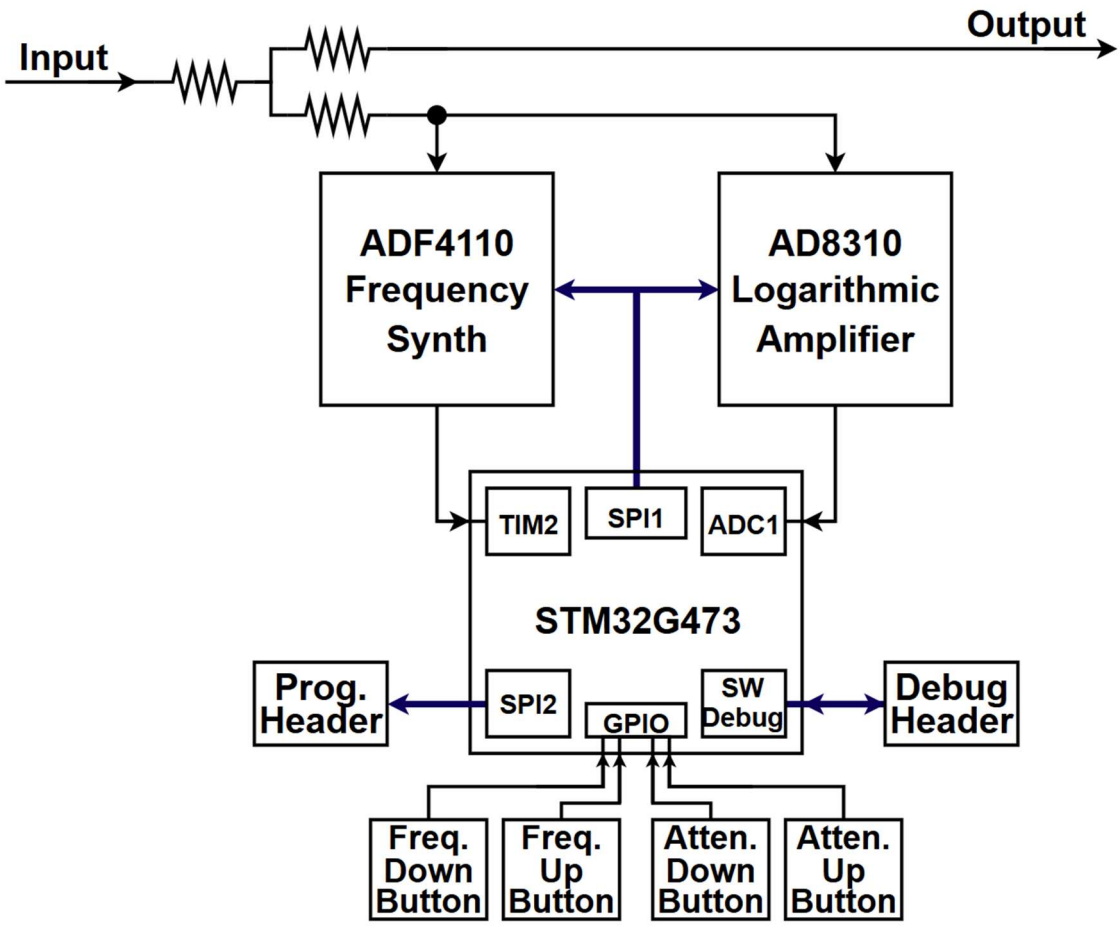

Figure 3.9. Auto-Tuning Control Board block diagram.

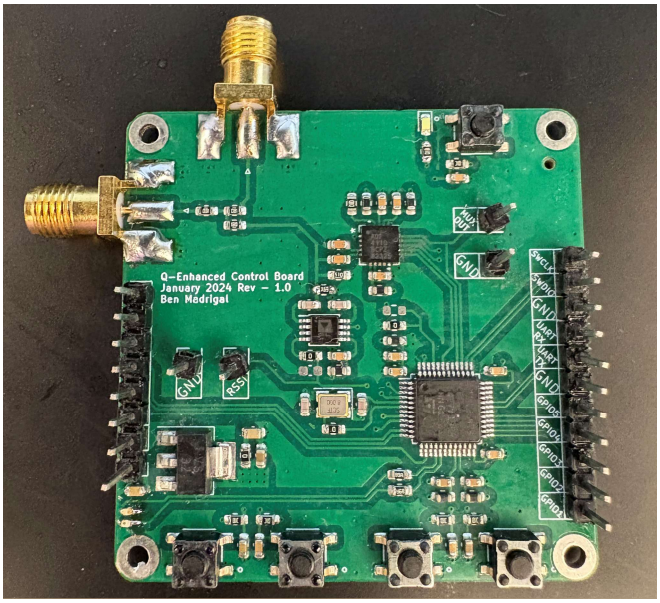

Figure 3.10. Assembled auto-tuning control board.

The key components on the auto-tuning control board are the ADF4110 frequency synthesizer and AD8310 logarithmic amplifier, both from Analog Devices, as well as the STM32G473CB from STMicroelectronics. The ADF4110 is used solely for its frequency divider capability, prescaling the RF signal before reaching the microcontroller. The selected microcontroller has many desirable peripherals, including multiple 12-bit analog-to-digital converters (ADCs) and both 32-bit and 16-bit general purpose timers with input capture channels [23]. The microcontroller also has several serial communication buses, namely SPI and UART which are used for programming of the DTCs and programmable step attenuator on the Q-enhanced filter board, as well as programming of the frequency synthesizer's prescaler divider ratios.

The AD8310 logarithmic amplifier has 95 dB of dynamic range, and is typically used for antenna power measurements, received signal strength indication (RSSI), and conversion of signal level to logarithmic form [4]. Unlike a normal operational or RF amplifier, a logarithmic amplifier produces an output voltage that is approximately proportional to the logarithm of the input, allowing for measurement of input power. Knowing the power level of the signal coming from the core amplifier allows the system to determine if the amplifier is oscillating or not, and how to adjust the positive feedback network accordingly. Oscillation of the core amplifier is required for the auto-tuning algorithm, as the amplifier will oscillate at, or close to, the center frequency of the LC tank of the core amplifier. As discussed in Section 4.2, being able to determine when the amplifier enters oscillation is also essential for being able to determine how the positive feedback network should be adjusted to achieve a desired amplifier gain and bandwidth.

The logarithmic amplifier datasheet provides the essential equation for output voltage based on the power of the input signal, shown here in Equation (3.3) [4].

$$V_{OUT} = V_{SLOPE}(P_{IN} - P_O) \tag{3.3}$$

V_{OUT} denotes the output voltage of the logarithmic amplifier, which is approximately proportional to the logarithm of the input signal. The quantities V_{SLOPE} and P_O denote the slope and intercept of the logarithmic response of the amplifier, specified as 24 mV/dB and -95 dB respectively. The final quantity P_{IN} is the measured power of the signal, and Equation (3.3) can be rearranged for P_{IN} as shown in Equation (3.4). By measuring the voltage V_{OUT} with an ADC channel on the MCU, Equation (3.4) can be used to calculate the power of the oscillating signal for use in the tuning algorithm.

$$P_{IN} = \frac{V_{OUT}}{V_{SLOPE}} + P_O \tag{3.4}$$

The frequency of the oscillating signal is also used by the tuning algorithm to adjust the capacitance provided by the DTCs, changing the center frequency of the LC tank in the core amplifier. While the selected frequency synthesizer can be used to implement a local oscillator, it has been configured to only act as a frequency divider in this application. The frequency divider is needed as measurement of the direct RF signal is impractical. The frequency synthesizer requires additional effort to use compared to the logarithmic amplifier, as programming is needed upon power up to set internal latches to the desired configuration.

The frequency divider is implemented by an N counter, consisting of a dual-modulus RF prescaler with division ratio P / P + 1, 6-bit A counter, and 13-bit B counter, where the overall division ratio N is defined by Equation (3.5) [5].

$$N = BP + A \tag{3.5}$$

The now divided signal then connects to an MCU timer, specifically TIM2, which has been configured to have its counter driven by the divided oscillation signal. By knowing the counter value of TIM2 after a given amount of time, the input frequency to the TIM2 channel can be calculated. An additional timer, TIM5, has been leveraged such that the counter threshold of TIM5 will be reached in 20 ms, at which time the timer callback will be called, and the count value of TIM2 will be stored. By dividing the count value of TIM2 by 20 ms and multiplying by the division ratio N, the original oscillation frequency can be estimated. The frequency synthesizer should be configured to be the lowest division ratio, minimizing tuning time, while still providing reasonable counter values. To set the value of the N divider and output the divided signal to the MCU, the reference, N counter, and function latches need to be programmed on boot. These registers are responsible for setting the prescaler and A/B counter values, as well as configuring the multiplexer (mux) out pin. Figures 3.11, 3.12, and 3.13 show the latch maps for each of the three latches that need to be programmed.

RESERVED	DLY	SYNC	LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	DLY	SYNC	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

X = DON'T CARE

Figure 3.11. ADF4110 Reference latch map [5].

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

X = DON'T CARE

Figure 3.12. ADF4110 N Counter latch map [5].

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

Figure 3.13. ADF4110 Function latch map [5].

While the datasheet provides significant detail into the functionality of every bit in the shown latch maps, the primary focus in this work is the programming of the proper prescaler and counter values, as well as the mux out pin. The minimum division ratio that can be achieved by the ADF4110 is 24, obtainable by programming the N counter and function latch with the minimum prescaler and A/B counter values. The reference latch does not contain any bits that need to be programmed for this use case and can effectively be ignored. Table 3.1 provides the codes to programmed into each latch to achieve the minimum division ratio and set proper operation of the mux out pin.

Latch Name	Programmed Value	Functionality
Reference	0x000004	N/A
N Counter	0x000301	Set division ratio of A and B counter to 0 and 3 respectively
Function	0x000022	Set prescaler to 8/9 and N divider to mux out

Table 3.1. ADF4110 latch values.

Having discussed the use of both the logarithmic amplifier and frequency synthesizer to take power and frequency measurements of the oscillation signal, an in-depth discussion of the auto-tuning algorithm is presented in Section 3.3.2.

3.3.1 – Auto-Tuning Algorithm Background

The auto-tuning algorithm requires minimal effort from the user to tune the amplifier's filter response to the appropriate gain, bandwidth, and center frequency. The auto-tuning control board has several button inputs to let the user set the desired radio station frequency and start the

tuning algorithm. As previously discussed, the output signals from both the logarithmic amplifier and frequency divider are used to adjust both the attenuation in feedback network and the DTCs on the Q-enhanced filter board discussed in Section 3.2.

In the time when the auto-tuning algorithm is not running, the user can change the desired radio station frequency in 200 kHz steps with the use of two push buttons. When the user has selected a desired frequency, the auto-tuning algorithm can be initiated by another push button to tune the bandwidth, gain, and center frequency. Note, while the user must tell the tuning algorithm to start in this design, it is preferred for the system to auto-tune as the user changes the desired frequency. This behavior would closely mimic that of a normal radio.

3.3.2 – Basic Algorithm

When the tuning algorithm is initiated, the microcontroller will program the step attenuator to 0 dB attenuation, causing the core amplifier to start oscillating. At that point the tuning algorithm will start, first tuning the center frequency of the amplifier's filter response before tuning the gain and bandwidth as it takes the amplifier out of oscillation. Figure 3.14 illustrates the flow of the tuning algorithm at the time of writing.

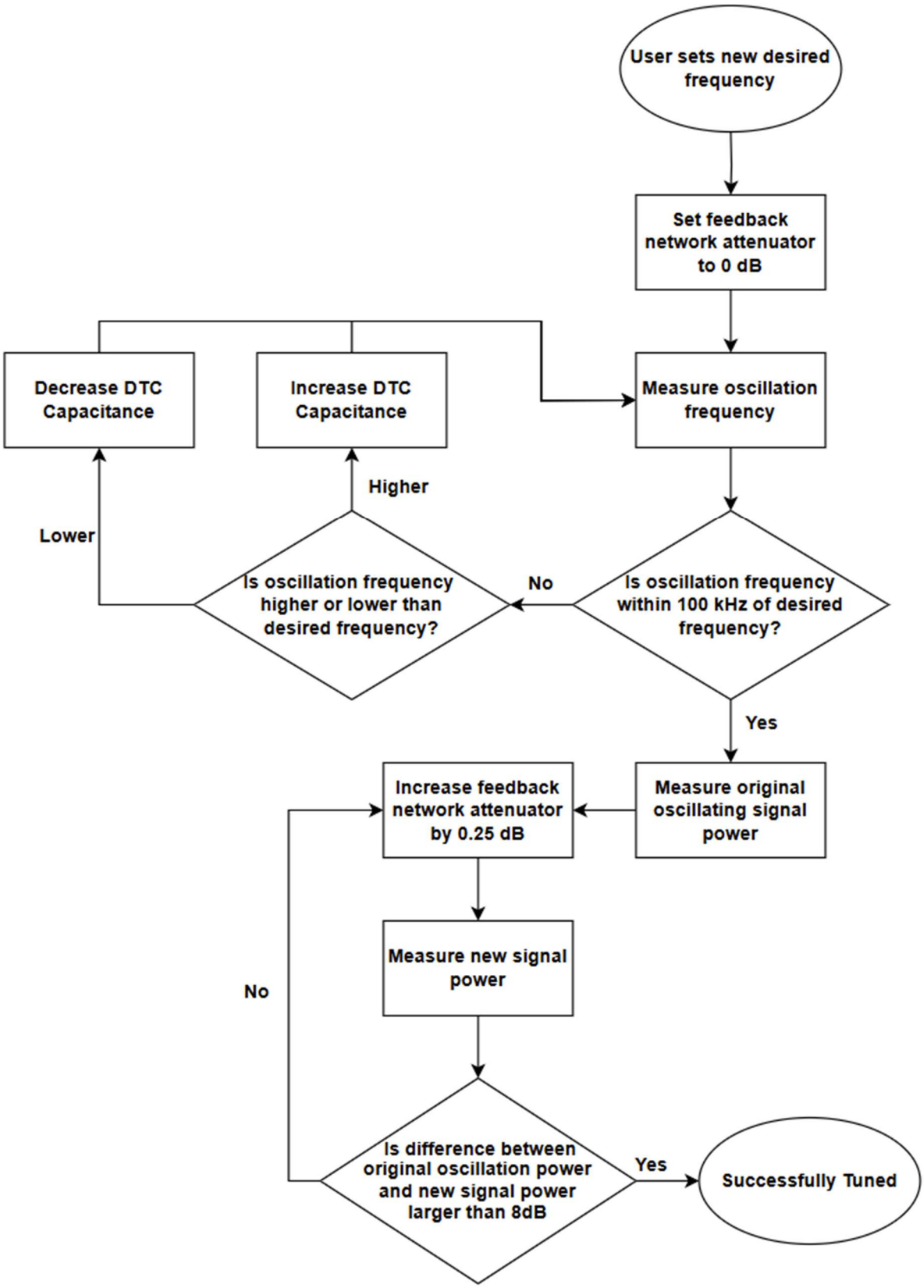

Figure 3.14. Flow diagram of auto-tuning algorithm.

There are several modifications that could be made to the tuning algorithm to increase tuning precision and prevent unintended emissions. As mentioned in Section 2.2.4, when the amplifier is in oscillation for tuning, there is the potential for the oscillating signal to reach the RF input, which is presumably an antenna, and unintentionally radiate back out of the system. This unintended radiation has the potential to violate regulations set by the FCC or other government agencies. To reduce the risk of this occurring, an additional programmable attenuator could be added to input signal chain, directly after the input connector. In normal operation this attenuator would be set at 0 dB, while during tuning the attenuation could be increased to a large value, like 40 dB, and effectively take the amplifier "offline". This additional attenuation between the input connector and the oscillating amplifier should provide enough protection against unintended radiation.

Additionally, Figure 3.14 shows two hardcoded decision parameters that prevent the tuning algorithm from continuously looping trying to achieve an exact center frequency or power. The first hardcoded parameter is the center frequency tolerance of 100 kHz. A range of 100 kHz either side of the desired frequency ensures that the desired frequency essentially receives the full gain. The second hardcoded parameter is used in determining if the amplifier has fallen out of oscillation based on measured power level. A value of 8 dB was set based on physical testing of the system, as a large jump in power was observed as the amplifier switches in and out of oscillation. By knowing the power of the oscillating signal, attenuation can be added in the feedback network until a large decrease in measured signal power occurs, at which point we make the claim that the amplifier is no longer oscillating.

These hardcoded values can be modified to produce more precise, and consistent tuning results. There are several known issues that can be mitigated by optimizing or altering the auto-

tuning algorithm. Firstly, the auto-tuning algorithm, at present, does not always take the amplifier completely out of oscillation. By increasing the power difference required to claim that the amplifier is out of oscillation, this problem should be solved. Additional attenuation could be switched in to ensure that the amplifier is no longer oscillating, even after the algorithm determines that the amplifier is out of oscillation.

Another issue is that the frequency of the oscillating signal differs slightly from the center frequency of the amplifier's filter response when the amplifier is no longer in oscillation. This can cause the amplifier's filter response to not land on the desired frequency, even though the tuning algorithm had deemed it to be reasonably aligned, causing the desired signal to be potentially attenuated. A more thorough characterization of this shift in frequency caused by the amplifier entering and exiting oscillation is needed.

3.4 – FM Receiver Board

The final board in the system is the FM receiver board. This board was originally designed as a final project for a university course at Kansas State University. The university course focuses on the design of RF amplifiers, matching networks, voltage-controlled oscillators (VCOs) and the design, construction, and testing of both an FM transmitter and receiver. Figure 3.15 depicts a system level overview of the FM receiver board, while Figure 3.16 depicts the assembled PCB.

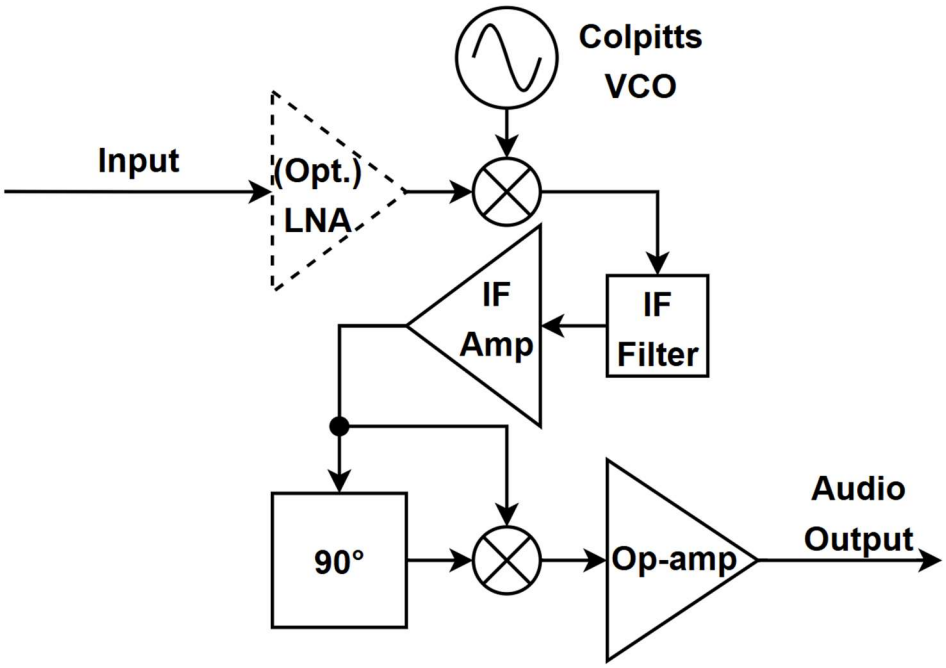

Figure 3.15. System overview of FM receiver board.

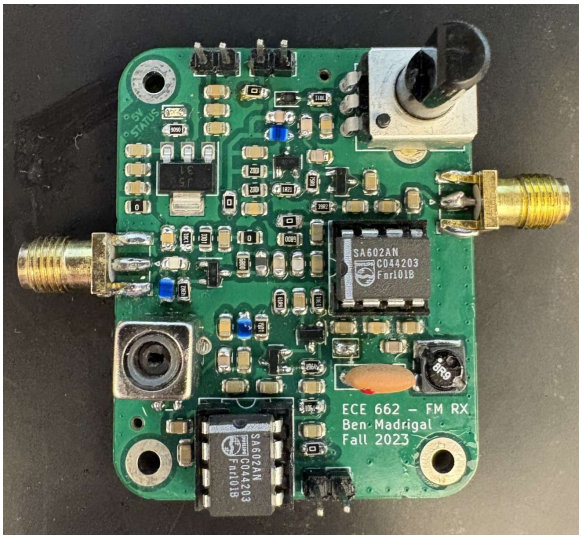

Figure 3.16. Assembled FM receiver board.

Since the board was originally designed as a part of a university course and not intended to be used in line with a Q-enhanced amplifier, the board has an “optional” non-Q-enhanced LNA at the board input. During system testing, this LNA can be bypassed by removing the

biasing circuitry and transistor and soldering a jumper wire from the board input to the intended amplifier output. There is also an onboard VCO that was designed using the Colpitts topology, responsible for creating the LO signal that will mix with the RF input to create the IF signal. The oscillation frequency of the Colpitts VCO is controlled by a potentiometer and requires the use of a spectrum analyzer to get precise LO frequencies.

The RF input signal and the VCO signal are mixed using a SA602AN mixer which provides another 14 dB of gain [21] and outputs the IF signal at 10.7 MHz. The IF signal passes through a ceramic filter centered at 10.7 MHz with a bandwidth of 280 kHz [13]. This is the final channel-selection filter before IF amplification. The IF signal then passes through an additional cascode amplifier providing 27 dB of gain to the IF signal.

Finally, the amplified IF is delivered to a traditional FM quadrature demodulator composed of a mixer and phase-shift network. After lowpass filtering, the output of this final mixer is the audible FM radio station signal, and an external op-amp or audio amplifier can increase the volume level of the radio station, although it is not required.

In lieu of using the FM receiver board & external speaker, a handheld radio such as the Yaesu VR120 [25] can be connected to the output of the Q-enhanced LNA and associated auto-tuning control board via an SMA to BNC coaxial cable or connector. Using a handheld radio to demodulate the RF signal may prove to be easier than using the board described here, as the VR120 will accurately tune and demodulate the FM signal with no issue.

3.5 – System Performance

To verify that an ultra-narrowband Q-enhanced LNA is capable of mitigating or preventing the issues discussed in Section 1.1, the system was assembled and connected to a large, external antenna capable of picking up the FM band. For ease of testing, the Yaesu VR120

was used instead of the FM receiver board discussed in Section 3.4. Figure 3.17 shows the complete system test up.

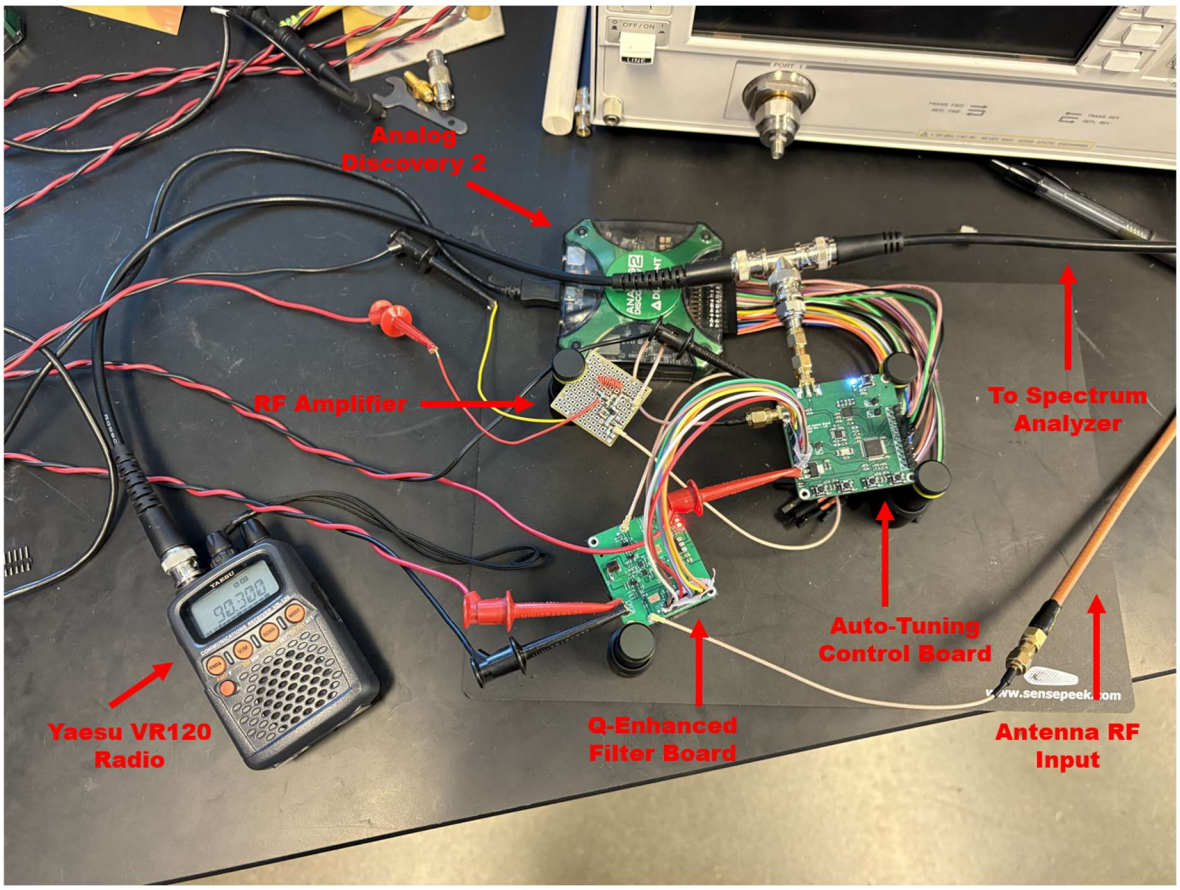

Figure 3.17. FM Q-enhanced system test setup.

It is important to note the use of an additional RF amplifier and Analog Discovery 2 (AD2). The AD2 is used to communicate with the auto-tuning control board over UART, as the control board reads out the desired frequency as the user changes it, as well as the current frequency and attenuation during the tuning algorithm. The RF amplifier provides additional gain to the Q-enhanced filter board output before it reaches the auto-tuning control board. While the additional gain is not needed for successful signal reception, it is needed to increase the oscillating signal power during the tuning algorithm as the frequency divider expects a minimum power of –10 dBm. If the oscillation is not at a high enough power, the frequency synthesizer

will output an inaccurate divided signal leading to inaccuracy in the tuning algorithm. Future iterations should use a frequency synthesizer, or divider, with a lower minimum input sensitivity.

A spectrum analyzer was used to visually verify that the system mitigates or prevents the discussed issues by measuring the power of several signals before and after the Q-enhancement is performed by the tuning board. As shown in Figure 1.5, there is potential for the signals at 96.3 MHz and 93.3 MHz to produce an intermodulation product that will overlap with the signal at 90.3 MHz based on the equations provided in Section 1.1. Figure 3.18 shows a zoomed in version of Figure 1.5, with markers denoting signal power level and frequency. Note, the power levels shown in Figure 3.18 and Figure 3.19 are shown to be lower than they are, due to the RBW being set at 3 kHz. Although the following discussion will use the measured power levels, it should be understood that the power levels are significantly higher, allowing the signals at 93.3 MHz and 96.3 MHz to generate an intermodulation product.

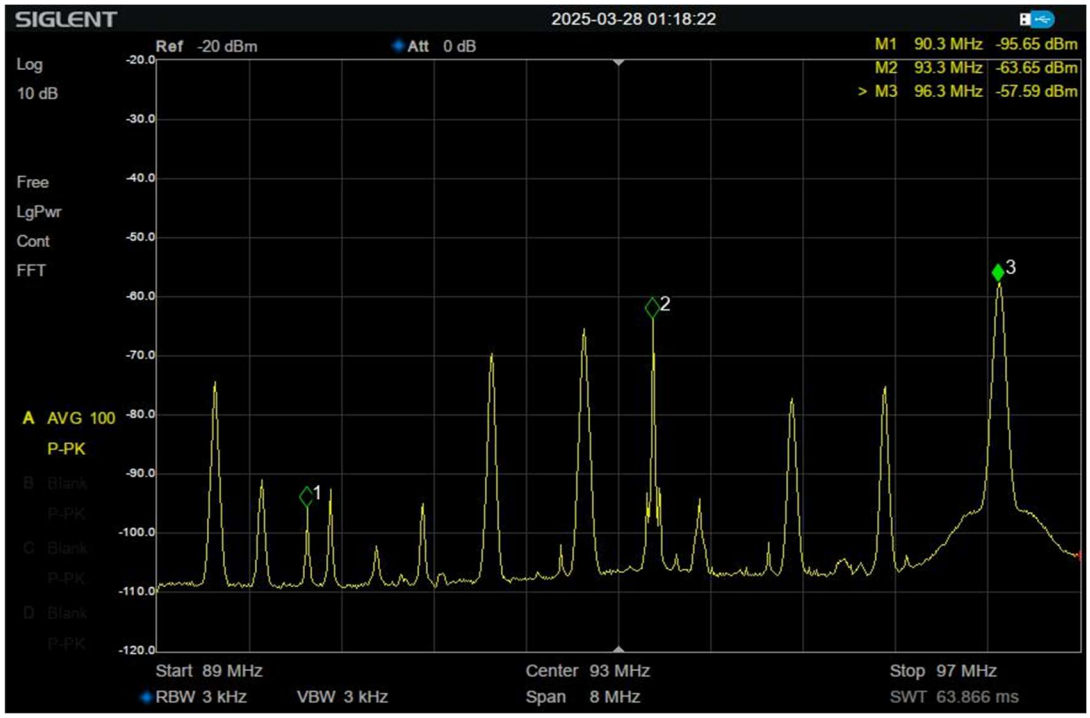

Figure 3.18. FM Spectrum pre-Q-enhancement, 89 MHz to 97 MHz

The signals with potential to generate an intermodulation product are the signals of the radio stations at 96.3 MHz and 93.3 MHz, with power levels of -57 dBm and -63 dBm respectively. From the equation $2f_1 - f_2 = f_o$, an intermodulation product can be expected at 90.3 MHz, which will overlap with the actual signal at 90.3 MHz. In fact, when the VR120 is tuned to 90.3 MHz without tuning the system, a combination of the radio stations at 93.3 MHz and 96.3 MHz can be heard, with the desired station at 90.3 MHz being inaudible.

If the actual radio station at 90.3 MHz can be heard clearly by tuning the system to 90.3 MHz, with no audible presence of the radio stations at 93.3 MHz and 96.3 MHz, that should be sufficient to determine that the Q-enhanced system works. Figure 3.19 shows the spectrum after tuning the system to 90.3 MHz.

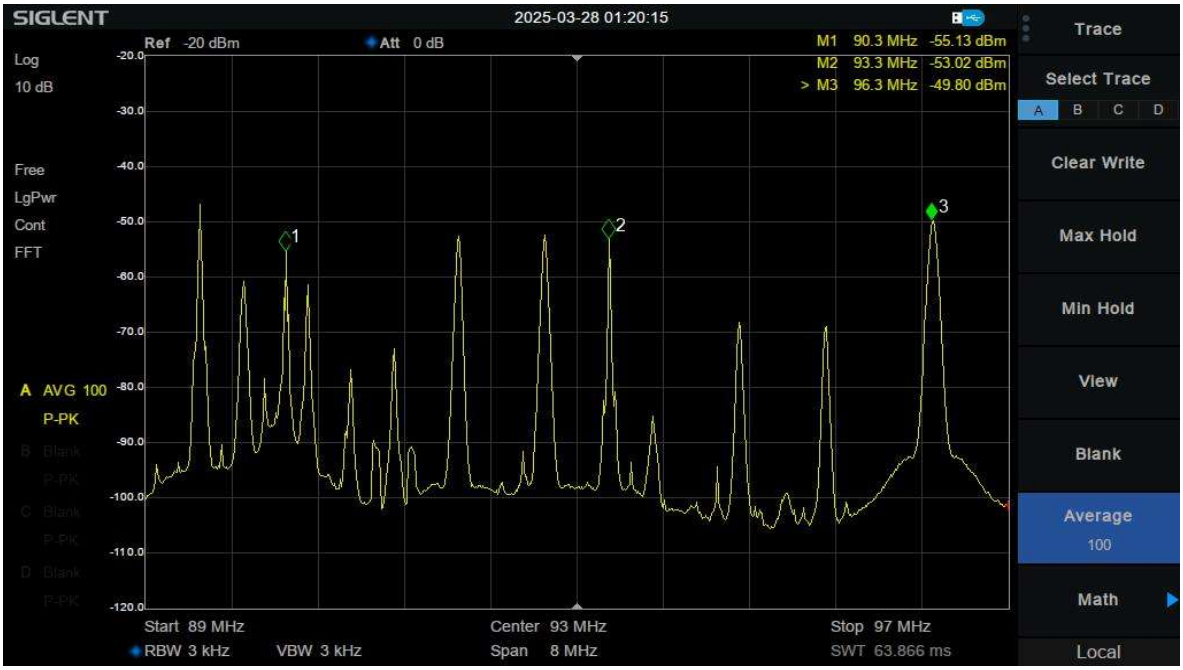

Figure 3.19. FM Spectrum post-Q-enhancement, 89 MHz to 97 MHz.

There is a substantial visible difference in the power level in the lower portion of spectrum shown in Figure 3.19 when compared to Figure 3.18. The signal at 90.3 MHz is 40 dB larger than it was before the tuning, while the power level of the signals at 93.3 MHz and 96.3

MHz did not receive nearly as much gain. Table 3.2 presents the measured power levels pre- and post-Q-enhancement.

Signal Frequency	Power Pre-Tune	Power Post-Tune	Change
90.3 MHz	-95.65 dBm	-55.13 dBm	40.52 dB
93.3 MHz	-63.65 dBm	-53.02 dBm	10.63 dB
96.3 MHz	-57.59 dBm	-49.80 dBm	7.79 dB

Table 3.2. Effect of auto-tuning and Q-enhancement on signal power level.

As expected, the bulk of the gain is applied to the signal at the frequency that has been tuned to. Additionally, with the VR120 tuned to 90.3 MHz, the actual radio station at that frequency is audible while the intermodulation product that was once present at this frequency is no longer audible. Effectively, the intermodulation product has been suppressed, solving the issue. From the results in Table 3.2, it is also apparent that the blocking issue has been addressed. This is evident by the fact that the off-channel signals did not receive the same amount of gain as the signal at the tuned to center frequency. This indicates that large, off-channel signals will not compress the LNA, and the desired signal will receive the full gain of the LNA.

As an additional note, the complete system draws 60 mA from a 9 V power supply. The majority of the power draw is from the auto-tuning control board, and can be reduced by utilizing the low-power features present on many different STM32 microcontrollers. The Q-enhanced filter board itself, only draws about 12 mA from the 9 V power supply. Of the 12 mA drawn by the Q-enhanced filter board, over half of it goes to the LEDs to show the system is powered on, while the programmable attenuator, DTCs, core amplifier, and buffers only account for about 4 mA. The crucial components of the auto-tunable Q-enhanced LNA only consume 36 mW, making this architecture suitable for low-power applications.

The results presented in this section confirm that a Q-enhanced receiver architecture addresses the issues discussed in Section 1.1. While there are still many portions of the Q-enhanced system that can be optimized, as a proof-of-concept system it verifies that this is a feasible architecture to use in a real-world environment and should be further developed. Chapter 4 presents the design of a tunable Q-enhanced LNA at the chip level, for use with 802.11ax, also known as Wi-Fi 6.

Chapter 4 - 2.4 GHz CMOS Q-Enhanced LNA

Having shown that the proof-of-concept board-level system covered in Chapter 3 is able to mitigate or prevent both blocking and intermodulation product issues, this chapter discusses the design of a Q-enhanced LNA in a 45nm CMOS RFSOI process. The Q-enhanced LNA was designed to meet 802.11ax, commonly known as Wi-Fi 6, channel bandwidths at 2.4 GHz outlined in [12]. The bandwidths used at 2.4 GHz are 20 MHz or 40 MHz, and while the designed LNA can meet these required bandwidths with its on-chip programmable feedback network, future development must be done to allow the LNA to tune to the center frequencies of each Wi-Fi channel. The center frequencies of these channels are presented in [12] and are in the 2.4 to 2.5 GHz range.

This chapter starts by discussing the core building blocks, such as the two-stage common-gate core amplifier, and the common-drain buffers. Emphasis is placed on the design of the feedback network, as great care must be taken to ensure that desired bandwidths can be met with reasonable precision across process variation and from run to run. Additionally, the feedback network design and core amplifier design are shown to impact noise figure significantly. The chapter concludes by presenting the full design of the Q-enhanced LNA as well as a variety of simulation results. At the time of writing, the physical chips were not available for validation of circuit functionality and simulation results. This presents an opportunity for future work, as discussed in Section 5.2.

4.1 – Core Building Blocks

Similar to the Q-enhanced filter board discussed in Section 3.2, the on-chip Q-enhanced LNA consists of both a primary amplification stage as well as two buffers, one being used for the overall output while the other drives the feedback network. The core amplifier making up the

LNA is discussed in Section 4.1.1, while Section 4.1.2 discusses the basic design of the common-drain buffers. An L-matching network is also used to provide additional attenuation to off-channel signals, as previously discussed in Section 2.2.2 and Section 3.2.3, although it is implemented off chip. Section 4.1.3 briefly covers the design and use of an L matching network for this design.

4.1.1 – CMOS Core Amplifier Design

The core amplifier went through several different designs, with both the amplifier topology and biasing network design changing with each iteration. A two-stage common-gate amplifier topology was eventually selected as it provides a reasonable non-Q-enhanced gain, and low input impedance for off-channel signals. Two different versions of the core amplifier were designed, known as version 2 (v2) and version 3 (v3), with the only difference being the technique used to set the amplifier's bias current. Version 2 uses a current mirror to set the bias current, while version 3 uses a resistor at the source of the first stage amplifier's transistor. Figures 4.1 and 4.2 display the schematics for the two-stage common-gate amplifier of version 2 and version 3 respectively.

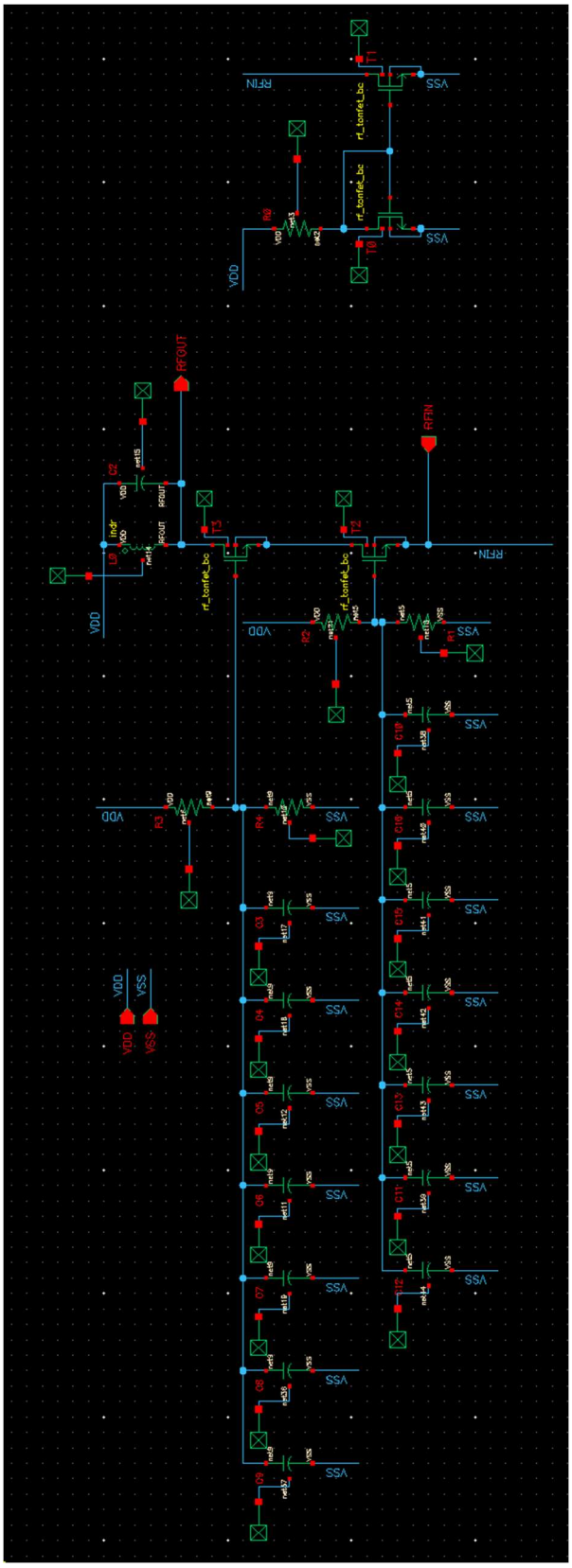

Figure 4.1. Chip level Q-enhanced LNA core amplifier v2 schematic.

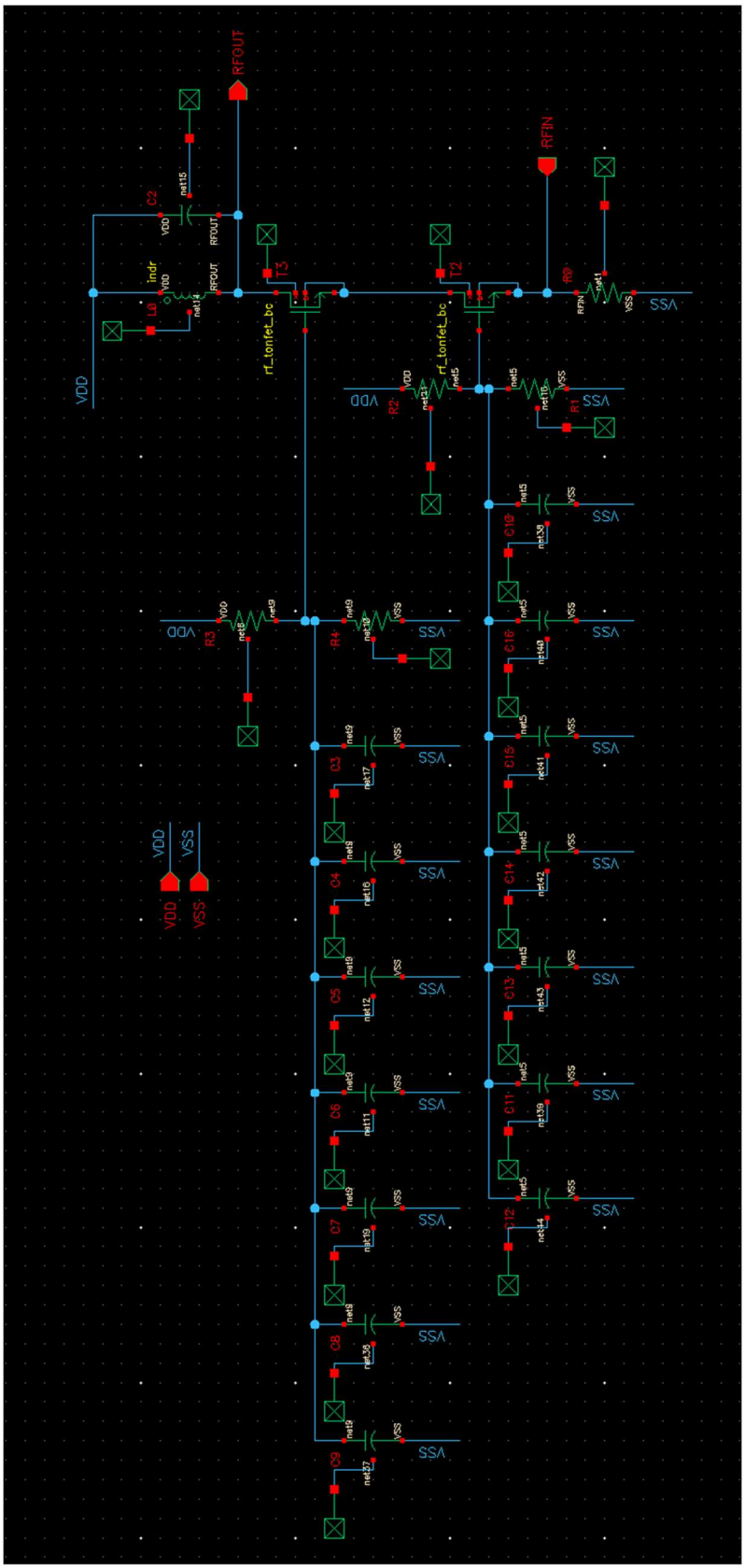

Figure 4.2. Chip level Q-enhanced LNA core amplifier v3 schematic.

In both versions of the core amplifier, the drain current and gate bias voltages are identical. It is important to note that the power supply voltage (VDD) is 1.8 V, with the gate bias voltages set by two individual voltage dividers. The gate of the top NFET, shown as T3 in both Figure 4.1 and 4.2, is biased to 1.5 V, while the gate of the bottom NFET, denoted as T2 in the same figures, is biased to 1.0 V. These bias points should allow for significant signal swing before reaching cutoff. Additionally, the gates of both T2 and T3 must have an AC connection to ground, which is achieved with two sets of capacitor banks each composed of parallel identical vertical natural capacitors (VNCAPs). A parallel combination of identical capacitors is used to create a more compact design with reasonable aspect ratios for the individual capacitors. Each capacitor bank uses 7 VNCAPs, totaling almost 800 fF when combined. This results in a reactance of 80 Ω at 2.4 GHz, which is much lower than the resistance presented by the biasing resistors and the reactance of the NFET gate capacitances, making a good AC ground.

The drain current in both versions is 1.8 mA. Like the board-level design in Section 3.2, the drain current sets the transconductance, denoted as g_m, which effectively sets the input impedance of the common-gate amplifier as well as the unloaded gain. Equation (4.1) shows the equation for input impedance of a common-gate amplifier [14].

$$R_{in} = \frac{1}{g_m} \tag{4.1}$$

In both versions of the core amplifier, the g_m of each transistor is roughly 17 mA/V. Since the core amplifier consists of two cascading common-gate amplifiers, the overall input resistance of the amplifier is set by the input resistance of the first common-gate amplifier, made by the NFET denoted as T2 in Figures 4.1 and 4.2. By using Equation (4.1), the R_{in} of the transistor T2 is estimated to be about 60 Ω in both versions. As version 3 is biased by a source resistor, shown as R0 in Figure 4.2, the overall input impedance of the amplifier will be brought

down to 50 Ω. Knowing the input impedance of the amplifier is important for the design of the L-matching network described in Section 4.1.3.

While both version 2 and version 3 of the core amplifier are biased and perform almost identically, they differ in one crucial area: noise figure. As will be discussed in Section 4.2.2, the noise figure of an LNA is extremely important, as it is normally one of the first devices received signals encounter. The LNA effectively sets the noise figure for the system, impacting the signal-to-noise ratio (SNR). Because there is a desire to minimize the noise figure of the LNA, version 3 of the core amplifier was selected to be used in the final design. The decision to use version 3 is discussed in depth in Section 4.2.2, as it also drove feedback network topology changes. The final layout of version 3 of the core amplifier is shown in Figure 4.3.

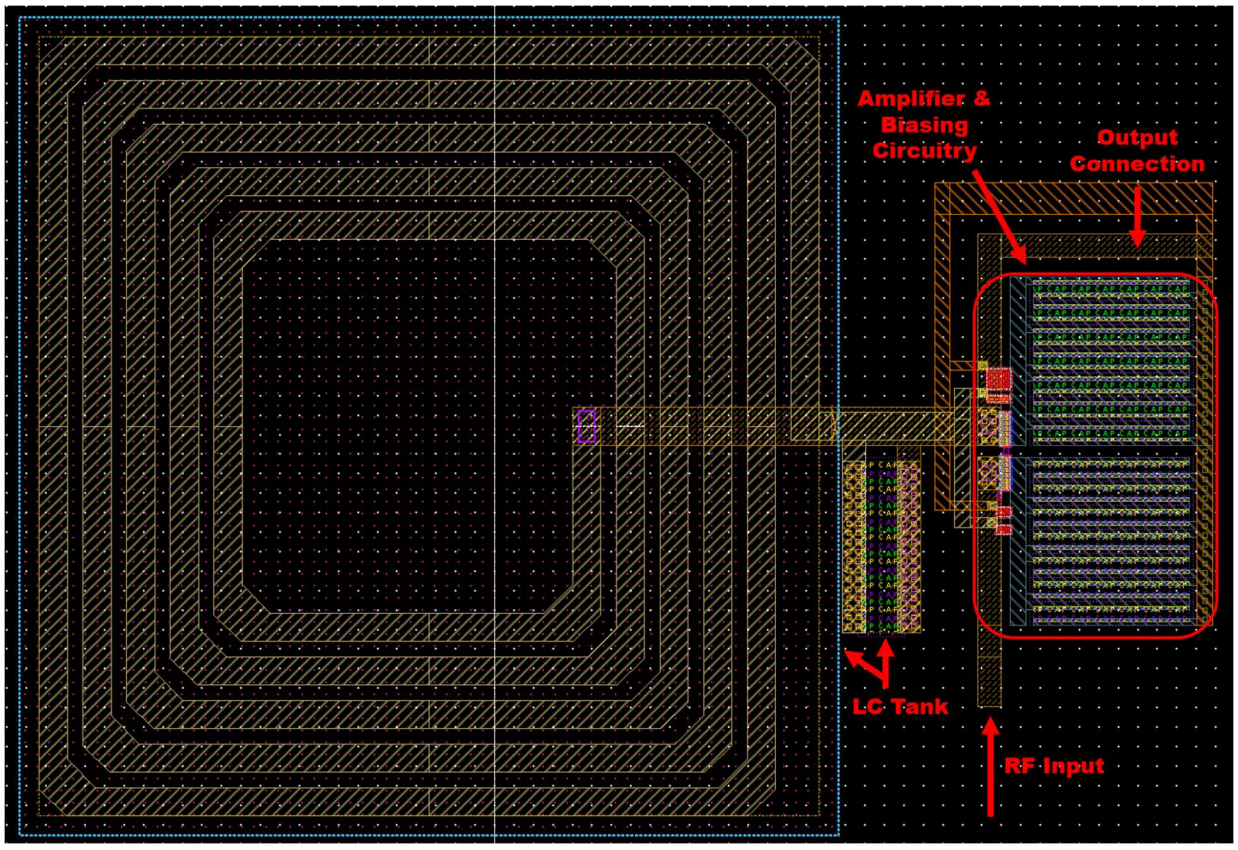

Figure 4.3. CMOS Core amplifier version 3 layout.

4.1.2 – CMOS Buffer Design

The design of the on-chip buffers is nearly identical to the BJT buffers designed in Section 3.2.2, although the output and feedback buffer use the same base cell in this design. The gates of each buffer are biased to 1.0 V by independent voltage dividers and use current mirrors to set a 1.8 mA drain current. Figure 4.4 shows the buffer schematic, while Figure 4.5 shows the buffer layout.

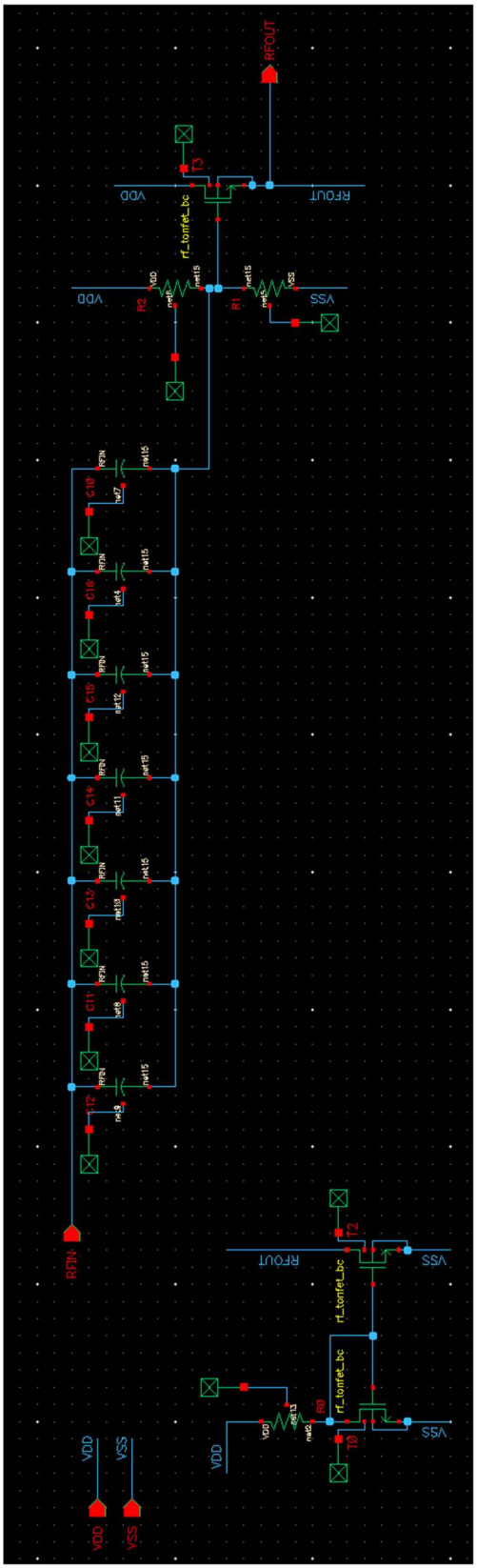

Figure 4.4. Chip level buffer schematic.

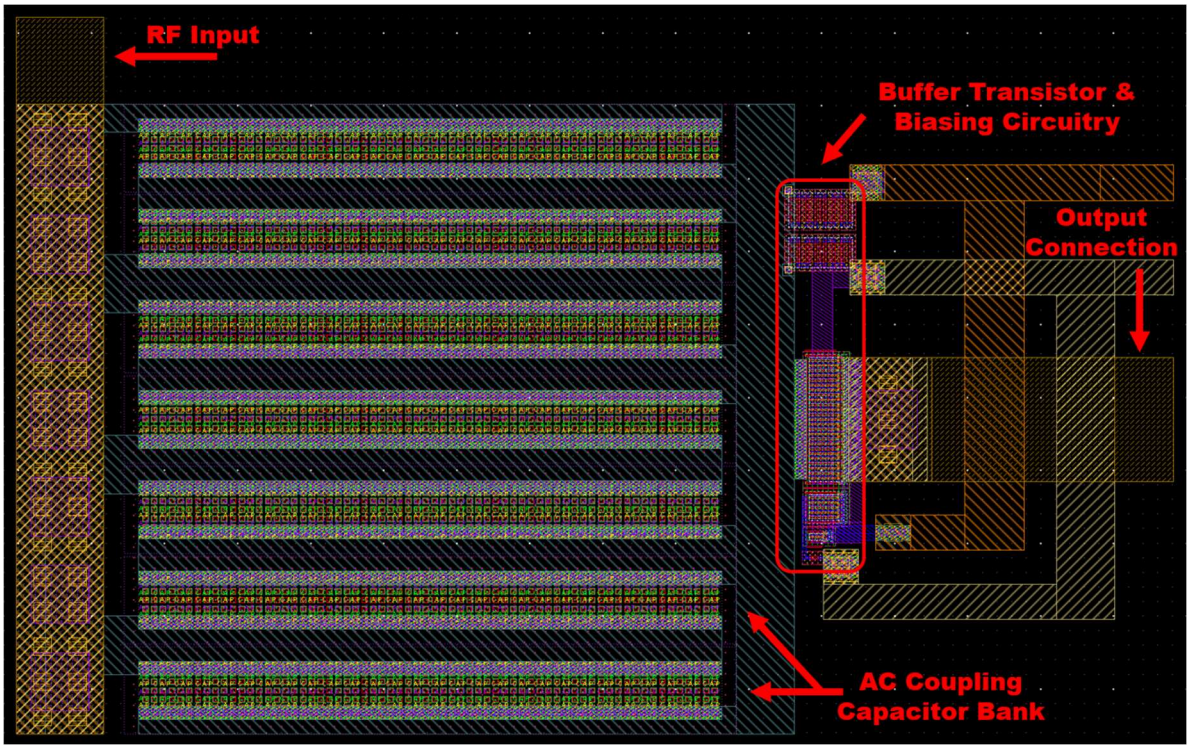

Figure 4.5. CMOS buffer layout.

In Figure 4.4, the capacitor bank made up by C10 through C16 acts as an AC coupling capacitor to the output of the core amplifier designed in Section 4.1.1. This capacitor bank is exactly the same as the decoupling capacitor bank on the gates of the core amplifier, totaling 800 fF with a reactance of 80 Ω at 2.4 GHz. While the output buffer nominally has unity gain there is an additional series resistor, shown as the series resistor at the RFOUT port in Figures 4.9 and 4.16, at the system output to increase the compression point, while adding some signal attenuation. The feedback buffer also has a series resistor at its output, although its design and use are dictated by the feedback network topology. Because of this, it is safe to assume that the feedback buffer provides unity gain, with all signal attenuation being controlled by the feedback network, which is discussed in depth in Section 4.2.

4.1.3 – Off Chip L Matching Network

An off-chip L matching network is used to provide additional attenuation to out-of-band and off-channel signals as described in Section 2.2.3 and Section 3.2.3. The L matching network was designed to match 50 Ω up to 560 Ω at 2.45 GHz creating an artificial voltage divider with the input impedance of the core amplifier, resulting in 10 dB or more of additional attenuation. Figure 4.6 depicts the designed L matching network.

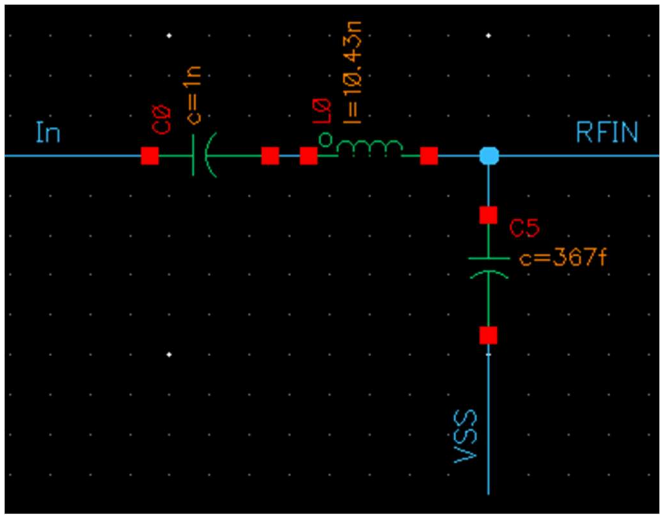

Figure 4.6. Chip level L matching network.

It should be noted that all the components in Figure 4.6 are ideal simulation components, and do not account for real life parasitics. The matching network is formed by L0 and C5, while C0 is used purely as a DC block. While the matching network could be implemented on-chip, it was not done so in this work due to size constraints, as on-chip inductors can consume a significant amount of space, although careful sizing of a bondwire or PCB trace could provide the necessary inductance for the matching network. It's important to note that the addition of the L matching network will effectively lower the input resistance of the core amplifier from the perspective of the feedback network. In both version 2 and version 3 of the core amplifier, the input impedance seen by the feedback network drops by about 6 Ω, to 54 Ω and 44 Ω

respectively. This is important to mention here, as these new input impedances are used in the design of the feedback networks discussed in Section 4.2.

4.2 – Feedback Network Design

The design of the feedback network proved to be a significant challenge, taking several iterations to get it right. The original feedback network design is discussed in depth in Section 4.2.1, while Section 4.2.2 provides a deep discussion into the design changes driven by the need to reduce the noise figure of the second version of the Q-enhanced LNA, as briefly discussed in Section 4.1.1. The final section, Section 4.2.3, showcases the final feedback network design.

4.2.1 – Shunt Attenuator Topology

The original feedback network topology was designed to be used with the second version of the core amplifier and uses a series resistor of 195 Ω with sets of shunt resistors that can be switched in to create varying voltage divider radios, increasing attenuation from a minimum of 13.26 dB. The minimum attenuation is set by the voltage divider made by the 195 Ω series resistor, and the roughly 54 Ω core amplifier input impedance seen by the feedback network. Figure 4.7 shows the basic block diagram of the feedback network.

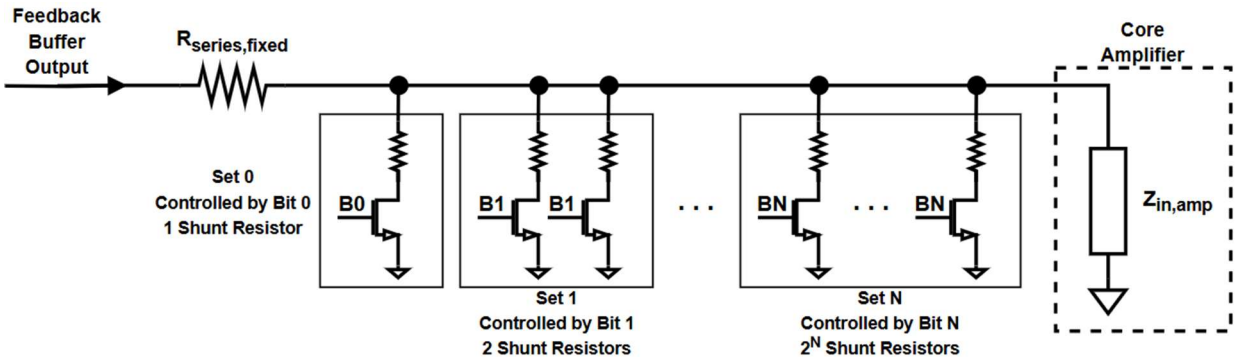

Figure 4.7. Shunt attenuator feedback network block diagram.

Each set of shunt resistors is controlled by a bit of programmable register, and in total there are 8 sets of shunt resistors that can be switched in by programming binary attenuation codes to the register. A bit being logic high in the programmable register switches in 2^n copies of the 3775 Ω base cell, where n is the bit with a logic high. For example, programming attenuation code 4 results in bit 2 being high, switching in 4 copies of the base cell. This allows for anywhere between 0 to 255 copies of the base cell to be switched in at any given time, increasing attenuation from 13.26 dB to a maximum of 25 dB of attenuation. Figure 4.8 depicts the schematic of base shunt attenuator cell.

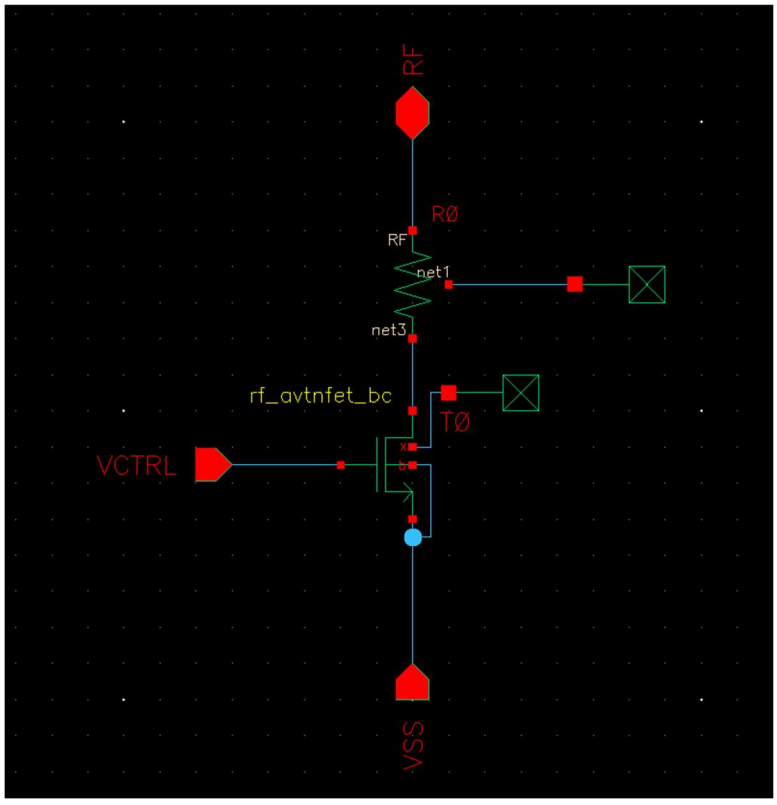

Figure 4.8. Shunt attenuator base cell schematic.

The design of the base cell depicted in Figure 4.8 was based upon the "simplified-T" attenuator shown in [2][6]. By switching in a 3775 Ω resistor to ground, a 0.1 dB attenuation is

applied, but only in a 50 Ω environment. This is not a 50 Ω environment however, and by switching in a single copy of this base cell the attenuation increases from 13.26 dB to 13.36 dB. By switching in another copy of the base cell, attenuation increases to 13.45 dB. As more copies of the base cell are switched in, the attenuation continues to rise reaching a maximum of 25 dB. It is important to note that the attenuation step size is non-linear, with higher codes having finer step sizes than lower codes. Figure 4.9 shows the full Q-enhanced LNA, using the second version of the core amplifier, two of the buffers designed in Section 4.1.2, and the shunt attenuator network discussed here.

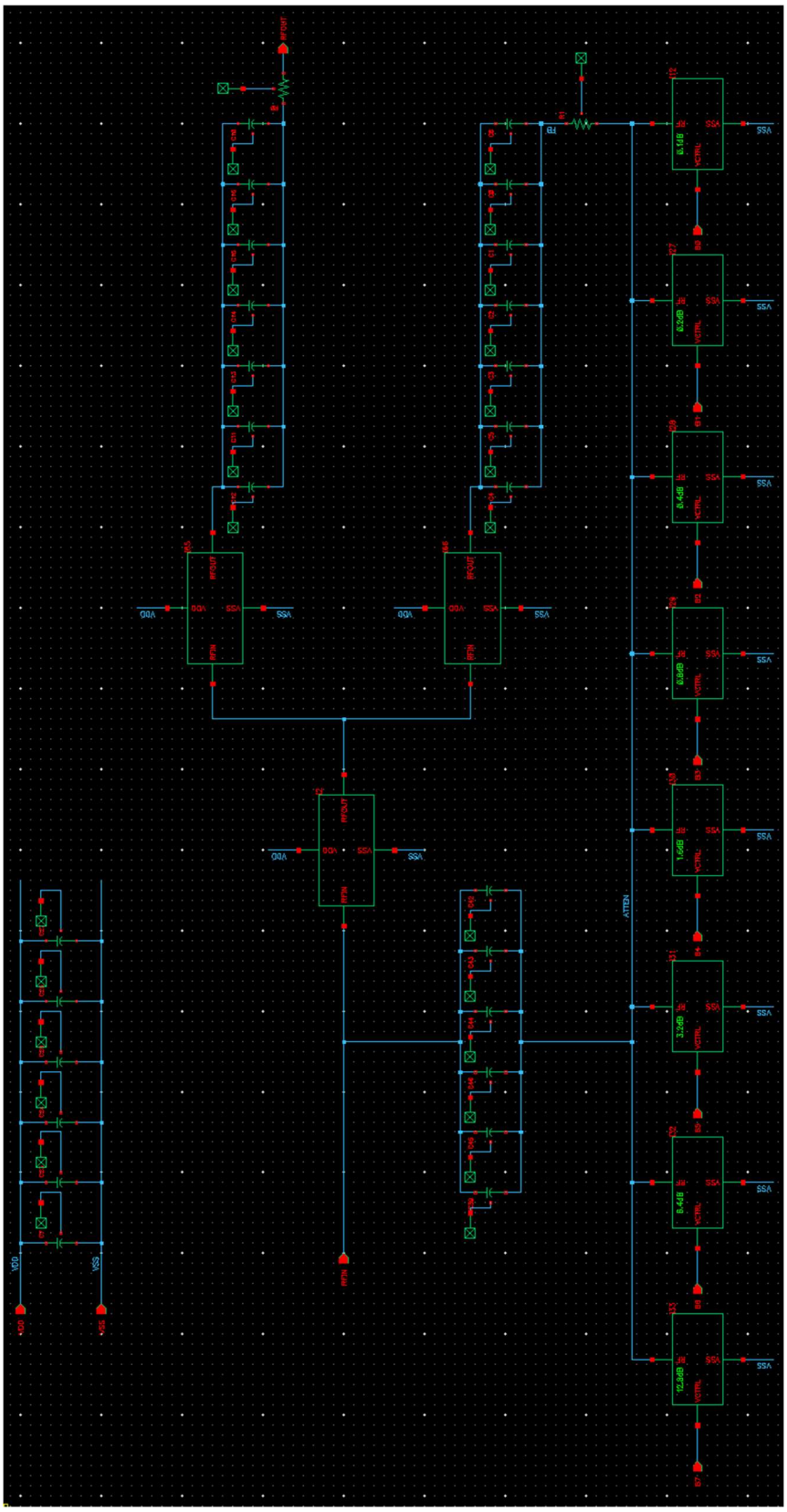

Figure 4.9. Q-Enhanced LNA schematic with shunt attenuator feedback topology.

Note the addition of DC blocking capacitors at the outputs of the buffers, and between the core amplifier input and output of the feedback network. Blocking the DC connection between the core amplifier input and output of the feedback network is necessary, as a direct connection could cause the drain current bias to change. The design shown in Figure 4.9 was able to reach the desired bandwidth of 20 MHz at 2.4 GHz, and Figure 4.10 shows the AC sweep results when using an attenuation code 138. That is to say that the feedback network attenuation is 21.4 dB, as 138 copies of the base cell in Figure 4.8 are switched in.

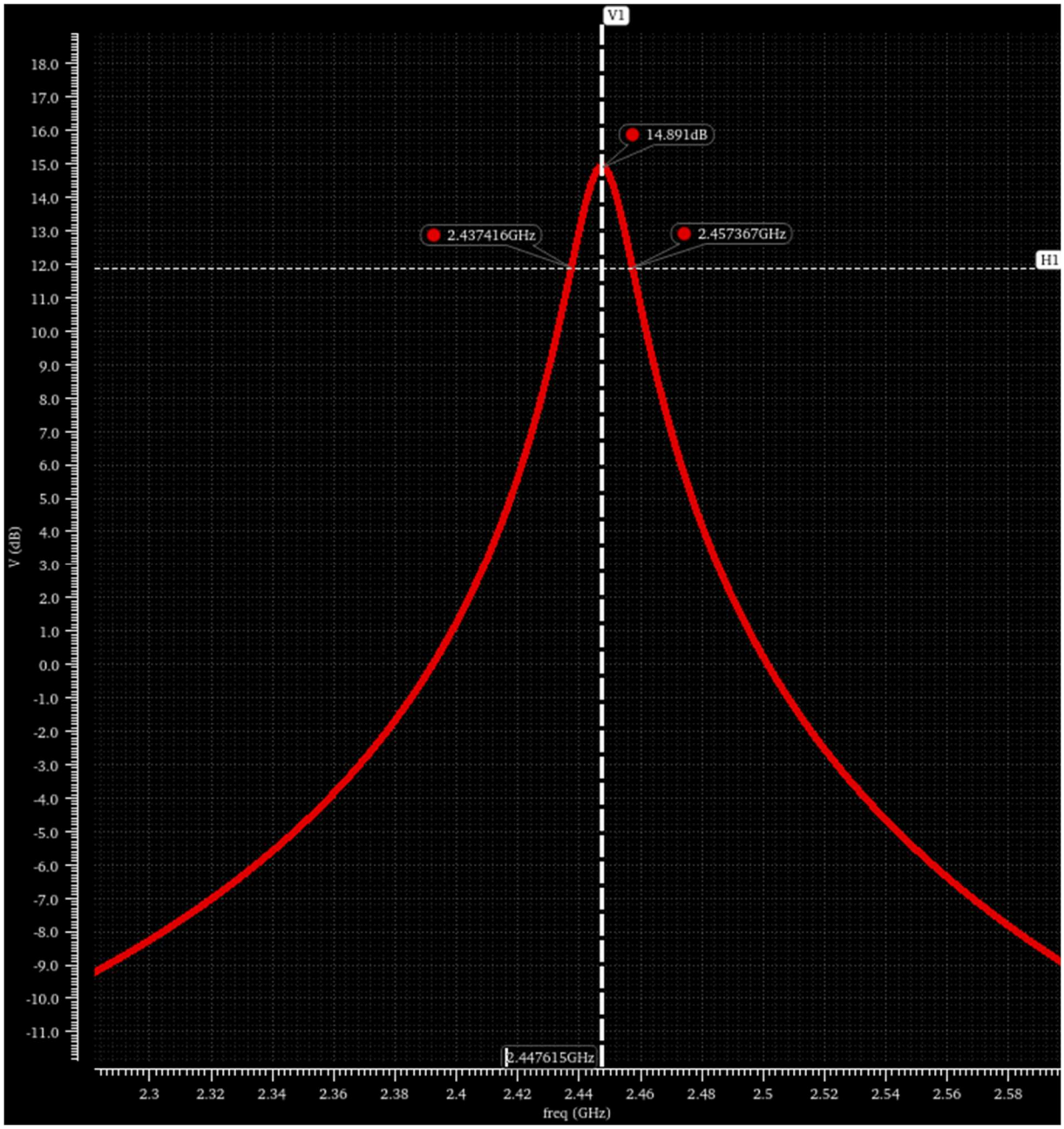

Figure 4.10. AC Sweep of Q-enhanced LNA with shunt attenuator feedback network.

At a code of 138, the gain is 14.9 dB, and the bandwidth is 19.9 MHz. At a center frequency of roughly 2.45 GHz, the Q of the system has been enhanced to 120. The system is also capable of achieving other bandwidths and gains, as the attenuation code can range from 0 to 255. At code 115 the amplifier starts oscillating, with all codes below code 115 producing an

oscillation. Attenuation codes above code 115 will result in varying gains and bandwidths, making it possible for this system to achieve a 40 MHz bandwidth at 2.4 GHz, which is also specified by 802.11ax. As mentioned and demonstrated in Chapters 2 and 3, this oscillation can be used for tuning the center frequency, so it is important for the first attenuation code that produces an oscillation to be roughly centered in the range of available codes. This ensures that the amplifier can oscillate and be tuned, even if process variation is large.

While the Q-enhanced LNA using the shunt attenuator feedback network topology would have likely sufficed, it suffered from a high noise figure. The design software allows for the simulation of noise alongside a traditional AC sweep, and by using the reported noise and gain, noise figure can be calculated. The system shown in Figure 4.9 has a 19.5 dB noise figure, making it largely unacceptable for practical use. To make the Q-enhanced LNA architecture practical, the noise figure had to be reduced. Section 4.2.2 discusses the importance and calculation of noise figure, as well as the changes brought on by the need to reduce the noise figure.

4.2.2 – Reduction of Noise Figure

As mentioned in Section 4.1.1, the noise figure of the LNA is extremely important, as it effectively sets the noise figure of the system, affecting the achievable SNR and ultimately the receiver's sensitivity. The Friis equation for noise shown in Equation (4.2) is normally taught in an undergraduate communication systems course and shows how the first gain element in the receiving chain sets noise figure [11].

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \tag{4.2}$$

In Equation (4.2) F_n denotes the linear noise figure for the n-th device, while the G_n terms denote the linear power gains of the n-th device. Division by linear power gain values in

the second and higher terms is responsible for the dominance of the LNA noise figure (F_1) on the overall receiver's noise performance.

At this point it is prudent to discuss how the noise figure of the system shown in Figure 4.9 was estimated, since it is the most crucial component in Equation (4.2). The design software used, Cadence, offers a noise simulation that can be run alongside a normal AC sweep. This provides both the gain, in V/V or dB, and noise, in $nV/\sqrt{Hz}$, at the center frequency of the amplifier. These quantities can be used to evaluate the noise figure, in dB, of the amplifier at various attenuation codes, as shown in Equation (4.3) [24]. The denominator represents the loaded noise from a 50 Ohm source times the linear voltage gain of the amplifier, while the numerator is the total noise at the output, including this noise and noise from all amplifier components.

$$NF_{dB} = 20\log_{10}\left(\frac{Virtuoso\ Reported\ Noise\ Figure\ in\ \frac{nV}{\sqrt{Hz}}}{(0.45\ nV/\sqrt{Hz}\ * 10^{(Virtuoso\ Reported\ Gain\ in\ dB\ /\ 20)})}\right) \quad (4.3)$$

Since both noise and gain are frequency dependent, the measurements used in Equation (4.3) must be at the same frequency. While Cadence offers tools that can provide a visible plot of noise across frequency, it can also provide a readout of noise at a given frequency, while also listing the top noise contributors at that frequency. Figure 4.11 shows this readout for the system pictured in Figure 4.9 at the center frequency of the filter. The total summarized noise, as well as the gain from Figure 4.10 can be used in Equation (4.3) to find the noise figure. As mentioned, the shunt attenuator topology, when combined with the second version of the core amplifier, results in a noise figure of 19.5 dB.

Device	Param	Noise Contribution	% Of Total
/I8/I2|T2	id	12.2955n	27.96
/I8/I2|T0	id	7.75464n	11.12
/I8/I2|T1	id	5.35428n	5.30
/I8/I2|T2	rgbi	4.31821n	3.45
/I8/I2|T2	rd	4.26878n	3.37
/I8/I2|T2	rbody	4.12127n	3.14
/I8/I2|T0	rbody	3.95107n	2.89
/I8/I2|L0/xind/rs3_leg	rn	3.66361n	2.48
/I8/I2|T2/rg	rn	3.63761n	2.45
/I8/I2|L0/xind/rs1_leg	rn	2.83749n	1.49

Spot Noise Summary (in V/sqrt(Hz)) at 2.45G Hz Sorted By Noise Contributors
Total Summarized Noise = 23.2514n
Total Input Referred Noise = 8.76586n
The above noise summary info is for noise data

Figure 4.11. Noise summary for Q-enhanced LNA with shunt attenuator topology.

It is apparent that the three largest contributors to noise are the channel thermal noise, denoted as id in Figure 4.11, of transistors T2, T0, and T1. Transistors T0 and T1 form the current mirror used to bias the drain current through the two-stage common-gate amplifier, while T2 is the transistor used for the first common-gate amplifier in Figure 4.1 and Figure 4.2. While it is impractical to remove T2 since it makes up the core amplifier, it is possible to remove the current mirror used to set the drain current.

As discussed in Section 4.1.1, another version of the core amplifier was designed, known as version 3, which uses a resistor to set the drain current through the core amplifier. Figure 4.2 in Section 4.1.1 shows version 3 of the core amplifier, where R0 is the biasing resistor setting the drain current to 1.8 mA. While the added resistor will add some thermal noise, the goal is that the thermal noise of the resistor is significantly lower than the channel thermal noise of the current mirror circuitry in version 2.

Unfortunately, at high attenuation codes the total parallel resistance of the shunt attenuators drops significantly, decreasing the value of the biasing resistor. This causes the drain

current to increase, increasing transconductance, which increases the gain of the core amplifier. Referring back to the feedback principles discussed in Section 2.1, an increase in the gain A of the core amplifier increases the loop gain, which decreases the feedback factor when using positive feedback. In turn, gain and selectivity increase even higher than originally designed for as shown in Equations (2.7) and (2.11). So, to maintain constant gain and bandwidth, the attenuation provided by the feedback network must increase to counteract the changing gain of the core amplifier.

Since it is not wise to have bias current be a function of attenuation code, and since this problem is not easily solved, a different attenuator topology was designed to be used with version 3 of the core amplifier. The new topology, discussed in Section 4.2.3, uses a variable series resistance in the feedback network to create a variable voltage divider with the input impedance of the core amplifier.

4.2.3 – Series Attenuator Topology

The series attenuator topology removes the 195 Ω series resistor used by the shunt attenuator topology and replaces the sets of switched shunt resistors with sets of switched series resistors between the output of the feedback buffer and the input of the core amplifier. To effectively design the series attenuator topology, it is important to know what the load impedance is from the perspective of the feedback network. The load impedance is the parallel combination of the impedance seen looking into the matching network from the core amplifier input, the input impedance of the amplifier, and the drain current biasing resistor. The parallel combination of these elements results in almost 44 Ω seen by the feedback network. Figure 4.12 shows a block diagram of the series attenuator topology.

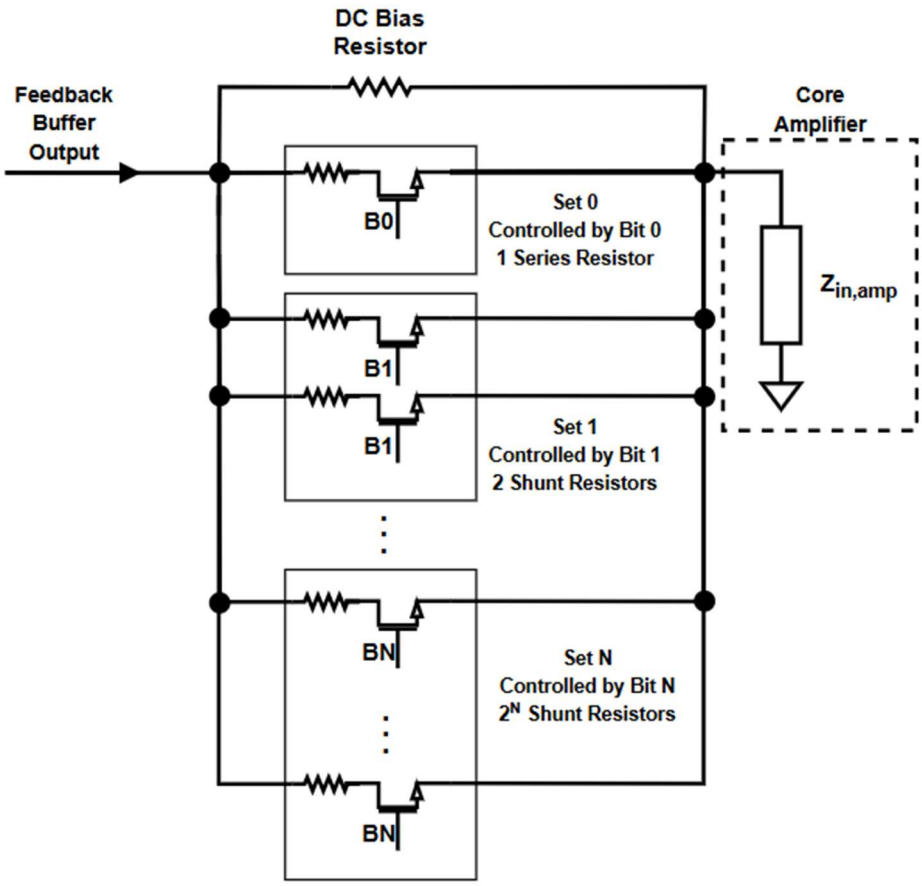

Figure 4.12. Series attenuator feedback network block diagram.

Unlike the shunt attenuator topology that used a voltage divider with a fixed series resistor and controllable load resistance, the series attenuator topology has a fixed load resistor and a controllable series resistance. Figure 4.13 shows the programmable series attenuator, while Figure 4.14 shows the layout of the feedback network.

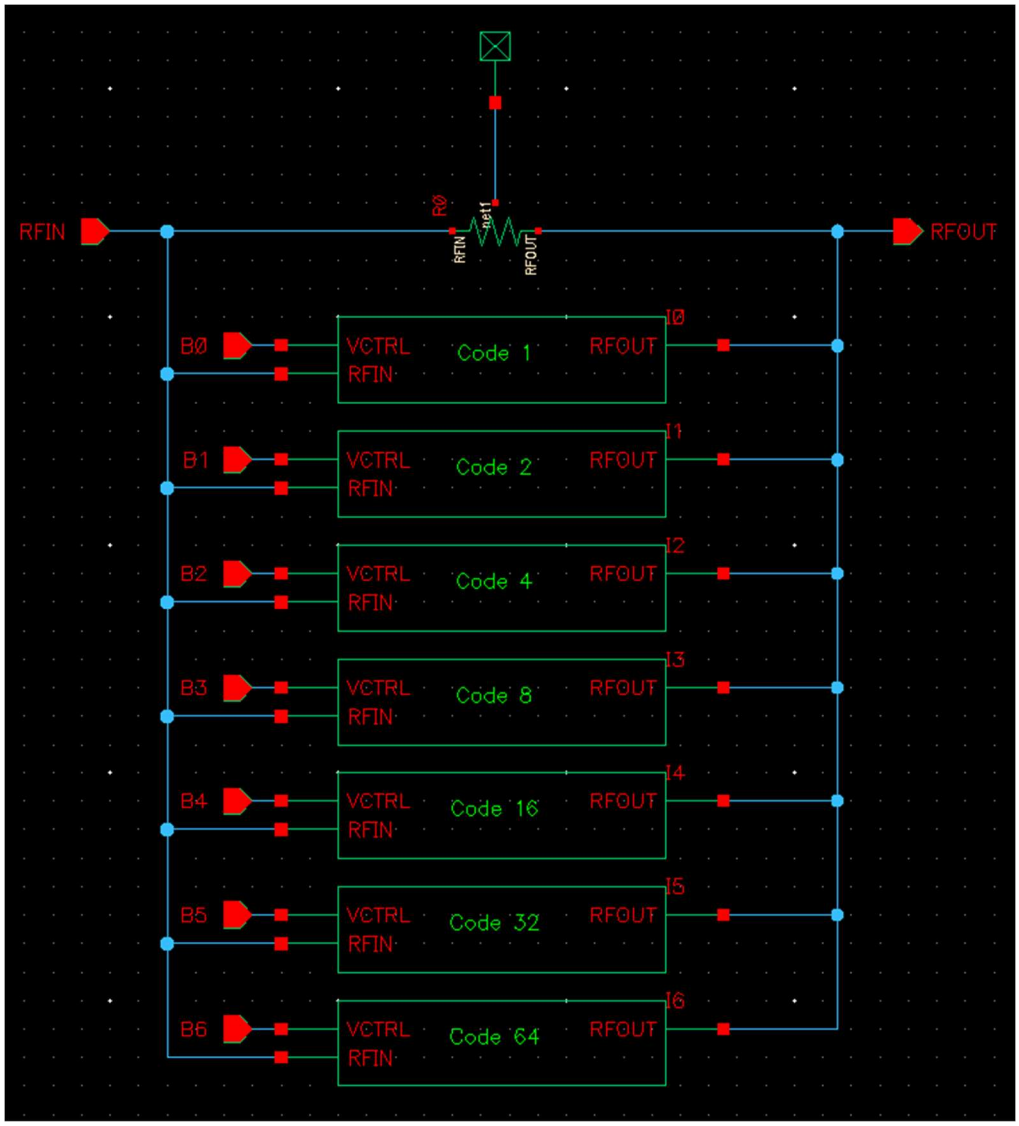

Figure 4.13. Programmable series attenuator schematic.

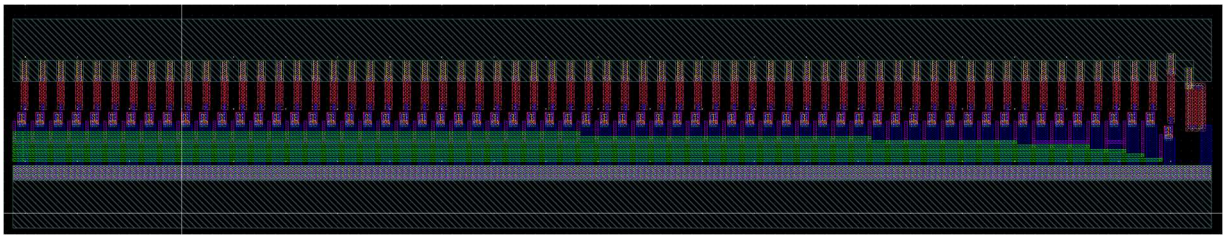

Figure 4.14. Shunt attenuator feedback network layout.

The design depicted in Figure 4.13 uses a 100 kΩ series resistor, R0, to DC bias both sides of the transistors used to switch in additional series resistors. The DC bias is provided by

the output of the feedback buffer and requires the DC block capacitors at the buffer output, shown as C0 through C6 in Figure 4.9, to be removed. The DC block capacitors between the output of the feedback network and the input of the core amplifier, shown as C39 and C42 through C46 in Figures 4.9 and 4.16, should remain to prevent the DC bias at the core amplifier input from changing. The blocks in Figure 4.13 denoted I0 through I6 are switched sets of series resistors, controlled by programming a 7-bit register. Each set switches in a given number of parallel series resistors to lower the effective series resistance, decreasing overall attenuation. Note, this behavior is the opposite to the shunt attenuator topology, where switching in more parallel resistors increased attenuation. This is why this design only uses 7-bits instead of 8-bits, as an additional bit would decrease attenuation even further, putting the core amplifier further into oscillation, which is not needed to be able to effectively tune the core amplifier.

Additionally, there is not a singular base cell that is replicated for each switchable set of resistors like there is in the shunt attenuator topology. The block denoted I0 is composed of its own series resistor and switch. Block I1 also contains a singular series resistor and switch, although the value of the series resistor is smaller than that used in block I0. Blocks I2 through I6 contain 2^{n-1} parallel duplicates of the resistor and switch used in block I1, where n is the bit responsible for switching on that attenuator set. Effectively, block I0 uses its own base cell, while blocks I1 through I6 share the same base cell. This was done to minimize the size of the finished design. Figure 4.15 shows the base cell schematic structure for all the switchable sets.

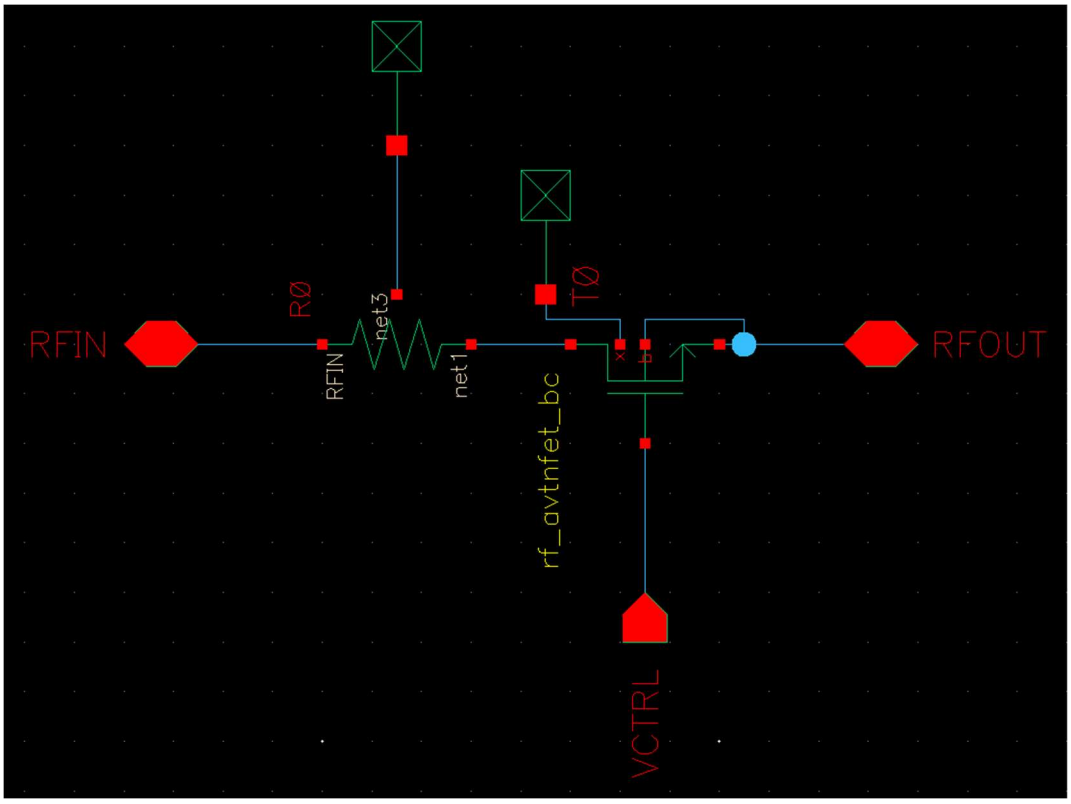

Figure 4.15. Series attenuator base cell schematic structure.

To speed up the design process, the attenuation provided by the shunt feedback network at the point where the amplifier enters oscillation was used as a starting point. By knowing the attenuation at the point of oscillation, and the overall core amplifier input resistance, the needed series resistance of the voltage divider can be calculated. Block I0 uses a series resistance of 40 kΩ, while blocks I1 through I6 use a base cell series resistance of 20 kΩ, since that is half the resistance used in I0, as that would be the effective resistance by using a parallel combination of the resistors used by block I0.

This topology proved to be quite effective, as codes in the center of the programmable range have a much finer step size than those towards extreme, allowing for bandwidth to be controlled more precisely than the shunt attenuator design. As will be discussed in Section 4.3, the noise figure of the design was also significantly reduced.

4.3 – Full Q-Enhanced LNA Design

Having discussed the need to use version 3 of the core amplifier, and the design of a different feedback network topology, Figure 4.16 presents the final Q-enhanced LNA schematic which uses version 3 of the core amplifier, the buffers, and the series attenuator feedback network topology. Figure 4.17 shows the final layout of the complete LNA, which was submitted for fabrication.

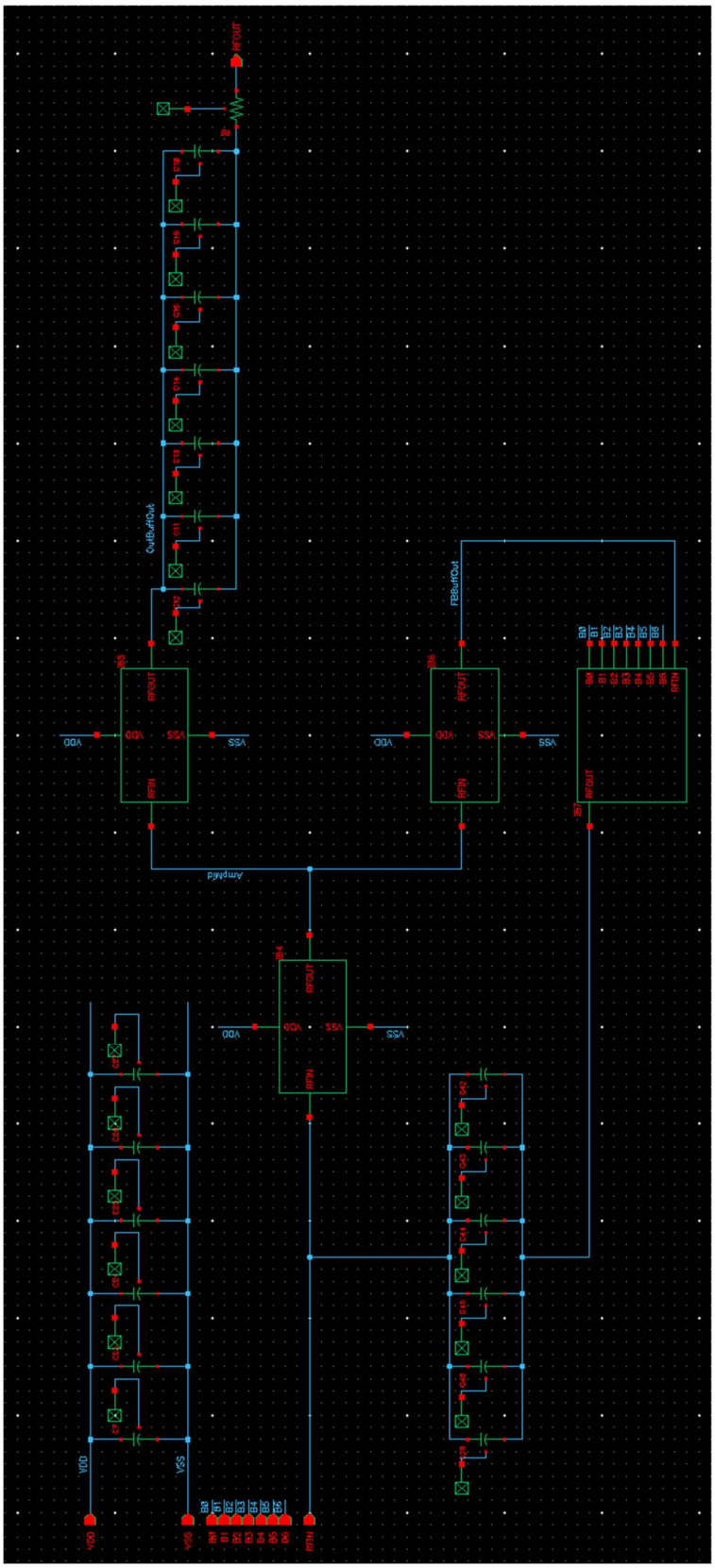

Figure 4.16. Final Q-enhanced LNA using series attenuator schematic.

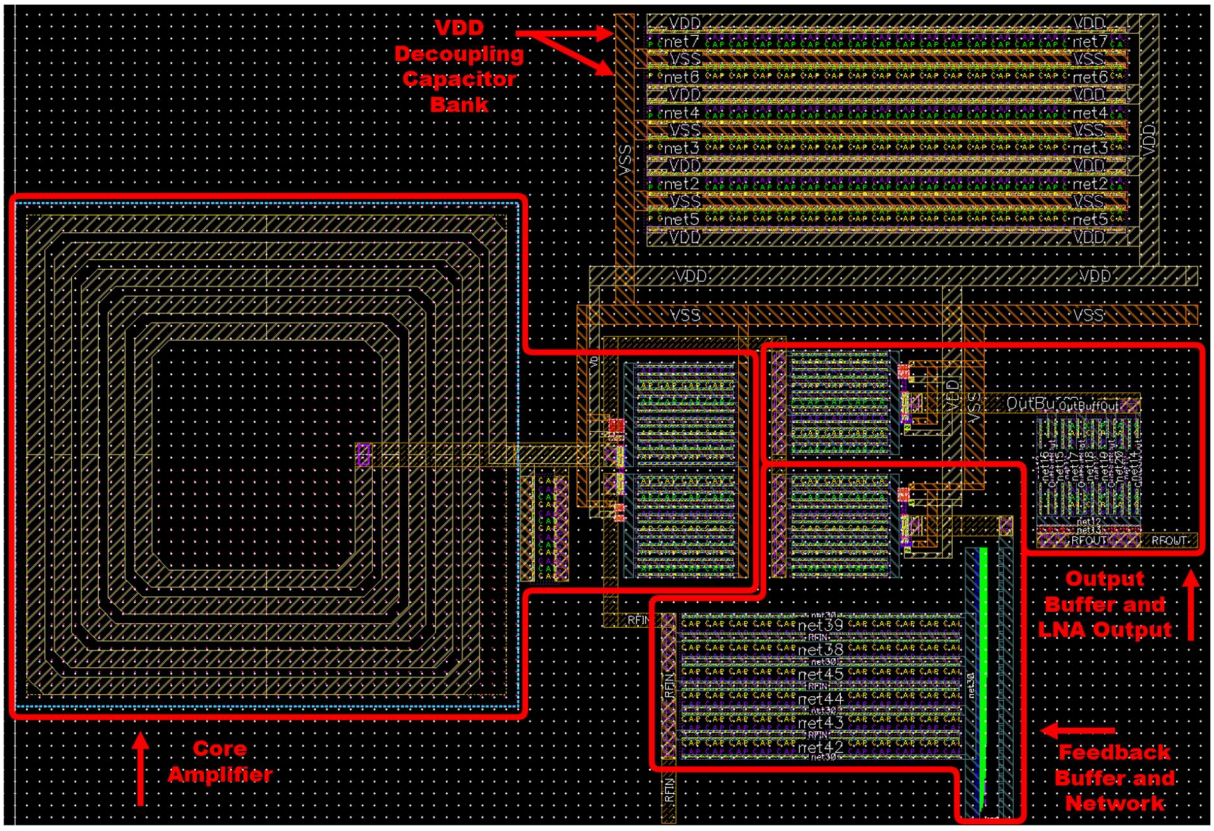

Figure 4.17. Final Q-enhanced LNA layout.

It is also important for this new design to achieve a 20 MHz bandwidth and have a lower noise figure than the system depicted in Figure 4.9. Figure 4.18 shows the AC sweep results, while Figure 4.19 shows the top noise contributors at a 20 MHz bandwidth.

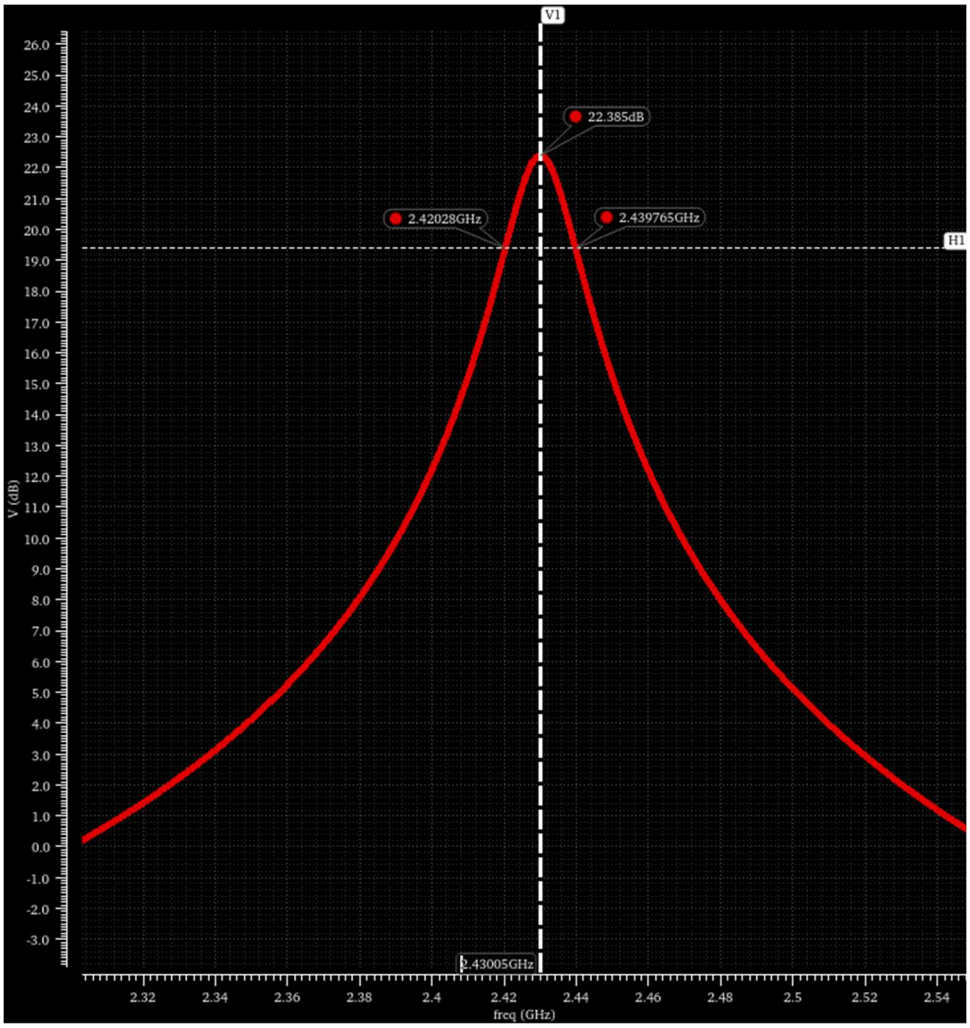

Figure 4.18. AC Sweep of Q-enhanced LNA with series attenuator feedback network.

Device	Param	Noise Contribution	% Of Total
/I6/I84|T2	id	6.04027n	14.69
/R2	rn	5.91156n	14.07
/I6/I84|R0/r2	thermal_noise	4.73063n	9.01
/I6/I84|R0/r4	thermal_noise	4.73063n	9.01
/I6/I84|R0/r3	thermal_noise	4.73063n	9.01
/I6/I84|L0/xind/rs3_leg	rn	3.8473n	5.96
/I6/I84|L0/xind/rs1_leg	rn	2.98912n	3.60
/I6/I84|L0/xind/rs2_leg	rn	2.82415n	3.21
/I6/I84|T2	rbody	2.1278n	1.82
/I6/I84|T2	rd	2.05666n	1.70

Spot Noise Summary (in V/sqrt(Hz)) at 2.43G Hz Sorted By Noise Contributors
Total Summarized Noise = 15.7612n
Total Input Referred Noise = 2.42722n
The above noise summary info is for noise data

Figure 4.19. Noise summary for Q-enhanced LNA with series attenuator topology.

Figure 4.18 shows a gain of 22.4 dB and a bandwidth of 19.5 MHz at 2.43 GHz, resulting in a Q of 125. Just like the shunt attenuator design seen in Figure 4.9, this design is also capable of achieving a 40 MHz bandwidth that is also used by 802.11ax. On the noise side, Figure 4.19 shows that the noise decreased significantly, and noise figure can be calculated by using Equation (4.3). The calculated noise figure comes out to be 8.5 dB, which is significantly lower than the 19.5 dB noise figure calculated for the shunt attenuator based design and is an acceptable value for a Q-enhanced LNA as this noise figure performance can be traded off against improvements in intermodulation product reduction performance [10].

4.3.1 – Use of External Components

As mentioned previously, the use of external components is currently required for the automated tuning of the Q-enhanced LNAs discussed in this work. It may be feasible, and should be desired, to add a logarithmic amplifier or frequency divider into the ideal chip design, as this will reduce the number of lines in the bill of materials (BOM) and likely reduce overall cost to successfully integrate this chip at the board level. An external microcontroller or FPGA will likely still need to be used, as software developers likely require full control over the tuning algorithm to meet their specifications. This is not a bad thing however, as most if not all modern systems already have some form of microcontroller or FPGA, allowing for easy integration of the Q-enhanced LNA chip.

4.4 – Simulation Results

The Cadence design software offers a wealth of different analyses that can be used to validate the successful performance of the Q-enhanced LNA design. While many different simulations using a variety of analyses were run during the design process, a small portion of

these results are presented to validate key points of operation. Figure 4.20 shows the testbench that was used to evaluate the Q-enhanced LNA design shown in Figure 4.16.

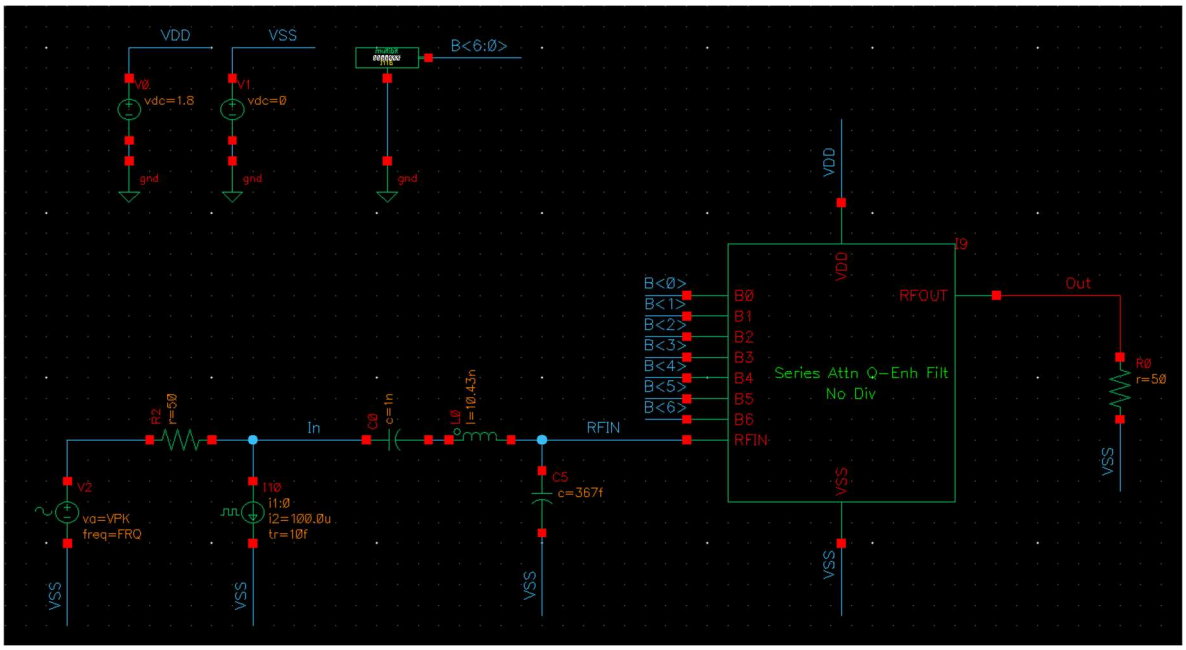

Figure 4.20. Q-Enhanced LNA test bench schematic.

Firstly, it is important to note the DC electrical characteristics of the design, which draws a mere 5.8 mA from a 1.8 V supply, for a total power consumption of less than 11 mW. Although this power consumption does not account for the power draw of a switched capacitor bank that will be added in the future, it illustrates that this LNA architecture is practical for use in low-power applications.

For tuning, a crucial property of the LNA design shown in Figure 4.16 is its ability to oscillate. By injecting a quick current pulse into the core amplifier input, a transient analysis can be used to determine if the amplifier is oscillating. This is used to verify that the point of oscillation occurs in the middle of the attenuation code range. Figures 4.21, 4.22, and 4.23 show the transient response of the amplifier output from an injected current pulse below, at, and above the point of oscillation respectively.

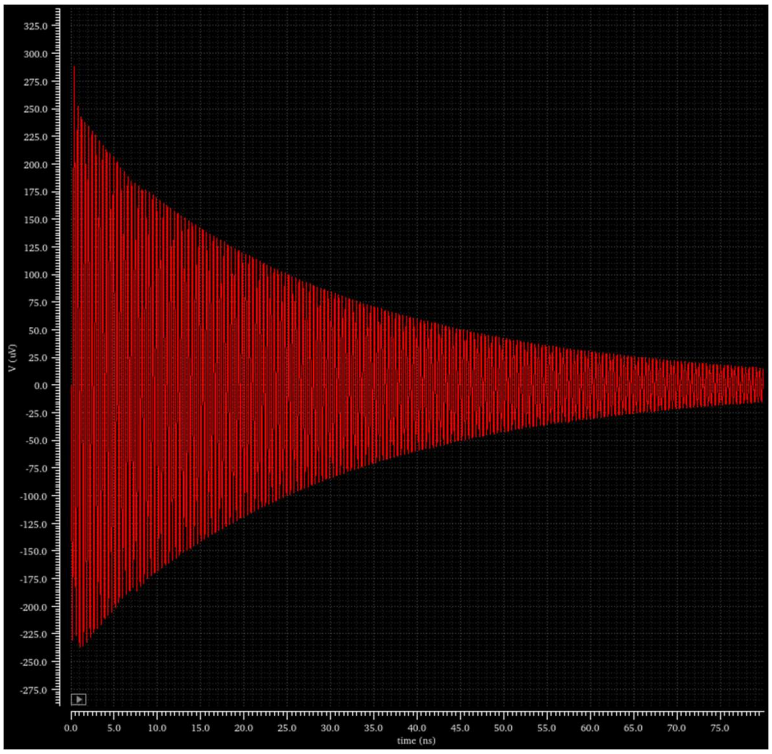

Figure 4.21. Injected current pulse transient response, code 60, not oscillating, -24.18 dB attenuation from feedback network.

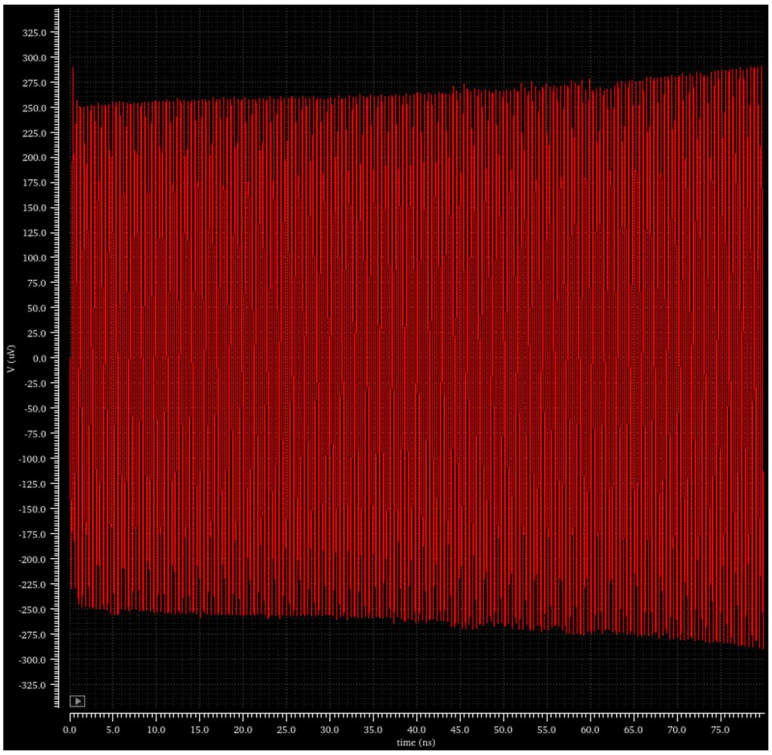

Figure 4.22. Injected current pulse transient response, code 68, point-of-oscillation, -23.17 dB attenuation from feedback network.

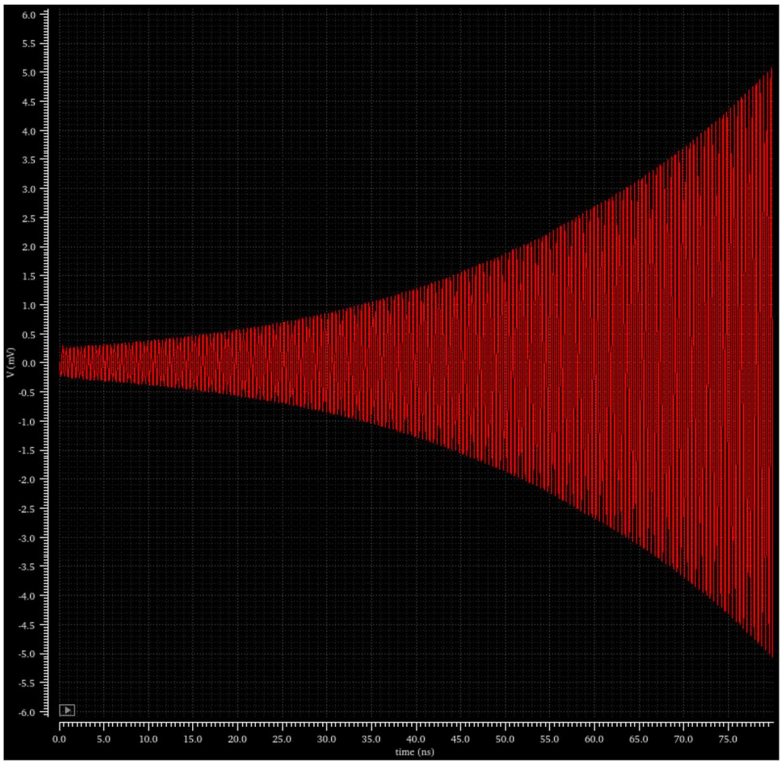

Figure 4.23. Injected current pulse transient response, code 70, oscillating, -22.94 dB attenuation from feedback network.

Figures 4.21 through 4.23 verify that the designed Q-enhanced LNA can enter and exit oscillation, and that the point-of-oscillation is reasonably close to the center of programmable codes, and hence attenuation range. Having margin on both sides of the point-of-oscillation is crucial to ensure it can successfully enter and exit oscillation if the manufacturing process or process variation changes the desired point-of-oscillation.

Having verified that the designed Q-enhanced LNA is capable of oscillating, and that the feedback network provides sufficient controllable attenuation to enter and exit oscillation, it should be confirmed that the Q-enhanced LNA can achieve the desired bandwidths. As briefly mentioned at the start of Chapter 4, and defined in [12], the necessary bandwidths for 802.11ax at 2.4 GHz are 20 MHz and 40 MHz. Furthermore, it is not necessary to simulate the generation of intermodulation products or issues caused by large off-channel interferers, as the system in

Chapter 3 validates that a Q-enhanced LNA architecture can mitigate these issues. Through experimentation in simulation, the point at which a 20 MHz and 40 MHz bandwidth are achieved can be found, as well as their respective attenuation codes. Figures 4.24 and 4.25 show the gain, bandwidth, and center frequency for the desired 20 MHz and 40 MHz bandwidths, achieved at codes 57 and 45 respectively.

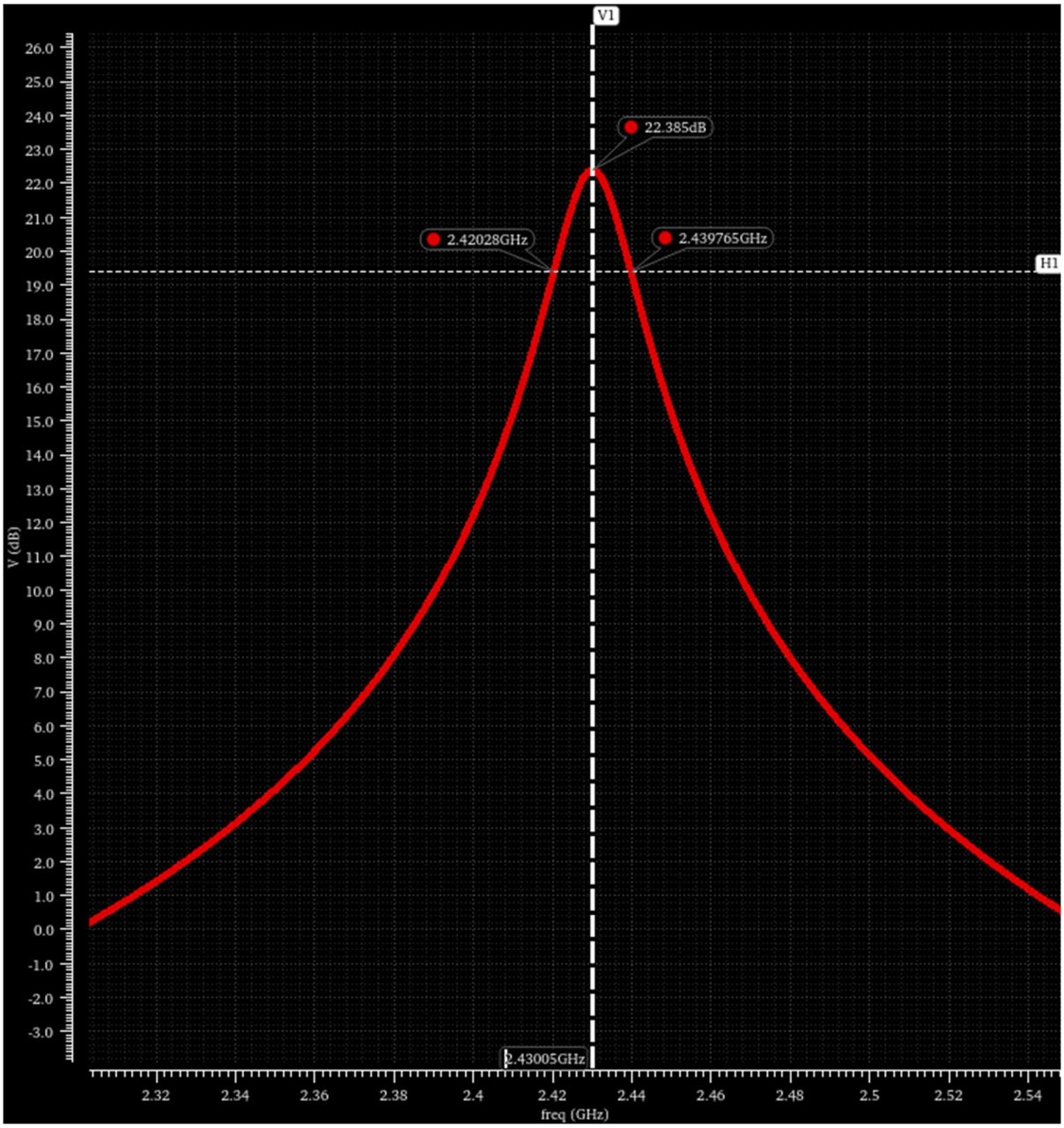

Figure 4.24. Q-Enhanced LNA 20 MHz bandwidth at code 57 verification.

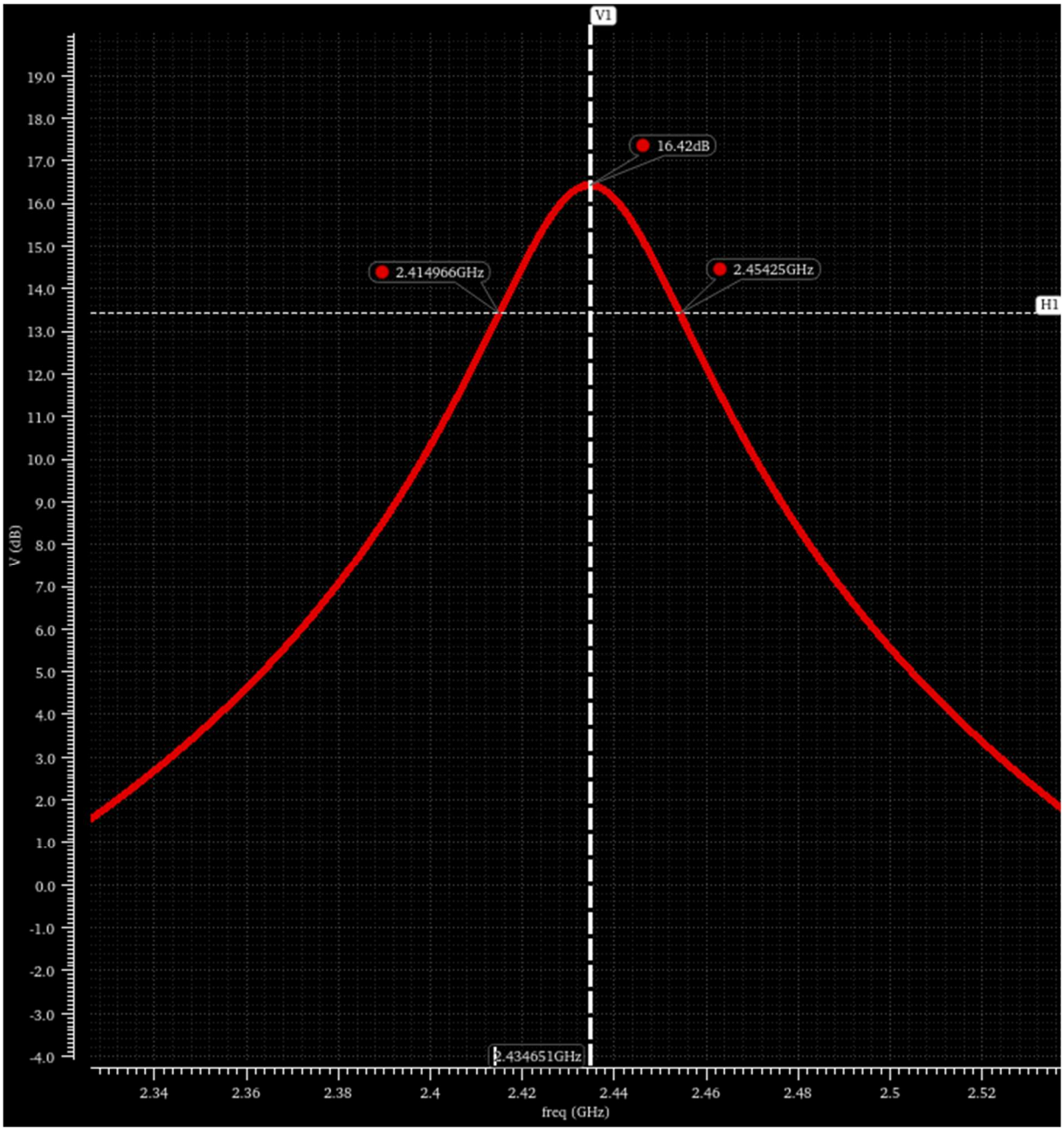

Figure 4.25. Q-Enhanced LNA 40 MHz bandwidth at code 45 verification.

One other important metric is the compression point of the core amplifier and the buffers. Compression point can be estimated by using a sinusoidal source in a transient simulation. By measuring the peak-to-peak voltage of the sinusoid at the inputs and outputs of the core amplifier and buffers, gain through each block can be estimated. Furthermore, the 1 dB compression point

can be estimated by increasing the peak-to-peak voltage of the sinusoid until the calculated gain through a given block decreases by 1 dB from the expected gain. It is easiest to present the estimated compression point in terms of the signal power at the input of the amplifiers in a 50 Ω system when the output compresses. This is known as input-referred 1 dB compression point, or P1dB. The results for signals at the center frequency are presented in Table 4.1, while Table 4.2 presents the input-referred compression point for signals that are 100 MHz off channel.

Device	Signal Amplitude at Compression	Power in 50 Ω
Core Amplifier	45.25 mVrms	-13.876 dBm
Output Buffer	189.64 mVrms	-1.43 dBm
Feedback Buffer	335.48 mVrms	3.524 dBm

Table 4.1. Estimate of center frequency compression point of Q-enhanced CMOS LNA.

Device	Signal Amplitude at Compression	Power in 50 Ω
Core Amplifier	181.02 mVrms	-1.835 dBm
Output Buffer	178.26 mVrms	-1.968 dBm
Feedback Buffer	374.06 mVrms	4.469 dBm

Table 4.2. Estimate of off-channel compression point of Q-enhanced CMOS LNA.

The input-referred 1 dB compression point of each block, specifically the core amplifier, can be improved by increasing the bias current through the core amplifier, although this may drive changes to the feedback network to increase attenuation. That being said, the results presented here confirm that the Q-enhanced LNA can achieve the desired bandwidths and is able to enter and exit oscillation for tuning. Additionally, the input-referred 1 dB compression point should suffice for real world applications, although it could be improved in future iterations. With successful simulations to verify the desired properties, it is safe to say that this design

should also work, as the real-world results in Section 3.5 suggest that at a fundamental level an ultra-narrowband LNA is capable of mitigating or preventing the issues discussed in Section 1.1.

Chapter 5 - Conclusion

As the radio spectrum becomes increasingly dense, it is becoming more crucial for receivers to maintain a high level of performance in the presence of large neighboring signals. Many receiver architectures are still susceptible to large in-band signals compressing the LNA, and to the generation of intermodulation products. Regenerative receivers of the past provide a great launch pad for the design of a new receiver architecture that mitigates these issues. Additionally, it is much more practical to tune a regenerative receiver in a modern-day system, as a basic tuning algorithm can be developed and deployed on a cheap microcontroller.

In this work, it was shown how the use of an ultra-narrowband Q-enhanced LNA architecture can successfully mitigate both the blocking and intermodulation product issues, implemented both at the board and chip level. It also shows the practicality of tuning a Q-enhanced LNA, with the use of an auto-tuning algorithm that was developed and successfully deployed at the board level. While the architecture shown in this work does have a higher noise figure than that of a traditional LNA, it may not be that significant as the noise floor in modern-day environments is quite high [10]. This makes the receiver architecture presented in this work a reasonable and practical choice for receivers operating in dense spectrums.

5.1 – Results

Chapter 3 showed the ability to implement an entire Q-enhanced system at the board level that could achieve a front-end bandwidth of 200 kHz for FM radio while providing significant gain. The complete system was able to successfully auto-tune to a desired frequency and could mitigate the impact of large signal interferers and intermodulation products. Figures 3.18 and 3.19 show spectrum plots before and after achieving channel bandwidth by enhancing Q to 500, showing that low-power signals can be received effectively.

Chapter 4 showed the ability to successfully implement the beginnings of a complete Q-enhanced system on chip at higher frequencies. An ultra-narrowband Q-enhanced LNA was successfully designed and simulated, capable of reaching a 20 MHz bandwidth and providing significant gain at 2.4 GHz for 802.11ax, also known as Wi-Fi 6. Figure 4.24 verifies that the designed Q-enhanced LNA can achieve a 20 MHz bandwidth.

While the simulated results of the Wi-Fi Q-enhanced LNA in Chapter 4 could not be verified at the time of this writing, simulation results, combined with the full results from Chapter 3, suggest the on-chip design will be capable of mitigating the impact of large signal interferers, while suppressing the generation of undesirable intermodulation products.

5.2 – Future Work

While this work covered the design of a full system at the board level, and a Q-enhanced LNA at the chip level, there are still many opportunities for future work. Firstly, the tuning algorithm can be further developed to improve tuning consistency, increase tuning precision, and minimize the tuning time. Characterizing the impact of different hardcoded parameters in the tuning algorithm, as well as the shift of center frequency by switching in and out of oscillation, will allow the tuning algorithm to improve in the aforementioned areas. In a similar manner, the addition of a controllable attenuator or switch between the Q-enhanced LNA and the antenna is paramount to the practical use of this system, as unintentional radiation may interfere with FCC regulations and degrade the performance of other systems nearby.

Additionally, the design of the Q-enhanced LNA at the chip level, as discussed in Chapter 4, still has several areas of work. First and foremost, at the time of this writing, the physical chips have not been returned. Testing of the chips will allow for correlation between simulation and reality and provide some insight into how process variation impacts the final

product. The ability to tune the center frequency of the Q-enhanced LNA should also be implemented, by designing some form of switchable capacitance in the main LC tank, as well as adding a series attenuator at the input of the chip to suppress the oscillating signal during tuning. It may also be desirable to add a frequency divided output of the oscillation signal, as well as an output that provides some characterization of oscillation power. Doing so would effectively eliminate the use of external components, except for a microcontroller running the tuning algorithm.

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