ELECTRICAL CHARACTERISTICS OF GALLIUM NITRIDE AND SILICON BASED METAL-OXIDE-SEMICONDUCTOR (MOS) CAPACITORS

by

MD TASHFIN ZAYED HOSSAIN

B.S., Bangladesh University of Engineering & Technology, 2001
M.S., North Carolina A&T State University, 2009

AN ABSTRACT OF A DISSERTATION

submitted in partial fulfillment of the requirements for the degree

DOCTOR OF PHILOSOPHY

Department of Chemical Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2013

Abstract

The integration of high-κ dielectrics with silicon and III-V semiconductors is important due to the need for high speed and high power electronic devices. The purpose of this research was to find the best conditions for fabricating high-κ dielectrics (oxides) on GaN or Si. In particular, high-κ oxides can sustain the high breakdown electric field of GaN and utilize the excellent properties of GaN.

This research developed an understanding of how process conditions impact the properties of high-κ dielectric on Si and GaN. Thermal and plasma-assisted atomic layer deposition (ALD) was employed to deposit TiO_2 on Si and Al_2O_3 on polar (*c*-plane) GaN at optimized temperatures of 200°C and 280°C respectively. The semiconductor surface treatment before ALD and the deposition temperature have a strong impact on the dielectric's electrical properties, surface morphology, stoichiometry, and impurity concentration. Of several etches considered, cleaning the GaN with a piranha etch produced Al_2O_3/GaN MOS capacitors with the best electrical characteristics. The benefits of growing a native oxide of GaN by dry thermal oxidation before depositing the high-κ dielectric was also investigated; oxidizing at 850°C for 30 minutes resulted in the best dielectric-semiconductor interface quality. Interest in nonpolar (*m*-plane) GaN (due to its lack of strong polarization field) motivated an investigation into the temperature behavior of Al_2O_3/*m*-plane GaN MOS capacitors. Nonpolar GaN MOS capacitors exhibited a stable flatband voltage across the measured temperature range and demonstrated temperature-stable operation.

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Finally, my heartfelt gratitude to Almighty Allah, my parents, brother and my sincere appreciation to my wife and son Alvan.

Dedication

I dedicate this dissertation to my father Md. Mosharrof Hossain, mother Hamida Hossain, brother Md. Tanzin Riad Hossain, wife Mahfuza Lima, and son Alvan.

Chapter 1 - Introduction

1.1 Dissertation outline

Metal-oxide-semiconductor capacitor (MOSCAP) is the fundamental building block to constitute microprocessor. The efficiency and reliability of the microprocessor depends greatly on the process condition of the fabrication of each element of the MOSCAPs. The ultimate goal is to obtain minimum leakage current through the gate oxide and minimize the interface traps in insulator-semiconductor interface. Achievement of these goals is highly dependent on the technique used to fabricate the MOSCAPs. If the MOSCAPs are optimized during fabrication, the electrical characteristics would improve significantly and the microprocessors can perform effectively.

This research aims to find the best conditions to fabricate high-k dielectrics (oxides) on GaN or Si. GaN is a wide bandgap semiconductor with exceptional material properties that play a key role in power electronics. The Si/SiO_2 interface is the heart of the modern metal-oxide-semiconductor field effect transistors but as transistors are down scaled, SiO_2 as a gate dielectric causes several problems; a high leakage current, reduced drive current, reliability degradation and impurity penetration [1]. Therefore, finding an alternate gate dielectric is essential, and much research across the globe has been devoted to investigate alternative high-κ dielectrics in MOS transistors. The motivation of using high-κ dielectrics is to reduce the leakage current without any reduction in oxide capacitance. In this research, Al_2O_3 and TiO_2 were used as high-κ dielectrics and were deposited on GaN and Si, respectively, by atomic layer deposition, a technique chosen for its exceptional uniform oxide film control. But deposited high-κ dielectrics do not form low defect density interfaces with semiconductors as well as SiO_2 with Si; there are many defects at the interface on silicon and III-V nitride (or III-N) semiconductors. Using high-κ oxide shows the flatband voltage to shift from its ideal position in capacitance-voltage measurement due to the existence of uncompensated charge in the dielectric and on silicon substrate; high-κ oxide can alter the oxide thickness by creating an interfacial layer.

In this research, methods to improve the high-κ dielectric-semiconductor interface and minimize leakage current density were investigated. The research focuses on fabrication and

characterization of the MOSCAPs, the fundamental element of the integrated circuits. The hypothesis is that if the dielectric-semiconductor interface quality and leakage current density of the MOS capacitors can be improved, the advantages will definitely be seen at the output of the various transistor devices used in power electronics and memory technology.

The properties of the high-κ dielectric and its interface with the semiconductor were evaluated using electrical measurements, such as capacitance-voltage (C-V) and current-voltage (I-V) measurements. C-V measurements were taken to determine the flatband voltage, threshold voltage, fixed charges and dielectric-semiconductor interface trap charges. I-V measurements were done to obtain the leakage current density. This research explored dry thermal oxidation of GaN. Thermal oxidation of Ga_2O_3 on GaN is a cheaper and simple process. The high interface trap density and foreign contaminants observed with the deposited dielectrics on GaN can be minimized with thermal oxidation. The GaN surface treatment before atomic layer deposition of the dielectric plays a significant role in reducing device defects. Finding the best semiconductor surface treatment with least surface roughness and impurity concentration along the depth of the device was an essential part of this research. Therefore, one of the goals of this research was to connect the electrical performance attributes to the physical and chemical properties of the devices. The chemical properties of the deposited dielectric on semiconductor were characterized by x-ray photoelectron spectroscopy (XPS) and surface roughness of the deposited dielectric was characterized by atomic force microscopy (AFM).

The first chapter of this dissertation presents the technical background of this research. It discusses the fundamental knowledge required for a basic understanding of MOS capacitors. The electrical measurement technique and characterization of MOS capacitor by capacitance-voltage measurement were discussed. Since this research revolves around Al_2O_3 gate oxide on GaN and TiO_2 on Si, an explanation is provided about the motivation for the selection of the high-κ dielectrics and the semiconductor, GaN. An explanation is provided about selecting sapphire as a substrate for the growth of GaN. The non-ideal effects of the MOS capacitor and defects are discussed. This chapter concludes by reviewing the previous work on high-k gate oxides on GaN MOS devices.

The second chapter describes the influence deposition temperature has on the structure, composition and electrical properties of TiO_2/Si MOS capacitors. The extraordinarily high dielectric constant of TiO_2, its deposition by plasma atomic layer deposition, and what impact TiO_2 had on leakage current density motivated this study.

The third chapter examines the electrical properties of Al_2O_3 on GaN, as prepared by thermal atomic layer deposition. The factors examined included the wet chemical etching of the GaN, the deposition temperature. Cleaning of the semiconductor prior to oxide deposition is very critical to fabricate high performance semiconductor devices. This study was motivated by the findings of Nepal *et al*. [2] and further study was done to investigate the effect of semiconductor surface treatment on average density of oxide trapped charge and Al_2O_3/GaN interface trap density.

The fourth chapter describes a study of the dry thermal oxidation of GaN at different process conditions with the objective of finding the best process condition to obtain a very thin native oxide of GaN with the best electrical properties. The hypothesis is that the native thermal oxidation may result in a low interface trap density compared to deposited dielectric films, not native to the semiconductor.

In fifth chapter, an investigation was done on nonpolar (*m*-plane) GaN-based MOS capacitors with Al_2O_3 as the gate dielectric. The study was motivated by the advantages of the *m*-plane GaN (lack of polarization effect, normally off operation) transistors, including low power consumption and failsafe operation in the power electronics industry. GaN MOSFETs are capable of exceptional performance in high temperature electronics, but their performance is deteriorated if polar GaN orientations are used since spontaneous polarization charge causes an unwanted threshold voltage shift and eventually causes the device to fail. Therefore, in this study, MOS capacitors were fabricated both on *c*- and *m*-plane GaN to investigate the temperature behavior. The work of Matocha et al. [3] on SiO_2/GaN on polar and nonpolar GaN crystal planes motivated this study with Al_2O_3/GaN MOS capacitors.

1.2 Technical Background

The semiconductor industry has achieved phenomenal growth over the last few decades due to rapid advancements in device (transistor) integration technologies. Hundreds of millions of field-effect transistors (FETs) are found in modern microprocessors. The transistor was first proposed by J.E.Lilienfeld in 1928, but due to surface states (electron traps) at the interface between semiconductor and insulator, it was not possible to achieve success during that time [4]. A breakthrough was achieved in 1960 by D. Kahng, when he fabricated a field effect transistor that had low trap interface between Si and its native oxide, SiO_2 [5]. The first integrated circuit with two transistors was made by Jack Kilby in 1958 at Texas Instrument; today a 16GB flash memory chip consists of more than 4 billion transistors. Since the integrated circuit was first invented, the transistor count has increased by orders of magnitude (Table 1.1). The limitations of bipolar transistors (quiescent power dissipated when circuit is not switching) were rectified by the invention of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) in 1960s as it draws almost zero current when idle. Based on an observation of Gordon Moore [6], the co-founder of Intel in 1965, the number of transistors has doubled every 26 months by scaling down the size of the transistors and thus reducing the cost of a chip.

Table 1-1 Transistor count, frequency, and market growth in integrated circuits [7]

	1st generation	2nd generation	3rd generation	4th generation
Year	1985	1993	2004	2010
Transistor counts	10^5-10^6	10^6-10^7	10^8-10^9	10^9-10^{10}
Clock frequencies	10^7	10^8	10^9	10^9
Worldwide Market	$25B	$60B	$170B	$250B

The transistor can act as an amplifier or a digital switch and it can be turned on or off by applying a bias to the gate. The MOSFET consists of drain, source, gate and bulk (Figure.1.1). The source and drain are the two terminals of the switch, which are electrically connected or isolated by applying a bias to the gate. The gate bias controls the channel that is insulated from gate by a dielectric. In inverters, power transistors are used as a switch.

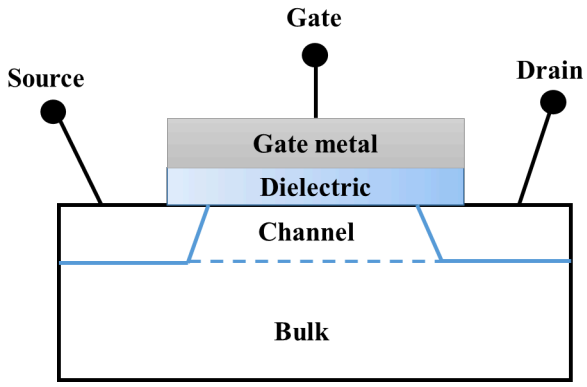


Figure 1.1 Si MOSFET

1.2.1 MOS capacitors and capacitance-voltage measurement

Hundreds of millions of field effect transistors (FETs) constitute modern microprocessor and the metal oxide semiconductor (MOS) capacitor is the central part of these transistors. MOS capacitors are the basis of digital logic circuits, random access memories (RAMs) and charge-coupled devices (CCDs). It operates using the field effect. MOS capacitors have two heterojunctions, a metal-dielectric and a dielectric-semiconductor. It is a transistor without source or drain, and it is formed when two conducting layers are isolated by a dielectric. The practical application of the MOS capacitor depends greatly on the quality of the dielectric-semiconductor interface. The metal contact of the MOS capacitor in a MOSFET is known as the gate and the dielectric as the gate oxide. Capacitance-voltage measurements are widely used to characterize MOS capacitors, to gain insights to improve of device performance. A C-V measurement is done to obtain interface trap density [8-12], oxide thickness [13-15], effective mobility [16-18] and substrate doping profile [19-21]. Compared to a parallel plate capacitor, the metal contact constitutes one plate with the dielectric and the majority carriers in the semiconductor constitute the other plate. In general, capacitance is the change in charge (integration of current over time) in a device with change in voltage, $C = \Delta Q/\Delta V$. Also, capacitance is expressed by $C=A\varepsilon_r\varepsilon_0/T_{ox}$ where A is the area of the capacitor, ε_r is the dielectric constant of the gate oxide, ε_0 is the permittivity in free space ($\varepsilon_0 = 8.854\times10^{-14}$ F/cm), and T_{ox} is the thickness of the gate oxide. As the capacitance of a dielectric is proportional to ε_r and inversely proportional to dielectric

thickness, a high gate dielectric capacitance is required to meet the drive current for proper operation in scaled semiconductor devices.

There are three characteristics region of operation of an MOS capacitor; accumulation, depletion and inversion. In the accumulation region, for an n-type semiconductor, application of positive gate voltage greater than flatband voltage ($V_{GB} > V_{FB}$) results in accumulation of negative charges (electrons) at the semiconductor surface just below the oxide-semiconductor interface (Figure 1.2a). V_{FB} is the flatband voltage where ideally there is no electric field across the oxide but in reality a built-in voltage is created due to difference in work function of metal and semiconductor and this results in band bending even when no voltage is applied. The flatband voltage is also the gate voltage that neutralizes the built-in potential, so there is no potential difference between the semiconductor surface and the bulk of the semiconductor (surface potential = 0 = $V_G - V_{FB}$, at flat band condition) [22]. The oxide capacitance can be measured as a function of gate voltage by superimposing a small ac signal on gate voltage. The change in applied gate voltage (ΔV_G) leads to accumulation charge density ($\Delta Q = C_{ox} \Delta V_G$). Capacitance per unit area is voltage independent and is determined by the gate oxide thickness, C_{ox} (F/cm^2) = ε_r/T_{ox}. Due to gate voltage, penetration of electric field into semiconductor or accumulation layer thickness can be determined from Poisson's equation and is known by Debye length (L_D), which is inversely proportional to doping level. At the flatband condition, the capacitance ($1/C_{FB} = 1/C_{ox} + 1/C_s$) is a series combination of gate-oxide capacitance and semiconductor capacitance ($C_s = \varepsilon_s/L_D$) where ε_s is the dielectric constant of the semiconductor. The band diagram of the accumulation region shows that the difference in Fermi level (E_F) between the metal and the semiconductor is equal to the applied gate voltage. Assuming downward bending for an *n*-type semiconductor, the application of a positive gate voltage shifts E_F towards the conduction band edge of the semiconductor (E_C) and electrons accumulates at the surface of the semiconductor underneath the oxide. The flatband voltage from the C-V plot was obtained at the corresponding capacitance (C_{FB}), which is expressed as

$$C_{FB} = \frac{\varepsilon_S C_{ox}}{C_{ox}\lambda + \varepsilon_s} \quad (1)$$

where ε_s is the permittivity of the semiconductor, C_{ox} is the oxide capacitance in accumulation region and λ is the Debye length expressed as

$$\lambda = \sqrt{\frac{\varepsilon_S kT}{q^2 N_D}} \tag{2}$$

where N_D is the doping density and k is the Boltzmann's constant.

In the depletion region, a negative dc gate voltage is applied and the majority carriers electrons are repelled from the oxide-semiconductor interface creating a depletion region to a depth x_D. This negative gate voltage is balanced by positive charge from the ionized semiconductor donor atoms. The capacitance of the depletion region per unit area is given by $C_D = \varepsilon_s / x_D$. x_D increases with gate voltage, and the overall capacitance of the MOS structure in the depletion region ($1/C = 1/C_{ox} + 1/C_D$) consists of C_{ox} and variable depletion capacitance (C_D). From Figure 1.2b, it can be observed from C-V plot in depletion region, as gate voltage becomes more negative, the capacitance decreases with increase in depletion depth x_D. The band diagram in depletion region shows an upward bending of the semiconductor conduction band and as a result, E_F remains away from both the conduction band (E_C) and valence band (E_v) edges. In depletion, gate charge per unit area, $Q_G = Q_D = N_D x_D$.

In the inversion region, the magnitude of dc gate voltage becomes more negative, and this attracts minority carriers (holes) in the semiconductor to the surface and inversion layers of holes are created (Figure 1.2c). The gate voltage at which this inversion occurs is called the threshold voltage. It is also the voltage at which a transistor actually turns on. After formation of inversion layer, the depletion depth x_D does not expand and remains "pinned" at x_{DMax}. The band diagram in inversion region shows that band bending placed E_F close to E_V, leading an exponential increase of holes in inversion layer. In inversion, gate charge per unit area, $Q_G = N_D x_D + Q_I$ where Q_I is the charge density in the inversion layer and gate charge is compensated mostly by inversion charge density in inversion region. The threshold voltage of a MOS capacitor is expressed as [23]

$$V_{th} = V_{FB} \pm \left[\frac{A}{C_{ox}} \sqrt{4\varepsilon_s q \left| N_{bulk} \phi_B \right|} + 2\left| \phi_B \right| \right] \quad (3)$$

where ε_s is the permittivity of the semiconductor, q is the electron charge (1.6×10^{-19}C), N_{bulk} is the bulk doping and ϕ_B is the bulk potential. The bulk potential is expressed as

$$\phi_B = -\frac{kT}{q} \ln\left(\frac{N_{bulk}}{N_i} \right) (Dopetype) \quad (4)$$

where T is the test temperature, N_i is the intrinsic carrier concentration and conductivity type is -1 for a n-type semiconductor

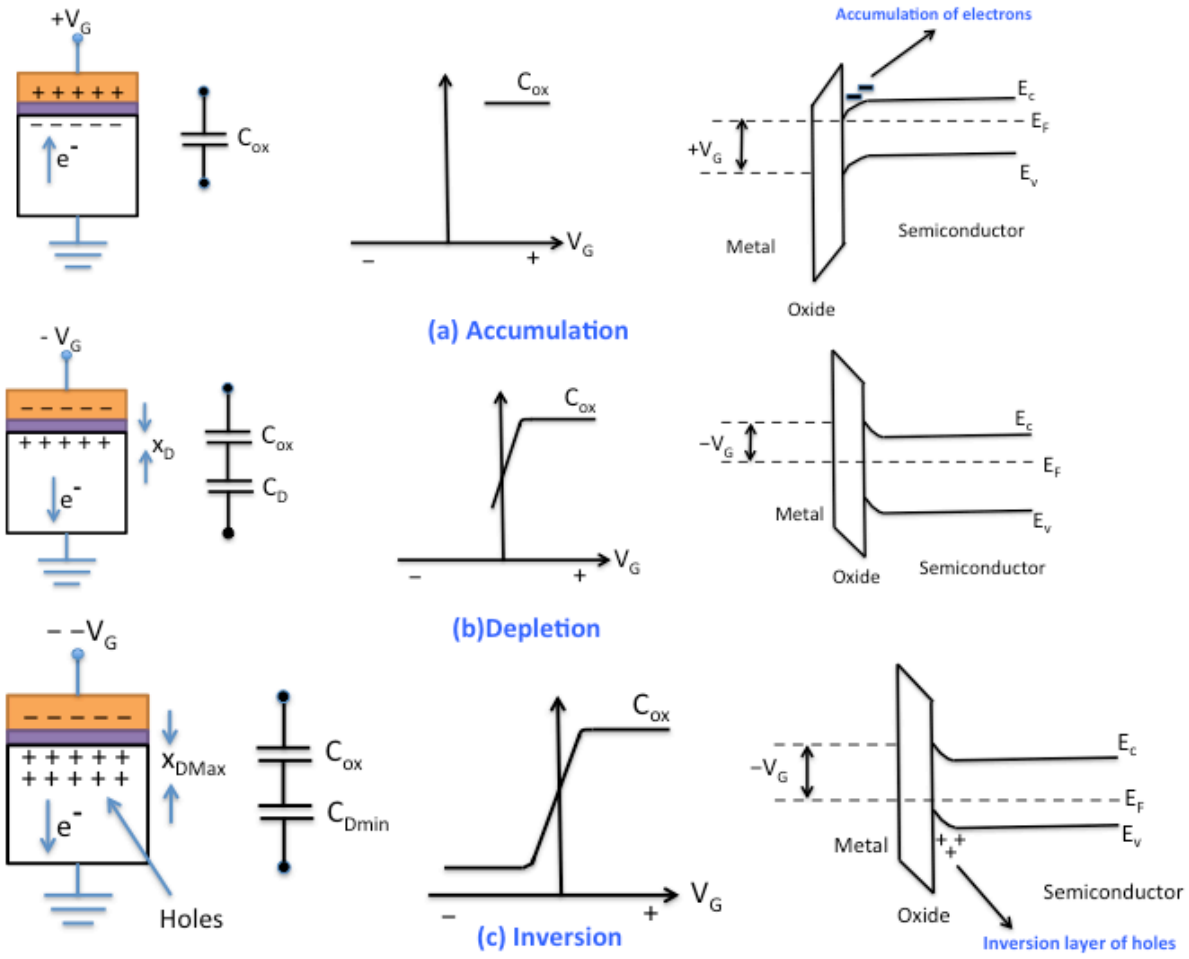


Figure 1.2 MOS capacitor structures, C-V plots and band diagrams in (a) accumulation, (b) depletion, and (c) inversion region [24].

C-V measurements can be done in quasistatic or high frequency conditions. During high frequency (100 kHz to 1MHz) C-V measurement, an ac signal is superimposed on a dc gate voltage (Figure 1.3). Due to high frequency ac signal, Q_I cannot provide the charge necessary for additional ΔQ_G because there are no additional holes in the substrate; and, in order to satisfy charge neutrality, majority carriers respond to the high frequency ac voltage by thermal generation and recombination [25]. Also, the oxide-semiconductor interface traps do not respond to high frequency ac gate voltage but can follow the slow change in dc gate voltage. This leads to a stretch out of the high frequency C-V curve. Quasistatic measurements (equilibrium condition) are taken at a very low frequency (1-10 Hz), which is almost dc (Figure 1.4). In quasistatic measurement Q_I can follow changes in Q_G. The asymmetrical shape of the high frequency C-V

plot can be used to determine the conductivity type of the semiconductor. For a MOS capacitor with a *p*-type semiconductor, the C-V plot sweeps from accumulation to inversion region as gate voltage becomes more positive and for MOS capacitor with an *n*-type semiconductor, the gate voltage approaches a negative value when sweeping from accumulation to inversion.

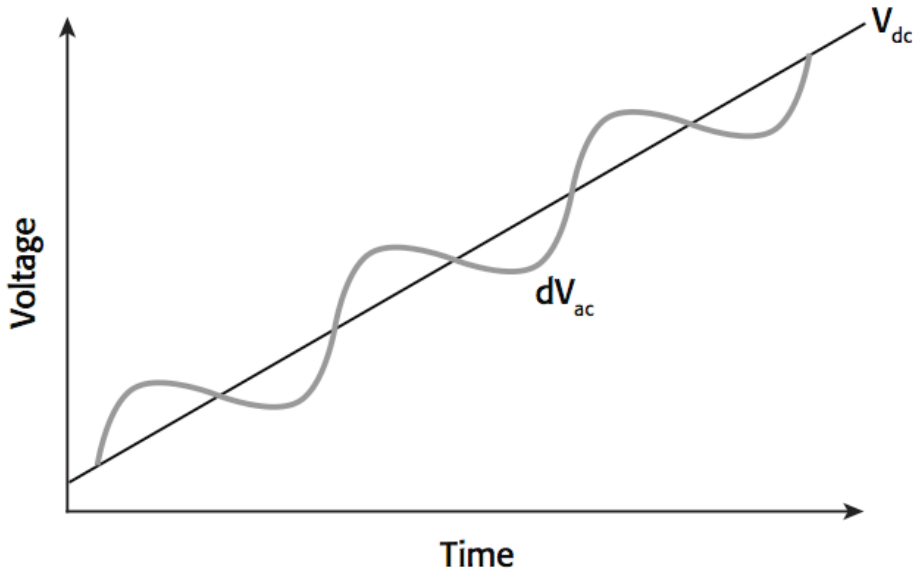


Figure 1.3 ac voltage superimposed on dc voltage during C-V measurement [26]

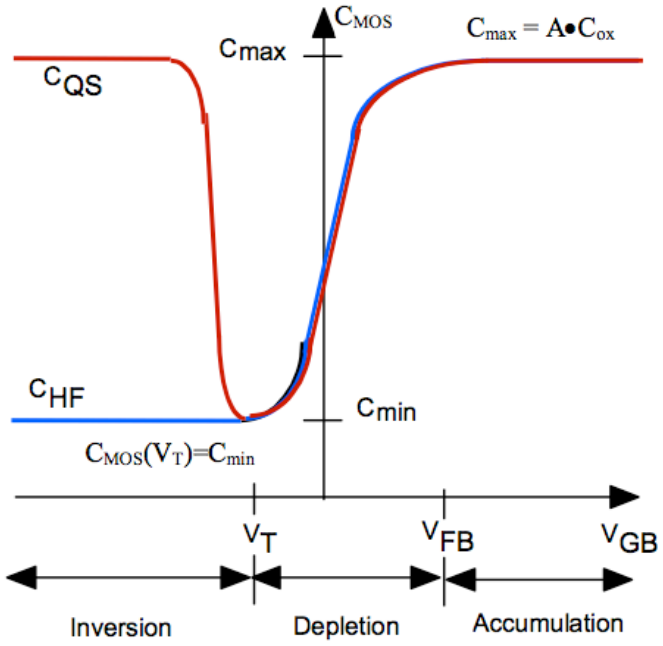


Figure 1.4 Low-frequency and high frequency capacitance-voltage plots [27]

In a high frequency capacitance-voltage plot, the accumulation region defines the oxide capacitance, C_{ox}; and most MOS capacitor characterization is dependent on C_{ox}. Therefore, it is important to select the start and stop voltage so that the depletion region remains within 1/3 to 2/3 of the dc voltage sweep range, and the device can be biased into strong accumulation region. During dc voltage sweep, the delay time is optimized to keep the device in equilibrium, otherwise a skewed C-V plot is obtained when the dc sweep rate is too fast. If the delay time is too small or the duration of the dc sweep is very short, the MOS capacitor does not have enough time to generate minority carriers for the formation of the inversion layer. It is better to start the dc voltage sweep from accumulation, because starting the sweep from inversion creates a non equilibrium situation that requires time to recover before the C-V sweep is initiated. Sometimes, sweeping the dc voltage from inversion is necessary to investigate hysteresis, and in that case, light can be used to generate minority carriers so equilibrium is reached quickly, and the hold time can be minimized before dc sweep. A device is in equilibrium if no hysteresis is observed while sweeping the dc voltage either from the accumulation or the inversion end.

1.2.2 Equivalent circuit model of MOS capacitor

Basic impedance parameters can be obtained by measuring the amplitude of the impedance. In order to extract actual capacitance from the impedance of MOS devices, an equivalent circuit model is required. There are parallel and series model as the two common ac impedance models. There are series circuit model for low leakage devices and parallel circuit model for low series resistance devices (Figure 1.5). A parallel model is also used to measure low values of the capacitance of dielectrics and contain interface trap information.

Current due to the small alternating (ac) signal response passes through the MOS capacitors connected to a circuit, and the ratio of alternating (ac) current to ac voltage (admittance) of the MOS capacitor consists of information about the MOS structure. Admittance is the reciprocal of impedance (Y =1/Z). In alternating current, impedance (Z=R+jX) is the sum of a real number, the ac resistance, and an imaginary part, the reactance (X). Admittance (Y=G+jB) is the sum of a real number, the ac conductance and an imaginary part, the susceptance (B). In the accurate model of the small-signal equivalent circuit, C is the actual frequency independent device capacitance, R_p is the effective device resistance due to tunneling through the oxide, and R_s is the series resistance of the substrate and the gate [28].

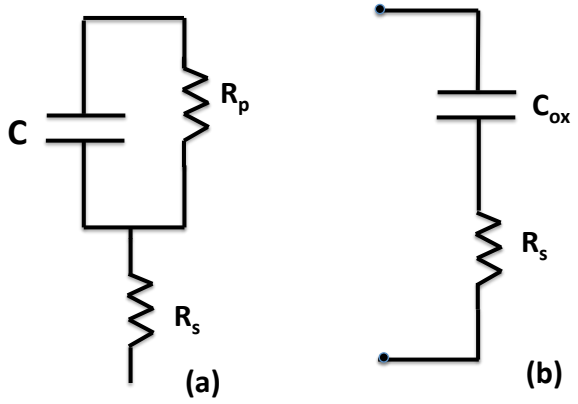


Figure 1.5 (a) Small-signal equivalent circuit model for MOS capacitor, (b) simplified model to obtain series resistance in strong accumulation

The admittance in strong accumulation in Figure 1.5b is $Y_{ma} = G_{ma} + j\omega C_{ma}$, where G_{ma} and C_{ma} are the measured conductance and capacitance, respectively. The series resistance is expressed as

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{5}$$

The equivalent parallel conductance method possess the same interface trap information as the equivalent parallel model, but the conductance method is more sensitive because conductance is directly related to the energy loss by the ac signal during capture and emission of carriers by interface traps (Figure 1.6). The Conductance method is more accurate in determining the interface trap density [29]. This model was used to determine interface trap density in chapter 2 and 5.

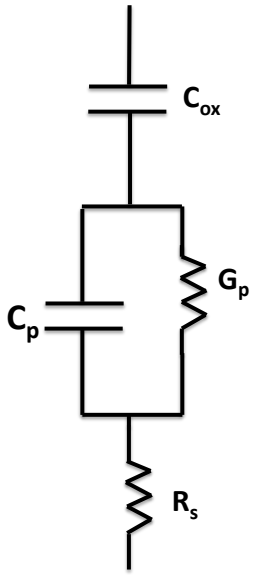


Figure 1.6 Equivalent circuit of the parallel capacitance and conductance with series resistance

1.2.3 Experimental approach

In this project, the fabrication of MOS capacitor samples was done at Naval Research Laboratory (NRL), Washington DC. The process of fabrication involves growth of GaN on

sapphire, deposition of the dielectrics on GaN or Si and deposition of metal contact by photolithography. The thickness of the dielectric was also measured in NRL using ellipsometry. At different stage of the fabrication process, the samples were sent to Kansas State University for surface characterization. After completion of the fabrication process, I was involved in electrical characterization of the samples using capacitance-voltage and current-voltage measurement. My group mate Daming Wei was involved in surface characterization using AFM, XPS and XRD.

Capacitance-voltage measurements were performed using a Keithley 4200 semiconductor characterization system, which is an ac impedance meter. In an ac impedance meter (Figure 1.8), the ac voltage originates from the high current terminal (HCUR) and the current at the output of the device under test (DUT) is measured at the low current terminal (LCUR). The voltage of the device under test is measured by the difference between the high (HPOT) and low terminal (LPOT). Stray capacitance is minimized by using a short coaxial cable between measurement leads. The impedance should be identical to the coaxial cable and the ac impedance meter. BNC connectors are attached to the coaxial cables to minimize deviation from the actual value due to a high series contact resistance. The dc current-voltage is measured using low noise triaxial cables. When the ac signal passes through a cable, a phase shift occurs that is proportional to the cable length and ac signal propagation delay. Therefore, cable length compensation is done to rectify the phase offset for a particular cable [30]. It is important in high frequency measurement to connect a very short wire jumper (red wire in Figure 1.7) between the two probes heads to confirm good ground connection and to prevent a large inductance and error in capacitance measurement.

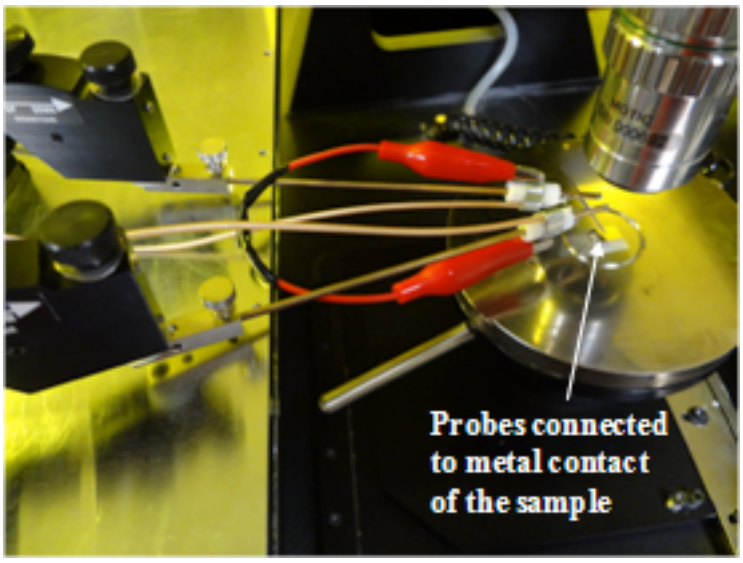


Figure 1.7 Wire jumper (red cable) between probes

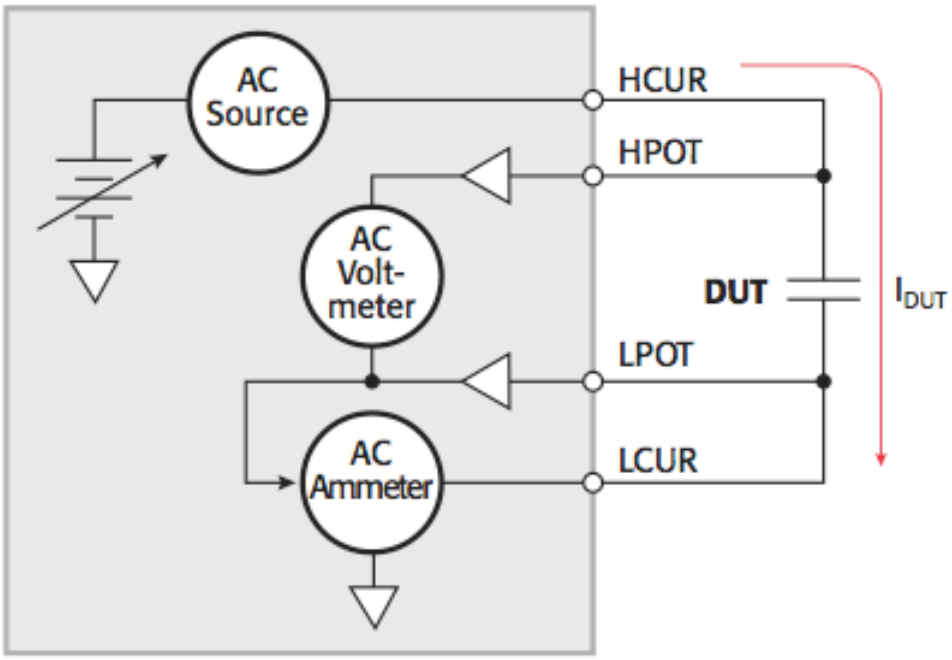


Figure 1.8 Schematic of an ac impedance meter [30]

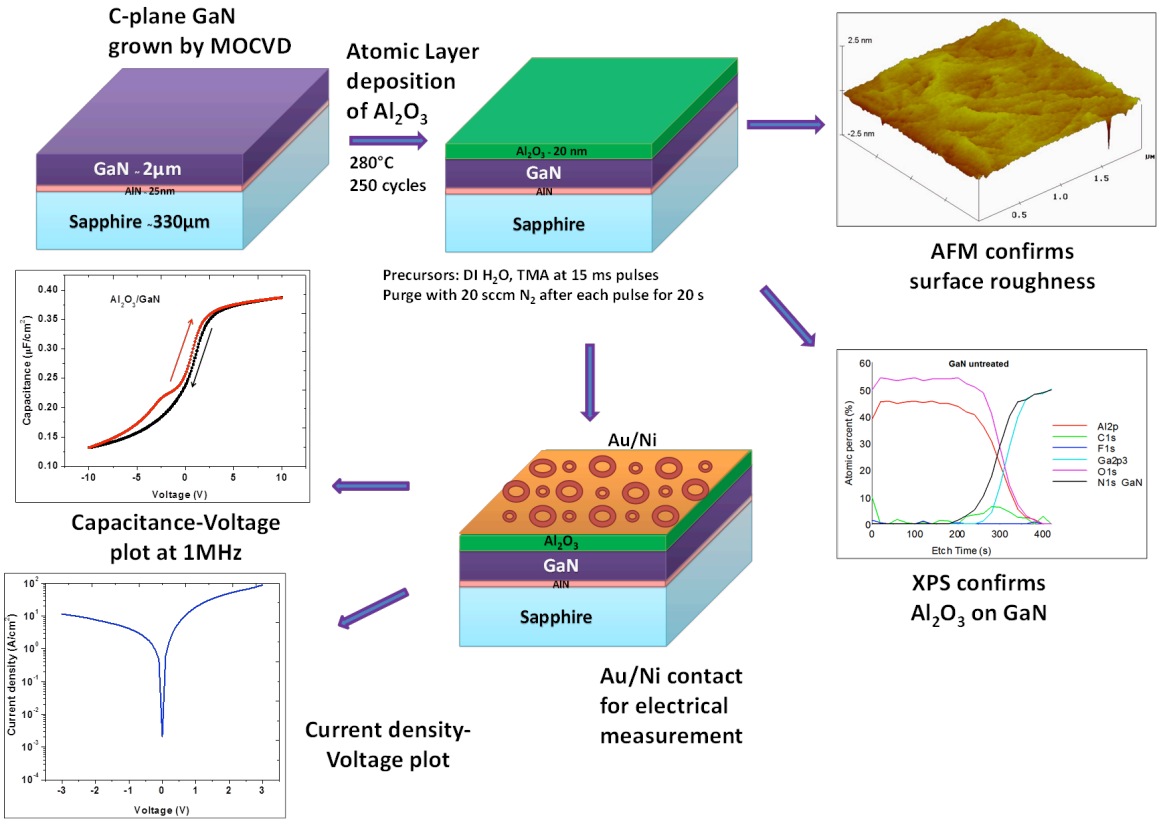


Figure 1.9 Experimental approach in the research

1.2.4 MOCVD of GaN epilayer

The GaN epilayers were grown by metal organic chemical vapor deposition (MOCVD). MOCVD has a faster growth rate than MBE and is thermodynamically stable. Ga-polar *c*-plane wurtzite GaN epilayers on sapphire were employed for the fabrication of Al_2O_3/n-GaN MOS capacitors. The epilayers consisted of a 1.5µm thick Si-doped, *c*-plane GaN grown on *a*-plane sapphire via MOCVD, using a 25 nm thick AlN buffer layer. The GaN epilayers were deposited at 1050°C, 150 Torr, using a V/III ratio of 3500. The precursors for the GaN epilayers were trimethylgallium and ammonia. Silicon doping, on the level of $1x10^{18}$ cm^{-3}, was achieved through the addition of silane.

1.2.5 Atomic layer deposition

Atomic layer deposition (ALD) is used to deposit high-k dielectrics for many applications including pin-hole free passivation layers for OLEDs [31], fuel cells [32], organic semiconductors [33], adhesion layers [34], BioMEMS [35] and passivation of crystal silicon solar cells as examples. During atomic layer deposition, deposition occurs due to chemisorption of precursor vapor one atomic layer per each cycle, pinhole and particle free. Conformal deposition is possible on structures with high aspect ratios. It is a self-limiting layer-by-layer deposition process. Compared to other deposition methods, ALD is capable of the highest step coverage (Figure 1.10).

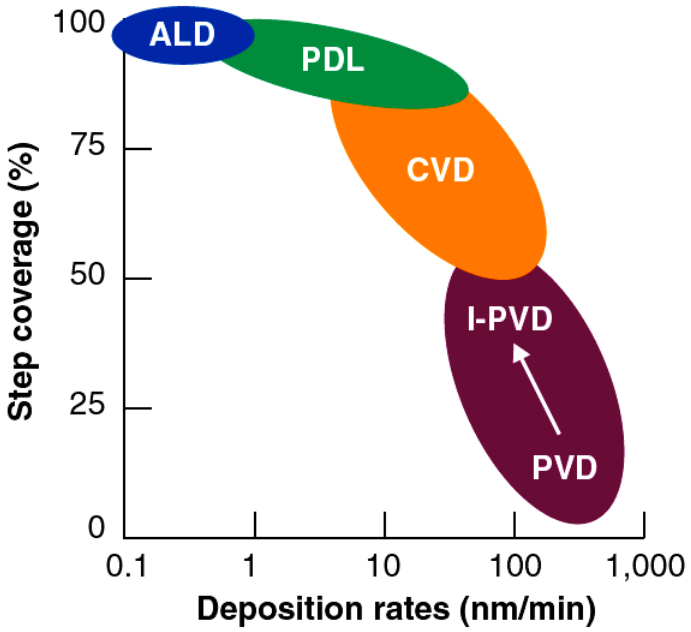


Figure 1.10 Step coverage (%) vs deposition rate [36]

During thermal ALD, Al_2O_3 is deposited using the precursor trimethylaluminum (TMA) and water, and methane is formed as a byproduct. During plasma ALD, an O_2 plasma is used instead of water. With a plasma discharge, the oxygen is dissociated. Plasma ALD enables deposition at a low temperature than thermal ALD and there is reduction in purge time of the

precursor as water is not used. The surface chemistry during atomic layer deposition of Al_2O_3 can be described as follows where the asterisks refers to surface species [37]

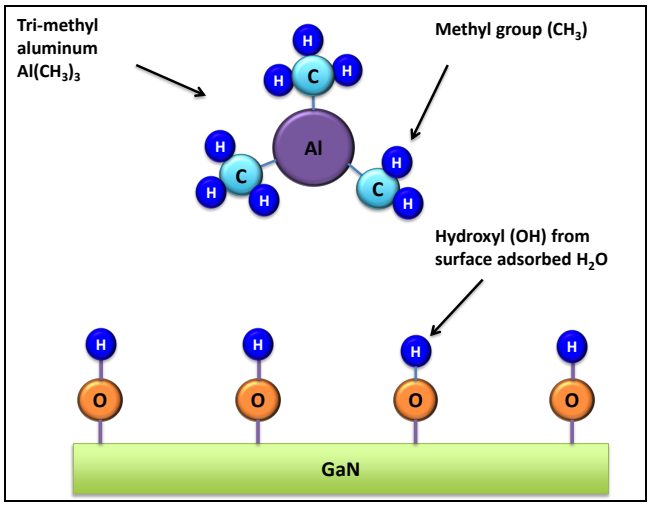
$$AlOH^* + Al(CH_3)_3 \rightarrow AlOAl(CH_3)_2^* + CH_4$$

$$AlCH_3^* + H_2O \rightarrow AlOH^* + CH_4$$

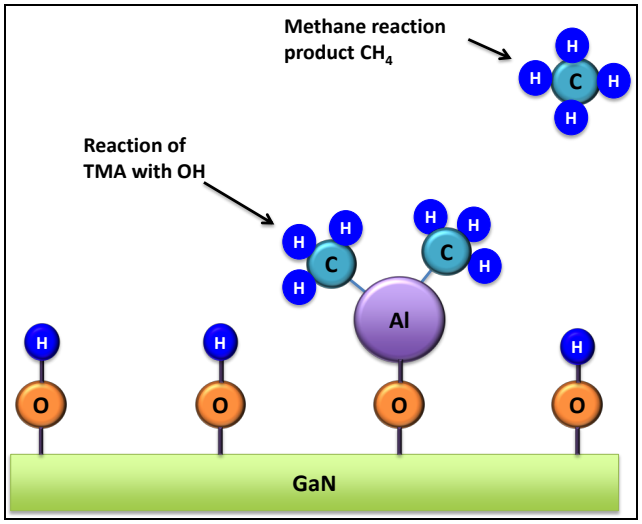
The driving force for the reaction is the formation of a strong Al-O bond. The overall exothermic reaction with an enthalpy of 376 kcal/mole is as follows

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 3CH_4$$

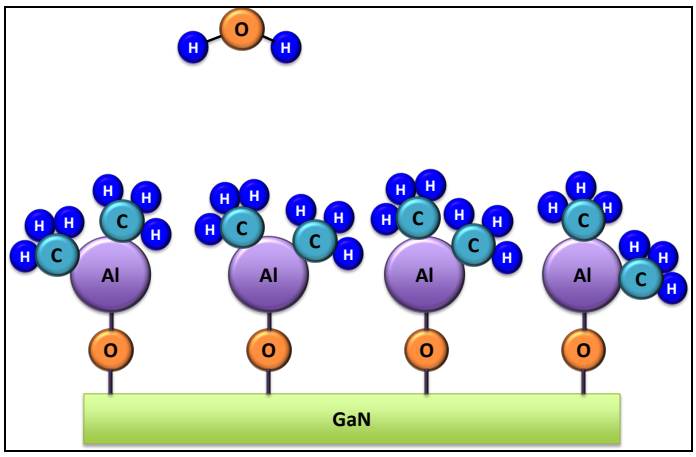
Due to contact with air, the GaN surface is terminated with hydroxyl groups (Figure 1.11a). The GaN epilayer on sapphire is placed inside ALD reactor and TMA is introduced as the first precursor. The TMA precursors (which don't react with each other) react with GaN surface hydroxyl groups and a single saturated monolayer is formed (Figure 1.11c). Methane is formed and both the methane and unreacted TMA are pumped out of the reactor. During the next half cycle, water vapor is introduced and creates saturated monolayer of oxygen on top of the aluminum atoms, and methane is formed as the reaction product. The methane and water are pumped away from the ALD reactor. Again TMA is introduced to start another cycle and the cycle repeats until target thickness of the dielectric is achieved (Figure 1.11f). In this research, the carrier gas of the precursors was 20 sccm ultra high purity nitrogen. The TMA pulse was 0.015 sec, the nitrogen purge was 20 secs, and the DI water pulse was 0.015 sec. The temperature of the reactor was 280°C for Al_2O_3 deposition at optimized conditions but other temperatures were also examined.


Tri-methyl
aluminum
Al(CH3)3
Methyl group (CH3)
Hydroxyl (OH) from
surface adsorbed H2O
Al
C
H
O
GaN

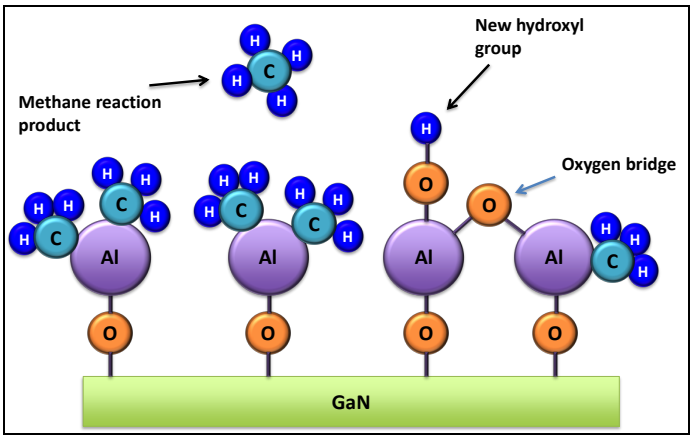
(a)


Methane reaction
product CH4
Reaction of
TMA with OH
Al
C
H
O
GaN

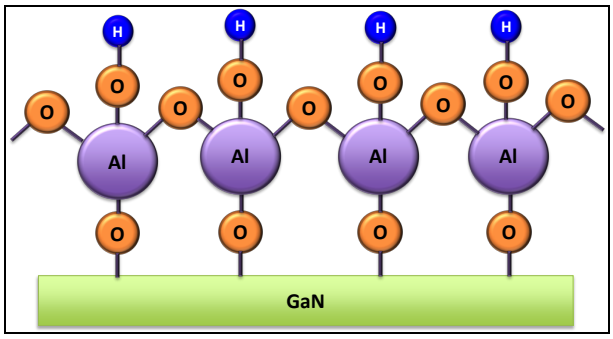
(b)


O
H
H
C
Al
O
GaN

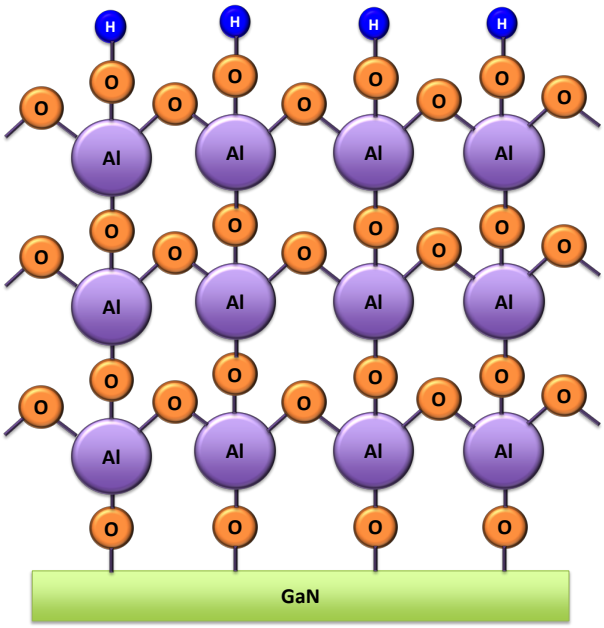
(c)


New hydroxyl group
Methane reaction product
Oxygen bridge
H
C
Al
O
GaN

(d)


H
O
Al
GaN

(e)



(f)

Figure 1.11 Schematic of the ALD process (a) TMA pulse in the reaction chamber, (b) TMA reacts with hydroxyl group, (c) Termination of reaction after one monolayer, (d) water reacts with dangling methyl groups forming Al-O strong bond, (e) formation of hydroxyl groups and, (f) after 3 ALD cycles [38]

1.2.6 Fabrication of metal contact

Metal contacts (Ni/Au) were fabricated using standard method of photolithography and e-beam evaporation. In this study, prior to any photolithography steps, the GaN samples were cleaned with warm acetone (~ 40°C), followed by rinsing in DI water and then drying off with compressed nitrogen. Excess water and moisture were removed by placing the samples on a hot plate at 175°C for approximately 5 minutes. Gradually lift-off resist (LOR) 5A (Microchem) and positive photoresist S1811 (Microchem) was applied. The photoresist was baked to harden, to improve the adhesion of the photoresist film, and to make it less susceptible to contamination. The photolithography mask was designed to produce circular capacitors of four different sizes

(50µm, 100µm, 150µm and 300µm). The sample was exposed to 320 nm UV light source for 35 seconds after mask alignment. Samples were immersed in developer CD-26 (RohmHaas) for 75 seconds to strip S1811 and lift-off resist from circular capacitors keeping unexposed photoresist only on the rings outside the capacitors (Figure 1.12). The samples were then rinsed in DI water and dried with N_2. Ni/Au (20nm/100nm) metal contacts were deposited by e-beam evaporation (TEMESCAL E-beam evaporator EC-200). Lift-off of S1811, LOR above Al_2O_3 around circular rings was done using PG remover at 80°C for 20 minutes, followed by cleaning of the sample with DI water and N_2.

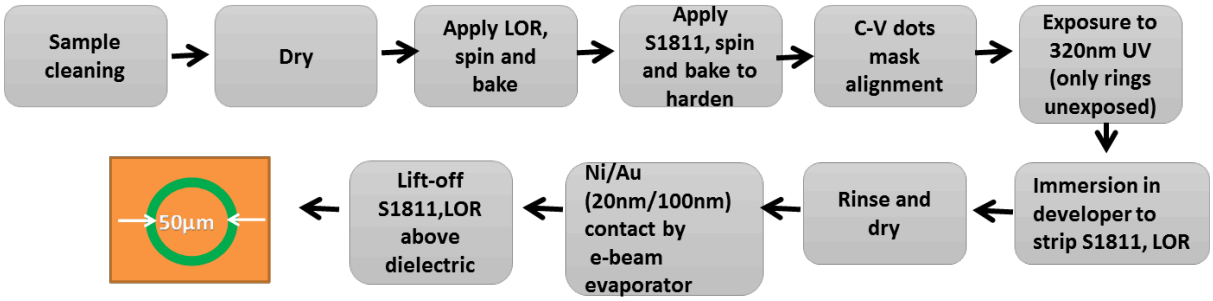


Figure 1.12 Basic steps of photolithography

For electrical measurements, the option of a top to the bottom contact was possible for Si based MOS capacitors but for GaN based MOS capacitors, only top to top contact are possible, since the GaN epilayer is on top of sapphire, an electrically insulating material.

1.2.7 Challenges with gate oxides and semiconductors

There are several challenges to fabricating MOSFETs as the complementary metal-oxide-semiconductor (CMOS) is scaled downward. A reduction in the dielectric thickness leads to exponential increase in direct tunneling current through the gate oxide [39]. High leakage current leads to increased power consumption and excess heat generation. As a result, electrical breakdown of the gate oxide may occur.

Nitrogen vacancies, native donor defects, creates *n*-type conductivity in undoped GaN [40]. Argon bombardment can remove nitrogen from GaN resulting in excess nitrogen vacancies and Fermi level pinning [41]. Point defects can be created in gate oxides as oxygen vacancies and degrade the electrical properties at the oxide-semiconductor interface (Y_2O_3/Si [42], HfO_2/Si [43]) of the device. Positive fixed charge is created in oxides due to point defects that cause a shift in the flatband voltage and electron traps are created that causes threshold voltage instability. Surface contamination of the semiconductor prior to deposition of dielectrics can form point defects by reaction among impurities and dielectrics. Degradation of semiconductor surface during plasma resist strip and oxide etch is a challenge as it increases semiconductor surface roughness and leads to defects in gate oxide at oxide/semiconductor interface [44].

1.2.8 Motivation for the selection of materials in MOS capacitor

1.2.8.1 Sapphire

In this research, sapphire was the substrate of choice to grow GaN epilayers due to its low cost [45], wide availability, hexagonal symmetry, and ease of handling and pregrowth cleaning. GaN epitaxial thin films are usually grown on sapphire by MOCVD, MBE and HVPE. This heteroepitaxy results in a high density of dislocations and cracks due to the mismatch (14% lattice mismatch) in lattice parameters and coefficients of thermal expansion between the GaN thin film and sapphire. Although the lattice mismatch (3.3%) between SiC and GaN is much lower compared to GaN and sapphire (14.8%), still sapphire is the most widely used and cheapest substrate to grow smooth films of [0001] oriented GaN (Table 1.2).

Table 1-2 GaN substrates [46]

	Lattice constant mismatch (%)	Dislocation density (cm^{-2})
GaN on bulk GaN	0	10^4-5×10^6
GaN on SiC	3.5	1×10^9
GaN on sapphire	14	5×10^9
GaN on Silicon	17	1×10^{11}

Sapphire is stable at high temperature (~1000°C), which is essential for epitaxy. Threading dislocation densities of epitaxial GaN on sapphire and SiC are typically between 10^8 to 10^{10} cm^{-2}. Despite the high threading dislocation density, light-emitting diodes based on GaN on sapphire demonstrate good luminescence efficiency [47]. Unlike most semiconductors, the presence of dislocations in GaN does not cause fast degradation of the optical or electric properties and thus sapphire still remains a good substrate for GaN electronics. The threading dislocations defects originate at the substrate/GaN interface and propagate into the epilayer. Sapphire has a higher thermal expansion coefficient than GaN, so GaN films grown on sapphire experience compressive strain. This strain is released by the formation of threading dislocations (Table 1.3). Yam *et al*. [48] studied dislocation density of GaN on sapphire grown by HVPE and found a reduction of the threading dislocation density with increasing GaN films thickness.

Table 1-3 GaN/sapphire defects

GaN growth method	Substrate	Type of defect	Source of defect	Reference
MOCVD	Sapphire	Threading dislocations	Nucleation layer	Kapolnek *et al.* [49]
MOCVD	Sapphire	Grain boundaries	Misorientation of crystal grains	Xu *et al.* [50]

Many different materials have been investigated as substrates for the epitaxial growth of GaN since bulk GaN crystals are scarce and expensive. Both *a*- and *c*-plane sapphire is being used for GaN growth and fabrication of LEDs. The lattice mismatch between GaN and *a*-plane sapphire is less than 2% [36]. The orientation of GaN is (0001) on both *a*- and *c*- plane sapphire. The crystal quality of GaN film grown on *a*-plane sapphire was identical compared to *c*-plane sapphire [51]. The advantage of *a*-plane sapphire is the presence of the cleavage plane (*r*-plane, (1012)) normal to the sapphire surface [36]. GaN epilayer grown on *a*-plane sapphire can be cleaved towards *r*-plane to obtain edge-emitting lasers.

High-quality nitride films can be grown on *c*-plane sapphire by the formation of a thin AlN buffer layer at low temperature [52]. Keller *et al.* [53] reported that nitrodizing sapphire by exposure to ammonia reduced the dislocation density in the GaN layer from 2×10^{10} to 4×10^{8} cm^{-2}. The AlN thin film is crystallographically rotated 30° in-plane with respect to the sapphire lattice; and, as a result, it decreases the lattice mismatch and strain between sapphire and GaN epilayer.

1.2.8.2 GaN

The market for GaN power semiconductors is expected to grow from nearly zero in 2011 to over $1 billion in 2021. Power supplies, solar inverters, and industrial motor drives are some of the markets for GaN electronics [54]. The cost of a GaN fabrication process is going down by growing GaN on top of silicon substrates with an aluminum nitride buffer layer. GaN high power HEMTs and MMICs are designed for high power, high efficiency amplifiers. GaN HEMT power devices can significantly reduce conduction and switching loss and help to solve environmental

issues with smaller power units [55]. GaN based devices are power saving and attractive for microwave power amplifiers, RADAR and satellite communication, hybrid electric vehicles, and the multi-billion dollar commercial lighting market (Figure 1.13).

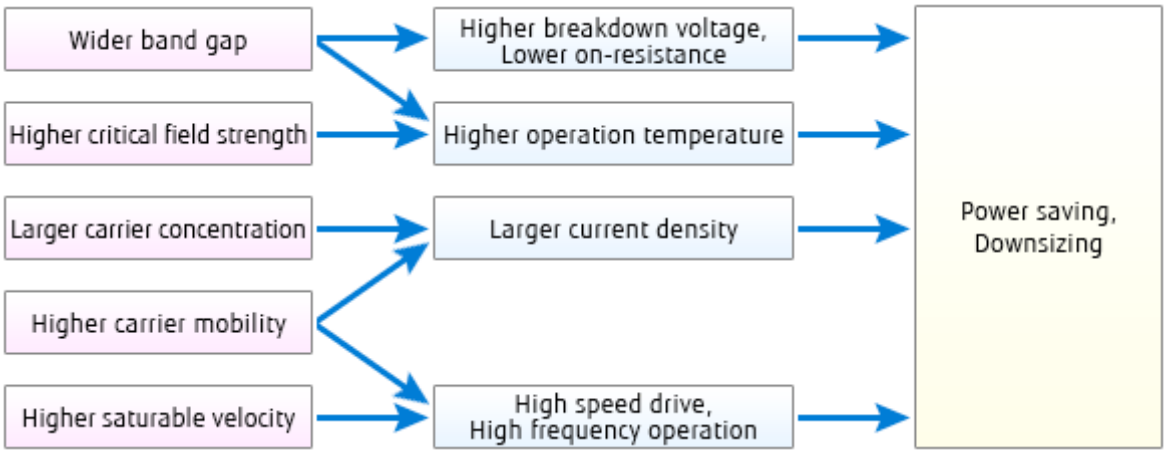


Figure 1.13 Advantage of GaN devices [55]

Due to the small bandgap of Si (1.12eV), Si-based power transistors shows inferior performance at high temperature (200°C), which has motivated researchers to investigate the performance of GaN based power devices. The first breakthrough with GaN semiconductor occurred in early 1990s with the invention of GaN based light-emitting diodes, other rapid developments in various applications have occurred since (Figure 1.14) [56]. GaN can be used to manufacture power electronics to create faster, heat-resistant and energy efficient transistors. For transistor applications, GaN is excellent for high frequency combined with high power, which is used for broadcast and cell phones.

To achieve *n*-type conductivity (carrier concentration 10^{17}-10^{19} cm^{-3} [57]) in GaN, Si doping (Si activation energy ~ 27meV [58]) is effective. In contrast, *p*-type conductivity in GaN (~10^{16} cm^{-3} [59]) is difficult to achieve due to hydrogen passivation and nitrogen vacancies. GaN can be made *p*-type by Mg doping and it is difficult to achieve high hole concentrations, due to the high activation energy of Mg acceptors[60] (Mg activation energy ~ 182 meV [61]).

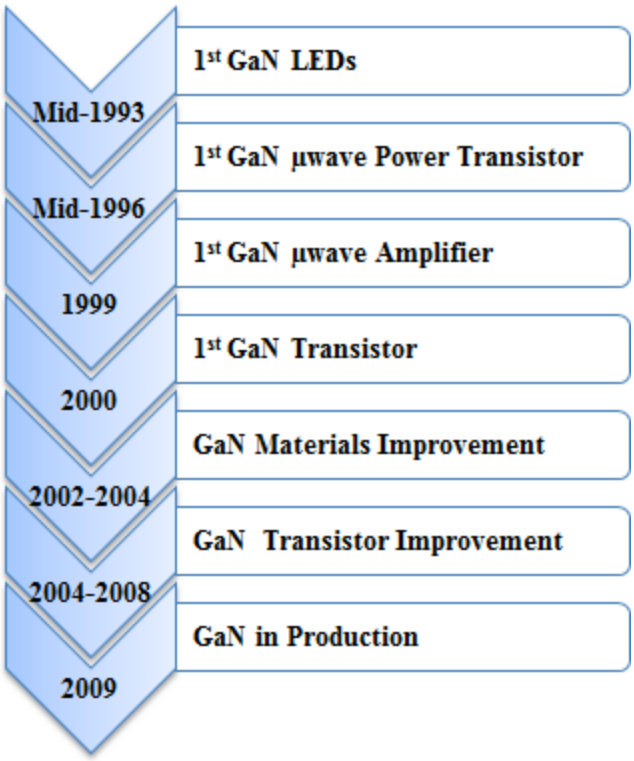


Figure 1.14 GaN technology timeline

1.2.8.2.1 Polarization in GaN

Spontaneous and piezoelectric (induced) polarizations are present in GaN (0001) planes. Wurtzite GaN has spontaneous charge along the [0001] direction, where negative charges form on the Ga face and positive charges on the N face (Figure 1.15). The piezoelectric field is not observed in orientations perpendicular to [0001] direction (the *a*- or *m*-planes) or other nonpolar planes [62]. The spontaneous polarization within the crystal is due to combination of ionization and irregular arrangement of gallium and nitrogen atoms[45]. The piezoelectric polarization is caused by crystal strain (mechanical perturbation) in the material, which changes the c/a ratio in wurtzite nitrides. For example, spontaneous polarization is significant in AlGaN/GaN due to a large spontaneous polarization of AlN, and piezoelectric polarization is significant in InGaN/GaN due differences in the lattice constant of InN and GaN [63] .

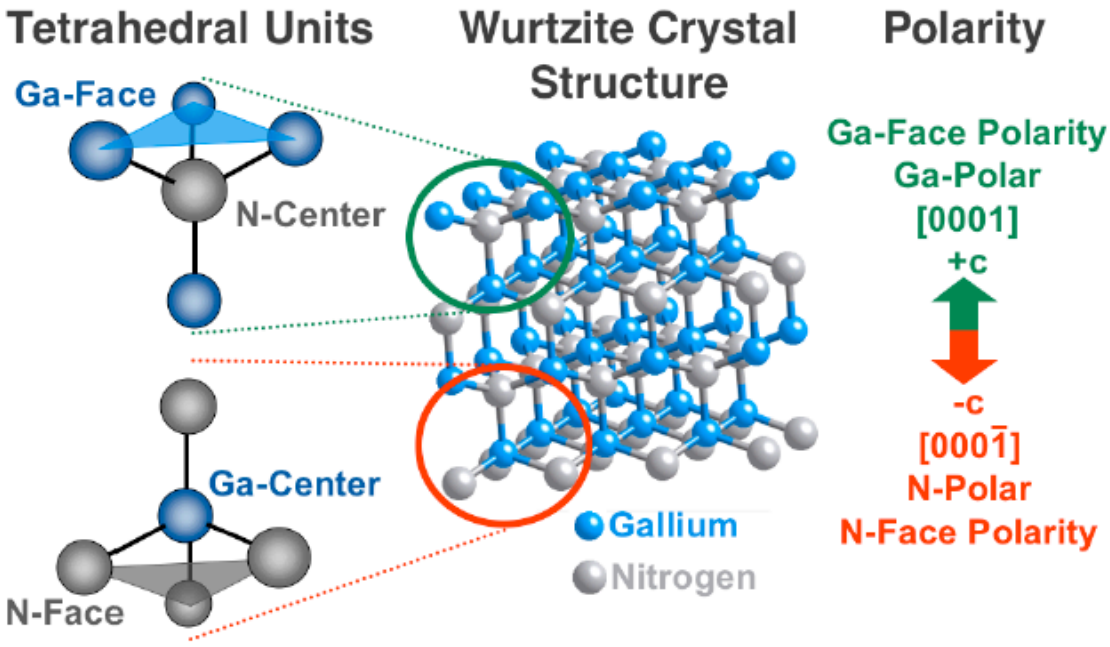


Figure 1.15 GaN wurtzite structure showing Ga-face and N-face polarity [64]

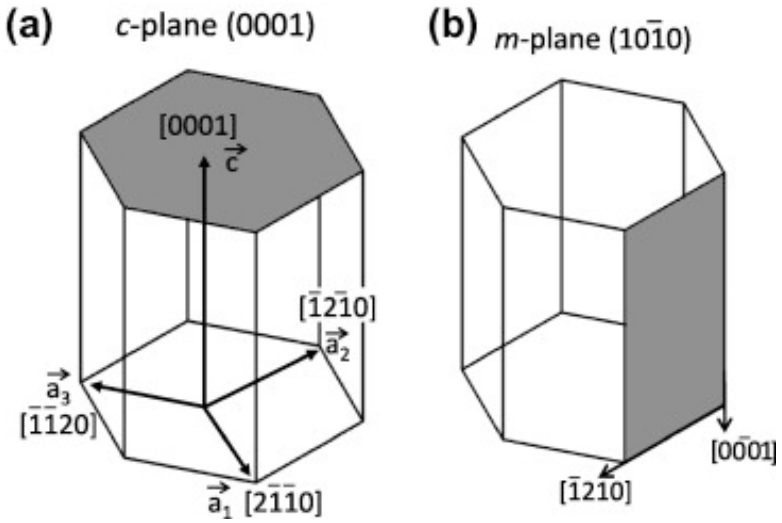


Figure 1.16 GaN planes: (a) polar *c*-plane and (b) nonpolar *m*-plane [38]

Nonpolar planes do not form polarization discontinuities in heterostructures; this has motivated great interest in *m*-plane GaN for devices with normally-off operation (Figure 1.16). For power and consumer applications, a normally off operation is preferred for the safety of the switching systems. GaN based MOSFETs on *c*-plane substrates show poor threshold voltage stability with temperature due to the strong pyroelectric polarization (polarization change due to temperature) present in polar GaN. Non-polar GaN leads to better temperature stability and normally-off transistor operation; polar GaN based devices do not. High quality and large sizes of *m*-plane GaN substrates are also useful for green lasers and miscut *m*-planes showed improvement in laser performance [65].

1.2.8.2.2 Properties of GaN

Si, GaAs, SiC and GaN are the main semiconductors used commercially for high-power/high-temperature switching applications. GaN transistors promise to deliver better linear power and efficiency than is possible with silicon.

It is the high breakdown voltage that makes SiC and GaN most suitable for RF power devices (Table 1.4). The temperature rise is lower for SiC and GaN due to their high thermal conductivity and low self heating. GaN alloyed with In and Al (nitrides), bandgap can be tuned between 0.7 eV to 6.2 eV, which is suitable for light emitters ranging from infrared to deep-ultraviolet. A great advantage of GaN over SiC, is the ability to grow heterostructures, e.g. AlGaN/GaN that produce a two-dimensional electron gas (2DEG), which is the conductive channel and the major, constitute to HEMTs (high electron mobility transistors).

GaAs exhibits a higher carrier mobility compared to GaN, but the higher saturation velocity of GaN HEMTs overcomes its lower mobility and is more applicable for high power amplifiers. GaN amplifier modules can be made much smaller than GaAs with the same output power and therefore lowers cost of a chip. GaN has a breakdown field of about 3MV/cm, more than seven times higher than GaAs 0.4 MV/cm (Table1.4). Therefore GaN can withstand higher voltages within smaller device dimensions. Different Figures of Merit (FOM) are used to merge relevant material properties into a unique number to express the strength of the material (Table 1.4). The Johnson FOM consists of the breakdown electric field, electron saturation velocity and for GaN this FOM is fifteen times greater than GaAs.

Table 1-4 Important properties of semiconductors [45]

Property	Si	GaAs	4H-SiC	GaN
Bandgap(eV)	1.12	1.43	3.26	3.4
Breakdown field (10^6 V/cm)	0.25	0.35	3.5	3.5
Temperature (max)	300°C	300°C	600°C	700°C
Saturation velocity (10^7 cm/sec)	1.0	1.0	2.0	1.5
Johnson's figure-of-merit ratio	1.0	3.5	60	80
Thermal Conductivity (W/cm-°K)	1.5	0.46	4.9	1.7
Electron Mobility (cm^2/V-sec)	1350	6000	800	1000

1.2.8.2.3 GaN MOSFET structure

In a transistor, a field effect is created by applying a positive bias on the gate relative to the source (Figure 1.17). The applied bias creates a conductive channel between the source and drain by attracting electron beneath the gate oxide. In this manner, small changes in gate voltage are amplified into relatively much higher changes and transferred to the external circuit that connects the source and the drain. The power handling capability of a transistor is defined by the number of watts the transistor can transfer per unit width of the gate [45]. The company EPC (efficient power conversion) has grown GaN on Si using AlN buffer layer technology using large volume silicon process equipment to bring cost efficient solution of power switching [66].

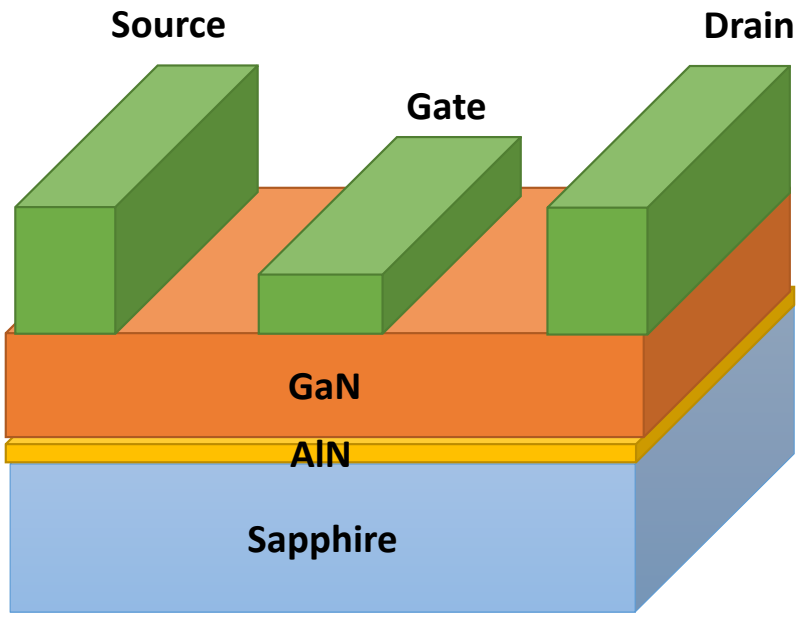
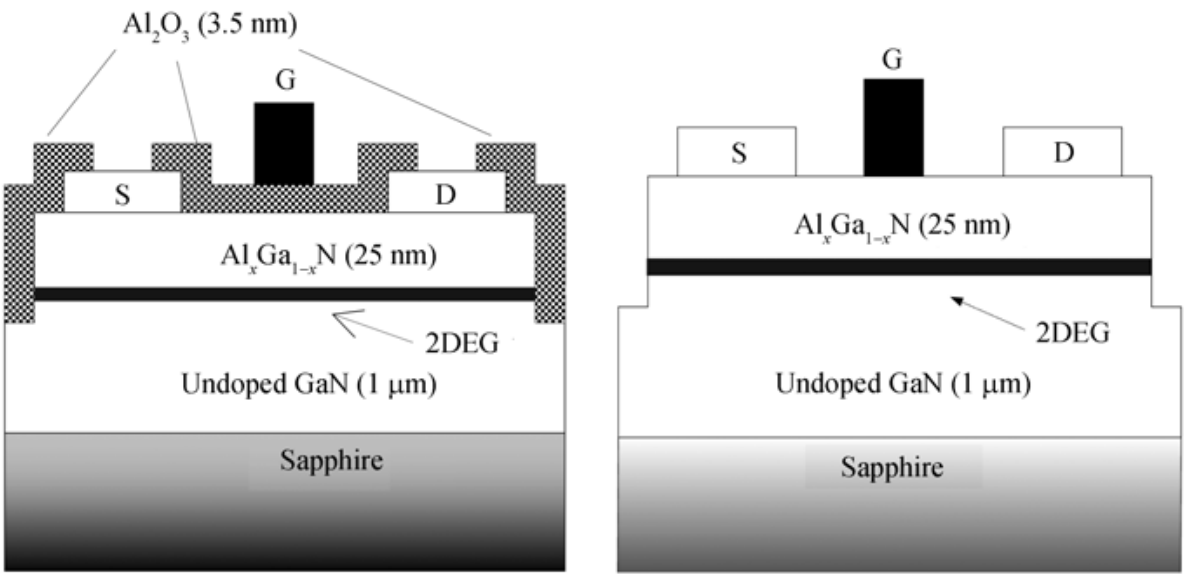


Figure 1.17 GaN MOSFET

1.2.8.2.4 MOS-HEMTs

In AlGaN/GaN HEMTs leakage current is of great concern due to electron trapping through the surface states and tunneling in the Schottky/GaN interface. Reducing the leakage current is essential to obtain highly efficient device without device failure. The MOS structure is an effective structure for AlGaN/GaN HEMTs to prevent leakage current. Remarkable improvements have been achieved to prevent high gate leakage and drain current collapse using SiO_2, Si_3N_4, Ga_2O_3, Al_2O_3 and Sc_2O_3 as gate dielectrics in MOS-HEMTs [67]. Seok *et al.* [68] recently fabricated MOS-HEMT on silicon substrate with HfO_2 as gate dielectric and reported significantly lower leakage current compared to conventional HEMT devices. Yue *et al.* [69] reported better interface property, lower leakage current and smaller C-V hysteresis for Al_2O_3/AlGaN/GaN MOS-HEMT compared to AlGaN/GaN HEMT.



(a) (b)

Figure 1.18 Cross section of (a) Al_2O_3/AlGaN/GaN MOS-HEMT, (b) AlGaN/GaN HEMT fabricated by Yue *et al.*[69]

1.2.8.3 Dielectrics

If the thickness of a SiO_2 gate dielectric goes below 2 nm, the leakage current through it becomes high due to quantum mechanical tunneling and circuit power dissipation would be unacceptable [70]. Power dissipation is a key factor in mobile phones, laptops etc. SiO_2 loses its bulk electronic properties when thinner than 0.7 nm [71]. To further increase integration of devices and their density in circuits, it is essential to lower the power supply voltage to improve the drain-current response due to thin gate oxide. The tunneling current decreases exponentially with oxide thickness and to keep the same capacitance ($C = \varepsilon_0 kA / t_{ox}$), a thicker layer of a new material with a higher dielectric constant compared to SiO_2 is necessary. Chu *et al.* [72] reported on a AlGaN/GaN/silicon heterostucture (MOS-HEMT) using high dielectric constant (high-κ) erbium oxide layer that exhibited improved performance, as compared with the conventional high electron mobility transistor (HEMT). To reduce the electric field strength imposed on the oxide, a SiO_2 replacement with a relatively high-*k* oxide is necessary. A promising candidate for gate dielectric (high-κ and high bandgap) can be chosen from the upper left corner of the plot bandgap vs dielectric constant (Figure 1.19).

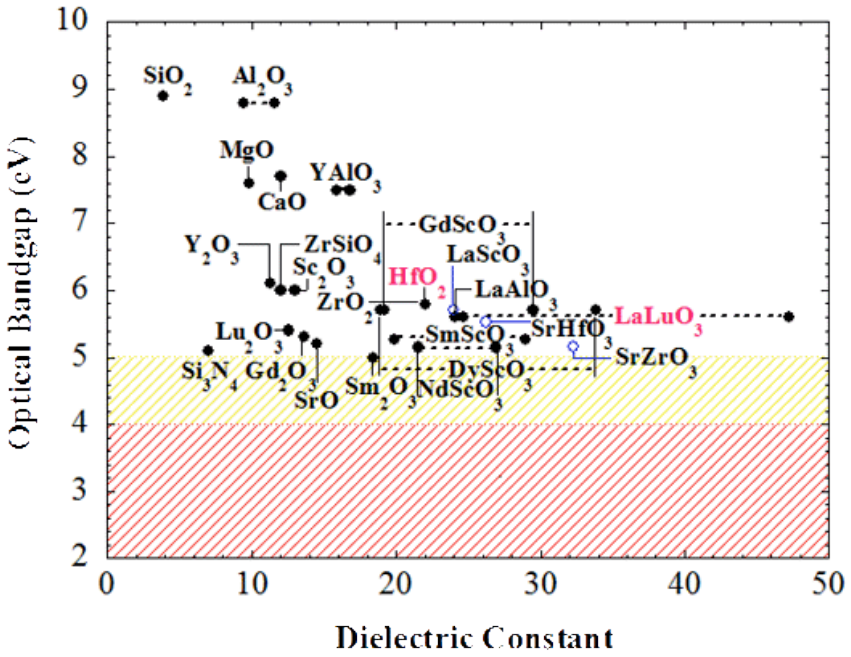


Figure 1.19 Plot of dielectric constant vs the optical bandgap of gate dielectrics [4]

In integrated circuits, speed is greatly improved by shrinking transistor dimensions [73]. To meet the scaling of complementary metal-oxide-semiconductor (CMOS) transistors, the thickness of SiO_2 had to approach 1.4 nm at 15 nm gate length [70,74]. Leakage current has a negative effect on the device performance. The oxide is not damaged due to tunneling currents, but gate leakage can lead to circuit failures and unacceptably high power consumption. In mobile devices, thin dielectrics may lead to reduced lifetime and increased operation temperature, which also increase gate leakage. Therefore, it has become essential to replace SiO_2, which has a low dielectric constant (κ =3.9) with a physically thicker layer of a new gate insulator with a higher dielectric constant. The efficiency of metal oxide semiconductor (MOS) capacitors and transistors for high power, high frequency applications depend on the quality of the gate dielectrics. FET power-switching applications require high-quality gate dielectrics that (i) have a high dielectric constant for scaling, (ii) low leakage current to reduce the standby-power consumption, (iii) have low interface trap density, and (iv) have band offsets with the semiconductor of over 1 eV to minimize carrier injection [70].

Intensive research is now ongoing around the world to develop insulators with a high dielectric constant to produce highly efficient transistors. Al_2O_3 was the first high-κ dielectric to

replace SiO_2 in CMOS digital integrated circuits. Al_2O_3 also has application in fabrication of high performance single-walled carbon nanotube field effect transistors [75], passivation of organic light-emitting diodes [76] and as wear-resistant coating for microelectromechanical (MEMS) devices [77]. The large bandgap of Al_2O_3 (8.9 eV) has a high energy band offset with GaN (3.4 eV) that prevents current tunneling [78]. TiO_2, due to its unusually high dielectric constant (up to 300 for rutile TiO_2) [79,80], is potentially a good alternative to SiO_2 for the gate dielectric of MOS capacitors [81]. TiO_2 has a high refractive index [82], high band gap (3.2 eV) [83], excellent optical transmittance [84], and is one of the promising oxide films for the fabrication of high density dynamic random access memories (DRAMs). If high-κ dielectrics are used in DRAM instead of low dielectric films, the complicated geometries with stacking and trenching can be minimized to achieve target charge storage density of the RAM [85]. The dielectric constants of various dielectrics with κ values are listed in table 1.5.

Table 1-5 Static dielectric constant (κ) of gate dielectrics [70,86]

	Dielectric constant (κ)	Bandgap (eV)
Si_3N_4	7	5.3
Al_2O_3	9	8.8
TiO_2	80	3.5
$SrTiO_3$	2000	3.2
HfO_2	25	5.8
La_2O_3	30	6
ZrO_2	25	5.8
SiO_2	3.9	9
Ga_2O_3	10	4.4

The major difficulty of using high-k dielectrics deposited on III–V semiconductors is the high-interface trap density ($D_{it} > 10^{13}$ $cm^{-2}eV^{-1}$) that is created at the interface of III–V semiconductors and high-κ gate dielectrics, as this is responsible for reduction in effective channel mobility in MOSFETs [87].

SiO_2 can be made from Si by thermal oxidation and it forms an excellent interface with Si with very few electronic defects. Ge, GaAs and GaN have poor native oxides; therefore deposition of oxide on these semiconductors is typical. For GaN, producing a native oxide is a

challenge due to its high D_{it} and various defects [88]. One of the goals of this research is to investigate whether thermal oxidation can be useful.

1.2.9 Current conduction through dielectric

While determining leakage current through the dielectric by current-voltage measurement of the MOS capacitor, it is also necessary to become familiar with its mechanism. Carrier conduction through the insulator occurs due to a high gate bias or sample temperature that can be explained by Schottky emission (SE) and Poole-Frenkel (PF) effects or by other mechanism. The Schottky emission process is dependent on temperature, and carrier tunneling is due to thermionic emission that occurs between the band of the semiconductor and the band of gate metal. In contrast, the Frenkel-Poole emission is due to field enhanced thermal excitation where electrons first tunnel from the semiconductor into a trap and then tunnel through the conduction band of the dielectric film to the gate electrode (Figure 1.20). These traps restrict current flow in dielectric due to capture and emission process within the bandgap [89-91].

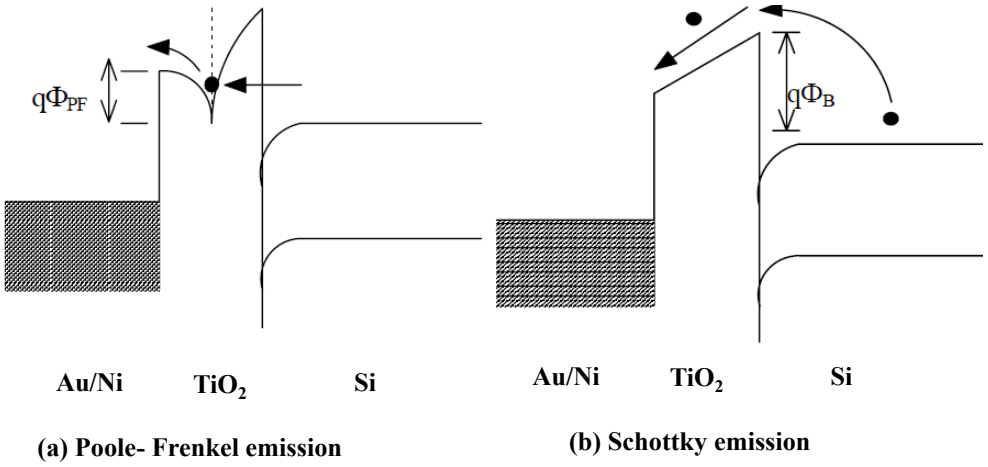


Figure 1.20 Energy-band diagrams showing conduction mechanisms of (a) Frenkel Poole emission and (b) Schottky emission mechanism for Au/Ni/TiO_2/n-Si MOS structure.

1.2.10 Gate Metal

In this study, metallic contacts (100 nm Au/ 20 nm Ni) were deposited on dielectric as top to top contact due to difficulty of creating ohmic contact on GaN. The gate metal is deposited

using e-beam evaporation at room temperature on an insulator and it is not expected to be ohmic. The large contacts are approximately ohmic due to their size.

Papanicolaou *et al.* [92] reported Cr/Al/Ni/Au system had a lower specific contact resistant and greater temperature stability than the Cr/Al system when annealed in the 800–1200°C temperature range. Au and Ni possess resistant to oxidation and can be deposited on top of Ti/Al contacts to form ohmic contact [93].

1.2.11 Previous studies of high-κ dielectrics on GaN

To achieve low gate oxide leakage current, it is very important that there exists conduction and valence band offset (> 1eV). Due to large band offset SiO_2 (CBO ~3.6 eV [94]) still remain as a good insulator for GaN MOSFETs. Placidi *et al*. [95] worked on properties of the SiO_2 (100 nm) on *n*- and *p*- type GaN interface using PECVD with different precursors; silane and TEOS. They found for n-type GaN annealed (800°C for 2 min in N_2) SiO_2 from silane exhibited lower interface trap density ($D_{it} = 6.1\times10^{10}$ $cm^{-2}eV^{-1}$) and surface roughness compared to p-type GaN sample ($D_{it} = 4.2\times10^{11}$ $cm^{-2}eV^{-1}$). The high dielectric constant enhances device current driving capability. Chang et al. [96] reported on deposition of Al_2O_3 and HfO_2 on n-type GaN by ALD and found that interfacial layer of GaON and HfON exists between HfO_2 and GaN that contributes to overall low dielectric constant. There was no interfacial layer at Al_2O_3 /GaN. They also studied TiN/HfO_2/Al_2O_3 /GaN stack to take advantage of high dielectric constant of HfO_2, large energy bandgap of Al_2O_3 and high quality Al_2O_3 /GaN interface and found that the composite film provided sharp oxide/GaN interface. Ko-Tao *et al*. [97] studied Al_2O_3/TiO_2/Al_2O_3 Nanolaminates on GaN and found low leakage current (3.8×10^{-8} A/cm^2 at 1V) with post metallization annealing and $(NH_4)_2S_x$ treatment. Table 1.6 lists previous work on high-κ dielectrics on GaN and it shows that improvement in leakage current density was observed after annealing treatment. It should be noted that extraction of interface trap density varies depending on what method is used and it is difficult to come to a conclusion based on different methods to extract D_{it} [94].

Table 1-6 Previous studies of high-κ gate oxide on GaN

Samples	Oxide deposition	D_{it} ($eV^{-1}cm^{-2}$)	Hysteresis (mV)	Leakage current (A/cm^2)	References
TiN(150nm)/Al_2O (8.9 nm)/GaN(800nm)/ *c*-sapphire	ALD at 200°C	(5-8)×10^{11} by conventional Terman method	50	1×10^{-9} A/cm^2 at 1V (post metallization annealing at 750°C for 30s)	Chang *et al.*[96]
TiN(150nm)/HfO_2 (8.8 nm)/ GaN(800nm)/*c*-sapphire	ALD at 300°C	(7-8)×10^{11} by conventional Terman method	360	1×10^{-9} A/cm^2 at 1V((post metallization annealing at 600°C for 10 min)	Chang *et al.*[96]
Ni/TiO_2-MgO (1:1 10 nm)/MgO (5 nm)/*p*-GaN/sapphire	Dual-target RF sputtering (O_2 annealing at 500°C for 15 min)	4×10^{11} near midgap by conductance method	230	6.9×10^{-9} A/cm^2 at 1V	Lee *et al.*[98]
Ni/Al_2O_3 (2.5 nm)/TiO_2 (5nm)/Al_2O_3 (2. 5nm)/GaN/ *c*-sapphire	RF sputtering (O_2 annealing at 550°C for 15 min)	(4.5-7.7)×10^{11} by Terman method	$(NH_4)_2S_x$ treatment eliminated hysteresis loop	3.0×10^{-8} A/cm^2 at 1V	Ko-Tao *et al.*[97]
Al/$MgTiO_3$ (200nm)/*n*-GaN/ sapphire	Solid state sintering at 1450°C for 4h (ε_r =17.8)	6.2×10^{12} by Terman method		1.8×10^{-8} A/cm^2 at 5V	Hsiao *et al.*[99]
β-Ga_2O_3/n-GaN/*a*-sapphire	Dry thermal oxidation at 880°C for 5hr	5.5×10^{10}	500		Nakano *et al.*[100]
Al/Ta_2O_5(281nm)/ *n*-GaN/*c*-sapphire	Sputtering (ε_r =37)	2.6×10^{11}		<10^{-8} A/cm^2 at 1MV/cm	Yeoh *et al.*[101]
Al/SiO_2/ α-Ga_2O_3 (80nm)/*n*-GaN/ *c*-sapphire	Ga_2O_3 (ε_r =10.6) by photo-electro-chemical oxidation and SiO_2 by PECVD	2.0×10^{11}		10pA at -10V (Ga_2O_3 film annealed at 900°C)	Ching *et al.*[102]
BeO(3nm)/GaN (2nm)/AlGaN (17.5nm)/GaN (800nm)	ALD at 250°C (ε_r = 8.5)			1.1×10^{-7} A/cm^2 at 0.8V (annealing in ambien N2	Johnson *et al.*[103]
SiO_2(50nm)/ n-GaN/sapphire	Photochemical vapor deposition (photo-CVD)	8.4×10^{11}		6.6×10^{-7} A/cm^2 at 4MV/cm	Chang *et al.*[104]

The III-nitride/dielectric interface is altered with exposure with ambient during different processing steps. Varying polarities and lattice mismatch of GaN with most dielectrics require more understanding. Commercial GaN wafers consist of high threading dislocation density, which still requires lot of understanding as it affects device performance.

1.2.12 Non-ideal effects in MOS capacitors

Due to the presence of charge at the gate-dielectric (Figure 1.21) and semiconductor-dielectric interface, there could be a shift in threshold voltage. Surface passivation is required to prevent trapped electrons from leaking from the gate metal under large electric field.

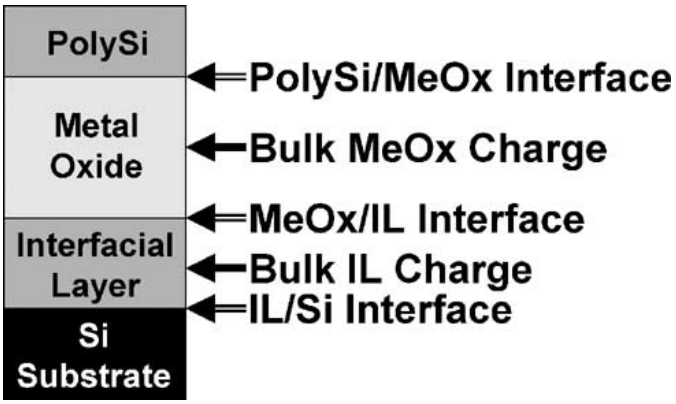


Figure 1.21 Location of charge to cause threshold voltage shift [105]

Non-ideal effects include four general types of charges related to dielectric-semiconductor MOS structure: fixed oxide charge, mobile oxide charge, oxide trapped charge, and interface trapped charge (Figure 1.22). The interface-trapped charges (positive or negative) are created due to structural defects, metal impurities, and are located at the dielectric-semiconductor interface and are in electrical communication with the semiconductor. The stretch-out of the experimental capacitance-voltage plot is indicative of the presence of interface traps while parallel shift indicates the presence of fixed oxide charge. Fixed oxide charges are positive near the dielectric-semiconductor interface, evolve from the oxidation process, and are not in electrical communication with the semiconductor. Oxide trapped charges (positive or

negative) are due to electrons or holes trapped in the dielectric. Mobile oxide charges (negative ions and heavy metals) are present due to ionic impurities [106]. Local non-stoichiometry or structural defects are responsible for the fixed charges.

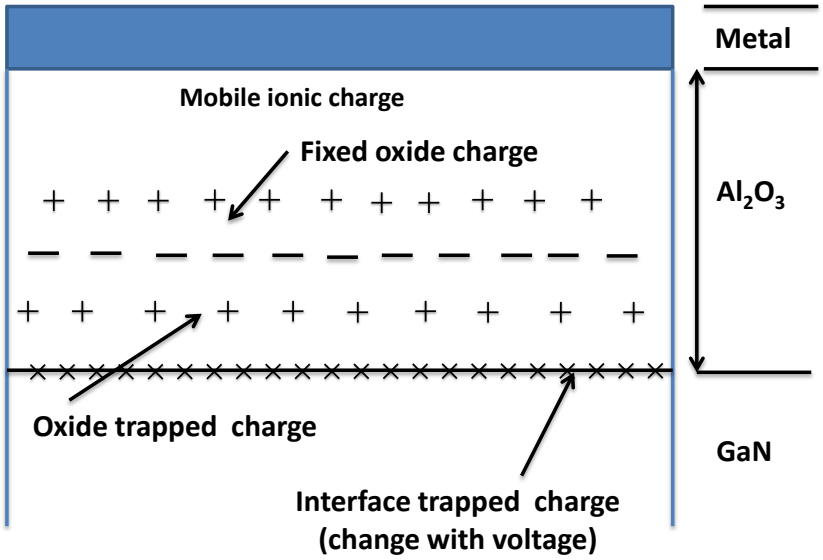


Figure 1.22 Location of oxide charges in MOS structure

Deposited high-κ dielectrics create defects at the dielectric/GaN interface. Interface defects can be investigated by observing the interface trap density distribution along the GaN bandgap. The factors responsible to the variation in D_{it} could be due to the dangling bond at the semiconductor surface, dielectric deposition condition and dielectric-semiconductor interfacial reactions. GaN surface treatment prior to dielectric deposition can minimize the dielectric-GaN interfacial defects.

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Chapter 2 - Influence of Atomic Layer Deposition Temperatures on TiO_2/*n*-Si MOS Capacitor

Abstract

This paper reports on the influence of deposition temperature on the structure, composition, and electrical properties of TiO_2 thin films deposited on *n*-type silicon (100) by plasma-assisted atomic layer deposition (PA-ALD). TiO_2 layers ~20 nm thick, deposited at temperatures ranging from 100 to 300°C, were investigated. Samples deposited at 200°C and 250°C had the most uniform coverage as determined by atomic force microscopy. The average carbon concentration throughout the oxide layer and at the TiO_2/Si interface was lowest at 200°C. Metal oxide semiconductor capacitors (MOSCAPs) were fabricated, and profiled by capacitance-voltage techniques. The sample prepared at 200°C had negligible hysteresis (from a capacitance-voltage plot) and the lowest interface trap density (as extracted using the conductance method). Current-voltage measurements were carried out with top-to-bottom structures. At -2 V gate bias voltage, the smallest leakage current was 1.22×10^{-5} A/cm^2 for the 100°C deposited sample.

2.1 Introduction

Titanium oxide thin films have many applications such as photocatalyst [1], solar cells [2], gate insulators [3], and dielectrics [4]. With the potential of achieving an extraordinarily high dielectric constant (up to 130 for rutile TiO_2 [5,6], 2000 for $SrTiO_3$ [7]), TiO_2 is also an appealing dielectric for capacitors in the dynamic random access memory (DRAM), the main memory device in modern computers. Since the capacity and performance of DRAM greatly affects the working speed of a computer, much attention has been given to optimize DRAM. As proposed by the International Technology Roadmap for Semiconductors (ITRS) [8], DRAM capacitors with higher capacitance, thinner equivalent oxide thickness (EOT) [9] and smaller leakage current density are highly desirable. The insulator deposition temperatures should be below 500°C, because capacitors are expected to be deposited after transistors formation [10]. However, further research on the high dielectric materials is needed to fulfill those requirements.

In the present study, plasma-assisted atomic layer deposition (PA- ALD) was employed to deposit thin insulating TiO_2 films, because it offers excellent atomic level control of layer thickness with good uniformity and conformality [11]. With an O_2 plasma, the deposition can be conducted at a lower temperature and with a shorter purge time in cold-wall reactors than a conventional thermal ALD system [12]. These characteristics are particularly suitable for growing capacitor dielectrics for use in DRAM, as it uses a three dimensional structure with a high aspect ratio to increase the effective surface area [13].

The present work reports on the impact of the deposition temperature on the properties of TiO_2 films prepared by PA-ALD and on the performance of said films in silicon MOSCAPs. By correlating the oxide structure, surface morphology and impurity concentration with electrical properties (hysteresis, interface trap density and leakage current), an optimal deposition temperature is identified.

2.2 Experimental

2.2.1 TiO_2 ALD Film growth and metal contact deposition

Before deposition, the *n*-type Si (100) substrates were cleaned with acetone and isopropyl alcohol (IPA) for 5 minutes at 40°C. TiO_2 was deposited by PA-ALD in an Oxford Instruments FlexAL ALD reactor with tetrakisdimethylamino titanium (TDMAT) kept at 39°C as the titanium precursor, and oxygen plasma as the oxidizing agent. The ALD growth temperatures were 100° C, 150° C, 200° C, 250° C and 300°C. All ALD depositions consisted of 400 cycles and each ALD cycle included a 0.4 second dose of TDMAT followed by a 4 second purge with Ar gas, and a 3 second exposure to the oxygen plasma followed by a 3 second purge. The plasma power and pressure during exposure was set to 400 Watts and 15 mTorr, respectively, with an O2 flow rate of 60 sccm. Circular capacitors (50–300 μm diameter) with Ni/Au (20/100 nm) metal contacts on top of the oxide were created by standard photolithography and E-beam evaporation methods. The current-voltage test structures consisted of the top capacitor contact and the bottom contact, which was bare silicon, held on the conductive measuring stage with constant vacuum pumping at the center of the sample.

2.2.2 TiO_2 Film characterization

The TiO_2 film morphology was measured by atomic force microscope (AFM, Digital Instrument MultiMode SPM from Veeco Instruments Inc) operating in tapping mode. Elemental compositions of the oxides were measured as a function of depth by X-ray photoelectron spectroscopy (XPS) with argon ion sputtering using a K-Alpha XPS from Thermo Scientific. The K- Alpha XPS uses monochromatic Al k-alpha X-rays to generate photo- electrons that pass through a double-focusing hemispherical electron energy analyzer onto a 128-channel detector. Depth profiling was carried out using 3 KV Ar-ions and set to a known sputtering rate for SiO_2, which is 6 nm/min, as calibrated on a SiO_2 standard.

The thickness and refractive index of the TiO_2 films was measured using a spectroscopic ellipsometry (alpha-SE model from J.A.Woollam Co. Inc.) at three incident angles, 65°, 70°, and 75°. The spectral range of the ellipsometry was from 380–900 nm (1.3– 3.25 eV), and measured

data were fitted with the Cauchy layer model [14] to determine the thickness of the ALD films.

The structure of the thin films was characterized by X-ray diffraction (XRD, PANalytical X'Pert Pro MPD) using a Cu-Kα radiation source. Measurements were taken over the range of 5–80° with a step size 0.0167° and a count time of 2 seconds. To avoid the high intensity peak of the Si (100) substrate, the samples were offset by 2° in omega.

C-V measurements were taken on the TiO_2/Si MOS capacitors using a Keithley 4200 semiconductor characterization system operating at 1 MHz at room temperature. To evaluate charge trapping in the oxide layers from the hysteresis behavior of the oxide, the bias was applied by sweeping the dc voltage back and forth between +10 V and −10 V at a sweep rate of 0.1 V/sec. The same results were obtained regardless of the sweep direction. The interface trap density, D_{it}, (at the oxide-dielectric interface) was determined by the ac conductance method[15] using an HP 4284A precision LCR meter, and conductance was measured from 20 Hz to 1 MHz with a long integration time at room temperature. The I-V measurements were taken by sweeping the voltage from +4 V to −4 V, and leakage current densities of each sample were compared at −2 V gate bias voltage.

2.3 Results and Discussion

The surface of the TiO_2 film deposited at 200°C was the most uniform, as it had the highest density of nucleation sites as determined by AFM. The next most uniform samples were those prepared at 250 and 300°C (Figure 2.1). By contrast, random, isolated islands formed at 150°C and 100°C, indicating a lower nucleation density at lower temperatures. The root mean square (RMS) surface roughness decreased with the growth temperature. Lee *et al.* [16] reported a similar trend for TiO_2 grown on amorphous Si by metal-organic chemical vapor deposition (MOCVD).

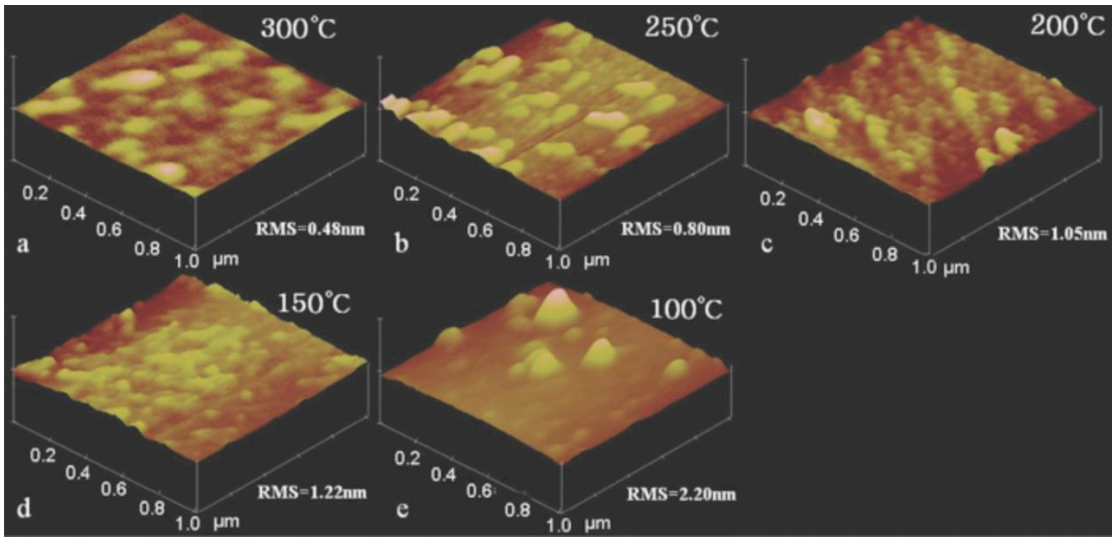


Figure 2.1 Three-dimensional AFM images of TiO_2 on Si deposited at different ALD temperatures. The Z height is 30 nm for all images. (a) 300°C (RMS = 0.48 nm), (b) 250°C (RMS = 0.80 nm), (c) 200°C (RMS = 1.05 nm), (d) 150°C (RMS = 1.22 nm), and (e) 100°C (RMS = 2.202 nm).

On all TiO_2 sample surfaces, nitrogen was detected by XPS. However, it disappeared after sputtering for 30 seconds, suggesting it was solely surface contamination. At the interface, silicon oxide was also observed. The average ratio of oxygen and titanium was calculated (Table 2.1) in the steady region in depth profile (Figure 2.2a). The sample deposited at 200°C had the O/Ti stoichiometry closest to 2/1 of TiO_2 followed by the 100 and 150°C samples. 250 and 300°C deposition temperatures lead to oxygen-rich titanium oxide films. The signal from the Ti 2p transition was also monitored in the depth profile (Figure. 2.2b). A single doublet, suggesting the presence of metallic titanium, was present at the oxide/Si interface for all samples, then disappeared away from the interface into the film. The observation of metallic titanium could be from the reduction during Ar+ sputtering. Carbon was detected throughout the oxide films. Figure 2.3 plots the average carbon concentration in the oxide layers as a function of the ALD deposition temperature. The minimum carbon concentration (2.6%) occurred at 200°C (Table 2.1).

Table 2-1 Oxygen and titanium ratio, average carbon concentration, thickness, dielectric constant of TiO_2 and calculated values of D_{it} for TiO_2/Si samples prepared at different ALD temperatures.

ALD temperature (°C)	0:Ti ratio	Average C concentration (%)	TiO_2 thickness (nm)	Dielectric constant	D_{it} (1×10^{13} eV^{-1} cm^{-2})
300	2.24	3.20	19.7	29.6	1.7-4.0
250	2.32	2.79	19.0	42.5	3.8-4.7
200	2.08	2.61	19.2	55.6	1.1-1.5
150	2.12	3.12	17.9	47.1	2.5-3.9
100	2.10	3.74	19.3	41.3	1.5-2.2

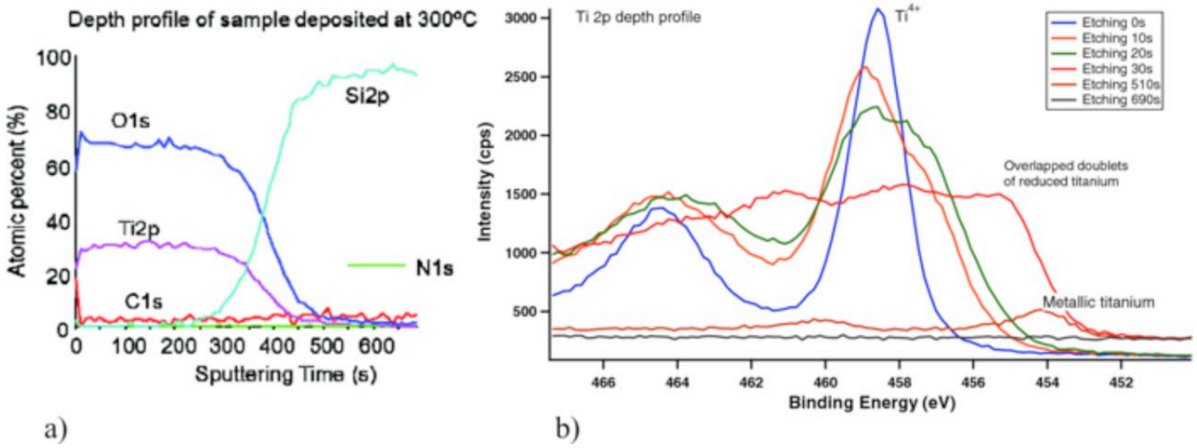


Figure 2.2 (a) XPS depth profile of sample deposited at 300°C. (The shape of the depth profile is similar for all the samples. Only one is demonstrated.)(b) XPS depth profile of Ti 2p at different sputtering times. The $2p^3$ of Ti^{4+} and metallic Ti peaks are 458.5 eV at 0 seconds and 454.2 eV at 510 seconds.

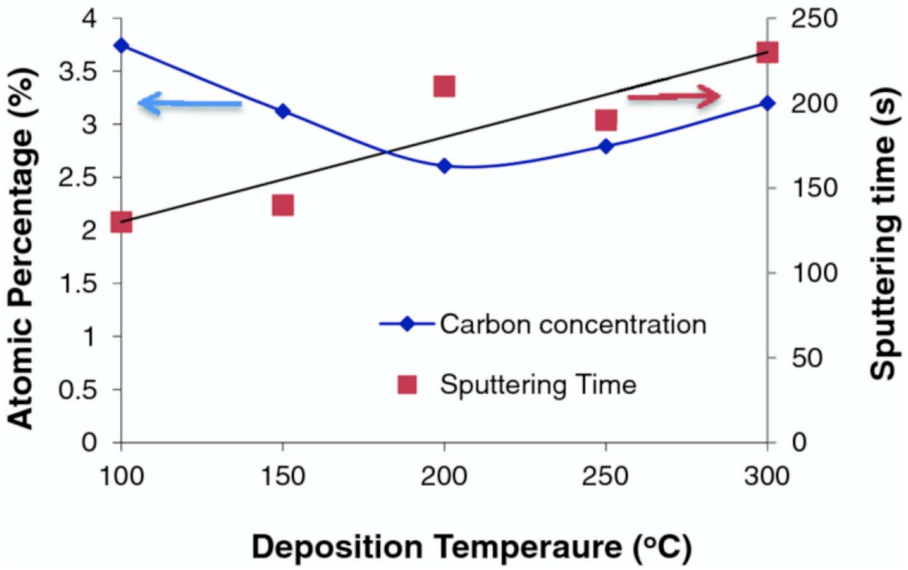


Figure 2.3 (Left axis) Average atomic carbon concentration in the TiO_2 layers versus ALD temperature. (Right axis) Sputtering time to remove the oxide layer and expose the Si substrate versus ALD deposition temperature.

The TiO_2 thickness was similar for all samples, 19 ± 1.2 nm (Table 2.1), as measured by ellipsometry. However, the time to sputter through the oxide layers increased with increasing deposition temperature (Figure 2.3). This suggests that the oxide film increased in density and was more resistant to sputtering as the deposition temperature was increased [17]. The TiO_2 films were amorphous, since no TiO_2 crystalline peaks were detected by X-ray diffraction.

The dielectric constant was calculated using the relationship $C = \varepsilon_r\varepsilon_0 A/d$, where C is the capacitance of the material, ε_r is dielectric constant, ε_0 is permittivity of free space and d is layer thickness. The TiO_2 and SiO_2 thin films were treated as capacitors in series, and it was assumed that the ε_r and thickness of SiO_2 are 3.9 and 1.9 nm respectively. The dielectric constant of TiO_2 (Table 2.1) was calculated from C-V plots using the equation:

$$\frac{1}{C_m} = \frac{1}{C_{TiO_2}} + \frac{1}{C_{SiO_2}} \qquad (1)$$

where C_m is the measured capacitance in the accumulation region. A wide range of ε_r for

amorphous TiO_2 [ε_r = 16–86] has been reported [18,19] and our values [ε_r = 29–56] were similar to those reported by Alexandrov *et al*. [18].

All TiO_2/Si samples had negligible hysteresis, similar to the observations of Fuyuki *et al*. [19] for TiO_2 grown on Si by chemical vapor deposition (CVD) between 200 and 400°C. For the 200°C sample, the oxide saturation capacitance (C_{ox}) was observed and the transition from accumulation to depletion region was sharp compared to the rest of the curves (Figure 2.4), which is indicative of having a better interface quality. At 250 and 300°C, a bump at approximately 1.0 V is seen in the C-V plot, due to drift in mobile charge[20]. At different bias voltages, the samples deposited at 100, 150 and 300°C did not show saturation of oxide capacitance (C_{ox}). An explanation of this phenomenon will require further examination.

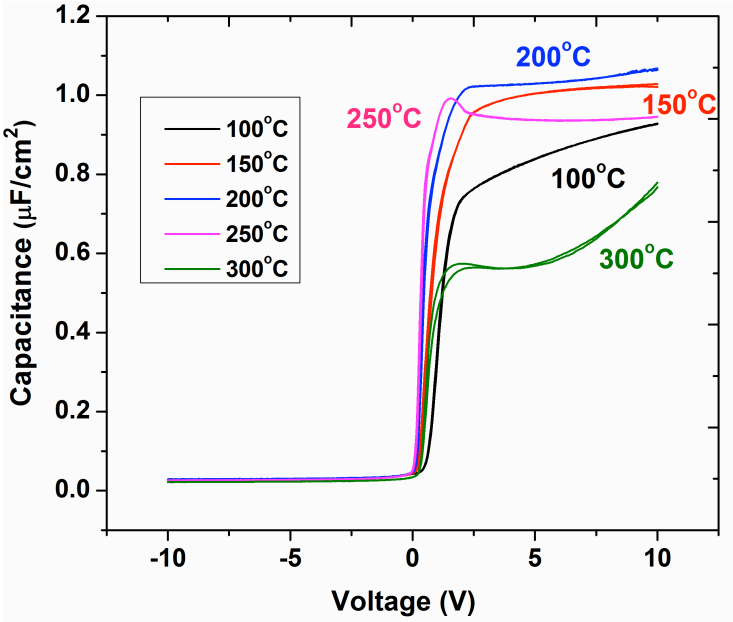


Figure 2.4 C-V measurement for TiO_2/Si MOS capacitors at different ALD temperatures.

To calculate D_{it} as a function of energy in the bandgap of Si, the series resistance and interface state conductance $G_P(\omega)$ were extracted as a function of angular frequency at a fixed voltage within the depletion region using an ac equivalent parallel circuit model as shown in Figure 2.5a. The parallel conductance (G_P) represents an energy loss due to interface traps and is a function of measured capacitance (C_m), angular frequency (ω), series resistance (R_s), measured

conductance (G_m) and oxide capacitance (C_{ox}). Capacitance and conductance data were corrected due to inclusion of series resistance. The series resistance was calculated using the equation 2

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{2}$$

Here G_{ma} and C_{ma} are the measured conductance and capacitance in the strong accumulation region respectively. Calculated values of R_s are similar to previously published results (i.e. 2000–2500 Ω) by Pakma *et al*. [21] Corrected capacitance, C_c, and corrected equivalent parallel conductance, G_c, are given by[15]

$$C_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) C_m}{a^2 + \omega^2 C_m^2} \tag{3}$$

$$G_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) a}{a^2 + \omega^2 C_m^2} \tag{4}$$

where a is given by

$$a = G_m - (G_m + \omega^2 C_m^2) R_s \tag{5}$$

G_P can be expressed after inclusion of corrected conductance and capacitance as

$$G_p = \frac{\omega^2 C_{ox}^2 G_c}{G_c^2 + \omega^2 \left(C_{ox} - C_c\right)^2} \tag{6}$$

The characteristic trap response time ($\tau = 2\pi/\omega$) is expressed by the Shockley-Read-Hall statistics of capture and emission rates by the following equation [22]:

$$\tau = \frac{\exp\left(\frac{\Delta E}{k_B T}\right)}{\sigma v_{th} D_{dos}} \quad (7)$$

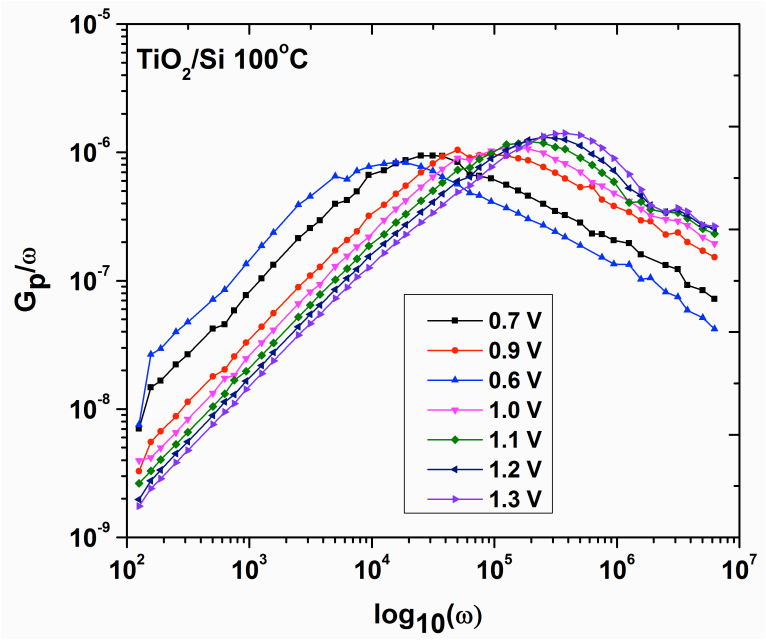
Here ΔE is the energy difference between the majority carrier band edge energy (E_{CB}) and the trap level E_T, k_B is the Boltzmann constant, v_{th} is the average thermal velocity of the majority charge carriers ($v_{th} = \sqrt{\left(3k_B T / m^*\right)} = 2.68 \times 107$ cm/s), D_{dos} is the effective density of states of the majority carriers ($D_{dos} = 2(2\pi m^* k_B T / h^2)^{3/2} = 2.07 \times 1018$ cm^{-3}), and T is the temperature. σ is the capture cross section of the trap (1×10^{-16} cm^{-2} [23]), which is assumed to be constant due to the dominance of the exponential term of Equation 7. Errors in the capture cross section by three orders of magnitude only made 0.18 eV energy difference within the bandgap of the semiconductor[24]. The trap level can be identified as the energy position from the frequency at which G_p/ω is maximum (Figure 2.5). Also, based on the maximum conductance from the measurement, an approximate equation to calculate interface trap density is given by [25]:

$$D_{it} = \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{\max} \quad (8)$$

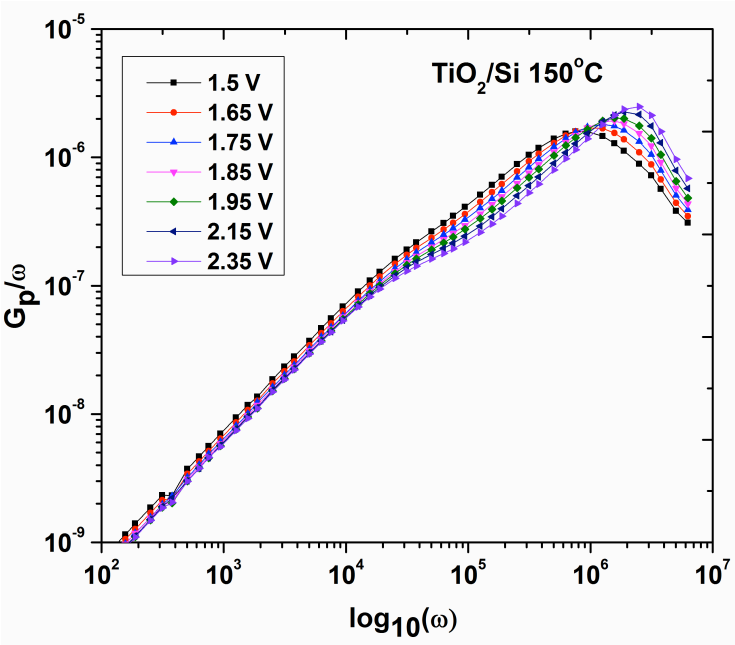
where A is the capacitor area.

The calculated values of interface trap density are on the order of 10^{13} $eV^{-1}cm^{-2}$ (Table 2.1) and are distributed between 0.09 eV to 0.18 eV energy range from the conduction band edge of the Si bandgap. They were similar to the results of Kumar *et al*. [26] in which a single value D_{it} = 1.2×10^{13} $eV^{-1}cm^{-2}$ was reported. The D_{it} distribution of the 200°C ALD sample is lower than that of the rest of samples (Figure 2.6b). Results also show that $qD_{it} > Cox$. In this case the conductance method becomes insensitive to the trap density and D_{it}, and it could be overestimated by an order of magnitude[27]. Figure 2.7 shows that the capacitance of the sample deposited under 200°C increases in the accumulation region when the frequency is decreased due to the effect of series resistance and localized interface states at the Si/TiO_2 interface [21].

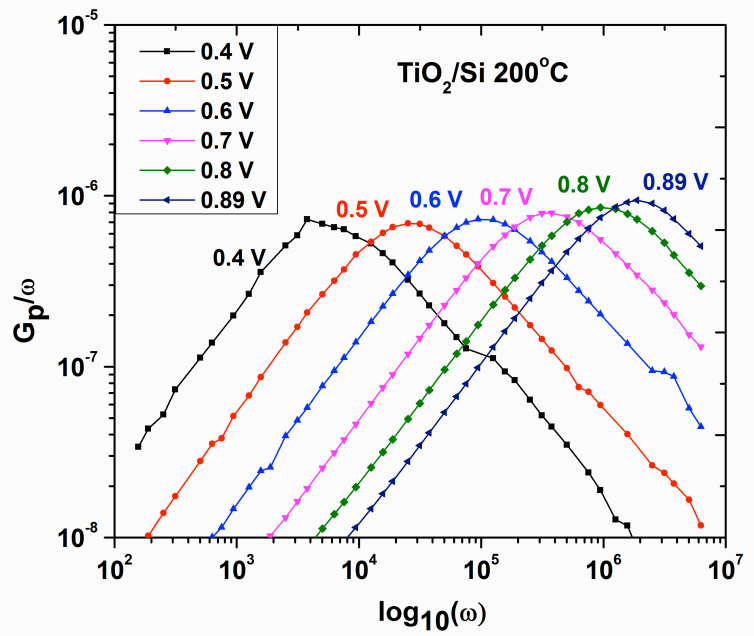
Similarly, the capacitance also increases in the depletion region with decreasing frequency due to recombination and generation from the interface states [28]. This frequency dispersion in C-V characteristics is negligible in the inversion region.



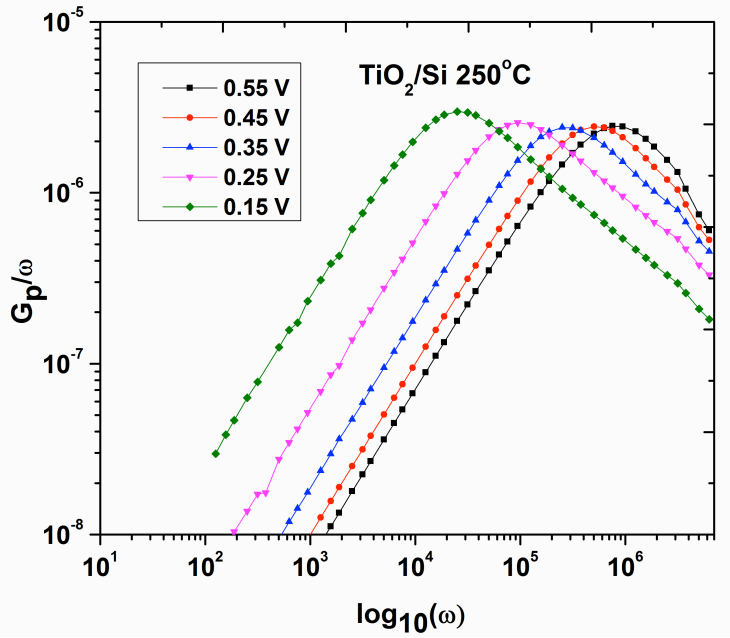
(a)



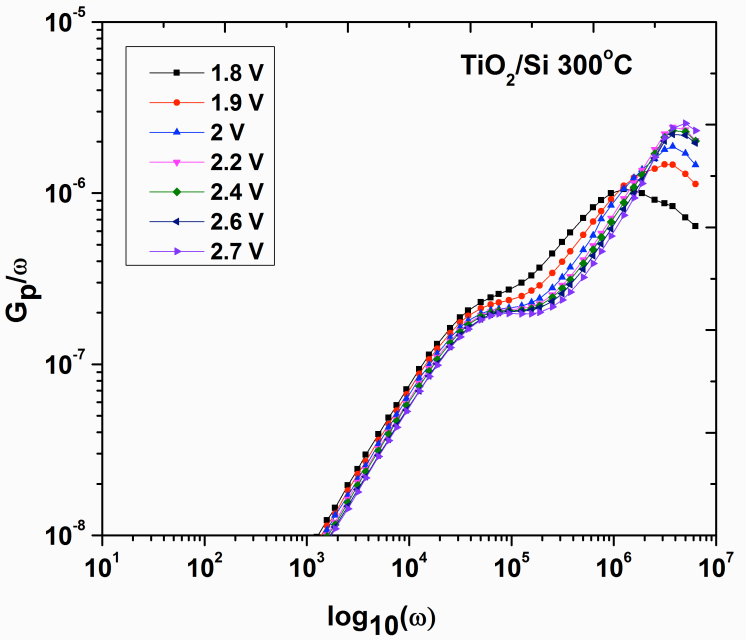
(b)


0.4 V
0.5 V
0.6 V
0.7 V
0.8 V
0.89 V
TiO2/Si 200°C
0.4 V
0.5 V
0.6 V
0.7 V
0.8 V
0.89 V
Gp/ω
log10(ω)

(c)

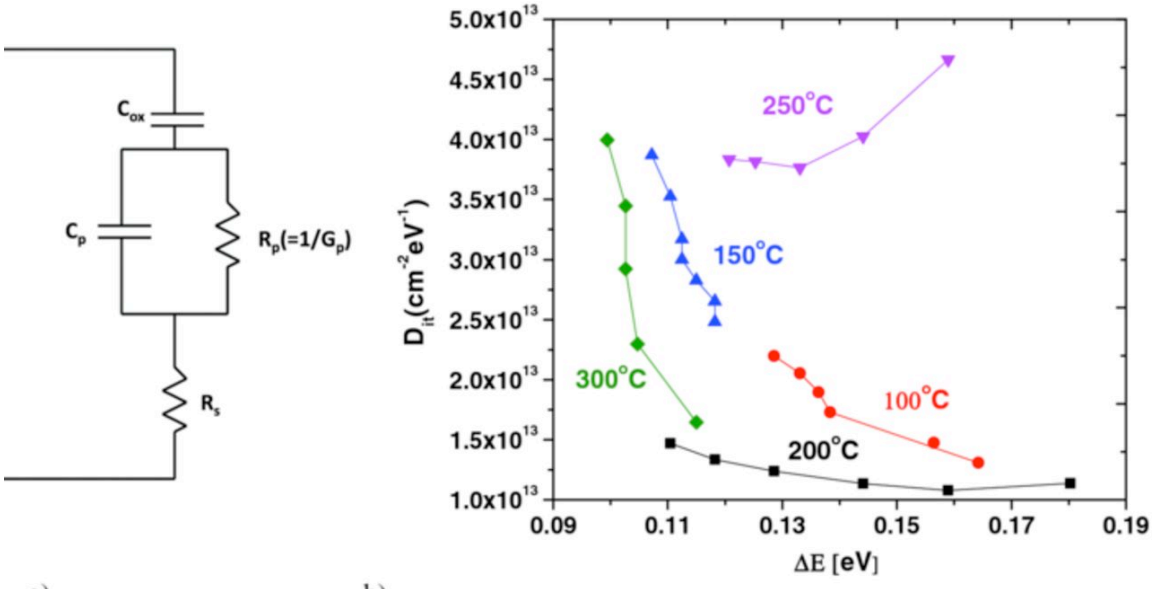

0.55 V
0.45 V
0.35 V
0.25 V
0.15 V
TiO2/Si 250°C
Gp/ω
log10(ω)

(d)



(e)

Figure 2.5 G_P / ω **versus** ω **as a function of gate voltage in the depletion region for TiO_2/Si MOS capacitors at (a) 100°C, (a) 150°C, (a) 200°C, (a) 250°C, and (a) 300°C.**



a) b)

Figure 2.6 (a) Simplified circuit of MOS capacitor including series resistance. (b) Interface trap density distributions of ALD samples at different deposition temperatures.

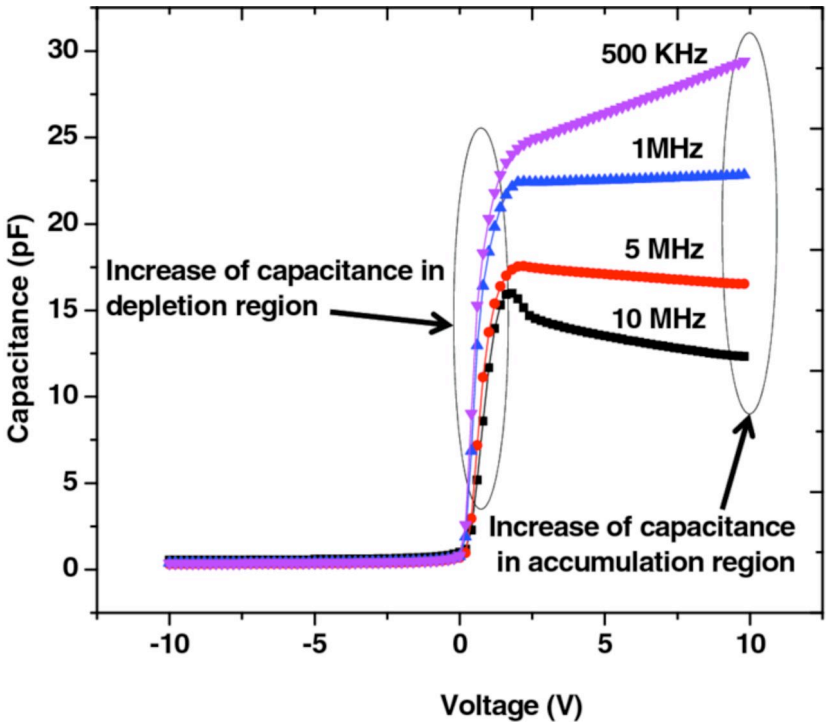


Figure 2.7 Measured capacitance vs gate voltage as a function of frequency for the TiO_2/Si at 200°C deposition temperature.

Figure 2.8 shows the current-voltage characteristics under positive and negative biases at room temperature for samples prepared at different ALD temperatures. The plots in figure 2.8 (semi-logarithmic scale) are linear at low gate bias voltages, but deviate from linearity at high voltages, which is attributed to the series resistance effect on the TiO_2 film [21]. The leakage current densities were on the order of 10^{-5}~10^{-4} A/cm^2 at −2 V, which is 2 orders of magnitude lower than that of the reactive sputtered TiO_2 film [58 nm] reported by Albertin *et al.* [29] and CVD grown TiO_2 film [20 nm] reported by Bae *et al.* [30].

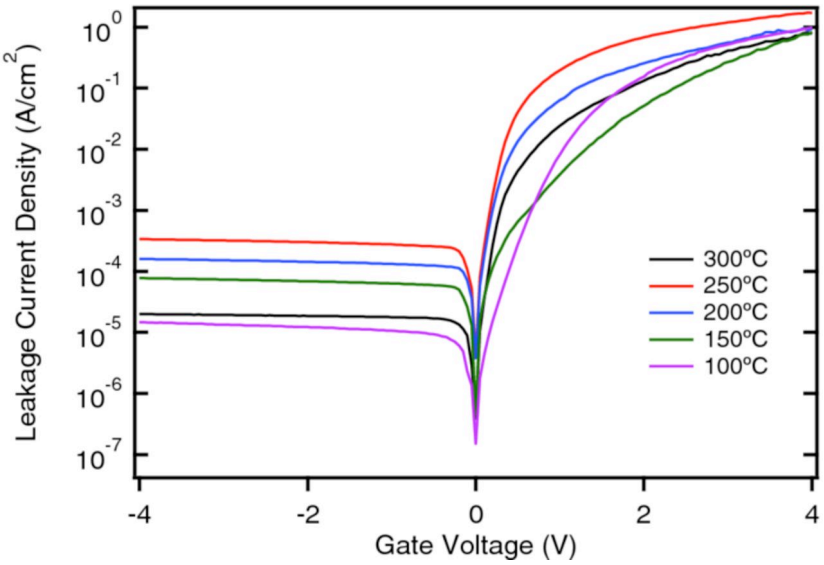


Figure 2.8 I–V characteristics of TiO_2/Si MOS capacitor at different ALD temperatures.

2.4 Conclusion

In this work, the influence of substrate temperature during plasma-assisted ALD on surface morphology, stoichiometry, impurity concentration and electrical properties of TiO_2/Si MOS capacitors is reported. Both surface morphology and roughness of the oxide layer were affected by the growth temperature. The impurity concentration at the oxide-silicon interface varied randomly with temperature. The TiO_2 dielectric constants are between 29 and 56, as obtained from C-V measurement, but the hysteresis in C-V plot did not change with temperature. The current density improved by two orders of magnitude compared to previous studies. Comparing the results of the TiO_2 film with different ALD temperatures, the optimal deposition temperature of TiO_2 is 200°C as this produces the highest dielectric constant, most uniform coverage and stoichiometry. This ALD temperature also has the lowest impurity concentration and lowest D_{it} at the interface, indicating a better quality sample. These results confirm that TiO_2 is a promising high k material for silicon devices.

2.5 Acknowledgments

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Chapter 3 - Effect of ALD growth temperature and GaN surface treatment on Al_2O_3/*n*-GaN MOS Capacitors

Abstract

The process conditions for fabricating Au/Ni/Al_2O_3/*n*-GaN (0001) MOS capacitors was optimized as a step toward realization of high performance GaN MOSFETs. The GaN surface preparations studied included cleaning with piranha (H_2O_2: H_2SO4 =1:5), $(NH_4)_2S$, and 30% HF etches. Al_2O_3 was deposited by atomic layer deposition at 240°C, 260°C, 280°C and 300°C. By several metrics, the MOS capacitor with the piranha etched GaN and Al_2O_3 deposited at 280 °C had the best characteristics. It had the lowest C-V hysteresis, the smoothest Al_2O_3 surface as determined by atomic force microscopy (AFM) (0.2 nm surface roughness), the lowest carbon concentration (~0.78%) at the Al_2O_3/*n*-GaN interface (from X-ray photoelectron spectroscopy), and the lowest oxide-trap charge ($Q_T = 1.59\times10^{11}cm^{-2}eV^{-1}$). Its interface trap density (D_{it}), as measured with photon-assisted capacitance-voltage method, had the lowest average interface trap density ($D_{it}= 3.73\times10^{12}cm^{-2}eV^{-1}$) from conduction band-edge to midgap.

3.1 Introduction

GaN based metal-insulator-semiconductor (MIS) structures; such as metal oxide semiconductor (MOS) capacitors are the basic building blocks of MOS field effect transistors (MOSFETs). High quality structures are essential to support large gate voltage swings, normally-off operation and high temperature operation with minimum gate leakage. A challenge to coupling high-k dielectrics with high mobility III-N semiconductors is its strong dependence on how the GaN surface in cleaned [1]. The surface chemistry of the GaN surface strongly affects the electrical properties of devices and therefore cleanliness of the GaN surface is a key factor [2]. Defects and impurities in GaN hinder its application in high-power-switching devices and high-brightness light-emitting diodes [3].

Gallium nitride is the semiconductor of choice for high power, high temperature, and high frequency electronic devices. GaN has a wide bandgap (3.43eV at 300K), high breakdown field, high electron mobility (in 2-D electron gas at AlGaN/GaN interface), thermal conductivity and radiation hardness that allows its transistors to operate at much higher temperatures and voltages compared to Si devices [4]. High electron mobility transistors (HEMT) have been the standard field effect transistor for GaN-based electronic devices, but this device suffers from a relatively high gate leakage current, since the gate metal is directly applied to the semiconductor [5,6]. A high permittivity metal oxide as gate insulator between the gate metal and the semiconductor rectifies this problem. In selecting the gate oxide, a band offset larger than 1 eV is needed to prevent undesirable leakage current [7]. In this respect, Al_2O_3 is an excellent high-κ dielectric, due to its high permittivity (8 –10), large bandgap (8.9 eV), and high energy conduction band edge offset with GaN (2.13 eV^2), which prevents current tunneling [8]. Al_2O_3/GaN structures can be used to constitute normally-off high voltage power switching device [9-11]. The deposition of oxides for gate dielectric applications is often performed by ALD because this method produces much better films than sputtering, electron beam evaporation, chemical vapor deposition or oxidation of pure Al films, due to its ability to control thickness on an atomic scale. This ability is achieved through the use of two separate, self-limiting surface chemical reactions that form each atomic layer in the binary oxide. Perfect 3D conformality, 100% step coverage and pinhole free films can be obtained by ALD [12]. The major obstacle to using high-k dielectrics deposited on III–V semiconductors is high-interface trap density (D_{it} >

10^{13} $cm^{-2}eV^{-1}$) created at the interface of III–V semiconductors [13]. These trap states are attributed to rough interfaces, incomplete and unsatisfied chemical bonds, and impurities.

This paper verifies the effectiveness of an *ex situ* wet chemical etching of GaN prior to ALD of Al_2O_3. Since the insulating dielectric must be deposited and is not produced by thermal oxidation, the most important cleaning requirement prior to the oxide deposition is to remove native oxides and carbon (and other) contamination while leaving the surface smooth. Therefore, reducing contamination (particulate, metallic and chemical) is extremely important to manufacture high performance semiconductor devices, as this prevents gate oxide breakdown, reduces contact resistance, minimizes MOS transistor threshold voltage shift, and maximizes peak mobility [14]. Nepal *et al.* [15] reported effects of GaN surface pretreatments prior to deposition of Al_2O_3 by atomic layer deposition at 240°C and 260°C. Studying various wet chemical treatment of GaN prior to ALD Al_2O_3 deposition, Nepal *et al.* found treating the GaN surface by piranha etching produced the lowest total trapped charge density and smoother Al_2O_3 films. Their findings motivated our study, which was initiated to find the best Al_2O_3 deposition temperature by ALD, and to investigate the effect of surface pretreatment on average density of all oxide trapped charge as well as Al_2O_3/GaN interface trap density. The interface trap density (D_{it}) is the areal density of electrically active defects per unit energy along GaN bandgap at the Al_2O_3-GaN interface [2]. Al_2O_3-GaN interface traps (fast states) are electrically linked to GaN and demonstrate fast response to dc bias sweep. On the other hand, oxide traps (slow states) exhibit quantum mechanical tunneling by transfer of charge through the oxide-semiconductor barrier [16,17].

In addition to the Nepal et al. study, GaN surface cleaning has been studied by a number of other researchers. Machuca *et al.* [18] used wet etching in H_2O_2:H_2SO_4 (1:4) to reduce surface carbon and oxygen concentrations and followed this by annealing at ultrahigh vacuum ($\leq 10^{-10}$ Torr) at 700°C to desorb carbon and oxygen. Lee *et al.* [14] found UV/O_3 exposure can remove residual carbon contamination from photolithography process and residual chlorine or fluorine after surface acid treatment. HF solutions remove native oxides from GaN and passivate its surface by binding the exposed dangling bonds with hydrogen [19]. Also, HF-based solutions have been shown to remove both carbon and oxygen from the GaN surface [20]. $(NH_4)_2S$ effectively eliminates native oxide and protects GaN surface from immediate re -oxidation by creating Ga-S

monolayer [21].

In this study, various wet-etching methods were used to clean the GaN surface, and the effects of these methods were investigated on the electrical properties of Al_2O_3/GaN MOS capacitors after determining the best temperature for depositing Al_2O_3 on GaN by atomic layer deposition. The concentrations and energies of defects (oxide-trap charge and interface trap charge) were quantified as functions of process parameters, to provide guidance for improving the reliability of MOS devices.

3.2 Experimental details

Ga-polar *c*-plane wurtzite GaN epilayers on sapphire were employed for the fabrication of Al_2O_3/*n*-GaN MOS capacitors. The epilayers consisted of 1.5μm thick Si-doped, *c*-plane GaN grown on *a*-plane sapphire via metal organic chemical vapor deposition (MOCVD), using a 25 nm thick AlN buffer layer. The GaN epilayers were deposited at 1050°C, 150 Torr, using a V/III ratio of 3500. The precursors for the GaN epilayers were trimethylgallium and ammonia. Doping, on the level of $1x10^{18}$ cm^{-3}, was achieved through the addition of silane.

Total eight samples were fabricated with different process conditions. For the first four samples, the same GaN surface cleaning procedure was used and for the rest of the four samples different GaN surface cleaning procedure was followed.

To investigate the impact of the ALD temperature, four samples were fabricated where all GaN surfaces were cleaned first with HF, followed by SC1 (NH_4OH (28%), H_2O_2 (30%) and DI water=1:1:5) at 70°C prior to oxide deposition. The temperature for Al_2O_3 deposition on *n*-type GaN (0001) was varied, to determine its effects. Al_2O_3 was deposited by ALD at 240°C, 260°C, 280°C and 300°C. Al_2O_3 was deposited by ALD using trimethylaluminum (TMA) and deionized water in a Cambridge NanoTech Savannah 200 ALD System. Ultrahigh purity nitrogen (99.999 %) flowing at 20 sccm was the carrier gas for the precursors. An ALD cycle consisted of a 0.015 s TMA pulse followed by a 20 s purge with N_2; and a 0.015 s pulse of deionized water followed by a 20 s purge. The 20 s purging step with ultrahigh purity nitrogen between precursor exposure is intended to remove unreacted precursors and reaction by-products from the ALD chamber and thereby ensure a true ALD mode (self-limited surface reaction

limited). A total of 250 ALD cycles were employed. For all of these samples, the Al_2O_3 thickness was approximately 20 nm.

The second objective of this study was to investigate the impact of the GaN surface cleaning and for this purpose four additional samples of *n*-type GaN were used. Three samples were cleaned using piranha (H_2O_2: H_2SO4 =1:5), $(NH_4)_2S$, and 30% HF, and the fourth sample was left untreated. During the process of photolithography circular capacitors of four different sizes (50µm, 100µm, 150µm and 300µm) were created. Ni/Au (20nm/100nm) metal contacts were deposited by e-beam evaporation. A schematic of single MOS capacitor is shown in figure 3.1 with top to top contact.

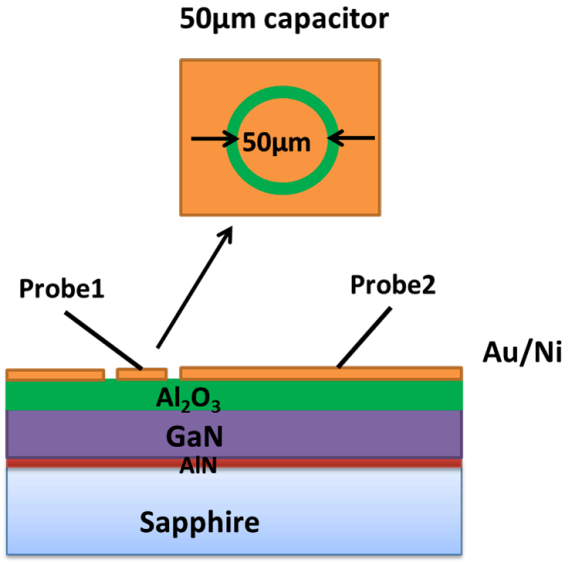

Figure 3.1 Schematic showing position of only one capacitor in a sample.

The Al_2O_3/GaN MOS capacitors were electrically characterized by capacitance-voltage (C-V) measurements at room temperature at 1MHz with a bias range of 3V to -8V. The most commonly used high frequency for C-V measurement is 1MHz and was used in this study so that at high frequency trap states cannot follow the applied ac signal [22,23]. C-V hysteresis was used to quantitatively study the MOS capacitors and was quantified by the shift in flatband voltage. For hysteresis measurements, the MOSCAPs were swept from zero voltage to the accumulation region (+3V), followed by immediate voltage sweep from accumulation to deep depletion (-8V) and deep depletion to accumulation region (+3V). Flatband capacitance was (C_{FB}) [22] obtained at

each voltage sweep to locate the flatband voltage (V_{FB}) from C-V plot according to equation (1).

$$C_{FB} = \frac{\varepsilon_s C_{ox}}{C_{ox}\lambda + \varepsilon_s} \tag{1}$$

where ε_s is the permittivity of GaN, C_{ox} the oxide capacitance at accumulation and λ is the Debye length expressed by

$$\lambda = \sqrt{\frac{\varepsilon_s kT}{q^2 N_D}} \tag{2}$$

where N_D is donor concentration in the GaN and q is electron charge. The average density of all trapped electrons along the GaN bandgap (E_g) was obtained from C-V hysteresis using the following equation (3)

$$Q_T = \frac{C_{ox}\Delta V_{FB}}{E_g} \tag{3}$$

In high frequency C-V measurement, interface traps do not follow ac gate voltage but respond to slow change in dc gate bias, which causes the high frequency C-V plot to stretch out along the dc gate voltage axis [22]. Bae *et al.* [24] performed C-V measurement on Al_2O_3/GaN structure by ramping the gate voltage sweep rate from 40 to 150 mV/s and observed no significant difference in C-V profile. In this study, a sweep rate of 100 mV/s was applied for most of the C-V measurement using Keithley 4200 semiconductor characterization device. Only 50 mV/s sweep rate was applied for the C-V hysteresis measurement of GaN surface treated with piranha, HF, $(NH_4)_2S$ and the untreated samples.

For GaN at room temperature, the thermal generation rate of electron-hole pairs is insignificant [25]. Thus, GaN exhibits deep depletion in C-V plots due to the low minority carrier

(holes) generation rate at room temperature; an inversion layer is not formed within the time frame of practical C-V measurements. According to Shockley-Read-Hall statistics, the emission time constant increases exponentially with distance from GaN band edge and, as a result at room temperature, electrons captured deep in the bandgap of GaN cannot emit to the conduction band [26]. Surface states may not be estimated at room temperature by the Terman or conductance technique because electrons are unavailable to be captured in inversion region. Consequently, photon-assisted [27,28] or high temperature C-V is needed to estimate the interface trap density. From C-V measurements at higher temperatures (up to 400°C, if leakage currents is not too large) the defects energies that are deep within the bandgap can be estimated.

In this study, the photon-assisted high frequency capacitance voltage procedure developed by Swenson [28] was applied to measure interface state density. Liu *et al.* [17] determined interface trap density using photon-assisted method to study effects H_2O pretreatment during ALD of Al_2O_3 on GaN. During photon-assisted method, exposure to UV light shifts the deep depleted region of the Al_2O_3/GaN C-V plot to inversion. Here the key factor is the leakage current coming from the gate in depletion mode causing interface states to ionize. A Hamamatsu lightning curing system, LC-L1was used as the monochrome (365nm) UV light source (photon flux 2×10^{19} photon/s.cm^2). If the C-V plot were in inversion instead of deep depletion, then any interface states that ionized would almost immediately capture inversion electrons. In this procedure, first the dark C-V plot was obtained by sweeping the dc voltage at 100 mV/s from deep depletion to the accumulation region under complete darkness at 1MHz. Next, a monochromatic ultraviolet (UV) light source with 365 nm wavelength was illuminated directly on the sample and bias was applied for a hold time of 8 minutes at -3 volts (pre-soak voltage at deep depletion). Immediately a second before completion of the hold time, UV light was turned off and dc voltage was swept from deep depletion to accumulation region (-3V to 8V) at dc voltage sweep rate of 100 mV/s. The ideal C-V plot was obtained by shifting the dark curve by the difference in built-in potential between dark C-V plot and post-UV C-V plot [29]. This difference in built-in potential includes interface state and fixed charge in Al_2O_3. dV is the voltage difference at a constant capacitance between the ideal C-V plot and the post-UV C-V plot and it is proportional to the interface state charge. Assuming constant GaN doping concentration, the amount of bend bending or semiconductor surface potential, was determined using equation (4).

$$\psi_s = \frac{q\varepsilon_s\varepsilon_0 \overline{N}_d A^2}{2C_{sc}^2} \tag{4}$$

Here $\overline{N}_d$ is the average doping concentration, and C_{sc} is the depletion capacitance. D_{it} was obtained using equation (5)

$$D_{it} = \frac{C_{ox}}{qA}\left(\frac{d\Delta V}{d\psi_s}\right) \tag{5}$$

The depletion capacitance C_{sc} is expressed by equation (6)

$$C_{sc} = \frac{C_{ox}C_m}{(C_{ox} - C_m)} \tag{6}$$

The electrical performance attributes of the Al_2O_3/GaN MOS capacitors were connected to the physical and chemical properties of the devices. Assessment of the Al_2O_3 surface roughness as a function of topography was done by atomic force microscope (AFM, Digital Instrument MultiMode SPM from Veeco Instruments Inc.) operating in tapping mode. Identification of Al_2O_3 surface contaminants and their relative concentrations were measured as a function of depth by x-ray photoelectron spectroscopy (XPS) with argon ion sputtering using a K-Alpha XPS from Thermo Scientific.

3.3 Results and Discussion

The C-V hysteresis plots (Figure 3.2) of four samples prepared at different temperatures showed that the Al_2O_3 deposited at 280°C exhibited the least hysteresis (0.23 V) at a sweep rate of 100mV/s. The small shift in flatband voltage and small hysteresis window is indicative of low interface trap density. Samples with Al_2O_3 deposited at 240°C, 260°C and 300°C showed 0.35 V, 0.33 V and 0.32 V hysteresis, respectively. The flatband voltage shift was towards the positive voltage in the C-V plots (forward sweep), which is due to the acceptor like interface electron

traps [30]. The lowest average density of all trapped electrons ($Q_T = 1.25\times10^{11}cm^{-2}eV^{-1}$) occurred in the sample deposited at 280°C (Table 3.1). Therefore, it was concluded that 280°C was the best temperature to deposit Al_2O_3 on GaN by ALD.

Table 3-1 C-V characteristics showing effect of ALD deposition temperatures

ALD deposition temperature of Al_2O_3/GaN sample	Hysteresis at flatband voltage (ΔV_{FB})	Average density of all trapped electrons, Q_T ($cm^{-2}eV^{-1}$)
240°C	0.35	1.75×10^{11}
260°C	0.33	1.51×10^{11}
280°C	0.23	1.25×10^{11}
300°C	0.32	1.33×10^{11}

Subsequently for the next four samples, the Al_2O_3 was deposited at 280°C but the GaN surface was treated with different processes. As seen from Figure 3.1, the GaN surface cleaned with the piranha solution showed the least hysteresis (0.25 V). The C-V hysteresis for $(NH_4)_2S$ and HF etched MOS capacitors were 1.22 V, 1.36 V, respectively. The lowest average density of all trapped electrons ($Q_T = 1.59\times10^{11}cm^{-2}eV^{-1}$) occurred with the piranha etched sample (Table 3.2). It was not possible to perform a voltage sweep of more than 1 volt with the untreated MOS capacitor as the capacitance appeared to decrease sharply beyond 1 volt due to dielectric breakdown and was not quantified due to its different dc voltage sweep range.

Table 3-2 C-V characteristics showing effect of GaN surface treatment

GaN surface treatment	Hysteresis at flatband voltage (ΔV_{FB})	Average density of all trapped electrons, Q_T ($cm^{-2}eV^{-1}$)
$(NH_4)_2S$	1.22	1.07×10^{12}
HF	1.36	9.21×10^{11}
Piranha	0.25	1.59×10^{11}
Untreated GaN	-	-

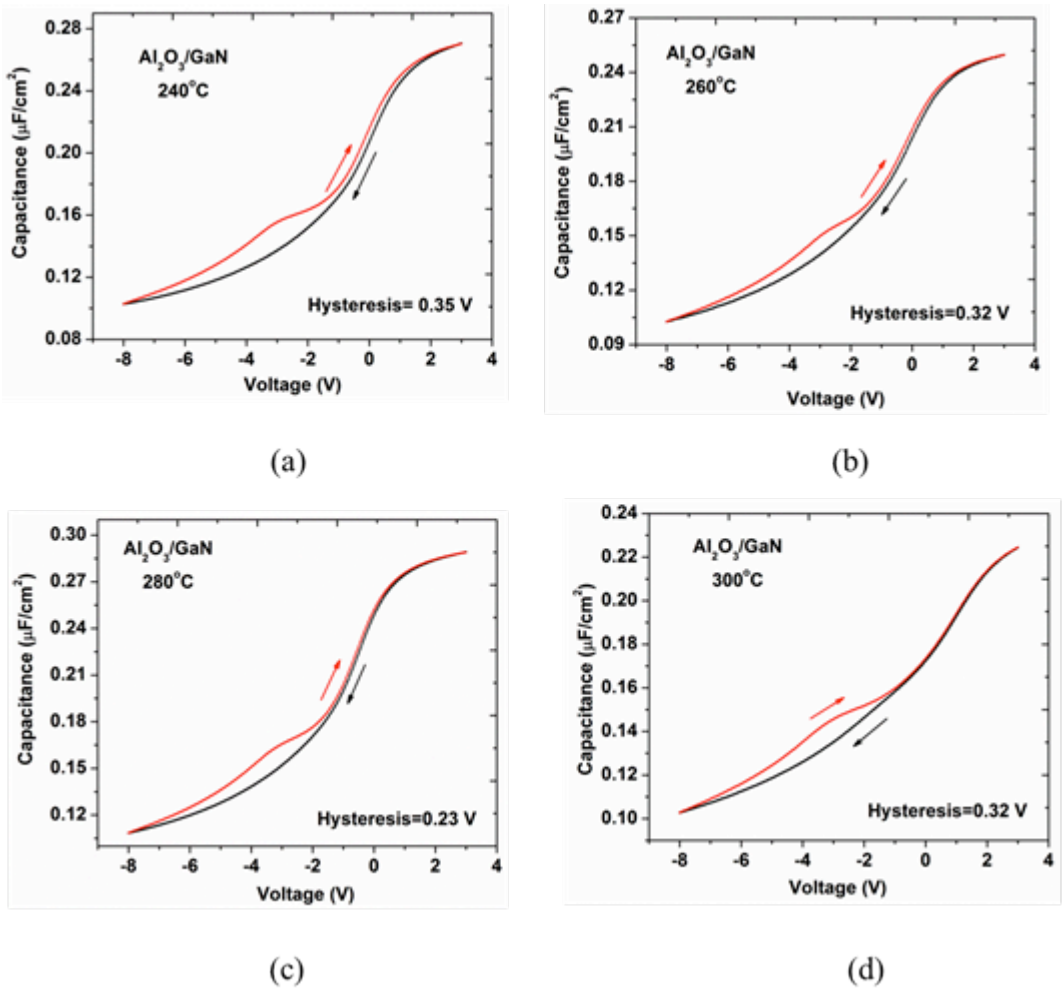

Figure 3.2 Hysteresis of C-V plots at 1MHz of Al_2O_3/GaN MOS capacitors at (a) 240°C, (b) 260°C, (c) 280°C and (d) 300°C ALD temperatures.

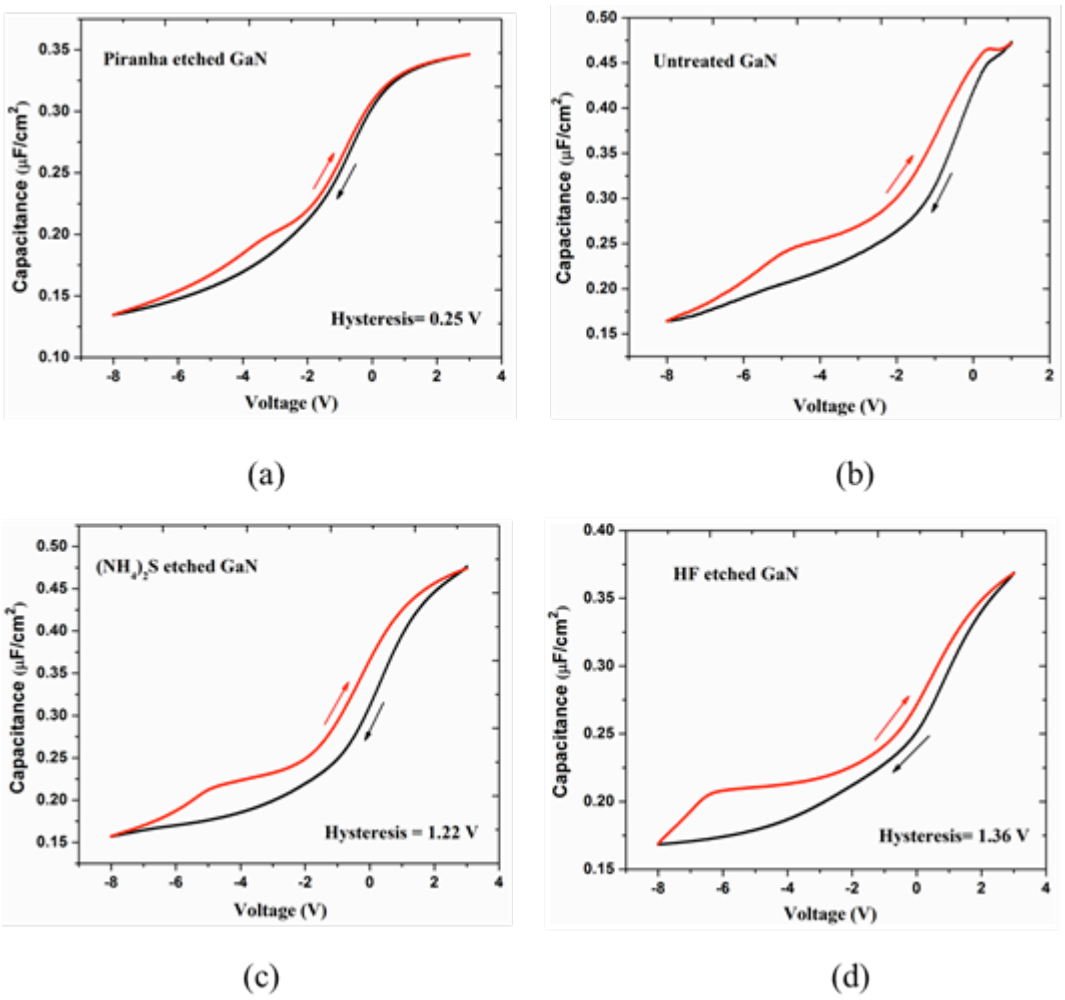

Figure 3.3 Capacitance-voltage hysteresis plots of Al_2O_3/GaN for (a) piranha, (b) no treatment, (c) $(NH_4)_2S$, and (d) 30% HF surface treatments at 280°C ALD deposition temperature.

AFM results showed that the piranha etched GaN surface produced the smoothest Al_2O_3 surface with minimum roughness (RMS =0.2nm). The surface roughness of $(NH_4)_2S$, HF, and untreated samples exhibited higher roughness as shown in Figure 3.4. For comparison, when Nepal *et al.*[15] deposited Al_2O_3 on GaN at 260°C, their Al_2O_3 surface roughness was 0.37 nm for the piranha etched GaN surface.

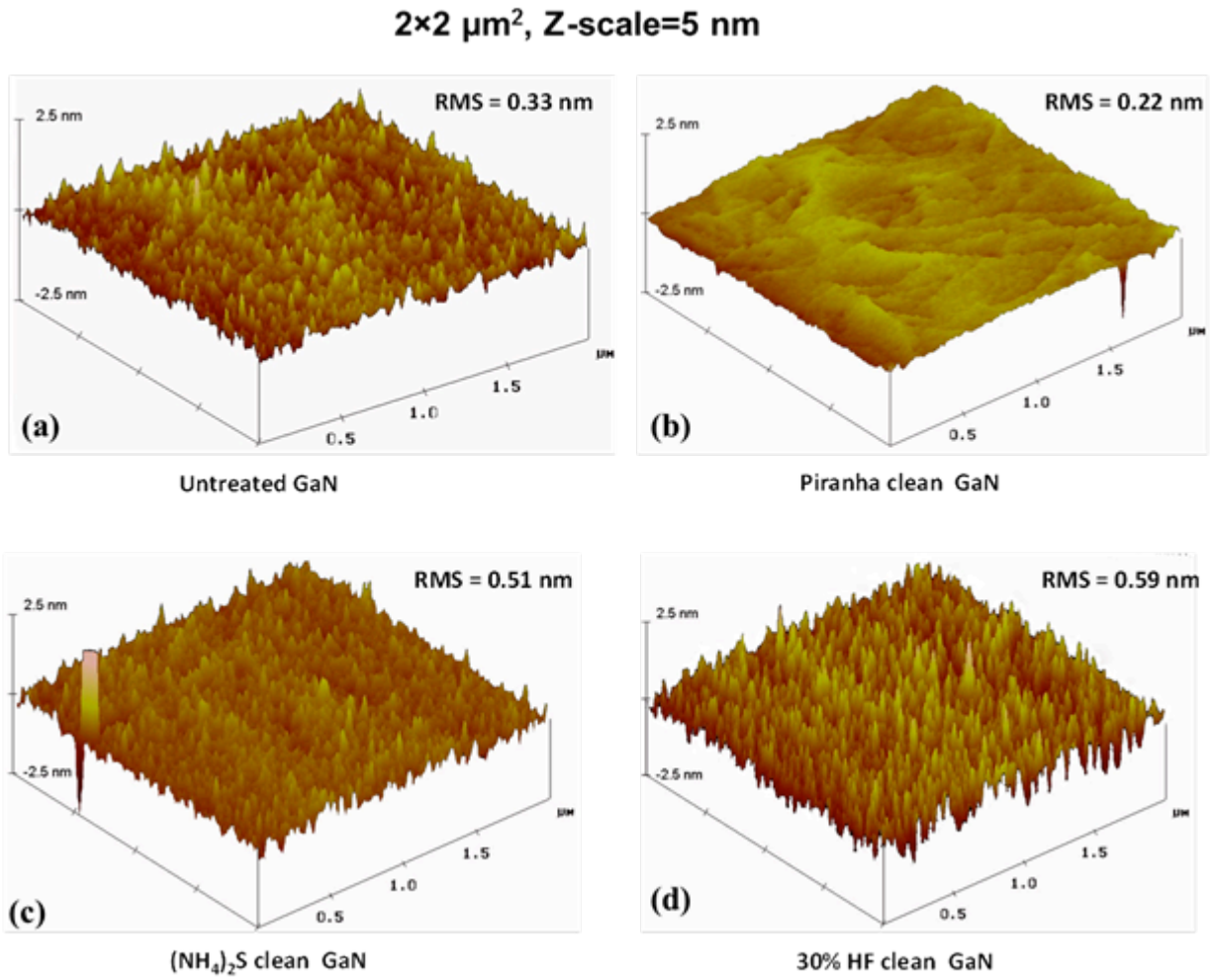

Figure 3.4 Atomic force microscopy images of Al_2O_3 where GaN surface pretreated with (a) no treatment, (b) piranha, (c) $(NH_4)_2S$, and (d) 30% HF before deposition of Al_2O_3.

Atomic carbon concentration was obtained for GaN surface treated samples from XPS depth profile, which attributes to residual ALD precursors not atmospheric contamination. XPS results showed that minimum carbon concentration was found for piranha treated sample and at the Al_2O_3/GaN interface compared to rest of the samples (Table 3.3). For piranha treated sample, the average atomic concentration of carbon was 0.78% at Al_2O_3/GaN interface and 0.20% in oxide.

Table 3-3 XPS analysis showing atomic percentage of carbon concentration in oxide and at Al_2O_3/GaN interface

GaN surface treatment	Carbon concentration in oxide (%)	Carbon concentration at interface (%)
$(NH_4)_2S$	0.60	4.14
HF	0.32	3.75
Piranha	0.20	0.78
Untreated GaN	0.55	4.27

During photon-assisted high-frequency capacitance-voltage characterization, it was observed that there is a shift of the deep depletion to inversion in the C-V plot due to the exposure of UV light. This shift to inversion region is highest for piranha treated sample (Figure 3.5a) and can be attributed to the generation of minority carriers in excess of the thermal equilibrium concentration. For the untreated GaN sample (Figure 3.5b), the C-V plot did not recover from deep depletion, and the voltage sweep of the post-UV C-V plot did not proceed beyond 0.5V due to oxide breakdown in the capacitor. From Figure 3.6, the minimum average D_{it} values from band-edge to midgap occurred with the piranha etched sample (D_{it}= $3.73\times10^{12}cm^{-2}eV^{-1}$). The average D_{it} for $(NH_4)_2S$, HF, and untreated samples were $8.07\times10^{12}cm^{-2}eV^{-1}$, $1.21\times10^{13}cm^{-2}eV^{-1}$ and $1.75\times10^{13}cm^{-2}eV^{-1}$ respectively. The distribution of D_{it} for piranha and $(NH_4)_2S$ etched samples were very similar but for piranha D_{it} was relatively constant between 1-2 eV from the conduction band edge. For the untreated sample, the D_{it} distribution was not observed beyond 0.6 eV from the conduction band of GaN, and this is attributed to the depletion capacitance extracted from figure 3.5b using equation (6).

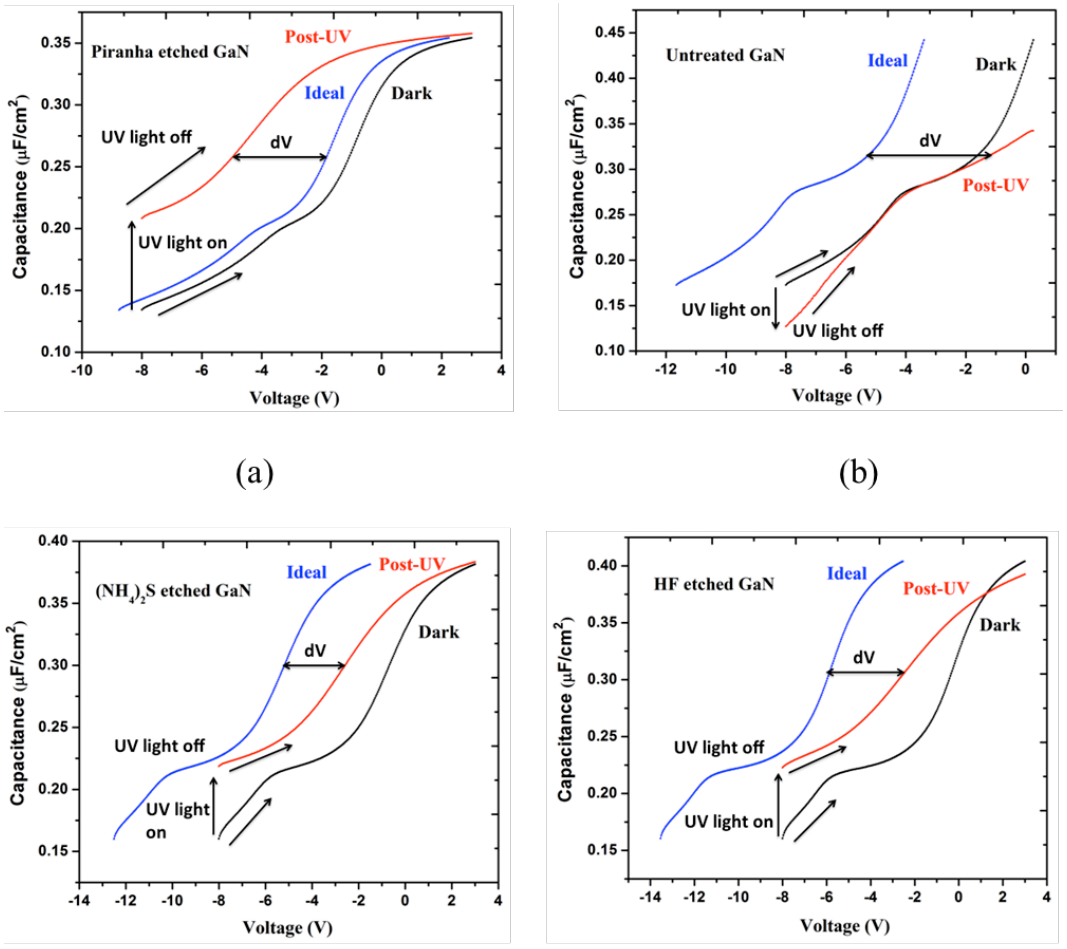

Figure 3.5 C-V plots measured at dark, post-UV exposure and ideal C-V plot for MOS capacitors with (a) piranha, (b) untreated (c) $(NH_4)_2S$, (d) 30% HF etched GaN surface before oxide deposition.

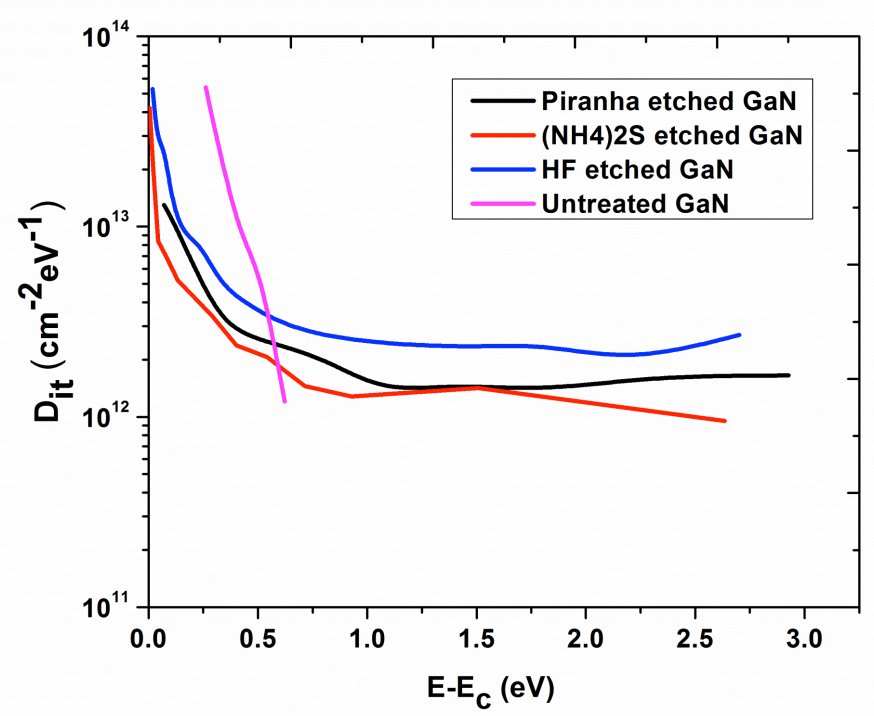

Figure 3.6 Plots of D_{it} ($cm^{-2}eV^{-1}$) vs. energy (eV) from the conduction band (E_c) of Al_2O_3/GaN for no treatment, 30% HF, $(NH_4)_2S$, and piranha surface treatments.

In addition, frequency dependent (10 kHz to 1MHz) C-V measurement were done for piranha, HF, $(NH_4)_2S$ and untreated samples. Frequency dispersion was observed in the accumulation regions for all samples; and, capacitance was found to increase with decreasing frequency, which is attributed to the series resistance effect [31]. Piranha treated sample showed the least dependence on frequency (Figure 3.7b.).

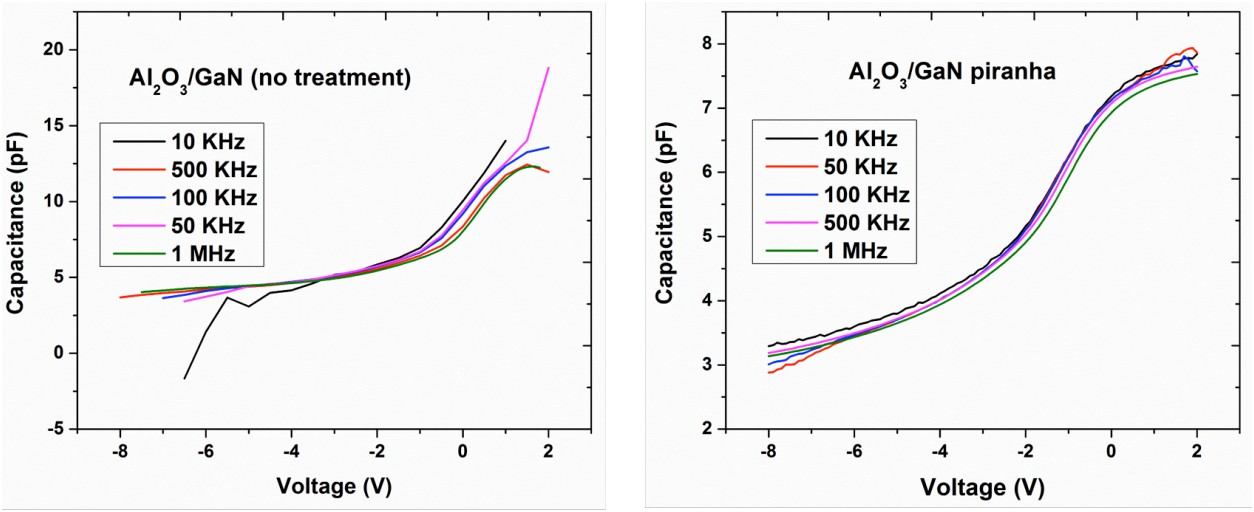

Figure 3.7 Least frequency dispersion in piranha treated sample (b)

3.4 Conclusion

This study is concerned with developing the best electrically performing ALD Al_2O_3/GaN interface. It was found that 280°C was the best temperature to deposit Al_2O_3 by ALD. Further, a study of the best treatment of the GaN surface revealed that the piranha treated GaN surface exhibited the lowest hysteresis; and, as a result lowest average density of trapped electrons was found. Photon-assisted high frequency C-V method was used to quantify interface trap density. The average interface trap density (D_{it}= $3.73\times10^{12}cm^{-2}eV^{-1}$) along the bandgap of GaN was minimum for piranha cleaned GaN sample compared to the samples treated with $(NH_4)_2S$, HF, and untreated sample. These electrical characteristics were strongly supported with the findings from surface morphology where minimum interface carbon concentration and smoothest GaN surface were also observed with the piranha cleaned GaN sample.

3.5 Acknowledgements

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Chapter 4 - Insulating gallium oxide layer produced by thermal oxidation of gallium-polar GaN

Abstract

The benefits of dry oxidation of *n*-GaN on sapphire for the fabrication of metal-oxide-semiconductor structures are reported. GaN thin films grown on sapphire by MOCVD were thermally oxidized for 30, 45 and 60 minutes in a pure oxygen atmosphere at 850°C to produce thin, smooth GaO_x layers. The GaN sample oxidized for 30 minutes had the best properties. Its surface roughness (0.595 nm) as measured by atomic force microscopy (AFM) was the lowest. Capacitance-voltage measurements showed it had the best saturation in accumulation region and the sharpest transition from accumulation to depletion regions. Under gate voltage sweep, capacitance-voltage hysteresis was completely absent. The interface trap density was minimum (D_{it} 2.75×10^{10} $cm^{-2}eV^{-1}$) for sample oxidized for 30 mins. These results demonstrate a high quality GaO_x layer is beneficial for GaN MOSFETs.

4.1 Introduction

Having proven to be a valuable semiconductor for optoelectronic devices (light emitting diodes and laser diodes emitting at blue and UV wavelengths), gallium nitride is now being developed for high power, high frequency transistors [1,2]. GaN based devices are attractive in microwave power amplifiers, RADAR, satellite communication, and hybrid electric vehicles. For these applications, gallium nitride (GaN) is combined with high-κ dielectrics to create a high performance metal-oxide semiconductor field-effect transistor (MOSFET) and metal oxide semiconductor high electron mobility transistors (MOSHEMTs). An insulated gate reduces leakage current and thus power consumption. This has typically been accomplished by depositing various gate dielectrics such as SiO_2, TiO_2, HfO_2, Al_2O_3, Si_3N_4, La_2O_3, and Ga_2O_3. However, deposited dielectric films that are not native to the semiconductor typically contain high impurity concentrations from the deposition source used, and they suffer from a high-interface trap density ($D_{it} > 10^{13}$ $cm^{-2}eV^{-1}$) [3]. These trap states are attributed to rough interfaces, incomplete and unsatisfied chemical bonds, and impurities. GaN device performance is hindered when charge or other defects accumulate at the GaN/dielectric interface during gate dielectric deposition. Much of the contamination at the interface could be prevented and interface trap density could be reduced if a smooth gallium oxide layer could be grown directly on a GaN epilayer by thermal oxidation. Our hypothesis is that a thermal grown oxide layer between GaN and deposited high-k dielectrics (Al_2O_3, HfO_2 etc) can reduce the interface trap density. Inspired by the good interface quality of Si with SiO_2, we examined a simple thermal oxidation process for producing a high-quality insulating layer on GaN. For many compound semiconductors, thermal oxidation is not a viable technique for preparing a dielectric since a mixed oxide is formed with a rough surface, such as Ga_2O_3+$GaAsO_4$+As_2O_3 where As oxide instability leads to increased defect density at the interface [4,5]. By contrast, more stable Ga_2O_3 can be obtained from thermally oxidized GaN with insulating GaO_xN_y [6]. In this study, the influence of oxidation time at constant temperature was investigated on thermally grown GaO_x on *n*-type gallium-polar (0001) epitaxial GaN thin films.

Many researchers have studied the dry thermal oxidation of GaN in oxygen. The reported ranges of oxidation temperature was 700 to 1000°C, oxidation times was 10 mins to 45 hrs, and oxide surface roughness was 0.8 to 3.4 nm [7]. β-Ga_2O_3 is the most known thermodynamically

stable phase of gallium oxides. Wolter *et al*. [8] reported on the thermal oxidation of GaN thin films over the temperature range (750-900°C). Zhou et al. [2] detected the formation of crystalline gallium oxide at 850°C, albeit for long oxidation times. Oon *et al*. [9] studied the thermal oxidation of GaN in N_2O ambient and found the gallium oxide surface roughness increased with oxidation duration and hence oxide thickness.

Investigating the dry thermal oxidation of bulk GaN substrates, Zhou *et al*. [2] found that at 850°C, the rate was interfacial reaction-controlled, and the roughness of the surface increased with the oxidation temperature. Wolter *et al.* [10] showed the oxidation rate of GaN in dry air at 450°C and 750°C is exceedingly slow. Poor current-voltage characteristics were also observed for thermal oxidation at 750°C [10]. In this study the oxidation temperature was fixed at a constant temperature of 850°C because Lin *et al*. [11] reported that the thermal oxidation of GaN at 850°C resulted in the best interface quality. In our own study with GaN oxidation at 650, 750 and 850°C for 60 mins, we also found that the atomic oxygen concentration was highest for 850°C sample (Table 4.1).

Table 4-1 Oxygen concentration for GaO_x /GaN samples oxidized for 60 mins at various oxidation temperature

Oxidation temperature GaO_x /GaN (60 mins)	Oxygen concentration (atomic %)
850°C	24.7
750°C	19.97
650°C	18.62

Oon *et al* [9] showed the thermal oxidation of GaN reduced the interface trap density several orders of magnitude compared to deposited high-k dielectric/GaN MOS structures [7]. Nakano *et al*. fabricated 100 nm thick β-Ga_2O_3/*n*-GaN MOS capacitors at 880°C for 5 hrs. and reported D_{it} of 5.5×10^{10} $cm^{-2}eV^{-1}$. Lee *et al*. [12] obtained interface state density of 2.53×10^{11} $cm^{-2}eV^{-1}$ on a 100 nm thick Ga_2O_3 deposited on *n*-GaN by photoelectrochemical method.

In this work, the thermal oxidation time was kept relatively short compared to the previously reported works to ensure the oxide is quite thin, consistent with a gate dielectric application, and to maintain a smooth oxide surface and oxide-nitride interface.

4.2 Experimental procedures

Ga-polar *c*-plane wurtzite GaN epilayers on sapphire were employed for the fabrication of GaO_x/*n*-GaN MOS capacitors. The epilayers consisted of 1.5μm thick Si-doped, *c*-plane GaN grown on *a*-plane sapphire via metal organic chemical vapor deposition (MOCVD), using a 25 nm thick AlN buffer layer. The GaN epilayers were deposited at 1050ºC and 150 Torr, using a V/III ratio of 3500. The precursors for the GaN epilayers were trimethylgallium and ammonia. Doping, on the level of $1x10^{18}$ cm^{-3}, was achieved through the addition of silane. These GaN thin films were cleaned with acetone, IPA and DI water, then thermally oxidized at 850°C for 30, 45 and 60 minutes, in a dry oxygen ambient. The structural and chemical properties of the GaO_x/GaN samples were analyzed by x-ray diffraction (XRD), atomic force microscopy (AFM) and x-ray photoelectron spectroscopy (XPS).

Capacitance-voltage (C-V) measurements were taken to quantify the electrical properties of the MOSCAPs through hysteresis flatband voltage shift assessments. Room temperature C-V measurements were performed with a bias range of 10V to -10V in the dark at 1MHz frequency (dc sweep rate 50 mV/s). For hysteresis measurements, the MOSCAPs were swept from zero voltage to the accumulation region (+10V), followed by immediate voltage sweep from accumulation to inversion (-10V) and inversion to accumulation region (+10V). The flatband capacitance (C_{FB}) [13] was obtained from the flatband voltage (V_{FB}) from each C-V plot according to equation (1).

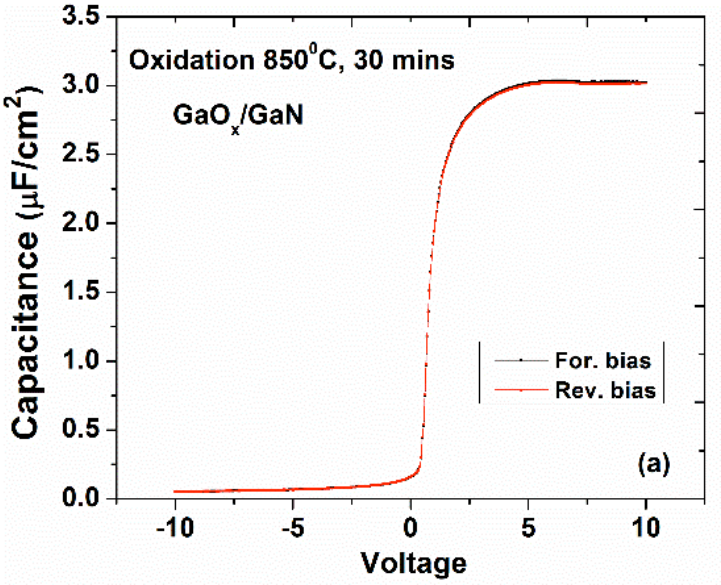
$$C_{FB} = \frac{\varepsilon_s C_{ox}}{C_{ox}\lambda + \varepsilon_s} \tag{1}$$

where ε_s is the permittivity of GaN, C_{ox} the oxide capacitance at accumulation and λ is the Debye length [15].

4.3 Results and Discussion

The high-frequency (1MHz) capacitance–voltage plots (dc voltage sweep rate 0.05 V/s) for samples oxidized for different amounts of time at 850°C are shown in Figure 4.1. For all samples, the transition from the accumulation to the depletion region was hysteresis-free. The sample oxidized for 30 minutes had the best saturation in accumulation region and the sharpest transition from accumulation region to the depletion region, which is indicative of good dielectric-semiconductor interface quality.

The oxide thickness (T_{ox}) was calculated from the gate oxide capacitance, the maximum capacitance in the accumulation region and assuming a gate oxide dielectric constant of 10 [15]. The estimated GaO_x thicknesses for the GaN oxidized for 30 mins, 45mins and 60 mins were 2.9 nm, 3.3 nm and 3.8 nm respectively (Table 4.2).



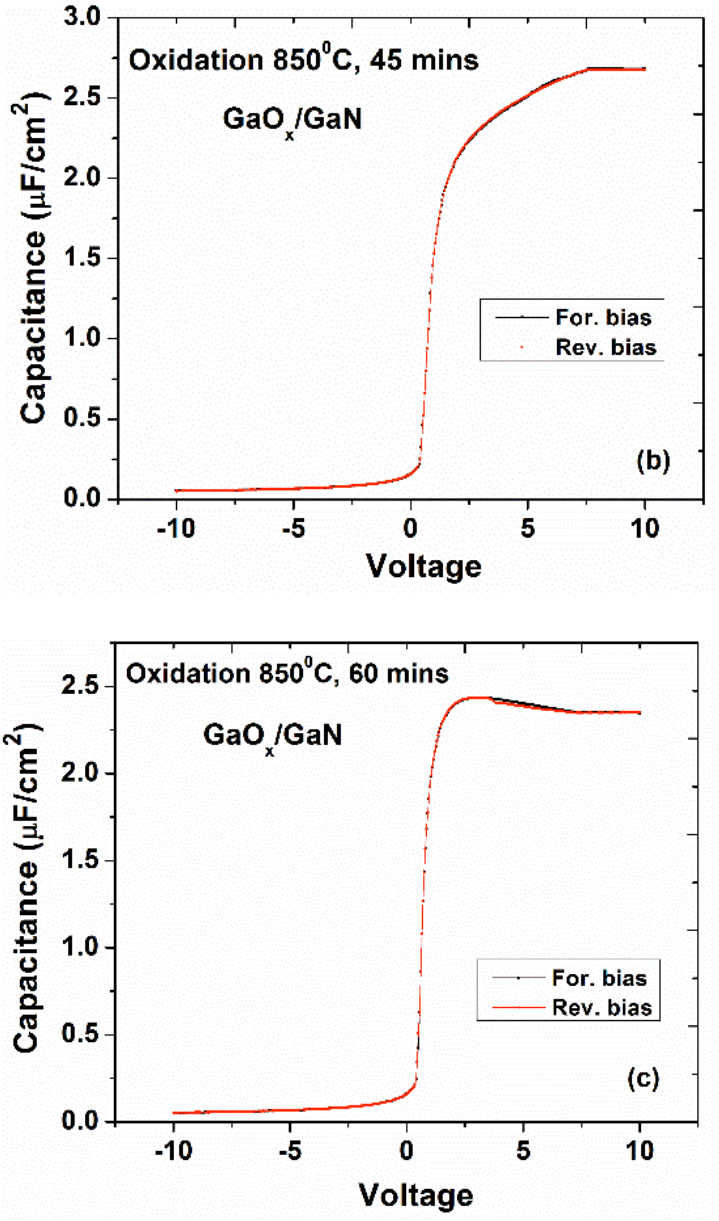


Figure 4.1 High frequency C-V measurement of GaO_x /GaN MOS capacitor, oxidized at 850°C for (a) 30 mins (b) 45 mins and, (c) 60 mins.

Table 4-2 Oxide thickness and O:Ga ratio from XPS

Samples	T_{ox} *(nm)*	*O:Ga ratio*
GaO_x /GaN (30 mins)	2.9	0.76
GaO_x /GaN (45 mins)	3.3	0.73
GaO_x /GaN (60 mins)	3.8	0.80

Due to such a thin GaO_x layer (Table 2), no peak was observed for GaO_x in the XRD 2θ scans from 20-80 degree. Characteristic diffraction peaks were observed for GaN in (002) and (004) planes. Sapphire (α-Al_2O_3) peak was observed at (110) plane. XPS data confirmed the existence of Ga and O and O: Ga stoichiometric ratios were 0.76, 0.73 and 0.80 for samples oxidized for 30, 45, and 60 mins respectively (Table 4.2). It can be noticed from Table 4.2 that non-stoichiometry in Ga and O ratio is indicative of oxygen deficiency in the Ga oxide films. Atomic percentage of Ga and O from XPS data is shown in Figure 4.2. The carbon atomic concentration was around 2% in all samples.

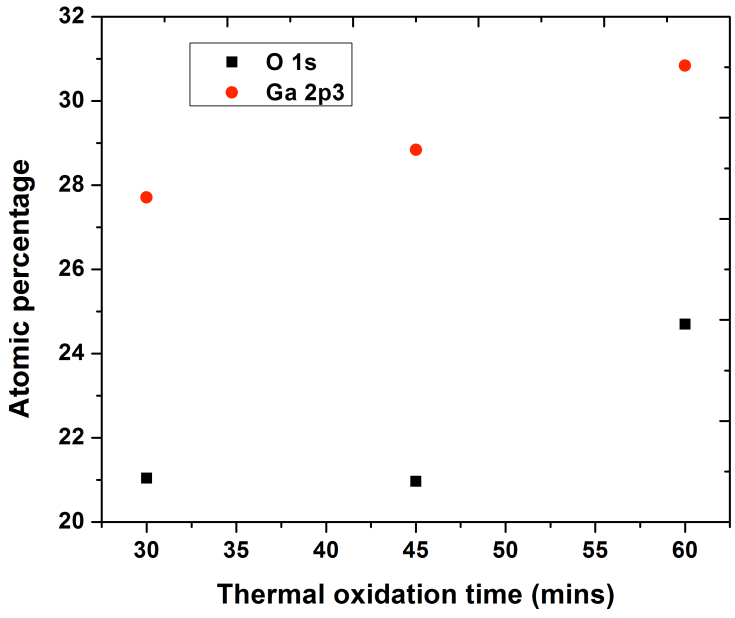


Figure 4.2 Atomic percentage of oxygen and gallium for GaO_x /GaN MOS capacitor, oxidized at 850°C for 30 mins, 45 mins and 60 mins.

The interface trap density was obtained following the single frequency approximation [16] ,

$$D_{it} = \frac{2}{qA} \frac{\frac{G_{m,\max}}{\omega}}{\left(\frac{G_{m,\max}}{\omega C_{ox}}\right)^2 + \left(1 - \frac{C_m}{C_{ox}}\right)^2} \quad (2)$$

where $G_{m,max}$ is the maximum conductance, ω is the angular frequency, C_m is the measured capacitance and A is the capacitor area.

The lowest interface trap density (D_{it} 2.75×10^{10} $cm^{-2}eV^{-1}$) occurred for the oxidation time of 30 mins and was comparable with values previously reported in the literature [17]. This low interface trap density can be attributed to the restoration of crystallinity of GaO_x and reduction of traps at the GaO_x/GaN interface [11].

Table 4-3 Interface trap density

Sample	D_{it} ($cm^{-2}eV^{-1}$)
GaO_x /GaN (30 mins)	2.75×10^{10}
GaO_x /GaN (45 mins)	5.71×10^{12}
GaO_x /GaN (60 mins)	4.8×10^{12}

The C-V data correlated with the surface morphology of the samples; the minimum surface roughness (0.59 nm) was attained from the sample oxidized for 30 minutes, (Figure 4.3) which also had the best electrical properties. The surface roughness of gallium oxide increased with oxidation time; thus, the minimum roughness was on the sample oxidized for only 30 mins. The leakage current was found to be on the order of 10^{-4} (A/cm^2) at a reverse bias (-4 volts) for these samples (Figure 4.4).

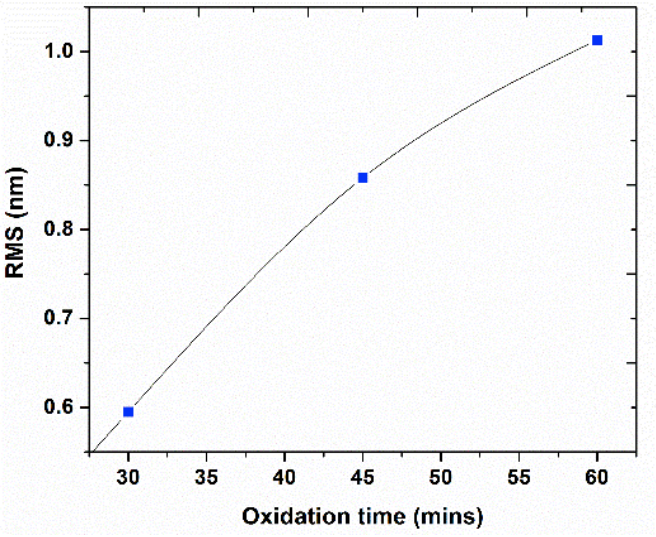


Figure 4.3 GaO_x surface roughness vs. oxidation time from AFM

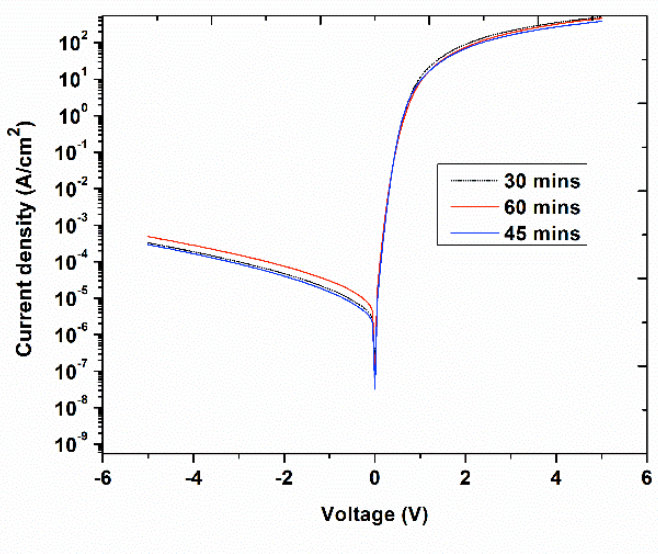


Figure 4.4 Leakage current at reverse bias

4.4 Conclusion

In summary, a dry thermal oxidation of GaN resulted in a non-stoichiometric gallium oxide. Further investigation is required in order to overcome oxygen deficiency in the gallium oxide film and obtain stoichiometry. Best electrical characteristics were obtained by oxidation at

850°C for 30 mins and were correlated to the surface morphology of the samples. The low interface trap density obtained for 30 mins oxidation sample indicates a high quality interface that is suitable for the fabrication of MOSFETs. These results suggest a thermally grown oxide on GaN can lead to superior interface quality when used as an intermediate layer between the GaN surface and a deposited high-κ dielectrics.

4.5 Acknowledgements

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Chapter 5 - Al_2O_3/*n*-GaN MOS capacitors based on polar *c*-plane and nonpolar *m*-plane GaN crystal faces

Abstract

The properties of metal-oxide-semiconductor capacitors (MOSCAPs) on *c*- and *m*-plane GaN were analyzed by capacitance-voltage measurements and compared. Recent interest in nonpolar (*m*-plane) GaN, due to its lack of a strong polarization field, motivated this investigation of the temperature behavior of Al_2O_3/GaN MOS capacitor. High temperature capacitance-voltage measurements showed relatively stable flatband voltage with temperature for *m*-plane GaN MOS capacitor. Greater shift in flatband voltage with temperature was observed for *c*-plane GaN MOS capacitor. It was observed that interface trap charge contributed more in this flatband voltage shift compared to fixed oxide charge estimated from the samples.

5.1 Introduction

GaN is an outstanding material for high voltage and high temperature devices. GaN MOSFETs are capable of excellent performance in high temperature electronics. Due to pyroelectricity (change in spontaneous charge density with temperature), polar GaN based MOSFETs exhibit strong shift in threshold and flatband voltage with temperature [1]. Nonpolar GaN surfaces can be used to prevent the effect of pyroelectric polarization in GaN MOS capacitors and transistors. *m*-plane $(10\bar{1}0)$ and *a*-plane $(11\bar{2}0)$ are among the nonpolar GaN surface and this study is focused on Al_2O_3/GaN MOS capacitors based on *m*-plane GaN. To achieve stable transistor operation, enhancement mode (E-mode) operation with a threshold voltage of over +3V is required for power switching applications. As a result, fail-safe operation in power electronics can be obtained [2] and simplification of circuit design can be done. However, it is difficult to gain +3V threshold voltage when *c*-plane GaN is used to fabricate Al_2O_3/AlGaN/GaN MOS structure. *m*-plane GaN can be utilized to fabricate Al_2O_3/AlGaN/GaN MOS HEMT structure because non-polar planes do not induce polarization charge. Fujiwara *et al*. [3] fabricated E-mode *m*-plane AlGaN/GaN HFETs (heterojunction field effect transistor) using Al_2O_3 gate dielectric deposited by atomic layer deposition and obtained a threshold voltage of +3V.

In this work GaN MOS capacitors were fabricated on polar (*c*-plane) and nonpolar (*m*-plane) GaN surfaces. An investigation was done to check their temperature stability because pyroelectricity is the cause for undesirable temperature shifts in flatband and threshold voltage of the GaN MOSFETs [4]. A positive shift in threshold voltage is likely to cause increment of on-state resistance of the GaN MOSFET. When the device is turned on, increase in on-state resistance causes power loss, which is undesirable. Also large negative threshold voltage shift has a tendency to increase leakage current through the device and results in power loss of the device [5]. In this study, temperature dependent capacitance-voltage measurement was done to extract flatband voltage at different temperatures of *c*- and *m*-plane MOS capacitor.

In our previous study, the leakage current density was lower for Al_2O_3/*m*-plane GaN compared to Al_2O_3/*c*-plane GaN but deposited Al_2O_3 formed smoother surface on *c*-plane GaN compared to *m*-plane GaN and total trapped charge for Al_2O_3/*c*-plane GaN (5.68×10^{11} cm^{-2}) was

less than that of Al_2O_3/*m*-plane GaN (5.83×10^{11} cm^{-2}) [6]. This total trapped charge or fixed charge was used in this current study and interface trap charge of *c*- and *m*-plane Al_2O_3. GaN were evaluated to determine which charge contributed most to the deviation of flatband voltage from its ideal value. The Interface trap charge was extracted using conductance method for *c*- and *m*-plane GaN MOS capacitors. Similar study was done by Matocha *et al*. [4] did similar study and it was based on SiO_2/GaN interface.

5.2 Experimental details

A 2μm thick layer of Ga-polar *c*-plane (0001) GaN (1×10^{18} cm^{-3} Si doped) was grown by MOCVD on an *a*-sapphire substrate and non-polar *m*-plane $(10\bar{1}0)$ *n*-GaN was grown by MOCVD on bulk *m*-plane GaN substrates. The GaN surfaces were treated with a piranha solution (H_2O_2: H_2SO_4 1:5) at 80ºC for 10 min before deposition of a gate oxide. Al_2O_3 was deposited at 280°C on *c*-plane and *m*-plane GaN by atomic layer deposition (ALD) and the thickness of Al_2O_3 was 19.2 nm obtained from ellipsometry. Using standard procedure of photolithography and e-beam evaporation 50 μm Au/Ni contacts were created on the oxide surface. The experimental setup for the high temperature (20°C to 98°C) C-V measurement is shown in Figure 5.1. The experimental setup shows that the sample is placed on a ceramic plate that consists of internal heating element and probes for electrical measurement and temperature sensor are in contact with the sample under test. A Kepco power supply unit was used to control the temperature in the ceramic plate. The ceramic C-V measurement was done using Keithley 4200 semiconductor characterization device at dc sweep rate of 0.1 V/s from accumulation to depletion region as a function of temperature. High temperature C-V was carried out in an inert atmosphere of argon to avoid any oxidation of the device.

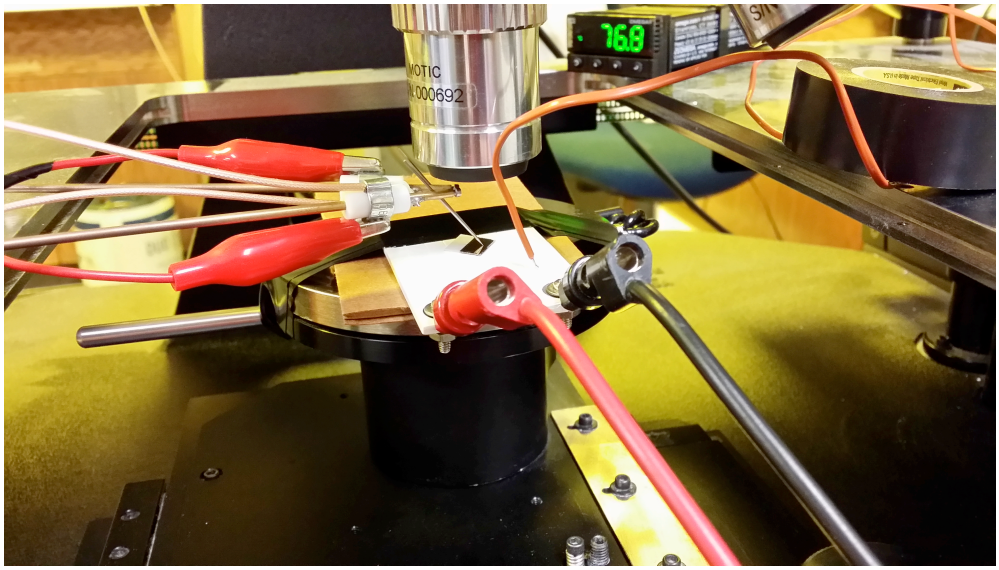

Figure 5.1 Experimental setup for high temperature measurement

The interface trap density (D_{it}) was determined by the ac conductance technique at room temperature. Extraction of interface state conductance $G_P(\omega)$ was done as a function of angular frequency at a fixed voltage within the depletion region. The parallel conductance (G_P) represents an energy loss due to interface traps and is expressed by [7]

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{1}$$

D_{it} was obtained from the magnitude of the G_P/ω peak from the G_P/ω vs frequency plot. The peak indicates that interface states are responding when the frequency of the ac signal is varied, and it is possible to extract interface trap properties from the ac response on Al_2O_3/GaN samples. D_{it} was determined using an HP 4284A precision LCR meter, and conductance was measured from 20Hz to 1MHz with long integration time. The characteristic trap response time ($\tau = 2\pi/\omega$) is expressed by the Shockley-Read-Hall statistics of capture and emission rates by $\tau = \exp(\Delta E / k_B T) / \sigma v_{th} D_{dos}$ where ΔE is the energy difference between the majority carrier band edge energy (E_{CB}) and the trap level E_T, k_B is the Boltzmann constant, v_{th} is the average thermal velocity of the majority charge carriers ($v_{th} = \sqrt{(3k_B T/m^*)} = 2.68 \times 10^7$ cm/s),

D_{dos} is the effective density of states of the majority carriers ($D_{dos} = 2(2\pi m^* k_B T/h^2)^{3/2} = 2.16 \times 10^{18}$ cm^{-3}), and T is the temperature. σ is the capture cross section of the trap (10^{-14} cm^{-2}). Based on the maximum conductance from the measurement, an approximate equation to calculate interface trap density is given by [8]

$$D_{it} = \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{\max} \quad (2)$$

5.3 Results and Discussion

C-V measurements were performed on c-plane and m-plane $(10\bar{1}0)$ Al_2O_3/GaN MOS capacitors.. Interface trap density determined by ac conductance technique showed that interface trap density was found to be on the order of 10^{13} eV^{-1}cm^{-2} (average) between 0.23 and 0.26 eV from the conduction band along the GaN bandgap. There was no significant difference in interface trap density between *c*- and *m*-plane GaN MOS capacitors (Figure 5.2). From the experimental data of current study it was found that $qD_{it} > C_{ox}$ and the conductance method becomes insensitive to the trap density and it could be overestimated by an order of magnitude [9].

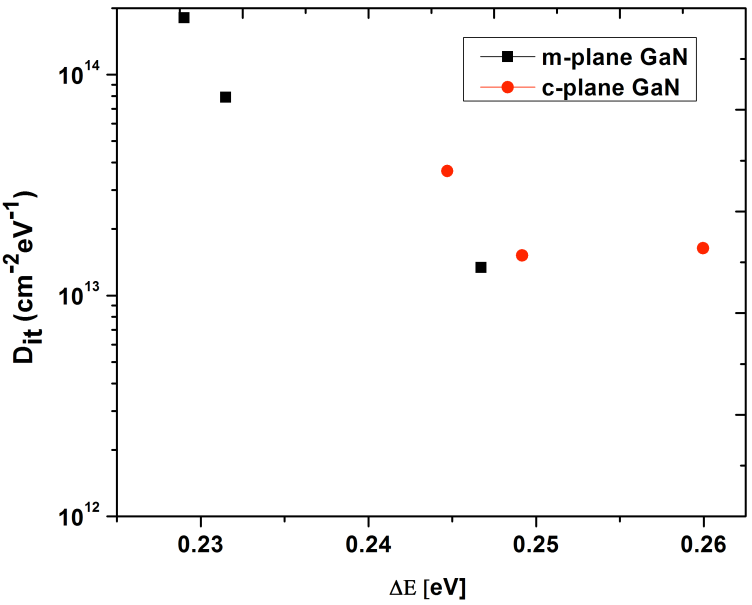

Figure 5.2 Interface trap density, D_{it} as a function of the energy separation from the conduction band edge for *c*- and *m*-plane GaN MOS capacitors measured at room temperature

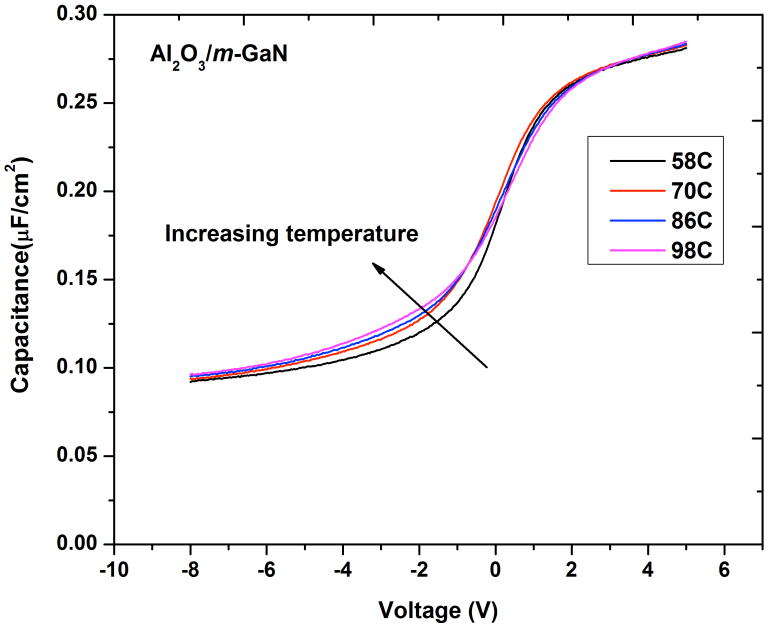

Figure 5.3 Capacitance-voltage plot as a function of temperature for *m*-plane GaN MOS capacitors at 100 KHz and dc sweep rate of 0.1 V/s

High temperature capacitance-voltage measurements were carried out for *c*- and *m*-plane GaN MOS capacitors (Figure 5.3 and 5.4). It was not possible to obtain C-V data beyond 73°C with c-plane GaN sample due to too much noise in the C-V plot. Minor presence of noise can be seen in the C-V plot of *c*-plane GaN sample at 57°C and 73°C (Figure 5.4). The trend in C-V plots with temperature for both *c*- and *m*-plane samples were found to be similar with Matocha *et al.*[5]. It has been observed that the flatband voltage of *m*-plane GaN showed comparatively more stability with temperature variation compared to *c*-plane GaN (Figure 5.5).

For n-type MOS capacitor, the flatband voltage is expressed as [10]

$$V_{FB} = \left[\chi_s + \left(\frac{E_g}{2} - \phi_b \right) \right] - \frac{Q_F + Q_{it}(T) + Q_{pol}(T)}{C_{ox}} \quad (3)$$

where χ_s is the semiconductor electron affinity, E_g is the semiconductor bandgap, ϕ_b is the semiconductor bulk potential, Q_F is the fixed oxide charge density, Q_{it} is the interface trapped charge and Q_{pol} is the negative polarization charge density at the oxide-semiconductor interface. It can be observed from figure 5.5 that exist positive flatband voltage shift at higher temperature, which can be attributed to more negative charges at the Al_2O_3/GaN interface [10]. In this study, as the fixed oxide charge density was found to be small, the shift in flatband with temperature is mainly due to the interface trap charge obtained from conductance method.

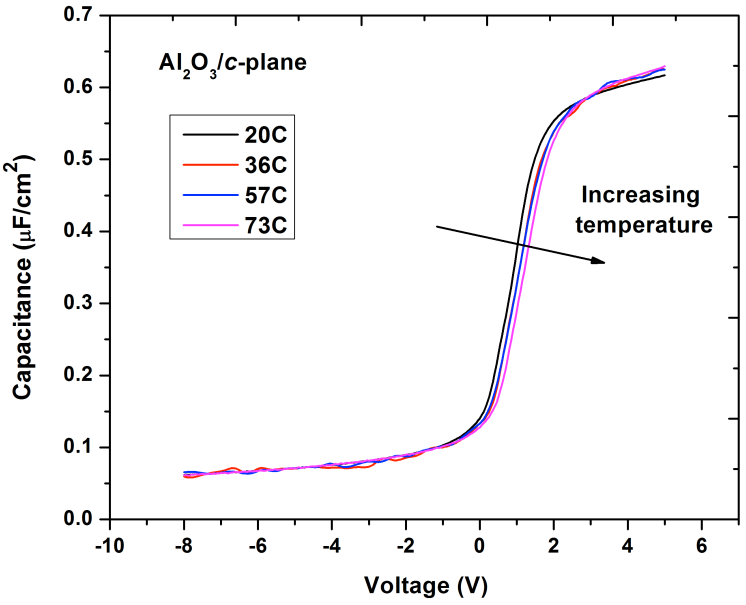

Figure 5.4 Capacitance-voltage plot as a function of temperature for *c*-plane GaN MOS capacitors at 100 KHz and dc sweep rate of 0.1 V/s

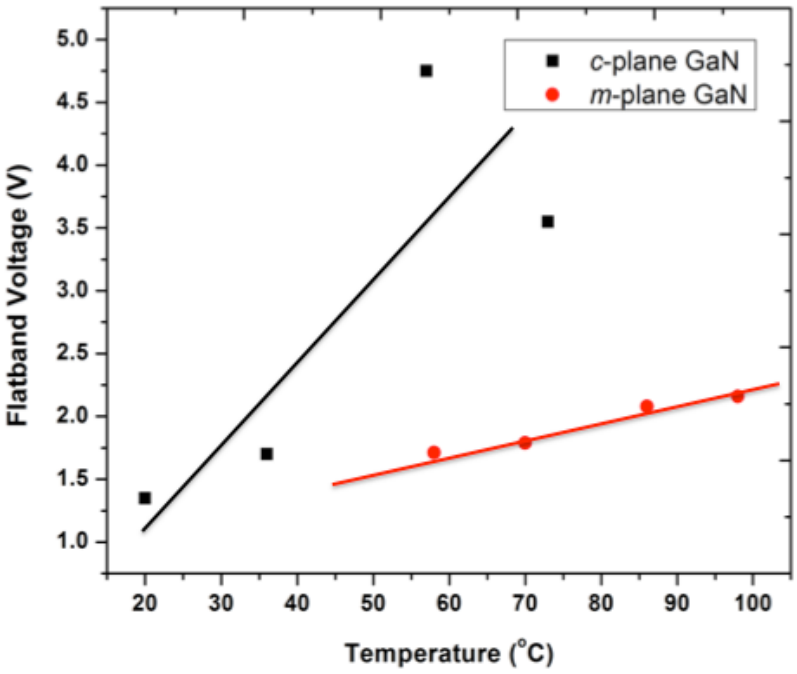

Figure 5.5 Flatband voltage as a function of temperature for *c*- and *m*-plane GaN MOS capacitors

5.4 Conclusion

It can be concluded from high temperature C-V measurements that m-plane GaN MOS capacitors will operate with more stability in high temperature environments. Interface trap charge density contributed more in this flatband voltage shift compared to fixed oxide charge density estimated from the samples.

5.5 References

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Chapter 6 - Overall Conclusion

GaN power devices are set to take over silicon power devices in terms of device speed, temperature tolerance and power handling capabilities. In addition, the integration of high-κ dielectrics with III-V semiconductors is important due to the need for high speed and high power electronic devices. But the major obstacle to using high-k dielectrics deposited on III–V semiconductors is high-interface trap density. Therefore, this research focuses on the development of GaN based MOS capacitor by minimizing the interface defects between deposited high-κ dielectric, Al_2O_3 on GaN and leakage current through the dielectric. To achieve this goal process condition during fabrication of the MOS capacitors were optimized by finding the best method to do *ex situ* wet chemical etching of GaN prior to ALD of Al_2O_3 and best condition for the dielectric deposition on GaN. The research also focused on obtaining high quality native oxide on GaN by dry thermal oxidation and the best condition to minimize leakage current and interface traps in TiO_2/Si interface.

It was demonstrated that ALD growth temperature and GaN surface treatment have profound impact on the gate oxide quality. To investigate the impact of the ALD temperature, Al_2O_3 was deposited by ALD at 240°C, 260°C, 280°C and 300°C. Due to 100% step coverage, ALD was employed to deposit Al_2O_3 on polar (*c*-plane) GaN at optimized temperatures of 280°C. The lowest average density of all trapped electrons ($Q_T = 1.25\times10^{11}cm^{-2}eV^{-1}$) occurred in the sample deposited at 280°C. The second objective of this study was to investigate the impact of the GaN surface cleaning. Three samples were cleaned using piranha (H_2O_2: H_2SO_4 =1:5), $(NH_4)_2S$, and 30% HF, and the fourth sample was left untreated.Cleaning the GaN with a piranha etch produced Al_2O_3/GaN MOS capacitors with the best electrical characteristics, $D_{it}= 3.73\times10^{12}$ $cm^{-2}eV^{-1}$.

Electrical characteristics of dry thermal oxidation of GaN was demonstrated because deposited dielectric films that are not native to the semiconductor typically contain high impurity concentrations from the deposition source used, and they suffer from a high-interface trap density. GaN thin films grown on sapphire by MOCVD were thermally oxidized for 30, 45 and

60 minutes in a pure oxygen atmosphere at 850°C to produce thin, smooth GaO_x layers. Compared to Al_2O_3/GaN MOS capacitors, no hysteresis loop was observed for gallium oxide/GaN MOS capacitors. Results showed that oxidizing at 850°C for 30 minutes resulted in the best dielectric-semiconductor interface quality, $D_{it}= 2.75\times10^{10}$ $cm^{-2}eV^{-1}$ but the gallium oxide was found to be in non-stoichiometry from the XPS measurement. This finding suggests that further investigation is required in order to overcome oxygen deficiency in the gallium oxide film. This thermally grown oxide on GaN can lead to superior interface quality when used as an intermediate layer between the GaN surface and a deposited high-κ dielectrics.

Investigation was done on Al_2O_3/*n*-GaN MOS capacitors based on polar *c*-plane and nonpolar *m*-plane GaN crystal faces. Nonpolar (*m*-plane) GaN MOS capacitors exhibited a stable flatband voltage across the measured temperature range and demonstrated temperature-stable operation. In this study, experimental setup was modified for temperature dependent capacitance-voltage measurement and flatband voltage was extracted at different temperatures for *c*- and *m*-plane MOS capacitors. It was also found that interface trap charge density contributed more in this flatband voltage shift compared to fixed oxide charge estimated from the samples.

Investigation was also done to study the influence of substrate temperature on TiO_2/Si MOS capacitors. Interfacial SiO_2 layer formed between TiO_2 and Si and calculated dielectric constant for TiO_2 was found to be maximum (ε_r = 55.6) for deposition temperature for 200°C. It was also demonstrated that the optimal deposition temperature of TiO_2 is 200°C as this produces the highest dielectric constant, most uniform coverage and stoichiometry. This ALD temperature also has the lowest impurity concentration and lowest D_{it} at the interface, indicating a better quality sample. The leakage current densities were on the order of $10^{-5}\sim10^{-4}$ A/cm^2 at −2 V.