Additive manufacturing of high-voltage electronics for gamma ray sensors

by

Devin James Burgett

B.S., Kansas State University, 2021

A THESIS

submitted in partial fulfillment of the
requirements for the degree

MASTER OF SCIENCE

Alan Levin Department of Mechanical and Nuclear Engineering
Carl R. Ice College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2023

Approved by:

Major Professor
Walter J. McNeil

Copyright

Abstract

Recent efforts in the field of additive manufacturing have included the construction of three-dimensional circuits. Circuits constructed through additive manufacturing have the potential to reduce the volume and weight of a design by using space more efficiently. However, research in additive circuitry is usually concerned with low-voltage electronics such as low power sensors and environmental monitoring.

In this work, a hybrid process to construct high-voltage electronics was developed. A compact high-voltage power supply for a photomultiplier tube was constructed through a combination of additive and traditional manufacturing processes. Advantages of individual processes were leveraged to reduce the volume and weight of the circuits constructed. Process methodology and parameters for fused deposition modeling, milling, automated placement, topographic scanning, and direct writing of conductive paste are covered. The dielectric is constructed using fused deposition modeling, with discrete slots for components. Surface roughness left behind by fused deposition modeling was greatly reduced through surface milling. Discrete components were placed into the build and the build surface was scanned to set the height for trace deposition. Finally, conductive material was deposited on the build surface to form circuit connections.

The compact electronics constructed were electrically tested and compared against a commercially manufactured high-voltage resistive divider base for electrical performance, volume, and weight. A high-voltage power supply was constructed which could produce up to -881 V $\pm$ 0.68 % with a stability of within less than 0.4 %. The high-voltage power supplies constructed were able to reduce the volume by up to 29.75 %, and the weight by up to 41.7 % compared to the resistive divider base. The electrical performance of the high-voltage bases were comparable to voltages from the commercial board and are expected to allow the photomultiplier tube to function similarly.

Table of Contents

List of Figures

List of Tables

Acknowledgments

I would like to thank my friends and staff of the Kansas State University Mechanical and Nuclear Engineering Department. This work was supported by the Defense Threat Reduction Agency contract number HDTRA1-20-C-0044.

Dedication

This work is dedicated to my parents, Warren and Jennifer Burgett. Thank you for your continued support and belief in me.

Chapter 1

Introduction

1.1 Motivation

In the past few years a research team at Kansas State University has been developing a high-voltage power supply circuit for a Hamamatsu R11265U series photomultiplier tube (PMT) that will be constructed using additive manufacturing[1]. The high-voltage supply circuit has been designed and validated for functionality in previous work conducted[2]. The three-dimensional construction will be performed using a multi-functional 3D printer from nScrypt.

The goal of this work is to develop a high-voltage circuit layout for additive manufacturing and to construct a high-voltage power supply for use with the R11265U PMT. The design is to be constructed through a hybrid process combining additive manufacturing and traditional manufacturing processes. Design development focused on the use of the additive manufacturing capabilities to perform as much of the construction as possible within the time frame of the project. Traditional processes were considered and modified as necessary to develop functioning circuitry. The nScrypt 3D printer was capable of performing an array of processes including, fused deposition modeling, milling, laser scanning, material deposition via SmartPump, pick-and-place, ultraviolet curing, and inspection via two gantry mounted cameras.

Additive manufacturing (AM) promises to reduce overall circuit volume by generating geometry not possible through traditional techniques. However, to leverage the manufacturing freedom that AM provides, specific layouts must be developed for use with the technology. Circuit layouts and discrete component placement will be developed to minimize the required volume and tested for electrical performance.

1.2 Previous Work

Previous research using traditional printed circuit board construction has examined the use of Cockcroft-Walton based power supplies for photomultiplier tubes. One such design constructed for the 12 stage FEU84-3 photomultiplier tube was capable of producing a final cathode voltage between 1000 V ± 2 % and 2023 V ± 2 % which may be set in 1 V increments[3]. Another design incorporating a Cockcroft-Walton multiplier was a circuit for a 10 stage PMT that was capable of producing between 800 and 2000 V from an input of 12 V[4]. Another group examined the performance of small photomultipliers with a 9 stage Cockcroft-Walton based power supply that was optimized for volume, requiring 3.5 in^3 to supply two Hamamatsu R7400P PMTs[5]. The use of Cockcroft-Walton voltage multipliers has been examined for the power supply of the 12 stage R11265U PMT in previous work conducted for the project[2].

The high-voltage circuit constructed was optimized for performance while minimizing the required number and size of components[2]. The design was developed with the final construction to be conducted using additive manufacturing. The full circuit schematic and bill of materials is included in Appendix A. The finalized circuit design was to operate as a charge pump pushing current into a filtered 16-stage half-wave Cockcroft-Walton voltage multiplier to generate high-voltage. The charge pump was constructed as a microcontroller which used pulse-width-modulation (PWM) to toggle a MOSFET, storing energy in an inductor. The microcontroller would continuously read the voltage output from the final stage of the voltage multiplier to determine the required duty cycle to maintain the target voltage. The microcontroller algorithm to set the duty cycle was based on a proportional-integral-

derivative (PID) control loop. The current pushed into the voltage multiplier enables the construction to generate a negative voltage exceeding -700 V at the final stage. The MOSFET used in the final circuit had to be modified due to international component shortages, the operating voltage of the circuit was raised to 5 V from 3.3 V to accommodate the change.

1.3 Design Goals

The goal of this work was to develop a process to construct high-voltage electronics through additive manufacturing and to build a high-voltage power supply for a R11265U Hamamatsu PMT. Specific goals included:

- To integrate analog and digital components into an additively manufactured assembly.
- Generate a high-voltage output of greater than -700 V, required by the R11265U PMT.
- Minimize the construction form-factor of the final design.
- Improve the repeatability of the hybrid manufacturing process developed.

1.4 Major Contributions

The manufacturing and testing of the high-voltage power supplies constructed through a hybrid additive manufacturing process has made the following contributions to the fields of mechanical, electrical, and nuclear engineering:

- Development of a layout for a high-voltage circuit for additive manufacturing.
- Generation of high-voltage using a circuit constructed incorporating fused deposition modeling.
- Development of a hybrid process to construct additive circuitry.

Chapter 2

Background

Developing a process to print high-voltage circuits requires knowledge of both additive manufacturing and design constraints from the sensor application. Recent developments in additive manufacturing and a brief overview of photomultiplier tubes will be covered in this chapter.

2.1 Additive Manufacturing

Additive Manufacturing (AM) are processes by which a computer generated model is sectioned into slices and printed layer-by-layer, generally from the bottom up. AM can be performed through a number of processes such as fused deposition modeling, stereolithography, selective laser sintering, powder bed fusion, and material jetting. When constructing circuits using AM, fused deposition modeling (FDM), stereolithography (SLA), and inkjet deposition are the most common[6;7;8]. Conductive material is applied to the printed part in multiple ways such as direct writing of conductive paste, printing conductive plastic, atomizing conductive material onto the print surface, and bonding metal to the printed surface[9;10;11]. Conductive material embedded in plastic filament generally has a high resistance compared to commercially available conductive pastes[6;12]. Reducing power lost to heat from trace resistance in the final circuit is important not only to reduce assembly

heating but, to reduce power consumption during operation. In order to construct additive circuits this work examines the methods of FDM and the writing of conductive paste onto the build surface.

Previous research has examined the construction of additive circuits and the creation of processes or systems by which circuits may be produced. A group developed a system and process to produce circuits using SLA and conductive paste by printing channels between individual components[7]. Another team developed a variable capacitor which was constructed using FDM to print the structure of the capacitor and conductive ink printed on a flexible medium to act as the plates[8]. However, most research focuses on the construction of low-voltage circuits which do not reach 600 V or greater defined as high-voltage circuitry[13]. While additive manufacturing provides advantages over traditional methods, shortcomings of the technology such as dimensional variability and surface roughness makes the combination of techniques in a "hybrid" process vital to developing functioning circuitry[14;15]. The focus of this research is to develop a hybrid process to construct high-voltage circuits which are able to maintain an operating voltage magnitude of 700 V or higher.

The 3D printer used for this endeavor was the 3Dn-300 from nScrypt capable of FDM and printing with conductive paste[16]. The gantry system was loaded with an FDM hot-end, pick-and-place, mill, laser height sensor, pump, and camera. The versatile tooling allows for multiple processes to be conducted on the bed in sequence, enabling complex workflows to be performed on a single machine. The pumping system used was the SmartPump from nScrypt, which is capable of dispensing conductive material onto the build as part of the on-bed processes[17]. Previous work from other groups using different equipment deposited conductive paste into milled channels to form traces between components[6]. In this work, traces are deposited via direct write as a conductive paste onto the build surface. Without preparation, the surface finish of parts printed through FDM had a rough surface finish, which obstructs a uniform distribution of conductive material[14;18]. Once dispensed, the paste will have the potential to settle into surface defects left from FDM. In order to minimize surface roughness, the surface is prepared using the mill prior to trace deposition. Other equipment within the printer was leveraged based upon specific design requirements and in

order to increase automation in the hybrid process.

2.2 Photomultiplier Tubes

Photomultiplier tubes (PMT) are optical sensors which convert light events into electrical pulses. Photons are absorbed by the photocathode which ejects electrons through the photoelectric effect. The electrons are guided to a series of dynode stages by electrical fields. Electrons are accelerated and guided by the biased dynode stages to the anode for collection. The flow of electrons form a pulse which is observed from the anode and measured as is commonly done in radiation detection and gamma-ray spectroscopy.

For gamma-ray spectroscopy a scintillating material is attached to a PMT. Scintillating materials are sensitive to ionizing radiation and emit light when radiation interacts within the medium. One such material is Cesium Iodide, Sodium doped (CsI(Na)). When gamma rays interact with the crystal of CsI(Na), 41 photons per keV are emitted[19]. CsI(Na) has a wavelength emission peak of 420 nm and light output of 85 %[19]. For this work CsI(Na) was used as it represented a durable crystal choice for mobile radiation detection. Depending on the sensitivity and applications, different sizes and compositions of crystals may be used. In this work a 1 inch by 1 inch by 3 inch CsI(Na) crystal was used in combination with a R11265U PMT from Hamamatsu, shown in Figure 2.1.

The pin socket at the top of the PMT shown in Figure 2.1 is used to bias the dynode stages and read the output signal. Incremental voltages are provided to the dynode stages to guide and accelerate electrons ejected from the photocathode. The range of photocathode voltages required for testing are between -700 V and -900 V. The E11807-01 is a commercially available passive resistive divider for the R11265U PMT that reduces the input high-voltage following a series of resistive dividers to bias each dynode following the calculated distribution shown in Figure 2.2. The E11807-01 and associated schematic are shown in Figure 2.3. While the E11807-01 is not a high-voltage supply, it represents the closest analog for size comparison that is publicly available. The R11265U PMT can be operated with a photocathode voltage of up to -1000 V[1].

Figure 2.1: *The R11265U PMT and CsI(Na) crystal assembly.*

In order to generate the required voltages, a circuit design incorporating a charge pump with a Cockcroft-Walton voltage multiplier was developed in previous work performed by Dodson, M., shown in Figure 2.4[2].The design of the circuit and optimization of circuit parameters is not the focus of this thesis, rather the processes and layout development necessary to construct the circuit using a hybrid AM process.

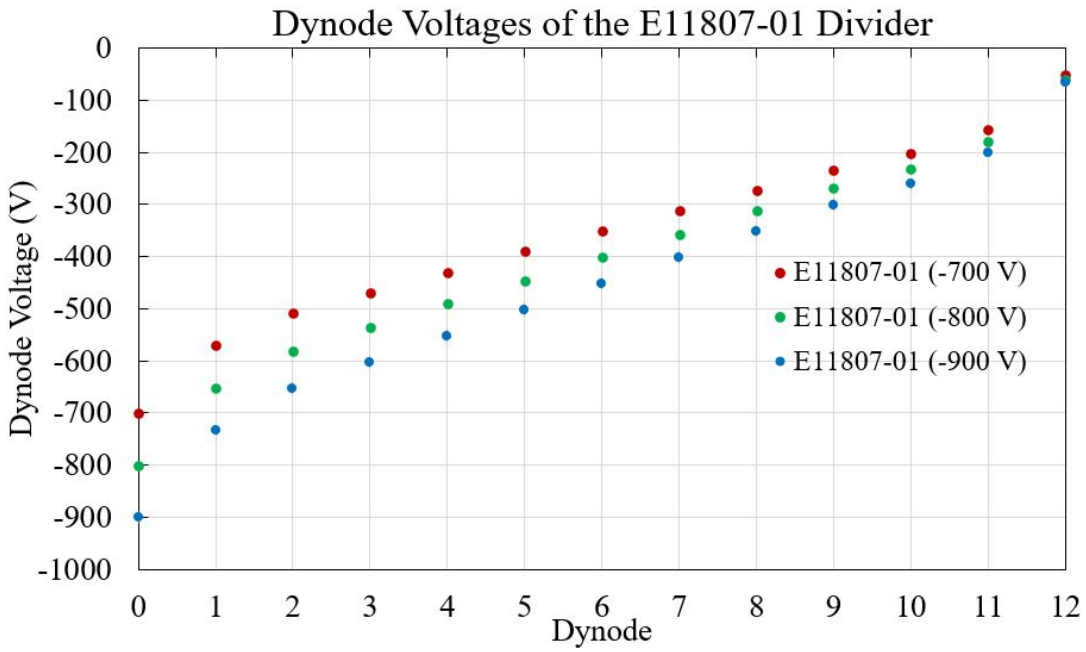


Figure 2.2: *The voltage distribution required by the dynodes of the R11265U PMT for the E11807-01 voltage divider biased at -700 V to -900 V. Dynode 0 refers to the photocathode.*

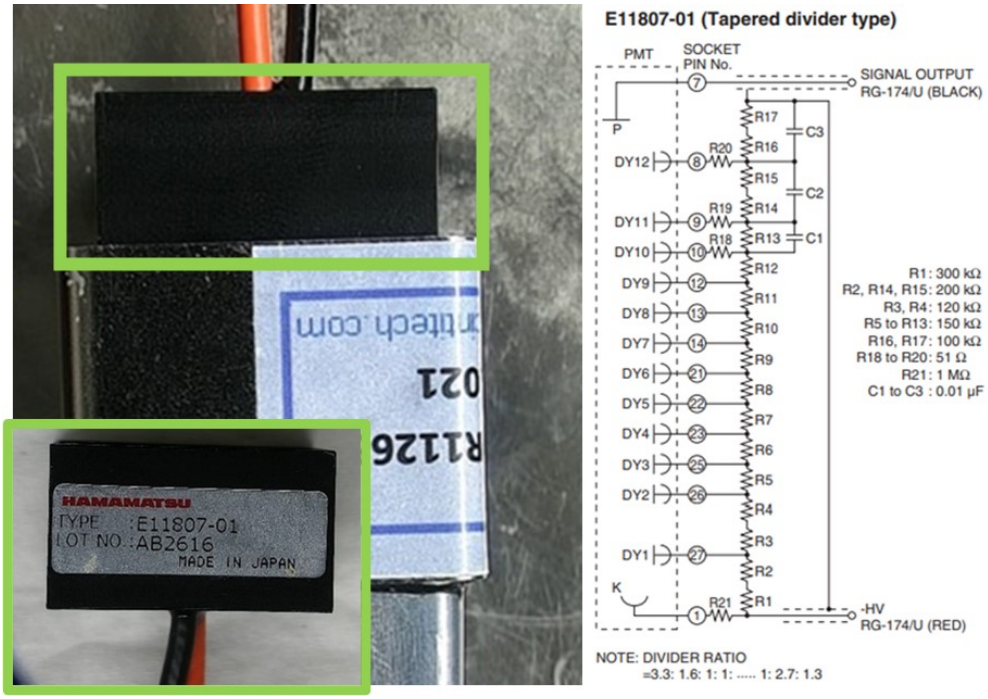


Figure 2.3: *The E11807-01 when biased at the target photocathode voltage produces the distinct voltages required by the 12 dynodes*[1].

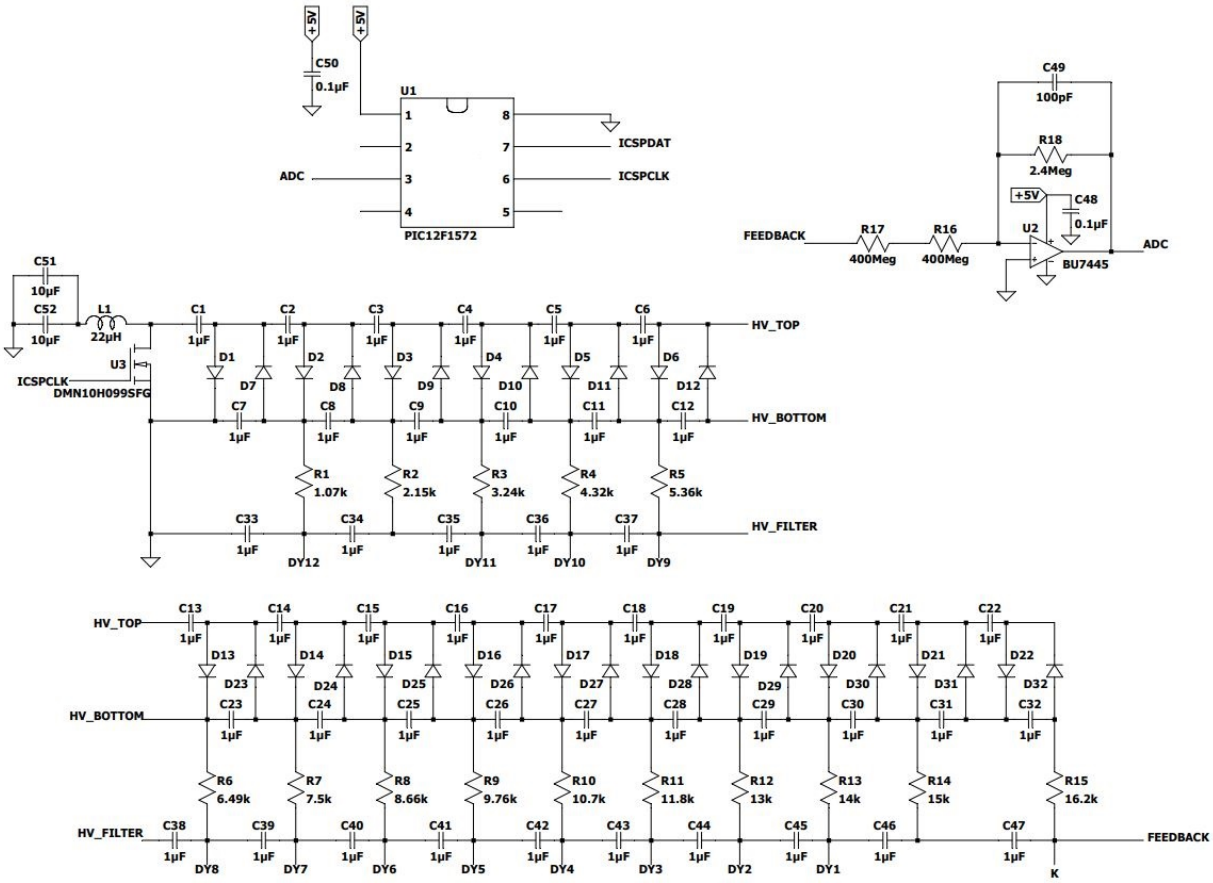


Figure 2.4: *The final circuit adapted from the previous work, incorporating the charge pump and Cockcroft-Walton voltage multipliers*[2].

The layout of the full circuit in Figure 2.4 will be developed to use the least amount of volume required given the constraints of the PMT assembly shown in Figure 2.1. The pins of interest are the dynode stages, photocathode, and anode, the remaining pins are internal connections to the anode and will not be connected. The pinout of the R11265U provided by Hamamatsu is shown below as Figure 2.5.

The goal was to use the 2.74 cm^3 available from the internal volume of the PMT, shown in Figure 2.1 to house the electronics, then to extend as little as possible from the top of the PMT socket. Certain elements of the PMT design such as the pin locations and alignment column shown in Figures 2.1 and 2.5 act as the primary constraints to the design. The design requires connections not only to the pins of the PMT but to external pins to supply a bias of 5 V and to readout the signal from the anode. This work seeks to address the manufacturing

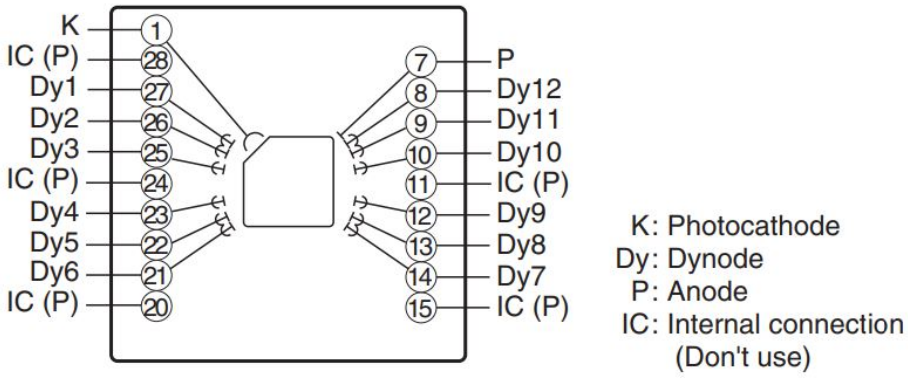


Figure 2.5: *The pinouts of the Hamamatsu R11265U PMT, the required connections are to each of the dynode stages, the photocathode, and the anode*[1].

concerns with constructing a compact circuit and providing power to the PMT, spectral data and discussion of radiological measurements will not be addressed.

Chapter 3

Method and Theory

This chapter is divided into two subsections to cover the details of each process required to construct the high-voltage circuitry and to briefly cover specific electrical tests performed to improve voltage regulation.

3.1 Manufacturing Test Articles

The hybrid process to manufacture test articles is discussed in this chapter, each section corresponds to a process step.

1. Section 3.1.1 describes how the dielectric material is deposited via FDM.
2. Section 3.1.2 explains the milling process to prepare the surface for traces.
3. Section 3.1.3 covers the automated placement of parts.
4. Section 3.1.4 describes the laser scanning techniques used to evaluate the build surface topology.
5. Section 3.1.5 explains the deposition of conductive traces via direct write onto the build surface.

Following the hybrid process developed, high-voltage power supplies (HVPS) were constructed with characteristics shown in Chapter 4. Finally, conclusions on the impact of the hybrid process and potential improvements are discussed in Chapter 5.

3.1.1 Fused Deposition Modeling

Fused Deposition Modeling (FDM) was used to print the dielectric build to hold the circuit. Circuits were expected to have discrete component slots constructed using FDM with any necessary geometric features for the final builds developed at the time of printing. A process was developed incrementally using a series of test articles to determine operating parameters and to determine the geometry that would be used for the final design. Developing the process for FDM began with determining extrusion parameters for the dielectric material. Acrylonitrile butadiene styrene (ABS) is extruded as the dielectric material. Prior research conducted shows that ABS has higher dielectric strength than polylactic acid (PLA) and will be sufficient to isolate components. The dielectric strength of ABS was measured to be 39 to 48 kV/mm compared to PLA with 26 to 34 kV/mm[20;21]. Printed ABS is also more durable than printed PLA having higher impact strength and is able to withstand higher temperatures[22;23].

ABS dielectric material was extruded using ceramic nozzles of 300 μm inner diameter (ID) and 400 μm outer diameter (OD), and with 125 μm ID and 175 μm OD. The filament used had a recommended extrusion temperature of 210 °C to 240 °C. The 3Dn-300 has an enclosed build volume reducing heat loss from the print area, shown in Figure 3.1. ABS is known to warp and may experience micro-cracking when cooled, decreasing the rate of cooling was expected to reduce the potential for deformation.

The material working temperatures were tested while using a 300 μm ID ceramic tip prior to switching to the precision 125 μm ID tip. ABS was extruded using a nozzle temperature range of 210 °C to 230 °C and bed temperature range of 90 °C to 110 °C. Since ABS is an amorphous thermoplastic it has no distinct glass transition temperature, continually softening as it is heated. The use of a 300 μm ID tip, bed temperature of 90 °C and nozzle

Figure 3.1: *The 3Dn-300 multi-functional 3D printer with enclosed build plate.*

temperature of 230 °C was sufficient for printing. However, an early test article with various slots for discrete components with the current parameters did not exhibit the necessary resolution as shown in Figure 3.2.

Tests run using the larger nozzle enabled test prints to be produced over the temperature range to observe factors of bed adhesion, material accumulation, and the effect of select slicer settings. The build plate was covered in polyethylene terephthalate (PET) strips and coated with a washable adhesive. The combination of PET strips and adhesive improved the first layer adhesion, and reduced warping in the base layer. In an attempt to improve feature resolution and adhesion between layers, perimeter speed was changed from 20 mm/s to 2 mm/s. The perimeter of an 0402 resistor is 3 mm, to improve the resolution the "Small Perimeter Speed", which controls the speed for perimeters less than 6.5 mm in radius, was reduced in PrusaSlicer from 15 mm/s to 1 mm/s[24;25]. It was also observed that excess material appeared to accumulate on the nozzle and would be deposited randomly throughout

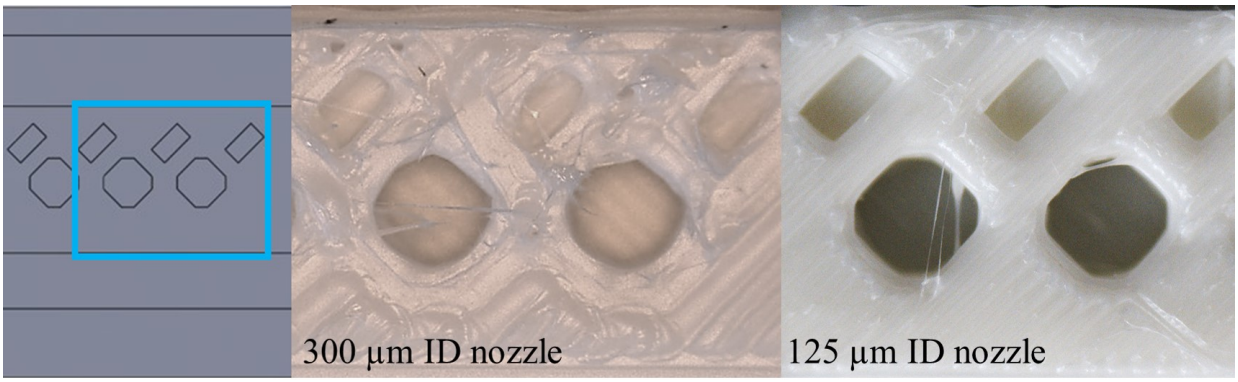


Figure 3.2: *A test of a 300µm ID nozzle for constructing pin sockets and resistor slots. Later test conducted with 125µm ID nozzle included for comparison.*

the build, creating additional surface roughness. To reduce the excess material the overlap between printed roads was varied between 25 % and 5 %. At the lowest end, the 5 % overlap resulted in printed roads becoming detached and the surface ridges became deeper, increasing surface roughness. After a series of tests the initial print settings were identified, they are shown in Table 3.1.

Table 3.1: *The initial testing focused on usable operating temperatures for the equipment and qualitative observation of build quality when using the 300 µm ID ceramic tip.*

Setting	Value
Nozzle Temperature	230 °C
Bed Temperature	90 °C
Perimeter Speed	2 mm/s
Small Perimeter Speed	1 mm/s
External Perimeter Speed	50 %
Infill Speed	4 mm/s
Infill	Rectilinear, 100 %
Layer Height	0.12 mm
First Layer Speed	40 %
Overlap (between printed roads)	10 %
Avoid Cross Perimeters	On

With initial settings identified and the print resolution of the 300 μm ID nozzle being insufficient, the nozzle was exchanged with the 125 μm ID nozzle to produce additional samples shown in Figure 3.2. Reducing the nozzle size worsened the adhesion of the first layer to the build plate. The print settings were modified to account for the lack of adhesion

by increasing the build plate temperature from 90 °C to 110 °C. The material was observed to burn onto the nozzle after long periods of printing, to reduce the rate at which the material appeared to accumulate, the nozzle temperature was reduced to 220 °C from 230 °C. The perimeter speed was also reduced from 2 mm/s to 1 mm/s to increase adhesion between perimeters. Modifications to printing settings are documented below as Table 3.2.

Table 3.2: *Settings were modified to improve the adhesion and resolution of the 125 µm ID ceramic tip.*

Setting	Value
Nozzle Temperature	220 °C
Bed Temperature	110 °C
Perimeter Speed	1 mm/s
Infill Speed	2 mm/s
First Layer Speed	30 %
Layer Height	0.1 mm

The print resolution of the 125 μm ID nozzle was sufficient for the discrete component slots and a modular approach was taken to circuit construction. As part of the modular approach the circuit in Figure 2.4 would be separated into functional modules. To reduce component placement steps the Cockcroft-Walton multiplier was constructed as a set of discrete assemblies which could be integrated with the printed build after being removed from the build plate.

The assembly developed reduced the number of circuit component placements for the final build, by soldering the Cockcroft-Walton multiplier assembly as two sub-assemblies. The Cockcroft-Walton multiplier was comprised of 64 components total to form the half-wave 16-stage configuration. However, by building the sub-assemblies the component placement steps for the final build were reduced from 106 to 44. Each sub-assembly consists of eight of the total sixteen stages in the multiplier, a single assembly is shown below in Figure 3.3, and soldered as Figure 3.4.

Each sub-assembly can be tested by pushing current into the first stage labeled 'WAVE-FORM', the final voltage may be drawn from the node '-HV' in Figure 3.3. The sub-assemblies reduced the number of slots required in the printed base, requiring only two slots

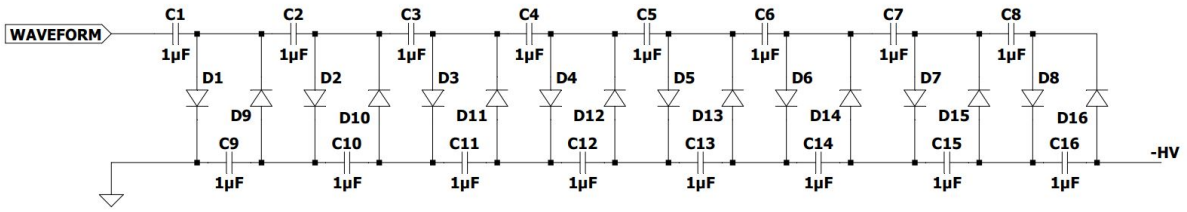


Figure 3.3: *The Cockcroft-Walton sub-assembly used in the printed build to reduce the number of component placement steps.*

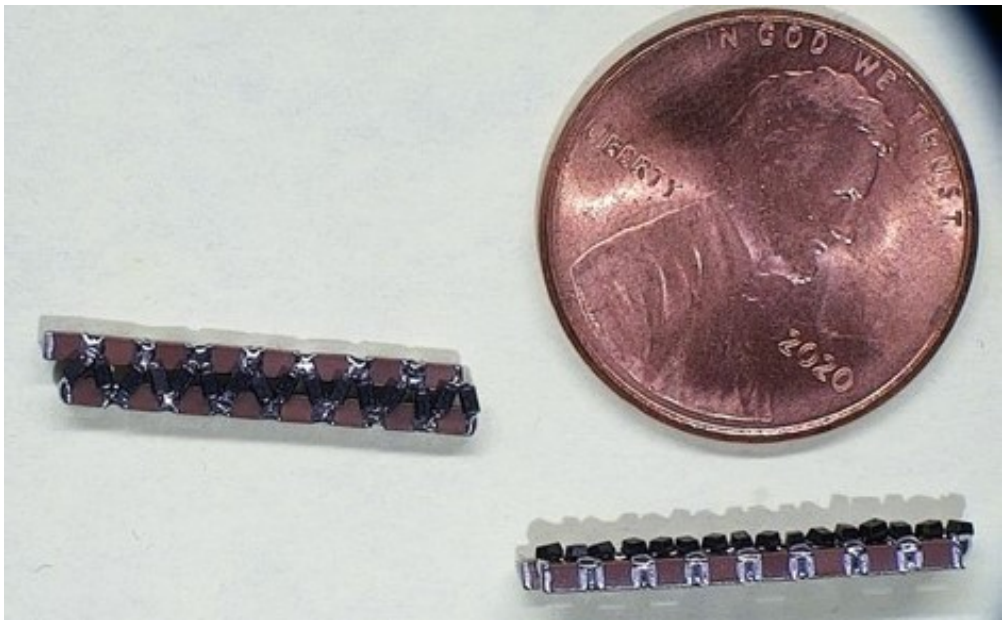


Figure 3.4: *The Cockcroft-Walton sub-assembly soldered, prior to integration with printed designs.*

in the design to accommodate the full Cockcroft-Walton (CW) ladder. The assemblies were connected end-to-end in the final assembly to complete the 16-stage multiplier.

After the CW sub-assemblies were constructed, a print to filter the CW multiplier was developed. The CW Base print was developed to hold a sixteen-stage CW multiplier and accommodate the low-pass filter associated with each stage, shown in Figure 3.5. The SolidWorks model of the part is shown in Figure 3.6. The outer dimensions were constrained by the sensor body, the central opening was used to align within the sensor body. Pin holes were aligned along each side to accommodate an interference fit with gold connector pins.

From Figure 3.6, the resistor slots were placed between the pins and CW multiplier assembly to conserve space. In order to simplify construction the layout in Figure 3.6 allows

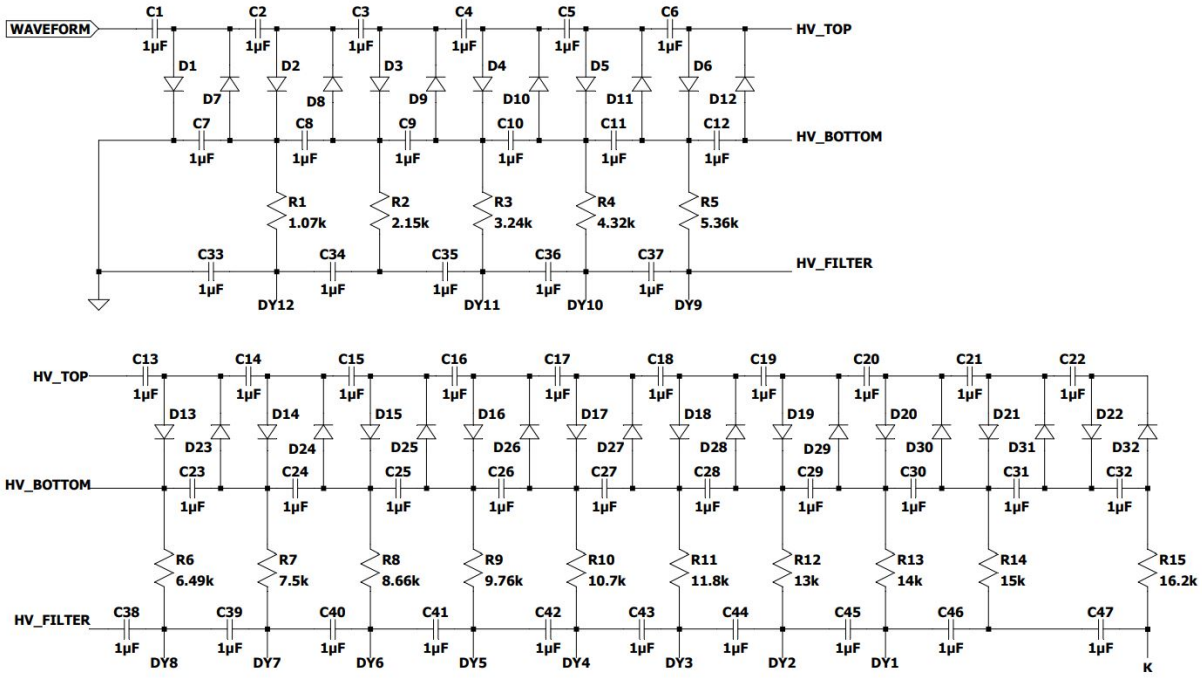


Figure 3.5: *The Cockcroft-Walton sub-assemblies will be integrated with the filtering circuitry through connections provided by the printed base.*

the dynode stages to be drawn from the multiplier node aligned with each connection pin. The central placement of the CW multiplier grants two advantages for the final design; the length of traces from each stage are minimized due to proximity with the output pins; and the placement of the CW multipliers requires less horizontal space in the design. The CW Base print was developed as a stand-alone part which when given a current source would act as a voltage multiplier with filtered stages. The horizontal space was limited by the placement of the sensor pins and necessary filtering circuitry. A spacing of at least two printed roads were required to maintain a solid edge along the pins and prevent deformation. A minimum of three printed roads were used for the other features. The filtering capacitors at each stage were positioned to provide mechanical support to the edge of the build. The part edges were not expected to undergo significant stresses or torsional forces during use, the support resulting from part placement was expected to be sufficient. A completed CW Base print is included in Figure 3.7.

The space available at the top of the design in Figure 3.7 was reserved for the high-

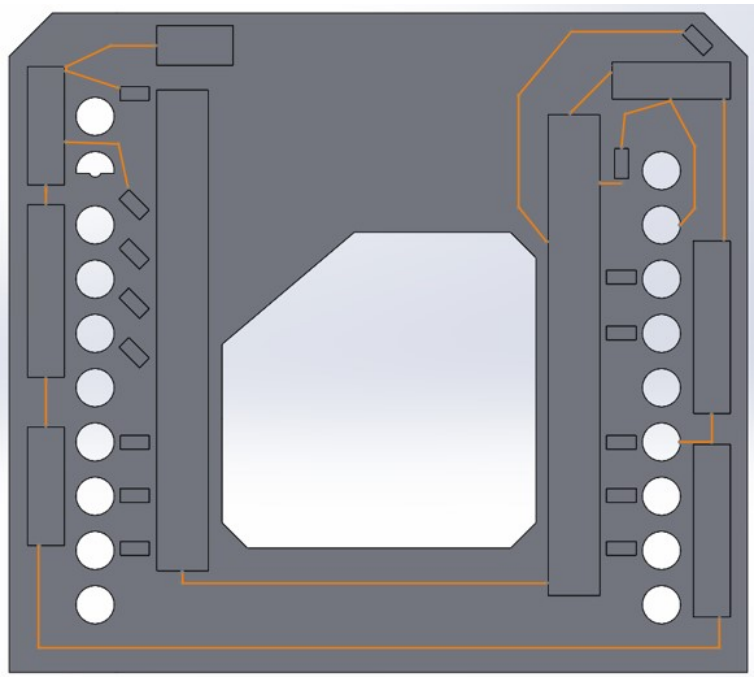


Figure 3.6: *The PMT pin locations have printed holes to affix sockets for the final connections. Trace routing is highlighted in orange, connections between the pins and RC filter will be conducted as a post-process. The CW slots have a spacing of three printed roads from the central slot. Minimum spacing of two roads is used for the resistor distance from the pin holes.*

voltage (HV) control circuitry. The HV control consisted of a microcontroller, MOSFET, op-amp, and decoupling capacitors, functioning as a feedback loop for the final stage of the CW multiplier. The control circuitry is included as Figure 3.8.

The volume of the control circuitry in Figure 3.8 was reduced horizontally to fit in a stand-alone print which could fit into the available space left in the CW Base print. A modular approach was taken to construction so that each part could be tested without the complete assembly. The HV control circuit was designed to be programmed in-circuit using small sockets to press temporary pins. The sockets would be lined with conductive material to ensure an interference fit during programming. A model showing the expected pin connection and printed geometry is shown in Figure 3.9. As depicted in Figure 3.9, the lower build will contain the digital circuitry such as microcontroller, MOSFET, op-amp, and associated decoupling capacitors. The upper build will connect to the inductor through the two large rectangular pads with printed vias extending to each.

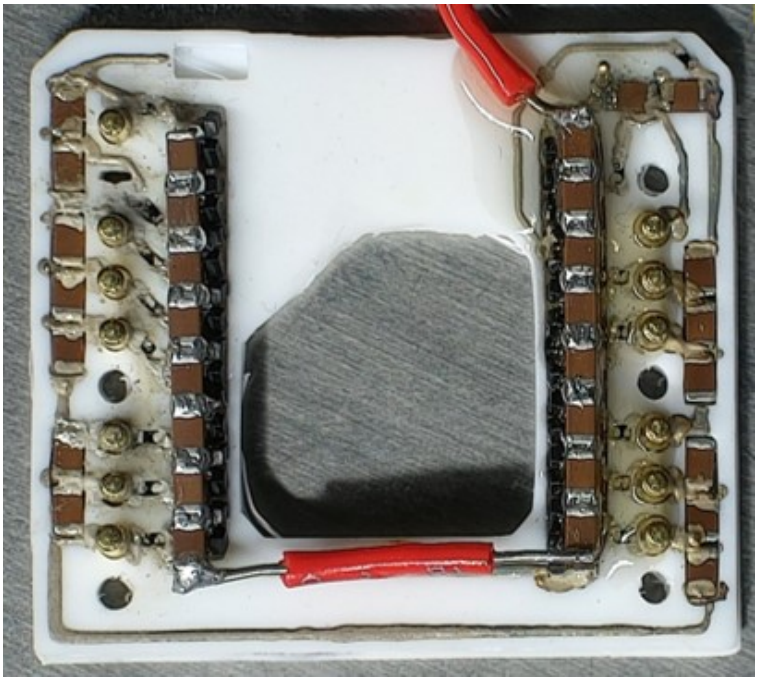


Figure 3.7: *The surface has been milled and components inserted into a CW Base, a short copper wire has been soldered across the CW terminals. Epoxy has been used to insulate the right-side dynode stages.*

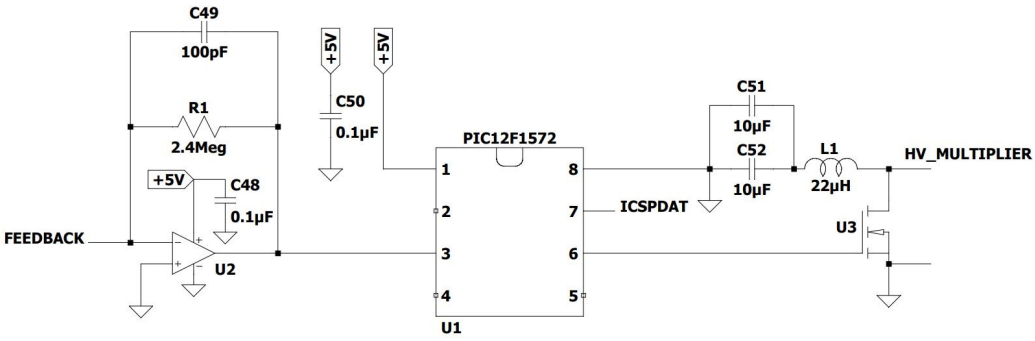


Figure 3.8: *The charge pump circuit, two 400 MΩ resistors are externally attached to the modular print in series on the feedback line for testing.*

Printing the HV control design, with bulk dimensions of 13.5 mm by 13.6 mm a lack of bed adhesion was observed. The triangular edges meant to mate to the space available in the CW base were especially vulnerable to delamination from the printer bed. To improve the printing of the edges, improve adhesion and prevent failure after multiple print layers, a 0.1 mm brim was introduced. The brim width was tested from 0.1 mm up to a maximum of 0.9 mm. The wider 0.9 mm brim expanded the surface area of the first layer by approximately

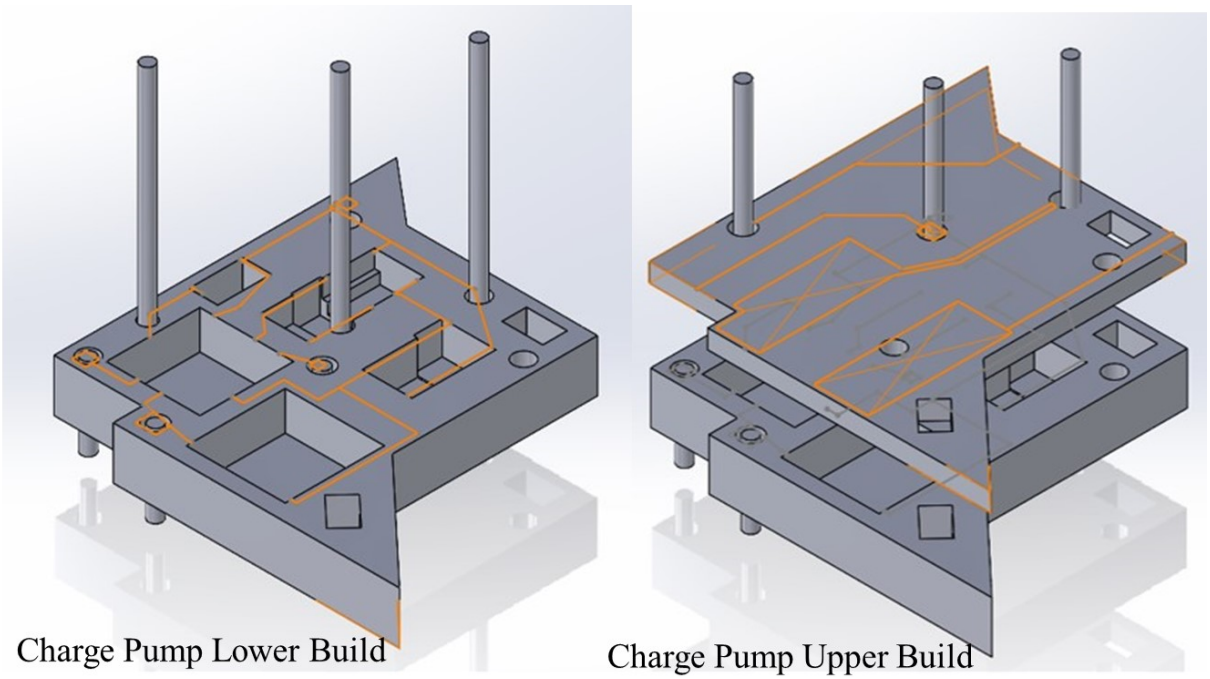


Figure 3.9: *Due to the constrained space available for the charge pump, the print was separated into two builds. Trace locations are marked in orange on the surface of each part. Holes were printed to insert pins which enabled programming and monitoring of charge pump operation.*

52 % and improved the adhesion at the edges by creating a rounded profile around the first layer. The brim could be easily removed after printing and did not modify any process steps aside from the initial printing. The brim was enabled for builds printed later to avoid potential adhesion failures. An example of the charge pump modular circuit print, without parts, is include as Figure 3.10.

After a series of trials using the silver paste sockets it was determined the connection provided was insufficient due to three factors

- The sockets vary in size dependent on location such that sufficient contact and fit is difficult to predict.
- The repeated use of the silver sockets induces stress throughout the part edges and can lead to material failure modes such as cracking.
- Contact between the pins and silver coating is difficult to maintain given unknown coating thickness and conductor distribution in the paste.

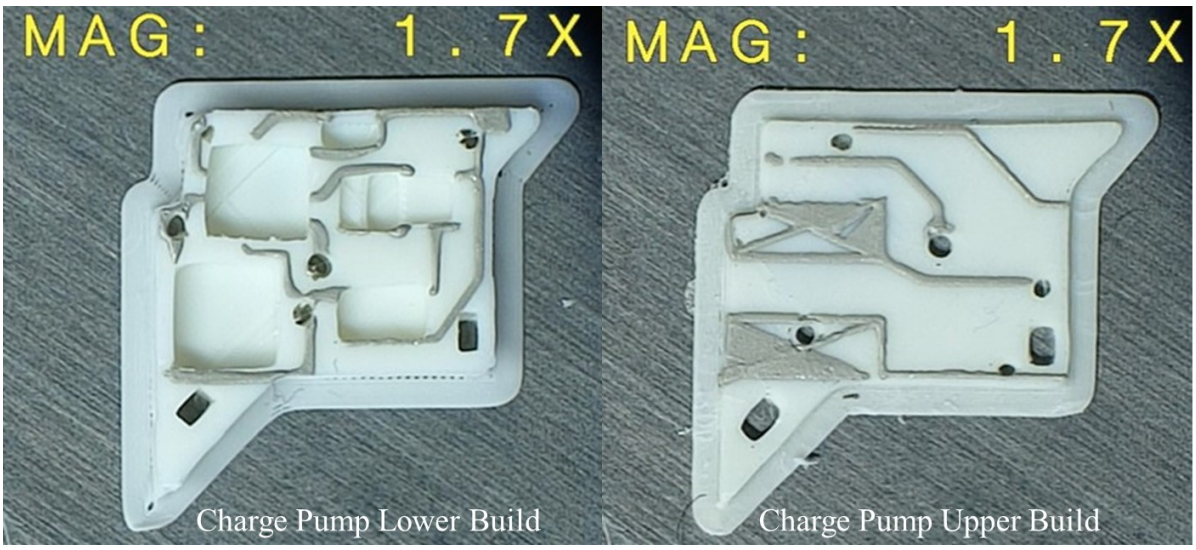


Figure 3.10: *An early print with some probe points omitted. The brim was left attached to show the required adhesion material.*

The modular testing approach confirmed operation of individual Cockcroft-Walton printed assemblies and modular HV control circuits. An obstacle to integrating separate modular constructions was the low volume available for mechanical connections between parts. In order to conserve build space, the design direction shifted to an integrated assembly by combining the HV control and the CW Base. Combining the circuits for printing was simplified by isolating each of the previously shown modular circuits within a single build for the final design. The circuits were electrically combined when the upper HVPS build was attached, connecting the inductor output to the Cockcroft-Walton multiplier inlet.

The electrical isolation of the lower HVPS build enabled the HV control circuit to be tested and reworked to confirm operation, prior to committing CW sub-assemblies to the sample. Additionally, by isolating the two circuit sections the source of connection errors could be limited to specific circuit areas during testing. The modular circuits were combined following the full circuit diagram adapted from previous work, shown in Figure 2.4.

The upper HVPS build depicted in Figure 3.12 connects the header pins to the CW Base circuit providing grounding for the full assembly. The +5 V input to the assembly is drawn from a via to the lower HVPS build rather than the center pin to increase available space on the upper HVPS build. The rightmost pin provides the raw signal output from the

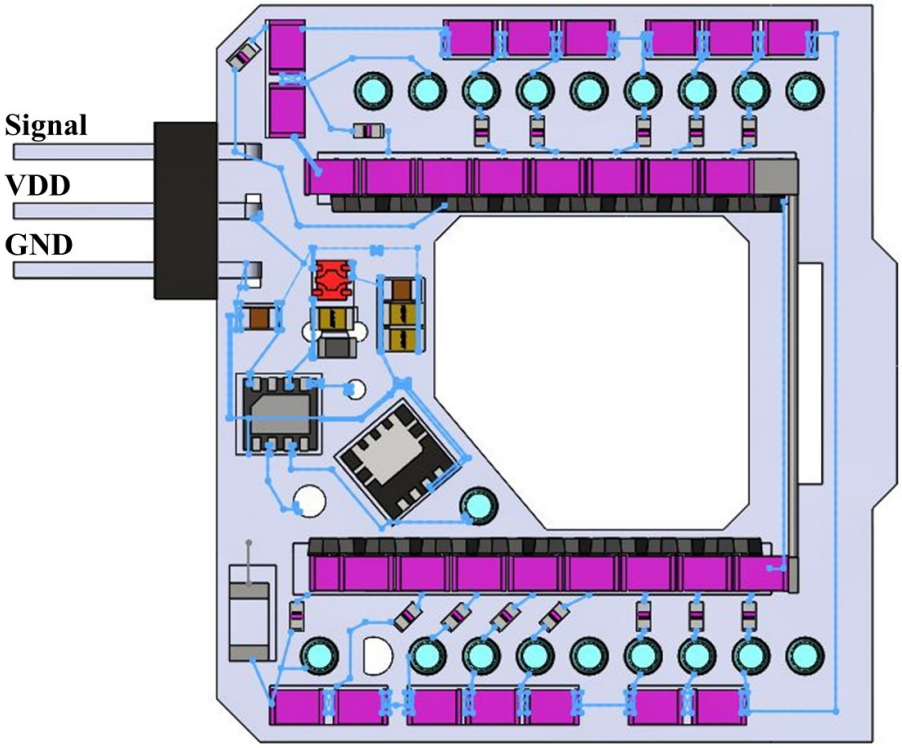


Figure 3.11: *The lower HVPS build of the integrated design combines the previous CW base and charge pump print. Square header pins are inserted to provide stable connections for testing equipment.*

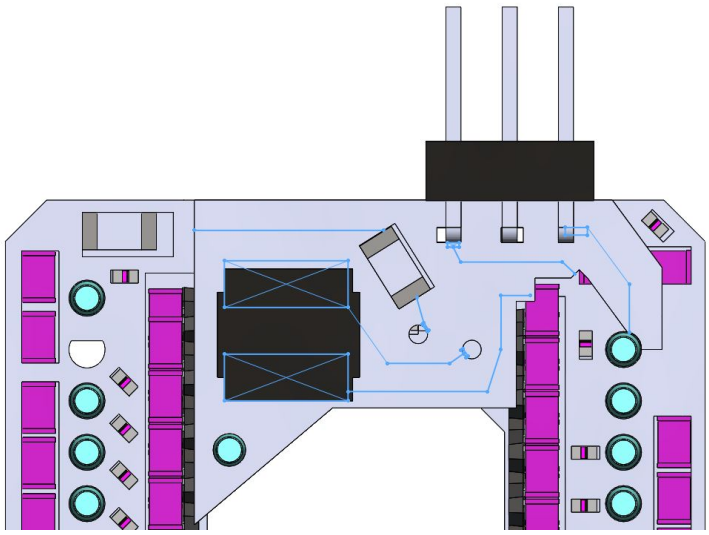


Figure 3.12: *The integrated design is structured as a two build design by using the upper HVPS build to hold the large inductor used by the charge pump circuit and one of the feedback resistors. Parts have been inserted and trace routing marked in blue.*

sensor and connects directly to the signal pin from the sensor. A concern when designing the control circuit in this configuration was the placement of the inductor directly above the feedback and control circuitry. The charge pump was expected to store energy in the inductor and push current to drive the Cockcroft-Walton multiplier. After each switch of the inductor grounding, ringing was expected at the inductor output. Repeated inductor ringing may effect surrounding circuitry through magnetic fields creating eddy currents within the assembly. The addition of a dedicated ground plane between the inductor and surrounding circuitry is recommended by Texas Instruments[26]. However, given the compact nature of the design there was not space available to include a large dedicated ground plane. Specific results relating to the magnetic effects of the inductor placement were not collected, however steps were taken to reduce potential effects from the package placement. The most sensitive feedback component was identified as the op-amp due to the current feedback of the circuit having a magnitude of nanoamps. From Figures 3.11 and 3.12 the op-amp, in red, is placed beyond the outline of the inductor package and the feedback line does not cross under the inductor. However, due to the close proximity of the feedback line to the inductor, one of the 400 MΩ resistors is connected near the via to the op-amp to increase the line impedance.

The assembled prototype in Figure 3.13 was coated with DP-270 non-conductive epoxy[27]. The signal pin for the final design was attached using a copper wire to improve mechanical support between the assembly sections. Prior to usage for equipment level testing the circuit in Figure 3.13 is potted in a protective cap to further increase the durability of the design and to insulate the high-voltage electronics. The housing was printed using PLA on an Ultimaker 3 Extended. The Ultimaker used a 0.4 mm extruder enabling larger builds compared to the high detail, slow build of the 3Dn-300. Leveraging the advantages of each printer the larger housing could be printed quickly on the Ultimaker 3, while the 3Dn-300 was used to generate the high-detail electronics package. The combined assembly is shown below, as Figure 3.14.

Settings which were considered significant which were modified from default values for ABS in PrusaSlicer are listed in Table 3.3. Individual settings were not extensively characterized however, settings listed performed sufficiently well for ABS on a PET surface with a coating of printing adhesive.

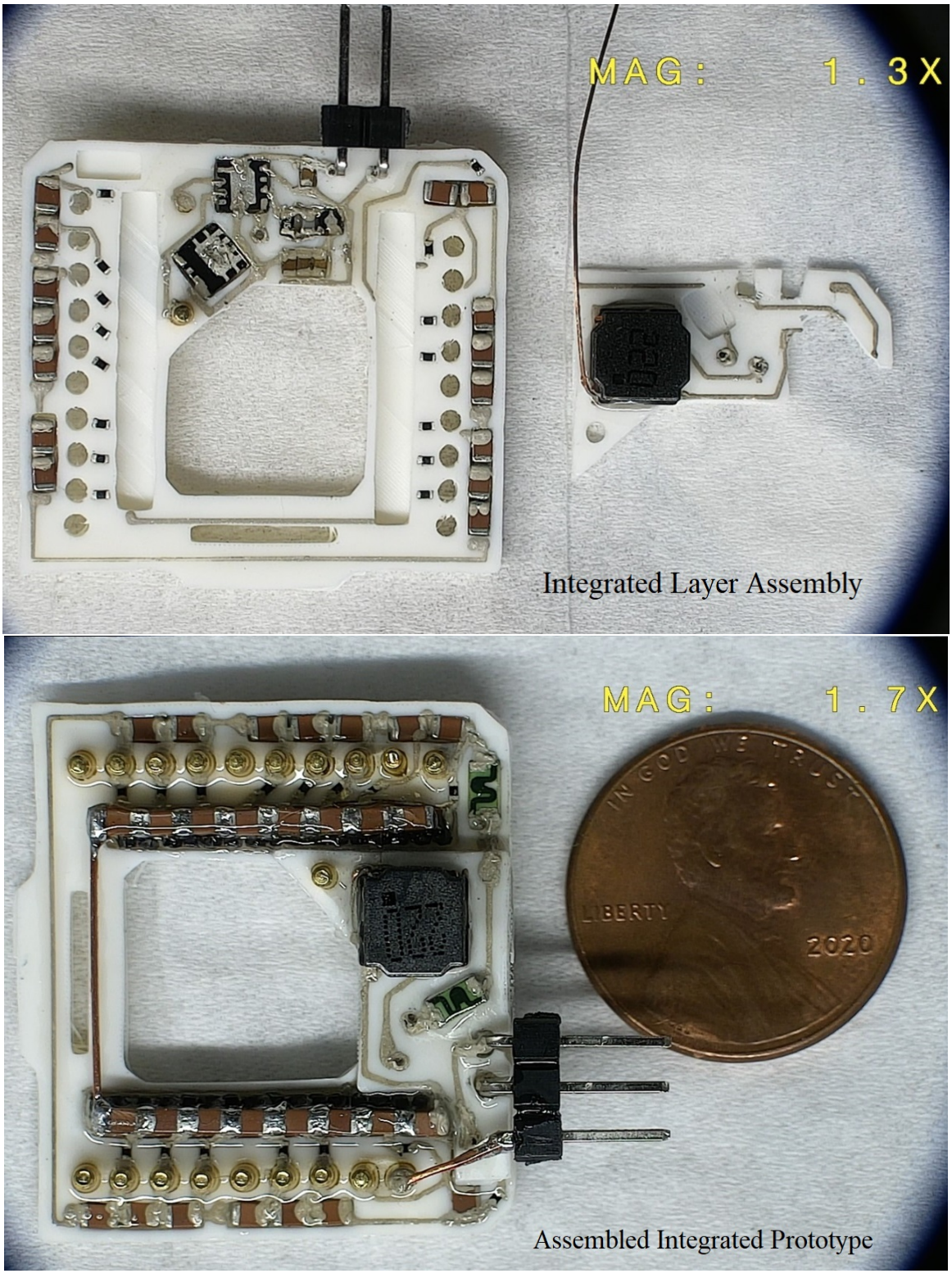


Figure 3.13: *The assembled integrated design, Top, the first layer circuitry is exposed, Bottom, the assembled build.*

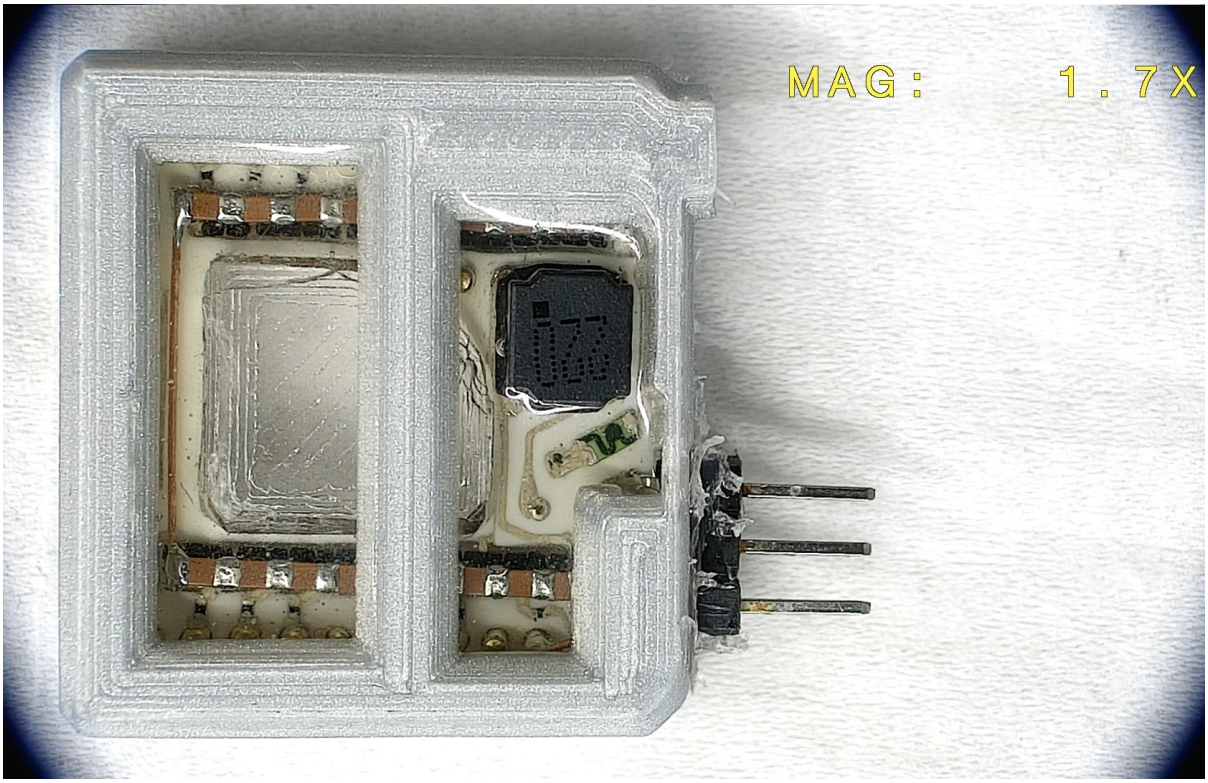


Figure 3.14: *The circuit has been encapsulated and filled with non-conductive epoxy, the header pins and dynode stage connections remain exposed.*

Table 3.3: *Subset of important print settings for use with the 125 µm ID ceramic tip in the construction of the finalized high-voltage circuits.*

Setting	Value
Nozzle Temperature	220 °C
Bed Temperature	110 °C
Perimeter Speed	1.2 mm/s
Small Perimeter Speed	1 mm/s
Infill Speed	4.5 mm/s
Infill	Rectilinear, 100 %
Layer Height	0.1 mm
First Layer Speed	25 %
Overlap (between printed roads)	10 %
Avoid Cross Perimeters	On
Brim	0.9 mm

3.1.2 Milling

For the construction of high-voltage circuits, designs must ensure that stresses due to high-voltage are minimized whenever possible to avoid unwanted high-voltage phenomena such as corona discharge and partial discharge. Corona discharge (CD) and partial discharge (PD) occur in high-voltage applications when the electrical field of a surface exceeds the dielectric strength of the fluid surrounding the conductor. When CD occurs the surrounding fluid becomes conductive and increases the load on the system. A PD can occur due to air voids in the conductor or dielectric which can begin to erode the surrounding dielectric material[28]. In order to minimize the occurrence of CD and PD, the number of areas with high potential gradients should be reduced[29]. High potential gradients can be formed by edges which do not have a rounded geometry. Due to the potential for voids and the inherent surface roughness created by the FDM process, potential gradients for traces and conductive surfaces should be reduced by creating rounded surfaces for conductive traces and connections.

In early testing the surface roughness left behind by fused deposition modeling resulted in jagged edges which may produce high potential gradients. Reducing surface roughness of the dielectric was required to prepare the surface for high-voltage operation. It was also expected that by reducing the surface roughness the pump head could be brought closer to the dielectric surface when traces were deposited, reducing the height of traces and improving the consistency of the trace width. One way to prepare the surface was through the use of a mill. The 3Dn-300 gantry end mill was incorporated into the hybrid process in order to investigate the milling of channels and entire faces of the FDM dielectric to create surfaces suitable for high-voltage traces.

In order to operate the mill a model was generated of the volume to be removed. The mill path was generated in SolidWorks and exported as an stereolithography file. The mill, accessed through the Machine Tool III interface, operates on the same g-code commands given by the slicer and software that controls the FDM path. Due to the nature of this operation reusing the same operating constraints as the FDM process, the depth is controlled by start location. The depth to be milled and the layer height is subtracted from the height

of the surface as Equation 3.1.

$$Starting\ Depth = Surface\ Height - (Mill\ Depth + Layer\ Height) \tag{3.1}$$

In Equation 3.1 if the layer height is omitted the software will add the programmed layer height as an offset from the surface, milling at a depth less than what is expected. This implementation also cuts from the bottom-up which results in only the first layer of the desired mill path cutting into the part. Subsequent layers will be cut above the print surface and did not impact resultant build geometry.

Additive circuits constructed by other groups implemented a method for trace deposition which avoided the surface roughness by milling channels[6]. A similar approach was taken initially in which channels were milled using a 305 μm OD drill bit similar in size to the desired trace width of 250 μm. Tests were conducted at depths ranging from a depth of 100 μm to 240 μm, an example of the 100 μm deep channels is included in Figure 3.15. Milling of the plastic surface was observed to bend the 305 μm bit when conducted at feedrates above 0.05 mm/s. For milling channels the bit feedrate did not exceed 0.05 mm/s and was limited to a maximum depth of 150 μm per pass to reduce friction on the drill bit. Preliminary testing was conducted with a spindle speed of 10000 and 20000 rpm, the higher rotational speed reduced the bending observed and was used for milling the channels.

The burrs observed in Figure 3.15 created an obstacle for filling the channels with conductive paste. To remove the burrs, additional milling routines were programmed to mill the channel up to three times. The repeated milling of the surface was thought to create smaller burrs by milling deeper incrementally, these smaller burrs may be removed by the next milling routine or be small enough to be negligible. A comparison between one milling routine and three milling routines of the same surface is included as Figure 3.16. The incremental milling was conducted with the first layer being 120 μm deep followed by two millings that extended the channel depth by 60 μm each. The larger first milling was expected to generate larger burrs and then be removed by the smaller incremental millings.

The visible burring observed in Figures 3.15 and 3.16 would cause significant irregular-

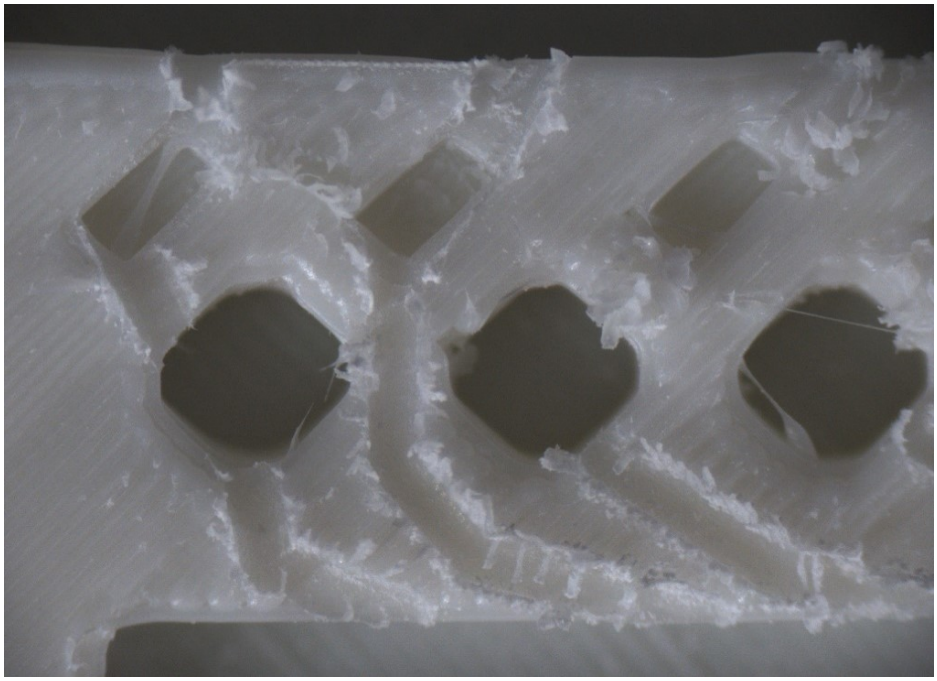


Figure 3.15: *The channels were able to be milled in the desired orientation. Visible burring impeded trace deposition and made the samples unusable. Additional melting or cracking along the mill path was not observed.*

ities in the trace deposition. The milling of channels from this test required an additional deburring process to be considered. The readily available processes to deburr the printed parts without removal from the bed were limited to

- Manual - using sandpaper or abrasive material to remove surface burrs.
- Reheating - melting of burrs back into the substrate material.

The use of manual deburring or reheating may reduce the dimensional accuracy of the part. If the nozzle were heated and passed over the part surface it was expected to reduce the appearance of burrs but, may redeposit the melted material onto the build surface. The most plausible method without significant modification to the printer equipment and housing was the use of an abrasive such as fine-grit sandpaper. If manual deburring was adopted, the process may become less repeatable dependent on variation from sanding technique. Neither method was expected to adequately remove the observed burrs without negatively impacting the resulting surface and deburring tests were not conducted. Ultimately, milled channels

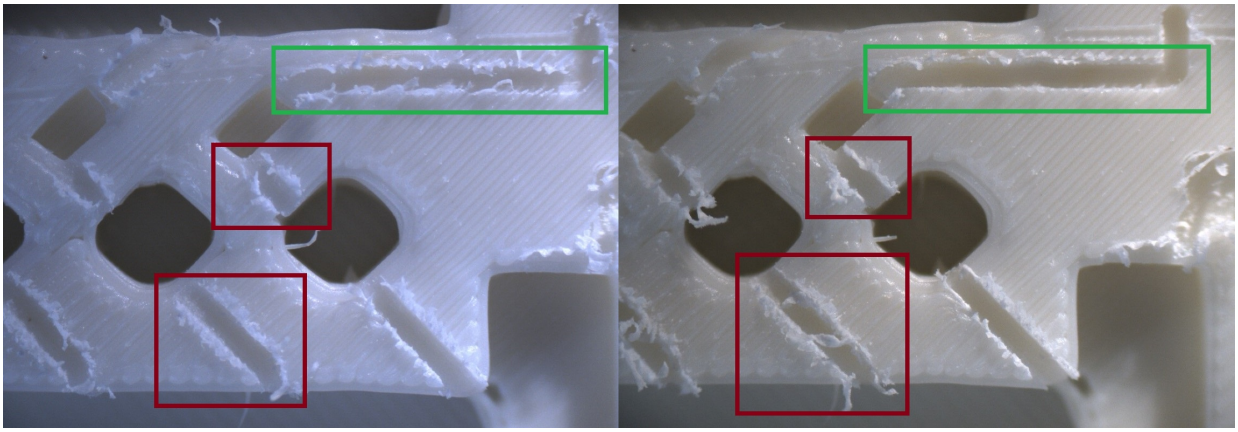


Figure 3.16: *A sample was viewed after each stage of milling, a comparison of a single sample with one milling on the left and the same sample after three incremental millings on the right. The area highlighted in green improved with a significant number of burrs being removed, the areas highlighted in red had increased burring after multiple mill routines were conducted.*

were not used due to the creation of burrs along the channel edges.

The bottom of the channels was observed to be free from burring. If burrs are created only at the edges of the mill bit then, if a face milling was conducted over the whole print surface the burrs would only occur at the part edges where traces are not placed. During milling burr formation is impacted by the size of mill bit used. Smaller diameter bits require more passes than larger diameter bits, in which each pass may generate burrs. Expecting a larger bit to reduce the occurrence of burring, a 3.175 mm (1/8") flat mill bit was selected. A larger bit was also expected to resist flexure during milling allowing a higher feedrate than the 305 μm bit.

Using the 3.175 mm bit, the feedrate was increased from 0.05 mm/s to 20 mm/s. The larger bit size was expected to generate more heat and forces on the surface, attempting to reduce these effects the spindle speed was decreased to 14000 rpm. The plunge speed was kept constant at 1.55 mm/s. To reduce thermal effects on the part such as warping and softening of the material, surface milling was performed when the bed temperature was approximately 40 °C or lower. A comparison of the surface before and after face milling is presented as Figure 3.17. A comparison of traces deposited on a milled surface and a surface without milling is shown in Figure 3.18. Milling two layers, 200 μm, was determined to be

the most advantageous as surface level defects such as the extruder tracks and distinct ridge formation are removed. The milling of less than two layers allowed certain defects from the surface to remain or create small burring in areas where extruded material was not properly fused.

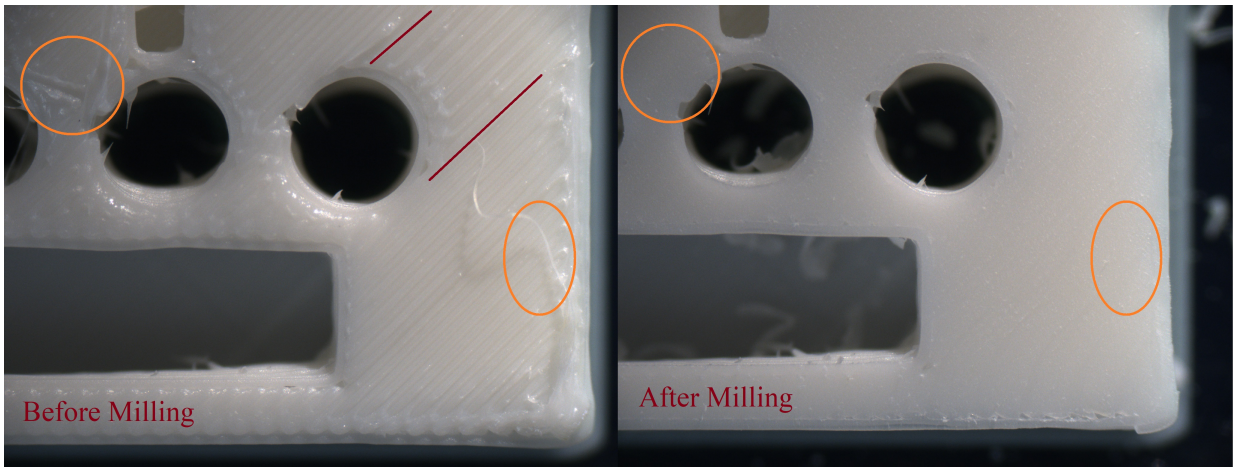


Figure 3.17: *The sample before face milling on the left, and after removing 200 µm by milling on the right. The surface defects and stringing observed before milling are shown to be completely removed on the right. The ridge pattern highlighted by the red lines is not present after milling.*

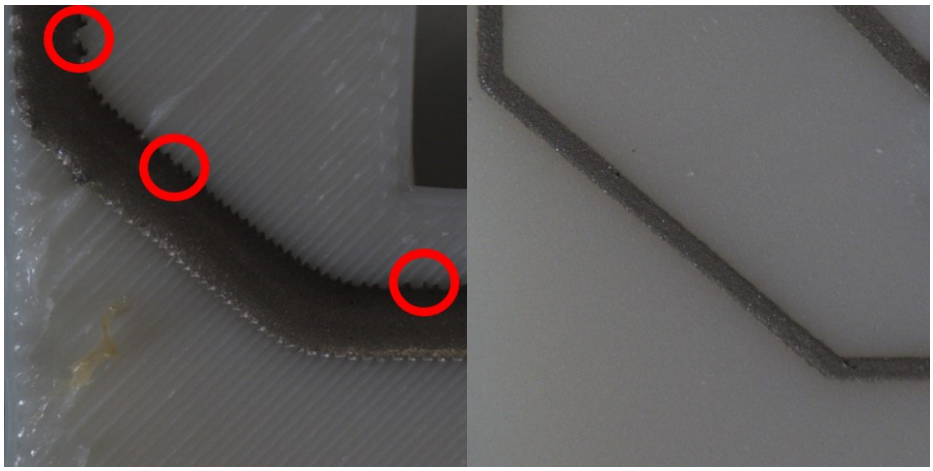


Figure 3.18: *Trace material deposited on a surface without milling, left, similar material deposition on a surface after having undergone surface milling. Both samples were printed using a 125 µm inner diameter ceramic nozzle. The milled surface with ridges removed, allowed the nozzle tip to be closer to the surface and improved control over conductive material width and height during deposition.*

In Figure 3.17 the surface ridges have been visibly removed without the creation of surface

burrs previously observed from the milled channels in 3.16. Small debris left from milling can be observed in Figure 3.17. The debris left from milling are scattered within the printer housing, requiring the housing to be cleaned prior to continuing production. The debris were removed via suction selectively applied to the build surface and individual builds.

To accommodate surface milling, additional material is added to the height of each part increasing the number of layers to be printed. However, since obstructive surface geometry is removed by milling, the speed of the extruder used for FDM may be increased. Print time for the samples with surface milling required an additional 47 minutes, the milling required 10 minutes for leveling and execution. The channel milling was conducted on samples which were approximately one-third the required trace routing, milling channels using the 305 μm bit required approximately 57 minutes. If the printing of two additional layers and removing them required 57 minutes, compared to milling one-third of the required channels, the time conserved by conducting a 0.2 mm face milling on the surface becomes significant. Milling 0.2 mm from the upper surface of the part was considered the best method to prepare the printed surface for traces usable with high-voltage in this work from the methods tested.

3.1.3 Pick-and-Place

A pneumatic pick-and-place (PNP) was attached to the 3Dn-300 tool plate enabling automated placement of electrical packages into the printed assembly. The PNP used replaceable EFD needles to pick the components using pressure. A 0.41 mm ID x 0.72 mm OD x 12.7 mm long flat-ended needle, referred to as EFD, was attached to enable the pick-up of necessary electronic packages. The electronic packages for the build included 0805, 0603, 0402 and integrated-circuit (IC) components.

The pick-and-place used .xml files that were generated on the machine through the printer interface software. Placement routines can be programmed using the laser height sensor or the gantry camera. The laser was insufficient for aligning the components into each build since component orientation and slot position could not be observed. The camera allowed component and slot orientations to be observed directly and camera focus was used

to determine the placement heights. Individual components were first brought into view on the tool screen as shown in Figure 3.19.

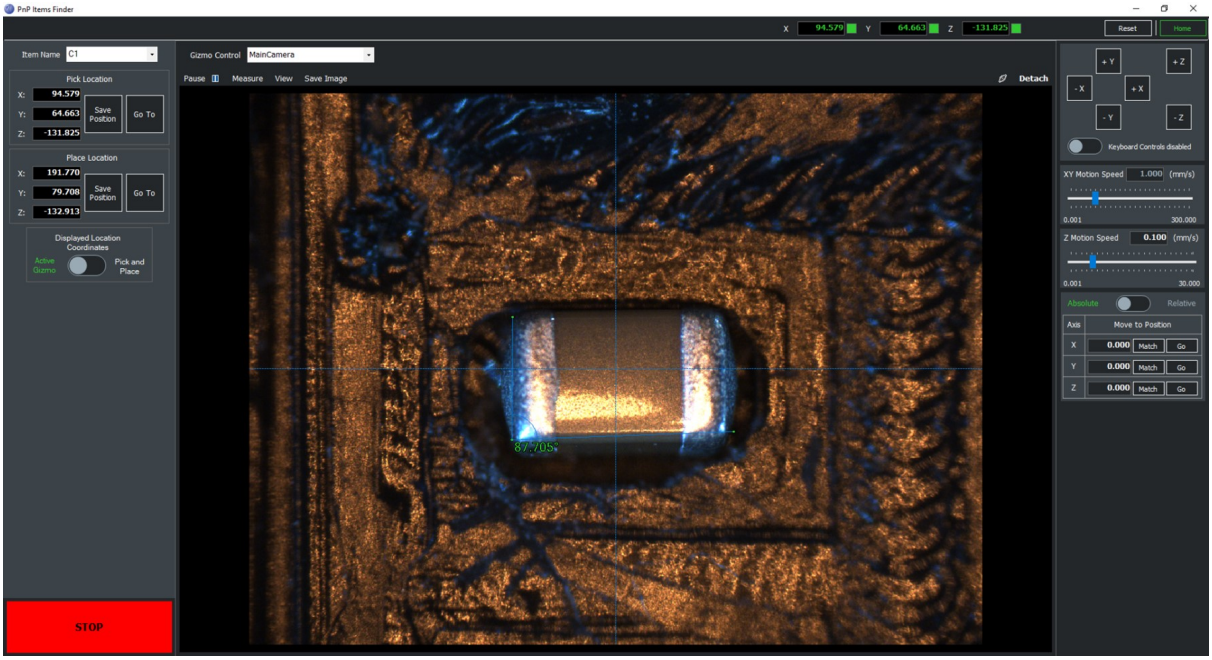


Figure 3.19: *The component center is aligned with the camera cross-hair, the PNP head will pick the component from the location of the cross-hair. An angle measurement is measured in software and displayed on the screen.*

From Figure 3.19, component position was observed and the head is aligned with the center of the component. The crosshair visible on the tool window is used to align the PNP head center with the component, the camera position was saved. Offsets relative to the PNP head are applied from the tool calibration. When determining the location to place a component, the component dimensions must be retained during movement. There was not a readily available method to retain the component dimensions however, using the angle measurement tool, two sides of the component could be retained during movement. The angle measurement tool is shown below as Figure 3.20, over the slot to place one of the capacitors. The graphic persists during camera movement. While the camera remains focused at the same view height, the dimensions observed were consistent between locations.

From Figure 3.20 the measurements are aligned with the placement location. Depending on the camera focus the edges captured with the measurement tool may vary from the

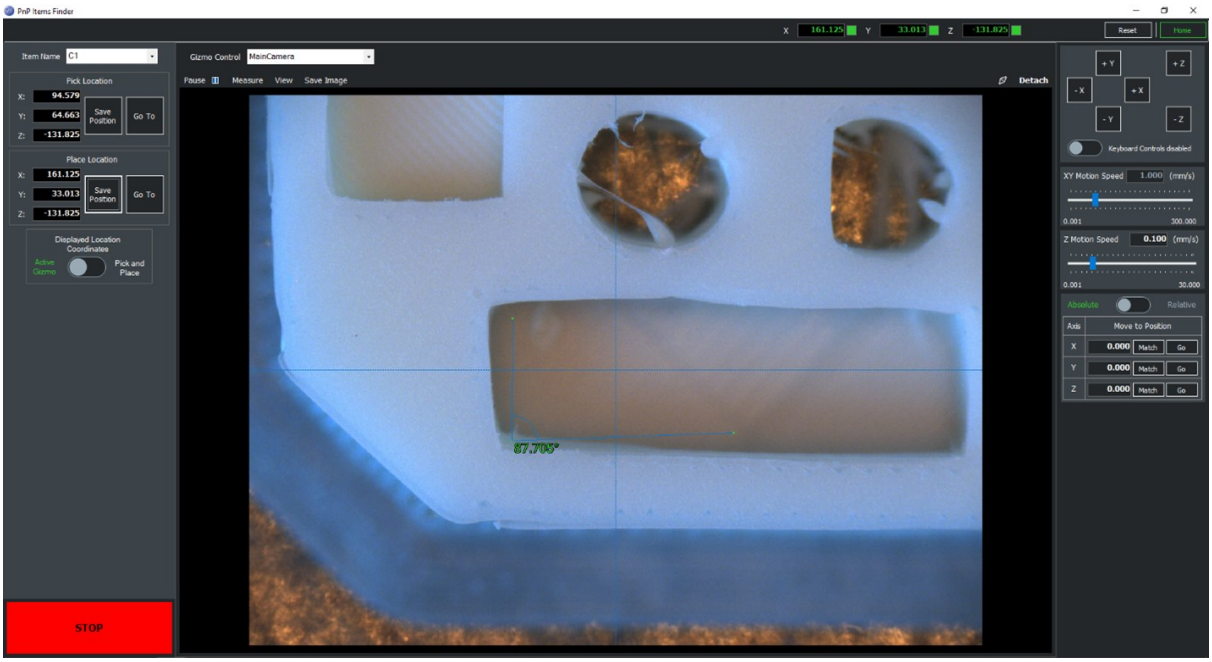


Figure 3.20: *The angle measured around the component is moved to the expected placement location.*

actual component. To ensure the component is fully inserted, the camera should be focused on the slot, if the camera is too high or too low it will result in the component not being fully inserted during execution or the component receiving extra pressure. For consistent placement height the camera height was kept constant for each series of components with similar package dimensions. The height was changed between the 0805 components, the charge pump integrated circuits, 0603 components, and the 0402 resistors. Once the pick and place locations are saved to the .xml file, the placement routine is started, automatically placing components into the build at the designated locations. Due to slot differences and errors encountered during the pick up or placement of components some may not be properly aligned.

The tolerance for printed slots was generated in two stages as: maximum component sizing from the manufacturer data sheet; and experimental tolerance for automated placement via PNP. The component tolerance from the data sheet was incorporated as the maximum size for each dimension. Parts were printed with the maximum tolerance and a series of test fits conducted. Given proximity between external perimeters and other component slots tol-

erances for printing were developed on a slot-by-slot basis. Slots with separation of at least three printed roads had reduced interference from adjacent slots. The variability caused by FDM also requires the tolerance to be widened to accommodate the changes which can occur throughout printing. The oversized slots which allowed parts to be placed, were coated in non-conductive epoxy, DP270, prior to performing the component placement, both insulating the side of the component in the slot and preventing movement of the part after placement and curing[27]. Working from the tolerance required to insert the component consistently, an additional tolerance was added to each slot based on empirical testing of samples with varying slot dimensions. Specific tolerance changes and accuracy of the PNP are covered in detail in Section 4.1.2.

3.1.4 Topographic Laser Scanning

Reducing the distance between the pump nozzle and the surface was considered the next step to improving control over the deposition of the trace material after using face milling to remove obstructive surface roughness. It was possible to manually set the deposition height however, to improve the repeatability of the process an automated approach was desired. Previous researchers have used laser scanning to set the material deposition height. This method involves scanning the build surface which enables the software to print material on a variable print surface, commonly used for printing on contoured surfaces[30;31]. The tool path is generated from a series of data points collected along the surface and stored in a point cloud format. The tool path generated is expected to account for the surface height more accurately than what can be performed manually, resulting in increased repeatability. In order to accurately set the layer height for trace deposition, a series of parameters for laser scanning were investigated.

For this study the 3Dn-300 printer used was equipped with an LK-H082 laser distance sensor from Keyence. The laser is fixed to the right edge of the tool plate and enables the printer gantry to scan parts to generate point cloud data files. The data stored in these files consists of the X, Y, and Z position of the scan and is output in a plain text format. Using

the Machine Tool III interface the operator can scan over a rectangular area of custom size at a set speed using the scan job screen, shown in Figure 3.21. When overscan is enabled an additonal set of points is collected along the perimeter of the scan positioned one resolution unit from the set X and Y scan size. The scan direction could be chosen from eight available options, for this work the scan direction was kept constant starting from the bottom left corner and ending at the top right corner, shown selected in Figure 3.21. The position to be scanned is set from another menu and can be moved within the build area, but not all areas within the build plate can be scanned due to the position of the laser sensor on the gantry.

Figure 3.21: *The operator can select the orientation to scan from, the speed of the scan, and whether to enable stops. When stops are enabled the printer will pause at each mesh node and collect data points until the measurement stabilizes.*

The LK-H082 has a laser spot size of 70 μm, this limits the use of the laser to features larger than 70 μm[32]. However, scans may be conducted at a finer meshing if more measurements within a region are desired such as for oversampling. The scanning routine stores data in memory prior to writing data to a file at the end of the process, this can result in large overhead memory usage during the process. When scanning without stops this functionality did not generally effect performance. When stops were enabled data is collected until the

measurement at a point stabilized, data collected prior to stabilization at a point appeared to be stored in the memory overhead, significantly impacting performance for large scans. During testing of fine meshes, a 30 micron grid spacing over a 28 mm x 30 mm area was scanned with stops enabled resulting in the software storing over 13 GB of data points before causing the software to crash. A scan with the same parameters was attempted with stops disabled and was able to be completed without incident within 8 hours and 21 minutes. The fine mesh scan was rendered as Figure 3.22.

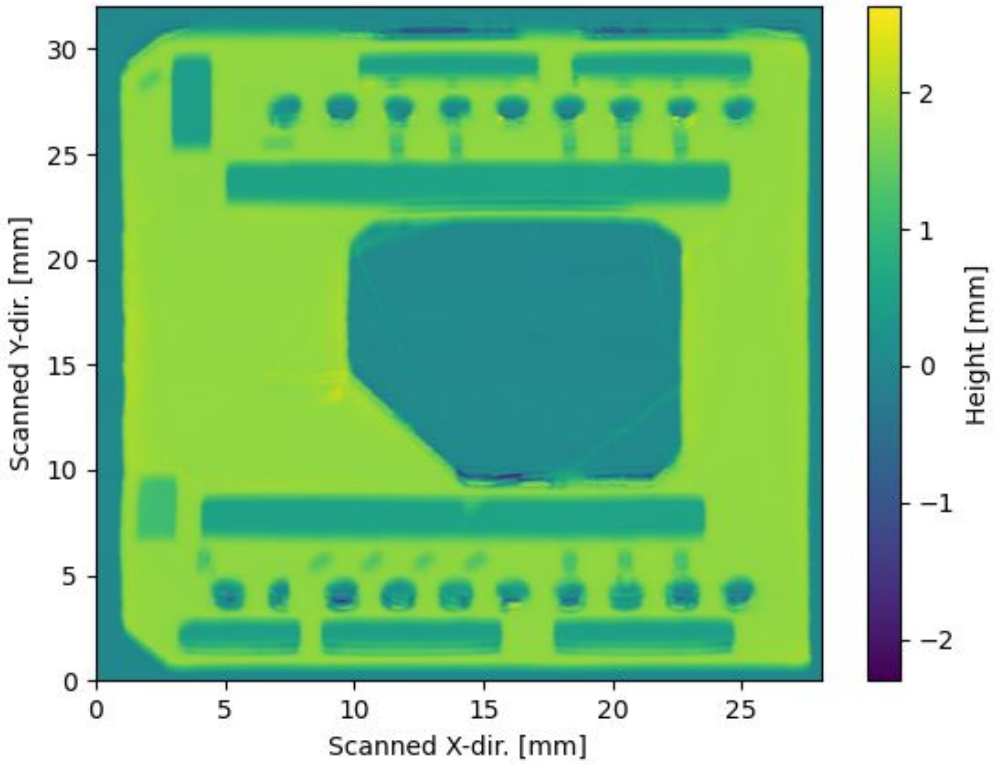


Figure 3.22: *A scan of a CW Base in Figure 3.6 using 30 µm grid spacing at a speed of 1 mm/s without stops.*

A detailed scan has potential as a validation of surface geometry versus the triangulated mesh from the SolidWorks model. In Figure 3.22, values below zero can be observed near edges, these edge effects can register a range of values including those which cannot exist. The presence of these outliers may create obstacles to scan utilization unless they are corrected. However, the purpose of scanning was to determine the height to print trace material and specific slot depths were not required. The large scan time and quantity of extraneous data

made a scan of the slotted geometry an unnecessary process.

In order to capture only the required surface geometry, the homogenized surface height, the printed surface geometry was covered in material to prevent the scanning of slots. The first material used was standard paper with a thickness of 0.066 mm. The paper was cut to cover the expected part area and extend over the part edges to be secured with adhesive. When scanning the material it became clear that the curvature of the paper would create an obstacle to a consistent height reading. An example of the curved scan surface is shown in Figure 3.23.

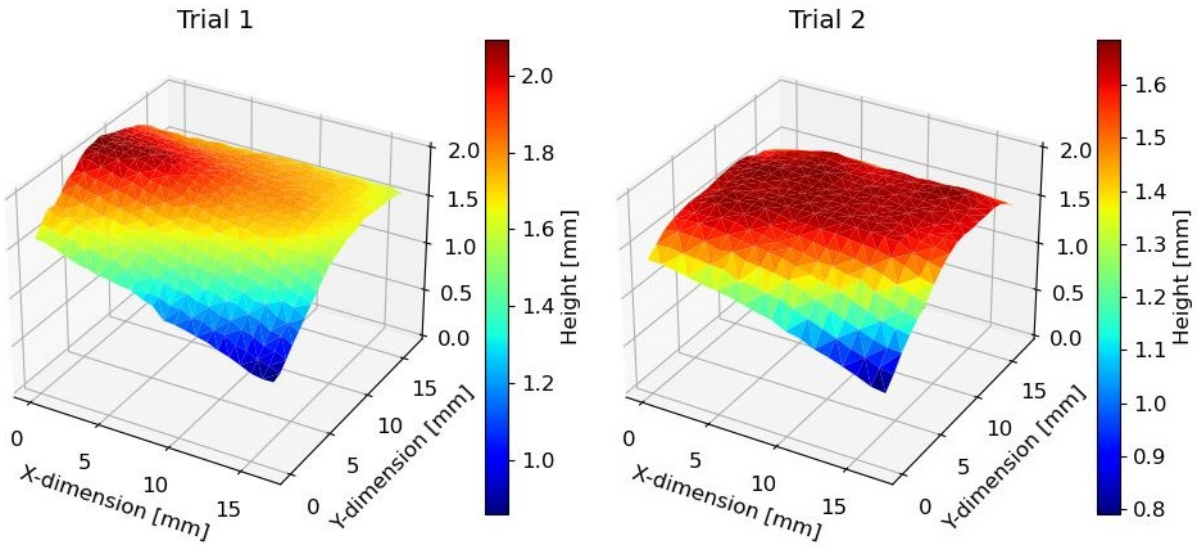


Figure 3.23: *Trial 1 shows the scan result if the part is small or if the paper is not stretched far enough. Trial 2 demonstrates the desired application of the paper covering, with a moderately homogeneous surface.*

The curved surface observed from the Trial 2 scan in Figure 3.23 appeared closer to the expected part surface compared to Trial 1. Relying on the approximation of the paper height without considering the curvature would not be sufficient to place the nozzle incident with the part surface consistently. A material which was more flexible and thinner was desired.

The second material used during scanning was an 80 gauge (0.02 mm) plastic film. There were concerns that a clear film would impact the laser scanning accuracy, thus a semi-opaque white film was chosen. The film was extended over the part surface and secured at each edge with adhesive. A scan over the material yielded a homogenized surface height shown in

Figure 3.24, with distinct edge locations. Additionally, two scan methods were attempted, a Quick scan and a Reduced scan. The Quick scan used a speed of 3 mm/s and almost twice as many points as the Reduced scan, stops were disabled for this routine. The Reduced scan was conducted at 3 mm/s and had stops enabled to determine if the excess time required to stop and scan resulted in an accuracy improvement.

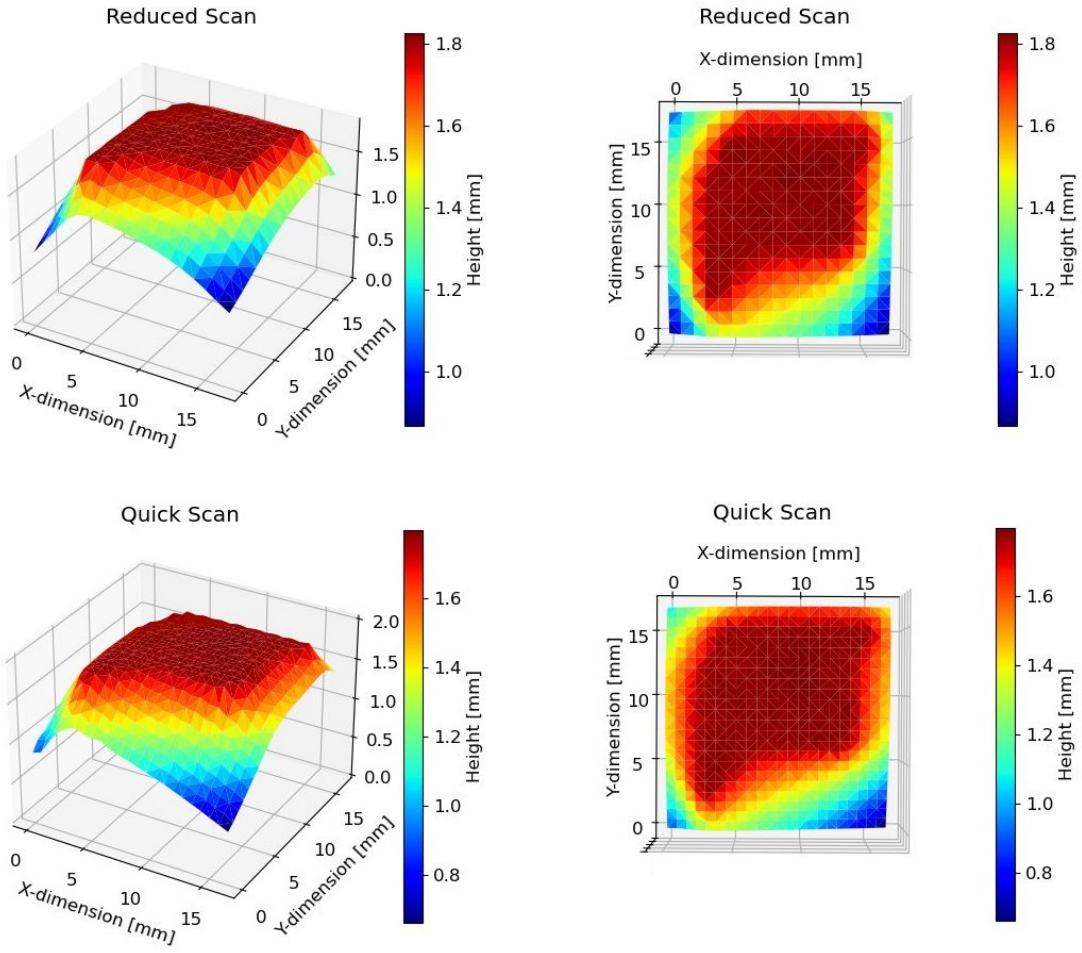


Figure 3.24: *The Reduced and Quick scanning methods between parts of the same batch. The number of points can be observed from the vertices in each mesh with the Quick scan having almost twice as many nodes.*

Comparing Figure 3.23 to 3.24 the previously observed curvature was minimized, part edges are also more visible using the flexible plastic. For a 17 mm x 17 mm scan with spacing of 0.75 mm for the Quick scan and 1 mm for the Reduced scan, the scan time was approximately 2 minutes and 30 seconds in both cases. The expected height of the modeled

part was 1.6 mm after milling. Variation in the actual part height is expected from FDM, and a difference of less than 0.1 mm between scanned parts is acceptable. For small parts such as the 17 mm x 17 mm scan used in Figure 3.24 the scanning methods were considered equivalent. From the results in Figure 3.24 and the increased overhead previously observed by enabling stops during scanning for finer meshes, stops were considered unnecessary for scans at 3 mm/s or slower given that the observed geometry from the scans possessed a homogenized surface height. For scans consisting of few points such as those using 0.75 mm gird spacing or larger, scanning without stops also enabled a greater number of points to be gathered in a similar time in addition to having comparable accuracy performance to observed in the Reduced scan in Figure 3.24.

During the manufacturing process a simplified scan is conducted using the results from the Quick scan trials. The implemented scan technique for prototype production was a scan at 3 mm/s with 1 to 2 mm grid spacing with stops disabled. For the previously mentioned lower HVPS build the scan area was 28 mm x 30 mm, and the upper HVPS build used a scan area of 18 mm x 23 mm. An example of the sample preparation is shown below, in Figure 3.25.

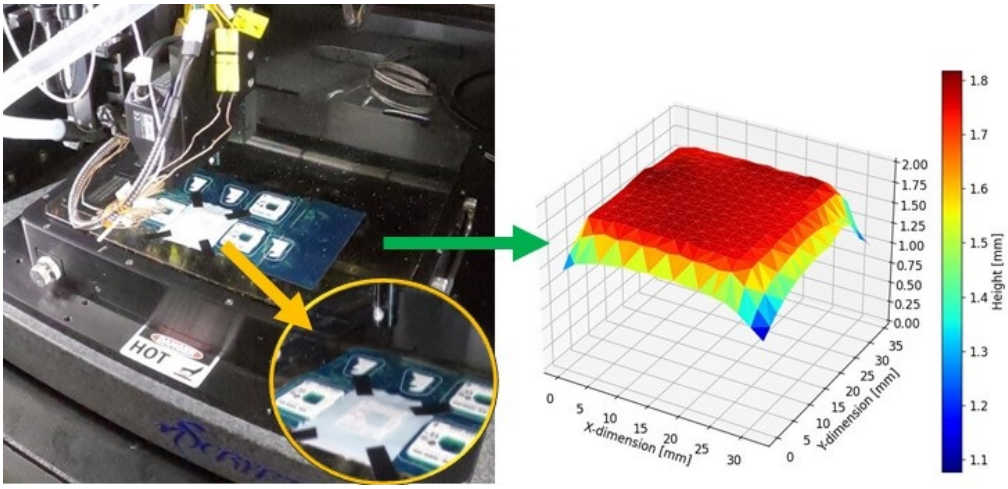


Figure 3.25: *The covered build is scanned and the point cloud data can be inspected for irregularities.*

3.1.5 Conductive Trace Printing

The printer software Machine Tool III enables the SmartPump to deposit conductive material on the surface by following instructions generated from a Drawing Exchange Format (DXF) file. A path to deposit material is referred to as a dispense job and contains the path and printing parameters for deposition. CB028 conductive paste was selected for testing, consisting of suspended silver particles as the conductor[33]. The conductive paste was applied using a 125 μm ID / 175 μm OD ceramic nozzle, and through the use of 100 μm ID / 240 μm OD flat-ended needles, referred to as EFD. Each of the chosen tip sizes was selected based on required trace size and manufacturer recommendation that the inner diameter be at least ten times the largest particle size[34].

CB028 was refrigerated in a standard refrigerator to prevent curing, it is removed from refrigeration within one hour before traces are applied. CB028 was loaded into the dispensing system using 3cc syringes which are mounted to the valve body. Fully loaded 3cc syringes may be used across multiple samples and were repeatedly refrigerated and thawed. The syringes were considered single-use and were not refilled. Once the material has been injected into the 3cc syringes for use it cannot be mixed with the available equipment. For prolonged storage the small syringes are rotated to prevent the silver particles from settling at one end of the syringe however, specific distribution of particles or viscosity of the paste was not monitored.

It was observed that over time the CB028 conductive paste may have particles settle and particles exhibited visible separation throughout the syringe. Given the unknown distribution of the conductive paste and necessity to disassemble and clean the valve body including the replacement of O-rings between separate production runs of parts, the required extrusion pressure experienced significant variation. For the 125 μm ID ceramic nozzles, a pressure of between 10.5 - 24 psi was required, extrusion at 12 psi occurred most often. For the 100 μm ID flat-ended EFD needles, a pressure of between 25 - 65 psi was required, with extrusion at 25 psi occurring most often. Traces were deposited when the bed temperature was between 22 °C and 40 °C in both cases. The lower pressure required for the ceramic tips

was thought to be due to the taper in the nozzle being more acute than the taper present in the EFDs used. Additionally, the EFD ID was 20 % smaller than the ceramic nozzles which likely increased the required extrusion pressure. The ceramic tips were cleaned and reused between production runs. The EFD tips were considered single-use and exchanged at the end of each day in which traces were printed.

The interface for the pump allows the operator to choose the valve position, valve speed, and the pump pressure. The pump movement may also be set using the job settings from another window. An example of the general settings shown for a dispensing job and the settings usable from the main panel are shown in Figure 3.26. The start position of the pump within a path set for trace deposition and deposition order cannot be changed from the SmartPump interface.

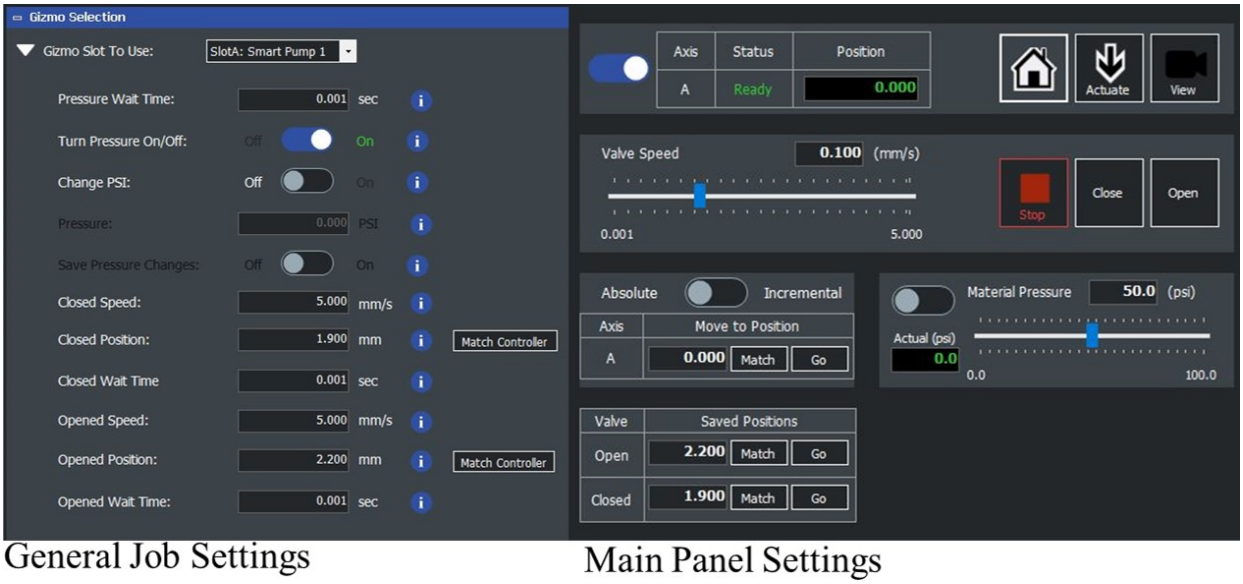


Figure 3.26: *The general menu from the dispense job is shown on the left, it allows the operator to set the pressure behavior and internal valve parameters. The main panel settings shown to the right allow the operator to change the pressure and to set the valve position.*

When preparing to deposit traces, the printer software Machine Tool III, displays an overlay of the extrusion path, an example of which is shown in Figure 3.27. The extrusion path includes arrow indicators of the deposition direction for each line in the DXF file, but it does not allow the operator to change the order or parameters of an individual extrusion within the generated print path. The displayed path represents the expected motion of the

pump, and variation can be caused by print misalignment and curvature in the extruding EFD. The trace print must be aligned by the operator, which depends on the geometry of the trace design developed and as such the reference point for the DXF file may vary. Alignment of the trace motion path was conducted experimentally by aligning a known trace edge to a known geometric feature on the build surface. For parts 0805 and larger, this method enabled connection of most surfaces. However, when aligning the trace motion path, variation was incurred through the manual alignment method which did not function well for the connection of components with pads 0.125 mm^2 and smaller such as those on ICs and 0402 components.

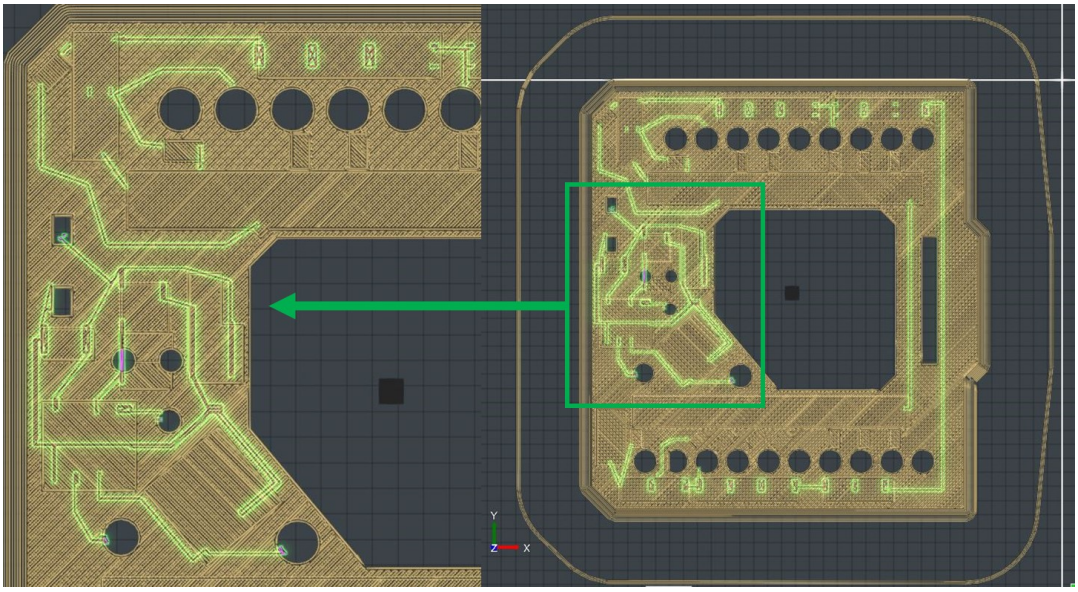


Figure 3.27: *Initially, the trace deposition path is manually aligned with the dielectric print. Further adjustment may be required depending on printed model accuracy versus the computer generated model.*

The expected trace path shown in Figure 3.27 have been aligned based on the expected dimensions of the dielectric model and layout of traces. When the trace material is deposited, any inaccuracies in the dielectric dimensions and any variation in the pump will change the traces produced. Since only objects to be printed are shown, specific pad locations for individual parts could not be determined. Since the preview of the trace deposition path did not include component surfaces, test runs were performed to determine the necessary alignment of the trace connections.

The desired trace width for the high-voltage sections of the circuit was 0.25 mm, if space was available the trace could be widened to reduce resistance during transmission. A primary constraint was the uniformity of the traces, ensuring no jagged edges occurred. PD and CD were previously discussed, reducing the number of high potential gradient surfaces was critical for manufacturing. Trace deposition parameters were discussed, surface preparations were previously covered in Section 3.1.2. Visible jagged edges are presented in Figure 3.18, demonstrating the importance of surface preparation in this study.

During testing it was observed that when the extruder was above the print surface a distance greater than the inner diameter of the nozzle, and the paste did not attach to the surface as it would accumulate on the nozzle tip. In order to deposit more uniform traces and to avoid buildup of material on the tip, an objective during printing was to print as close to the surface as possible without contacting the surface.

Another concern during extrusion was to avoid potential obstacles. Due to milling, plastic obstacles were removed in a majority of cases; however, the presence of electrical components created a risk of tip fracture for the ceramic nozzle. The EFD needles would bend when encountering an obstacle and recover. Whereas, the ceramic nozzles fracture and are rendered inoperable if a collision occurred. As printing progressed it became necessary to print over component surfaces or in close proximity to raised components. The downtime and costly replacement created by collisions with the ceramic tip made using EFD needles more feasible in testing as they were significantly cheaper than the ceramic nozzles and provided similar printing performance.

In the high-voltage control circuit, the traces connecting the +5 V supply to the inductor and the inductor to the MOSFET were of specific concern. These traces required additional volume to ensure that the resistance was as low as reasonably achievable. If the trace supplying voltage to the inductor became thin, the inductor will supply too little current to sustain high-voltage operation. Meanwhile if the trace from the inductor to the MOSFET becomes constrained the supplied voltage reduces in magnitude. Other failure modes of the charge pump circuit included becoming decoupled from the feedback, the design becomes unstable and will reach the breakdown voltage of the MOSFET leading to device failure. In

order to mitigate the catastrophic failure modes, traces around the MOSFET and op-amp of the design shown in Figure 2.4 were inspected thoroughly and reworked as necessary to ensure operation.

Trace routing on inclined surfaces was conducted to determine if usable traces could be deposited on printed inclines without surface treatment. An inclined surface could not be milled due to constraints from the three-axis mill configuration. Tests were performed with inclines which were 45 and 35 degrees from the plane in which layers are deposited. An example of the inclined traces is included as Figure 3.28. In order to print on inclines, a scan was generated and used to approximate the angled print surface. The stepped incline produced from the FDM layer construction process created an obstacle during trace writing. When the print head contacted the surface a thinner extrusion was printing up the incline, and wider extrusion was printing when traversing down the incline. For high-voltage applications this was of particular concern due to acute geometry generated as the paste settled into the individual steps. Using the circuit layout developed, it was determined that the addition of inclined connections would not improve the resulting prototype due to the jagged traces formed from the incline steps and minimal space conserved when using 35 degree inclined surfaces.

The trace deposition consisted of routing over dielectric material and the connection of individual components. 0805 and 0603 parts were connected, however, smaller parts were not. Connections to 0402 resistors and to ICs were attempted but, were generally unsuccessful. The larger pad size of 0805 and 0603 components compared to smaller 0.125 mm^2 pad size present on 0402 and IC packages allowed the conductive material to connect more often. General slot tolerance for components is discussed in sections 3.1.1 and 3.1.3, specific slot tolerances are discussed in Section 4.1.2 in reference to the FDM and PNP processes. The resulting gaps between the component and the slot edges were an obstacle to connecting parts through direct write. One method to mitigate the effect of the gaps was when priming the slots with non-conductive epoxy, where a portion of the gap could be filled with epoxy. Reducing the depth of the gap assisted in preventing unwanted shorting across components. Reducing the depth of gaps did not significantly improve component

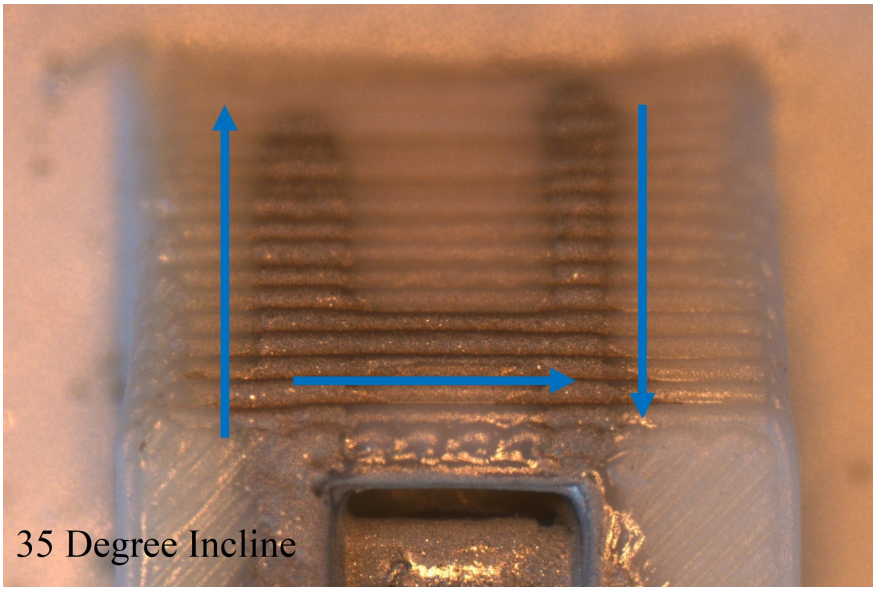


Figure 3.28: *Inclined surfaces were evaluated for trace routing feasibility. The 35 degree incline was measured from the build surface. Blue arrows indicate print direction.*

connection for the IC components. To improve accuracy of connections to components pads 0.125 mm^2 and smaller would require a closer estimate for trace positioning. Variation in printed slot position and aligning the trace deposition overlay in software complicated connection to small components in this work. In order to address disconnected components, the circuit connections are reworked using CB028 conductive paste and cured at 22 °C. If the slot tolerance required for the pick-and-place could be reduced, then the success rate of IC connections may increase.

3.2 Electrical Testing

Tuning the microcontroller regulation code and electrical testing procedures are discussed.

3.2.1 Controller Tuning

The high-voltage supply is regulated by augmenting the pulse-width-modulation (PWM) from the microcontroller used to switch the MOSFET gate. Switching the MOSFET using different voltage values allows the charge pump in Figure 3.8 to push varying quantities of

current into the Cockcroft-Walton multiplier. The quantity of current supplied from the charge pump into the multiplier is set by the feedback read by the microcontroller. To evaluate the feedback loop, Ohm's law must be introduced as Equation 3.2.

$$V = IR \tag{3.2}$$

Applying Equation 3.2 to the feedback circuit, the feedback current is converted to a voltage using the two 400 MΩ resistors and amplified by an inverting op-amp. The regulation target or voltage set point, Vset, in units of microcontroller analog-to-digital converter (ADC) resolution stages, was calculated using the value of feedback resistors at the op-amp, written below as Equation 3.3. The equation represents the ideal case when resistors of the exact value are used and there are no additional losses in the feedback loop.

$$Vset = (\frac{2.4\ M\Omega}{800\ M\Omega})(\frac{1023}{5\ V})(Desired\ Voltage) \tag{3.3}$$

By taking the expected current through the 2.4 MΩ resistor across the op-amp the expected feedback voltage can be calculated for a given desired voltage at the photocathode. This result is converted into the microcontroller ADC resolution, since the PIC12F1572 has a 10-bit ADC there are 1023 voltage states between ground and the five volt potential. The resulting Vset can be used directly as the regulating target in code to achieve a similar voltage. Due to losses along the Cockcroft-Walton multiplier and electrical contact between components, the photocathode voltage will not be ideal and will require a higher set point to reach a given target voltage.

The feedback voltage interpreted by the ADC is processed by the microcontroller to determine the current photocathode voltage. A proportional-integral-derivative (PID) controller was implemented to modify the PWM duty cycle based on the feedback value. A PID controller enables the system to respond to the feedback by interpreting the voltage error, rate of change of error, and to integrate the error of the voltage across a domain. The three terms are set individually, by setting a combination of these gains controller behavior is tuned to regulate a specific system.

The previous research at Kansas State University had implemented a PIC12F1572 microcontroller to regulate the output voltage and used a PID controller that was able to reach the range of -700 V[2]. The system plant was the sixteen stage half-wave Cockcroft-Walton voltage multiplier with a distinct low-pass filter at each stage. The analytical method to solve this system was complicated by the rectifying diodes at each stage contributing voltage losses. During prototyping the analytical path was determined to be unnecessary since experimental models of the final system had been constructed and could be observed. A series of empirical studies were undertaken to determine the most usable range for the voltage regulation.

A breadboard circuit was constructed using discrete components of the same values and when possible the same packages as used in the additive construction. The circuit diagram for the PID tuning circuit has been included as Figure 3.29, the breadboard layout is shown in Figure 3.30.

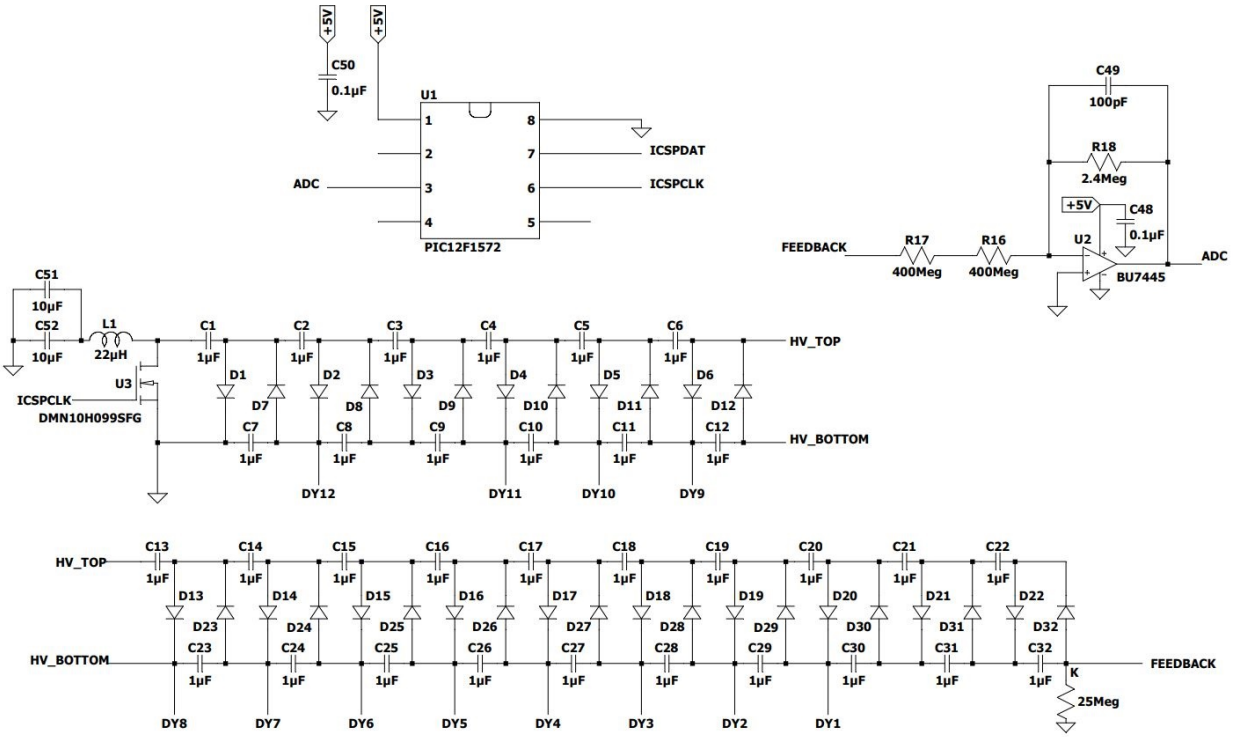


Figure 3.29: *The circuit utilizes the same components but, does not include the low-pass filter at each stage of the Cockcroft-Walton multiplier.*

During testing the PWM output by the PIC12F1572 was monitored to observe changes

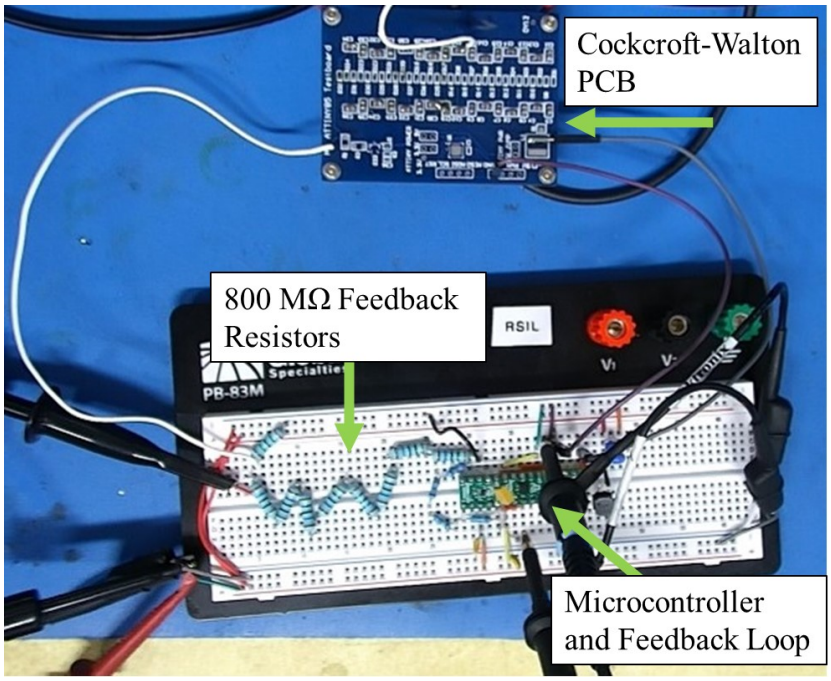


Figure 3.30: *The breadboard equivalent circuit was used to tune the PID controller. A separate printed circuit board (PCB) was used to house the half-wave Cockcroft-Walton circuit, which omitted the low-pass filter at each stage.*

in the duty cycle, additionally the feedback voltage received by the microcontroller was observed. The voltage of the final stage, the photocathode (K) was monitored to determine how each PID configuration regulated to the set value, and to determine the peak-to-peak voltage of the mean value. The system was powered using +5 Vdc with a current limit of 40 mA. The current limiter was used to reduce the damage to components if feedback was lost and the system was unable to determine the voltage at the photocathode. If the controller reads the voltage at the photocathode to be too low it will increase current through the MOSFET drain based on the duty cycle. If the current is drawn too often from the inductor through the MOSFET, it will be exposed to high-voltage at the output of the inductor which will exceed the breakdown voltage of the MOSFET if not properly moderated. The current limit of 40 mA was identified during testing of early prototypes, at startup the controller must charge the Cockcroft-Walton from the ground state, storing energy in the capacitors at each of the sixteen stages including the filtering capacitors. In order to charge the multiplier, the system during the first three to five seconds will spike in current consumption to near 40

mA. Afterwards the system will reduce in consumption to a steady state of approximately 20 mA. If current is observed to reach a value greater than 40 mA, then the system is in an open loop condition in which a component in the feedback loop had failed. The most susceptible component to failure in the feedback loop was the op-amp. The op-amp was observed in multiple cases to become inoperable and would result in the feedback line being pulled low.

Early in testing it was observed that the breadboard circuit would experience large oscillations with a Kp = 100, Ki = 1, and Kd = 20 PID configuration. The period of oscillation appeared consistent, as if the controller or code encountered an error routinely. A general purpose input-output (GPIO) pin was configured as an output and monitored with an oscilloscope to determine if some function of the code or circuit might cause the controller to reset and restart operation. After multiple tests it was determined that the cause was not physical and the microcontroller was not observed to reset during testing. Further investigation of the code resulted in the cause to be limited to the PID controller code. The integral term of the microcontroller was left unbounded and could increase repeatedly if conditions remained unchanged from the feedback loop. The integral term was assigned as a signed integer with a maximum value of 32,767, once this value was reached the variable would roll over, resulting in a new value of 0. The periodic behavior of this rollover caused the system to oscillate in a semi-predictable pattern which created large variation in the final voltage at the photocathode. The periodic roll over was removed with the addition of an anti-windup term to monitor the integral. If the integral reached a set value, the code would reset the value to match the maximum rather than allowing it to further increase. By bounding the integral term, the controller ceased to have the previously observed periodic large oscillations.

Before modifying the regulating values of the PID controller, the performance of the system was improved by changing the interval of measurement of the regulating feedback. The system clock (FOSC) for the microcontroller is passed to the ADC module using a fractional multiplier to set the oscillation frequency of the ADC clock. The number of cycles within the ADC determines the rate that measurements that can be read from the ADC output register. ADC conversion time was calculated from the datasheet of the PIC12F1572

microcontroller and is included as Equation 3.4[35].

$$Conversion\ Time = \frac{System\ Clock}{ADC\ Clock\ Divider} * (11.5\ cycles) \tag{3.4}$$

Initially, the system used a divider of 64, outputting 13.89 waves per conversion with the PWM produced at a frequency of 151 kHz. If the voltage changed between fully computed values from the ADC, the resulting correction may not be the expected response to the current state of the photocathode. It was hypothesized that if an ADC value could be calculated each time the controller changed the duty cycle, the system would better regulate the voltage of the final stage, the photocathode (K). Multiple oscillator divider values are available ranging from FOSC/2 to FOSC/64. The recommended range from the manufacturer was limited to FOSC/8 to FOSC/32, within the recommended range the regulating performance of three configurations are listed in Table 3.4. Contrary to expectation, the system performed better not at the fastest ADC conversion speed but, at an intermediary value of FOSC/16 allowing 3.47 waves to be output for each measurement read from the ADC.

Table 3.4: *Evaluating the performance of the ADC using different clock dividers for a system at 8 MHz, FOSC = 8 MHz. The PID controller gains where Kp = 100, Ki = 1, and Kd = 20 with an integral limit of 100 and voltage target of -715 V.*

ADC Clock	Conversion Time	Waves per ADC conversion	K Vpk-pk (V)
FOSC/64	92 μs	13.89	16 to 26
FOSC/16	23 μs	3.47	16 to 22
FOSC/8	11.5 μs	1.74	22 to 34

It was determined that increasing the speed of each ADC conversion improved the response of the PID controller without directly changing controller gains. The microcontroller was adjusted to use the FOSC/16 timer source, responding approximately four times faster to reduce regulation noise.

A new controller configuration was expected to provide improved response to regulation errors. The testing configuration from Figure 3.30 was used to iterate through different controller settings to determine a new controller configuration. The testing was limited to

five controlling terms, the three PID gains, the voltage set point, and the bounds which prevent the integral term from causing overflow. The terms were considered interdependent in the minimization of photocathode (K) peak-to-peak voltage, the regulating noise. A subset of the testing is included as Table 3.5, the last row achieved the lowest regulating noise.

Table 3.5: *Subset of empirical data used to establish a PID controller configuration to improve voltage regulation. Vset corresponds to the voltage set point used by the microcontroller, the target regulating value.*

Vset	Kp	Ki	Kd	Integral Bounds	K Voltage (V)	Vpk-pk (V)
590	30	0	0	300	-885	20 to 34
590	30	0	5	300	-881	20 to 30
590	30	3	0	300	-928	22 to 38
585	26	2	18	300	-898	14 to 26
592	26	2	16	180	-895	16 to 24
594	26	1	12	180	-887	18 to 30
604	25	1	17	180	-902	18 to 30
590	26	2	16	200	-893	14 to 22
590	26	2	16	215	-890	12 to 16

The controller with sufficiently low regulating noise, the last row of Table 3.5, was implemented on the second functioning prototype. Two high-voltage control configurations were tested on fully constructed additive circuits, listed in Table 3.6.

Table 3.6: *The control parameters of the two prototypes which achieved continued operation.*

Model	Vset	Kp	Ki	Kd	Integral Bounds	Photocathode Voltage (V)
Prototype 1	439	100	1	20	200	-715
Prototype 2	590	26	2	16	215	-890

The controllers for the two prototypes in Table 3.6 were programmed to achieve different voltages as required for full system testing. The PID controller tuned for the second prototype used a higher integral gain and lower proportional and derivative gains. The system for the second prototype was expected to be slower than the first system but, achieve a more stable steady state value. Testing of the prototypes under intensive loading is included in Section 4.2. The code adapted from the previous work is included as Appendix B[2].

3.2.2 Feedback Test

The design which enables measurement of circuit functionality at an intermediate stage was developed in Section 3.1.1 and is explained in this section. The circuit was sectioned between the low-voltage charge pump, and the high-voltage Cockcroft-Walton multiplier. The control loop was tested routinely to ensure expected operation before completely assembling HVPS prototypes.

The goal for separating the circuit was to develop a testing procedure which could be used to evaluate the performance for multiple iterations of the additive circuit. The high-voltage control testing circuit is shown in Figure 3.31. A high-voltage source was not available for testing, to develop a testing system for the feedback loop the external feedback resistor values were reduced to operate for a -5 V potential. A bench-top power supply supported up to 30 V sourcing at 1 A was used to provide an adjustable voltage source. The feedback current that would enter the op-amp feedback resistor was expected to be 875 nA for a desired voltage of -700 V. Using Equation 3.2 in order to produce the desired current of 875 nA associated with the feedback from -700 V, a 5.95 MΩ resistor should be used for an input of -5 V. The testing set up was constructed as Figure 3.32.

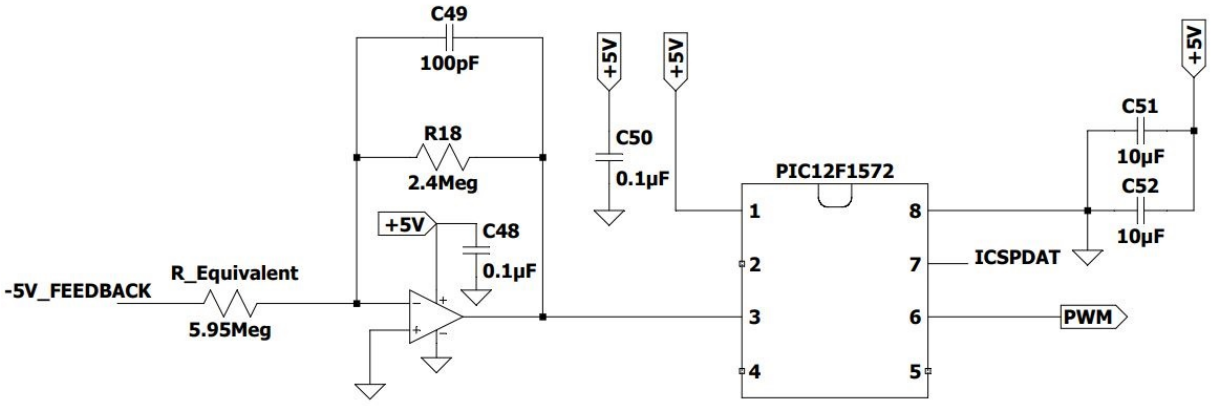


Figure 3.31: *The circuit is fed a simulated feedback voltage and the PWM output is observed to determine performance.*

The 5 V output of the bench-top power supply was connected to earth ground and power was drawn from the ground output of the generator channel. Drawing from the ground output enabled the power supply to output a negative voltage which could be used

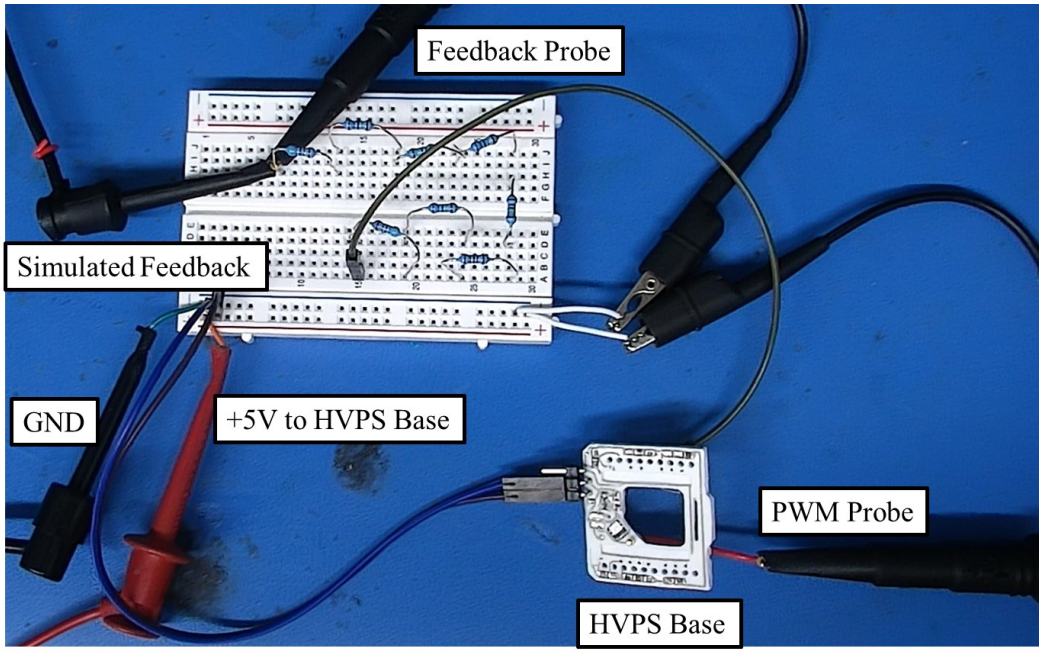


Figure 3.32: *During testing both the PWM and input to the feedback loop are monitored to observe any changes while the feedback voltage is raised and lowered.*

to simulate the feedback to the PID loop of the charge pump circuit. In this configuration -5 V is seen by the circuit being analogous to -700 V in the fully constructed circuit. The feedback voltage was limited to provide up to 1 mA, the lowest current setting available. Supplying a low current assisted in determining if the feedback loop was discharging prior to being read by the microcontroller.

The supplied feedback voltage and resultant duty cycle were observed from the oscilloscope. It was expected that as the feedback voltage reaches the steady state regulating value, the PWM should approach a duty cycle of 0 %. Likewise, as the feedback voltage decreases below the steady state regulating voltage, the PWM will increase up to a maximum duty cycle of 50 %. If this behavior was not observed, the feedback loop was considered compromised. Units which failed the op-amp feedback test were re-evaluated to determine the failure mode. If each component is connected, other possible causes are a damaged op-amp, or discharge within the feedback loop. The feedback loop was susceptible to discharge due to the low volume of current available to the input of the PIC12F1572 ADC. To improve the functionality of the feedback loop the area on and around the components was cleaned

repeatedly before and after testing and probing. Constructions which passed the feedback testing were coated in non-conductive epoxy to prevent damage to the traces or components.

Chapter 4

Results

Results relating to the hybrid process may be found in Section 4.1. Results relating to the physical characteristics and electrical performance of the high-voltage power supplies constructed may be found in Section 4.2.

4.1 Hybrid Process Parameters

Results obtained during experimentation varying process parameters. The two areas which were observed to have the most variability are addressed.

4.1.1 Trace Routing on Printed Parts

A combination of techniques were implemented in the hybrid process to facilitate the deposition of trace material. It was determined that printing the dielectric surface with a 125 μm ID/ 175 μm OD ceramic tip required surface milling of 0.2 mm. During the trace deposition process, minimizing the nozzle separation from the part surface was performed using the surface scan conducted prior to deposition. Combining the respective advantages of FDM, the mill, laser height scanning, and the material pump, functional traces could be printed on the additive build.

The obstructive surface roughness was removed through milling 0.2 mm from the build

face. A visual comparison of traces deposited throughout the hybrid process development is shown in Figure 4.1. Control over the trace deposition improved significantly by milling the build face before applying traces. Traces deposited on milled surfaces were observed to be more uniform and could be printed narrower than traces deposited on the unmilled surface.

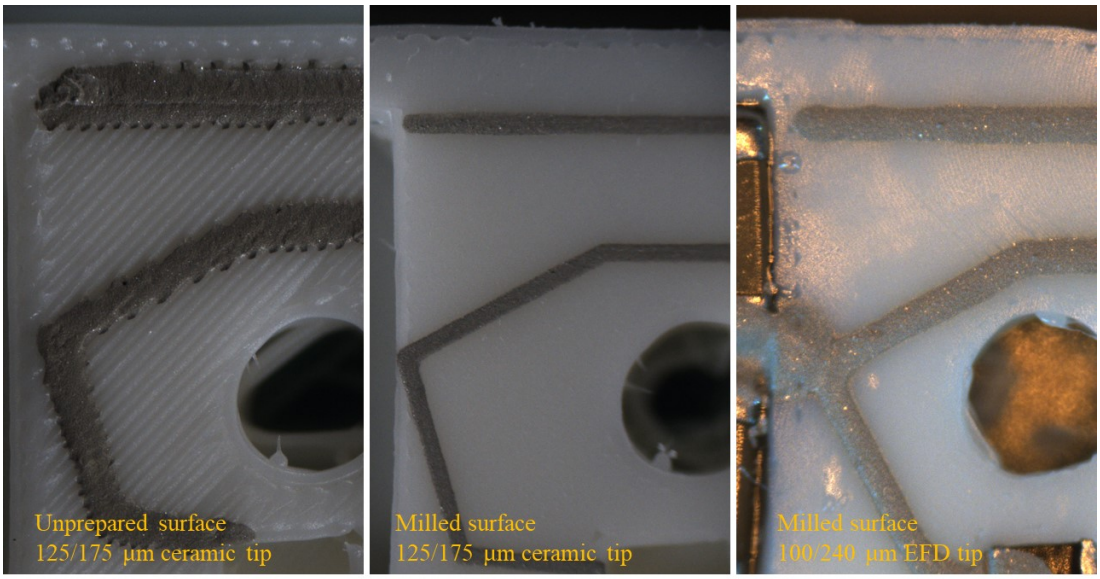


Figure 4.1: *Throughout process development traces were deposited on unprepared surfaces, milled surfaces, and using both ceramic tips and EFD needles.*

In Figure 4.1, the jagged edges observed on traces for surfaces that were not milled were visibly eliminated by milling prior to trace deposition. The ceramic nozzle used was 125 μm ID / 175 μm OD which contributes to the thinner traces compared to the traces deposited using the 100 μm ID / 240 μm OD EFD. When the EFD is pressed close to or on the surface the material from the smaller inner diameter was observed to spread to a similar width as the outer diameter of the tip. Narrower traces may be achieved using the ceramic tips due to the smaller diameter of tips available. Smaller diameter EFD needles were not tested but, may be able to produce narrower traces if a similar size was used.

A wide pressure range was used for each extruder head, the ceramic tips required 10.5 - 24 psi, whereas the EFD needles required 25 - 65 psi. The larger pressure difference between the tips may be attributed to internal differences or materials between the tips used. Additionally, the wide pressure range observed for each pump extruder may be impacted by

the mixture of conductive material used. Over time as particles in the paste settled, the required pressure to extrude the paste may increase. Since neither viscosity nor particle distribution were monitored the range of pressure is attributed to general variation in the pump due to material properties, pump extruder materials, and potential differences internal to the pump.

For the deposition of traces for use with high-voltage the traces produced using the smaller 125 μm ID / 175 μm OD nozzles and the 100 μm ID / 240 μm OD needles were acceptable. A key difference was that the EFD tips were able to flex when printing close to parts whereas, the ceramic tips would fracture. In both cases depositing the material benefited from positioning the nozzle tip close to the print surface within 0.1 mm or less separation. Reducing the distance to the tip from the surface improved control over trace uniformity but, resulted in shorter traces which may have higher resistance. When routing traces to the parts that have been inserted into the assembly, parts pads similar in size to 0805 capacitors could be successfully connected, shown below in Figure 4.2.

The smaller 0402 parts in Figure 4.2 have 0.125 mm^2 pads which were not connected accurately in most trials. Parts which are not connected as part of the on-bed processing were reworked to achieve operation. Rework was conducted using an EFD needle coated in CB028 which was manually used to connect pads or traces which were not connected during the hybrid process. In this study rework of conductive traces was required for each part produced. The use of both flat-ended EFD needles and ceramic nozzles can be used to route traces of width 0.25 mm. The use of laser scanning to determine the print height for traces enabled traces to be printed consistently on the build surface. However, on the print bed, determining the height of traces could not be performed using the laser height sensor for the settings attempted. Placing the parts prior to routing traces posed an obstacle for connecting the trace edges. Improvements to the deposition height through finer height meshing near sockets or through reducing the conductive paste viscosity may improve connection results.

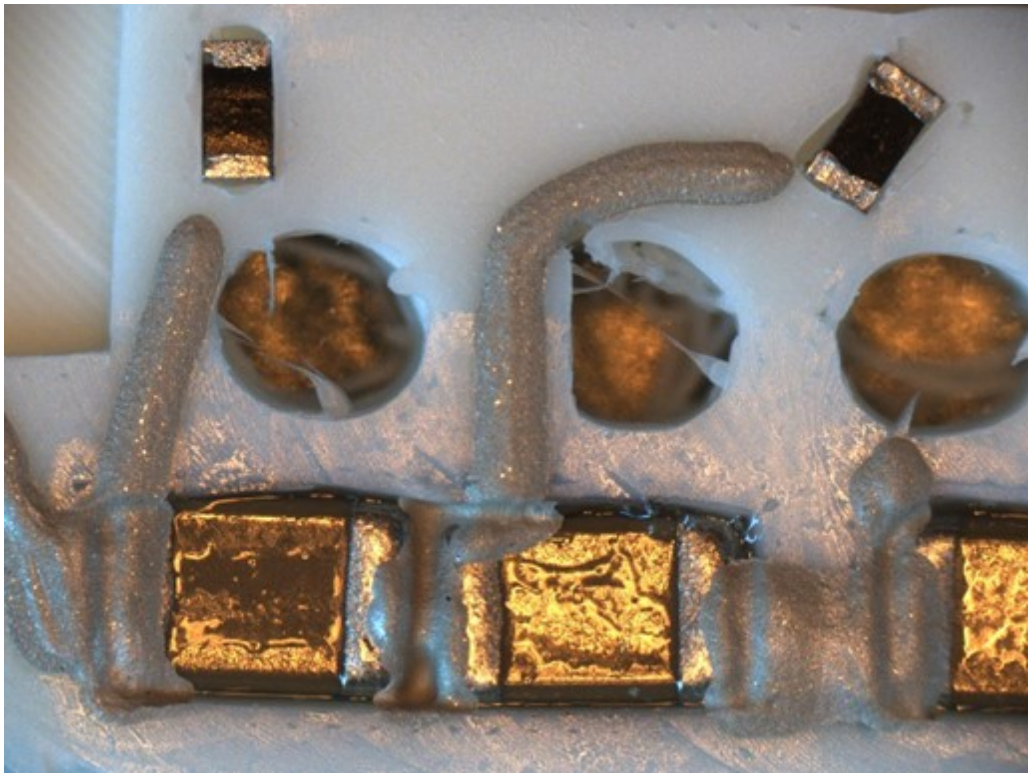


Figure 4.2: *0805 parts can be connected by the printer during trace deposition, in some cases a second extrusion routine may be required.*

4.1.2 Accuracy of Pick-and-Place for AM Slots

Success was defined as the ability for a part to be placed in the correct position, above or in the designated slot. A part which was placed above the designated slot but, could be pressed down with a vertical force was considered successful. This definition of success was adopted with the intent to continue the automation of the process. A vertical press could be integrated into the gantry as an attached plate and a series of g-code instructions. Dimensional modifications to component slots in the printed dielectric to accommodate automated placement are discussed.

For the 3Dn-300 model printer used and printing parameters outlined in Section 3.1.1, a slot for an 0805 capacitor along the external perimeter was modeled as 2.4 mm by 1.5 mm by 1.35 mm. The modeled slot tolerance represented an 8.6 % increase in the length (X-dim.), 7.1 % increase in the width (Y-dim.), and 8 % increase in the height (Z-dim.) from the maximum part tolerance. Slots with the additional tolerance could accommodate

the manual placement of capacitors after printing. After optimizing for the PNP, the final slot had dimensions of 2.4 mm by 1.6 mm by 1.35 mm. The finalized modeled slot tolerance represented an 8.6 % increase in the length (X-dim.), 14.3 % increase in the width (Y-dim.), and 8 % increase in the height (Z-dim.) from the maximum part tolerance. Due to slots for capacitors being nested with two to three capacitors per slot, the slot width was the narrowest dimension for placement.

Intergated circuits such as the microcontroller required additional tolerance to account for the rectangular packages. The ICs used had more defined right angle edges compared to the rounded terminals of the 0805 capacitors. However, the ICs generally had larger package sizes than the capacitors. The finalized modeled slot tolerance for the microcontroller represented a 3 % decrease in the length (X-dim.), 3 % increase in the width (Y-dim.), and no change in the height (Z-dim.) from the maximum part tolerance. While the decrease in slot length may impact placement success, it was performed to improve the alignment of trace connections to the microcontroller. In the parts tested the tolerance required for manual placement was sufficient to accommodate automated placement via PNP.

After circuit subsections were adjusted for population using the PNP, the integrated design was developed as outlined in Section 3.1.1. Results from an early batch of the integrated HVPS circuit were collected in Table 4.1. A total of 39 components are placed via PNP into each integrated assembly.

Table 4.1: *Average PNP placement accuracy for each circuit subsection, and average overall performance for an early series of three integrated HVPS bases.*

Placement Routine	Number of Components	Success
Average Performance (All sections)	39	56 %
CW Filter Capacitors (0805)	15	67 %
CW Filter Resistors (0402)	15	42 %
Charge Pump Components	9	59 %

From the early testing shown in Table 4.1, slot tolerances for the integrated design were modified following details outlined previously in sections 3.1.1 and 3.1.3. The new settings were tested throughout the production of 13 additional assemblies which were printed as

four separate batches. The finalized circuit subsection success rates and success rate for the full circuit have been tabulated as Table 4.2, below. The largest improvements to overall performance were in the 0402 resistor placement, and in the placement of the charge pump components which consisted of 0603 components and multiple integrated circuits. The largest improvement was for the placement of the 0402 resistors which had select slots enlarged by 8.2 % length (X-dim.), 17.9 % width (Y-dim.), and no change in height (Z-dim.) from the previous part tolerance. Tolerances for each section of the model may vary depending on the surrounding features. Some tolerances could not be increased further without compromising the necessary printed perimeters for surrounding features. Additionally, the angle at which components were picked was aligned with the placement angle to reduce uncertainty for rotation of the pick-and-place, this was most important for the angled resistors in the integrated design, Figure 3.11.

Table 4.2: *Average PNP placement accuracy for each circuit subsection, and overall performance for the later series of HVPS bases.*

Placement Routine	Number of Components	Success
Average Performance (All sections)	39	68 %
CW Filter Capacitors (0805)	15	70 %
CW Filter Resistors (0402)	15	55 %
Charge Pump Components	9	76 %

From the success rates shown in Table 4.2 for each circuit section, the placement of the charge pump components had the highest success rate of 76 %, meanwhile the lowest success rate was the placement of the 0402 filter resistors of 55 %. Components populated via the pick-and-place which were unsuccessful were replaced manually and each assembly produced required some level of placement correction during production. The larger component sizes of the charge pump circuit and the filtering capacitors had similar component sizing having at least 2.2 times the surface area used for picking compared to the 0402 resistors. Enlarging slot dimensions for select resistor slots and accounting for the inherent variability of the pick-and-place process, the average placement success rate was increased from 56 % to 68 % for the integrated HVPS design. The use of a shorter EFD needle for the PNP to reduce

needle curvature and continued study of slot tolerances for the specific model geometry may improve overall placement success. The results covered in Table 4.2 aligns with the choice of the PNP needle sizing, prioritizing the placement of the larger build components.

4.1.3 Process Timing

The approximate time required to conduct the hybrid process was monitored and shown below as Table 4.3. For the construction of the high-voltage power supply the printing of the dielectric through FDM required the most time. The placement of components via PNP required the second most time when compared to other per-build processes. Cooling the print bed prior to milling and curing the parts by heating the print bed after traces were deposited were performed for a series of parts at once. A series of parts in this context is considered a batch, and has the cooling and curing performed as a group. If this process were conducted for builds differing in overall size or complexity from the HVPS described, the process times are expected to change. In a large scale environment a larger print bed could accommodate more printed assemblies, reducing overall time required for cooling and trace curing processes. Reducing total time required for per-build processes within a batch would require additional 3D printers to conduct processes simultaneously or optimization of processes described.

Table 4.3: *The time required by each process in the hybrid process flow, for construction of a single HVPS build. Per-batch processes conducted for all parts present on the print bed.*

Process	Lower HVPS Build	Upper HVPS Build
Fused Deposition Modeling	14 hours	2.5 hours
Cooling (Per-batch)	30 - 45 min.	
Surface Milling	10 min.	5 min.
Pick-and-Place	45 min.	-
Laser Scan	5 min.	2.5 min.
Trace Deposition	25 min.	10 min.
Trace Curing (Per-batch)	12 hours	
Per-Build Process Time	15.5 hours	2.75 hours

4.2 Prototype Characteristics

Circuits constructed through the hybrid process were evaluated for the physical size of the construction and the characteristics of the high-voltage output. In some cases the prototypes are compared to the E11807-01 tapered divider which is the closest analog for size comparison to the constructed circuit that is publicly available. The E11807-01 is not a high-voltage supply but rather a passive resistive divider board used to reduce an input high-voltage.

4.2.1 Physical Size

The bulk dimensions for the prototypes were measured, excluding header pins and connectors. The prototypes are compared against the Hamamatsu E11807-01 tapered divider, omitting the Bayonet Neill-Concelman (BNC) connectors. The data is included in Table 4.4.

Table 4.4: *Bulk dimensions and weight of each high-voltage power supply. Note the E11807-01 is a tapered voltage divider and requires external high-voltage to supply power to the PMT.*

PMT HVPS	Length [cm]	Width [cm]	Height [cm]	Volume [cm^3]	Weight [g]
E11807-01	2.610	2.615	1.498	10.22	11.84
Prototype 1	3.021	2.783	0.895	7.52	6.90
Prototype 2	2.994	2.771	0.865	7.18	8.36

From the dimensions in Table 4.4 each prototype required at least 26% less volume compared to the E11807-01. Prototype 1 had a volume reduction of 40.3% and was 41.7% lighter than the E11807-01. Prototype 2 had a volume reduction of 42.3% and was 29.4% lighter than the E11807-01. Prototype 2 and the E11807-01 are included in Figure 4.3 connected to the R11265U PMT. The difference in weight between Prototype 1 and 2 is due to Prototype 1 being only partially filled with non-conductive epoxy. If Prototype 2 was only partially filled it would have a similar weight to Prototype 1. No electrical differences were attributed to the difference in potting. Prototype 1 and 2 operate from +5 V bias whereas the E11807-01 requires a high-voltage input, which eliminates the need for an external HV source.

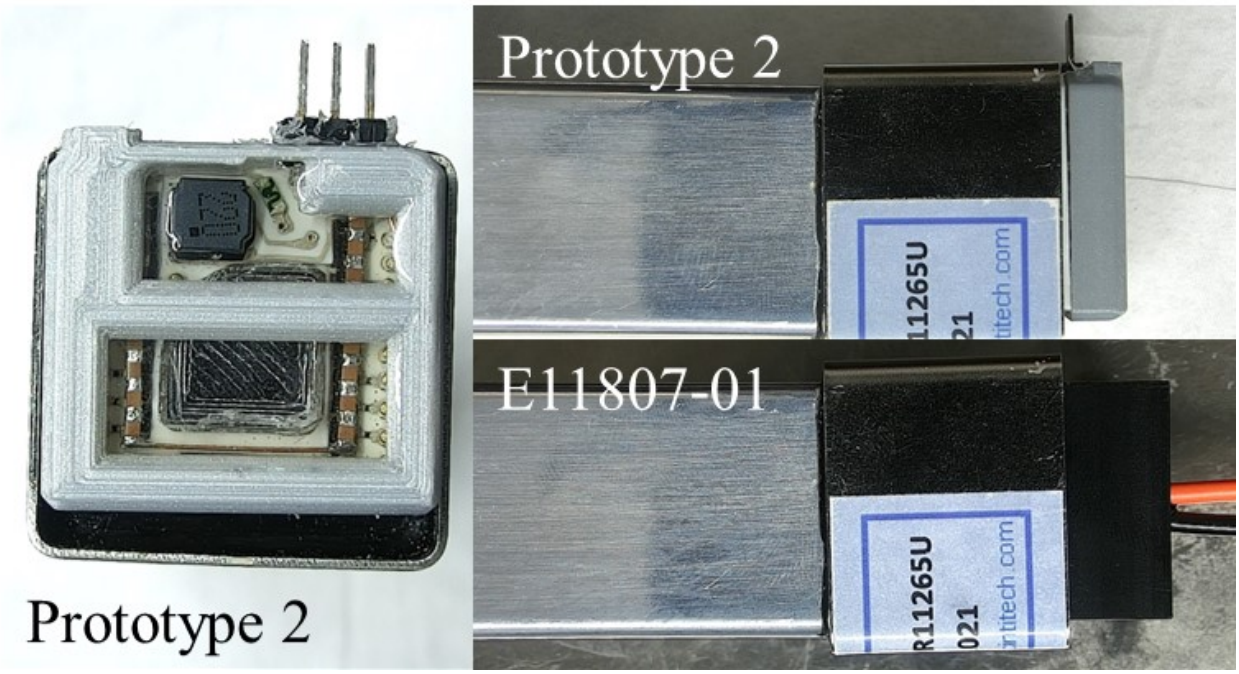


Figure 4.3: *Prototype 2 with the largest volume reduction connected to the R11265U compared to the E11807-01.*

4.2.2 Dynode Voltages

The dynode stages were measured for each prototype and compared to the expected voltages calculated for the E11807-01 tapered divider, included below as Figure 4.4. The prototypes were measured under intensive loading, defined as 25 MΩ to ground at the photocathode stage.

The target voltage for Prototype 1 was -715 V compared to the -890 V target of Prototype 2 and E11807-01. The target voltages were obtained during testing of the PID controller on the breadboard test circuit, discussed in Section 3.2. The prototypes were developed at different times during testing with the R11265U PMT and changes in target voltage were made to improve sensor performance. The voltage trend of each prototype follows the distribution of the E11807-01. In both cases the PID control on the prototype was below the target voltage by 0.84% for Prototype 1 and by 1.01% for Prototype 2. Under intensive loading Prototype 1 reached -709 V +0.71% / -1.55%. Prototype 2 with an improved PID controller achieved -881 V ± 0.68%.

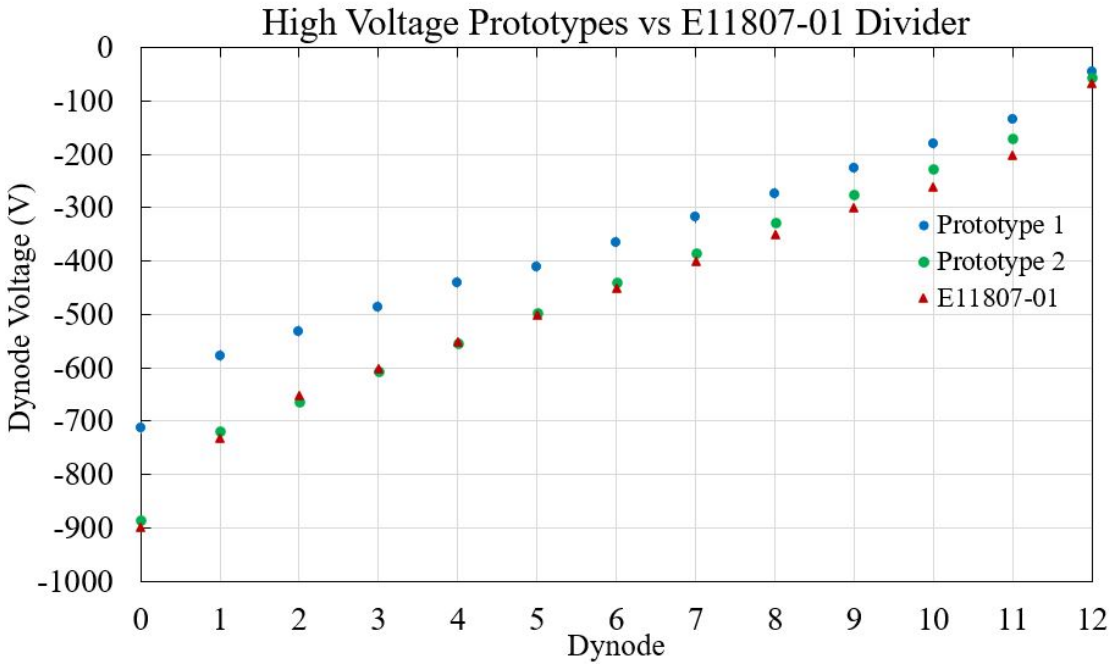


Figure 4.4: *The voltage observed at each dynode stage for the prototypes and the expected voltages from the Hamamatsu E11807-01 tapered divider. The photocathode is labeled as dynode 0.*

4.2.3 Voltage Stability

Applications such as mobile detection may require long measurement intervals spanning hours to days. For long precision measurements, instability from the supplied bias may create additional error. A test of voltage stability was measured using the intensive loading condition as a uniform load of 25 MΩ to ground at the photocathode stage. Data was collected every thirty seconds from a probe clipped to the load resistor. The data for both prototypes have been plotted below, as Figure 4.5, changes in voltage have been normalized about the mean voltage for each supply.

No trends were observed in either Prototype 1 or 2 over the hour long measurement. Prototype 1 was observed to have larger magnitude corrections to maintain the target voltage. At times Prototype 1 deviated by up to -1.137% from the mean. Prototype 2 maintained a voltage of -884 V during a majority of the measurement intervals, shown as a +0.036% change in Figure 4.5.

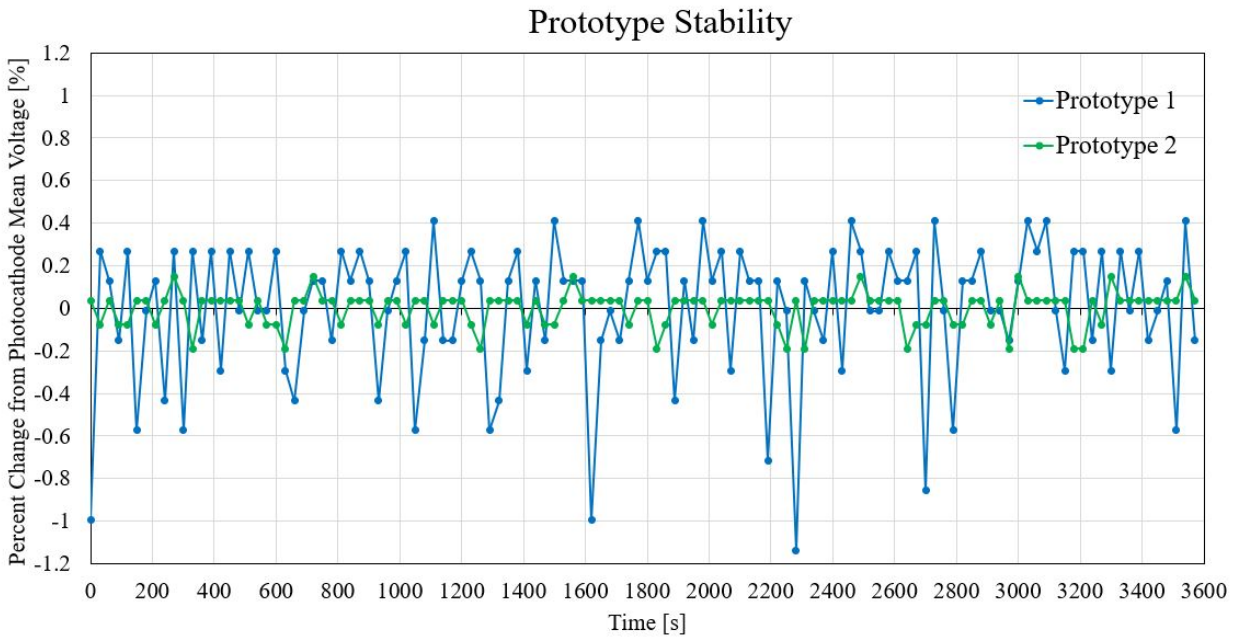


Figure 4.5: *The variation in voltage at the photocathode normalized about the mean voltage observed over the measurement interval.*

4.2.4 Power Consumption

The power consumption of the prototypes was performed by placing a 10 Ω resistor in series with the power inlet to the device. The load resistor from the photocathode to ground was varied from 500 MΩ to a maximum loading of 10 MΩ. The loading represents consistent signal pulses registering in the detector pulling a constant current from the power supply. The series of measurements have been plotted in Figure 4.6. It is expected that reducing the resistance of the high-voltage output at the photocathode, the power consumption should increase due to the smaller load drawing more current from the final multiplier stage.

The increase in power consumption appeared exponential as observed in Figure 4.6 for both prototypes. A sharp increase in power draw was observed as the load approached 10 MΩ. The power consumption observed at 10 MΩ is considered the maximum. Comparing the performance of the prototypes in Figure 4.6, Prototype 2 was observed to draw more current under maximum loading conditions. The difference in power consumption is assumed to be significantly impacted by the difference in photocathode voltage between the prototypes however, specific build characteristics may also impact overall power consumption.

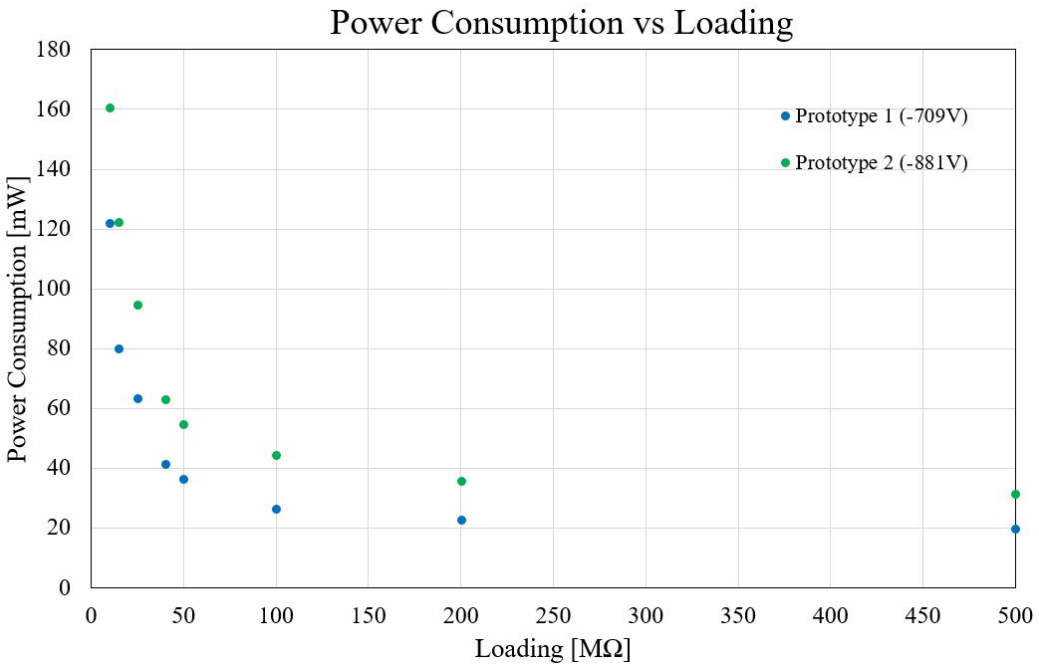


Figure 4.6: *The power consumed by each prototype with uniform loading of the photocathode.*

The expected power consumption at idle from the internal resistance of the E11807-01 was calculated from the total resistance between the photocathode and anode. For a bias of -700 V the E11807-01 was expected to consume 182 mW, while at a bias of -900 V power consumption would be 301 mW. At idle when each supply was disconnected from any loading, considered infinite resistance, Prototype 1 required 16.58 mW and Prototype 2 required 26.9 mW. Both prototypes experienced a significant reduction in power consumption compared to the resistive divider board E11807-01. The difference in power consumption between the prototypes was highest with a 10 MΩ load for a difference of 38.79 mW. The lowest difference was 10.33 mW experienced at idle. At maximum loading, Prototype 2 required 160.72 mW compared to the 121.93 mW required by Prototype 1.

Chapter 5

Conclusion

A hybrid additive manufacturing process to construct high-voltage electronics was developed. The materials used such as printed ABS and CB028 conductive paste were suitable for construction of high-voltage electronics. Two functioning prototypes were constructed which had comparable performance to the E11807-01 tapered divider. Prototype 1 produced -709 V +0.71% / -1.55% with stability within less than 1.6%. Prototype 2 was able to produce -881 V $\pm$ 0.68% with stability within less than 0.4%. The voltage distribution of both HVPS were similar to the calculated distribution from the E11807-01.

The hybrid process developed involved the combination of five processes used in additive and traditional subtractive manufacturing. The dielectric was printed using fused deposition modeling. The ABS dielectric was printed with a 125 μm ID / 175 μm OD ceramic nozzle which was sufficient to construct slots for surface mount components. The build variability and slot spacing within the build required experimental validation for manual and automated part insertion. In general slots should be sized based on the maximum component dimensions and adjusted based on slot proximity to other features. A separation of at least three printed roads between slots and edges reduced dimensional interference to component slots. Surface roughness produced from fused deposition modeling was an obstacle to the direct write of conductive paste and was removed by face milling. The end mill was used to remove 0.2 mm from the part face and minimized obstructive surface geometry. The smoothed surface

improved control over trace width and height during deposition by enabling a lower print height compared to an unmilled surface. The next step was to prepare the build for part placement. Slots were primed with non-conductive epoxy prior to inserting parts via PNP. The non-conductive epoxy ensured that parts did not move following curing. Individual slots required experimental resizing to account for variation caused by movement during pick and place operations. In this work, components 0603 and larger had the highest rates of placement success. In order to partially automate the direct write process and improve the repeatability of traces, a laser height sensor was used to scan the build surface. The surface was homogenized by covering it with a flexible 80 gauge plastic. The material was thin such that the resultant scan could be used to set the print height for the direct write of conductive paste with minimal modification. Traces were deposited through the direct write of CB028 performed when the 100 μm ID / 240 μm OD extrusion tip was between 50 and 100 μm from the milled print surface. Component pads smaller than 0.125 mm^2 were not connected in most cases due to the lack of software tools available for alignment and variation within the preceding processes. The hybrid process developed in this work describes one way in which high-voltage electronics may be fabricated but, requires build specific modification for operations such as part placement and sizing. The general guidance of separating discrete part locations depending on printer operating parameters and part sizing, and reducing the surface roughness prior to depositing conductive material can be applied to circuits constructed in a similar manner. Further work toward improving the manufacturing repeatability of the hybrid process described should be conducted.

Future work may include improving: pick-and-place placement accuracy; trace connection for components with small pads; and increasing overall repeatability of the hybrid process through automation. If a method to track components used in the construction could be implemented, determining the specific location of connections would become more consistent. The construction of circuitry through additive manufacturing still experience multiple sources of variation that are not well characterized. The methods described herein represent a series of ways in which potential obstacles to the construction of additive circuits may be addressed through the integration of processes.

Bibliography

[1] Hamamatsu. Photomultiplier tubes and photomultiplier tube assemblies R11265U series / H11934 series, 2019.

[2] Miranda Dodson. *Design of a photomultiplier tube high-voltage power supply base for integration into three-dimensional additive manufacturing.* Thesis, Kansas State University, 2021.

[3] A. Brunner, R.R. Crittenden, A.R. Dzierba, J. Gunter, R.W. Gardner, C. Hamm, R. Lindenbusch, D.R. Rust, E. Scott, P.T. Smith, C. Steffen, T. Sulanke, and S. Teige. A cockcroft-walton base for the feu84-3 photomultiplier tube. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 414(2-3):466–476, 1998. ISSN 0168-9002. doi: 10.1016/S0168-9002(98)00651-2.

[4] V. M. Ainutdinov, N. N. Vonsovskii, K. G. Kompaniets, A. I. Kozyr', and Yu. V. Mikhailov. An efficient high-voltage power supply for a photomultiplier tube. *Instruments and Experimental Techniques*, 46:376–379, 2003. ISSN 1608-3180. doi: 10.1023/A:1024474607600.

[5] D.F. Spencer, R. Aryaeinejad, and E.L. Reber. Using the cockroft-walton voltage multiplier with small photomultipliers. *IEEE Transactions on Nuclear Science*, 49(3):1152–1155, 2002. doi: 10.1109/TNS.2002.1039629.

[6] David Espalin, Danny W. Muse, Eric MacDonald, and Ryan B. Wicker. 3d printing multifunctionality: structures with electronics. *International Journal of Advanced Manufacturing Technology*, 72:963–978, 2014. doi: 10.1007/s00170-014-5717-7.

[7] Amit Joe Lopes, Eric MacDonald, and Ryan B. Wicker. Integrating stereolithography and direct print technologies for 3d structural electronics fabrication. *Rapid Prototyping Journal*, 18(2):129–143, 2012. ISSN 1355-2546. doi: 10.1108/13552541211212113.

[8] Goran Stojanovìc, Vesna Mandìc, Milan Èurčìc, Dragana Vasiljevic, Milica Kisìc, and Nikola Radosavljevìc. Combining rapid prototyping techniques in mechanical engineering and electronics for realization of a variable capacitor. *Rapid Prototyping Journal*, 20(2):115–120, 2014. doi: 10.1108/RPJ-07-2012-0061.

[9] Andrea Bellacicca, Tommaso Santaniello, and Paolo Milani. Embedding electronics in 3d printed structures by combining fused filament fabrication and supersonic cluster beam deposition. *Additive Manufacturing*, 24:60–66, 2018. ISSN 2214-8604. doi: 10.1016/j.addma.2018.09.010.

[10] Nathan Lazarus, Joshua B. Tyler, Jorge A. Cardenas, Brendan Hanrahan, Harvey Tsang, and Sarah S. Bedair. Direct electroless plating of conductive thermoplastics for selective metallization of 3d printed parts. *Additive Manufacturing*, 55, 2022. ISSN 2214-8604. doi: 10.1016/j.addma.2022.102793.

[11] Patrick F. Flowers, Christopher Reyes, Shengrong Ye, Myung Jun Kim, and Benjamin J. Wiley. 3d printing electronics components and circuits with conductive thermoplastic filament. *Additive Manufacturing*, 18:156–163, 2017. ISSN 2214-8604. doi: 10.1016/j.addma.2017.10.002.

[12] Simone Luigi Marasso, Matteo Cocuzza, Valentina Bertana, Francesco Perrucci, Alessio Tommasi, Sergio Ferrero, Luciano Scaltrito, and Candido Fabrizio Pirri. Pla conductive filament for 3d printed smart sensing applications. *Rapid Prototyping Journal*, 24(4):739–743, 2018. ISSN 1355-2546. doi: 10.1108/RPJ-09-2016-0150.

[13] DOE Handbook Electrical Safety, 2013. URL https://www.standards.doe.gov/standards-documents/1000/1092-BHdbk-2013.

[14] Mercedes Pèrez, Gustavo Medina-Sànchez, Alberto Garcìa-Collado, Munish Gupta, and Diego Carou. Surface quality enhancement of fused deposition modeling (fdm) printed samples based on the selection of critical printing parameters. *Materials*, 11, 2018. doi: 10.3390/ma11081382.

[15] Trieu Khoa Nguyen and Bong-Kee Lee. Post-processing of fdm parts to improve surface and thermal properties. *Rapid Prototyping Journal*, 24(7):1091 – 1100, 2018. doi: 10.1108/RPJ-12-2016-0207. URL https://www.scopus.com/inward/record.uri?eid=2-s2.0-85054805242&doi=10.1108%2fRPJ-12-2016-0207&partnerID=40&md5=278a95eada4acb0fb5034773eee84592.

[16] nScrypt. 3Dn Series, 2021.

[17] nScrypt. Specification sheet: Smartpump, 2016. URL http://www.nscrypt.com.

[18] Clayton Neff, Matthew Trapuzzano, and Nathan B. Crane. Impact of vapor polishing on surface quality and mechanical properties of extruded abs. *Rapid Prototyping Journal*, 24(2):501–508, 2018. ISSN 1355-2546. doi: 10.1108/RPJ-03-2017-0039.

[19] Saint-Gobain Crystals. CsI(Tl), CsI(Na) Cesium Iodide Scintillation Material, 2018.

[20] Tomáš Tichý, Ondřej Šefl, Petr Veselý, and Tomáš Cápal. Application possibilities of fused filament fabrication technology for high-voltage and medium-voltage insulation systems. In *2019 42nd International Spring Seminar on Electronics Technology (ISSE)*, pages 1–6, 2019. doi: 10.1109/ISSE.2019.8810300.

[21] P Veselý, T Tichý, O Šefl, and E Horynová. Evaluation of dielectric properties of 3d printed objects based on printing resolution. *IOP Conference Series: Materials Science and Engineering*, 461(1):012091, dec 2018. doi: 10.1088/1757-899X/461/1/012091. URL https://dx.doi.org/10.1088/1757-899X/461/1/012091.

[22] Hafiz Ahmed, Ghulam Hussain, Sohail Gohar, Aaqib Ali, and Mohammed Alkahtani. Impact toughness of hybrid carbon fiber-pla/abs laminar composite produced through fused filament fabrication. *Polymers*, 13(18), 2021. doi: 10.3390/polym13183057.

[23] A.M. Oviedo, A.H. Puente, C. Bernal, and E. Pérez. Mechanical evaluation of polymeric filaments and their corresponding 3d printed samples. *Polymer Testing*, 88:106561, 2020. ISSN 0142-9418. doi: https://doi.org/10.1016/j.polymertesting.2020.106561. URL https://www.sciencedirect.com/science/article/pii/S0142941819321695.

[24] YAGEO. Data sheet thin film chip resistors rt series, 2022.

[25] Prusa Research. Prusaslicer, 2021. URL https://help.prusa3d.com/category/prusaslicer_204. Accessed: July 20 2021.

[26] Frank De Stasi. Working with Boost Converters, 2015.

[27] 3M. Epoxy Potting Compound/Adhesive DP270 Clear and Black Technical Data Sheet, 2019.

[28] Ali Nasr Esfahani, Saeed Shahabi, Greg Stone, and Behzad Kordi. Investigation of corona partial discharge characteristics under variable frequency and air pressure. page 31 – 34. Institute of Electrical and Electronics Engineers Inc., 2018. ISBN 978-153864178-1. doi: 10.1109/EIC.2018.8481047. URL https://www.scopus.com/inward/record.uri?eid=2-s2.0-85056261463&doi=10.1109%2fEIC.2018.8481047&partnerID=40&md5=971e8ea17f7c3476469913942dd58569.

[29] Pau Bas-Calopa, Jordi-Roger Riba, and Manuel Moreno-Eguilaz. Measurement of corona discharges under variable geometry, frequency and pressure environment. *Sensors*, 22(5), 2022. ISSN 14248220. doi: 10.3390/s22051856. URL https://www.scopus.com/inward/record.uri?eid=2-s2.0-85125188926&doi=10.3390%2fs22051856&partnerID=40&md5=ba3880505f87c093b6a93e11e95ef38a.

[30] Ezgi Kucukdeger, Yuxin Tong, Manjot Singh, Junru Zhang, Leon K. Harding, Alejandro Salado, Steven W. Ellingson, and Blake N. Johnson. Conformal 3d printing of non-planar antennas on wrinkled and folded kapton films using point cloud data. *Flexible and Printed Electronics*, 6(4), 2021. doi: 10.1088/2058-8585/ac28f1. URL https://iopscience.iop.org/article/10.1088/2058-8585/ac28f1.

[31] Nils Bausch, David P. Dawkins, and Regina Frei. Inspired - advances in conformal printing: 3d printing onto unknown uneven surfaces, 2017.

[32] Keyence. LK-H082 data sheet, 2021.

[33] DuPont. Cb028 safety data sheet, 2018.

[34] Clayton Neff, Edwin Elston, Matthew Burfeindt, Nathan Crane, and Amanda Schrand. A fundamental study of printed ink resiliency for harsh mechanical and thermal environmental applications, 2018.

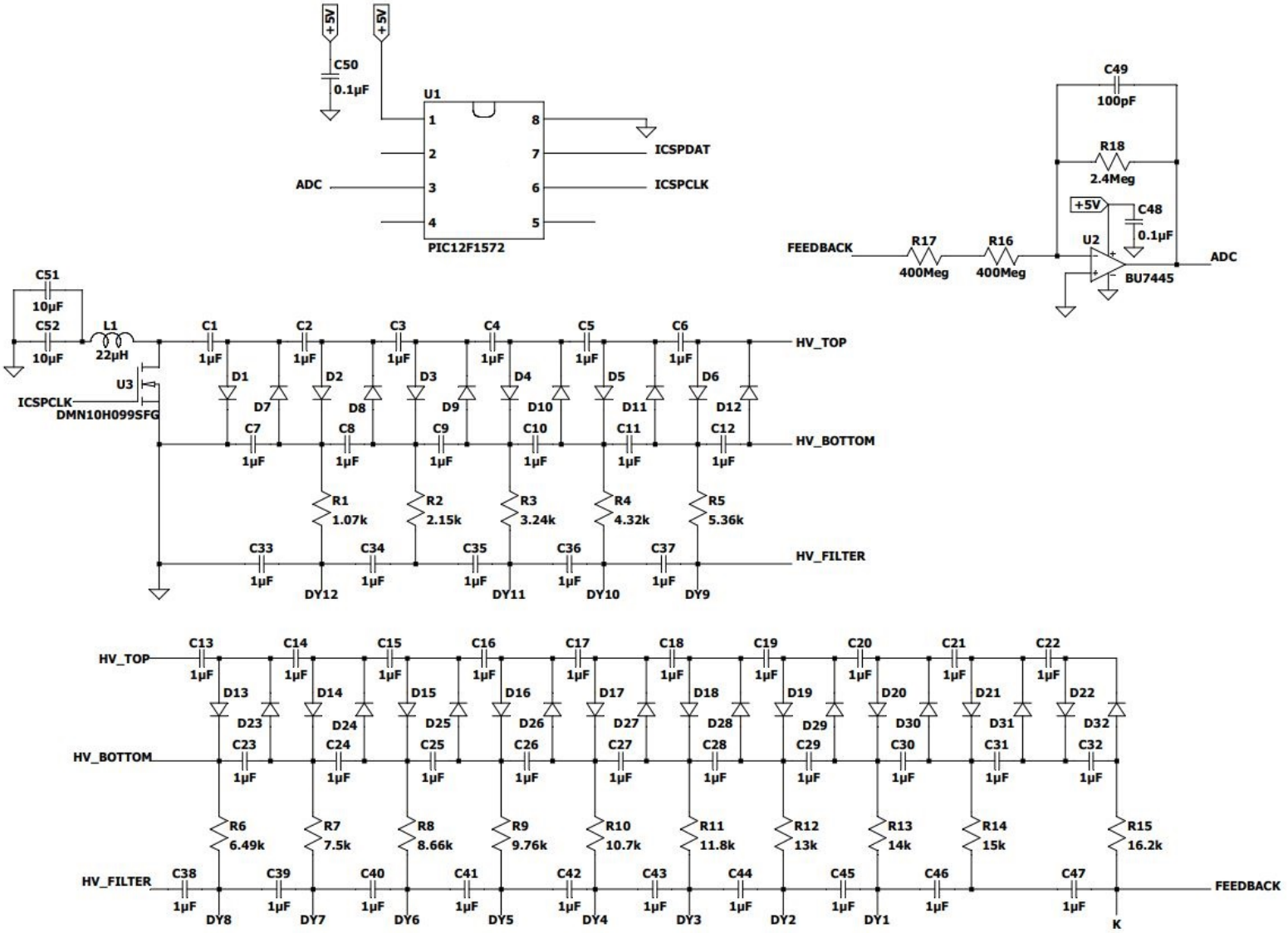
[35] Microchip Technology Inc. PIC12(L)1571/2 Data Sheet, 2015.

Appendix A

Reference Materials: High-Voltage Circuit

Appendix A contains a full reference schematic and bill of materials adapted from previous work[2].

A.1 Full Circuit Schematic and Bill of Materials



Name	Description	Designator	Quantity	Manufacturer	Part Number
100pF	CAP CER 100PF 50V NP0 0603	C49	1	TDK Corporation	C1608NP01H101J080AA
0.10μF	CAP CER 0.1UF 100V X7R 0603	C48, C50	2	KEMET	C0603C104J5RAC7867
1.0μF	CAP CER 1UF 100V X7S 0805	C1 - C47	47	TDK Corporation	C2012X7S2A105M125AE
10μF	CAP CER 10UF 6.3V JB 0603	C51, C52	2	TDK Corporation	C1608JB0J106K080AB
Diode	100V 200mA (DC) Surface Mount SOD-523	D1 - D32	32	Onsemi	1SS400T1G
Inductor 22μH	FIXED IND 22UH 1.8A 89 MOHM SMD	L1	1	Wurth Electronics	74404064220
PIC12F1572	PIC12F Microcontroller IC 8-bit 32MHz 3.5KB (2K x 14) FLASH 8-DFN (3x3)	U1	1	Microchip	PIC12F1572-I/MF
Op - Amp BU7445HFV-TR	IC OPAMP GP 1 CIRCUIT HVSOF5	U2	1	Rohm	BU7445HFV-TR
N-FET DMN10H099SFG	MOSFET N-CH 100V 4.2A POWERDI3333-8	U3	1	Diodes Incorporated	DMN10H099SFG
1.07k	RES SMD 1.07K OHM 0.1% 1/16W 0402	R1	1	Panasonic	ERA-2AEB1071X
2.15k	RES SMD 2.15K OHM 1% 1/16W 0402	R2	1	YAGEO	RC0402FR-072K15L
3.24k	RES SMD 3.24K OHM 0.1% 1/16W 0402	R3	1	YAGEO	RT0402BRD073K24L

Name	Description	Designator	Quantity	Manufacturer	Part Number
4.32k	RES SMD 4.32K OHM 1% 1/16W 0402	R4	1	YAGEO	RC0402FR-074K32L
5.36k	RES SMD 5.36K OHM 1% 1/16W 0402	R5	1	YAGEO	RC0402FR-075K36L
6.49k	RES SMD 6.49K OHM 1% 1/16W 0402	R6	1	YAGEO	RC0402FR-076K49L
7.5k	RES SMD 7.5K OHM 5% 1/16W 0402	R7	1	YAGEO	RC0402FR-077K5L
8.66k	RES SMD 8.66K OHM 1% 1/16W 0402	R8	1	YAGEO	RC0402FR-078K66L
9.76k	RES SMD 9.76K OHM 1% 1/16W 0402	R9	1	YAGEO	RC0402FR-079K76L
10.7k	RES SMD 10.7K OHM 0.1% 1/16W 0402	R10	1	YAGEO	RT0402BRD0710K7L
11.8k	RES SMD 11.8K OHM 1% 1/16W 0402	R11	1	YAGEO	RC0402FR-0711K8L
13k	RES SMD 13K OHM 1% 1/16W 0402	R12	1	YAGEO	RC0402FR-0713KL
14k	RES SMD 14K OHM 0.1% 1/16W 0402	R13	1	YAGEO	RT0402BRD0714KL
15k	RES SMD 15K OHM 0.1% 1/16W 0402	R14	1	YAGEO	RT0402BRD0715KL
16.2k	RES SMD 16.2K OHM 1% 1/16W 0402	R15	1	YAGEO	RC0402FR-0716K2L
2.4M	RES SMD 2.4M OHM 1% 1/10W 0603	R18	1	YAGEO	AC0603FR-072M4L
400M	RES 400MEG 5% 1206	R16, R17	2	Vishay Dale	CRHV1206AF400MJNE5

Appendix B

Reference Materials: Microcontroller Regulation

The microcontroller regulation code, implemented as a PID controller adapted from the previous work[2]. PID configuration was optimized for use with the additive HVPS through experimentation. Modifications performed in this work are in the main.c and adc1.c files, other files included are required to program the microcontroller but, were developed by the previous work[2]. The PIC12F1572 microcontroller code files are included as:

1. main.c
2. adc1.h
3. adc1.c
4. device_config.h
5. device_config.c
6. interrupt_manager.h
7. interrupt_manager.c
8. mcc.h

9. mcc.c
10. pin_manager.h
11. pin_manager.c
12. pwm1.h
13. pwm1.c
14. tmr0.h
15. tmr0.c
16. tmr2.h
17. tmr2.c

B.1 main.c

The PID regulation parameters were modified in main.c, the anti-windup term was implemented.

```
#include <stdint.h>
#include "mcc_generated_files/mcc.h"
#include "stdlib.h"

int16_t voltageSetPoint = 590; //(DESIRED_VOLTAGE*(2.4/800))*(1023/5V)
uint16_t offset = 155; // 0.25V offset target for PID loop
bool Started;
uint16_t duty_cycle;

#define max_integral 215 //The maximum contribution the integral can make

//Prototype 1 voltageSetPoint: 439
//PID Prototype 1: P:100 I:1 D:20

//Finalized PID Prototype 2
int16_t Kp = 26; //proportional gain
int16_t Ki = 2;//integral gain
int16_t Kd = 16; //derivative gain
int16_t errorIntegral = 0; //sum of errors
int16_t lasterr = 0;

void softStart(int16_t voltsetpoint,uint16_t voltRead);
void pwm_maintain(int16_t voltsetpoint,uint16_t voltRead);
void pwm_startup(void);
uint16_t pid_controller(int16_t error);

void main(void)
{
    // initialize the device
    SYSTEM_Initialize();
    Started = false;

    // Enable the Global Interrupts
    INTERRUPT_GlobalInterruptEnable();

    // Enable the Peripheral Interrupts
    INTERRUPT_PeripheralInterruptEnable();

    PWM1_PhaseSet(0);
    PWM1_PeriodSet(52); // 150kHz
    duty_cycle = 0; //Percent
```

```
    //Regulate the high voltage based on the PID controller
    while (1)
    {
        if(!Started){
            softStart(voltageSetPoint, ADC1_GetConversion(ADC_INPUT));
        }
        else {
            pwm_maintain(voltageSetPoint,ADC1_GetConversion(ADC_INPUT));
        }
    }
}
//Implementation of softStart from the previous work
void softStart(int16_t voltageSetPoint, uint16_t voltRead) {
    if(voltageSetPoint- offset >= voltRead){
        pwm_startup();
    }
    else {
        Started = true;
    }

}

/*
The PWM startup function was slowed down to reduce spikes in current draw
*/
void pwm_startup(void){
  __delay_ms(500);
    PWM1_Stop();
    if(duty_cycle <= 5 ){
          duty_cycle = duty_cycle + 1;
      }
    else if(duty_cycle <= 13 ){
          duty_cycle = duty_cycle + 2;
      }
    else if(duty_cycle <= 24 ){
          duty_cycle = duty_cycle + 3;
      }
    else {
        duty_cycle = 26;
        Started = true;
      }
      PWM1_DutyCycleSet(duty_cycle);
      PWM1_Start();
}
```

```
void pwm_maintain(int16_t voltsetpoint,uint16_t voltRead) {
    int16_t error; //error constant
    /*
    Check the difference between the set point and what was measured at the ADC
    */
    error = (voltsetpoint) - (int16_t)voltRead;
    uint16_t dutycycle;
    dutycycle = pid_controller(error);
    if(dutycycle == 0){
        PWM1_Stop();
    }
    //Safety check to prevent voltage spikes from changing the duty cycle
    else if(voltRead > 1.5*voltsetpoint){
       PWM1_Stop();
    }
    else {
       PWM1_Stop();
       PWM1_DutyCycleSet(dutycycle);
       PWM1_Start();
    }
}

uint16_t pid_controller(int16_t err) {
    //Apply the proportional gain to the error from the feedback
    int16_t P = Kp*err;

    //Integral Term
    errorIntegral = errorIntegral + err;

    //Prevent integral windup
    //If the integral exceeds the max_integral bound, set the value to the bound.
    if (errorIntegral > max_integral) { errorIntegral = max_integral; }
    //If the integral reaches a value below the integral minimum bound, set the
        value to the minimum bound.
    if (errorIntegral < -max_integral) { errorIntegral = -max_integral; }

    int16_t I = 0;

    I = Ki*(errorIntegral);

    int16_t D = Kd*(lasterr - err);
    lasterr = err;
    int16_t PID = P + I + D;
    PID = PID/100;
    //Bound the value of the PID control return value to 26, requiring a duty
        cycle of 50%.
```

```
    if(PID >= 26) {
        return 26;
    }
    if(PID <= 0) {
        return 0;
    }
    return (uint16_t)PID;
}
```

B.2 adc1.h

The C header file used by adc1.c to initialize ADC1 and to define specific conversion parameters.

```
#ifndef ADC1_H
#define ADC1_H

/**
  Section: Included Files
*/

#include <xc.h>
#include <stdint.h>
#include <stdbool.h>

#ifdef __cplusplus // Provide C++ Compatibility

    extern "C" {

#endif

//voltageRead declaration
uint16_t voltageRead;

// result size of an A/D conversion
typedef uint16_t adc_result_t;

/*
 *  result type of a Double ADC conversion
 */
typedef struct
{
    adc_result_t adcResult1;
    adc_result_t adcResult2;
} adc_sync_double_result_t;

/* ADC Channel Definition */

typedef enum
{
    ADC_INPUT = 0x3,
    channel_Temp = 0x1D,
    channel_DAC = 0x1E,
    channel_FVR = 0x1F
} adc_channel_t;
```

```
/*
    This routine initializes ADC1 and must be called prior to using other
        function of ADC1. THis function should only be called once during system
        initialization.
*/
void ADC1_Initialize(void);

/*
    Starts conversion
    This routine is used to start conversion of desired channel.
    The function ADC1_Initialize() must be called prior to using
        ADC1_GetConversionResult(void).
*/

/*
    Returns the ADC1 conversion value.
    This routine is used to get the analog to digital converted value from the
        specified channel. A value will only be returned after the conversion is
        complete, to check the status of the conversion use the
        ADC1_IsConversionDone() function.
 */
adc_result_t ADC1_GetConversionResult(void);

/*
    Returns the ADC1 conversion value from a specific channel. A channel number
        is required in order for the function to return a converted value.
    "For available channel refer to enum under adc.h file"
*/
adc_result_t ADC1_GetConversion(adc_channel_t channel);

/**
    Implements ISR, required for interrupt-driven actions.
*/
void ADC1_ISR(void);

/*
    Set ADC1 Interrupt Handler, this routine defines the function that will be
        called once an interrupt is triggered by ADC1.
*/
 void ADC1_SetInterruptHandler(void (* InterruptHandler)(void));

/*
    Timer Interrupt Handler
    This is a function pointer to the function that will be called during the
        ISR, the associated ADC1_SetInterruptHandler must be set prior to calling
        this function.
*/
```

```
extern void (*ADC1_InterruptHandler)(void);

/**
    Default Timer Interrupt Handler
    This is the default Interrupt Handler function and requires that the ADC1
       module and ADC1 ISR have been initialized.
*/
void ADC1_DefaultInterruptHandler(void);
#ifdef __cplusplus // Provide C++ Compatibility

    }

#endif

#endif  //ADC1_H
/**
 End of File
*/
```

B.3 adc1.c

The following C file initializes and configures ADC1.

```
#include <xc.h>
#include "adc1.h"
#include "device_config.h"

/**
  Section: Macro Declarations
*/

#define ACQ_US_DELAY 5


void (*ADC1_InterruptHandler)(void);

/**
  Section: ADC Module APIs
*/

void ADC1_Initialize(void)
{
    // set the ADC1 to the options selected in the User Interface

    // ADFM left; ADPREF VDD; ADCS FOSC/16;
    ADCON1 = 0xD0;

    // TRIGSEL TMR0_overflow;
    ADCON2 = 0x30;

    // ADRESL 0;
    ADRESL = 0x00;

    // ADRESH 0;
    ADRESH = 0x00;

    // GO_nDONE stop; ADON enabled; CHS AN0;
    ADCON0 = 0x01;

    // Enabling ADC1 interrupt.
    PIE1bits.ADIE = 1;

   // Set Default Interrupt Handler
    ADC1_SetInterruptHandler(ADC1_DefaultInterruptHandler);
}
```

```
adc_result_t ADC1_GetConversionResult(void)
{
    // Conversion finished, return the result
    return ((adc_result_t)((ADRESH << 8) + ADRESL));
}

adc_result_t ADC1_GetConversion(adc_channel_t channel)
{
    // select the A/D channel
    ADCON0bits.CHS = channel;

    // Turn on the ADC module
    ADCON0bits.ADON = 1;

    // Acquisition time delay
    __delay_us(ACQ_US_DELAY);

    // Start the conversion
    ADCON0bits.GO_nDONE = 1;

    // Wait for the conversion to finish
    while (ADCON0bits.GO_nDONE)
    {
    }

    // Conversion finished, return the result
    return ((adc_result_t)((ADRESH << 8) + ADRESL));
}


void ADC1_ISR(void)
{
    // Clear the ADC interrupt flag
    PIR1bits.ADIF = 0;

   if(ADC1_InterruptHandler)
    {
        ADC1_InterruptHandler();
    }
}

void ADC1_SetInterruptHandler(void (* InterruptHandler)(void)){
    ADC1_InterruptHandler = InterruptHandler;
}

void ADC1_DefaultInterruptHandler(void){
    voltageRead = ADC1_GetConversionResult();
```

```
}
/**
 End of File
*/
```

B.4 device_config.h

This is the header file to initialize the microcontroller clock and was auto-generated by MPLAB IDE.

```
#ifndef DEVICE_CONFIG_H
#define DEVICE_CONFIG_H

#define _XTAL_FREQ 8000000

#endif  /* DEVICE_CONFIG_H */
/**
 End of File
*/
```

B.5 device_config.c

This file initializes the microcontroller clock and was auto-generated by MPLAB IDE. Some methods were omitted as described by the previous work[2].

```
// Configuration bits: selected in the GUI

// CONFIG1
#pragma config FOSC = INTOSC // ->INTOSC oscillator; I/O function on CLKIN pin
#pragma config WDTE = OFF // Watchdog Timer Enable->WDT disabled
#pragma config PWRTE = OFF // Power-up Timer Enable->PWRT disabled
#pragma config MCLRE = ON // MCLR Pin Function Select->MCLR/VPP pin function is
    MCLR
#pragma config CP = OFF // Flash Program Memory Code Protection->Program memory
    code protection is disabled
#pragma config BOREN = NSLEEP // Brown-out Reset Enable->Brown-out Reset enabled
    while running and disabled in Sleep
#pragma config CLKOUTEN = OFF // Clock Out Enable->CLKOUT function is disabled.
    I/O or oscillator function on the CLKOUT pin

// CONFIG2
#pragma config WRT = OFF // Flash Memory Self-Write Protection->Write protection
    off
#pragma config PLLEN = OFF // PLL Enable->4x PLL disabled
#pragma config STVREN = ON // Stack Overflow/Underflow Reset Enable->Stack
    Overflow or Underflow will cause a Reset
#pragma config BORV = LO // Brown-out Reset Voltage Selection->Brown-out Reset
    Voltage (Vbor), low trip point selected.
#pragma config LPBOREN = OFF // Low Power Brown-out Reset enable bit->LPBOR is
    disabled
#pragma config LVP = ON // Low-Voltage Programming Enable->Low-voltage
    programming enabled
```

B.6 interrupt_manager.h

This code generates the interrupts used for the microcontroller, the code was auto-generated by MPLAB IDE. Some methods were omitted as described by the previous work[2].

```
#ifndef INTERRUPT_MANAGER_H
#define INTERRUPT_MANAGER_H


/*
    Enable global interrupts.
 */
#define INTERRUPT_GlobalInterruptEnable() (INTCONbits.GIE = 1)

/*
    Disable global interrupts.
 */
#define INTERRUPT_GlobalInterruptDisable() (INTCONbits.GIE = 0)
/**
    Enable peripheral interrupts.
 */
#define INTERRUPT_PeripheralInterruptEnable() (INTCONbits.PEIE = 1)

/**
    Disable peripheral interrupts.
 */
#define INTERRUPT_PeripheralInterruptDisable() (INTCONbits.PEIE = 0)


#endif // INTERRUPT_MANAGER_H
/**
 End of File
*/
```

B.7 interrupt_manager.c

The following code enables various interrupts used by the microcontroller. Some methods were omitted as described by the previous work[2].

```
#include "interrupt_manager.h"
#include "mcc.h"

void __interrupt() INTERRUPT_InterruptManager (void)
{
    // interrupt handler
    if(INTCONbits.PEIE == 1)
    {
        if(PIE1bits.ADIE == 1 && PIR1bits.ADIF == 1)
        {
            ADC1_ISR();
        }
        else
        {
        }
    }
    else
    {
    }
}
/**
 End of File
*/
```

B.8 mcc.h

This file defines states required for the microcontroller, some methods were omitted as described by the previous work[2].

```
#ifndef MCC_H
#define MCC_H
#include <xc.h>
#include "device_config.h"
#include "pin_manager.h"
#include <stdint.h>
#include <stdbool.h>
#include <conio.h>
#include "interrupt_manager.h"
#include "pwm1.h"
#include "tmr2.h"
#include "adc1.h"
#include "tmr0.h"



/*
    Initializes the device to the default states configured in the MCC GUI
 */
void SYSTEM_Initialize(void);

/*
    Initializes the oscillator to the default states configured in the MCC GUI
 */

void OSCILLATOR_Initialize(void);
/*
   Initializes the WDT module to the default states configured in the MCC GUI
 */
void WDT_Initialize(void);

#endif  /* MCC_H */
/**
 End of File
*/
```

B.9 mcc.c

This file defines states required for the microcontroller, some methods were omitted as described by the previous work[2].

```
#include "mcc.h"


void SYSTEM_Initialize(void)
{

    PIN_MANAGER_Initialize();
    OSCILLATOR_Initialize();
    WDT_Initialize();
    PWM1_Initialize();
    ADC1_Initialize();
    TMR2_Initialize();
    TMR0_Initialize();
}

void OSCILLATOR_Initialize(void)
{
    // SCS FOSC; SPLLEN disabled; IRCF 8MHz_HF;
    OSCCON = 0x70;
    // TUN 0;
    OSCTUNE = 0x00;
    // SBOREN disabled; BORFS disabled;
    BORCON = 0x00;
}

void WDT_Initialize(void)
{
    // WDTPS 1:65536; SWDTEN OFF;
    WDTCON = 0x16;
}

/**
 End of File
*/
```

B.10 pin_manager.h

This file initializes the microcontroller pin configurations and was auto-generated by MPLAB IDE. Functionality not required was removed following the method defined in the previous work[2].

```
#ifndef PIN_MANAGER_H
#define PIN_MANAGER_H

/**
  Section: Included Files
*/

#include <xc.h>

#define INPUT  1
#define OUTPUT 0

#define HIGH   1
#define LOW    0

#define ANALOG    1
#define DIGITAL   0

#define PULL_UP_ENABLED   1
#define PULL_UP_DISABLED  0

// get/set RA1 procedures
#define RA1_SetHigh()         do { LATAbits.LATA1 = 1; } while(0)
#define RA1_SetLow()          do { LATAbits.LATA1 = 0; } while(0)
#define RA1_Toggle()          do { LATAbits.LATA1 = ~LATAbits.LATA1; } while(0)
#define RA1_GetValue()           PORTAbits.RA1
#define RA1_SetDigitalInput() do { TRISAbits.TRISA1 = 1; } while(0)
#define RA1_SetDigitalOutput() do { TRISAbits.TRISA1 = 0; } while(0)
#define RA1_SetPullup()         do { WPUAbits.WPUA1 = 1; } while(0)
#define RA1_ResetPullup()       do { WPUAbits.WPUA1 = 0; } while(0)
#define RA1_SetAnalogMode()     do { ANSELAbits.ANSA1 = 1; } while(0)
#define RA1_SetDigitalMode()    do { ANSELAbits.ANSA1 = 0; } while(0)

// get/set ADC_INPUT aliases
#define ADC_INPUT_TRIS             TRISAbits.TRISA4
#define ADC_INPUT_LAT              LATAbits.LATA4
#define ADC_INPUT_PORT             PORTAbits.RA4
#define ADC_INPUT_WPU              WPUAbits.WPUA4
#define ADC_INPUT_OD               ODCONAbits.ODA4
#define ADC_INPUT_ANS              ANSELAbits.ANSA4
```

```
#define ADC_INPUT_SetHigh()         do { LATAbits.LATA4 = 1; } while(0)
#define ADC_INPUT_SetLow()          do { LATAbits.LATA4 = 0; } while(0)
#define ADC_INPUT_Toggle()          do { LATAbits.LATA4 = ~LATAbits.LATA4; }
    while(0)
#define ADC_INPUT_GetValue()        PORTAbits.RA4
#define ADC_INPUT_SetDigitalInput() do { TRISAbits.TRISA4 = 1; } while(0)
#define ADC_INPUT_SetDigitalOutput() do { TRISAbits.TRISA4 = 0; } while(0)
#define ADC_INPUT_SetPullup()       do { WPUAbits.WPUA4 = 1; } while(0)
#define ADC_INPUT_ResetPullup()     do { WPUAbits.WPUA4 = 0; } while(0)
#define ADC_INPUT_SetPushPull()     do { ODCONAbits.ODA4 = 0; } while(0)
#define ADC_INPUT_SetOpenDrain()    do { ODCONAbits.ODA4 = 1; } while(0)
#define ADC_INPUT_SetAnalogMode()   do { ANSELAbits.ANSA4 = 1; } while(0)
#define ADC_INPUT_SetDigitalMode()  do { ANSELAbits.ANSA4 = 0; } while(0)

/*
    GPIO and peripheral I/O initialization
 */
void PIN_MANAGER_Initialize (void);

#endif // PIN_MANAGER_H
/**
 End of File
*/
```

B.11 pin_manager.c

This file initializes the microcontroller pin configurations and was auto-generated by MPLAB IDE. Functionality not required was removed following the method defined in the previous work[2].

```
#include "pin_manager.h"




void PIN_MANAGER_Initialize(void)
{
    /* LATx registers*/
    LATA = 0x00;

    /* TRISx registers */
    TRISA = 0x3D;

    /* ANSELx registers */
    ANSELA = 0x14;

    /* WPUx registers */
    WPUA = 0x00;
    OPTION_REGbits.nWPUEN = 1;

    /* ODx registers */
    ODCONA = 0x00;

    /* SLRCONx registers */
    SLRCONA = 0x37;

    /* INLVLx registers */
    INLVLA = 0x3F;

    /* APFCONx registers */
    APFCON = 0x00;

}


/**
 End of File
*/
```

B.12 pwm1.h

This file initializes the PWM for the microcontroller and was auto-generated by MPLAB IDE. Functionality not required was removed following the method defined in the previous work[2].

```
#ifndef PWM1_H
#define PWM1_H

/**
  Section: Included Files
*/

#include <xc.h>
#include <stdint.h>
#include <stdbool.h>

#ifdef __cplusplus // Provide C++ Compatibility

    extern "C" {

#endif

/**
  Section: PWM Module APIs
*/

/*
    This routine initializes PWM1 and must be called prior to using PWM1, this
        function should only be initialized once.
*/
void PWM1_Initialize(void);

/*
    This function starts PWM1 and must be called after PWM1 is initialized.
*/
void PWM1_Start(void);

/*
    This function stops PWM1 and must be called after PWM1_Start(void) has been
        called.
*/
void PWM1_Stop(void);

/*
    Load required 16 bit phase count
```

```
    Set the expected phase count
*/
void PWM1_PhaseSet(uint16_t phaseCount);

/**
  Load required 16 bit Duty Cycle
  Set the expected Duty Cycle
*/
void PWM1_DutyCycleSet(uint16_t dutyCycleCount);

/*
  Load required 16 bit Period
  Set the expected Period
*/
void PWM1_PeriodSet(uint16_t periodCount);

#endif  /* PWM1_H */
/**
 End of File
*/
```

B.13 pwm1.c

This file uses the pwm1.h header file to perform PWM as required by the microcontroller and was auto-generated by MPLAB IDE. Functionality not required was removed following the method defined in the previous work[2].

```
#include <xc.h>
#include "pwm1.h"

/**
  Section: PWM1 APIs
*/

void PWM1_Initialize(void)
{
    // set the PWM1 to the options selected in the User Interface

     //PHIE disabled; DCIE disabled; OFIE disabled; PRIE disabled;
    PWM1INTE = 0x00;

     //PHIF cleared; OFIF cleared; DCIF cleared; PRIF cleared;
    PWM1INTF = 0x00;

     //PS No_Prescalar; CS FOSC;
    PWM1CLKCON = 0x00;

     //LDS reserved; LDT disabled; LDA do_not_load;
    PWM1LDCON = 0x00;

     //OFM independent_run; OFS reserved; OFO match_incrementing;
    PWM1OFCON = 0x00;

     //PWM1PHH 0;
    PWM1PHH = 0x00;

     //PWM1PHL 0;
    PWM1PHL = 0x00;

     //PWM1DCH 0;
    PWM1DCH = 0x00;

     //PWM1DCL 0;
    PWM1DCL = 0x00;

     //PWM1PRH 0;
    PWM1PRH = 0x00;
```

```
    //PWM1PRL 31;
    PWM1PRL = 0x1F;

    //PWM1OFH 0;
    PWM1OFH = 0x00;

    //PWM1OFL 31;
    PWM1OFL = 0x1F;

    //PWM1TMRH 0;
    PWM1TMRH = 0x00;

    //PWM1TMRL 0;
    PWM1TMRL = 0x00;

    //MODE standard_PWM; POL active_hi; OE enabled; EN enabled;
    PWM1CON = 0xC0;

}


void PWM1_Start(void)
{
    PWM1CONbits.EN = 1;
}

void PWM1_Stop(void)
{
    PWM1CONbits.EN = 0;
}


void PWM1_PhaseSet(uint16_t phaseCount)
{
    PWM1PHH = (uint8_t)(phaseCount>>8);    //writing 8 MSBs to PWMPHH register
    PWM1PHL = (uint8_t)(phaseCount);       //writing 8 LSBs to PWMPHL register
}

void PWM1_DutyCycleSet(uint16_t dutyCycleCount)
{
    PWM1DCH = (uint8_t)(dutyCycleCount>>8); //writing 8 MSBs to PWMDCH register
    PWM1DCL = (uint8_t)(dutyCycleCount); //writing 8 LSBs to PWMDCL register
}

void PWM1_PeriodSet(uint16_t periodCount)
{
```

```
    PWM1PRH = (uint8_t)(periodCount>>8); //writing 8 MSBs to PWMPRH register
    PWM1PRL = (uint8_t)(periodCount); //writing 8 LSBs to PWMPRL register
}

/**
 End of File
*/
```

B.14 tmr0.h

The following header file defines timer 0 for the microcontroller. This file was auto-generated by MPLAB IDE and methods not required were removed[2].

```
#ifndef TMR0_H
#define TMR0_H

/**
  Section: Included Files
*/

#include <stdint.h>
#include <stdbool.h>

#ifdef __cplusplus // Provide C++ Compatibility

    extern "C" {

#endif

/**
  Section: TMR0 APIs
*/

/*
  Initializes the TMR0 module and registers, this initialization must be called
      before using the other functions of TMR0.
*/
void TMR0_Initialize(void);

#ifdef __cplusplus // Provide C++ Compatibility

    }

#endif

#endif // TMR0_H
/**
 End of File
*/
```

B.15 tmr0.c

The following C file uses the definition from the tmr0.h header file to initialize timer 0. This file was auto-generated by MPLAB IDE and methods not required were removed[2].

```
#include <xc.h>
#include "tmr0.h"

/**
  Section: Global Variables Definitions
*/

volatile uint8_t timer0ReloadVal;
/**
  Section: TMR0 APIs
*/

void TMR0_Initialize(void)
{
    // Set TMR0 to the options selected in the User Interface

    // PSA assigned; PS 1:256; TMRSE Increment_hi_lo; mask the nWPUEN and INTEDG
       bits
    OPTION_REG = (uint8_t)((OPTION_REG & 0xC0) | (0xD7 & 0x3F));

    // TMR0 236;
    TMR0 = 0xEC;

    // Load the TMR value to reload variable
    timer0ReloadVal= 236;

    // Clearing IF flag
    INTCONbits.TMR0IF = 0;
}

/**
  End of File
*/
```

B.16 tmr2.h

The following header file defines timer 2 for the microcontroller. This file was auto-generated by MPLAB IDE and methods not required were removed[2].

```
#ifndef TMR2_H
#define TMR2_H

/**
  Section: Included Files
*/

#include <stdint.h>
#include <stdbool.h>

#ifdef __cplusplus // Provide C++ Compatibility

    extern "C" {

#endif

/*
    Initializes the TMR2 module and registers, this is required prior to using
        any other TMR2 functions.
*/
void TMR2_Initialize(void);

/**
    This function starts TMR2
*/

 #ifdef __cplusplus // Provide C++ Compatibility

    }

#endif

#endif // TMR2_H
/**
 End of File
*/
```

B.17 tmr2.c

The following C file uses the definition from the tmr2.h header file to initialize timer 2. This file was auto-generated by MPLAB IDE and methods not required were removed[2].

```
#include <xc.h>
#include "tmr2.h"

/**
  Section: Global Variables Definitions
*/

/**
  Section: TMR2 APIs
*/

void TMR2_Initialize(void)
{
    // TMR2 options selected in the User Interface

    // PR2 12;
    PR2 = 0x0C;

    // TMR2 0;
    TMR2 = 0x00;

    // Clearing IF flag.
    PIR1bits.TMR2IF = 0;

    // T2CKPS 1:1; T2OUTPS 1:1; TMR2ON on;
    T2CON = 0x04;
}

/**
  End of File
*/
```