The Future of Semiconductor Manufacturing: EUV Lithography

by

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A REPORT

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Abstract

The global semiconductor industry is projected to grow exponentially from $775 billion to $1.6 trillion by 2030 which has motivated companies to find more efficient ways to manufacture semiconductors by reducing costs or reducing transistor sizes as proposed by Moore's Law. Once DUV lithography hit its cap at 32 nm node sizes with immersion lithography, a new lithographic technique needed to be developed in order to continue the shrinkage; EUV lithography, first readily used, in 2019, provided an innovative way to push node sizes to sub-7 nm by decreasing the wavelength of light by 14x. With the adoption of EUV lithography in advanced logic and memory-based applications, there still continues to be innovation aimed at increasing overall process efficiency through process improvements, as well as pushing node sizes even smaller to most recently <2nm with the introduction of the next generation EUV technology. This report provides a deep understanding of the EUV process that is critical for maintaining the pace of transistor miniaturization. In order to accomplish this, everything relating to the EUV process: fundamentals, system architecture, masks and pellicles, photoresists, technical challenges, industrial adoption, recent advances, and future possibilities are explained. Despite ongoing challenges, recent advancements in this space have spurred next generation lithographic techniques along with the potential to make EUV lithography realistic for more mature nodes.

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Introduction

Semiconductors, which contain integrated circuits (chips) constructed using hundreds to thousands of transistors, are fundamental components of modern-day life and can be found everywhere. Whether it's a car, mobile phone, or even a microwave, all of these applications contain chips that are necessary for them to operate. Consequently, the semiconductor industry market is massive, generating an immense amount of revenue to companies who sell analog and embedded devices for electronics. As of 2024, the sector's market cap is $775 billion worldwide with no signs of stopping. In fact, McKinsey & Company estimates that the semiconductor industry could amass a market cap of greater than $1.6 trillion by 2030 primarily with the help of AI adoption[1]. Although every sector is projected to grow into 2030, computing and data storage applications alone are estimated to be ~55% of the industries combined market cap. This is especially amazing considering that mainstream adoption of AI didn't start until around 2020.

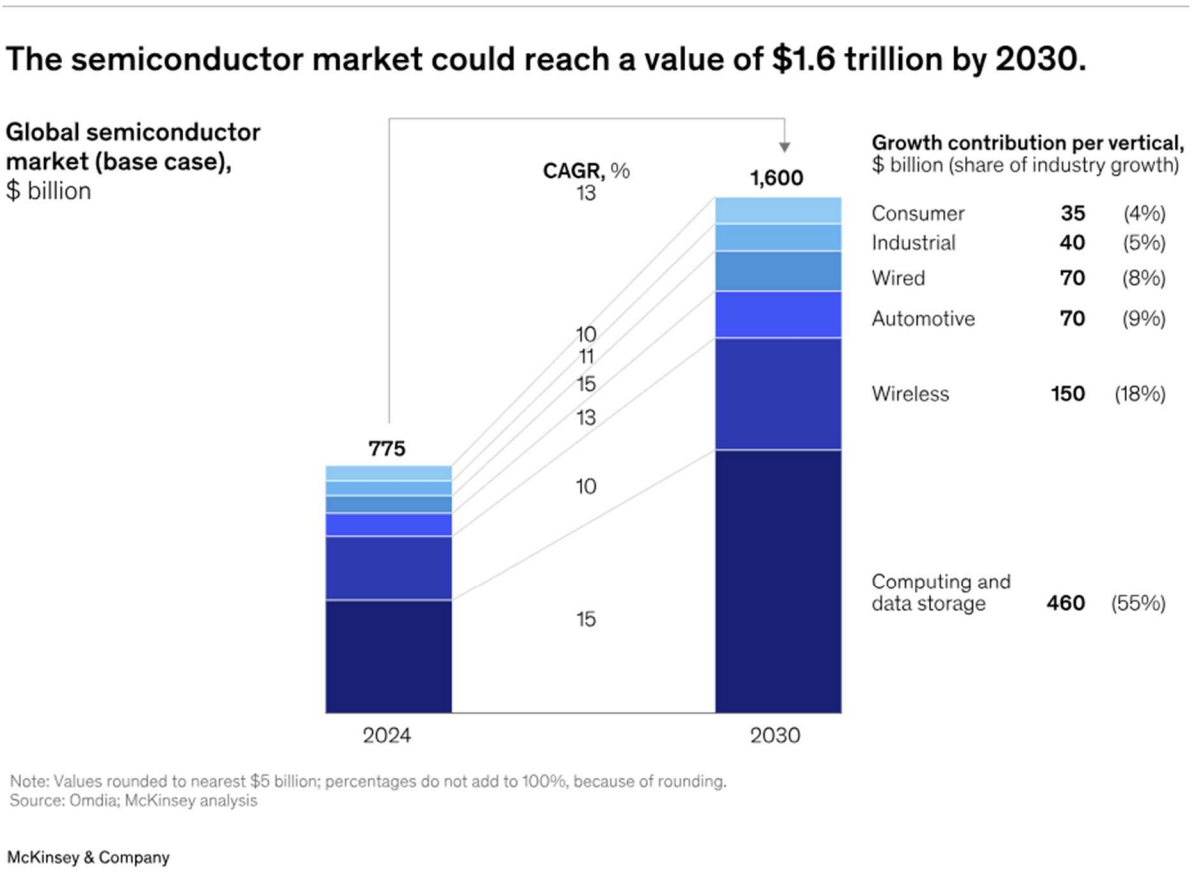

Figure 1: Global Semiconductor Market Projection [1]

In the semiconductor market, there are three major semiconductor markets: leading-edge, advanced and mature nodes, and memory. The leading-edge and advanced and mature node markets are both composed of analog and logic-based devices, unlike memory, although differ in the device's actual node size. The leading-edge market is by far the most advanced of the three with sub-7nm nodes and a focus on maximum performance which is necessary for AI-based applications. Advanced and mature nodes represent more core semiconductor markets with their node sizes of ~7nm – 28nm and >28nm respectively. The memory market is separated due to its focus on data storage rather than pure calculation and casts a wide net. Currently, leading-edge

dominates market share, followed by memory-based applications advanced and mature nodes only retaining a small fraction. This trend is expected to continue due to the projected growth in the wireless and computer and data storage segments.

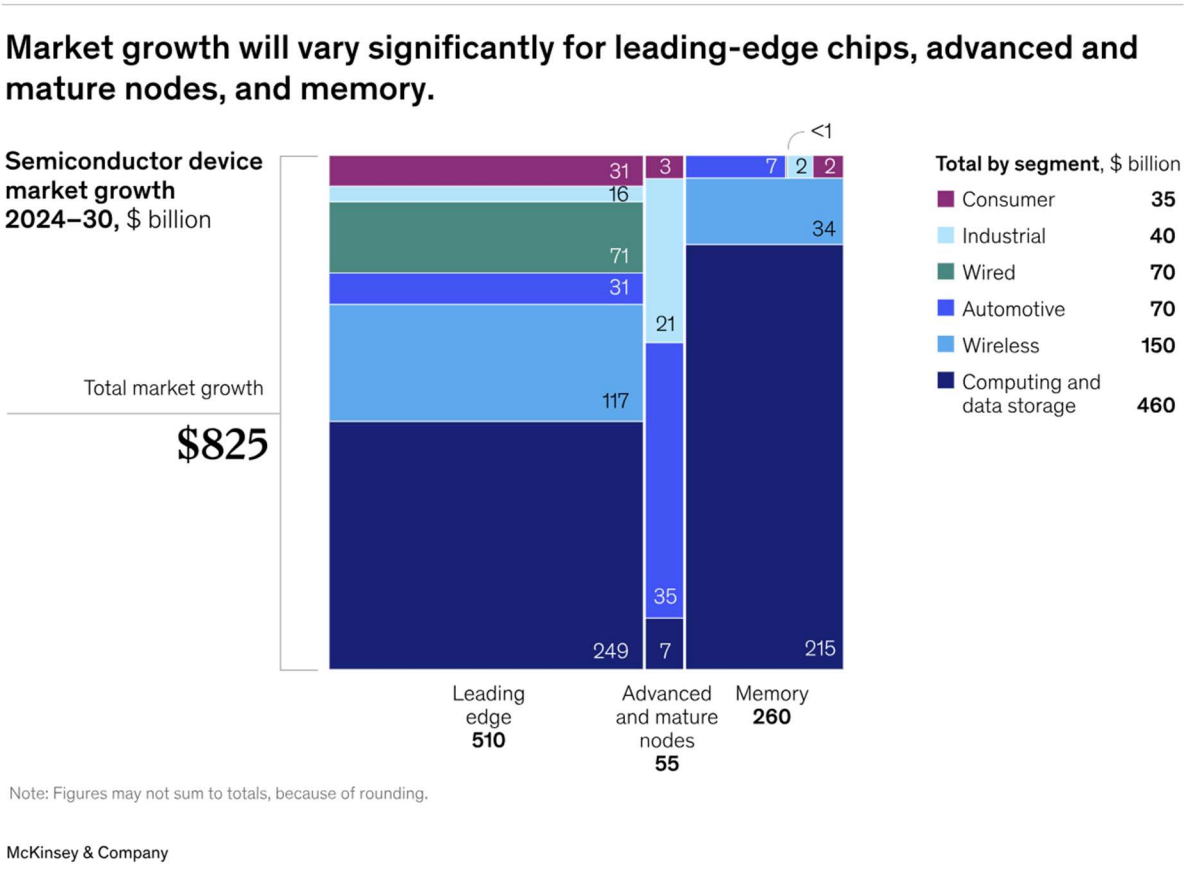

Figure 2: Global Semiconductor Market Projection by Segment ***[1]***

With an already multi-billion-dollar industry, it is important for companies to economically produce as many chips as possible so that they can maximize their total revenue; this is where innovation comes into play. Currently, hundreds to thousands of individual chips

can be cut off from a single 300mm silicon wafer which can contain millions of transistors. For a company wanting to increase their profit margins, there's no better way to do this than to manufacture smaller transistors which can in turn allow for more transistors to fit on a single silicon wafer. Along with high profit margins, creating smaller transistors also improves their performance and efficiency. These factors have created a need for constant innovation and, therefore, a rapid advancement in modern electronics through decreasing transistor sizes.

Due to the benefits of decreasing transistor sizes, the co-founder of Intel: Gordon Moore in 1965 made an important observation that still mostly holds up to this day and is coined Moore's Law. Moore's Law observed that the number of transistors in a microchip doubles approximately every two years with minimal rise in cost.

Some experts, such as Nvidia CEO Jensen Huang, have declared this Law to have been invalidated since around 2023 due to Moore's Law flattening driven by an increase in miniaturization time (see figure 3). Piggy backing off the now "obsolete" Moore's Law, the Nvidia CEO observed that the performance of GPUs has significantly increased and will more than double every two years. Although it seems like there is a bit of flattening when it comes to transistor density doubling, a redefinition of Moore's Law instead relating to the features critical dimension over time still holds true (see figure 4) [2]. Even though the current validity of the original Moore's law has been debated, it's effect on the semiconductor industry as well as the Laws aspiration still continues to guide the industry.

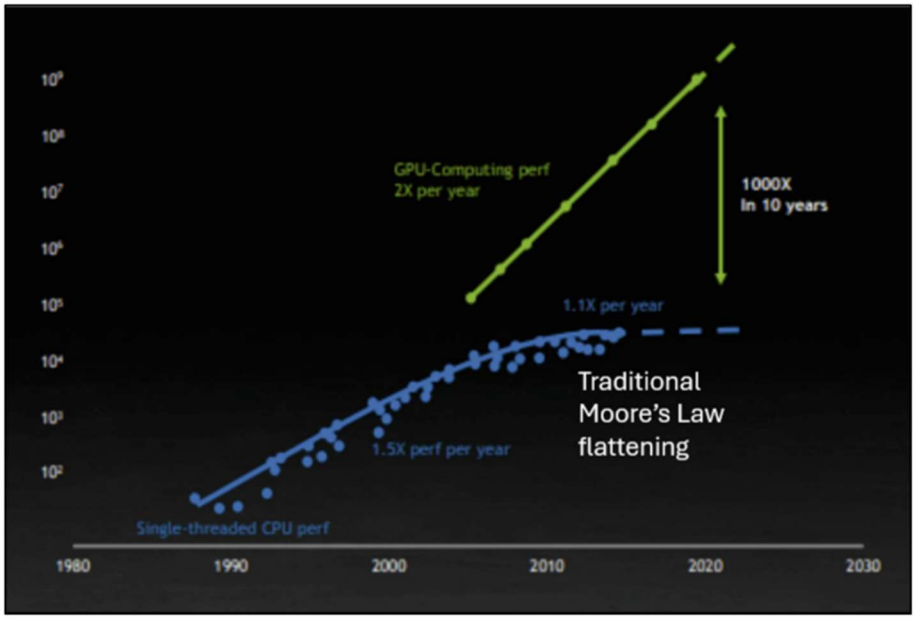

Figure 3: NVIDIA's prediction of the end of Moore's Law with its replacement of GPU performance [2]

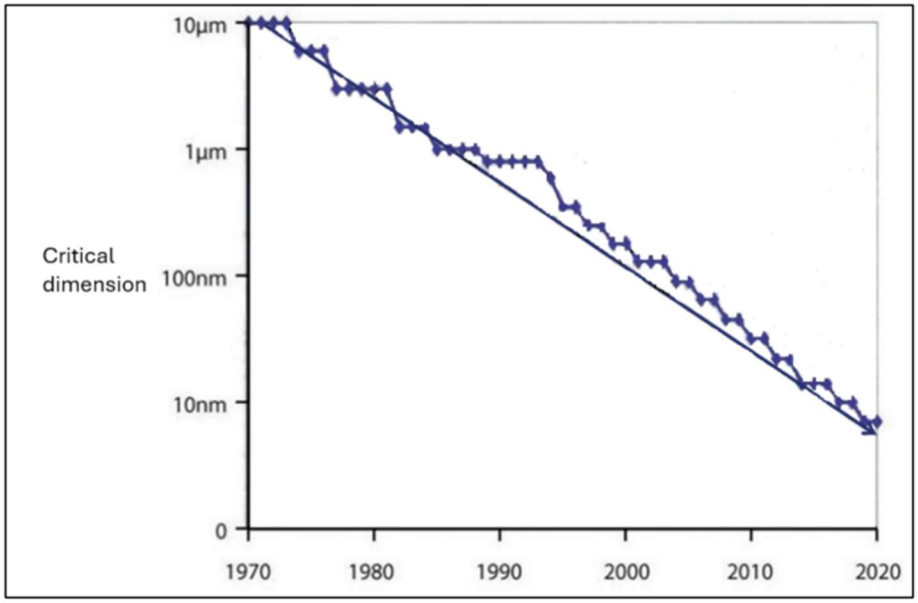

Figure 4: Overall critical dimension (CD) vs Time [2]

Intel, like other companies, are continuing to find ways to fit even more transistors per package and are aspiring to hit a whopping 1 trillion transistors per package in 2030 (see figure 5). They are just one company that proves that the drive leading to Moore's Law still exists.

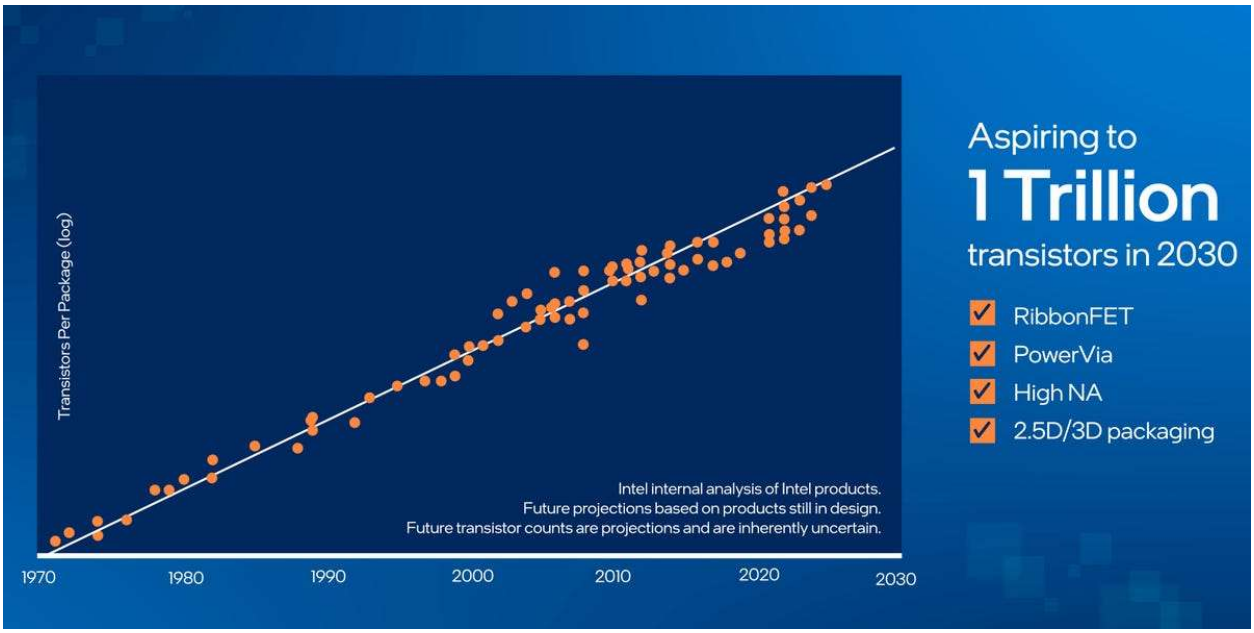

Figure 5: Intel's Projection to reach 1 trillion TPP by 2030 [2]

When it comes to miniaturization, the most essential process in semiconductor manufacturing is photolithography as it directly defines the size of the transistors. In its simplest terms, photolithography is a process of transferring patterns from a mask to the surface of a silicon wafer with the help of photoresist. The last major technology, 193nm lithography, was first introduced in 2003 [3]. 193nm lithography, also known as dry deep ultraviolet (DUV) lithography employs an ArF laser to print patterns on the silicon wafer. With this technology, printed features down to 90nm can be achieved. Immersion lithography, a breakthrough DUV technology was implemented in 2009 and was able to further shrink printed features down to 32nm [3]. Immersion lithography utilizes purified water between the lens and the wafer, as

opposed to the use of air in dry lithography, which significantly increases the numerical aperture. This increase in NA translates to an increase in the minimum resolution making it possible to print smaller feature sizes [4]. After 2009, it seemed like semiconductor manufacturers were stuck and unable to find feasible ways to cost-effectively print feature sizes smaller than 32nm but as Moore's Law states, decreasing transistor sizes will occur [3]. It wasn't until 10 years later that Extreme Ultraviolet (EUV) Lithography was fully developed, enabling printed feature sizes all the way down to 7nm [3].

EUV lithography is a new and innovative technique that continues to push the boundaries of the semiconductor industry. A proper understanding of this technology is foundational not only to create the world's most advanced microchips, but also to act as a necessary milestone for maintaining the pace of transistor miniaturization. In order to convey this message to its entirely, EUV lithography will be thoroughly explained into the following sections: fundamentals, system architecture, EUV masks and pellicles, photoresists for EUV, technical challenges, industrial adoption, recent advances, and future possibilities. Only then can we predict the future of the semiconductor manufacturing industry.

EUV Fundamentals

The current limits of resolution directly define the smallest feature size that is possible on a transistor which was first developed by Lord Rayleigh in the 19th century. This principle is known as the Rayleigh Criterion and has been used to guide lithographic innovations ever since. The Rayleigh Criterion (equation 1) is made up of 3 different variables: k_1, λ, and NA. The first variable, most commonly called the k_1 factor, represents a collection of physical lithographic factors that can enhance resolution [5].

$$\boldsymbol{CD = k_1 * \frac{\lambda}{Na}}$$

Equation 1: Critical Dimension (CD)

The type of lens, resist, equipment, and process control strategy all influence the k_1 factor. With the physical limit of lithography being set at a typical k_1 value of 0.25, the other variables are commonly manipulated to maximize resolution. The wavelength of light (λ) and the numerical aperture (NA) are the other two variables in the Rayleigh Criterion and represent the workhorses for innovation. The wavelength of light represents the distance between the peaks of a light wave and with a shorter wavelength, smaller feature sizes can be printed. The numerical aperture is a dimensionless number that characterizes the light-gathering ability of an optical system and is typically the easiest of the three to manipulate. As can be seen from the Rayleigh Criterion, to achieve the smallest resolution value requires the combination of a shorter wavelength, a larger numerical aperture and pushing the k_1 factor as close to its physical limit of 0.25 as possible.

Lithographic Technique	Wavelength (λ, nm)	Numerical Aperture (NA)	Smallest CD size (nm)
DUV Lithography (Dry)	193	0.50 – 0.93	~50-65
Immersion Lithography	193	1.20 – 1.35	28
EUV Lithography	13.5	0.33	~7
High-NA Lithography	13.5	0.55	<2

Table 1: Lithographic techniques and their associated properties

Table 1 provides us with the most widely used lithographic techniques in the semiconductor industry today along with their associated properties. As can be seen, EUV lithography is able to produce smaller feature sizes than DUV lithography due to a 14x decrease in the wavelength of light (193nm to 13.5nm). Its unique light generation process produces a pattern onto the individual wafers. To generate this light, a high-powered CO_2 laser fires two pulses at fast-moving droplets of molten tin in a vacuum chamber to flatten and superheat them [6], [7]. Thus, creating an excited plasma that emits light at 13.5nm and enables the ability to produce such small feature sizes. Despite the clear advantages of this process, in practice, there are a few major generation challenges. First, the overall conversion efficiency is quite low; Only around 5-6% of energy generated by the laser is converted into usable photons that emit

plasma[8]. Second, there are power challenges that limit its functionality. The EUV scanners require an immense amount of power. On average, these scanners have an annual consumption of roughly 1400 kW/hr per machine which is enough to power a small city [9]! This can be extremely costly and might not even be feasible in some places due to power regulation laws.

Third, the optical system of EUV Lithography tools is quite complex. Unlike DUV machines which use refractive optics, EUV requires reflective optics. Both refractive and reflective optics relate to how light interacts with materials/surfaces but differ in function. In reflection, light bounces off of a surface and returns to the same medium while refraction involves the bending of light through a medium. EUV cannot use refractive optics due to the emitted light having such a short wavelength that it is strongly absorbed by materials.

EUV systems use reflective optics composed of multilayer reflectors, also called Bragg mirrors, that are alternating layers of Mo/Si pairs [10]. This optical system was specifically designed for EUV lithography as light in this wavelength region is absorbed by every material, so refractive optics aren't possible. This process occurs at vacuum pressure to maximize potential efficiency as air molecules absorb the emitted light caused by the superheating of tin droplets.

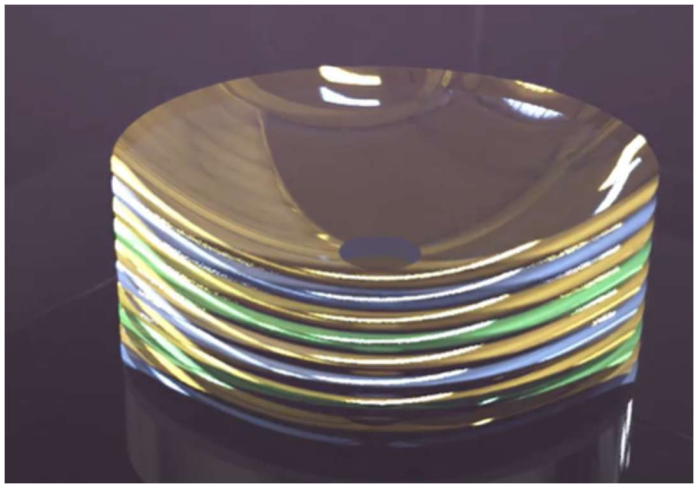

Figure 6: A Bragg Mirror containing Mo/Si pairs [10]

These mirrors are curved and operate via constructive interference where light is reflected by each of the individual Mo/Si pairs that in turn get superimposed causing the light to be amplified into a usable intensity; one pair of Mo/Si layers only reflect around 1% of light [10]. To improve reflectivity, a stack of around 100 pairs, that are only a few atomic layers, increases the reflectivity of usable light to around 70%. Given the extremely small node sizes for this application, extreme precision is necessary and possible through this technique although even the smallest irregularity degrades the overall imaging quality that is transferred to the wafers surface.

EUV Lithography System Architecture

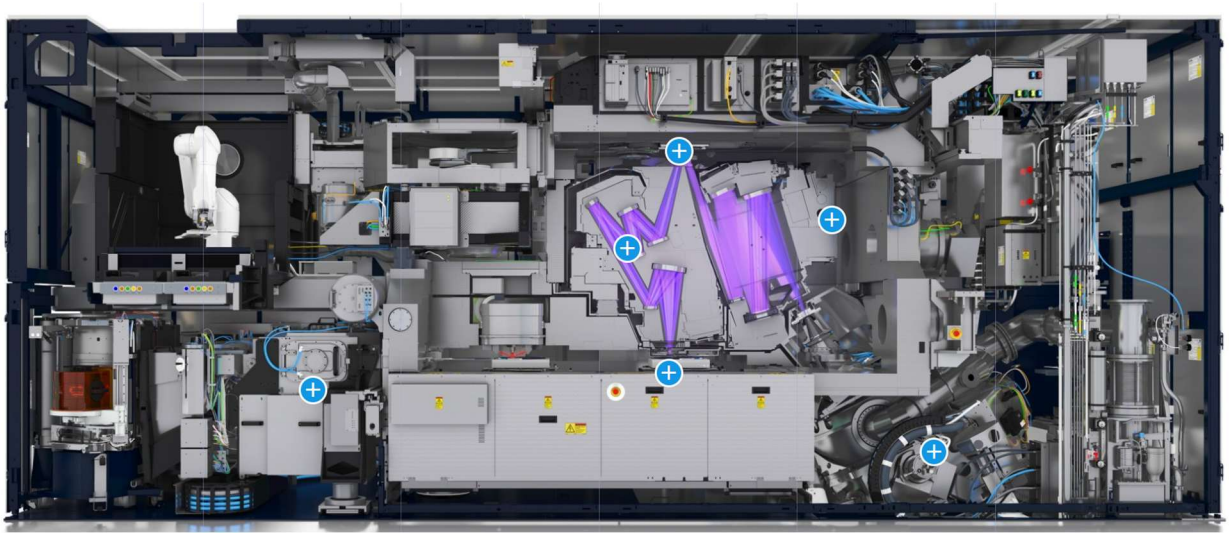

Figure 7: Inside of NXE lithography system [7]

The system architecture design of EUV machines is quite complex overall, but necessary to print such small feature size. ASML currently dominates the market for these machines and owns a monopoly on its technology [11] although there are others who are quickly trying to catch up and take market share. As a result, this section will be specifically talking about the architecture of ASML's NXE systems. Before and after a wafer gets exposed to the EUV scanner, it needs to go through an integrated, but separate machine that is merely focused on the photoresist process that is called a photolithographic track. This photoresist process is mostly identical to previous lithographic iterations due to the preparation, coating, baking, and developing of photoresist being the exact same with the exception of different photoresists being used.

The scanner (exposure) side of the process makes EUV lithography different and innovative. After photoresist is applied and baked, wafers go into the exposure unit to get patterned. During this process, all of the scanner components differ immensely from DUV lithography: light source, optics, reticles, wafer handler, and wafer stage [7].

The sole objective of optics in an EUV system is to direct the energy generated from the light source to the silicon wafer itself so that it can be used for patterning. Through the use of Bragg mirrors, this light can be guided onto the wafer with limited waste.

In photolithography, reticles are used to transfer a pattern onto silicon wafers. For DUV applications, reticles are transparent quartz plates with an opaque chrome pattern. For these reticles, the light that passes through the reticle is absorbed by the photoresist onto the wafer while opaque regions block the light thus creating the necessary pattern. The reticles in EUV applications are instead reflective and are in the form of a multilayer Bragg mirror which guides the light to its spot on the silicon wafers.

Although they might seem trivial, the wafer handler and wafer stage are both crucial processes for proper lithography processes. The wafer handler transfers wafers in and out of the system's environment with great precision; this is important to ensure the care of the delicate wafers. ASML mentions operating conditions with a positioning accuracy of 25 micrometers (um)I and a uniform surface temperature within 2 mK. The wafer stage is responsible for positioning the wafer during exposure for proper and uniform exposure. This stage positions the

wafer within a quarter of a nanometer for each exposure and checks/adjusts 20,000 times per second [7].

A unique aspect of EUV lithography involves vacuum conditions for the wafer during exposure. The tool has a vacuum chamber design that is unlike other lithography machines due to its extremely small wavelength of light. The 13.5 nm light is absorbed by everything, including air itself, so the entire unit must be in complete vacuum for maximum efficiency. A very low vacuum condition is achieved by a series of vacuum chambers, dry pumps, and tools such as pressure gauges that help to keep the integrity of the system. In addition, the vacuum environment also helps to prevent any contamination build-up in the system that can be detrimental to the devices. Since EUV lithography enables sub-7 nm nodes, this means that contamination control is more important than ever because even the smallest defect can destroy hundreds to thousands of individual die at once. By maintaining a very low-pressure environment, there are a few sources of contamination that can be mitigated. The first comes from the cracking of adsorbed organic molecules such as carbon which can negatively impact image and critical dimension (CD) performance [12]. These organic molecules get cracked as a result of getting hit by the very low wavelength photons which break the chemical bonds in photoresists. Once this happens, contaminants may be outgassed and deposited onto a spot where it degrades the reflective performance of the mirror causing worse overall process efficiency and costly tool maintenance. By maintaining low pressure, the rate of surface-adsorbate contamination is lessened. Figure 8 shows the carbon growth rate as a function of pressure as monitored in real time with a null-field imaging ellipsometer (NEIS) and an electrometer. It is clear that at higher pressures, the level of EUV-induced carbon growth accelerates rapidly.

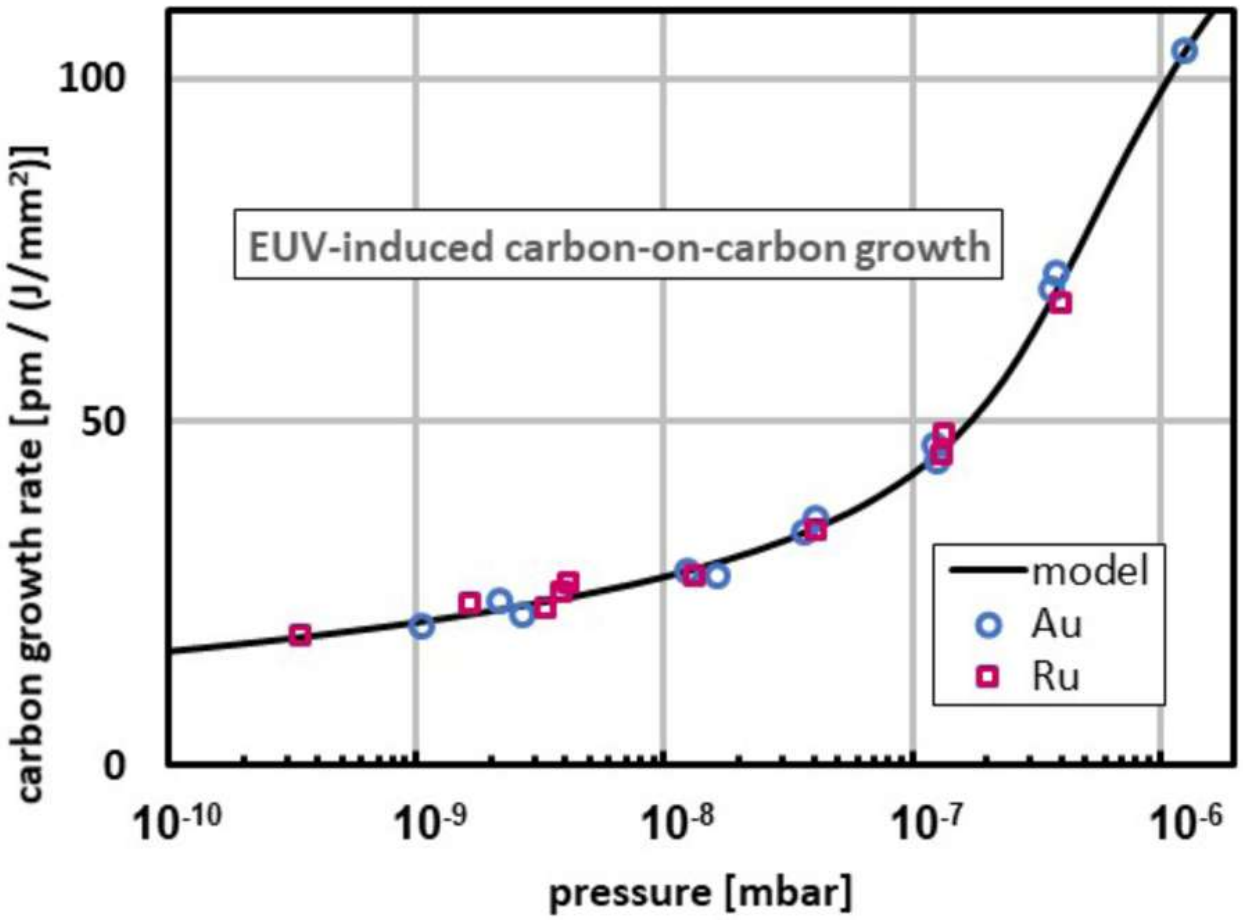

Figure 8: EUV-induced Carbon Growth vs Pressure [12]

Another potential contamination source is from tin droplet deposits that might build up onto the mirrors during operation. These droplets are very harmful to the system as they reduce the overall reflectivity of the mirror [13]. With the combination of vacuum pressure and regular cleaning, this issue can be mitigated.

EUV Masks and Pellicles

The innovative mask design for these EUV machines is one aspect that truly makes the process possible. The substrate of the mask is made from material containing a low thermal expansion coefficient aimed at maintaining cleanliness on the surface of the mask. Materials with a low thermal expansion coefficient are inherently great since they are less prone to size fluctuations as a result of thermal effects which in turn can generate defects onto the photomask.

The core of the mask is a multi-layer Bragg mirror composed of around 40 alternative Mo/Si layers which helps to reflect the light generated from the excited electrons from the tin droplet [14]. With a photomask, the pattern is transferred to the wafer with the help of an absorber layer. The current standard for the absorber layer is a tantalum-based material which blocks the pattern in specific areas [15]. With the combination of the absorber layer and areas without an absorber layer, a pattern can be created on photomask that will then be transferred to the silicon wafer. The last component of the photomask is a protective capping layer that keeps the photomask free from damage and in good overall shape. Table 2 shows the necessary criteria that must be met in selecting a capping layer [16].

Table 2: Capping Layer Criteria [16]

Requirement	Specifics
Optical property	High EUV reflectivity
Structural property	Oxidation resistance
Durability	Stable in H_2 plasma
	Stable in clean condition
Mask process	High etch selectivity

Due to its many favorable properties, a ruthenium based capping layer is the most common in EUV although there is still active research in testing alternative forms of ruthenium based layers: pure Ru, doped Ru materials, etc. [16]. All of these components make up a EUV photomask, and each one plays an important role.

Defects on the photomask can lead to a variety of different problems such as CD uniformity issues and reduced process windows so they must be avoided/corrected as much as possible. The most common EUV photomask defects are phase defects, stochastic defects, absorber defects, and particles. The easiest method to remove loose particles is by using dry, filtered N_2 gas although embedded defects need more sophisticated techniques through photomask repair.

Despite the careful preservation of the photomasks, they occasionally need to be repaired. The most common reasons for this are defects in the absorber layer or in the mirror itself. Zeiss is the major company that repairs these photomasks using their MeRiT mask repair technology. This particular technology employs a technique called gas-assisted, electron beam lithography. Through this technique, a gas is introduced into the area followed by a low energy electron beam that initiates a chemical reaction. Depending on the material, this chemical reaction will either deposit new material or etch away defective material to repair the photomask [17].

Since defect control is a huge issue for EUV photomasks, something to protect the photomask is necessary. Despite having the ruthenium capping layer on the photomask itself, this layer actually only protects the surface of the photomask from chemical degradation and

provides no protection from physical contamination such as particles. This is where pellicles come into play. Pellicles are thin, highly transparent membranes that sit above the photomask and prevent particles from contacting the mask. During exposure, the pellicle is out of focus from the scanner so even if there were a few particles on it, then there would be no affect to the pattern printed on the wafer [18]. If the pellicle gets too dirty, they can quickly be replaced, and this is easier and less expensive than letting defects build up on the photomask. Without a pellicle, the amount of time needed to ensure that the mask is clean would be excessive and the photomask repairing process can be costly.

Photoresists for EUV

Photoresists in the semiconductor industry are light-sensitive polymers that are used to transfer patterns onto silicon wafers. For an EUV application, photoresists are typically ~40-60 nm which are crucial to maintain pattern collapse as well as provide a uniform expose on the wafer. Because EUV light is strongly absorbed, there must be a very thin photoresist layer so that the light can pass through the entire thickness. If the photoresist layer is too thick, then there is potential for underexposure towards the bottom of the photoresist.

There are two different working mechanisms of photoresists: positive and negative photoresists. In positive photoresists, a pattern will be left on the wafer in spots where light was absent while the opposite is true for negative. Despite sounding rather simple, these mechanisms bring rise to cost and large performance differences.

Currently, positive photoresists are much more common in the industry when compared to negative photoresists although that hasn't always been the case. Back in the1970s, negative resists were more prominent in the industry due to the excessive cost and poor adhesion properties of positive resists[19]. Despite their performance benefits, device sizes back then were so large that these types of resists were considered to be unnecessary. As device sizes continued to shrink, as proposed by Moore's Law, the performance benefits of positive resist started to greatly unweigh its drawbacks. Positive photoresists offer better performance from superior resolution, high contrast, enhanced etch resistance, absence of swelling behavior during development, better edge resolution, and improved structural aspect ratios. For these reasons,

positive photoresists are seemingly preferred for EUV applications although negative resists can still be used in applications where a higher etching resistance is necessary.

In addition to positive and negative photoresists, there are both organic and inorganic compound photoresists. These types of photoresist materials are both greatly used in EUV lithography with each being highly application based due to their unique characteristics[20]. Table 2 describes a few specific types of organic and inorganic photoresists along with their principle and processing challenges. Chemical Amplified Resists (CARs), inorganic EUV photoresists, non-chemical amplified resists, and hybrid EUV photoresists will all be explained in great detail. As can be seen, from the two difference working mechanisms of photoresists along with their different types, there is a lot to consider before choosing one for a specific application.

Table 3: Types of Extreme UV Photoresist Materials [20]

	Principle	Resolution Potential	Design and Optimization	Processing Challenges
Chemical Amplified Resist (CAR)	Photoacid generator absorbs the energy and undergoes a photolysis reaction	CARs have been developed to achieve sub-10nm resolution	PAG releases acid upon exposure to light, initiating the acid-catalyzed reactions	• Pattern collapse • Line-edge roughness • Stochastic effects
Inorganic EUV Photoresists	Inorganic materials absorb the energy to trigger direct chemical changes which in turn alter solubility (ex: ligand removal, cross-linking, etc.)	Inorganic EUV Photoresists can achieve high-resolution capabilities below 20nm	It converts the incoming EUV photons into the necessary energy for the desired photochemical or physical reactions	• Etch resistance • Sensitivity and dose requirements • Thermal stability
Non-chemical Amplified Resists	NCARs use mechanisms like cross-linking or phase changes to alter its solubility properties	Non-chemical Amplified Resists are considered for sub-20nm resolution	It undergoes physical changes upon exposure, leading to the desired pattern formation	• Resolution • Sensitivity • Contrast and latent image formation
Hybrid EUV Photoresists	Combination of both organic and inorganic	Hybrid EUV Photoresists can achieve resolution under sub-10nm	Optimizing the ratio of components, compatibility between	• Adhesion • Compatibility • Pattern transfer

	materials to enhance lithographic performance		both materials, and interactions	

Before choosing a photoresist, it is vital to first consider the three different factors and their impact on lithography: resolution, line edge/width roughness (LER/LWR), and sensitivity; Table 3 provides a definition for each factor.

Table 4: Lithographic Factors and their definitions

Factors	**Definition (Lithography)**
Resolution	The minimum feature size that a system can reliably print
Line Edge/Width Roughness (LER/LWR)	Critical variations in the edge and width positions of printed features (aims to quantify the precision of the edges feature aka how far it deviates from being an ideal straight line)
Sensitivity	The minimum exposure dose needed in order to properly expose a photoresist

These three factors make up the pillars of what is called the RLS triangle and represents the important tradeoff that must be made in lithography: improving any two parameters often sacrifices the third [21]. Figure 9 provides a visual representation of the RLS triangle with its tips representing the best possible outcome for each pillar. Clearly, in a perfect world, the best way to improve all three simultaneously is to merely make the RLS triangle larger. The center of the triangle is important as it signifies average, balanced performance for each pillar; this can seem optimum at first although semiconductor manufacturing isn't usually this black and white. In

reality, one or two of the pillars need to be prioritized over the other due to their greater importance. Despite this, moving any pillar(s) towards the edge(s) of the triangle will cause the others to go in the opposite direction. Increasing sensitivity may help to fully expose the photoresist, but this creates rougher edges and increases the minimum feature size. Considering this tradeoff, it is important to operate in the RLS triangle where needed and as efficiently as possible since this will ultimately lead to the best patterning. Many strategies have been tested with the goal of optimizing or lessening this RLS trade-off although nothing can completely eliminate it.

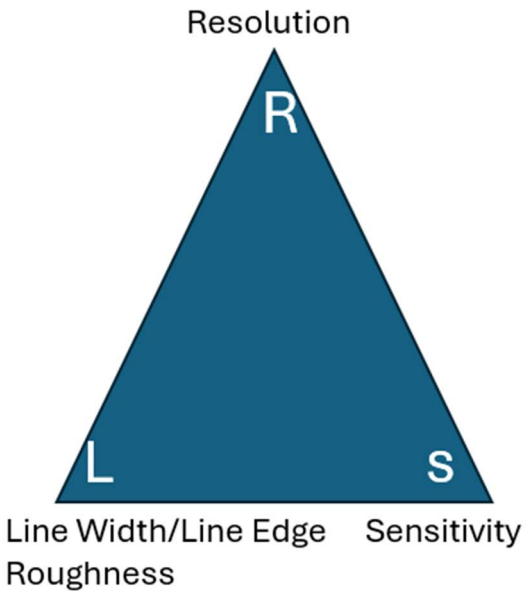

Figure 9: RLS triangle

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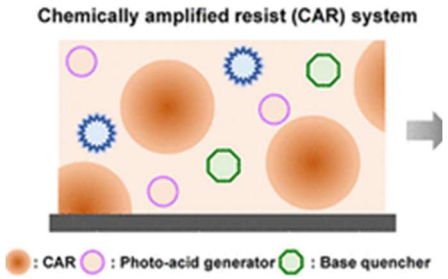

Figure 10: Visual representation of CAR System [22]

In EUV lithography, there are three major types of organic photoresists: chemically amplified resists (CARs), photosensitized chemically amplified resists (PSCARs), and non-chemical amplified resists (n-CARs), one major type of inorganic photoresist: metal-oxide photoresists (MORs), and a hybrid photoresist.

Chemically amplified resists are the most widely used organic photoresists in the EUV space; They are also very common for DUV lithography. CARs, made of organic compounds, consist of four different components: a polymer resin, a photoacid generator, a base quencher, and a solvent (see figure 10) [22]. CARs work by using radiation from DUV or EUV light to decompose a photoacid generator which produces strong acid in exposed regions.

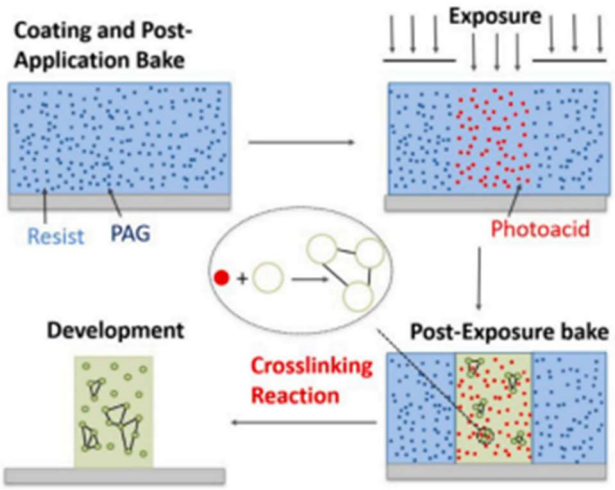

Figure 11: Lithographic process for negative CARs [23]

Figure 11 above provides a great visual representation of the photolithography process for chemically amplified resists [23]. In the first step, the photoresist is coated onto the silicon wafer and then baked in order to evaporate any solvents still left on the wafer as well as hardening the resist so that it doesn't stick to the photomask during exposure. Once baked, wafer is exposed to light which chemically alters the photoresist and breaks down the PAGs in exposed areas. After exposure, this resist then gets baked at a fairly high temperature where the acid acts as a catalyst for chemical reactions to occur causing the solubility of the polymer to change significantly through the dissociation of the polymer cross-linking. This change in solubility is crucial for lithography as a difference in photoresist solubility across the wafer helps to develop the pattern that is needed. For the most part, CARs are the primary resist in EUV lithography although there are significant downsides. Despite offering high sensitivity, chemically amplified resists have issues satisfying the RLS triangle by commonly making a significant sacrifice on one of the pillars.

Photosensitized chemically amplified resists (PSCARs) is one approach to tackle the RLS triangle. PSCARs are similar to CARs although they introduce a second, much lower energy UV exposure post the initial one as shown in figure 12[24]. This second UV exposure enhances the production of overall photoacid generators through the use of photosensitizers. Using this approach, resolution, line width roughness, and sensitivity can all be improved leading to fewer tradeoffs [25].

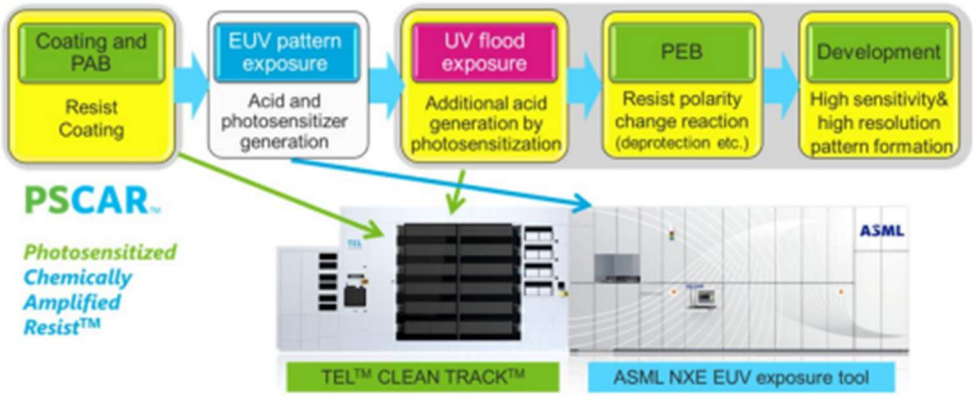

Figure 12: Process flow of PSCARs [24]

Non-chemical amplified resists differ from CARs and PSCARs due to not having to rely on acid-catalyzed reactions. Instead, they directly undergo a photolytic reaction upon EUV exposure resulting in a change in solubility. They require a larger dose of EUV light in order to fully pattern a wafer although they tend to fare better in terms of resolutions and LER/LWR so it certainly has its use cases.

Inorganic photoresist is the other major type of EUV photoresist with metal-oxide based materials being the most common. Metal-oxide resists (MORs) are a fairly new advancement in the EUV space developed to further minimize the tradeoff of the RLS triangle in addition to

PSCARs. MORs are favorable for smaller node technologies because they have higher EUV light absorption which in turn reduces the line width roughness and improves the sensitivity [26]. The corresponding resolution on the wafer isn't affected at all leading to a less harsh trade off. To date, tin or zin oxides have been the most common materials to use for this purpose. Another advantage of these resists is that these metal-oxide resists have better etching resistance. They are more robust than organic photoresist, potentially avoiding the need for separate hard mask deposition steps.

Hybrid EUV photoresists contain both organic and inorganic materials aimed at enhancing lithographic performance. In concept, this sounds like a highly promising candidate which can seemingly satisfy both to an extent. Its inorganic components help to improve sensitivity as their absorption at the EUV wavelength is higher while its organic components allow for the resist increased mechanical strength, making them less susceptible to pattern collapse[27]. Currently, the compatibility and overall adhesion of the photoresist to the wafer is problematic which limits its applications right now.

Technical Challenges in EUV Lithography

Despite the overwhelming benefits of EUV Lithography, there remain a few technical challenges that limit its overall manufacturability. Firstly, the equipment itself is highly complex with all of the new state-of-the-art technologies. This complexity makes the tools difficult to produce which in turn make them very expensive to manufacture. Currently, only ASML manufactures EUV machines. Consequently, the price of the EUV scanners is completely controlled by them. In 2026, the baseline EUV machines are around $220 million while the next-generation high-NA EUV machines can push $400 million [11]. These next-generation machines help to push the boundaries for advanced semiconductor manufacturing, so the market is gigantic. There have been a few other companies that are trying to create their own EUV machines or reverse engineer ASML's unit although it has been quite difficult. Until others take ASML's lead to develop EUV lithography tools of their own, as well as, more efficient manufacturing techniques are found, production difficulties and cost will continue to be a great technical challenge and a roadblock to manufacturability.

Power scaling issues is another key technical challenge that is currently hindering the feasibility of EUV machines. One problem regarding power scaling is the low conversion efficiency. Currently only around 6-7% of the CO_2 plasma is generated into photons that emit the necessary 13.5nm light with the rest turning into heat energy that must be dissipated. Further improvement of the process can help to increase this conversion efficiency. The low efficiency is due to the optics reflective native caused by significant losses from the Bragg mirror. Process

improvement in reducing the number of overall Bragg mirrors needed or increasing the reflectivity of each individual Mo/Si pair is crucial for increasing overall conversion efficiency.

Although other methods have been investigated, thermal treatment is a promising candidate for helping to increase the reflectivity of each Mo/Si pair in the Bragg mirror primarily due to modifying the interface composition along with smoothing it [28], [29].

Defects are another big technical challenge in EUV Lithography. Of course, complete elimination of all defects is preferred although that isn't feasible, so defect reduction is pursued. Mirror defects, mask defects and stochastic defects are the major nuisances. For mirror defects, these can come from many different sources although the most common one is contamination from tin particles. These particles coat the Bragg mirrors which in turn degrade their overall efficiency. Finding a way to minimize these defects and keep the mirrors clean can be beneficial from an efficiency standpoint. There is an active US Patent that aims to prevent tin contaminants in an EUV Lithography system with a passivation coating and a gettering agent [30]. The passivation coating is the first line of defense and helps to prevent the tin from adhering to the EUV collector mirrors while the gettering agent eliminates any tin particles from the outside of the mirrors. When considering a passivation coating, it is important to not only select a material that doesn't adhere very well to tin, but it is also crucial that the material also doesn't affect the reflectivity of the mirrors. Molybdenum oxide (MoOx) is one passivation coating that was employed due to its favorable properties. The gettering agent, on the other hand, should be a material that reacts strongly with tin such as copper, nickel, and ruthenium.[31].

The main mask defects are phase defects and amplitude defects. Phase defects, as shown in figure 13, occur through the introduction of particles into the photomask which then become bumps or pits that deform the multilayer. This causes less than ideal reflection characteristics on the Bragg mirrors reducing the amount of EUV light generated.

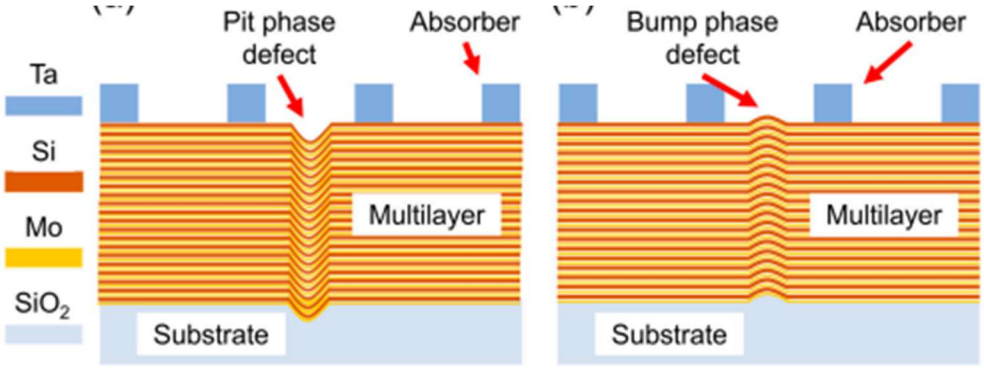

Figure 13: Illustrations of phase defects [32]

Amplitude defects also occur through the introduction of particles into the photomask although instead lead to a bad pattern from the given light. With these defects, a localized intensity change can occur leading to variations in the printed image. Typically, these defects can blur images on the wafer or reduce the edge contrast needed for the proper inspection further down the line. Figure 14 shows how phase and amplitude defects can affect what the photomask is transferring onto the wafer given its reference image. With phase defects, the image changes significantly with even a small change in focus and is not seen in the reference group. This not only limits the overall process window, but it also can cause the feature to be entirely different, which is undesirable.

With amplitude defects on the other hand, there is a clear change in light intensity at the photomask. This can be seen on the silicon wafer through areas of under/over exposure which can alter the CD uniformity and pattern fidelity.

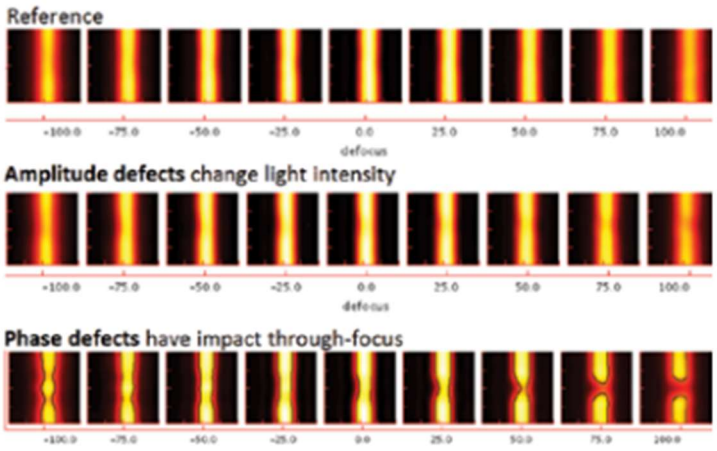

Figure 14: EUV mask line comparison imaged through focus [33]

Stochastic defects represent a very large class of other defects that can be generated during the EUV lithographic process. Unlike the previously described defects, stochastic defects can never be completely eliminated due to their inherently random nature in the process, hence the word stochastic. That being said, there are still a few things that engineers can do in order to mitigate them as best as they can. Within this broad term of defects, photon shot noise is the most common one that has been actively worked on.

Photon shot noise has always been a problem in lithography although it has become more severe recently due to the decreasing node sizes that drive further improvement and therefore, a drive for more power. Using EUV techniques, the energy generated by these EUV photons is exponentially greater than those generated during DUV techniques. Since these photons need

more energy, there will be less of them overall in the EUV system [34]. With fewer overall photons, there is bound to be more statistical variation of these photons and their adsorption rates, particularly in their energy levels, leading to random defects. Equation 2 estimates the probability of detecting “n” photons for a given volume (also known as the Poisson distribution); In the equation, the volume (CV) and amount of photons “n” must be known. Through this, engineers can get a rough estimate of the statistical variation at hand.

$$\boldsymbol{P(n) = \frac{(CV)^n}{n!} * e^{-CV}}$$

Equation 2: Probability of detecting "n" photons in a volume [35]

Equation 3 is a basic, but important equation used to quantitatively calculate the photon shot noise from the square root of the mean number (signal) of generated photons. Common problems that arise as a result of photon shot noise include microbridges, line break, and via failures.

$$\boldsymbol{Shot\ Noise = \sqrt{Signal}}$$

Equation 3: Shot Noise [36]

Equation 4 calculates the relative uncertainty in the number of molecules for a given volume. This term is inversely proportional to the square root of the average number of photons which can also be useful for quantifying photon shot noise. Equations 2, 3, and 4 all signify ways

that one can quantify the photon shot noise and potentially draw a comparison between EUV and DUV Lithography techniques.

$$\sigma = \frac{1}{\sqrt{CV}}$$

Equation 4: Relative uncertainty in the number of molecules in a volume [35]

Given phase, amplitude, and stochastic defects, it's crucial to be able to properly detect them so that we can identify, minimize, and make decisions based on them.

Industrial Adoption and Applications

Due to its high cost and fairly limited manufacturability, the industrial adoption of EUV lithography is currently limited. Only the most advanced applications right now, such as in the advanced logic and memory chip space, are utilizing this technology. Apple silicon, specialized AI chips, and DRAM/NAND memory are all current applications in this field due to their need for smaller chip sizes. This need is driven by further innovation so that companies can deliver even higher performing devices while also making them smaller. Apple, TSMC, Samsung, Intel, Nvidia, and Micron are a few large companies that have adopted EUV lithography as part of their semiconductor flow.

There are a few companies on the horizon that are hoping to also garner EUV lithographic capabilities sometime in the near future so that ASML can be rivaled. Nikon, another giant in the lithography industry, as well various smaller Chinese companies are looking into developing EUV-capable tools of their own so that they can take some market share for themselves/develop domestic capabilities.

Recent Advances and Research Directions

Even though EUV lithography is still in its early phases of use, the innovation never stops in the semiconductor industry so it's always ever-changing. Since its inception in the high-volume manufacturing space in 2019, there have been several advances to either improve the existing EUV technology or to push the boundaries of sub-7nm nodes even further.

First, both photoresist materials and mechanisms have been improved. A new development called resistless lithography has come into the horizon which completely eliminates the use of photoresist in the process through direct patterning on partially H-terminated Si[37]. Although still in its early research phases, resistless lithography could potentially pave the way for further transistor downscaling through the elimination of photoresist limitations, higher precision, and the removal of chemical processing and cleaning steps[37].

The low efficiency and high cost of EUV's light generation process has created a need for alternative sources to generate EUV light such as discharged-produced plasma, High-harmonic generation, and free-electron laser.

Discharged-produced plasma (DPP) is an older, but potential source of EUV energy that is more affordable although isn't really feasible for high volume manufacturing (HVM)

presently. This process uses high power electrical currents to rapidly heat a material that in turn produces light at a wavelength of 13.5nm. There has been a bit of investigation into DPP and how it might be feasible in the HVM space. Both xenon and tin materials were investigated although only tin seemed to be a HVM viable option [38]. When using xenon as a source material, the conversion efficiency was only around 0.5% meaning that the input power must be at 200kW in order to meet HVM requirements which is way too large. Tin on the other hand was able to achieve a conversion efficiency of around 2% which, while not great, is much more feasible.

High-harmonic generation (HHG) is another alternative EUV light generation technique. In this technique, a femtosecond laser is focused on an argon-filled gas cell. The result of these outputs is an EUV beam that can then be used as a light source. This is a great technique for metrology, but is currently too weak for photolithography [39].

Free-electron laser (FEL) has been arguably the most promising option right now to replace LPP as the light source for EUV lithography. The process begins when an electron gun (injector) injects a beam of free electrons into a very long and cryogenically chilled tube called the accelerated beam. Superconductors transmit RF signals that speed up the movement of electrons infinitely fast through the main linear accelerator (LINAC) until they make a 180-degree turn where they enter a region filled with opposite oriented magnets called a magnetic undulator. As the electrons continue to move, the magnets guide their path sinusoidally which causes the electrons to emit light through the free-electron laser. These spent electrons then loop back around in the LINAC through the recirculating beam until the decelerated beam eventually

diverts and then stops their movement into a block of material all while new electrons get injected (figure 15). This light contains a wavelength of 13.5 nm and can theoretically be used for EUV lithography [40].

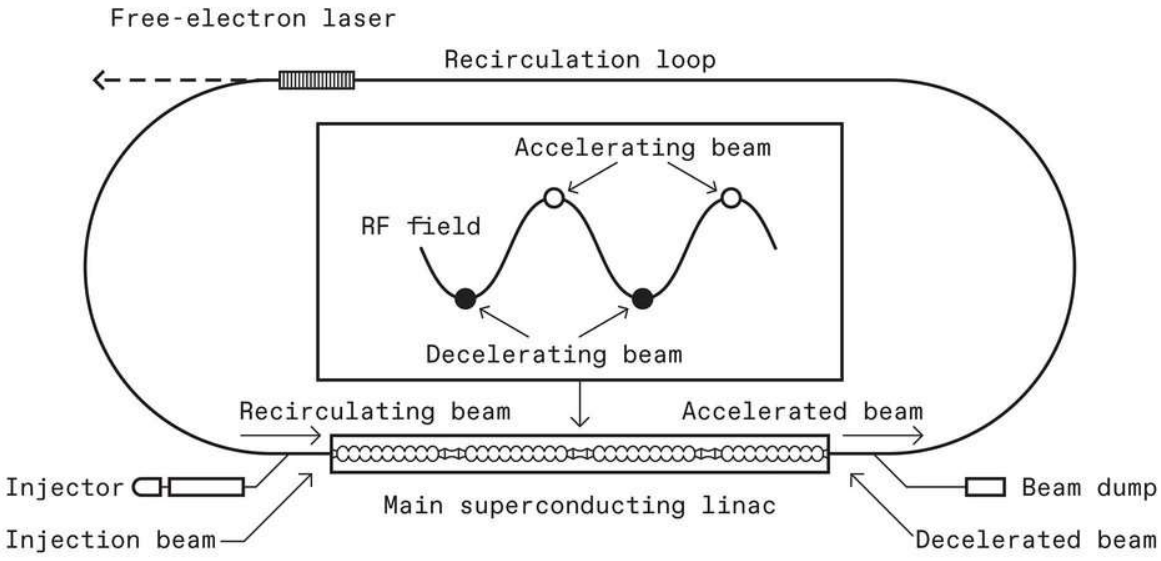

Figure 15: Diagram of a Linear Accelerator (LINAC) [40]

The great benefit of this particular light source is that it is much more efficient than the conventional LPP method. Higher efficiency, of course, in turn means that it can lower overall operating costs of a EUV lithography machine which is vital for supporting high volume manufacturing.

Despite EUV lithography still being in its infant stages, there is already an even more advanced next-generation technology called High-NA EUV lithography that was first installed commercially in 2024. Looking back at the Rayleigh criterion, the minimum resolvable feature size is a function of the k_1 factor, the wavelength of light, and the numerical aperture. ASML

employed a method of increasing the numerical aperture from 0.33 all the way to 0.55 without affecting the other variables which is how they were able to now provide CDs for nodes <2nm [41].

Numerical aperture is the ability for an optical system to collect and focus light. By increasing this ability, ASML was able to provide their tools with a better resolution directly attributing to the possibility for these smaller feature sizes. At first, it might seem simple to make the NA larger although it can be quite complex. ASML ended up implementing bigger mirrors in their system which enabled this higher numerical aperture but came with drawbacks. With bigger mirrors, the angle at which light hits the reticle increases, leading to a loss in reflectivity and preventing the patterns transfer to the wafer. Merely shrinking the pattern on the wafer from 4x to 8x solves this problem, although that came at the expense of having to create larger reticles.

Instead of creating larger reticles, ASML employed their next-generation innovation by avoiding this problem through the use of anamorphic optics. In anamorphic optics, there was a demagnification from 4x to 8x in the scanning direction while the orthogonal direction stayed at 4x[42].

The use of artificial intelligence (AI) and machine learning (ML) have been eyed as a key opportunity to improve process control as well as improving overall manufacturability due to decreasing cycle time. In general, CD becomes harder to control as the k1 factor decreases due to

the smaller allowable overall process window. This process window is affected by features of small size which creates a much higher sensitivity to potential variations in the process such as chemical fluctuations, contamination, defects, etc.

The use of this up-and-coming technology allows the system to best optimize the process in two major ways. First, statistically driven AI algorithms help to optimize critical parameters associated with the lithography process such as dose control, focus consistency, and pattern overlay accuracy. Through these methods, the RLS trade-off talked about in an earlier section can be managed easier [43]. Secondly, the use of AI can help when it comes to the recognition of defects on the wafers which can help to spot trends or problems before they become too big.

Future Possibilities

EUV Lithography is overall a very powerful tool that can help push the semiconductor industry further along its journey to make transistors smaller and smaller. Like everything, this technology doesn't come without its downsides. Firstly, the cost of having EUV Lithography as a part of the manufacturing process is still quite high. The complexity of the EUV machines makes them hard to manufacture, which in turn drives up the cost. Moreover, the lack of competition gives ASML a monopoly on the EUV market, therefore, eliminating any level of healthy competition. Lastly, there is still a high operating cost of using these tools driven by its high energy requirement due to the low overall process efficiency.

Having a low energy conversion rate also makes EUV unfavorable when it comes to a throughput standpoint because the time required to generate energy can be much greater when compared to DUV machines. Until the conversion rate is brought up or further process improvement occurs, this process will continue to be the bottleneck of the fab. In a similar vein, due to the complexity of the tools, more maintenance is needed on the systems which might require specific personnel to perform the work further, leading to more downtime.

Unrelated to the EUV Lithography tools, the nature of printing smaller CDs leads to greater difficulty in controlling CDs and managing defects. Lastly, the RLS triangle becomes more severe which pushes harsher trade-offs between resolution, line edge/width roughness (LER/LWR), and sensitivity. Through further innovation, many of these EUV lithography growing pains can be minimized.

There is a lot of research going on regarding potential advancements to any aspect of EUV Lithography from the tool itself to an aspect of the process. Improved resist materials, alternative EUV sources, the emergence of high NA EUV Lithography, and AI assistance are all areas that could significantly make the process cheaper, more efficient, or capable of patterning even smaller features. Currently, EUV Lithography isn't utilized in much of the semiconductor industry due to its cost and inability to thrive in a high-volume manufacturing environment. That being said, companies that require sub-7nm node technologies have no choice but to accept EUV's current flaws. With EUV Lithography still being in its infant stages, its long-term impact is still relatively unknown although it has the potential to do great things. Once more EUV manufacturers come into the business, as well as a few of the recent advances get implemented, EUV technology can solidify itself as not only an advancement in transistor size, but also without the sacrifice of extreme costs or high-volume manufacturing.

Conclusion

Despite researchers initially thinking that sub-7nm chip sizes were practically impossible, it's amazing what a deep understanding of the previous generation's technology (DUV) could do. Combined with curiosity and motivation, this everlasting need to maintain the pace of transistor miniaturization gave way to the creation of EUV lithography through the means of an entirely different system architecture along with process fundamentals necessary to create light with a wavelength of 13.5nm. The goal of this report was to continue spurring lithographic innovation by providing a wholistic understanding of EUV lithography. For EUV, industrial adoption has been somewhat limited to the advanced logic and memory chips space due to expensive baseline processes and its inability to support high-volume manufacturing. Although in this space, deeper lithographic innovation is already underway with the recent creation of High-NA EUV which has now shrunk node sizes to <2 nm.

It has become evident that smaller companies in the advanced logic and memory chips space or players in the mature nodes market have been left behind on EUV in favor of its cheaper and more manufacturable counterpart: DUV lithography. As a result, they have been limited to node sizes ~28nm. Although a path for further lithographic innovation in advanced sectors is clearly there, with High-NA EUV for example, something that was implied from research is that basic EUV is not going to sunset anytime soon, like some literature reviews state, but rather will expand into less sophisticated sectors of the semiconductor market. Through general

improvements in EUV such as advances in photoresist technology, light generation technology, and reflectivity, the process can become more efficient, affordable, and HVM friendly which is exactly what these more mature nodes need before implanting them in their factories. Even though companies who sell more mature nodes aren't necessarily the ones who care about the industry's cutting-edge lithographic innovations, they themselves still benefit from and heavily utilize smaller nodes when possible as this can lead to lower production costs per unit. In conclusion, the future of EUV lithography is beyond bright for both advanced and mature players. For advanced players in the industry, miniaturization continues through improvements in EUV such as high-NA while for more mature players, EUV can move from being a nice-to-have in the semiconductor industry to setting the new "gold standard" as DUV lithography starts to fade out.

References

[1] “The underestimated size of the semiconductor Industry | McKinsey.” Accessed: Mar. 09, 2026. [Online]. Available: https://www.mckinsey.com/industries/semiconductors/our-insights/hiding-in-plain-sight-the-underestimated-size-of-the-semiconductor-industry

[2] A. R. Hatfield and A.-H. A. Badawy, “Moore’s Law: What Comes Next?,” in *Software Engineering Research and Practice and e-Learning, e-Business, Enterprise Information Systems, and e-Government*, H. R. Arabnia and L. Deligiannidis, Eds., Cham: Springer Nature Switzerland, 2025, pp. 195–206. doi: 10.1007/978-3-031-86644-9_15.

[3] G. D. Hutcheson, “Moore’s law, lithography, and how optics drive the semiconductor industry,” in *Extreme Ultraviolet (EUV) Lithography IX*, SPIE, Mar. 2018, p. 1058303. doi: 10.1117/12.2308299.

[4] H. Sewell, A. Chen, J. Finders, and M. Dusa, “Progress in Extending Immersion Lithography for the 32 nm Node and Beyond,” *Jpn. J. Appl. Phys.*, vol. 48, no. 6S, p. 06FA01, Jun. 2009, doi: 10.1143/JJAP.48.06FA01.

[5] “What is the Rayleigh criterion?,” ASML. Accessed: Mar. 09, 2026. [Online]. Available: https://www.asml.com/en/technology/lithography-principles/rayleigh-criterion

[6] O. O. Versolato, “Physics of laser-driven tin plasma sources of EUV radiation for nanolithography,” *Plasma Sources Sci. Technol.*, vol. 28, no. 8, p. 083001, Aug. 2019, doi: 10.1088/1361-6595/ab3302.

[7] “ASML EUV lithography systems,” ASML. Accessed: Mar. 09, 2026. [Online]. Available: https://www.asml.com/en/products/euv-lithography-systems

[8] Y. Mostafa *et al.*, “Production of 13.5 nm light with 5% conversion efficiency from 2 μm laser-driven tin microdroplet plasma,” *Appl. Phys. Lett.*, vol. 123, no. 23, p. 234101, Dec. 2023, doi: 10.1063/5.0174149.

[9] “Analyst firm raises alarm about EUV chipmaking tools — each consumes as much power as a small city, fabs to consume 54,000 Gigawatts by 2030 | Tom’s Hardware.” Accessed: Mar. 09, 2026. [Online]. Available: https://www.tomshardware.com/tech-industry/each-euv-chipmaking-tool-consumes-as-much-power-as-a-small-city-euv-fabs-to-consume-54-000-gigawatts-by-2030-more-than-singapore

[10] “EUV lithography and technology | ZEISS SMT.” Accessed: Mar. 09, 2026. [Online]. Available: https://www.zeiss.com/semiconductor-manufacturing-technology/inspiring-technology/euv-lithography.html
[11] K. Tarasov, “Exclusive look at the creation of High NA, ASML’s new $400 million chipmaking colossus,” CNBC. Accessed: Mar. 23, 2026. [Online]. Available: https://www.cnbc.com/2025/05/22/exclusive-look-at-high-na-asmls-new-400-million-chipmaking-colossus.html
[12] S. B. Hill, C. Tarrio, R. F. Berg, and T. B. Lucatorto, “EUV-induced carbon growth at contaminant pressures between 10−10 mbar and 10−6 mbar: Experiment and model,” *J. Vac. Sci. Technol. Vac. Surf. Films Off. J. Am. Vac. Soc.*, vol. 38, no. 6, p. 10.1116/6.0000437, Dec. 2020, doi: 10.1116/6.0000437.
[13] W. Shen, Q. Lu, Y. Song, X. Gong, K. Chai, and S. Li, “Study on tin contamination deposition mechanism on collector mirror surfaces in LPP-EUV light sources based on hydrodynamics and particle simulation theory,” *Vacuum*, vol. 233, p. 114024, Mar. 2025, doi: 10.1016/j.vacuum.2025.114024.
[14] Y. Hao *et al.*, “Impact of EUV multilayer mask defects on imaging performance and its correction methods,” in *International Conference on Extreme Ultraviolet Lithography 2019*, SPIE, Sep. 2019, pp. 142–155. doi: 10.1117/12.2536707.
[15] H. Nakano, D. Miyawaki, Y. Hasegawa, I. Yoshida, K. Seki, and Y. Kojima, “Development of mask absorbers for next generation EUV lithography,” in *Optical and EUV Nanolithography XXXVIII*, SPIE, Apr. 2025, pp. 503–507. doi: 10.1117/12.3050948.
[16] C.-H. Wang *et al.*, “Novel capping layer evaluation for EUV mask,” in *Photomask Technology 2025*, SPIE, Nov. 2025, pp. 45–54. doi: 10.1117/12.3071741.
[17] “Mask Repair Solutions by ZEISS SMT.” Accessed: Mar. 09, 2026. [Online]. Available: https://www.zeiss.com/semiconductor-manufacturing-technology/products/photomask-solutions/mask-repair.html
[18] Y.-Y. Lin *et al.*, “EUV pellicle technology for high volume wafer production,” in *International Conference on Extreme Ultraviolet Lithography 2023*, SPIE, Nov. 2023, pp. 184–189. doi: 10.1117/12.2688127.

[19] M. Hassaan, U. Saleem, A. Singh, A. J. Haque, and K. Wang, “Recent Advances in Positive Photoresists: Mechanisms and Fabrication,” *Materials*, vol. 17, no. 11, p. 2552, May 2024, doi: 10.3390/ma17112552.

[20] manageCore_wp, “Advancing Semiconductors with Novel Extreme UV Photoresist Materials,” Ingenious-e-Brain. Accessed: Mar. 30, 2026. [Online]. Available: https://www.iebrain.com/advancing-semiconductor-processing-with-novel-extreme-uv-photoresist-materials/

[21] J. Deng, S. Bailey, S. Jiang, and C. K. Ober, “Modular Synthesis of Phthalaldehyde Derivatives Enabling Access to Photoacid Generator-Bound Self-Immolative Polymer Resists with Next-Generation Photolithographic Properties,” *J. Am. Chem. Soc.*, vol. 144, no. 42, pp. 19508–19520, Oct. 2022, doi: 10.1021/jacs.2c08202.

[22] Y. Ku *et al.*, “Positive Role of Iodine Atoms in Chemically Amplified Photoresists for Extreme Ultraviolet Lithography,” *ACS Appl. Mater. Interfaces*, vol. 17, no. 52, pp. 70920–70931, Dec. 2025, doi: 10.1021/acsami.5c22668.

[23] Z. Hu, K. Cao, and T. Yan, “Photoacid diffusion in chemically amplified photoresists and its detection methods: A review,” *Micro Nano Eng.*, vol. 30, p. 100347, Mar. 2026, doi: 10.1016/j.mne.2025.100347.

[24] S. Nagahara *et al.*, “Photosensitized Chemically Amplified Resist (PSCAR) 2.0 for high-throughput and high-resolution EUV lithography: dual photosensitization of acid generation and quencher decomposition by flood exposure,” presented at the SPIE Advanced Lithography, C. K. Hohle and R. Gronheid, Eds., San Jose, California, United States, Mar. 2017, p. 101460G. doi: 10.1117/12.2258217.

[25] I. Hossain, “Photosensitized Chemically Amplified Resist (Pscar) For Extreme Ultraviolet Lithography (Euvl),” *Leg. Theses Diss. 2009 - 2024*, Dec. 2023, doi: 10.54014/84EQ-Y032.

[26] M. W. Hasan, L. Deeb, S. Kumaniaev, C. Wei, and K. Wang, “Recent Advances in Metal-Oxide-Based Photoresists for EUV Lithography,” *Micromachines*, vol. 15, no. 9, p. 1122, Aug. 2024, doi: 10.3390/mi15091122.

[27] “Vapor-Phase Infiltrated Organic–Inorganic Positive-Tone Hybrid Photoresist for Extreme UV Lithography.” Accessed: Mar. 30, 2026. [Online]. Available: https://advanced.onlinelibrary.wiley.com/doi/epdf/10.1002/admi.202300420

[28] A. Kloidt *et al.*, “Enhancement of the reflectivity of Mo/Si multilayer x-ray mirrors by thermal treatment,” *Appl. Phys. Lett.*, vol. 58, no. 23, pp. 2601–2603, Jun. 1991, doi: 10.1063/1.104835.

[29] M. Rovezzi *et al.*, “Characterization of thermally treated Mo/Si multilayer mirrors with standing wave-assisted EXAFS,” *Nucl. Instrum. Methods Phys. Res. Sect. B Beam Interact. Mater. At.*, vol. 246, no. 1, pp. 127–130, May 2006, doi: 10.1016/j.nimb.2005.12.023.

[30] B. J. Rice, M. Fang, P. Barnak, and M. Shell, “(76) Inventors: Robert Bristol, Portland, OR (US);”.

[31] B. J. Rice, M. Fang, P. Barnak, and M. Shell, “(76) Inventors: Robert Bristol, Portland, OR (US);”.

[32] K. He and Z. Zeng, “Impact of Phase Defects on the Aerial Image in High NA Extreme Ultraviolet Lithography,” *Micromachines*, vol. 16, no. 11, p. 1210, Oct. 2025, doi: 10.3390/mi16111210.

[33] E. Gallagher *et al.*, “EUVL mask repair: expanding options with nanomachining,” *Photomask*, vol. 29, no. 3, SPIE, Mar. 2013.

[34] J. M. Hutchinson, “Shot-noise impact on resist roughness in EUV lithography,” in *Emerging Lithographic Technologies II*, SPIE, Jun. 1998, pp. 531–536. doi: 10.1117/12.309612.

[35] C. A. Mack, “Shot noise: a 100-year history, with applications to lithography,” *J. MicroNanolithography MEMS MOEMS*, vol. 17, no. 4, p. 041002, Jul. 2018, doi: 10.1117/1.JMM.17.4.041002.

[36] “What is photon shot noise? | Hamamatsu Photonics.” Accessed: Mar. 10, 2026. [Online]. Available: https://camera.hamamatsu.com/jp/en/learn/technical_information/thechnical_guide/photon_shot_noise.html

[37] L.-T. Tseng *et al.*, “Resistless EUV lithography: Photon-induced oxide patterning on silicon,” *Sci. Adv.*, vol. 9, no. 16, p. eadf5997, Apr. 2023, doi: 10.1126/sciadv.adf5997.

[38] V. Borisov *et al.*, “Discharge produced plasma source for EUV lithography,” in *Laser Optics 2006: High-Power Gas Lasers*, SPIE, Apr. 2007, pp. 79–86. doi: 10.1117/12.740590.

[39] C. Klein *et al.*, “Optimized EUV scatterometry measurements with tunable high harmonic generation and the Fisher information matrix,” in *Metrology, Inspection, and Process Control XXXIX*, SPIE, Apr. 2025, pp. 24–25. doi: 10.1117/12.3051113.

[40] “EUV Light Source: Is the Future in a Particle Accelerator? - IEEE Spectrum.” Accessed: Mar. 10, 2026. [Online]. Available: https://spectrum.ieee.org/euv-fel
[41] “5 things you should know about High NA EUV lithography.” Accessed: Mar. 10, 2026. [Online]. Available: https://www.asml.com/en/news/stories/2024/5-things-high-na-euv
[42] T. Li, Y. Chen, Y. Li, and L. Liu, “Design of a high transmission illumination optics for anamorphic EUV lithography optics using deep reinforcement learning,” *Opt. Express*, vol. 33, no. 2, p. 2261, Jan. 2025, doi: 10.1364/OE.547606.
[43] B. Finlay, M. Faria, S. Gueci, E. Holzer, N. Latham, and F. Ortega, “AI-Powered Process Optimization for EUV MOR: Equipment Trace Data Feature Extraction and Machine Learning is Essential for CD Control,” in *2024 35th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*, May 2024, pp. 1–5. doi: 10.1109/ASMC61125.2024.10545368.