Control and stability enhancement of grid-interactive voltage source inverters under grid abnormalities

by

Aswad Adib

B.Sc., Bangladesh University of Engineering and Technology, Bangladesh, 2012

AN ABSTRACT OF A DISSERTATION

submitted in partial fulfillment of the
requirements for the degree

DOCTOR OF PHILOSOPHY

Department of Electrical and Computer Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2018

Abstract

Voltage source inverters (VSIs) are an essential interface for grid integration of renewable energy resources. Grid-tied VSIs are employed in power grids to integrate distributed generation units, e.g. photovoltaic arrays, wind turbines and energy storage units, to the utility and extract the maximum energy from the DG units in an efficient manner. However, the stability of VSIs and by extension the entire DG system can be degraded under abnormal grid conditions. In this dissertation, new control and switching techniques for stability and power quality improvement of grid-tied VSIs under abnormal grid conditions are presented. For grids with a low inertia and a low short-circuit ratio, commonly referred to as weak grids, grid connection may make VSIs susceptible to voltage distortion and instability. In this dissertation, through root locus analysis of a detailed state-space model, the design of several circuit and control parameters of the grid-tied VSI are evaluated for improving stability in weak grids. It is shown that grid-side filter inductances can be increased for stable operation of VSIs in weak grids. Accordingly, a virtual inductance emulating the effect of an increased inductance in the grid-side filter is developed in this dissertation, which enables stable operation of VSIs in weak grids without the tradeoffs, i.e. additional voltage drop, increased cost and larger size, associated with a larger inductor. The virtual inductance scheme is realized through the injection of a feedforward current element in the VSI controller through a gain component. The measured grid currents, which are sensed for regular VSI controller operation, are employed as the feedforward component eliminating the need for any additional sensors for the utilization of this control scheme. Furthermore, a direct model reference adaptive control (MRAC) scheme is employed in this dissertation to tune the virtual inductance gain block according to a stable reference model for varying grid conditions. The use of direct MRAC scheme allows tuning of the virtual inductance block without the need for a plant parameter estimation stage. The virtual inductance scheme

enables stable operation of VSIs in weak grids without system parameter redesign, thereby maintaining the steady-state performance of the system. The efficacy of the virtual inductance feedforward scheme is verified through hardware tests carried out on a three-phase grid-tied experimental setup. Along with extracting energy from the DG sources, grid-tied VSIs are capable of providing various ancillary services to the utility under abnormal conditions. However, providing ancillary services could drive the inverter voltages beyond the linear modulation region resulting in grid current distortions, which could violate the requirements for grid integration of DGs. An atypical pulse width modulation (PWM) technique is proposed in this dissertation, which maximizes the dc-bus utilization of VSIs, which in turn enables the VSIs to supply the maximum extracted power from the DG units to the grid when providing ancillary services while operating in the linear modulation region. The switching scheme is realized by injecting common mode components in the PWM references, computed based on instantaneous reference magnitudes. The proposed scheme is suitable when providing both symmetrical and asymmetrical ancillary services. In this dissertation, negative-sequence compensation and harmonic compensation are employed as instances of symmetrical and asymmetrical ancillary services. The proposed scheme can be integrated with any control scheme and carrier-based PWM combinations. The efficacy of the proposed atypical PWM scheme is verified through both simulation and hardware tests.

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throughout this whole process. Also, her authentic attitude towards research has always been an inspiration for me.

Dedication

To my parents and my siblings.

Chapter 1

Introduction

The objective of this dissertation is to develop new techniques for improving stability and power quality of grid-tied voltage source inverters (VSIs) under abnormal grid conditions. The motivation and the importance of developing new techniques are outlined in Section 1.1. The state-of-the-art regarding stability and power quality of grid-tied VSIs are discussed, and the possible avenues for improvement in those areas are identified in Section 1.2. The contributions of this dissertation, in developing new control and switching techniques to address some of the shortcomings of the state-of-the-art techniques identified in Section 1.2, are presented in Section 1.3. Finally, the organization of this dissertation is outlined in Section 1.4.

1.1 Motivation and Objectives

Electric power in traditional power systems is generated through large-scale generators, which operate on fossil fuels. The use of fossil fuels has a negative impact on our environment and their quantity is finite, giving rise to renewable energy based resources, e.g. wind, solar and hydro, being integrated into the power systems that have the advantages of being environment-friendly and having an infinite supply. Renewable energy sources require a power electronic (PE) interface to be integrated to the power grid. As the integration of re-

newable resources are becoming more affordable, more PE interfaces are being introduced to the power grid, changing the landscape of the traditional power system. Small-scale renewable energy sources in the distribution side of the power system, in the form of distributed generation (DG) units, e.g. photovoltaic (PV) arrays, wind turbines, and energy storage units, are giving rise to active consumers, which have the capability of supplying power to the utility as well as consuming power when necessary, thus creating a bidirectional flow of power between the utility and the consumer. Therefore, the integration of PE units in the power system is introducing new challenges for power engineers to overcome.

The most essential interface for the integration of DG units to the utility is an inverter, with VSIs being the prevalent option [1–3]. The primary function of an inverter is to convert dc quantities into ac quantities, which is a necessary step for the integration of DG units under most circumstances. For sources such as PVs and energy storage units, the voltage and current these DG units generate are dc quantities. Therefore, to operate these energy sources in conjunction with the ac power grid, an inverter interface is mandatory. Even for a resource such as wind power that generates ac voltages and currents, an energy conversion step consisting of an inverter is necessary due to the stochastic nature of the renewable resources. Specifically for the case of wind energy, as the wind speed fluctuates, the angular speed of the generators connected to the wind turbines also fluctuate, resulting in ac quantities with wild voltage and frequency. With the power grid operating at a fixed standard voltage and frequency, the wind power units cannot be directly connected to the grid. A two-stage conversion process is commonly utilized, where the wild ac quantities are first converted to dc and then converted to ac signals with standard voltage and frequency values using an inverter [1]. Single stage conversion strategies equipped with ac-ac converters can also be found in the literature [4]. The most commonly employed topologies for grid-tied solar, energy storage, and wind DG units are illustrated in Fig. 1.1. It can be seen from Fig. 1.1 that an LCL filter is introduced between the PE interface and the grid, which reduces the high-frequency switching harmonics associated with the PE converters. The grid-tied DG units are also equipped with a control system that fulfills certain objectives, e.g. control of active and reactive power, dc-link voltage control and terminal voltage control, among other

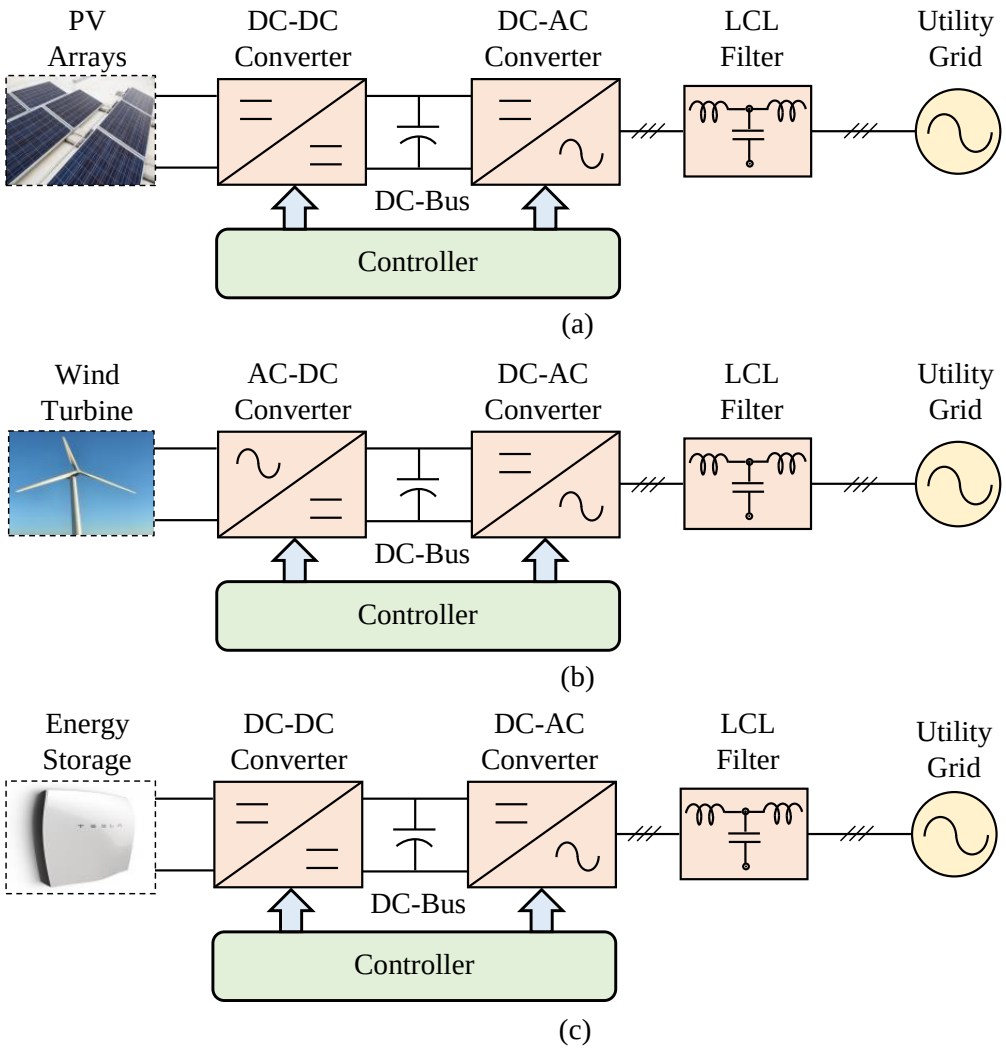


Figure 1.1: *Schematic diagrams of grid-tied DG units powered through (a) PV arrays equipped with DC-DC and DC-AC converter, (b) wind turbines units equipped with AC-DC and DC-AC converter, and (c) battery energy storage equipped with DC-DC and DC-AC converter based PE interfaces.*

things depending on the application.

The DG units primarily provide power to their associated loads, while they could supply power to the utility as well if the generated power is greater than their load demand. The PE interfaces play a vital role in ensuring that the maximum power is being extracted from the DG units under various operating conditions. For solar powered DG units, the maximum power that can be extracted under certain operating conditions, i.e. temperature and solar irradiation, depends on the voltage of the PV array. Several maximum power

point tracking (MPPT) techniques exist for PV systems, which are embedded in the control system illustrated in Fig. 1.1, that manipulate the voltage of the PV arrays to obtain the maximum power [5]. To extract the maximum power output from wind energy systems under varying wind speeds, MPPT techniques exist that adjust the wind turbine generator speed. MPPT techniques that control the dc-link voltage and duty cycle of the PE interfaces to obtain maximum power output from wind-powered DG units can also be found in literature [6]. MPPT schemes are commonly employed in the dc conversion stage of the PE interface, while VSIs equipped with MPPT schemes also exist [7, 8].

The performance of the VSI, when fulfilling its role of being an energy conversion interface for DG units, is heavily dependent upon the grid condition at the point of common coupling (PCC) between the VSI and the electric grid. Abnormal grid conditions could severely distort the VSI waveforms and even make the grid-tied system unstable, which could result in loss of power due to triggering of the safety equipment and potentially damage sensitive loads connected to the system. A form of abnormal grid condition is unbalanced grid voltages at the PCC that could occur due to single-line-to-ground faults [9–11]. Moreover, lower order harmonic components could be present in the grid voltages due to grid connection through large line impedances and the presence of non-linear loads in the distribution grid [12–14]. Both of these phenomena result in distortions in the grid currents. Asymmetrical and non-linear loads connected at the PCC could also cause distorted grid currents. Various compensators can be integrated to the VSI control system to counteract the distortion in the grid currents [10, 15–19], however, this could affect the maximum power the DG unit could provide. This situation will be discussed in detail in this dissertation. An extreme case of grid abnormality is a weak grid, resulting from a large grid impedance associated with the point of grid connection. The grid-tied VSI could become unstable in the presence of a weak grid [3, 20–30]. This is another major topic of discussion in this dissertation. The grid abnormalities considered in this dissertation are illustrated in Fig. 1.2. The negative effects of such abnormalities are also illustrated in Fig. 1.2, which will be discussed in detail in the following subsections.

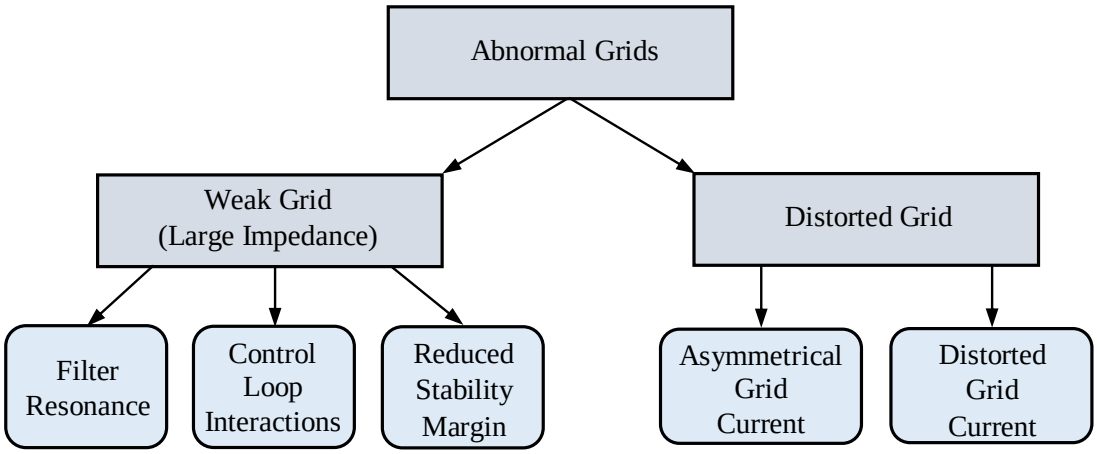


Figure 1.2: *Abnormal grid conditions considered in this dissertation and their impacts.*

1.1.1 Instability in Weak Grids

A weak grid is commonly defined as a power grid with a low short-circuit ratio (SCR), i.e. large impedance, and a low inertia constant (H) [20]. The weak grid phenomenon can be observed in remote or rural areas connected through radial feeder lines [3, 21]. In order to provide grid connection to DG units located in remote areas, the medium voltage transmission lines could be overextended resulting in large inductive grid impedances. The low power step-down transformers could further contribute to the inductive grid impedance. Long distribution lines, typical in radial distribution feeder connections, contribute a predominantly resistive impedance to the total grid impedance [3]. The voltage and frequency at the PCC can be distorted in weak grids due to the large grid impedance.

Instability can occur in a grid-tied system connected to a weak grid if the voltage at the PCC has a harmonic component at the natural frequency of the LCL filter. Small harmonic components in grid voltage could trigger harmonic resonance in the LCL filter under the presence of a large grid impedance and as the grid impedance increases further, the system could become unstable as the stability margin of the system becomes negative [22].

The varying grid impedance in weak grids could lead to undesirable resonance and stability issue for grid-tied VSIs [23, 24]. Voltage feedforward paths, employed in grid-tied VSI control schemes to reduce the response time of the closed-loop system, could make the system

unstable under varying grid impedance in weak grids [23]. Voltage feedforward reduces the stability margin of the closed-loop system in weak grids, thereby deteriorating the stability of the terminal voltage [24].

The interaction between the control systems and grid distortions can also cause instability in weak grids [25–30]. The stability of dc-link voltage control worsens due to the interaction between the control loops in a weak grid [25]. The performance of the phase-locked loop (PLL), employed to synchronize the VSI with the grid, is deteriorated in the presence of large grid impedances, which in turn has a negative impact on the performance of the control loops in weak grids [26, 27]. In [28, 29], the interaction between PLL bandwidth and grid impedance is studied. It is shown that a grid-tied system with a large PLL bandwidth can become unstable in weak grids. A large PLL bandwidth increases the coupling effect between the control loops in grid-tied VSI control schemes, which makes the system more susceptible to instability in the presence of large grid impedances [28]. In addition, the positive feedback gains of anti-islanding methods, which is a mandatory feature of DG units such as PV and battery energy storage, are restricted for stable operation in weak grids as reported in [30].

From the above discussion, it can be concluded that weak grids severely degrade grid-tied inverter stability. The LCL filter resonance issue gets aggravated in the presence of a large grid impedance associated with a weak grid. In addition, the distortion present in weak grids deteriorates the performance of the control schemes present in VSIs. In Section 1.2, the state-of-the-art techniques to tackle the stability issue in weak grids are discussed.

1.1.2 Power Quality Issues when Providing Ancillary Services

Grid-tied VSIs connected to distribution grids could encounter balanced (symmetrical) or unbalanced (asymmetrical) voltage sags, which are a balanced or an unbalanced reduction in voltages, in different phases of the three-phase grid-tied system [9–11]. The grid voltage sag phenomenon arises due to faults occurring in the power system. Faults that result in a symmetrical voltage sag are extremely rare, whereas single-phase-to-ground, two-phases-to-ground, and phase-to-phase faults are more common in the power system, which manifest

as an asymmetrical voltage sag at the terminals of grid-tied DG units [9]. Asymmetrical grid voltages at the terminals result in asymmetrical currents being supplied to the grid. Asymmetrical grid currents could also arise from unbalanced loads present in the distribution grids [12]. The rise of power electronics has also given rise to non-linear loads in the power system as the power electronic devices are non-linear in nature. Diode or thyristor rectifiers, cycloconverters, and arc furnaces are some of the loads that are identified as harmonic producing loads [13]. Due to the presence of grid impedance, harmonic currents drawn by the loads result in distorted supply voltages at the PCC of DG units [14]. Degradation of power quality could cause excessive heating, reduction in efficiency and lifetime of line conductors and grid-tied systems. Therefore, asymmetrical and symmetrical compensation services in the form of negative-sequence compensation and harmonic compensation are necessary for proper operation of grid-tied DG units.

Negative-sequence compensation and harmonic compensation have traditionally been provided through external power conditioning devices such as STATCOMs and active filters [31–34]. Such devices could be utilized to provide compensation services to single DG units or in a distribution system to a group of DG units. However, the power conditioning devices are typically enabled through VSIs, therefore, the VSIs equipped with the DG units could offer the same services [35]. Negative-sequence compensation and harmonic compensation provided through grid-tied VSIs are commonly referred to as ancillary (auxiliary) services, as they are added functionalities the VSIs could provide on top of guaranteeing maximum power extraction from the DG units.

However, providing ancillary services could affect maximum power extraction from the DG units. The inverter voltages are restricted to the linear modulation region of operation by the input dc-bus voltage. As a result, providing ancillary services could drive the inverter voltages beyond the linear modulation to the overmodulation region, which introduces harmonic distortions in the VSI waveforms. For example, providing negative-sequence compensation would require asymmetrical inverter voltage references, which might drive one of the references beyond the linear modulation region even if the DG unit is providing rated power. To avoid power quality issues resulting from operating in the overmodulation region,

the fundamental positive-sequence inverter voltages have to be decreased, which in turn reduces the maximum power the VSIs can extract from the DG units. The state-of-the-art regarding issues related to providing ancillary services is discussed in the following section.

1.2 Literature Review

In this section, firstly, the recently presented techniques in literature to enable stable operation of grid-tied VSIs are discussed. Next, the state-of-the-art regarding the grid-tied VSI ancillary services is presented.

1.2.1 Techniques to Improve Stability in Weak Grids

Three main approaches can be seen to be adopted by researchers to tackle the grid-tied VSI stability issue in weak grids. One set of works focus on different procedures to design existing VSI parameters to ensure stability in weak grids [23, 24, 30]. Another set of researchers propose techniques that require hardware modifications to achieve stable operation in weak grids [26, 36, 37]. Finally, new control (software) techniques are presented in some works to improve grid-tied VSI adaptability in weak grids [21, 29, 38, 39].

In [23], conservative design recommendations for filter and controller parameters are provided for stable operation in weak grids. Depending on the ratio between the resonance frequency of the LCL filter and sampling frequency of the controller, an upper limit for the controller gains are presented. In [24], a feasible region for the controller proportional gains is presented depending on the grid impedance to ensure stable operation in weak grids. In [30], a modified frequency estimation method is proposed that reduces the deleterious effect of PLLs on system stability under weak grids. For the proposed method to work under all operating conditions, the second order PLL characteristics have to be designed so as to attain a critically damped or overdamped response. In all three works, existing controller gains in the control system of grid-tied VSIs have been adjusted to ensure stability in weak grids. However, the control gains are typically chosen to achieve a certain dynamic response

rather than stability. As a result, there is a significant tradeoff between the performance and stability of the system. Moreover, in a practical scenario where a controller commonly consists of cascaded loops [40], controller gains of a particular loop cannot be changed independently of the other loops to avoid interaction among them. Therefore, the allowable limits for alterations in controller gains might be limited and the techniques based on such procedures would not able to ensure stable operation for a wide range of grid impedances.

A second set of methods can be found in literature that employs active damping techniques to improve stability of grid-tied VSIs in weak grids. A resistor in series with the LCL filter capacitor, commonly referred to as a passive damping resistance, can improve the stability of grid-tied VSIs [41]. An additional resistance in the circuit, however, increases the power loss and it also deteriorates the high-frequency harmonic rejection capability of the LCL filters. The principle of active damping techniques is based upon emulating the behavior of the passive damping resistance in the control system. In [26], an active damping strategy based on capacitor current feedback is presented to enable stable operation in weak grids. The proposed scheme requires an additional sensor to measure the current in the capacitor branch, which is not required under normal controller operation. A hybrid damping method combining both passive and active damping techniques is presented in [36], to extend the range of traditional active damping strategies in stabilizing grid-tied VSI operation over a large range of grid impedances. Although a smaller resistor can be used compared to the case when only passive damping is utilized, nonetheless, the efficiency of the system decreases and an additional sensor is necessary to adopt active damping. A low-power full-bridge dc-ac converter is connected in series with the grid-tied VSI unit in [37], to mitigate the effects of the large grid impedance in weak grids by implementing a virtual negative grid impedance through active damping. Due to the increased number of parts, the overhead cost increases and efficiency decreases for higher rated VSIs in adopting the proposed solution in [37]. Therefore, from the above discussion, it can be concluded that there is a tradeoff between stability and system cost when adopting active damping techniques.

Several techniques can be found in literature that employs new control techniques to enable stable operation in weak grids. Control schemes utilizing modified voltage feedforward

paths are presented in several works [29, 38, 39]. In [29], a voltage feedforward is designed considering the PLL dynamics to decrease the interaction between the control loops and grid distortions for improving the stability in weak grids. The voltage feedforward is added to the control scheme through a digital filter, however, the parameters and design process of the filter has not been presented. In [38], a capacitor voltage feedforward strategy is implemented to improve the adaptability of grid-tied VSIs in weak grids. A delay compensation link is added in the path of the voltage feedforward, which improves stability in weak grids by reducing the interaction between the control scheme and grid distortions. In [39], a modified voltage feedforward method containing an impedance-phased compensation strategy is presented to improve the stability margin of grid-tied VSIs in weak grids. However, modification of the voltage feedforward path alters the amplitude and phase of grid currents from their desired values [39]. As a result, there is a tradeoff in the steady-state performance of the closed-loop grid-tied system when employing voltage feedforward methods to improve stability in weak grids. In [21], an impedance shaping method to make the grid-tied system more adaptable to weak grids is presented, which shapes the Thevenin equivalent output impedance of the inverter by adding virtual impedances, to increase its stability margin in the presence of a large grid impedance. However, a series and a parallel virtual impedance are added to the equivalent inverter impedance, which complicates the control structure of the system. Moreover, the proposed scheme in [21] is applied to a grid-tied system with a simplified control scheme neglecting the outer power loops of the typical cascaded control loop structure [40, 42].

Therefore, the most promising solution to the issue of instability in weak grids is possibly the development of a new control structure. However, no such technique is present in literature that is ready to be deployed for practical grid-tied VSI applications.

1.2.2 State-of-the-art in Ancillary Services of Grid-Tied VSIs

The state-of-the-art regarding ancillary services is focused on improving the dynamic performance of the grid-tied system when providing ancillary services. As such, several techniques

are presented in literature for compensating the negative-sequence and harmonic components in grid currents using VSIs, primarily through the implementation of new control strategies [10, 15–19].

In [15], two negative-sequence compensation strategies are presented for grid-tied VSIs providing ancillary services. In the first strategy, the active power oscillations of the VSI, a by-product of providing the negative-sequence current requirements of the system, is minimized. Active power oscillations lead to voltage ripples in the dc-link voltage of the VSI, which has an adverse effect on grid-tied VSI operation. An alternate scheme to compensate the negative-sequence component of the PCC voltages by controlling the negative-sequence inverter current to be in-phase with the negative-sequence grid current is also presented in [15]. The superiority of the presented methods with respect to each other depends on the operation conditions of the system. In [10], a negative-sequence compensation strategy to minimize the active power oscillations of VSIs by controlling the ratio of positive-sequence and negative-sequence conductance and susceptance is presented. To protect the grid-tied VSI from overcurrent, a maximum current limitation scheme is also imposed in the control scheme presented in [10]. The issue of minimizing active power oscillations along with peak current limitation is tackled in [16] through the derivation of a new analytical expression to calculate the desired active and reactive power while providing negative-sequence compensation.

To provide negative-sequence compensation and harmonic compensation in the presence of non-linear and unbalanced loads along with abnormal grid conditions, new control strategies employing a gain scheduling multi-resonant controller and a non-linear backstepping controller based on high-order sliding mode differentiator are presented in [17] and [18], respectively. To satisfy ancillary service requirements in abnormal grid conditions considering grid frequency fluctuations, a control strategy employing third-order sinusoidal signal integrator-based frequency adaptive filter is proposed in [19]. Therefore, it is apparent that several control solutions exist in literature to improve the dynamic performance of grid-tied VSIs when providing ancillary services. However, the decrease in maximum power that can be extracted from DG units when providing ancillary services, due to the restrictions on the

operating limit of VSIs set by the input dc-bus voltage, is yet to be investigated. Providing ancillary services could drive the inverter voltages beyond the linear modulation limit unless pulse width modulation (PWM) references, which are necessary to generate gate signals for the inverter switches in carried-based switching strategies, are adjusted. When employing carrier-based PWM strategies, which have the advantages of implementation simplicity and a well-defined harmonic spectrum [43], the PWM references define line-to-neutral voltages of the VSI. Therefore, by adjusting the PWM references through the injection of a common-mode component, the inverter operating range may be increased when providing ancillary services.

Common-mode injection techniques can be broadly divided into two categories, i.e. instantaneous sequence injection and optimal sequence injection techniques [44–46]. Instantaneous sequence injection techniques are more straightforward to implement in real-time, whereas optimal sequence injection techniques are capable of fulfilling multiple performance criteria. Since the only objective in the context of this work is to extend the linear modulation region of grid-tied VSIs when providing ancillary services, instantaneous sequence injection would be more suitable. Common-mode techniques implemented to improve inverter performance, e.g. decreasing switching losses and increasing the linear modulation region, can be found in literature [43, 47]. However, as is the case for well-known third harmonic injection technique, existing common-mode injection techniques for VSIs typically focus only on symmetrical conditions [43, 48]. A common-mode injection technique suitable for both symmetrical and asymmetrical conditions, as would be the case if the linear modulation range were to be increased when compensating negative-sequence and harmonic components of the grid currents, is not present in literature.

1.3 Contributions of the Dissertation

In this section, the contributions of this dissertation in improving the stability and performance of grid-tied VSIs in the presence of abnormal grid conditions are outlined.

To enhance the stability of grid-tied VSIs in weak grids, an adaptive virtual inductance

feedforward scheme is presented in this dissertation. The concept of virtual impedance has primarily been utilized for active and reactive power sharing between paralleled inverters [49–52]. For accurate power sharing between paralleled inverters, their equivalent output impedances are expected to be equal, therefore, instead of manipulating circuit parameters to match the impedances, virtual impedance terms are added to obtain equal output impedances. The concept of virtual impedance has been extended to other cases as well. In [53–55], virtual impedance is utilized to improve the stability of dc microgrids with constant power loads. In [56, 57], virtual impedance is used for resonance mitigation and power quality improvement through active damping. In [58, 59], the concept of virtual impedance is employed for harmonic compensation of grid-tied inverters, whereas it is used for harmonic current sharing in islanded microgrids in [60]. However, the use of virtual impedance for the stability enhancement of grid-tied VSIs in weak grids is limited. Moreover, in the referenced works [49–60], virtual impedance is applied on the Thevenin equivalent output impedance of the inverters, derived based on impedance-based models. Since, the equivalent impedance is a lumped value containing different system parameters, the role of virtual impedance in these works is not intuitive.

In this work, a detailed state-space model of a grid-tied VSI is first developed. The model contains a general open-loop structure that can be integrated with various control schemes for both grid-tied and standalone operations. An active-reactive power controller model is integrated with the open-loop model to obtain the full-order model for the grid-tied VSI. The comprehensive model contains filter, controller and grid parameters, and thereby allows a detailed study on the role of different parameters for stability in weak grids. Through eigenvalue analysis and continued-fraction-expansion method, it is identified that for systems adopting grid-side current feedback, the grid-side filter inductance of the LCL filter can be increased to improve the stability of grid-tied VSIs in weak grids. To utilize the stabilizing effect of the additional inductance without its drawbacks, a virtual inductance feedforward scheme emulating the behavior of an additional filter inductance in the grid-side LCL filter is developed in this dissertation. The presented scheme is realized by introducing a grid current feedforward path in the inner current control loops of the

PQ controller. The virtual inductance feedforward scheme can be realized without adding any additional sensors to the system. The developed scheme also retains the steady-state performance of the system. Furthermore, for adapting the virtual inductance to ensure stability under varying grid impedances, a direct model reference adaptive control (MRAC) scheme is integrated to the PQ controller of the grid-tied VSI. The direct MRAC scheme adaptively varies the virtual inductance value according to a stable reference model for different weak grid scenarios without requiring grid impedance estimation. The presented scheme is validated by performing stability analysis through root-locus studies and hardware test scenarios carried out on a three-phase grid-tied experimental setup.

To extract the maximum power from DG units when providing ancillary services under abnormal grid conditions, an atypical PWM method is developed in this dissertation to increase the linear modulation region of grid-tied VSIs by maximizing the dc-bus utilization. The atypical PWM scheme is realized by injecting a common-mode component in the PWM references, computed based on instantaneous reference magnitudes. The presented scheme is applicable for both symmetrical, i.e. harmonic compensation, and asymmetrical, i.e. negative-sequence compensation, ancillary services. The atypical scheme acts as an intermediate step between controller output generation and gate signal creation by the PWM generator. Therefore, the presented scheme can be used with any inverter control structure employing carried-based PWMs. The validity of the developed atypical PWM scheme is verified through simulation studies performed in MATLAB/Simulink and through experimental scenarios carried out in a three-phase grid-tied hardware setup.

The contributions of the dissertation can be summarized as follows:

- A comprehensive model for a grid-tied VSI is presented containing filter, controller and grid parameter. Detailed analyses regarding the interaction among the different parameters can be performed using the model. The effect of several parameters on the stability of grid-tied VSIs in weak grids is presented.

- A virtual inductance feedforward scheme is presented to enable stable operation of grid-tied VSIs in weak grids. The presented scheme is an improvement over the existing

techniques in literature as the stability region of grid-tied VSIs is enhanced without any hardware modifications and without compromising the steady-state performance of the system.

- A direct MRAC method is integrated with the virtual inductance feedforward scheme to vary the virtual inductance adaptively for different grid impedances. Introduction of the adaptive design procedure in the control scheme makes the presented technique more suitable for practical applications under various weak grid conditions.

- A common-mode injection technique is presented to maximize the dc-bus utilization of grid-tied VSIs when providing ancillary services. The presented technique is suitable for both symmetrical and asymmetrical ancillary services and is applicable for any controller structure employing carrier-based PWMs.

1.4 Organization of the Dissertation

The remainder of this dissertation is organized as follows:

The detailed state-space model of the grid-tied VSI is presented in Chapter 2. An open-loop circuit model for the VSI is first derived. The model is validated through simulation and experimental studies. A model for an active-reactive power controller is then derived and integrated with the open-loop model to develop the full-order model for the grid-tied system.

The effect of various system parameters on the stability of the grid-tied system in weak grids is studied in Chapter 3. Through root-locus of the eigenvalues of the model derived in Chapter 2, several parameters are identified that can be designed to improve the stability of the grid-tied system in weak grids. The results obtained from the eigenvalue analysis are verified through hardware tests. The tradeoff in performance associated with the redesign of grid-tied system parameters is also discussed.

The virtual inductance feedforward scheme for stable operation of grid-tied VSIs in weak grids is developed in Chapter 4. The stabilizing effect of increased grid-side filter inductance

in weak grids is first validated through the application of the continued-fraction-expansion method on the system transfer function derived from a lossless signal flow graph of the grid-tied system. A virtual inductance emulating an additional inductance in the grid-side LCL filter is then derived and integrated to the controller model to obtain a modified state-space model including virtual inductance feedforward. Root locus studies of the eigenvalues of the modified model validate the efficacy of the virtual inductance scheme. The validity of the presented scheme and its steady-state performance are verified through hardware tests.

The direct MRAC scheme is integrated into the virtual inductance feedforward method in Chapter 5. The motivation behind employing the direct MRAC scheme over indirect adaptive control techniques is first discussed. The adaptation law for updating the virtual inductance value according to a stable reference model is then derived based on the Lyapunov stability criterion. The modified control scheme including the adaptive virtual inductance feedforward is then developed. The efficacy of the adopted scheme is verified for different weak grid conditions through hardware tests.

The atypical PWM scheme to extend the linear modulation range for grid-tied VSIs providing ancillary services is developed in Chapter 6. The modified control scheme of a grid-tied VSI providing negative-sequence compensation and harmonic compensation is first presented. Then the common-mode reference generation procedure for the atypical scheme is derived and the extent to which the presented scheme can increase the linear modulation range is also discussed. The efficacy of the atypical scheme is then verified through simulation and experimental studies performed under unbalanced loads and distorted grid voltages.

Finally, a summary of the presented research in this dissertation and the contribution to the state-of-the-art regarding grid-tied VSI performance in abnormal grid conditions are presented in Chapter 7. Furthermore, suggestions for future work in updating the developed virtual inductance feedforward scheme for stability and improved power quality in unbalanced weak grids is also presented in Chapter 7.

Chapter 2

Grid-Tied VSI - Modeling and Control

This chapter presents a full-order state-space model of a three-phase two-level grid-tied VSI equipped with an active power (P) and reactive power (Q) controller. Two-level VSIs are the prevalent choice for grid integration of DG units. Compared to multi-level inverter topologies, two-level VSIs may require larger filter values to eliminate the harmonic components of the generated voltage. However, two-level VSIs are more reliable as they can be realized using fewer switches and the switching schemes of such inverters are far less complicated than their multi-level inverter counterparts. In this dissertation, a two-level VSI is implied when discussing VSIs. The grid-tied VSI system includes a PQ controller to control the P and Q supplied by the VSI to its associated loads and the utility.

The contents of this chapter are organized into four sections. An open-loop model of a grid-tied VSI is presented in Section 2.1. The open-loop model is based on a similar work proposed in [61]. The model is briefly described herein, for continuity and reproducibility of the work presented. For the purposes of this dissertation, the model is then verified through both simulation and hardware tests. A model of the PQ controller employed in this dissertation is provided in Section 2.2. The models are combined to derive a full-order state-space model of a grid-tied VSI in Section 2.3, which is one of the contributions of this

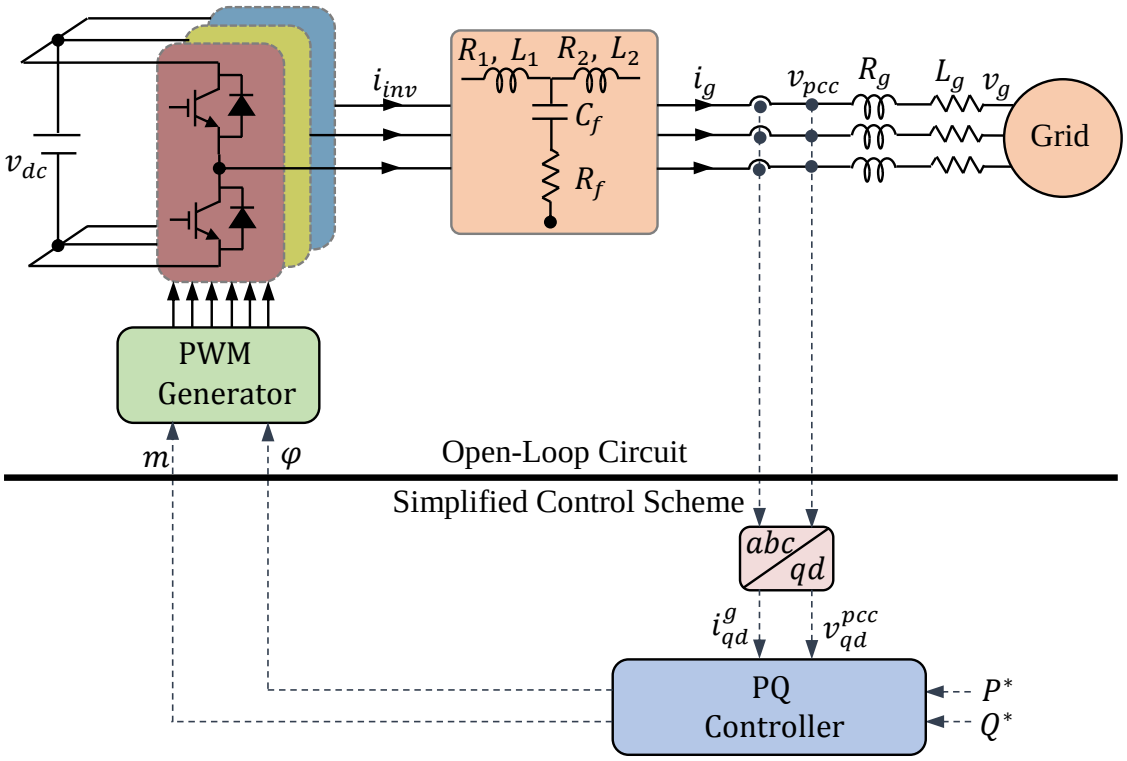


Figure 2.1: *Schematic block diagram of a grid-tied VSI equipped with an LCL filter and a PQ controller*

dissertation. Concluding remarks are given in Section 2.4.

2.1 Open-Loop Model

In this section, an open-loop circuit model of a grid-tied VSI is developed. The general structure of the model enables it to be integrated with various control schemes employing both carrier-based pulse width modulation (PWM) and space vector PWM (SVPWM) techniques.

2.1.1 Derivation of the Open-Loop Model

The schematic block diagram of a grid-tied VSI is shown in Fig. 2.1. The switching module of the VSI consists of three legs representing the three phases of the system with each leg containing two semiconductor switches. An LCL filter is employed to reduce the switching harmonics of the inverter voltage. The LCL filter includes inverter side filter inductor L_1,

grid side filter inductor L_2, and delta-connected capacitor C_f with series resistor R_f. The parasitic resistances of L_1 and L_2 are denoted by R_1 and R_2, respectively. The grid is represented by an ideal voltage source v_g with series equivalent resistance and inductance denoted by R_g and L_g, respectively. For generality, an ideal dc voltage source v_{dc} is employed as the input to the inverter bridge. The PQ controller illustrated in Fig. 2.1 will be discussed and modeled in the next section.

The open-loop model is obtained in three main steps. In the first step, the state-space equations of the circuits corresponding to each switching state are derived. The SVPWM switching technique is considered in this work to determine the various switching states of the VSI, while the final model will also be applicable for VSIs employing other switching techniques, e.g. SPWM and SPWM injected with third harmonic [61]. In the SVPWM technique, the VSI alternates between seven circuit configurations corresponding to six active switching states, i.e. (100), (110), (010), (011), (001), and (101), and two zeros switching states, i.e. (111) and (000). The circuit configuration for the two zero switching states is the same. The switching states for SVPWM are illustrated in Fig. 2.2. The zero switching states result in a zero voltage and are placed at the origin as can be seen from Fig. 2.2. Notice that the switching states can be defined sufficiently through the state of the top switches of each

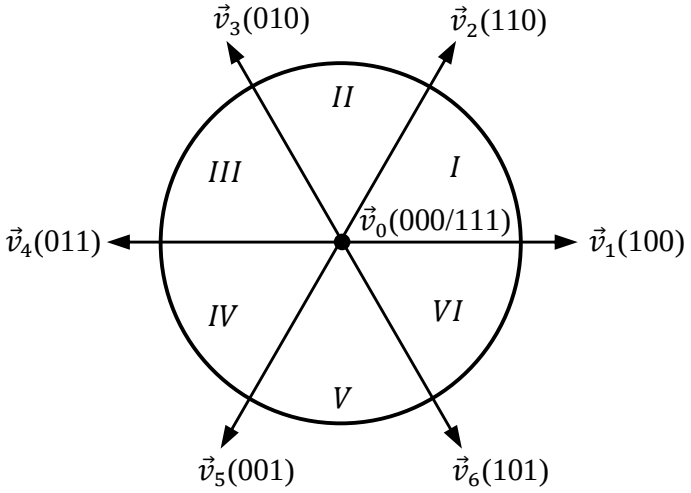
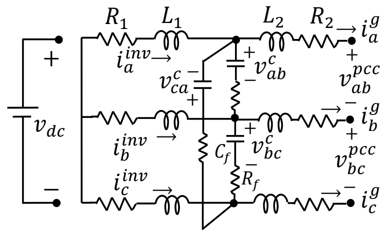
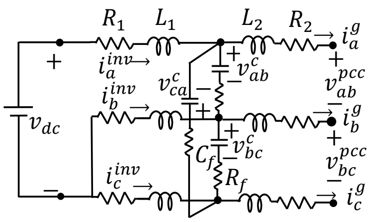
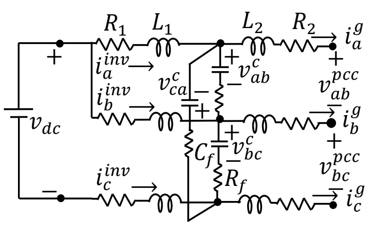


Figure 2.2: *Switching states and sectors for SVPWM technique.*

Table 2.1: *State-space model derivation steps of VSI for Sector I of SVPWM*

		
$\dot{x}_{abc} = Ax_{abc} + B_0 u_{abc}$	$\dot{x}_{abc} = Ax_{abc} + B_1 u_{abc}$	$\dot{x}_{abc} = Ax_{abc} + B_2 u_{abc}$
$\dot{x}_{abc} = Ax_{abc} + \overline{B}_I u_{abc},$	$x_{abc} = [i_a^{inv}, i_b^{inv}, v_{ab}^c, v_{bc}^c, i_a^g, i_b^g]^T,$	$u_{abc} = [v_{dc}, v_{ab}^{pcc}, v_{bc}^{pcc}]^T,$

$$A = \begin{bmatrix} \frac{-3R_1-R_f}{3L_1} & 0 & \frac{-2}{3L_1} & \frac{-1}{3L_1} & \frac{R_f}{3L_1} & 0 \\ 0 & \frac{-3R_1-R_f}{3L_1} & \frac{1}{3L_1} & \frac{-1}{3L_1} & 0 & \frac{R_f}{3L_1} \\ \frac{1}{3C_f} & \frac{-1}{3C_f} & 0 & 0 & \frac{-1}{3C_f} & \frac{1}{3C_f} \\ \frac{1}{3C_f} & \frac{2}{3C_f} & 0 & 0 & \frac{-1}{3C_f} & \frac{-2}{3C_f} \\ \frac{R_f}{3L_2} & 0 & \frac{2}{3L_2} & \frac{1}{3L_2} & \frac{-3R_2-R_f}{3L_2} & 0 \\ 0 & \frac{R_f}{3L_2} & \frac{-1}{3L_2} & \frac{1}{3L_2} & 0 & \frac{-3R_2-R_f}{3L_2} \end{bmatrix} \qquad \overline{B}_I = \begin{bmatrix} \frac{2d_1+d_2}{3L_1} & 0 & 0 \\ \frac{-d_1+d_2}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix}$$

leg since at any instant only one switch from each leg is turned ON to prevent dc-bus short circuits. For instance, a switching state of (100) indicates that the top switch connected to phase-A and the bottom switches connected to phase-B and phase-C are ON, while the remaining switches are OFF.

As one can see from Fig. 2.2, the operation of the VSI in SVPWM can be divided into six sectors, with the VSI alternating between two active and one zero switching state in each sector. Hence, each sector contains three state-space representations corresponding to the three circuit configurations. The circuit diagrams of the three switching states of sector I, i.e. (111) or (000), (100) and (110), are illustrated from left to right in the first row of Table 2.1. In the following row of Table 2.1, the short forms of the state-space representations corresponding to the circuit configurations are also provided. Notice that the A matrix is the same for all three equations, while the B matrices are different due to the contrasting ways the input dc source is connected to the rest of the circuit. Three such state-space models exist for each of the six sectors. In the second step, the three state-space equations for each

sector are averaged over the PWM switching interval T_s to obtain averaged models for each sector [62, 63]. The averaged model for sector I is shown in the last row of Table 2.1, where $d_0(d_0 = t_0/T_s)$, $d_1(d_1 = t_1/T_s)$, and $d_2(d_2 = t_2/T_s)$ are the duty cycles for the zero switching states and the two active switching states, respectively, with $t_0 + t_1 + t_2 = T_s$. As shown in Table 2.1, the states of the state-space models are the three-phase current i_{inv} going through L_1, the voltage v_c across C_f and the current i_g going through L_2. The inputs to the open-loop model are the dc-bus voltage and three-phase voltage v_{pcc} at the PCC. Only two phases of the three-phase quantities are considered as the system is balanced, i.e. $x_a + x_b + x_c = 0$. Following the same procedure, the averaged state-space models of all six sectors are derived. The averaged state-space models of the remaining sectors are provided in Appendix A.

In the final step, the averaged state-space models for all six sectors are transferred from the *abc* frame to the synchronously rotating *dq* frame of reference through Park's transformation [64, 65], which remarkably results in a unique dynamic model for all six sectors that is given in (2.1).

$$\frac{d}{dt}\begin{bmatrix} i_q^{inv} \\ i_d^{inv} \\ v_q^c \\ v_d^c \\ i_q^g \\ i_d^g \end{bmatrix} = \begin{bmatrix} \frac{-3R_1-R_f}{3L_1} & -\omega & \frac{-1}{2L_1} & \frac{\sqrt{3}}{6L_1} & \frac{R_f}{3L_1} & 0 \\ \omega & \frac{-3R_1-R_f}{3L_1} & \frac{-\sqrt{3}}{6L_1} & \frac{-1}{2L_1} & 0 & \frac{R_f}{3L_1} \\ \frac{1}{2C_f} & \frac{\sqrt{3}}{6C_f} & 0 & -\omega & \frac{-1}{2C_f} & \frac{-\sqrt{3}}{6C_f} \\ \frac{-\sqrt{3}}{6C_f} & \frac{1}{2C_f} & \omega & 0 & \frac{\sqrt{3}}{6C_f} & \frac{-1}{2C_f} \\ \frac{R_f}{3L_2} & 0 & \frac{1}{2L_2} & \frac{-\sqrt{3}}{6L_2} & \frac{-3R_2-R_f}{3L_2} & -\omega \\ 0 & \frac{R_f}{3L_2} & \frac{\sqrt{3}}{6L_2} & \frac{1}{2L_2} & \omega & \frac{-3R_2-R_f}{3L_2} \end{bmatrix} \begin{bmatrix} i_q^{inv} \\ i_d^{inv} \\ v_q^c \\ v_d^c \\ i_q^g \\ i_d^g \end{bmatrix} + \begin{bmatrix} \frac{\sqrt{3}mcos(\psi)}{3L_1} & 0 & 0 \\ \frac{-\sqrt{3}msin(\psi)}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-1}{2L_2} & \frac{\sqrt{3}}{6L_2} \\ 0 & \frac{-\sqrt{3}}{6L_2} & \frac{-1}{2L_2} \end{bmatrix} \begin{bmatrix} v_{dc} \\ v_q^{pcc} \\ v_d^{pcc} \end{bmatrix}. \tag{2.1}$$

The Park's transformation for a balanced system is expressed as follows:

$$\begin{bmatrix} x_q \\ x_d \end{bmatrix} = \frac{2}{\sqrt{3}} \begin{bmatrix} -sin(\theta - 2\pi/3) & sin(\theta) \\ cos(\theta - 2\pi/3) & -cos(\theta) \end{bmatrix} \begin{bmatrix} x_a \\ x_b \end{bmatrix}, \tag{2.2}$$

where, the reference angle for Park's transformation $\theta = \omega t$ is set as the instantaneous phase angle of v_{pcc}, which can be obtained using a PLL. In this dissertation, an instantaneous phase detector is used to obtain the reference angle at the PCC as defined below [66, 67]:

$$\theta = tan^{-1}(\frac{v_{ab} + 2v_{bc}}{\sqrt{3}v_{ab}}), \tag{2.3}$$

where, $d\theta/dt = \omega$ is the angular frequency of the grid. It can be seen from (2.1) that the B matrix of the state-space model contains the modulation index m and the angle between the inverter phase voltage and the reference ψ, which are control parameters (directly in SPWM or indirectly in SVPWM technique) that vary by control signals of the system. Hence, the model presented in (2.1) is time-variant and non-linear. Furthermore, the fundamental frequency of the system ω is also expected to be an input rather than a constant quantity. Therefore, to obtain a linear time-invariant model of the open-loop VSI, the model in (2.1) is linearized around a steady-state operating point to derive the small-signal model of the system as follows:

$$\frac{d}{dt} \begin{bmatrix} \tilde{i}_{qd}^{inv} \\ \tilde{v}_{qd}^{c} \\ \tilde{i}_{qd}^{g} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \\ A_{31} & A_{32} & A_{33} \end{bmatrix} \begin{bmatrix} \tilde{i}_{qd}^{inv} \\ \tilde{v}_{qd}^{c} \\ \tilde{i}_{qd}^{g} \end{bmatrix} + \begin{bmatrix} 0 & B_{12} & b_1 \\ 0 & 0 & b_2 \\ B_{31} & 0 & b_3 \end{bmatrix} \begin{bmatrix} \tilde{v}_{qd}^{pcc} \\ \tilde{z} \\ \tilde{\omega} \end{bmatrix}, \tag{2.4}$$

where, the state and input variables in the dq frame of reference are expressed in vector form as, $\tilde{i}_{qd}^{inv} = \begin{bmatrix} \tilde{i}_q^{inv} & \tilde{i}_d^{inv} \end{bmatrix}^T$, $\tilde{v}_{qd}^{c} = \begin{bmatrix} \tilde{v}_q^{c} & \tilde{v}_d^{c} \end{bmatrix}^T$, $\tilde{i}_{qd}^{g} = \begin{bmatrix} \tilde{i}_q^{g} & \tilde{i}_d^{g} \end{bmatrix}^T$, $\tilde{v}_{qd}^{pcc} = \begin{bmatrix} \tilde{v}_q^{pcc} & \tilde{v}_d^{pcc} \end{bmatrix}^T$, and $\tilde{z} = \begin{bmatrix} \tilde{m} & \tilde{\psi} \end{bmatrix}^T$. The block matrices introduced in (2.4) are provided in Appendix A. Instead of developing a small-signal model through linearization, non-linear techniques, e.g. Lyapunov stability criterion, can also be utilized for stability analysis. However, selection of

an appropriate Lyapunov function could significantly complicate the analysis [68, 69], therefore, linearized models are commonly employed. The small-signal model derived in (2.4) is verified through laboratory experiments in Subsection 2.1.2. Compared to the large-signal model in (2.1), the B matrix of the small-signal model in (2.4) has three additional columns associated with the new inputs, $\tilde{m}$, $\tilde{\psi}$, and $\tilde{\omega}$, where $m = \tilde{m} + M$, $\psi = \tilde{\psi} + \Psi$, and $\omega = \tilde{\omega} + \Omega$. The steady-state values M and Ψ can be calculated for any given operating point using the active and reactive power generated by the VSI, while Ω for a grid-tied VSI is $377 rad/s$. The A matrix of the small-signal model is the same as that of the large-signal model with ω replaced by its steady-state value. Notice that v_{dc} is considered as an ideal voltage source, hence $\tilde{v}_{dc} = 0$. Therefore, v_{dc} is not considered as an input in the small-signal model. It should be noted that the circuit models in the second step of the derivation process are averaged over the switching period, where the typical switching frequency of grid-tied VSIs is $4 - 10 kHz$. On the other hand, the dominant eigenvalues of grid-tied VSI models are reported to have frequencies below $750 Hz$($5000 rad/sec$) [38, 42, 68], therefore, the impact of averaging on the analysis of system stability is insignificant. The developed open-loop model in (2.4) can be incorporated with various control schemes by replacing the inputs $\tilde{m}$ and $\tilde{\psi}$ by the respective controller outputs.

2.1.2 Open-Loop Model Verification

The open-loop model derived in (2.4) is verified using both simulation and experimental results. For open-loop model verification in grid-tied mode, the grid can be incorporated in the model by replacing R_2 and L_2 by $R_2 + R_g$ and $L_2 + L_g$, respectively. Also, the input v_{pcc} gets replaced by v_g. Depending on the point of current measurement, a different procedure might have to be followed to incorporate the grid in a closed-loop model, which will be further elaborated in Section 2.3.

Model verification via circuit simulation is performed in MATLAB making use of circuit components from the SimPowerSystem toolbox. To validate the efficacy of the open-loop model, the states of the model and the corresponding simulation waveforms are plotted

simultaneously in Fig. 2.3 as the input m was changed from 0.8 to 0.9 at instant $0.45s$. Notice, in solving (2.4), M was fixed at 0.8, while $\tilde{m}$ had a step change of 0.1. As one can see from Fig. 2.3, the model is an impressive match for its circuit simulation counterpart. Since the model is derived through averaging over the switching interval, the switching harmonics are not represented by the model. The circuit parameters employed for this scenario are presented in Table 2.2.

The open-loop model derived in (2.4) is also verified through a hardware experiment. For the hardware test carried out, the power board of an Allen-Bradley drive, Powerflex 755, was used while the inverter switching signals were generated by an Altera Cyclone III FPGA interfaced with a dSpace 1103 Controller Board [70]. The experimental setup is shown in Fig. 2.4. Circuit parameters used for this test are provided in Table 2.2. Utilizing a four-channel Lecroy Waverunner 64 Xi-A oscilloscope with CP030 current probes and ADP300 differential voltage probes, two voltages across the filter capacitors and two line currents being injected to the grid were measured at a sampling frequency of $100kHz$ and compared against the respective open-loop model state variables as shown in Fig. 2.5. Notice that the model state variables obtained through solving (2.4) were transformed from the dq frame to the abc frame as the measured experimental waveforms are in the abc frame of reference. As one can see from Fig. 2.5, the developed model matches the laboratory test results under both steady-state operation and for a sudden change in m from 0.83 to 0.93 at instant $0.4s$. Therefore, the developed linear time-invariant state-space model in (2.4) is verified to be an accurate representation of an open-loop VSI through both simulation and hardware tests.

Table 2.2: *Parameters employed for open-loop model verification*

Parameter	Simulation	Experiment
L_1	$2.5mH$	$2.5mH$
L_2	$2.5mH$	$2.5mH$
C_f	$10\mu H(\Delta)$	$10\mu H(\Delta)$
R_f	0.5Ω	0.05Ω
Ψ	$-0.4rad$	$0.46rad$

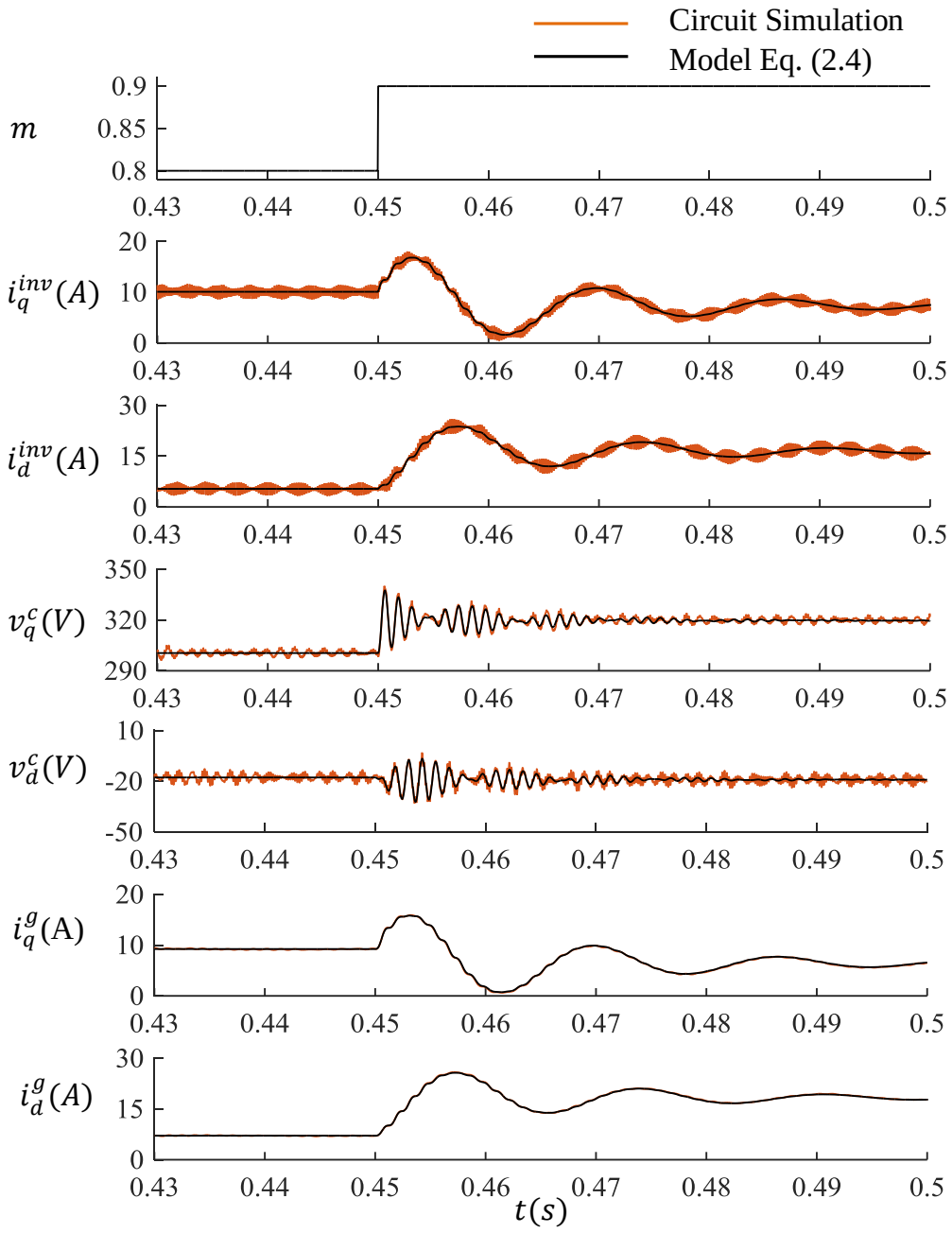


Figure 2.3: *Open-loop model verification through circuit simulation under a change in* m *from* 0.8 *to* 0.9 *at instant* $0.45s$

2.2 Active-Reactive Power Controller Model

Grid-tied inverters are equipped with PQ controllers to control the active and reactive power supplied to the grid, whereas other control schemes might be implemented in the standalone

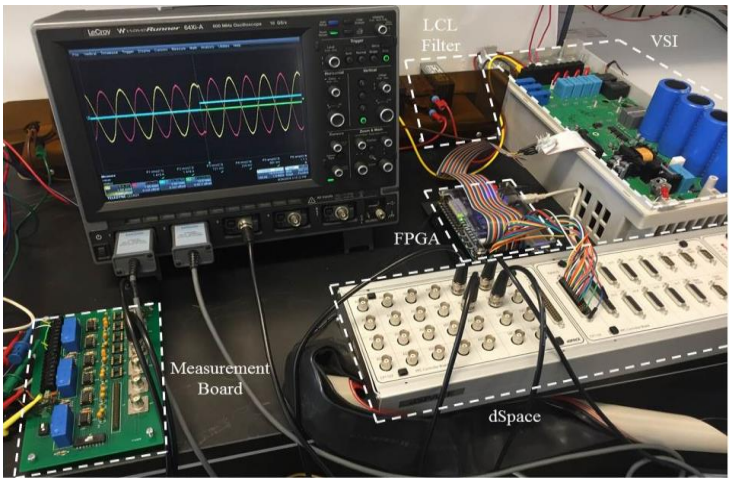


Figure 2.4: *Experimental setup for open-loop model verification test*

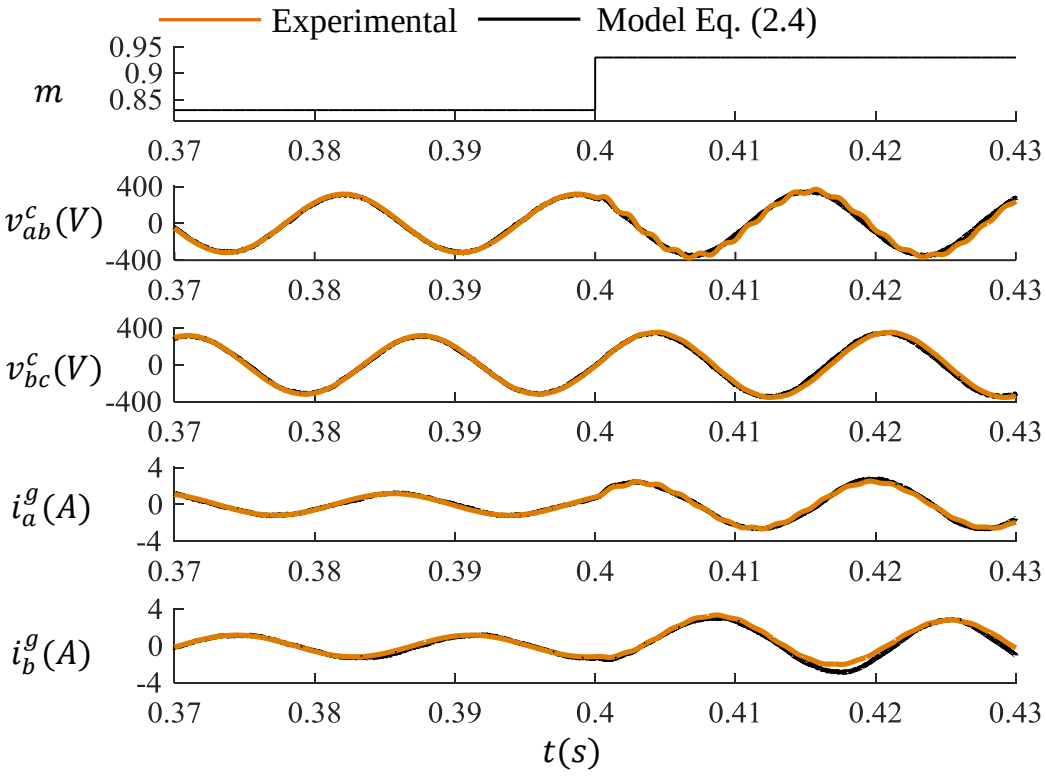


Figure 2.5: *Open-loop model verification in the abc frame through hardware test under a change in* m *from* 0.83 *to* 0.93 *at instant* $0.4s$

mode to regulate the voltage at the PCC [40, 71]. In this section, a state-space model for a PQ controller is developed, which is to be interfaced with the open-loop model developed in Section 2.1 to derive a full-order state-space model of the grid-tied system in Section 2.3.

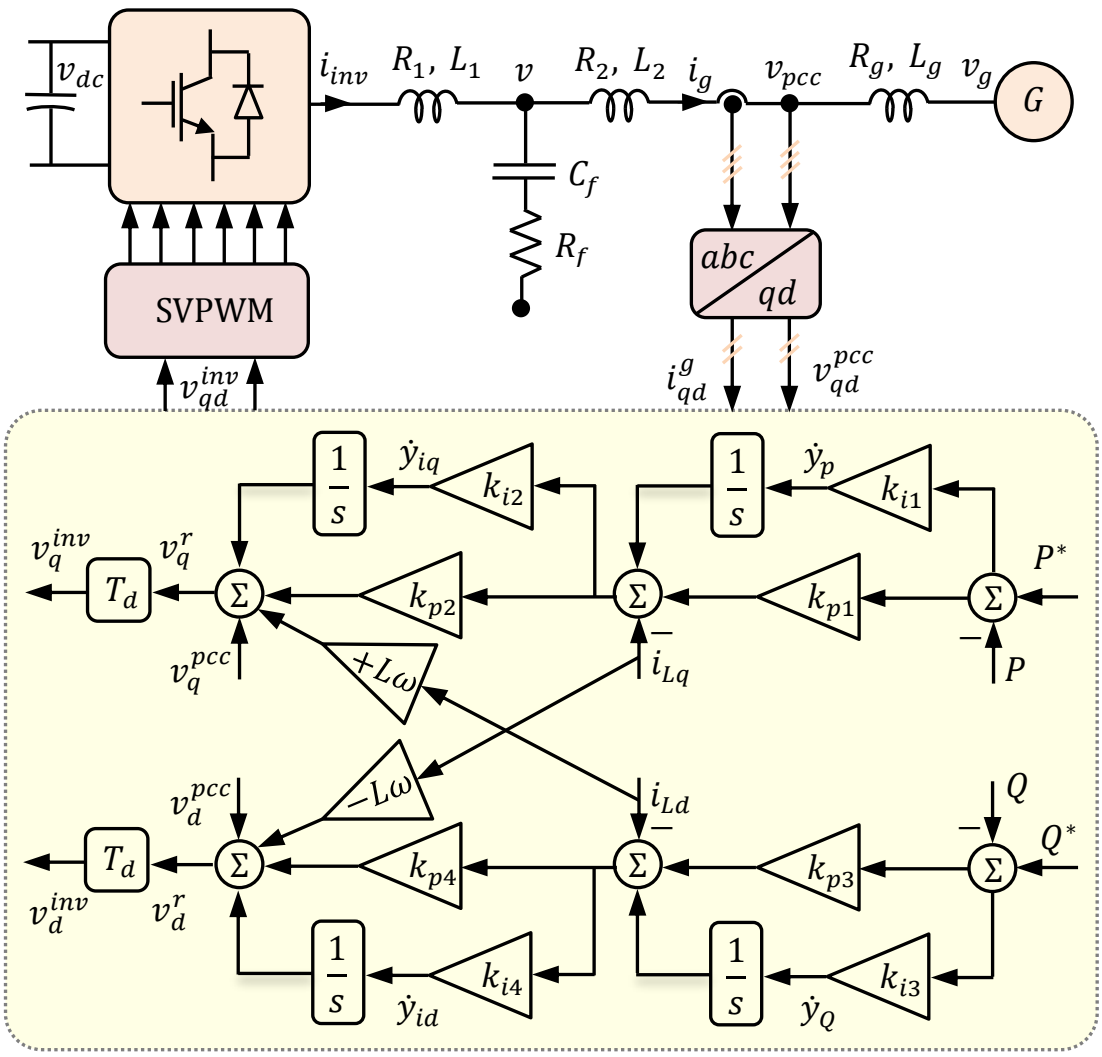


Figure 2.6: *Control block diagram of a PQ-controlled grid-tied VSI*

A detailed block diagram of the PQ controller employed in this work is illustrated in Fig. 2.6. The controller operates in the synchronously rotating *dq* frame of reference. The control scheme utilizes positive-sequence components of the measured signals as balanced grid voltages are considered. Independent controllers can be added to the control scheme to provide negative-sequence compensation under unbalanced grid voltages, which will be discussed in detail in Chapter 6. The P and Q control loops are cascaded with q- and d-axis current control loops, respectively, to independently control the active and reactive power supplied to the grid [42]. The cascaded dual loop structure displays improved dynamic performance compared to single loop control schemes [40]. Each loop is realized using a

proportional integral (PI) controller. A PCC voltage feedforward term is added at the end of both the P and Q control loops, which improves controller performance under distorted grid voltages [40]. In PV and wind-powered applications, similar control structure can be utilized with the inner q-axis current loop interfaced with an outer dc-bus voltage control loop instead of the outer P loop. The active power can then be controlled using maximum power point tracking techniques. The outer loop, having slow dynamics, aims for system stability under changes in operating conditions such as solar irradiance, wind speed, and temperature variation.

As illustrated in Fig. 2.6, line-to-line voltages and line currents are sensed at the PCC and converted to the *dq* frame, which are then used as inputs to the PQ control scheme. The measured line currents are transformed to *virtual* line-to-line currents, which can be defined in the *abc* frame as $i_{ab} = i_a - i_b, i_{bc} = i_b - i_c$, and $i_{ca} = i_c - i_a$. With the use of virtual line-to-line currents the noise associated with current measurements is reduced. The conversion between line currents and virtual line-to-line currents in the *dq* frame can be expressed as follows:

$$\begin{bmatrix} i_q^g \\ i_d^g \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & \frac{-1}{2\sqrt{3}} \\ \frac{1}{2\sqrt{3}} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{qL} \\ i_{dL} \end{bmatrix}. \tag{2.5}$$

It should be noted that the controller model will remain unchanged if one chooses to utilize phase voltages and line currents instead of line-to-line voltages and virtual line-to-line currents. Therefore, the derived grid-tied VSI controller model will be directly applicable to PQ control schemes using phase voltages and line currents [42].

The four integrators associated with the control loops contribute four state variables to the controller model. The four state variables, i.e. y_P, y_{iq}, y_Q, and y_{id}, are highlighted in Fig. 2.6 and can be expressed as follows:

$$\dot{y}_P = k_{i1}(P^* - P), \tag{2.6}$$

$$\dot{y}_{iq} = k_{i2}(y_P + k_{p1}(P^* - P) - i_{qL}), \tag{2.7}$$

$$\dot{y}_Q = k_{i3}(Q^* - Q), \tag{2.8}$$

$$\dot{y}_{id} = k_{i4}(y_Q + k_{p3}(Q^* - Q) - i_{dL}), \tag{2.9}$$

where, P^* and Q^* are the desired active and reactive power supplied to the grid, respectively, which are the inputs to the controller model. Also, the k_p's and k_i's are the proportional and integral gains of the controllers as shown in Fig. 2.6.

The output P and Q of the VSI can be expressed in terms of measured quantities as:

$$P = \frac{1}{2}v_q^{pcc}i_{qL} + \frac{1}{2}v_d^{pcc}i_{dL}, \tag{2.10}$$

$$Q = \frac{1}{2}v_q^{pcc}i_{dL} - \frac{1}{2}v_d^{pcc}i_{qL}. \tag{2.11}$$

Linearizing (2.10) and (2.11) around a steady-state operating point and replacing them in (2.6) through (2.9), the controller state variables can be expressed as follows:

$$\dot{y}_P = k_{i1}P^* - \frac{1}{2}k_{i1}V_q^{pcc}i_{qL} - \frac{1}{2}k_{i1}I_{qL}v_q^{pcc} - \frac{1}{2}k_{i1}I_{dL}v_d^{pcc}, \tag{2.12}$$

$$\dot{y}_{iq} = k_{i2}y_P - \frac{1}{2}k_{p1}k_{i2}V_q^{pcc}i_{qL} - k_{i2}i_{qL} - \frac{1}{2}k_{p1}k_{i2}I_{qL}v_q^{pcc} - \frac{1}{2}k_{p1}k_{i2}I_{dL}v_d^{pcc} + k_{p1}k_{i2}P^*, \tag{2.13}$$

$$\dot{y}_Q = k_{i3}Q^* - \frac{1}{2}k_{i3}V_q^{pcc}i_{dL} - \frac{1}{2}k_{i3}I_{dL}v_q^{pcc} + \frac{1}{2}k_{i3}I_{qL}v_d^{pcc}, \tag{2.14}$$

$$\dot{y}_{id} = k_{i4}y_Q - \frac{1}{2}k_{p3}k_{i4}V_q^{pcc}i_{dL} - k_{i4}i_{dL} - \frac{1}{2}k_{p3}k_{i4}I_{dL}v_q^{pcc} + \frac{1}{2}k_{p3}k_{i4}I_{qL}v_d^{pcc} + k_{p3}k_{i4}Q^*. \tag{2.15}$$

Now, (2.12) through (2.15) can be expressed in matrix from as follows:

$$\frac{d}{dt}\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} A_{43} & 0 & 0 \\ A_{53} & A_{54} & 0 \end{bmatrix} \begin{bmatrix} i_{qdL} \\ y_1 \\ y_2 \end{bmatrix} + \begin{bmatrix} B_{41} & B_{43} \\ B_{51} & B_{53} \end{bmatrix} \begin{bmatrix} v_{qd}^{pcc} \\ R^* \end{bmatrix}, \tag{2.16}$$

where, $y_1 = \begin{bmatrix} y_P & y_Q \end{bmatrix}^T$, $y_2 = \begin{bmatrix} y_{iq} & y_{id} \end{bmatrix}^T$, $i_{qdL} = \begin{bmatrix} i_{qL} & i_{dL} \end{bmatrix}^T$ and $R^* = \begin{bmatrix} P^* & Q^* \end{bmatrix}$. Notice that the tilde operator is omitted from the small-signal states and inputs for simplicity. The block matrices introduced in (2.16) are provided in Appendix A.

The controller output equations can be written from Fig. 2.6 as follows:

$$v_q^r = v_q^{pcc} + k_{p2}(y_P + k_{p1}(P^* - P) - i_{qL}) + \omega L i_{dL} + y_{iq}, \tag{2.17}$$

$$v_d^r = v_d^{pcc} + k_{p4}(y_Q + k_{p3}(Q^* - Q) - i_{dL}) - \omega L i_{dL} + y_{id}. \tag{2.18}$$

A time delay associated with PWM signal update can affect the stability of grid-tied inverters [72, 73]. A simple approach to implement the effect of delay in continuous-time controllers is through the following differential equations:

$$\dot{v}_q^{inv} = \frac{1}{T_d}(v_q^r - v_q^{inv}), \tag{2.19}$$

$$\dot{v}_d^{inv} = \frac{1}{T_d}(v_d^r - v_d^{inv}), \tag{2.20}$$

where, T_d is the control delay as shown in 2.6. Now, linearizing (2.17) and (2.18), and substituting in (2.19) and (2.20) yield:

$$\begin{aligned}\dot{v}_q^{inv} = \frac{k_{p2}}{T_d}(-1 - \frac{1}{2}k_{p1}V_q^{pcc})i_{qL} + \frac{1}{T_d}\omega L i_{dL} + \frac{k_{p2}}{T_d}y_P + \frac{1}{T_d}y_{iq} - \frac{1}{T_d}v_{inv}^q + \frac{k_{p1}k_{p2}}{T_d}P^* \\ + \frac{1}{T_d}(1 - \frac{1}{2}k_{p1}k_{p2}I_{qL})v_q^{pcc} - \frac{1}{2T_d}k_{p1}k_{p2}I_{dL}v_d^{pcc}\end{aligned} \tag{2.21}$$

$$\begin{aligned}\dot{v}_d^{inv} = -\frac{1}{T_d}\omega L i_{qL} + \frac{k_{p4}}{T_d}(-1 - \frac{1}{2}k_{p3}V_q^{pcc})i_{dL} + \frac{k_{p4}}{T_d}y_Q + \frac{1}{T_d}y_{id} - \frac{1}{T_d}v_{inv}^d + \frac{k_{p3}k_{p4}}{T_d}Q^* \\ - \frac{1}{2T_d}k_{p3}k_{p4}I_{dL}v_q^{pcc} + \frac{1}{T_d}(1 + \frac{1}{2}k_{p3}k_{p4}I_{qL})v_d^{pcc}\end{aligned} \tag{2.22}$$

Now, (2.21) and (2.22)can be expressed using $2X2$ block matrices as follows:

$$\frac{d}{dt}v_{qd}^{inv} = A_{63}i_{qdL} + A_{64}y_1 + A_{65}y_2 + A_{66}v_{qd}^{inv} + B_{61}v_{qd}^{pcc} + B_{63}R^*, \tag{2.23}$$

where, $v_{qd}^{inv} = \begin{bmatrix} v_q^{inv} & v_d^{inv} \end{bmatrix}^T$. The block matrices introduced in (2.23) can be found in Appendix A. Equations (2.16) and (2.23) define the state-space model for the grid-tied VSI PQ controller. In the next section, the derived controller model and the open-loop model in (2.4)

will be integrated to derive the full-order state-space model of a PQ-controlled grid-tied VSI.

2.3 Full-Order State-Space Model

In this section, the open-loop model derived in Section 2.1 and the PQ-controller model obtained in Section 2.2 are integrated to develop a full-order state-space model for a grid-tied VSI.

The first thing to note about the open-loop circuit model and the controller model is that the open-loop model contain grid line currents i^g_{qd} as state variables whereas the controller model is defined in terms of virtual line-to-line currents i_{qdL}. Therefore, to allow integration of the models, i^g_{qd} have to be expressed in terms of i_{qdL} or vice versa. Using the transformation between i^g_{qd} and i_{qdL} provided in (2.5), the open-loop model in (2.4) can be expressed in terms of i_{qdL} as:

$$\frac{d}{dt}\begin{bmatrix} i^{inv}_{qd} \\ v^c_{qd} \\ i_{qdL} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A^L_{13} \\ A_{21} & A_{22} & A^L_{23} \\ A^L_{31} & A^L_{32} & A^L_{33} \end{bmatrix} \begin{bmatrix} i^{inv}_{qd} \\ v^c_{qd} \\ i_{qdL} \end{bmatrix} + \begin{bmatrix} 0 & B_{12} & b_1 \\ 0 & 0 & b_2 \\ B^L_{31} & 0 & b^L_3 \end{bmatrix} \begin{bmatrix} v^{pcc}_{qd} \\ z \\ \omega \end{bmatrix}, \tag{2.24}$$

where, the modified block matrices are denoted by superscript L and are included in Appendix A. Notice that the tilde operators have been removed from the small signal variables for simplicity.

The open-loop model in (2.24) contain the control variables $z = \begin{bmatrix} m & \psi \end{bmatrix}^T$ as inputs. On the other hand, from Fig. 2.6, the controller outputs can be identified as the inverter voltages $v^{inv}_{qd} = \begin{bmatrix} v^{inv}_q & v^{inv}_d \end{bmatrix}^T$. By definition of the inverter voltage:

$$\vec{v}_{inv} = m v_{dc} e^{j\psi} \tag{2.25}$$

The inverter voltage as shown in (2.25), is plotted at the dq axis in Fig. 2.7. From Fig. 2.7, the q and d components of the inverter voltages can be expressed as:

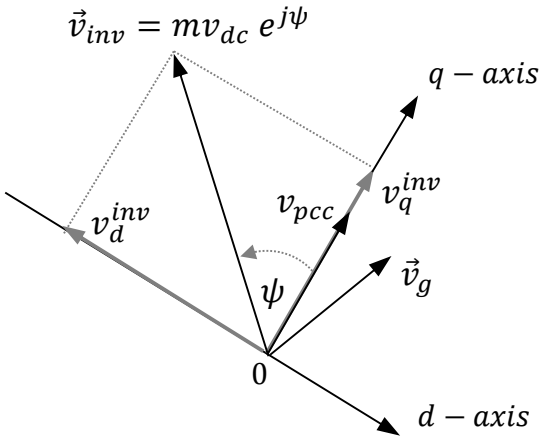


Figure 2.7: *The inverter voltage plotted at dq axis*

$$v_q^{inv} = mv_{dc}cos(\psi) \tag{2.26}$$

$$v_d^{inv} = -mv_{dc}sin(\psi) \tag{2.27}$$

Linearizing (2.26) and (2.27) and expressing them in matrix form

$$\begin{bmatrix} v_q^{inv} \\ v_d^{inv} \end{bmatrix} = \begin{bmatrix} V_{dc}cos(\Psi) & -MV_{dc}sin(\Psi) \\ -V_{dc}sin(\Psi) & -MV_{dc}cos(\Psi) \end{bmatrix} \begin{bmatrix} m \\ \psi \end{bmatrix}. \tag{2.28}$$

Using (2.28), the open-loop control inputs can be expressed in terms of the inverter voltages as follows:

$$z = M^{-1}v_{qd}^{inv} \tag{2.29}$$

The block matrix M introduced in (2.29) is provided in Appendix A.

Up to this point in the modeling process, the voltage at the PCC has been assumed as the input to the model. To study the impact of weak grids on grid-tied VSI stability, the grid impedances have to be incorporated into the system model. From Fig. 2.1, the voltage at the PCC can be expressed in terms of the grid components through KVL as:

$$\begin{bmatrix} v_{ab}^{pcc} \\ v_{bc}^{pcc} \end{bmatrix} = R_g \begin{bmatrix} i_{ab} \\ i_{bc} \end{bmatrix} + L_g \frac{d}{dt} \begin{bmatrix} i_{ab} \\ i_{bc} \end{bmatrix} + \begin{bmatrix} v_{ab}^{g} \\ v_{bc}^{g} \end{bmatrix}. \tag{2.30}$$

Using the Park's transformation matrix provided in (2.2), the equation presented in (2.30) can be expressed in the dq frame of reference as follows:

$$\begin{bmatrix} v_{q}^{pcc} \\ v_{d}^{pcc} \end{bmatrix} = \begin{bmatrix} R_g & \omega L_g \\ -\omega L_g & R_g \end{bmatrix} \begin{bmatrix} i_{qL} \\ i_{dL} \end{bmatrix} + L_g \frac{d}{dt} \begin{bmatrix} i_{qL} \\ i_{dL} \end{bmatrix} \begin{bmatrix} v_{q}^{g} \\ v_{d}^{g} \end{bmatrix}, \tag{2.31}$$

which can be expressed in block matrix form as:

$$v_{qd}^{pcc} = G_1 i_{qdL} + G_2 \frac{d}{dt} i_{qdL} + v_{qd}^{g}, \tag{2.32}$$

where, the newly introduced block matrices are included in Appendix A. Replacing the state equation for di_{qdL}/dt from (2.24) in (2.32):

$$v_{qd}^{pcc} = (I - G_2 B_{31}^{L})^{-1}(G_2 A_{31}^{L} i_{qd}^{inv} + G_2 A_{32}^{L} v_{qd}^{c} + (G_1 + G_2 A_{33}^{L}) i_{qdL} + G_2 b_3^{L} \omega + v_{qd}^{g}). \tag{2.33}$$

Combining (2.24), (2.23), and (2.16), the model of the closed-loop grid-tied VSI can be expressed as follows:

$$\frac{d}{dt} \begin{bmatrix} i_{qd}^{inv} \\ v_{qd}^{c} \\ i_{qdL} \\ y_1 \\ y_2 \\ v_{qd}^{inv} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13}^{L} & 0 & 0 & 0 \\ A_{21} & A_{22} & A_{23}^{L} & 0 & 0 & 0 \\ A_{31}^{L} & A_{32}^{L} & A_{33}^{L} & 0 & 0 & 0 \\ 0 & 0 & A_{43} & 0 & 0 & 0 \\ 0 & 0 & A_{53} & A_{54} & 0 & 0 \\ 0 & 0 & A_{63} & A_{64} & A_{65} & A_{66} \end{bmatrix} \begin{bmatrix} i_{qd}^{inv} \\ v_{qd}^{c} \\ i_{qdL} \\ y_1 \\ y_2 \\ v_{qd}^{inv} \end{bmatrix} + \begin{bmatrix} 0 & b_1 & B_{12} & 0 \\ 0 & b_2 & 0 & 0 \\ B_{31}^{L} & b_3^{L} & 0 & 0 \\ B_{41} & 0 & 0 & B_{43} \\ B_{51} & 0 & 0 & B_{53} \\ B_{61} & 0 & 0 & B_{63} \end{bmatrix} \begin{bmatrix} v_{qd}^{pcc} \\ \omega \\ z \\ R^{*} \end{bmatrix}, \tag{2.34}$$

Replacing z and v_{qd}^{pcc} through (2.29) and (2.32) in (2.34), the complete model of the grid-tied VSI is derived as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{qd}^{inv} \\ v_{qd}^{c} \\ i_{qdL} \\ y_1 \\ y_2 \\ v_{qd}^{inv} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13}^{L} & 0 & 0 & A_{16}^{c} \\ A_{21} & A_{22} & A_{23}^{L} & 0 & 0 & 0 \\ A_{31}^{c} & A_{32}^{c} & A_{33}^{c} & 0 & 0 & 0 \\ A_{41}^{c} & A_{42}^{c} & A_{43}^{c} & 0 & 0 & 0 \\ A_{51}^{c} & A_{52}^{c} & A_{53}^{c} & A_{54} & 0 & 0 \\ A_{61}^{c} & A_{62}^{c} & A_{63}^{c} & A_{64} & A_{65} & A_{66} \end{bmatrix} \begin{bmatrix} i_{qd}^{inv} \\ v_{qd}^{c} \\ i_{qdL} \\ y_1 \\ y_2 \\ v_{qd}^{inv} \end{bmatrix} + \begin{bmatrix} 0 & b_1 & 0 \\ 0 & b_2 & 0 \\ B_{31}^{c} & b_3^{c} & 0 \\ B_{41}^{c} & b_4^{c} & B_{43} \\ B_{51}^{c} & b_5^{c} & B_{53} \\ B_{61}^{c} & b_6^{c} & B_{63} \end{bmatrix} \begin{bmatrix} v_{qd}^{g} \\ \omega \\ R^{*} \end{bmatrix}, \quad (2.35)$$

where, the newly added block matrices and the modified matrices, which are denoted by the superscript c, are provided in Appendix A. The derived full-order model in (2.35) contains a detailed circuit model as well as controller and grid components, which will allow a comprehensive stability study of grid-tied VSIs.

2.4 Conclusion

In this chapter, an open-loop model for a grid-tied VSI is presented, which can be integrated with any control scheme employing both carrier-based PWM and SVPWM switching schemes. Following that, a state-space model for a PQ controller is derived and integrated with the circuit model to derive a detailed full-order state-space model for a grid-tied VSI containing filter, controller, and grid parameters. The procedure outlined in this chapter to integrate the controller model can be followed to include different controllers in the open-loop model. The full-order model derived in (2.35) is used in Chapter 3 to study the impact of VSI design parameters on the stability of grid-tied VSIs in weak grids.

Chapter 3

Stability Analysis of Grid-tied Voltage Source Inverters in Weak Grids

In this chapter, the stability analysis of a grid-tied VSI in weak grids is performed using the full-order model developed in Chapter 2. The design of various VSI parameters in weak grids is studied and several design solutions for stability are analyzed, which are enabled through the detailed full-order model in (2.35) as the model contains filter, controller, and grid parameters.

The contents of this chapter are organized into four sections. In Section 3.1, root locus studies are carried out to analyze the stability of grid-tied systems in weak grids through the design of several inverter components. The results obtained from Section 3.1 are verified through hardware tests in Section 3.2. The practicality of such design solutions is discussed in Section 3.3. Concluding remarks for this chapter are given in Section 3.4.

3.1 Root Locus Studies

In this section, the stability of a closed-loop grid-tied VSI is studied using the model developed in (2.35). In particular, the impact of a weak grid on the stability of a grid-tied VSI is analyzed through root locus of the model eigenvalues with respect to variations in VSI

Table 3.1: *Parameters employed for root locus analysis*

Parameter	Value	Parameter	Value
L_1	$1.0mH$	k_{p1}, k_{p3}	0.01
R_1	0.15Ω	k_{p2}, k_{p4}	0.5
L_2	$0.5mH$	k_{i1}, k_{i3}	2
R_2	0.1Ω	k_{i2}, k_{i4}	5
C_f	$30\mu H(\Delta)$	T_d	$0.3ms$

parameters, i.e. control time delay T_d, passive damping resistance R_f, LCL filter and PQ controller gains. The initial values of the parameters are provided in Table 3.1. In addition, the coupling path gain in the PQ controller is set to a constant value of $\omega L = 0.575\Omega$. The controller proportional gains K_ps are chosen based on the remaining system parameters, deliberately with a slight margin from the unstable region for the stability study using root locus. No passive damping resistance is initially considered with the equivalent series resistance (ESR) of the LCL filter film capacitors is modeled by setting $R_f = 0.008\Omega$ for the frequency range of the case studies presented in this section. Moreover, in Table 3.1, a higher value is considered for R_1 than R_2, to account for the on-state switching resistances of the semiconductor switches.

In the first scenario, the stability of the grid-tied VSI system is studied for an increase in grid impedance. The X/R ratio of the grid for transmission systems is usually much larger than one, i.e. $X/R >> 1$, as the grid resistance is negligible compared to the grid inductance in such systems. In low-voltage distribution grids, the X/R ratio is usually around one as the grid resistance becomes comparable to the inductance [74]. The line impedance is mostly resistive in islanded microgrids. As a result, the X/R ratio can become as low as 0.2 [75]. In the scenario presented in Fig. 3.1, the root locus of the systems poles (eigenvalues) is shown as X/R ratio is gradually increased from 0.5 to 5 through an increase in grid inductance L_g from $0.16mH$ to $1.6mH$ while the grid inductance R_g is kept constant at 0.12Ω. As one can see from Fig. 3.1, increasing L_g drives a pair of poles (λ_3, λ_4) toward the unstable region while the remaining poles stay in the stable region. A zoomed-in plot of the dominant eigenvalues is shown in Fig. 3.1 (right). As highlighted in the zoomed-in plot of Fig. 3.1,

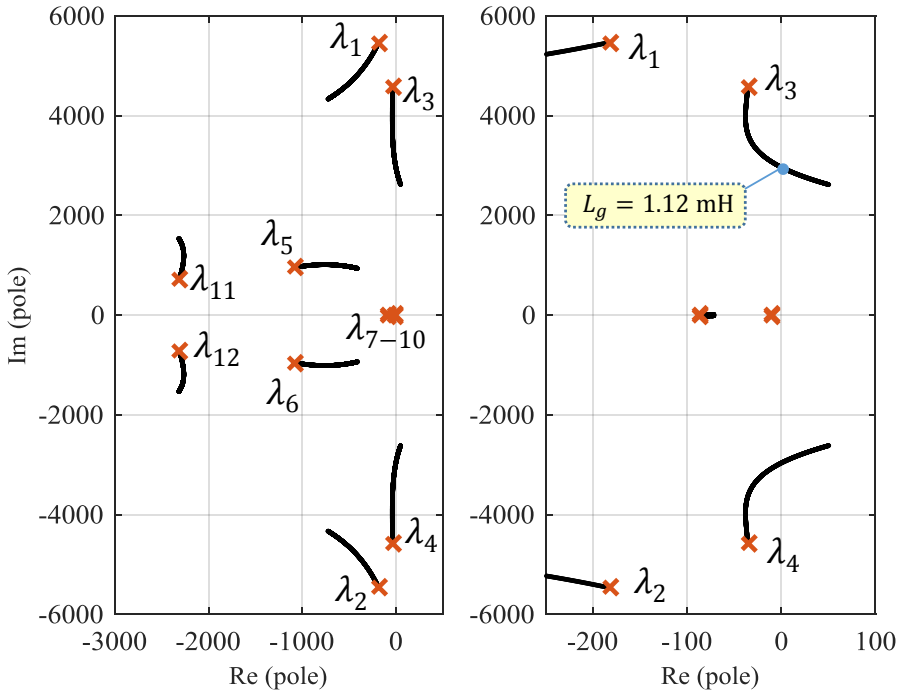


Figure 3.1: *The root locus of the grid-tied VSI when L_g varies from $0.16mH$ to $1.6mH$ and $R_g = 0.12\Omega$ is kept constant (left), with a zoomed-in plot of the dominant poles (right).*

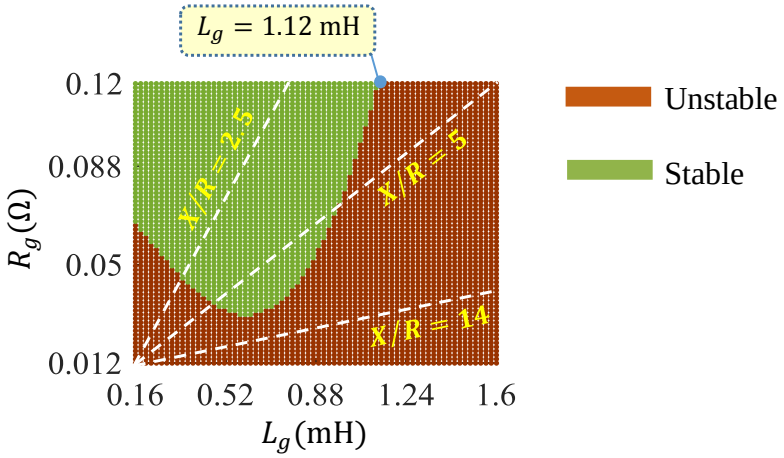


Figure 3.2: *The stable and unstable regions of grid-tied VSI with respect to grid resistance and inductance values for the parameters provided in Table 3.1.*

the poles move to the right-half plane for $L_g > 1.12mH$, i.e. $X/R > 3.5$, thereby making the system unstable. On the other hand, if instead the X/R ratio is increased from 0.5 to 5 by decreasing R_g from 0.12Ω to 0.012Ω, when $L_g = 0.16mH$, the system becomes stable

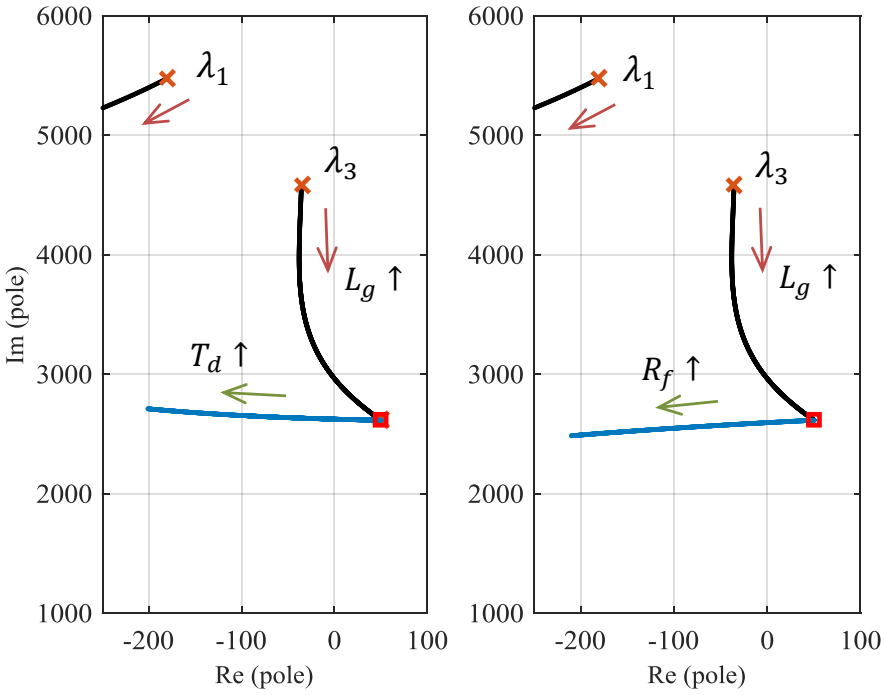


Figure 3.3: *The root loci of* λ_3 *as initially* L_g *increases from* $0.16mH$ *to* $1.6mH$ *followed by an increase in* T_d *from* $0.3ms$ *to* $0.4ms$ *(left), an increase in* R_f *from* 0.008Ω *to* 2Ω.

for $R_g > 0.064$ as shown in Fig. 3.2. It can also be seen from Fig. 3.2 that for the same X/R ratio, the stability of the system can depend on both L_g and R_g values. Therefore, the weakness of a grid is determined by both L_g and R_g.

An increase in time delay of the feedback control path can improve the stability of grid-tied systems when current measurement is performed after the LCL filter [73]. Similarly, increasing passive damping resistances can have a positive impact on the stability of VSIs [41]. To demonstrate the impact of these parameters in weak grids, the root loci of one of the dominant poles, i.e. λ_3, is plotted in Fig. 3.3 for two different scenarios. In the scenario plotted in Fig. 3.3 (left), the root loci is shown as L_g is increased from $0.16mH$ to $1.6mH$, followed by an increase in T_d from $0.3ms$ to $0.4ms$. As one can see from Fig. 3.3 (left), for a larger T_d the grid-tied system can remain stable in weak grids. In the scenario presented in Fig. 3.3 (right), the root loci of the dominant pole is plotted for the same increase in L_g, followed by an increase in R_f from 0.008Ω to 2Ω. Similar to the case of T_d, an increase in

R_f improves the stability of grid-tied VSIs in weak grids as can be seen from the root loci illustrated in Fig. 3.3 (right). It should be noted that the same stabilizing impact of T_d is not applicable when current measurement is conducted at the inverter-side, that is before the capacitor branch.

The controller gains for the control scheme are generally chosen considering the dynamic performance and stability of the system. As can be seen from Fig. 2.6, the PQ controller contains four proportional gains K_ps and four integrator gains K_is corresponding to the four PI control loops present in the control scheme. However, for a wide range of variations in the K_i values, the eigenvalues remain relatively constant and in the stable region. Whereas the dynamic performance of the system, e.g. settling time, steady-state error, are impacted by the K_i gains. Moreover, the root locus of the poles shows similar characteristic with variations in the outer power loop proportional gains k_{p1} and k_{p3}, while the inner current loop proportional gains k_{p2} and k_{p4} also exhibit similar characteristic. With these remarks in

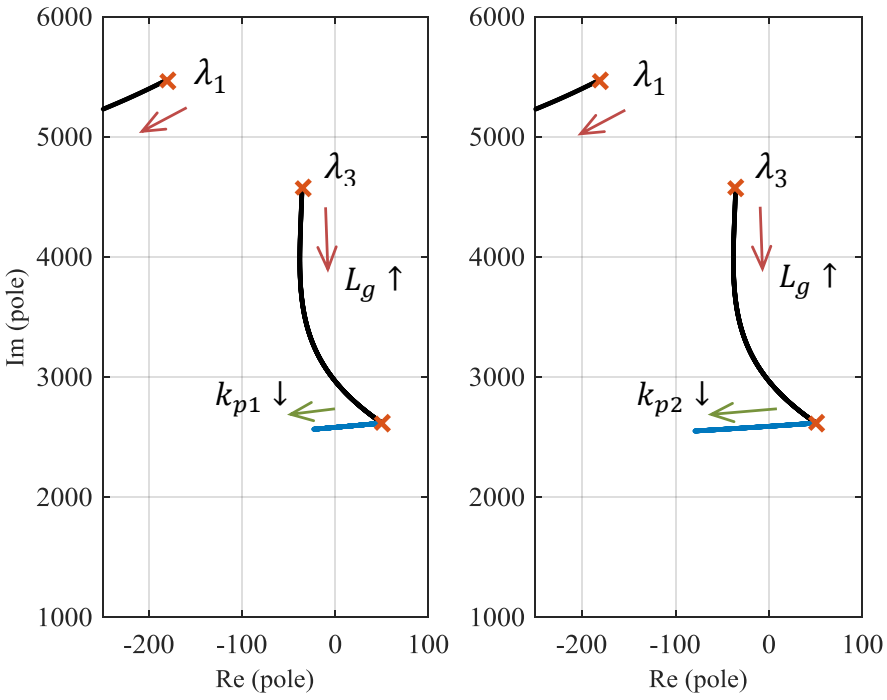


Figure 3.4: *The root loci of λ_3 as initially L_g increases from $0.16mH$ to $1.6mH$ followed by a decrease in k_{p1} from 0.01 to 0.001 (left), a decrease in k_{p2} from 0.5 to 0.05 (right).*

mind, to study the effect of controller gains on the stability of grid-tied VSIs in weak grids, the root loci of λ_3 is plotted in Fig. 3.4 as L_g is increased from $0.16mH$ to $1.6mH$, following which k_{p1} is varied from 0.01 to 0.001 (left) and k_{p2} is decreased from 0.5 to 0.05 (right). As one can see from Fig. 3.4, the root loci of the pole move to the stable region as the K_ps are decreased. Therefore, a grid-tied system can be operated in the stable region under weak grids, by decreasing the K_p gains.

The traditional LCL filter design procedures do not consider the grid impedance. The maximum boundary of $L_1 + L_2$ is commonly determined for a voltage drop of 0.02 to 0.05 *p.u.* across the filters. The lower and upper bounds of L_1 can also be obtained by limiting the maximum current ripple of the inverter-side inductor in one cycle, while for optimum LCL filter performance and to satisfy the harmonic restriction standards such as IEEE Std. 1547, $L_1 \geq L_2$ is usually selected [76]. The PWM frequency and C_f can be chosen to avoid the inverter output circuit resonance frequency. In addition, a capacitor value of less than 3%

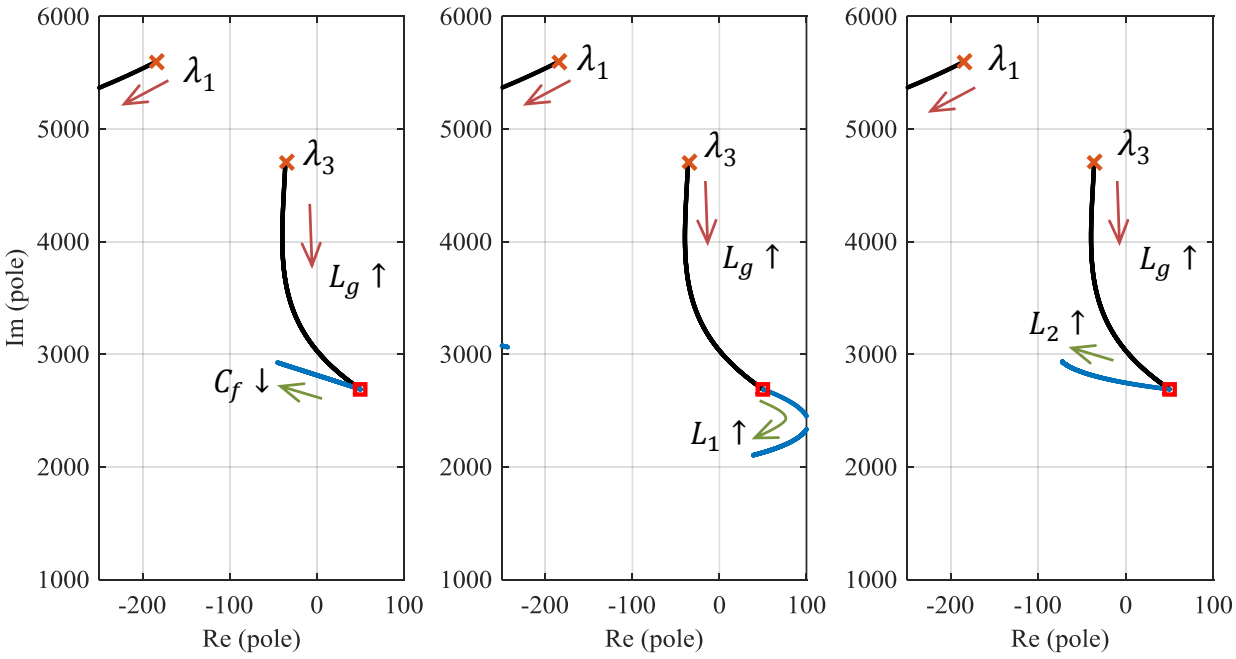


Figure 3.5: *The root loci of λ_3 as initially L_g increases from $0.16mH$ to $1.6mH$ followed by a decrease in C_f from $30\mu H$ to $25\mu H$ (left), an increase in L_1 from $1mH$ to $5mH$ (middle), an increase in L_2 from $0.5mH$ to $5mH$ (right).*

of its base impedance value is commonly chosen to limit the decrease in the power factor of grid-tied VSIs [77]. The above-mentioned criteria might be valid for grid-tied VSIs operating in stiff grids but might result in instability under weak grids. The effect of filter parameters on system stability in weak grids is demonstrated in Fig. 3.5. Three cases are depicted in Fig. 3.5, where initially L_g is increased from $0.16mH$ to $1.6mH$ in all three cases. In the root loci shown in Fig. 3.5 (left), C_f is decreased from its initial value of $30\mu H$ to $25\mu H$, which moves the dominant pole of the system to the stable region. Therefore, stability can be achieved in weak grids by designing a smaller C_f value. In the scenario illustrated in Fig. 3.5 (middle), the value of L_1 increases from $1mH$ to $5mH$. Even though the dominant pole is seen to be moving towards the stable region, the system remains unstable for a large increase in L_1 in a weak grid. In the third scenario shown in Fig. 3.5 (right), L_2 is increased from its initial value of $0.5mH$ to $5mH$. As one can see from the root loci presented in Fig. 3.5 (right), increasing L_2 moves the dominant pole to the stable region. Although from an open-loop circuit point of view L_2 and L_g seem to be connected in series, as the current measurement is conducted from the point between them (see Fig. 2.6) their impact on system stability seem to be opposite, where increasing L_2 is beneficial for system stability in weak grids. It should be noted that the stabilizing effect of L_2 is valid only for grid-side current measurement.

3.2 Experimental Verification

In this section, some of the findings obtained through the root locus analysis in Section 3.2 is verified through laboratory experiments. The same parameters provided in Table 3.1 was employed for the hardware tests except for the integrator gains, which were set to a small value of 0.002 to avoid overshoots that could damage the laboratory equipment. A schematic of the hardware setup used in this section is illustrated in Fig. 3.6. A more detailed description of the setup can be found in Subsection 2.1.2.

In the first test scenario, the impact of a weak grid on grid-tied VSI stability is demonstrated. Three-phase $5mH$ inductors were inserted to the circuit between the PCC and the

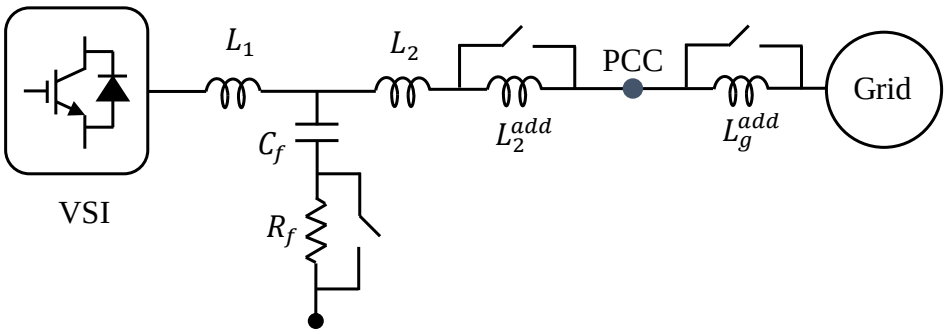


Figure 3.6: *Schematic diagram of the hardware setup employed in Section 3.2.*

point of grid connection, which were initially bypassed through a three-phase circuit breaker as shown in Fig. 3.6. The line current of phase-A is displayed in Fig. 3.7, as the grid inductance was inserted at instant $0.1s$. As one can see from Fig. 3.7, the grid-tied system becomes unstable, as the grid gets weaker due to a large grid impedance.

Two test scenarios are displayed in Fig. 3.8, with the operating points also highlighted in the root locus plot presented in Fig. 3.9, using the model developed in Chapter 2. In both the scenarios presented in Fig. 3.8, the system is initially seen to be stable (Point A in Fig. 3.9). The system then became unstable when line inductors were added to the grid impedance at instant $t = 0.1s$ (Point C in Fig. 3.9). In Fig. 3.8 (top), the system becomes stable again as three-phase inductors, $L_2^{add} = 2.5mH$, were inserted at the inverter-side of the PCC through opening a circuit breaker as shown in Fig. 3.6, which increases the value of L_2 to $3mH$ (Point D in Fig. 3.9). Hence, increasing L_2 indeed improves the stability in weak grids when grid-side current measurement is employed, as discussed in Section 3.1 and also in the root loci plot of the dominant pole shown in Fig. 3.9. Notice that the magnitude of the current is initially smaller upon returning to the stable region in Fig. 3.8 (top) due to the sudden increase in filter inductance. The controller then slowly restores the current to its original value, which is not apparent from the figure as a small time period is displayed to highlight the stability phenomenon. In Fig. 3.8 (bottom), the unstable system is brought back to the stable region by inserting a R_f of 10Ω through opening a circuit breaker at instant $t = 0.29s$ (Point E in Fig. 3.9). The scenario in Fig. 3.8 (bottom) is also displayed in the scope screen in Fig. 3.10 along with the test setup. These tests validate the efficacy of

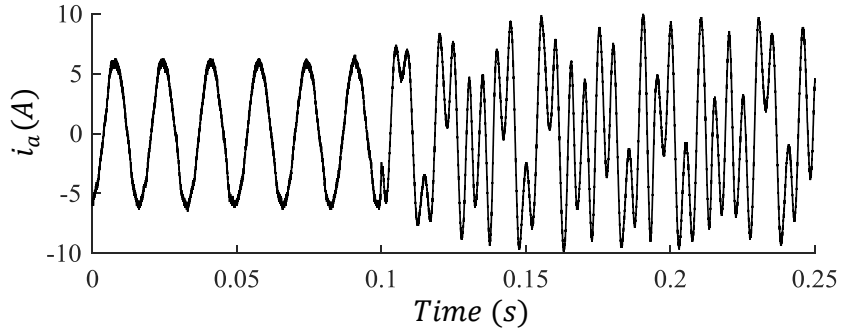


Figure 3.7: *Line current injected to the grid when at instant* $0.1s$ *a* $5mH$ *inductor is added per phase to the grid impedance.*

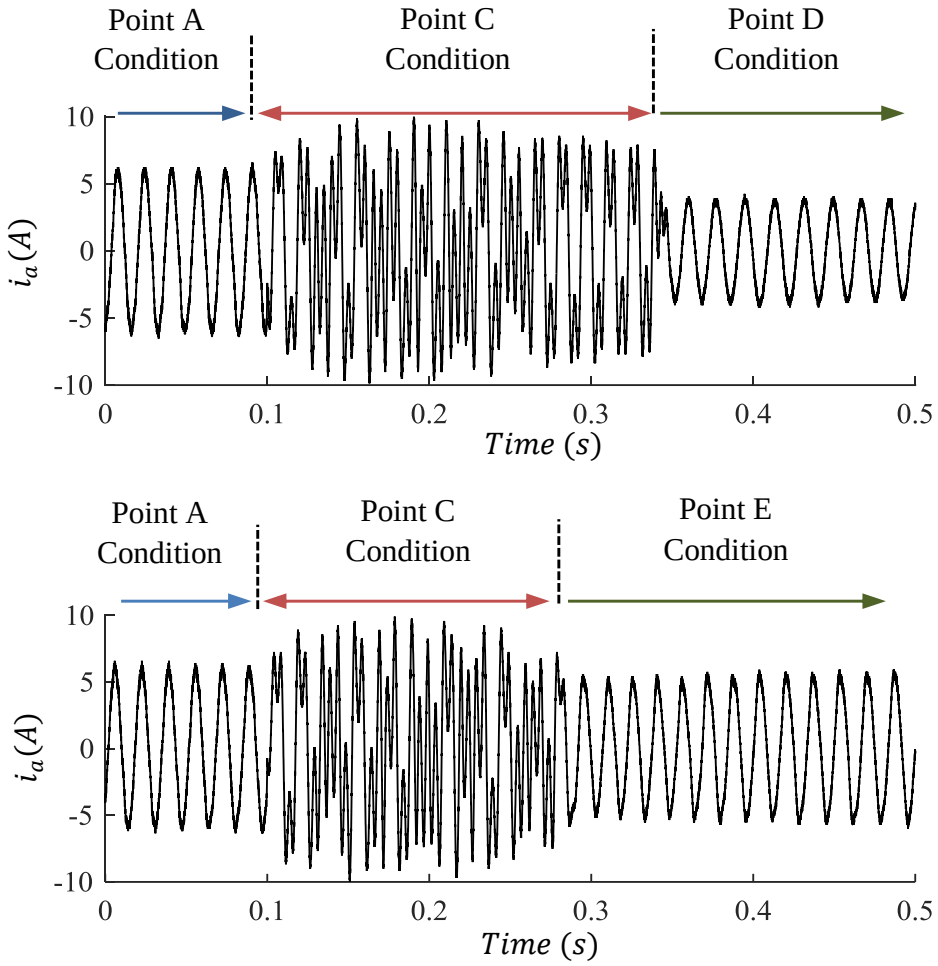
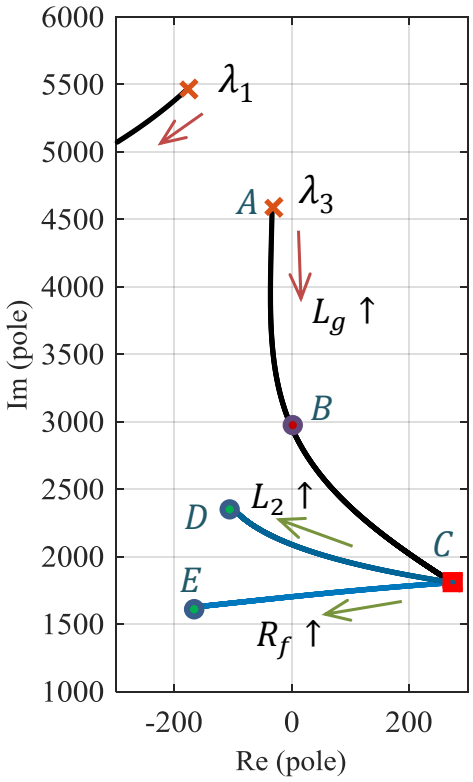


Figure 3.8: *Line current injected to the grid when a grid inductance of* $5mH$ *is added at instant* $0.1s$ *followed by the insertion of a* L_2 *of* $2.5mH$ *at instant* $0.33s$ *(top), the insertion of a* R_f *of* 10Ω *at instant* $0.29s$ *(bottom).*



Point A	$L_g = 0.16\,mH$
$\lambda_{3,4}$	$-33 \pm j4585$
Point B	$L_g = 1.12\,mH$
$\lambda_{3,4}$	$0 \pm j2958$
Point C	$L_g = 5\,mH$
$\lambda_{3,4}$	$274 \pm j1808$
Point D	$L_2 = 3\,mH$
$\lambda_{3,4}$	$-97 \pm j2346$
Point E	$R_f = 10\,\Omega$
$\lambda_{3,4}$	$-161 \pm j1629$

Figure 3.9: *Root loci of the dominant pole λ_3 with the system being initially stable at point A, following which L_g increases to $5mH$ at point C, followed by (i) an increase in L_2 up to $3mH$ at point D, (ii) an increase in R_f up to 10Ω at point E.*

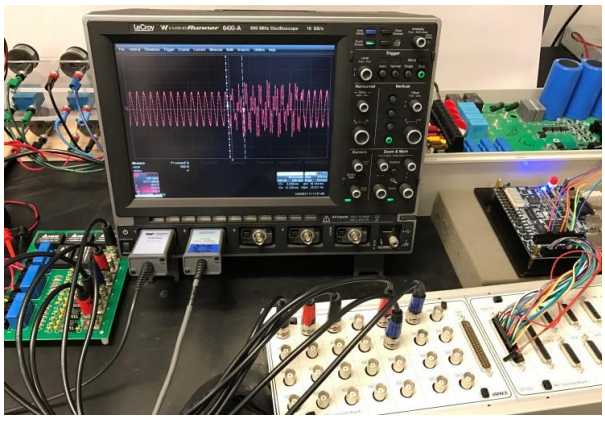


Figure 3.10: *Experimental setup for Section 3.2 along with the scope display for the case study demonstrated in Fig. 3.8 (bottom).*

the developed model presented in (2.35) for the stability analysis of grid-tied VSIs in weak grids.

3.3 Practicality of VSI Design Parameters in Stability Improvement

The design criteria for several VSI parameters are studied through the root locus analysis in Section 3.2 to improve the stability of grid-tied VSIs in weak grids. Some of the findings are also verified experimentally in Section 3.3. However, there is a tradeoff in implementing each of the findings.

As already mentioned in Section 3.2, the filter inductances are designed allowing a maximum voltage drop of around 0.05 $p.u.$ across them. Increasing L_2 to improve stability could violate this criterion. Furthermore, a bigger inductance means more cost and an increase in the size of the inverter unit. On the other hand, decreasing C_f could improve the stability in weak grids. However, a smaller C_f could decrease the harmonic rejection capability of the LCL filter, which will result in an increased total harmonic distortion (THD).

Although an increase in the passive damping resistance R_f can improve the stability of grid-tied VSIs, the introduction of a resistive element in the system will increase the losses and decrease the efficiency of the inverter unit. Moreover, a resistive element in the capacitive branch of the LCL filter could reduce the efficacy of the filter in eliminating high-frequency harmonics.

The dynamic performance of the system depends on the proportional gains of the controller and decreasing the proportional gains will inevitably result in slower controller dynamics, although the stability of the system may improve. The same is true for the control time delay T_d, as increasing T_d has a positive effect on system stability but at the cost of a slower dynamic response.

The filter and controller parameters can be designed to enable stable operation of VSIs in weak grids, however, performance criteria of VSIs may not be satisfied under all operating

scenarios. Therefore, there is a need for novel techniques for stability improvement of grid-tied VSIs in weak grids.

3.4 Conclusion

In this chapter, several VSI parameters have been identified, through root locus analysis of the eigenvalues of the full-order model, that can be designed to improve the stability of VSIs in weak grids. The efficacy of some of the design parameters has been experimentally verified. The drawbacks of implementing the various design criteria have also been discussed. Based on the analysis carried out in this section, a virtual inductance feedforward emulating the behavior of an additional L_2 in the LCL filter is presented in this dissertation, which is discussed in details in the next chapter.

Chapter 4

Virtual Inductance Feedforward Scheme

In this chapter, a virtual inductance feedforward control technique is developed to enable stable operation of VSIs in weak grids. The virtual inductance feedforward path is integrated to the inner current loops of the PQ controller. A larger grid-side inductor L_2 could improve the stability of grid-tied VSIs in weak grids, as verified through root locus analysis and hardware tests in Chapter 3. The virtual inductance feedforward scheme is derived in this chapter emulating the behavior of an additional L_2 without the drawbacks associated with an increased L_2, i.e. additional voltage drop, larger size, and higher cost, while retaining its stabilizing effect. The implementation of the developed technique does not require any additional hardware components, e.g. sensors, and does not affect the steady-state performance of the system.

The contents of this chapter are organized into six sections. In Section 4.1, an analytical expression is derived to demonstrate the stabilizing impact of L_2 in weak grids. The virtual inductance term emulating an additional L_2 is derived in Section 4.2. A modified control scheme for grid-tied VSIs is developed in Section 4.3 by integrating the virtual inductance feedforward in the PQ controller. The efficacy of the presented technique is validated through root locus analysis in Section 4.4. The performance of the developed scheme is compared

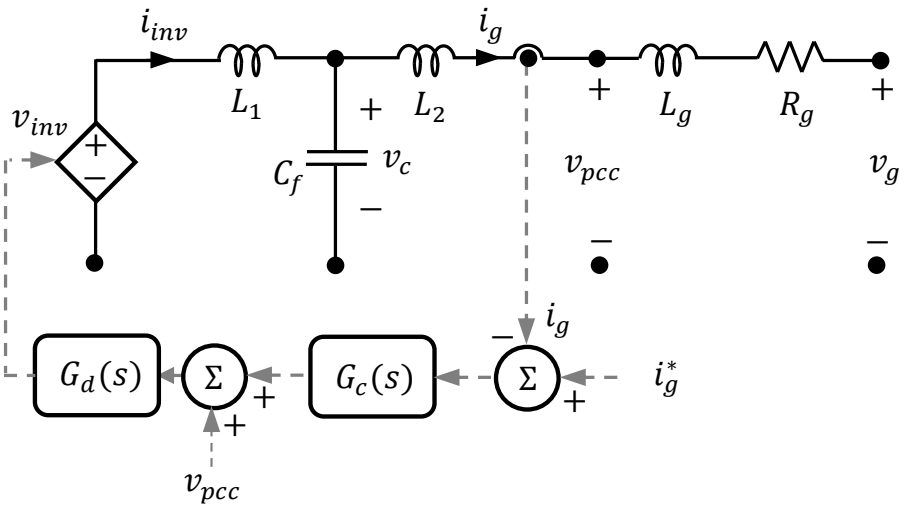


Figure 4.1: *Simplified schematic diagram of one phase of a current-controlled grid-tied VSI.*

against controller design procedures in Section 4.5. The virtual inductance feedforward scheme is verified through experimental scenarios in Section 4.6. Finally concluding remarks for this chapter are provided in Section 4.7.

4.1 Effect of Filter Inductance on Stability

In this section, an analytical equation expressing the impact of filter inductances on the stability of grid-tied VSIs in weak grids is derived through continued-fraction-expansion of the system transfer function based on a simplified grid-tied VSI model. The simplified schematic of an individual phase of a balanced VSI considered in this section is shown in Fig. 4.1.

The inverter unit is represented by a controlled voltage source in Fig. 4.1. The grid-tied system employs a current controller, which is expressed through the transfer function $G_c(s)$ and is equipped with the PCC voltage feedforward. Same notations used in the previous chapters is also used in Fig. 4.1 to represent the LCL filter and grid parameters as well as the voltage and current components of the circuit. The input to the controller is considered to be the desired grid current i_g^*.

Applying KVL on the loops on both sides of C_f, the voltages can be written as follows:

$$-v_{inv} + L_1 \frac{d}{dt} i_{inv} + v_c = 0, \tag{4.1}$$

$$-v_c + L_2 \frac{d}{dt} i_g + v_{pcc} = 0. \tag{4.2}$$

Also, v_{pcc} can be written in terms of v_g through KVL as follows:

$$v_{pcc} = R_g i_g + L_g \frac{d}{dt} i_g + v_g. \tag{4.3}$$

Applying KCL at the capacitor node, the current flowing through the capacitor branch can be expresses as follows:

$$C_f \frac{d}{dt} v_c = i_{inv} - i_g. \tag{4.4}$$

Substituting v_{pcc} from (4.3) to (4.2) and transferring to s-domain yield:

$$sI_g = \frac{V_c}{L_2 + L_g} - \frac{V_g}{L_2 + L_g} - \frac{R_g I_g}{L_2 + L_g}. \tag{4.5}$$

From Fig. 4.1, the inverter voltage can also be expressed in the s-domain in terms of the control variables as follows:

$$V_{inv} = G_d(V_{pcc} + G_c(I_g^* - I_g)). \tag{4.6}$$

Replacing V_{pcc} from (4.3), following conversion to the s-domain, and sI_g from (4.5) in (4.6) yield:

$$V_{inv} = G_d\left(\frac{L_g V_c + L_2 V_g}{L_2 + L_g} + (\frac{R_g L_2}{L_2 + L_g} - G_c) I_g + G_c I_g^*\right). \tag{4.7}$$

Replacing V_{inv} from (4.7) in (4.1) in s-domain yields:

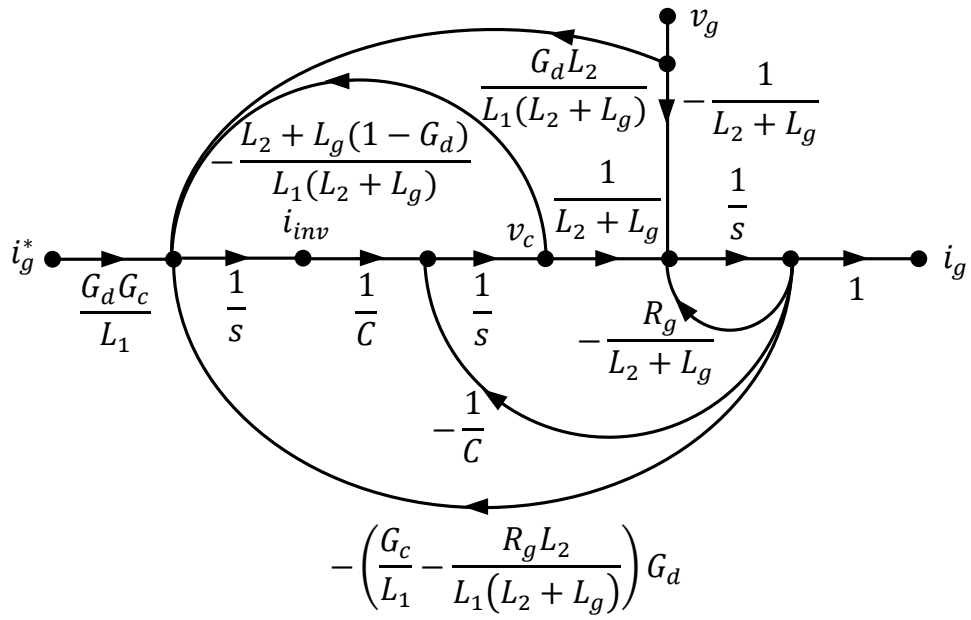


Figure 4.2: *A signal flow graph of the grid-tied VSI presented in Fig. 4.1.*

$$sI_{inv} = -\frac{L_2 + L_g(1-G_d)}{L_1(L_2+L_g)}V_c + \left(\frac{G_d R_g L_2}{L_1(L_2+L_g)} - \frac{G_d G_c}{L_1}\right)I_g + \frac{G_d L_2}{L_1(L_2+L_g)}V_g + \frac{G_d G_c}{L_1}I_g^*. \quad (4.8)$$

Following transformation into s-domain, (4.4) can be expressed as follows:

$$sV_c = \frac{1}{C_f}I_{inv} - \frac{1}{C_f}I_g. \quad (4.9)$$

Using (4.9), (4.8), and (4.5), a lossless signal flow graph of the simplified grid-tied VSI is obtained, which is illustrated in Fig. 4.2. The inputs to the signal flow graph are I_g^* and V_g, while the output is the current supplied to the grid I_g. Now, applying Mason's rule on the signal flow graph presented in Fig. 4.2, a transfer function of the grid-tied system is derived, i.e. $H(s) = I_g(s)/I_g^*(s) = N(s)/D(s)$, where,

$$N(s) = G_c(s)G_d(s), \quad (4.10)$$

$$D(s) = s^3 L_1 C_f (L_2 + L_g) + s^2 L_1 C_f R_g + s(L_1 + L_2 + L_g(1 - G_d(s))) + G_c(s)G_d(s) + R_g(1 - G_d(s)). \tag{4.11}$$

The denominator $D(s)$ is then expressed in a form suitable for continued-fraction-expansion as follows:

$$\frac{D_1(s)}{D_2(s)} = \frac{s^3 L_1 C_f (L_2 + L_g) + s(L_1 + L_2 + L_g(1 - G_d(s)))}{s^2 L_1 C_f R_g + G_c(s)G_d(s) + R_g(1 - G_d(s))}, \tag{4.12}$$

where, the term $D_1(s)$ contains the highest power coefficient and the following alternate power coefficients of $D(s)$, while $D_2(s)$ contains the remaining power coefficients. Now, applying repeated long division on (4.12), three criteria for the stability of this system can be determined using the continued-fraction-expansion method as follows: (i) $(L_2 + L_g) > 0$, (ii) $L_1 C_f R_g^2 > 0$, and (iii) $R_g(L_1 + L_2 G_d(s)) - (L_2 + L_g)G_d(s)G_c(s) > 0$. As circuit parameters are physical quantities and therefore positive, only the inequality present in the third criterion can be used to extract some information on system stability. Moreover, the control delay can be expressed as $G_d(s) = e^{-sT_d}$ for systems operating in continuous domain [73], which has a magnitude of $|G_d(s)| = 1$. The inequality in the third criterion can then be re-written as follows:

$$\frac{L_1 + L_2}{L_g + L_2} R_g > |G_c(j\omega)|. \tag{4.13}$$

From (4.13), it can be interpreted that for a given control gain, i.e. $|G_c(j\omega)$, a higher L_g will result in a lower stability margin. This is in agreement with the analysis carried out in Chapter 3. One can also interpret from (4.13) that increasing $L_1 + L_2$ can result in a higher stability margin. However, this will be an improper hardware solution as discussed in 3.3. Herein, two extreme cases are considered as follows: (i) stiff grids when $L_g \ll L_2$ and (ii) weak grids when $L_g \gg L_2$. It should be noted that in resistive standalone microgrids, the line impedance could be predominantly resisitive [74, 78], as a result the abovementioned second case may not be valid even if the connection at the PCC is weak. However, the focus of this dissertation is on grid-tied applications, therefore the second case mentioned

above is a sufficient condition for weak grids in both inductive and resistive-inductive grid connections. Now, considering the two cases, the inequality expression in (4.13) can be re-written as follows:

$$\begin{cases} (1+\frac{L_1}{L_2})R_g > |G_c(j\omega)| & \text{for stiff grids,} \\ (L_1+L_2)(\frac{R_g}{L_g}) > |G_c(j\omega)| & \text{for weak grids.} \end{cases} \tag{4.14}$$

As one can see from (4.14), only under weak grids, an LCL filter with a slightly higher value of L_2 can be designed to improve the stability of the grid-tied system. Instead, a control solution emulating the impact of an additional inductance is presented in this dissertation to avoid the tradeoff associated with a physical increase in the inductance value.

4.2 Derivation of Virtual Inductance

In this section, a virtual inductance term to enable stable operation of grid-tied VSIs is derived. To virtually represent the impact of an additional L_2, the current going through L_2, which is the grid current i_g, is utilized. From (4.14), it can be interpreted that an additional L_1 could also contribute towards the stable operation of grid-tied VSIs. However, the current going through L_1, i.e. i_{inv}, is not a measured quantity as can be seen from the detailed schematic of the grid-tied VSI illustrated in Fig. 2.6. As a result, the implementation of a virtual inductance term representing L_1 would require an additional sensor to measure i_{inv}. The passive damping resistance R_f can also be utilized to improve the stability of grid-tied VSIs as discussed in Chapter 3 and active damping strategies based on virtual R_f can be found in literature [79–82]. However, development of virtual R_f may require (i) an additional sensor measuring the voltage or current of the filter capacitor [79–81], (ii) complicated capacitor current estimation strategies [82]. Therefore, a virtual inductance emulating L_2 is the preferred choice.

A schematic diagram of a VSI focusing on the effect of grid-side LCL filter inductance is shown in Fig. 4.3. The grid-side inductor is denoted as L_{vir} for analysis purposes. The

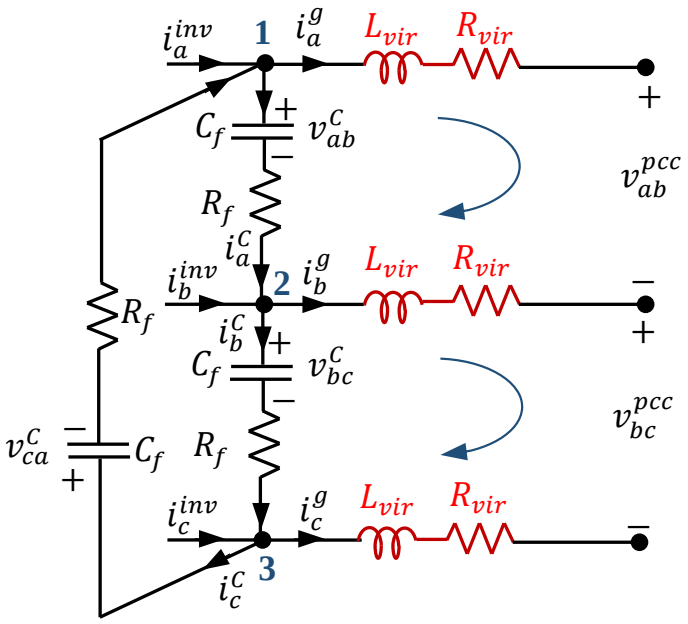


Figure 4.3: *Schematic diagram of a three-phase VSI focusing on the effect of filter inductance on the grid-side, which will be added virtually.*

resistor R_{vir} shown in Fig. 4.3 denotes the parasitic resistance of the inductor. Performing KVL on the two loops shown in Fig. 4.3, the following equations can be written:

$$-v_{ab}^c + L_{vir}\frac{d}{dt}(i_a^g - i_b^g) + R_{vir}(i_a^g - i_b^g) + v_{ab}^{pcc} - R_f i_a^c = 0, \tag{4.15}$$

$$-v_{bc}^c + L_{vir}\frac{d}{dt}(i_b^g - i_c^g) + R_{vir}(i_b^g - i_c^g) + v_{bc}^{pcc} - R_f i_b^c = 0. \tag{4.16}$$

Performing KCL on the numbered nodes shown in Fig. 4.3, the currents in the capacitor branch can be expressed in terms of the line currents as follows:

$$i_a^c = \frac{i_a^{inv} - i_a^g - i_b^{inv} + i_b^g}{3}, \tag{4.17}$$

$$i_b^c = \frac{i_b^{inv} - i_b^g - i_c^{inv} + i_c^g}{3}. \tag{4.18}$$

Substituting the values of i_a^c and i_b^c from (4.17) and (4.18) into (4.15) and (4.16), respectively, the equations can be expressed as follows:

$$-v_{ab}^{c}+L_{vir}\frac{d}{dt}(i_{a}^{g}-i_{b}^{g})+(R_{vir}+\frac{R_f}{3})(i_{a}^{g}-i_{b}^{g})+v_{ab}^{pcc}-\frac{R_f}{3}(i_{a}^{inv}-i_{b}^{inv})=0, \tag{4.19}$$

$$-v_{bc}^{c}+L_{vir}\frac{d}{dt}(i_{b}^{g}-i_{c}^{g})+(R_{vir}+\frac{R_f}{3})(i_{b}^{g}-i_{c}^{g})+v_{bc}^{pcc}-\frac{R_f}{3}(i_{b}^{inv}-i_{c}^{inv})=0. \tag{4.20}$$

Isolating the currents going through the virtual inductances, the effect of virtual inductance on the virtual line-to-line currents can be written as follows:

$$i_{ab}^{vir}=i_{ab}^{g}=\frac{1}{3R_{vir}}(-3v_{ab}^{c}-R_f i_{ab}^{g}-3v_{ab}^{pcc}+R_f i_{ab}^{inv}-3L_{vir}i_{ab}^{g}), \tag{4.21}$$

$$i_{bc}^{vir}=i_{bc}^{g}=\frac{1}{3R_{vir}}(-3v_{bc}^{c}-R_f i_{bc}^{g}-3v_{bc}^{pcc}+R_f i_{bc}^{inv}-3L_{vir}i_{bc}^{g}). \tag{4.22}$$

Since, only the high frequency component of the current flows through the capacitor branch, it can be assumed that $i_{ab}^{g}\approx i_{ab}^{inv}$ and $i_{bc}^{g}\approx i_{bc}^{inv}$ by considering only the fundamental current components. In addition, it can be assumed that $v_{ab}^{c}\approx v_{ab}^{pcc}$ and $v_{bc}^{c}\approx v_{bc}^{pcc}$ as the equivalent impedances of the filter components are very small. Applying the abovementioned simplifications, (4.21) and (4.22) can be written as follows:

$$i_{ab}^{vir}=-\frac{L_{vir}}{R_{vir}}\frac{d}{dt}i_{g}^{a}, \tag{4.23}$$

$$i_{bc}^{vir}=-\frac{L_{vir}}{R_{vir}}\frac{d}{dt}i_{g}^{b}. \tag{4.24}$$

The next step is to convert the virtual inductance terms to quantities in the dq frame of reference as the controller operates in the synchronously rotating dq frame as shown in Fig. 2.6. Applying the Park's transformation provided in (2.2) on (4.23) and (4.24), the virtual inductance terms can be expressed in a matrix form in the dq frame as follows:

$$\begin{bmatrix} i_{q}^{vir} \\ i_{d}^{vir} \end{bmatrix}=-\frac{L_{vir}}{R_{vir}}\frac{d}{dt}\begin{bmatrix} i_{q}^{g} \\ i_{d}^{g} \end{bmatrix}-\frac{L_{vir}}{R_{vir}}\begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} i_{q}^{g} \\ i_{d}^{g} \end{bmatrix}. \tag{4.25}$$

The derivative terms have minimal impact on steady-state operation, as a result they can

be neglected for simplification. Furthermore, the term R_{vir} just acts as an inverse gain and is set to 1. The virtual inductance terms in the dq frame of reference can then be expressed as follows:

$$i_q^{vir} = -\omega L_{vir} i_d^g, \tag{4.26}$$

$$i_d^{vir} = \omega L_{vir} i_q^g. \tag{4.27}$$

It can be seen from (4.26) and (4.27) that the derived virtual inductance strategy (i) requires the tuning of only one parameter and (ii) can be expressed only in terms of the grid currents, hence no additional sensors are required. Therefore, the presented virtual inductance strategy is a more practical solution compared to existing techniques present in the literature for improving the stability in weak grids [26, 36, 37].

4.3 Control Scheme with Virtual Inductance

In Section 4.2, a virtual inductance term is derived, as shown in (4.26) and (4.27), based on the virtual line-to-line grid currents. Therefore, the virtual inductance terms should be integrated to the current control loops of the VSI controller. The modified PQ controller including the virtual inductance is shown in Fig. 4.4. As one can see from Fig. 4.4, the virtual inductance scheme is implemented using feedforward virtual line-to-line grid current components fed through the virtual inductance gain block.

The controller model presented in Section 2.2 has to be modified to include the virtual inductance feedforward. As discussed in Section 2.1, the open-loop model has a generalized structure, therefore it can integrated with the modified controller model without any alterations. In addition, the virtual inductance feedforward is incorporated in the inner current control loops. As a result, the state equations corresponding to y_P and y_Q will remain unchanged, which are provided in (2.6) and (2.7), respectively. The modified state equations associated with y_{iq} and y_{id} can be expressed as follows:

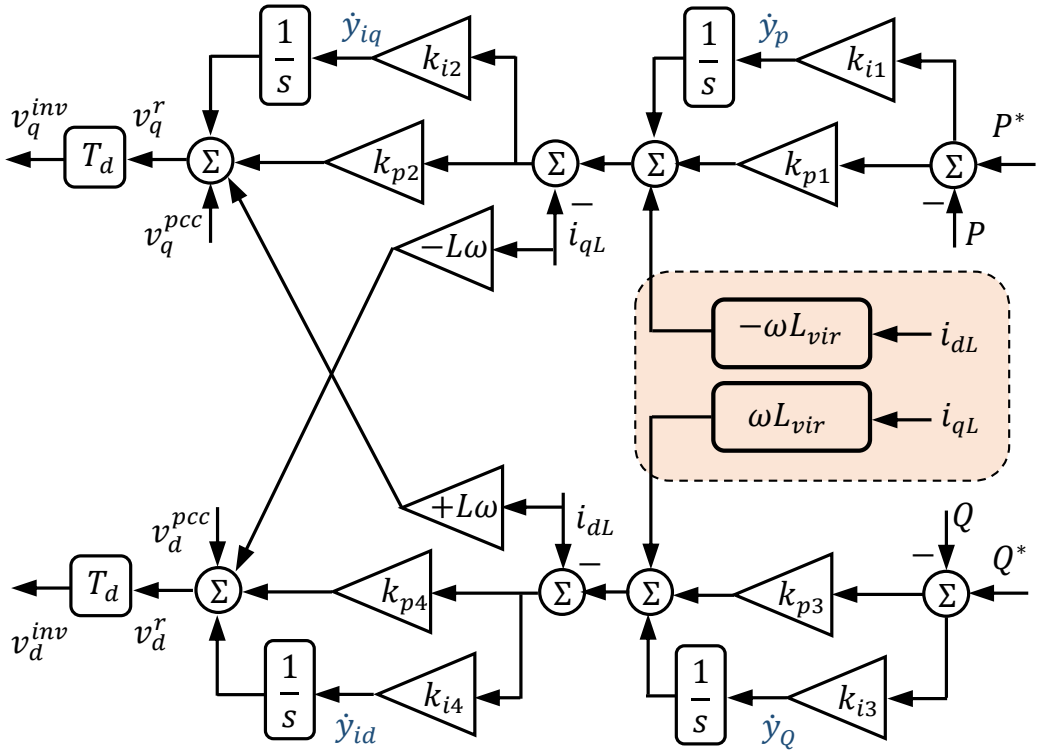


Figure 4.4: *Modified control scheme of a grid-tied VSI equipped with virtual inductance feedforward (highlighted).*

$$\dot{y}_{iq} = k_{i2}y_P - k_{i2}(\frac{1}{2}k_{p1}V_q^{pcc} + 1)i_{qL} - k_{i2}\omega L_{vir}i_{dL} + k_{i2}k_{p1}P^* - \frac{1}{2}k_{i2}k_{p1}I_{qL}v_q^{pcc} - \frac{1}{2}k_{i2}k_{p1}I_{dL}v_d^{pcc}, \tag{4.28}$$

$$\dot{y}_{id} = k_{i4}y_Q - k_{i4}(\frac{1}{2}k_{p1}V_q^{pcc} + 1)i_{dL} + k_{i4}\omega L_{vir}i_{qL} + k_{i4}k_{p3}Q^* - \frac{1}{2}k_{i4}k_{p3}I_{dL}v_q^{pcc} + \frac{1}{2}k_{i4}k_{p3}I_{dL}v_d^{pcc}. \tag{4.29}$$

Note that P and Q have been replaced by the state and input varaibles using (**??**) and (**??**). Furthermore, the modified controller output equations can be expressed as follows:

$$v_q^r = v_q^{pcc} + \omega L i_{dL} + y_{iq} + k_{p2}(y_P + k_{p1}(P^* - \frac{1}{2}V_q^{pcc} i_{qL} - \frac{1}{2}v_q^{pcc} I_{qL} - \frac{1}{2}v_d^{pcc} I_{dL}) \\ -\omega L_{vir} i_{dL} - i_{qL}) \tag{4.30}$$

$$v_q^r = v_d^{pcc} - \omega L i_{qL} + y_{id} + k_{p4}(y_Q + k_{p3}(Q^* - \frac{1}{2}V_q^{pcc} i_{dL} - \frac{1}{2}v_q^{pcc} I_{dL} + \frac{1}{2}v_d^{pcc} I_{qL}) \\ +\omega L_{vir} i_{qL} - i_{dL}) \tag{4.31}$$

The modified state equations corresponding to v_q^{inv} and v_d^{inv} can then be expressed as follows:

$$\dot{v}_q^{inv} = \frac{1}{T_d}(v_q^{pcc} + \omega L i_{dL} + y_{iq} + k_{p2}(y_P + k_{p1}(P^* - \frac{1}{2}V_q^{pcc} i_{qL} - \frac{1}{2}v_q^{pcc} I_{qL} - \frac{1}{2}v_d^{pcc} I_{dL}) \\ -\omega L_{vir} i_{dL} - i_{qL}) - v_q^{inv}) \tag{4.32}$$

$$\dot{v}_d^{inv} = \frac{1}{T_d}(v_d^{pcc} - \omega L i_{qL} + y_{id} + k_{p4}(y_Q + k_{p3}(Q^* - \frac{1}{2}V_q^{pcc} i_{dL} - \frac{1}{2}v_q^{pcc} I_{dL} + \frac{1}{2}v_d^{pcc} I_{qL}) \\ +\omega L_{vir} i_{qL} - i_{dL}) - v_q^{inv}) \tag{4.33}$$

The state-space model of a grid-tied VSI equipped with a modified PQ controller including virtual inductance feedforward is presented in (4.34). Comparing the derived model with the model presented in (2.35), it can be seen that two entries of the previous model have been modified, i.e. A_{53}^{vir} and A_{63}^{vir}. The full form of the modified block matrices is provided in Appendix A. The model derived in this section will be utilized in Section 4.4 to demonstrate the efficacy of the virtual inductance scheme through root locus studies.

Table 4.1: *Circuit and controller parameters for Chapter 4*

Parameter	Value	Parameter	Value
L_1	$1.0mH$	k_{p1}, k_{p3}	0.005
R_1	0.15Ω	k_{p2}, k_{p4}	0.5
L_2	$0.5mH$	k_{i1}, k_{i3}	0.002
R_2	0.1Ω	k_{i2}, k_{i4}	0.2
C_f	$30\mu H(\Delta)$	T_d	$390\mu s$
R_f	0.01Ω	f	$60Hz$

$$\frac{d}{dt}\begin{bmatrix} i_{qd}^{inv} \\ v_{qd}^{c} \\ i_{qdL} \\ y_1 \\ y_2 \\ v_{qd}^{inv} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13}^{L} & 0 & 0 & A_{16}^{c} \\ A_{21} & A_{22} & A_{23}^{L} & 0 & 0 & 0 \\ A_{31}^{c} & A_{32}^{c} & A_{33}^{c} & 0 & 0 & 0 \\ A_{41}^{c} & A_{42}^{c} & A_{43}^{c} & 0 & 0 & 0 \\ A_{51}^{c} & A_{52}^{c} & A_{53}^{vir} & A_{54} & 0 & 0 \\ A_{61}^{c} & A_{62}^{c} & A_{63}^{vir} & A_{64} & A_{65} & A_{66} \end{bmatrix} \begin{bmatrix} i_{qd}^{inv} \\ v_{qd}^{c} \\ i_{qdL} \\ y_1 \\ y_2 \\ v_{qd}^{inv} \end{bmatrix} + \begin{bmatrix} 0 & b_1 & 0 \\ 0 & b_2 & 0 \\ B_{31}^{c} & b_3^{c} & 0 \\ B_{41}^{c} & b_4^{c} & B_{43} \\ B_{51}^{c} & b_5^{c} & B_{53} \\ B_{61}^{c} & b_6^{c} & B_{63} \end{bmatrix} \begin{bmatrix} v_{qd}^{g} \\ \omega \\ R^{*} \end{bmatrix}. \quad (4.34)$$

4.4 Stability Analysis

In this section, the efficacy of the virtual inductance feedforward scheme in improving the stability of grid-tied VSIs in weak grids is discussed through root locus studies. A $10kW$ grid-tied system with a rated voltage of $240V$ is considered for this section. The circuit and controller values used are provided in Table 4.1, which are also employed for the experimental verification of the proposed scheme in Section 4.6. The LCL filter values are chosen to place the system close to the stability boundary, while small values for the integrator gains, i.e. K_is are selected to avoid overshoots, which could potentially harm the hardware components.

To demonstrate that the effect of L_2 and L_{vir} is similar on the stability of grid-tied VSIs in weak grids, the root locus plots for both L_2 and L_{vir} are illustrated in this section. In the scenario displayed in Fig. 4.5, the root locus plot of the dominant eigenvalues are shown as the grid inductance L_g is increased, i.e. SCR is decreased, up to $6mH$ for three values of

L_2. As one can see from Fig. 4.5, for the smallest L_2 value, i.e. $0.5mH$, the system becomes unstable as the grid becomes weaker, while for the same increase in L_g the system remains stable for the larger L_2 values. It can also be seen from Fig. 4.5 that for smaller values of L_g, i.e. for stiff grids, the higher L_2 values can have a negative impact on stability as the dominant pole gets closer to the imaginary axis, which is in agreement with (4.14). The efficacy of L_{vir} is studied next, which is proposed in this dissertation to emulate the stability behavior of L_2 while eliminating its drawbacks.

The root locus of the dominant eigenvalues is plotted in Fig. 4.6, as L_g is increased up to $6mH$ for three virtual inductance values 0, 0.002, and 0.004. As one can see from Fig. 4.6, the system becomes unstable as L_g is increased when L_{vir} is not enabled, i.e. set to zero. For $L_{vir} = 0.002$, the system remains stable for larger values for L_g, while for $L_{vir} = 0.004$, the system operates in the stable region for the entire range of L_g similar to the case of

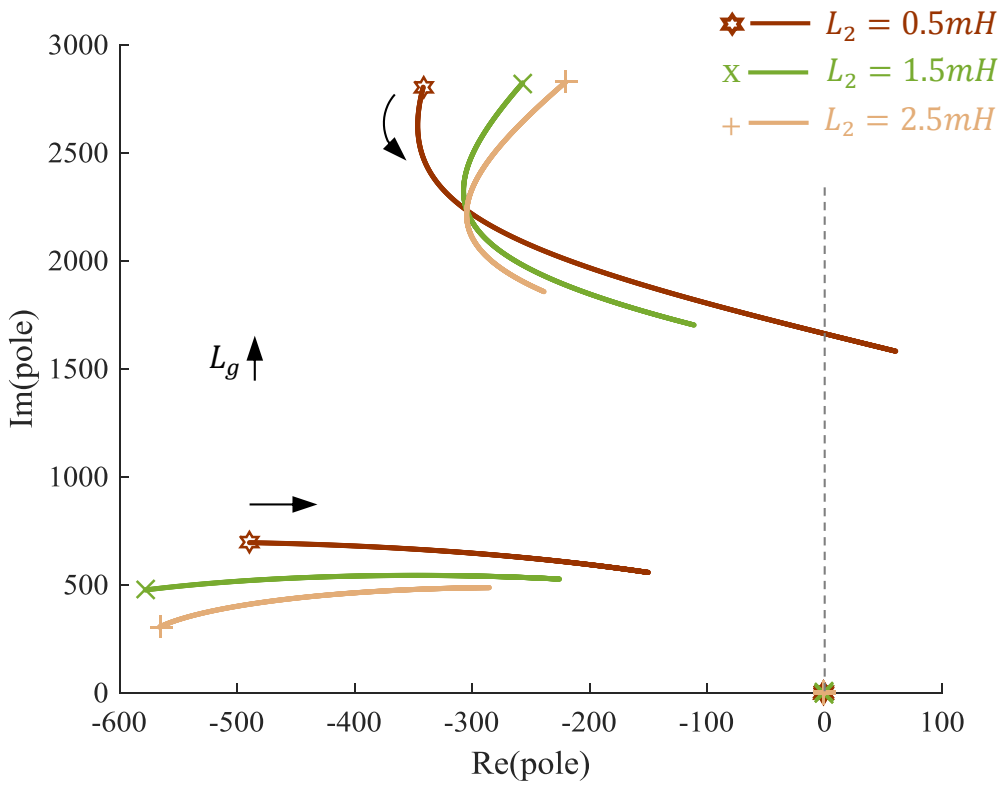


Figure 4.5: *Root locus of the dominant eigenvalues as L_g is increased from $1.5mH$ to $6mH$ for L_2 values of $0.5mH$, $1.5mH$ and $2.5mH$.*

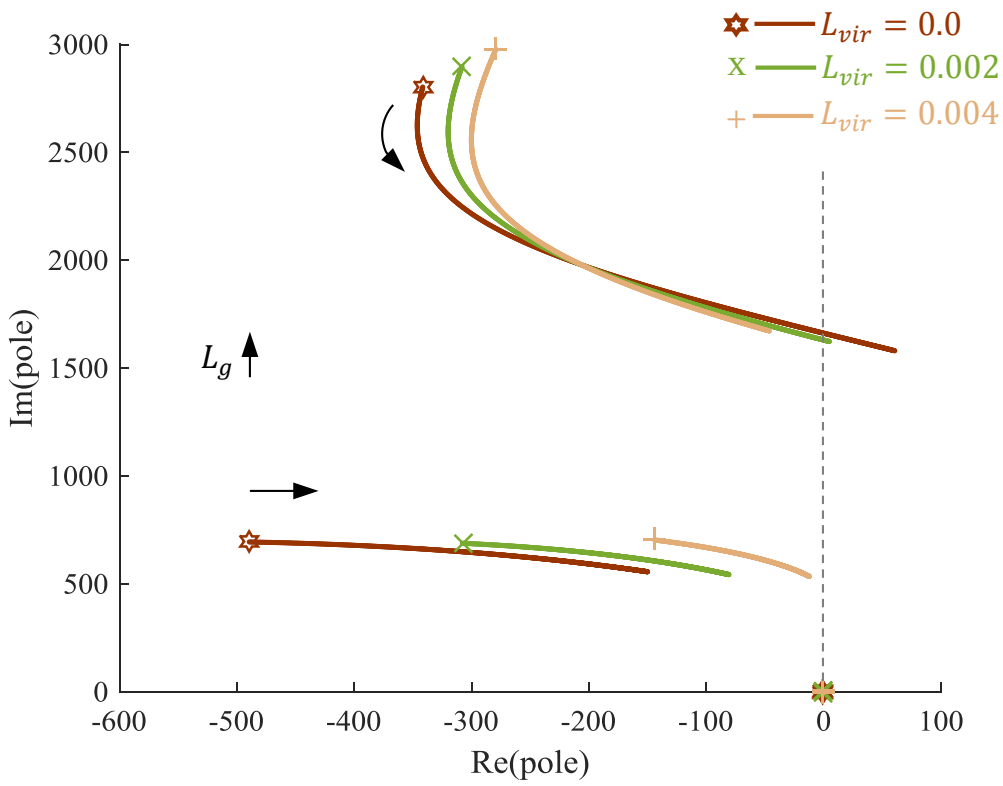


Figure 4.6: *Root locus of the dominant eigenvalues as L_g is increased from $1.5mH$ to $6mH$ for L_{vir} values of 0, 0.002 and 0.004.*

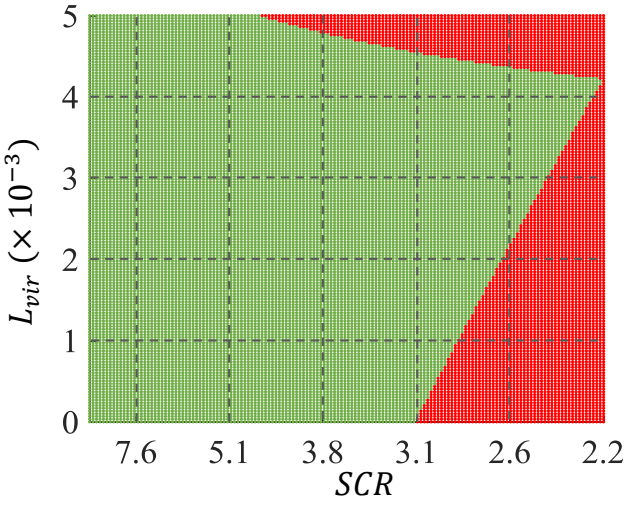


Figure 4.7: *Stability regions of the grid-tied VSI under weak grids with virtual inductance implemented.*

larger L_2s. Therefore, a grid-tied VSI can be operated in the stable region by introducing virtual inductance feedforward in its control structure. It can also be seen from Fig. 4.6, while increasing L_{vir} keeps the dominant pole in the left half plane, another pole is seen to be approaching the right half plane as L_{vir} becomes larger. Therefore, from a stability perspective, the value of L_{vir} cannot be increased without bounds and depending on the grid inductance there is a range of L_{vir} values for which the system can be kept stable. This property of L_{vir} is further explored in Fig. 4.7 where the stability of the system is emphasized as L_{vir} is increased while SCR of the grid is decreased, i.e. L_g is increased. The stable and unstable regions are denoted by green and red, respectively. As one can see from Fig. 4.7, a virtual inductance term can be designed to enable stable operation under various weak grid conditions. However, as the grid becomes weaker, i.e. SCR decreases, the range of L_{vir} values for which the system remains stable becomes restricted. For the operating condition provided in Table 4.1, the virtual inductance scheme can ensure stable operation of grid-tied VSIs up to an SCR value of 2.2 as shown in Fig. 4.7, whereas the existing standards for grid-tied VSI interconnection recommends $SCR \geq 10$ [21]. Therefore, the proposed scheme ensures stability for much smaller SCR values, extending the range of stable operation. The efficacy of the virtual inductance feedforward scheme will be verified through hardware tests in Section 4.6. A technique to adaptively choose the virtual inductance value based on grid conditions will be presented in Chapter 5.

4.5 Performance Comparison with Controller Parameter Redesign

In this section, the performance of the virtual inductance feedforward scheme is compared against stability enhancement procedures employing the design of controller proportional gains. The dynamic response of both methods is also compared through time-domain simulations carried out in MATLAB/Simulink. The parameter values provided in Table 4.1 are employed in this section, with the exception of the integrator gains, which are selected to be

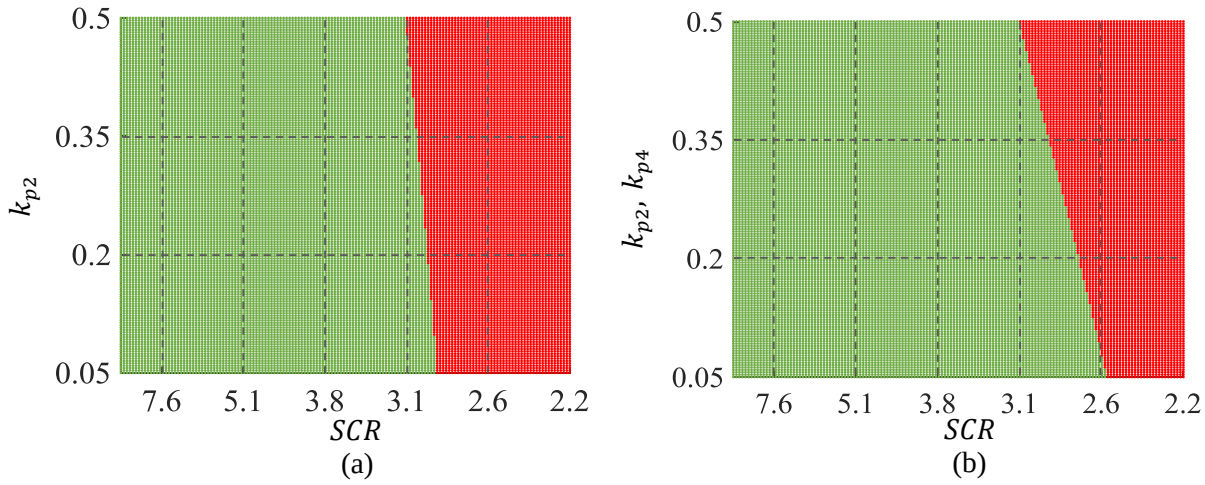


Figure 4.8: *Stability regions of the grid-tied VSI under weak grids when decreasing (a) k_{p2} and (b) k_{p2} and k_{p4}.*

larger, i.e. $k_{i1} = k_{i3} = 2$ and $k_{i2} = k_{i4} = 5$, to observe the dynamic response over a small time-scale.

The controller proportional gains can be decreased to improve the stability of grid-tied VSIs in weak grids, as discussed in Section 3.1. The proportional gains of the outer power loops are usually selected to be very small to begin with and as such, these gains cannot be decreased over a wide range. Furthermore, for the same grid inductance and for the same tenfold decrease in values, the inner current loop gains are seen to be moving the dominant poles much further into the stable region than the outer loop gains, in the scenario presented in Fig. 3.4. Therefore, the effect of the inner current loop proportional gains on stability is highlighted in this section.

The stability regions of the grid-tied VSI as SCR is decreased, i.e. L_g is increased, and the proportional gain k_{p2} is decreased are shown in Fig. 4.8(a). As one can see from Fig. 4.8, the stable region of VSIs is only slightly increased for a tenfold decrease in k_{p2}. Note that, k_{p2} is decreased up to 0.05 to avoid any interaction with the outer power loop. The response time ratio between cascaded loops is commonly set at a minimum of 10 [24, 83]. Since the outer loop gains are set at 0.005, k_{p2} can only go as low as 0.05.

The stability regions of the grid-tied VSI are demonstrated in Fig. 4.8(b), as both k_{p2}

and k_{p4} are decreased simultaneously for decreasing values of SCR. As can be seen from Fig. 4.8(b), the stability region has increased for decreases in both k_{p2} and k_{p4} compared to the case when only k_{p2} is decreased. However, the developed virtual inductance feedforward scheme demonstrates a much larger increase in the stability region as can be seen from comparing Figs. 4.7 and 4.8(b).

In the scenario presented in Fig. 4.9, the dynamic response of the virtual inductance feedforward method is compared against the controller redesign method. For a fair comparison, parameter gains at the stability boundary should be chosen. Comparison of Figs. 4.7 and 4.8(b) show that for a SCR of 2.6, $k_{p2} = k_{p4} = 0.05$ and $L_{vir} = 0.003$ should display similar stability performance. Hence, these values are selected for the analysis. In Fig. 4.9(a), the output active and reactive power of the VSI are displayed for a step change in the desired active power from $2000W$ to $3000W$ at instant $0.1s$, for the nominal operating condition of $k_{p2} = k_{p4} = 0.05$ and $L_{vir} = 0$ to set a performance benchmark. In Fig. 4.9(b), the dynamic response of the system is shown as the same input step change is applied for $k_{p2} = k_{p4} = 0.05$. As can be seen from Fig. 4.9(b), the response of the system have become significantly slower for a decrease in the proportional gains and the closed-loop system does not reach the steady-state values in the time-scale displayed in the figure. The same step change is applied to the system for $L_{vir} = 0.003$ and the original control gains as shown in Fig. 4.9(c). As one can see from Fig. 4.9, the dynamic response of the system with virtual inductance is almost identical to the original system. A slight deviation in the reactive power can be observed in Fig. 4.9(c) during the step change, as the q component of the current, which is responsible for active power generation, is fed to the reactive power controller to realize the virtual inductance scheme according to (4.27). The reactive power quickly converges to its desired value again, as larger controller gains can be maintained when employing virtual inductance feedforward for stability enhancement. Therefore, the presented virtual inductance feedforward scheme is an improvement over the controller redesign technique in both dynamic performance and enhancing the stable region of operation.

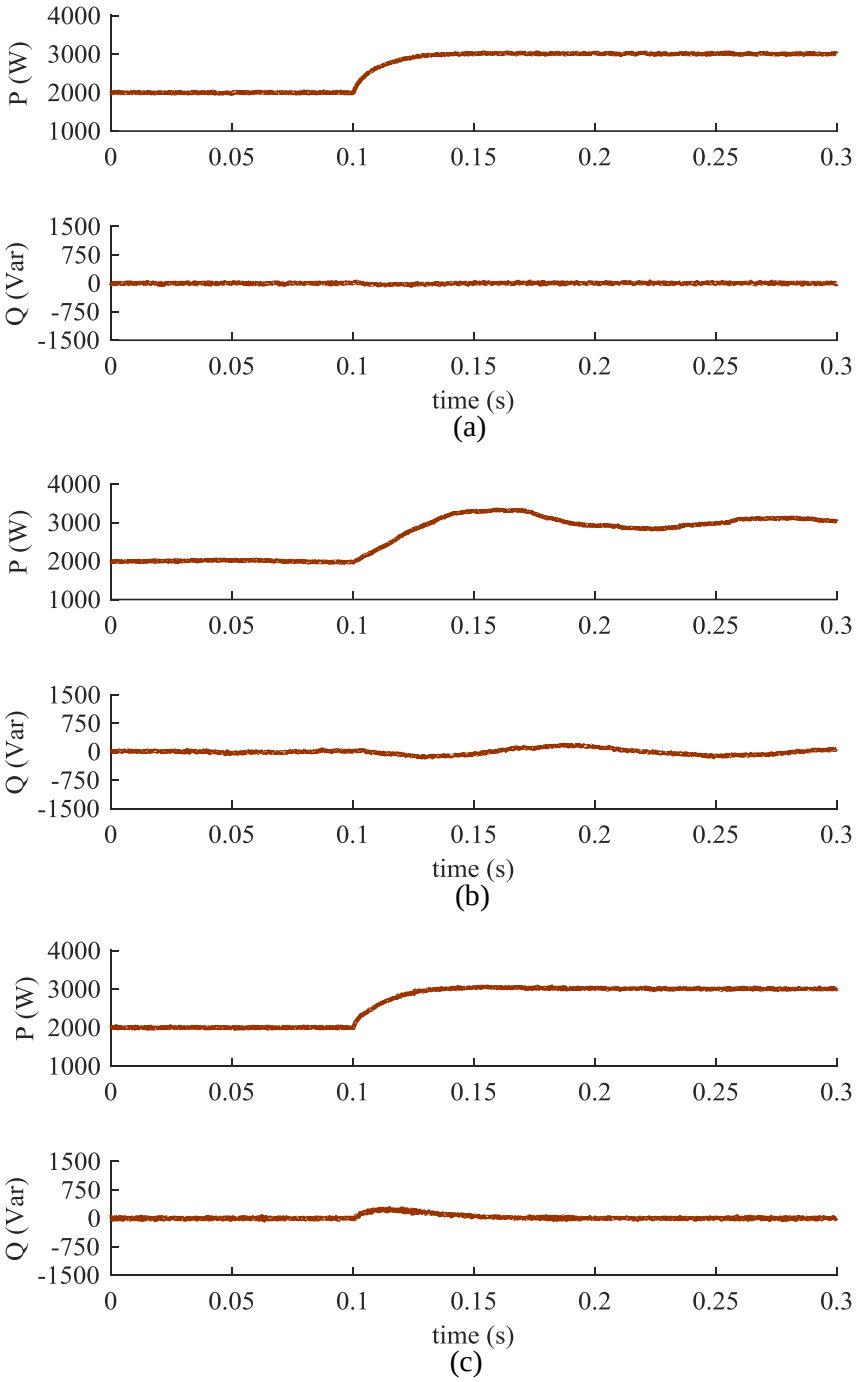


Figure 4.9: *Output active and reactive power of the grid-tied VSI as the desired active power is changed from* $2000W$ *to* $3000W$ *at instant* $0.1s$ *when (a)* $k_{p2} = k_{p4} = 0.5$ *with no virtual inductance, (b)* $k_{p2} = k_{p4} = 0.05$ *with no virtual inductance, (c)* $k_{p2} = k_{p4} = 0.5$ *and* $L_{vir} = 0.003$.

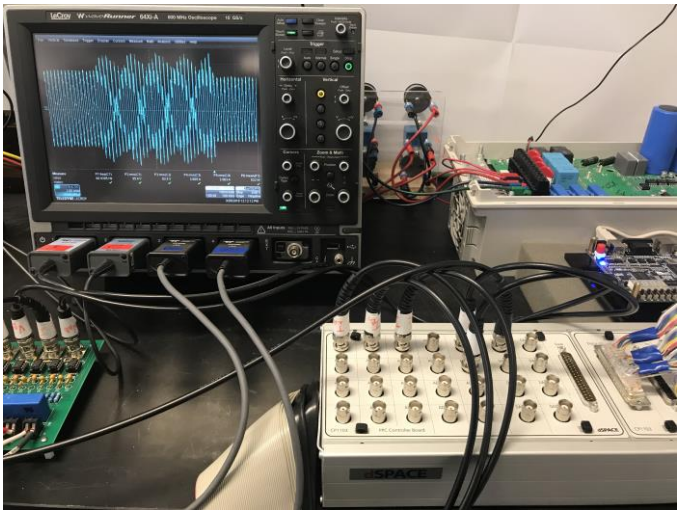


Figure 4.10: *Experimental setup and scope display for the scenario demonstrated in Fig. 4.12.*

4.6 Experimental Verification

In this section, the efficacy of the virtual inductance feedforward scheme is verified through hardware tests carried out on a three-phase grid-tied inverter setup. The experimental setup is shown in Fig. 4.10. The modified PQ controller including virtual inductance feedforward was built in MATLAB/Simulink, which was integrated with the hardware setup using dSpace 1103 Controller Board. More details on the laboratory setup employed in this dissertation are provided in Subsection 2.1.2. The parameter values used in this section can be found in Table 4.1. For all experiments carried out, the active power was set to $550W$ at unity power factor. A PWM carrier frequency of $5kHz$ was used in the experiments.

In the first scenario presented in Fig. 4.11, the line-to-line voltage at the PCC and the grid current of phase-A are shown as the system is initially stable under a stiff grid and virtual inductance is disabled. At instant $t = 2.35s$, a $5mH(SCR = 3.1)$ inductance was inserted between the grid and the PCC that was initially bypassed through a three-phase circuit breaker. As one can see from Fig. 4.11, the system became unstable with the introduction of a large grid inductance. To bring the system back to the stable region, $L_{vir} = 0.0025$ was enabled at instant $t = 2.5s$ through Control Desk, a real-time software interface linked with dSpace. As can be seen from Fig. 4.11, the system became stable under a weak grid with

$5mH$ grid inductance as the virtual inductance feedforward scheme was introduced. The test outcome is in agreement with the stability analysis carried out in Section 4.4. In addition, the stability characteristic observed in this scenario can be verified through Fig. 4.7.

In the scenario presented in Fig. 4.12, a stable grid-tied system became unstable at instant $t = 2.22s$ as a grid inductance of $5.5mH(SCR = 2.8)$ was inserted to the circuit. From the stability regions demonstrated in Fig. 4.7, it can be seen that a suitable virtual inductance value can be chosen to bring the system back to the stable region under this SCR value. As one can see from Fig. 4.12, with the injection of $L_{vir} = 0.0025$ at instant $t = 2.5s$, the grid-tied system returns to the stable region of operation as predicted from the stability regions of Fig. 4.7.

To further validate the usefulness of the presented virtual inductance scheme under various degrees of weak grid situations, a grid inductance of $6mH(SCR = 2.6)$ was inserted into the system at instant $t = 2.28s$ following which a 0.0025 virtual inductance was injected at instant $t = 2.5s$, as shown in Fig. 4.13. Similar to the previous scenarios, the virtual inductance feedforward scheme brought the system back to the stable region, which became unstable due to the introduction of a large grid inductance. The scenario presented

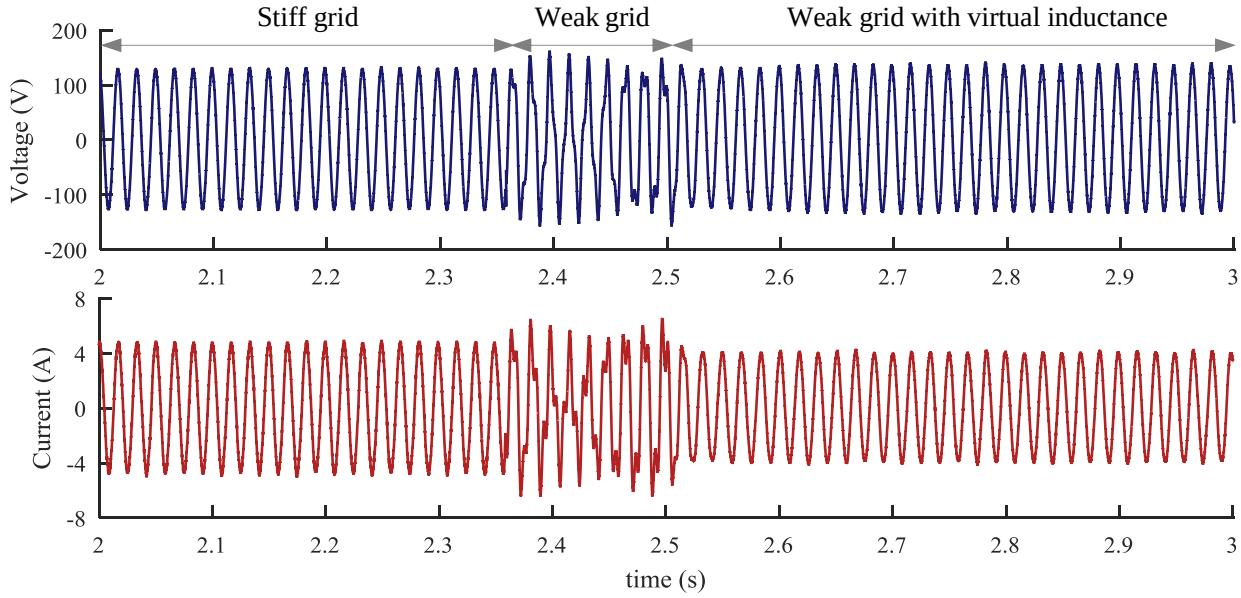


Figure 4.11: *Voltage at the PCC (top) and grid current (bottom) as $L_g = 5mH$ is inserted at instant $2.35s$ followed by the introduction of a virtual inductance of 0.0025 at $2.5s$.*

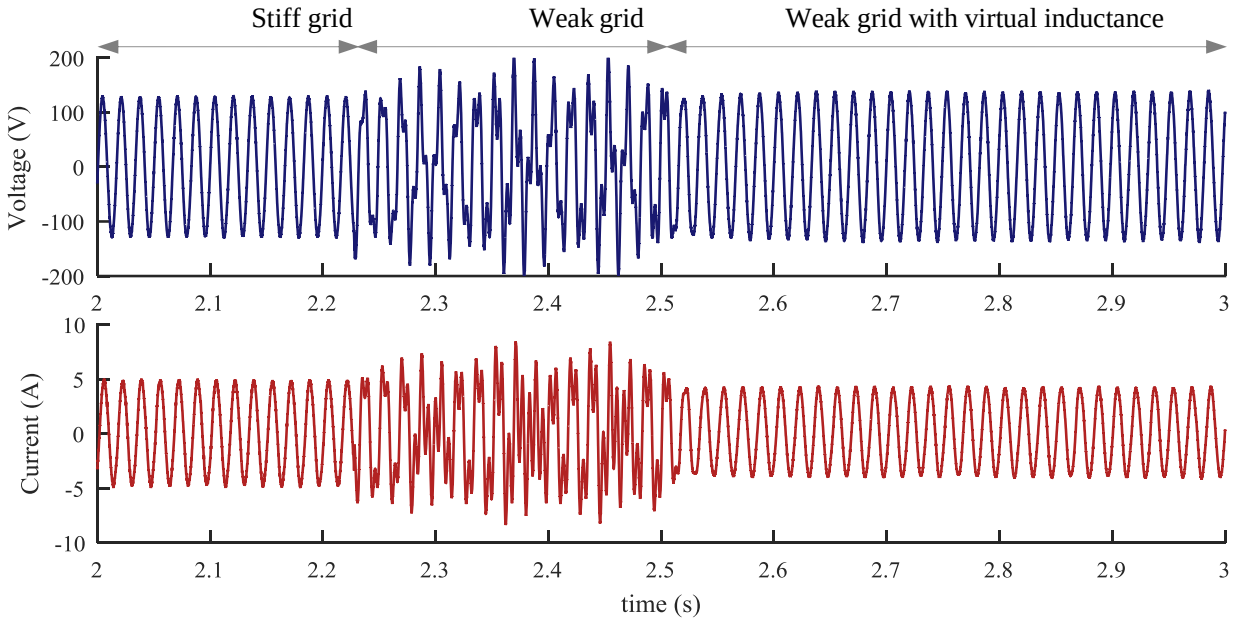


Figure 4.12: *Voltage at the PCC (top) and grid current (bottom) as* $L_g = 5.5mH$ *is inserted at instant* $2.22s$ *followed by the introduction of a virtual inductance of 0.0025 at* $2.5s$.

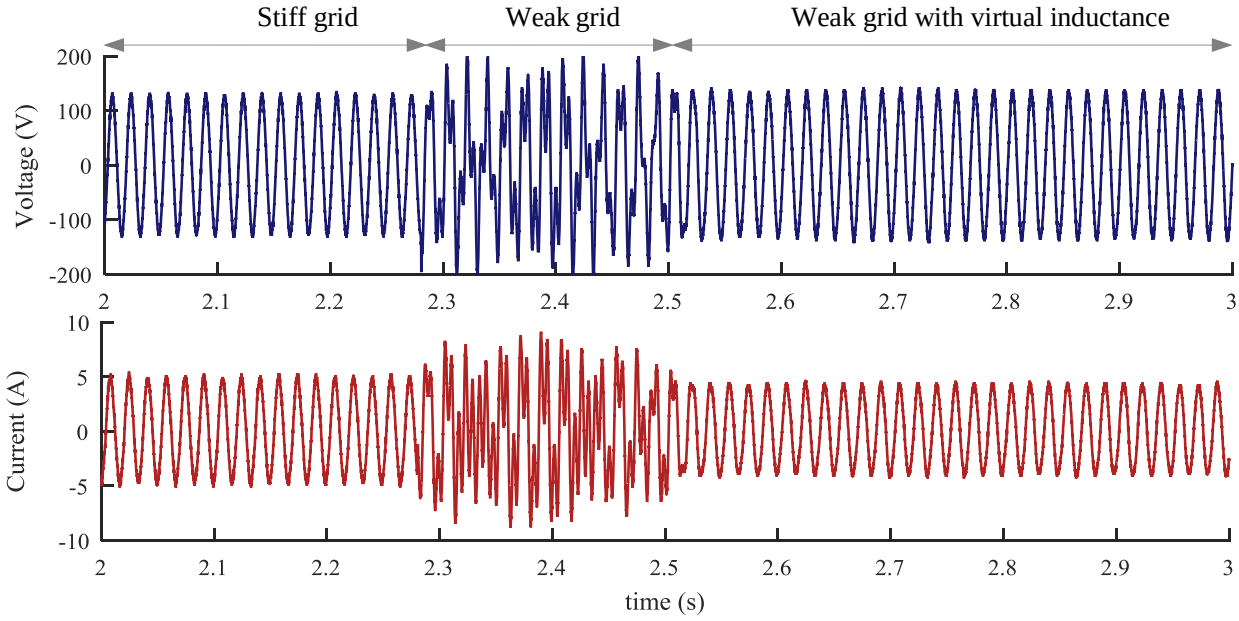


Figure 4.13: *Voltage at the PCC (top) and grid current (bottom) as* $L_g = 6mH$ *is inserted at instant* $2.28s$ *followed by the introduction of a virtual inductance of 0.0025 at* $2.5s$.

in Fig. 4.13 is also in agreement with the stability regions demonstrated in Fig. 4.7. It should be noted that if the virtual inductance scheme remains active from the beginning of system operation as it should be in practical applications, the grid-tied system would stay stable

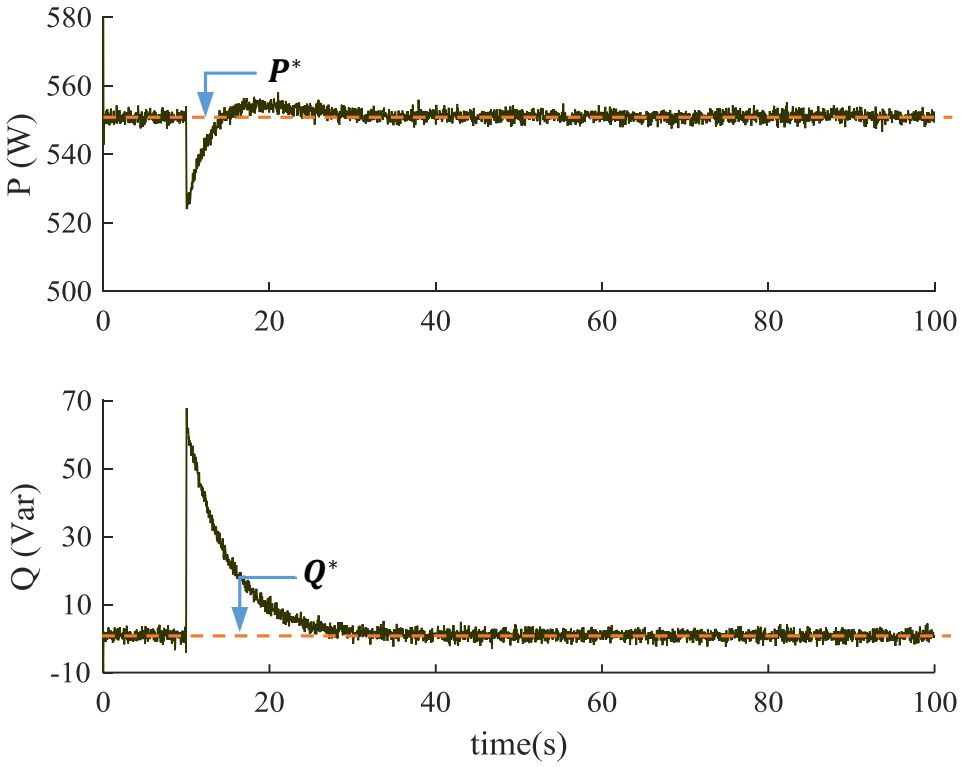


Figure 4.14: *Active power (top) and reactive power (bottom) supplied by the VSI as a virtual inductance of 0.003 is injected at instant* 8*s*.

even under weak grid conditions. The virtual inductance has been activated after the system had become unstable in these case studies to demonstrate the efficacy of the presented scheme.

In the experimental scenarios depicted in this section up to this point, the efficacy of the virtual inductance scheme in stabilizing VSI operation in weak grids is demonstrated. In the scenarios presented in Figs. 4.11 - 4.13, the currents after the system became stable with the injection of virtual inductance, are seen to be lower than their original values. The currents are not seen to return to their reference values in these scenarios as the signals are displayed for a very small time-scale, i.e. 1*s*, to highlight the stability phenomenon. To observe the steady-state performance of the system when employing virtual inductance feedforward, the output active and reactive powers of the VSI are illustrated over a large time period, i.e. 100*s*, in the scenario presented in Fig. 4.14. As one can see from Fig. 4.14, a 0.0003 virtual inductance was injected at instant 8*s* into the control scheme of the VSI,

which initially deviated P and Q from their desired values. As can be further seen from the figure, following this deviation the PQ controllers bring the P and Q back to their reference values, i.e. P^*, Q^*, and the signals remain in their reference values with no steady-state error. Therefore, it can be concluded that the proposed scheme can enable stable operation of grid-tied VSIs in weak grids without compromising its steady-state performance.

4.7 Conclusion

In this section, a virtual inductance feedforward strategy has been presented to improve the stability of grid-tied VSIs in weak grids. Using the presented scheme, stability has been achieved by emulating the stabilizing characteristic of grid-side filter inductance while eliminating its drawbacks, e.g. additional voltage drop, increased size and cost. The presented scheme can be realized by feedforward of the grid current component through a virtual inductance block. As a result, no additional sensors are necessary for the implementation of this strategy. The efficacy of the virtual inductance scheme has been studied through root locus analysis based on the derived model of a modified PQ controller, which includes the virtual inductance feedforward path. The results have been verified through hardware tests carried out for three different weak grid scenarios. The steady-state performance of the system is retained when using virtual inductance feedforward scheme as also validated through hardware experiments.

Chapter 5

Virtual Inductance Feedforward with Direct Model Reference Adaptive Control

In this chapter, a direct MRAC scheme is applied to adaptively change the virtual inductance term presented in Chapter 4 with respect to variations in the grid impedance. From the analysis performed in Section 4.4, it was concluded that for a particular weak grid, there is an upper and a lower boundary for the virtual inductance value that can be chosen to ensure stable operation of grid-tied systems. As the grid becomes weaker, the acceptable range of virtual inductance values also becomes narrower. In addition, the grid impedance is not commonly a known quantity. Therefore, selection of an appropriate virtual inductance value for the stability of grid-tied VSIs might become challenging in practical applications. To eliminate concerns pertaining to the design of virtual inductance values, a direct MRAC scheme is presented in this chapter to select an appropriate virtual inductance term to enable stable operation of grid-tied VSIs under various weak grid conditions.

The contents of this chapter are organized into five sections. In Section 5.1, the motivations behind employing a direct adaptive control method instead of indirect methods are discussed. The adaptation law of the direct MRAC technique for a simple first-order

system is derived in Section 5.2. The adaptation law is updated for a grid-tied VSI and the modified control scheme of the grid-tied VSI including an adaptive virtual inductance feed-forward is presented in Section 5.3. In Section 5.4, the developed control scheme is verified through tests carried out in a hardware setup. Finally, concluding remarks for the chapter are presented in Section 5.5.

5.1 Direct vs. Indirect Adaptive Control Scheme

In this section, a brief description of the operating principles of indirect and direct adaptive control schemes are provided. Furthermore, the motivations behind using the direct MRAC, instead of its indirect adaptive control counterparts are also discussed.

The block diagrams of two indirect adaptive control methods, namely indirect MRAC and self-tuning controller (STC) are illustrated in Fig. 5.1 (a) and Fig. 5.1 (b), respectively. In indirect adaptive control methods, the parameters of the plant, which is the open-loop VSI circuit for the purposes of this dissertation, are estimated based on the input and output signals of the plant [84]. Then based on the estimated plant parameters, the controller gains of the closed-loop system are calculated. Since there is an intermediate step of estimating the plant parameters when adjusting the controller gains instead of directly calculating them

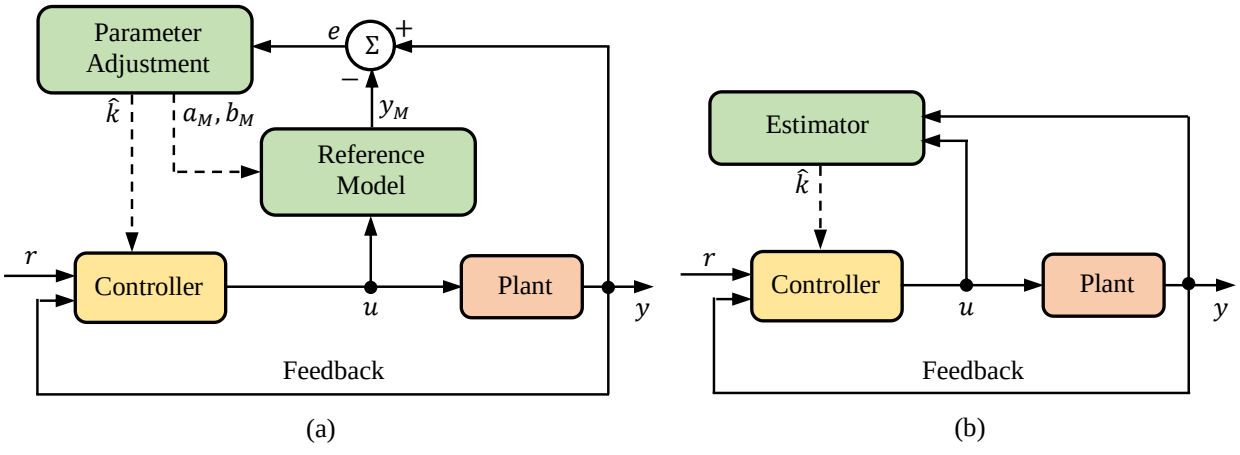


Figure 5.1: *Block diagrams of (a) an indirect model reference adaptive control scheme and (b) a self-tuning controller scheme.*

from the input and output signals, such methods are known as indirect methods. In the case of indirect MRAC methods, there exists a reference model as can be seen from Fig. 5.1 (a), the parameters of which are constantly adjusted to estimate the unknown parameters of the plant. Based on the error between the outputs of the plant and the reference model, and the input to the plant which is also fed as an input to the reference model, an adaptation law is derived using the Lyapunov stability criterion to adapt the parameters of the reference model with the objective of minimizing the model error.

STC method belongs to a category of indirect adaptive control methods that do not contain a reference model as can be seen from Fig. 5.1 (b). The STC technique contains an on-line parameter estimator that estimates the unknown parameters of the plant and based on the estimated parameters the controller gains are calculated [84]. The online estimator and the controller operate simultaneously in the STC method. In both the indirect MRAC and the STC method, the unknown plant parameters have to be estimated. In the case of grid-tied VSI systems, the only relevant unknown plant parameter is the grid inductance as the filter values are design parameters. Therefore, to ensure stable operation in weak grids employing indirect adaptive control methods, the grid inductance has to be estimated and based on the estimated value an appropriate virtual inductance value has to be calculated. However, the value of grid inductance for which the system becomes unstable also depends on the system operating conditions, i.e. the filter and controller parameters, as discussed

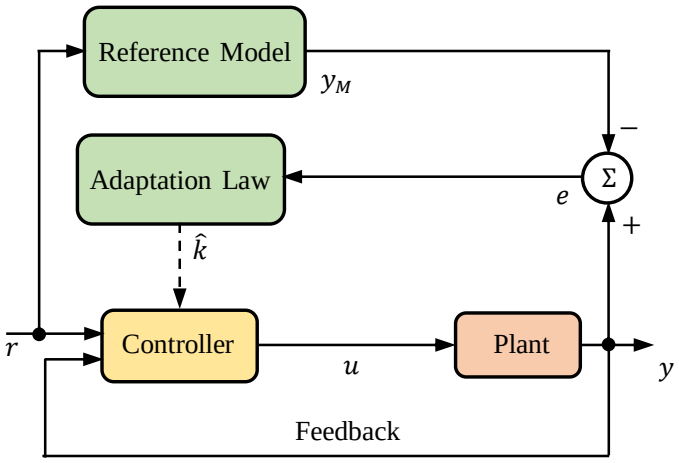


Figure 5.2: *Block diagram of a direct model reference adaptive control scheme.*

in Section 3.1. Therefore, deriving an independent relationship between the grid inductance and the virtual inductance is not a straightforward process, which is an obstacle in using indirect adaptive control methods. Furthermore, in the case of the STC method, there might be an additional difficulty in integrating the online estimator of the STC, which operates in the z-domain, to the PQ controller of the grid-tied VSI, which operates in the s-domain.

In the direct MRAC method, which is illustrated in Fig. 5.2, the unknown parameters of the system are not estimated. Instead, a reference model is chosen that specifies the desired closed-loop response of the system. Based on the error between the output of the reference model and the actual system output, an adaptation law is designed using Lyapunov stability criterion to adapt the controller gains, which in turn adjust the inputs to the plant such that the output of the system follows the output of the reference model [84]. Since the controller gains are adjusted directly using the error signals without the intermediate parameter estimation step as can be seen in Fig. 5.2, this method is referred to as the direct MRAC method. The first step in utilizing the direct MRAC method for stable operation of grid-tied VSIs is to choose a stable reference model. Based on the full-order model in (4.34), an accurate second-order model for a grid-tied VSI operating near the stability boundary can be derived using a suitable model-order reduction method as discussed in Appendix B. Using the procedure outlined in Appendix B, a stable second-order model can then be chosen as the reference model. In case the system becomes unstable under the influence of a large grid inductance, the virtual inductance value will be adjusted based on the deviation of the system output from the reference model output, to bring the system back to the stable region without requiring the estimation of the grid inductance value. Therefore, the direct MRAC method is employed in this dissertation to develop the adaptive virtual inductance feedforward scheme.

5.2 Derivation of the Adaptation Law

In this section, the adaptation law for a direct MRAC scheme is derived. The adaptation law is derived considering a first-order system with unknown parameters. The adaptation

law will be updated for a grid-tied VSI equipped with virtual inductance feedforward scheme in the next section.

The state-space representation of a first-order plant with a known structure can be expressed as follows:

$$\dot{y} = ay + bu, \tag{5.1}$$

where, a and b are constant but unknown parameters. Also in (5.1), u and y are the input and output to the plant, respectively. The stable reference model of the system can be expressed as:

$$\dot{y}_M = a_M y_M + b_M r. \tag{5.2}$$

The input to the reference model is the closed-loop input of the system r, as the reference model defines the ideal response of the closed-loop system. Then the objective is to find a plant input u such that:

$$\lim_{t\to\infty} e = 0, \tag{5.3}$$

where, $e = y - y_M$ is the error between the system output and the model output. As discussed in Section 6.2, in MRAC direct methods the controller gains are adjusted based on the input and output signals of the system. The plant input u can be calculated from the controller gains as follows:

$$u = \hat{k}r - \hat{h}y, \tag{5.4}$$

where, $\hat{h}$ and $\hat{k}$ are the controller gains. Replacing (5.4) in (5.1), the closed-loop equation of the first-order system can be expressed as follows:

$$\dot{y} = (a - b\hat{h})y + b\hat{k}r. \tag{5.5}$$

The error dynamics of the system can be expressed as follows:

$$\dot{e} = \dot{y} - \dot{y}_M. \tag{5.6}$$

Replacing $\dot{y}$ from (5.5) and $\dot{y}_M$ from (5.2) in (5.6) yield:

$$\dot{e} = (a - b\hat{h})y + b\hat{k}r - a_M y_M - b_M r. \tag{5.7}$$

By adding and subtracting the term $a_M y$, (5.7) can be expressed as follows:

$$\dot{e} = a_M e + (a - b\hat{h} - a_M)y + (b\hat{k} - b_M)r. \tag{5.8}$$

The controller gains $\hat{h}$ and $\hat{k}$ are adjusted in real time to make the error e go to zero over time. For a system with known quantities, i.e. a and b are known, the adaptation law for the control gains can be derived by setting (5.8) to zero. For systems with unknown quantities, the Lyapunov stability criterion has to be used.

According to the Lyapunov stability criterion, a system is asymptotically stable if a Lyapunov function V can be identified that is positive definite, i.e. $V > 0$, and the derivative of the Lyapunov function with respect to time is negative definite, i.e. $\dot{V} < 0$. Herein, a Lyapunov function is chosen such that the identifier system is asymptotically stable.

The positive-definite Lyapunov function for a system designed using direct MRAC can be chosen as follows:

$$V = \frac{1}{2}[e^2 + (a - a_M - b\hat{h})^2 + (b\hat{k} - b_M)^2] \tag{5.9}$$

An appropriate adaptation law can now be derived such that $\dot{V} < 0$. From (5.9), the derivative of V can be expressed as follows:

$$\dot{V} = e\dot{e} + (a - a_M - b\hat{h})(-b\dot{\hat{h}}) + (b\hat{k} - b_M)(b\dot{\hat{k}}) \tag{5.10}$$

In (5.10), a_M and b_M are constant as they are the parameters of the chosen reference model.

Furthermore, a and b can be assumed to be constant over short time intervals. Hence, the derivatives of the aforementioned parameters can be set to zero. Performing these changes and replacing $\dot{e}$ from (5.8)in (5.10) yield:

$$\dot{V} = a_M e^2 + (a - a_M - b\hat{h})(-b\dot{\hat{h}} + ey) + (b\hat{k} - b_M)(b\dot{\hat{k}} + er) \tag{5.11}$$

Since, for a stable reference model $a_M < 0$, the condition for asymptotic stability can be expressed as follows:

$$\begin{cases} -b\dot{\hat{h}} + ey = 0 \\ b\dot{\hat{k}} + er = 0 \end{cases} \tag{5.12}$$

The adaptation law for the controller gains of a direct MRAC scheme can then be expressed as follows:

$$\begin{cases} \hat{h} = \int b^{-1} ey dt \\ \hat{k} = -\int b^{-1} er dt \end{cases} \tag{5.13}$$

The adaptation law derived in this section for a first-order system will be updated for a grid-tied VSI system in the following section to adaptively change the virtual inductance term with variations in grid impedance.

5.3 Control Scheme with Adaptive Virtual Inductance

In this section, the adaptation law for direct MRAC scheme derived in the previous section is updated for a grid-tied VSI with a PQ controller. The block diagram of a modified PQ controller with virtual inductance feedforward can be seen in Fig. 4.4. For the derivation of the adaptation law, only the inner current control loops are considered, as the virtual inductance scheme is added to the current loops. From Fig. 4.4, the equations for the inner current loops can be written as follows:

$$v_q^{inv} = k_{p2} i_{qL}^* - k_{p2} i_{qL} + (\omega L - \omega L_{vir} k_{p2}) i_{dL} + v_q^{pcc}, \tag{5.14}$$

$$v_d^{inv} = k_{p4} i_{dL}^* - (\omega L - \omega L_{vir} k_{p4}) i_{qL} - k_{p4} i_{dL} + v_d^{pcc}, \tag{5.15}$$

where, i_{qL}^* and i_{dL}^* are the desired q-axis and d-axis virtual line-to-line currents, which are the outputs of the outer power loops. Notice that, the control delay has not been considered for simplicity of analysis. In addition, v_q^{pcc} and v_d^{pcc} are considered as disturbances and omitted from the analysis. Performing these changes, (5.14) and (5.15) can be expressed in matrix form as follows:

$$\begin{bmatrix} v_q^{inv} \\ v_d^{inv} \end{bmatrix} = \begin{bmatrix} k_{p2} & 0 \\ 0 & k_{p4} \end{bmatrix} \begin{bmatrix} i_{qL}^* \\ i_{dL}^* \end{bmatrix} - \begin{bmatrix} k_{p2} & -\omega L + \omega L_{vir} k_{p2} \\ \omega L - \omega L_{vir} k_{p4} & k_{p4} \end{bmatrix} \begin{bmatrix} i_{qL} \\ i_{dL} \end{bmatrix}, \tag{5.16}$$

where, v_q^{inv} and v_d^{inv} are outputs of the PQ controller and therefore inputs to the plant, which was denoted by u in Section 5.2. Comparing the controller output equation provided in the previous section in (5.4) to the one presented in (5.16), the following relationships can be obtained:

$$\hat{k} = \begin{bmatrix} k_{p2} & 0 \\ 0 & kp4 \end{bmatrix}, r = \begin{bmatrix} i_{qL}^* \\ i_{dL}^* \end{bmatrix}, \hat{h} = \begin{bmatrix} k_{p2} & -\omega L + \omega L_{vir} k_{p2} \\ \omega L - \omega L_{vir} k_{p4} & k_{p4} \end{bmatrix}, y = \begin{bmatrix} i_{qL} \\ i_{dL} \end{bmatrix}. \tag{5.17}$$

The stability of grid-tied VSIs, equipped with the virtual inductance feedforward scheme, can be ensured by only tuning the virtual inductance term as shown in Chapter 4. Therefore, the controller proportional gains in (5.17) can remain constant according to their design values and do not need to be changed adaptively. Denoting the individual elements of $\hat{h}$ as $\hat{h}(x, y)$, where x defines the row number and y defines the column number, the virtual inductance term can be expressed from (5.17) as follows:

$$\omega L_{vir} = \frac{\hat{h}(1,2) + \omega L}{k_{p2}} \tag{5.18}$$

Note that, a similar equation can also be derived considering the $\hat{h}(2,1)$ element, which will also be valid. Now, the characterisitic of a grid-tied VSI can be accurately expressed through a second-order model near the stability boundary as validated in Appendix B. Therefore, a second-order model can be chosen as the stable reference model for the direct MRAC scheme. A simplified second-order model for the plant, i.e. the grid-tied VSI circuit, can also be derived from the open-loop model in (2.4) by ignoring the filter capacitor branch, in which case the currents going through both the filter inductors are the same. As mentioned previously when deriving the controller equations in this section, the PCC voltages are considered as disturbances when deriving the plant model. Furthermore, the controller outputs are v_q^{inv} and v_d^{inv} are considered as inputs to the plant and can be replaced in (2.4) through (2.26) and (2.27). The simplified plant model can be expressed as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{qL} \\ i_{dL} \end{bmatrix} = \begin{bmatrix} -\frac{R_1+R_2}{L_1+L_2} & -\omega \\ \omega & -\frac{R_1+R_2}{L_1+L_2} \end{bmatrix}\begin{bmatrix} i_{qL} \\ i_{dL} \end{bmatrix} + \frac{1}{L_1+L_2}\begin{bmatrix} v_q^{inv} \\ v_d^{inv} \end{bmatrix} \tag{5.19}$$

Comparing (5.19) to (5.1), the following relationships can be obtained:

$$a = \begin{bmatrix} -\frac{R_1+R_2}{L_1+L_2} & -\omega \\ \omega & -\frac{R_1+R_2}{L_1+L_2} \end{bmatrix}; b = \frac{1}{L_1+L_2}. \tag{5.20}$$

The adaptation law for $\hat{h}$ can be updated for a second-order system as follows:

$$\hat{h} = (L_1+L_2)\begin{bmatrix} \int e_1 y_1 dt & \int e_1 y_2 dt \\ \int e_2 y_1 dt & \int e_2 y_2 dt \end{bmatrix} \tag{5.21}$$

where, b is replaced from (5.20). Now, substituting the expression for $\hat{h}(2,1)$ from (5.21) into (5.18), the adaptation law for the virtual inductance term can be expressed as follows:

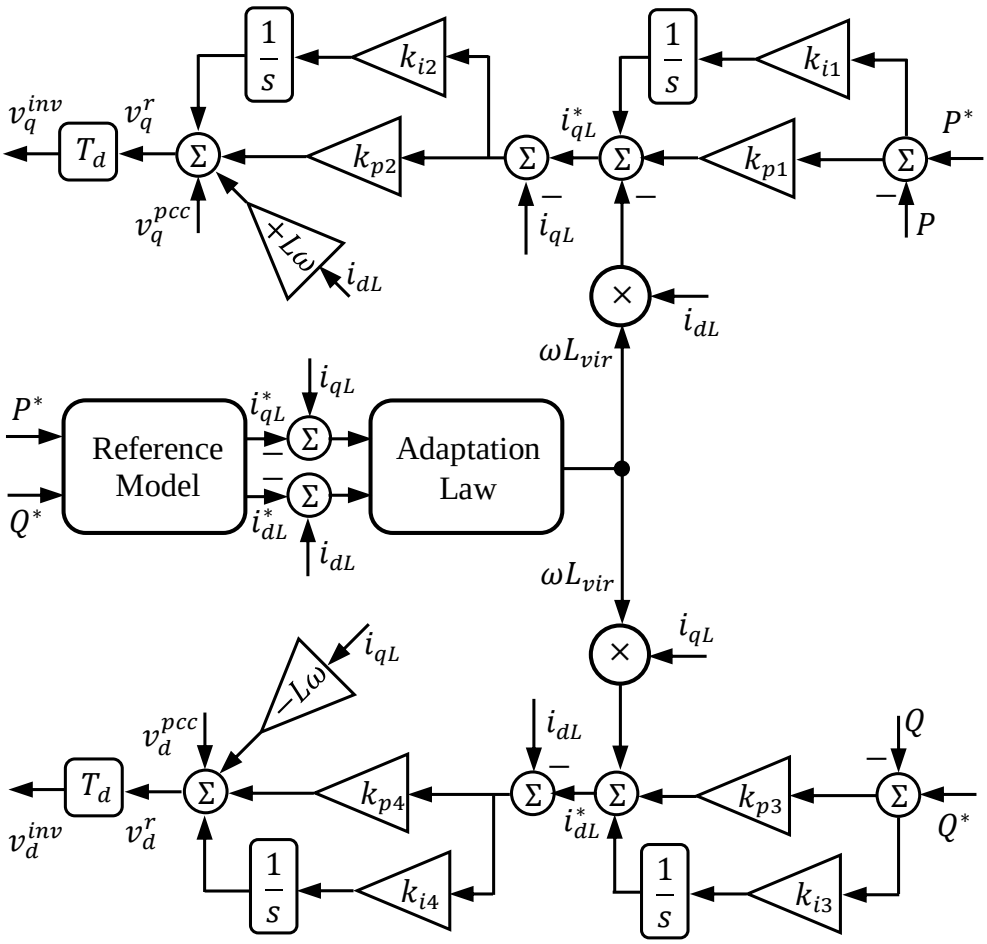


Figure 5.3: *Block diagram of a modified PQ controller for a grid-tied VSI equipped with adaptive virtual inductance feedforward.*

$$\omega L_{vir} = \frac{(L_1 + L_2)\int e_1 y_2 dt + \omega L}{k_{p2}} \tag{5.22}$$

The modified PQ controller with adaptive virtual inductance feedforward is illustrated in Fig. 2.4. The efficacy of the presented control scheme will be validated in the next section.

5.4 Experimental Verification

In this section, the performance of the adaptive virtual inductance feedforward scheme in enabling stability of grid-tied VSIs in weak grids is validated through several hardware tests. The hardware testbed for conducting the tests is shown in 5.4. The parameter values

for this section are provided in Table 5.1. The parameters shown in Table 5.1 are also utilized to obtain a second-order reference model for the direct MRAC embedded in the modified PQ controller. The second-order model is developed from the full-order grid-tied VSI model presented in (4.34) using the balanced truncation method detailed in Appendix B. Although no passive damping resistance R_f is present in the experimental setup, a R_f of 1Ω is considered in the reference model to obtain a desired model firmly in the stable region. The state-space matrices of the reference model are as follows:

$$A_{ref} = \begin{bmatrix} -632.5 & 6613.3 \\ -8175.5 & -709.4 \end{bmatrix}, B_{ref} = \begin{bmatrix} -0.433 & -0.345 \\ 0.354 & -0.557 \end{bmatrix}, \\ C_{ref} = \begin{bmatrix} 24.62 & -28.46 \\ 34.21 & 31.26 \end{bmatrix}, D_{ref} = \begin{bmatrix} 0.017 & 0.003 \\ -0.003 & 0.017 \end{bmatrix}. \tag{5.23}$$

Note that only the controller inputs are considered as inputs to the reference model, while the small-signal inputs to the open-loop model, i.e. grid voltage and frequency, are considered as disturbances. It should also be mentioned that the efficacy of the adaptive virtual inductance feedforward method does not depend on the specific reference model provided in (5.23) and should be valid for other stable reference models. A $12kW$ Primate Power grid emulator was utilized as the three-phase grid, while a Magna-Power SL400-15/208 programmable dc supply was used as the input dc source of the grid-tied VSI. More details on the experimental setup can be found in Subsection 2.1.2. For all tests carried out in this section, the inverter

Table 5.1: *Parameter values for Section 5.4*

Parameter	Value	Parameter	Value
L_1	$1.0mH$	k_{p1}, k_{p3}	0.005
L_2	$0.5mH$	k_{p2}, k_{p4}	0.5
C_f	$30\mu H(\Delta)$	k_{i1}, k_{i3}	0.01
V_{dc}	$240V$	k_{i2}, k_{i4}	0.2
$v_{LL,rms}$	$90V$	f_{PWM}	$10kHz$

Figure 5.4: *Experimental setup for the hardware tests performed in Section 5.4 with the scenario presented in Fig. 5.6 displayed on the screen.*

was set to deliver $600W$ at unity power factor.

In the scenario demonstrated in Fig. 5.5, the voltage at the PCC, grid current, active power, and reactive power of the VSI are shown as the VSI was initially providing $600W$ to the grid at unity power factor in the presence of a $2.5mH$ grid inductance. The developed

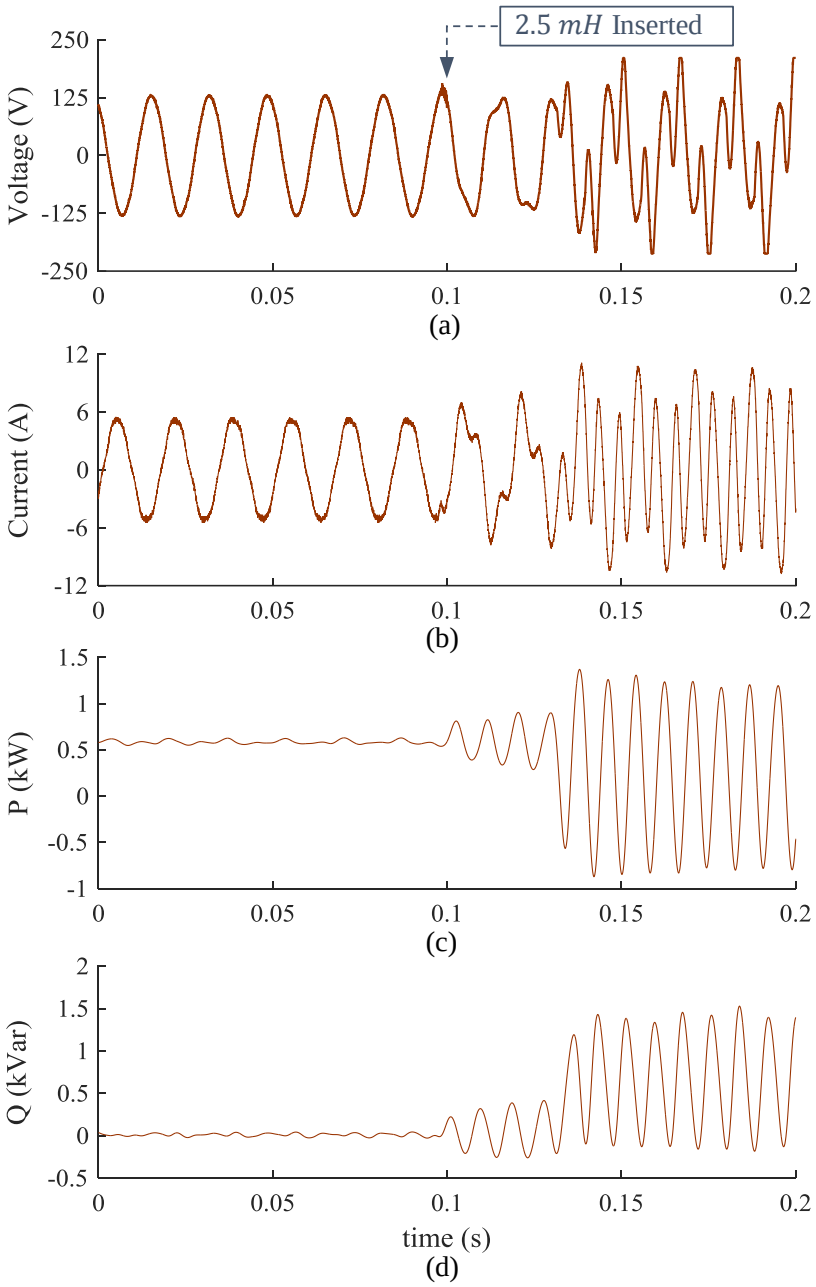


Figure 5.5: *(a) Voltage at the PCC, (b) grid current, (c) active power of the VSI, and (d) reactive power of the VSI as a grid inductance of* $2.5mH$ *is added at instant* $0.1s$ *to an already present* $2.5mH$ *grid inductance without the adaptive virtual inductance feedforward scheme enabled.*

adaptive virtual inductance feedforward scheme was not employed in the scenario depicted in Fig. 5.5. At instant $0.1s$, a $2.5mH$ grid inductance was inserted into the system making the total grid inductance $5mH$, which resulted in the grid-tied system becoming unstable

as no stabilization technique was employed. The adaptive virtual inductance feedforward will be enabled in the remaining scenarios to keep the system stable under such weak grid conditions.

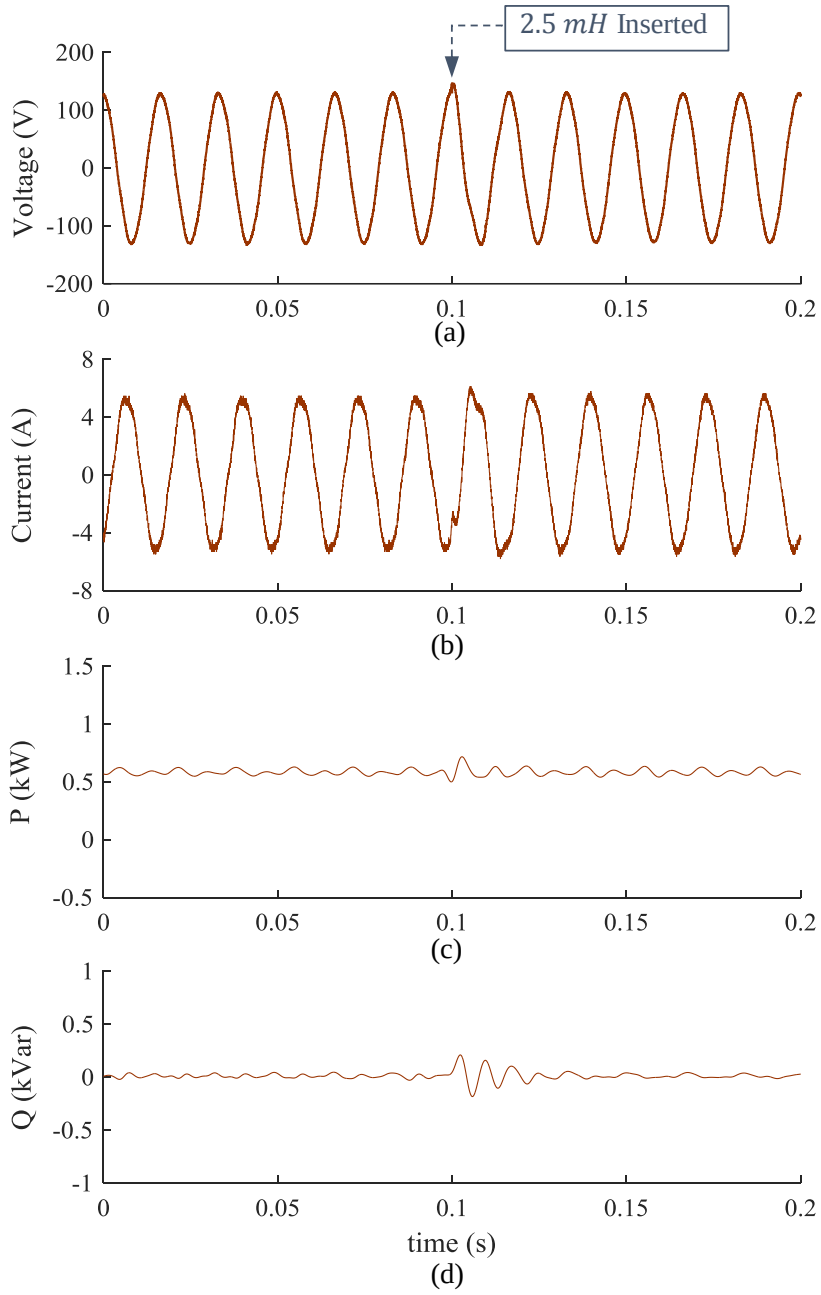


Figure 5.6: *(a) Voltage at the PCC, (b) grid current, (c) active power of the VSI, and (d) reactive power of the VSI as a grid inductance of* $2.5mH$ *is added at instant* $0.1s$ *to an already present* $2.5mH$ *grid inductance with the developed adaptive virtual inductance feedforward scheme enabled.*

The adaptive virtual inductance feedforward scheme was activated for the scenario depicted in Fig. 5.6. As one can see from the circuit waveforms shown in Fig. 5.6, the presented scheme kept the system in the stable region following the insertion of a $2.5mH$ grid inductance at instant $0.1s$, which made the total grid inductance equal to $5mH$. The screen capture of the oscilloscope waveforms for this scenario is shown in Fig. 5.7. This scenario is also depicted in the scope screen of the experimental setup shown in Fig. 5.4.

In the scenario presented in Fig. 5.8, the performance of the developed adaptive virtual inductance scheme is verified under different weak grid conditions. The circuit waveforms for this scenario are shown in Fig. 5.8 as the system can initially be seen to be stable under $L_g = 2.5mH$, with the adaptive virtual inductance scheme active. At instant $0.1s$, a grid inductance of $2.5mH$ was inserted into the circuit following which an additional grid inductance of $2.5mH$ was inserted at instant $0.14s$ making the total grid inductance $7.5mH$. As one can see from Fig. 5.8, the adaptive virtual inductance was able to keep the system in the stable region under consecutive step increases in grid inductance in quick succession by adjusting the virtual inductance value adaptively to retain the response of the system as close to the reference model as possible. Therefore, the adaptive virtual inductance scheme integrated with direct MRAC improves the virtual inductance scheme presented in Chapter 4

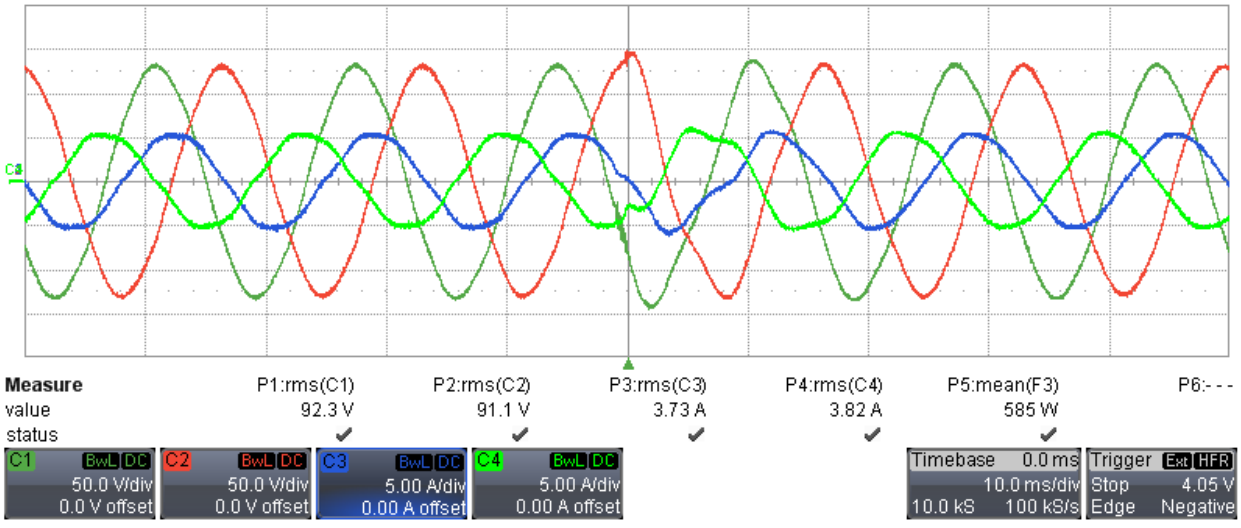


Figure 5.7: *Oscilloscope screen capture of the scenario presented in Fig. 5.6.*

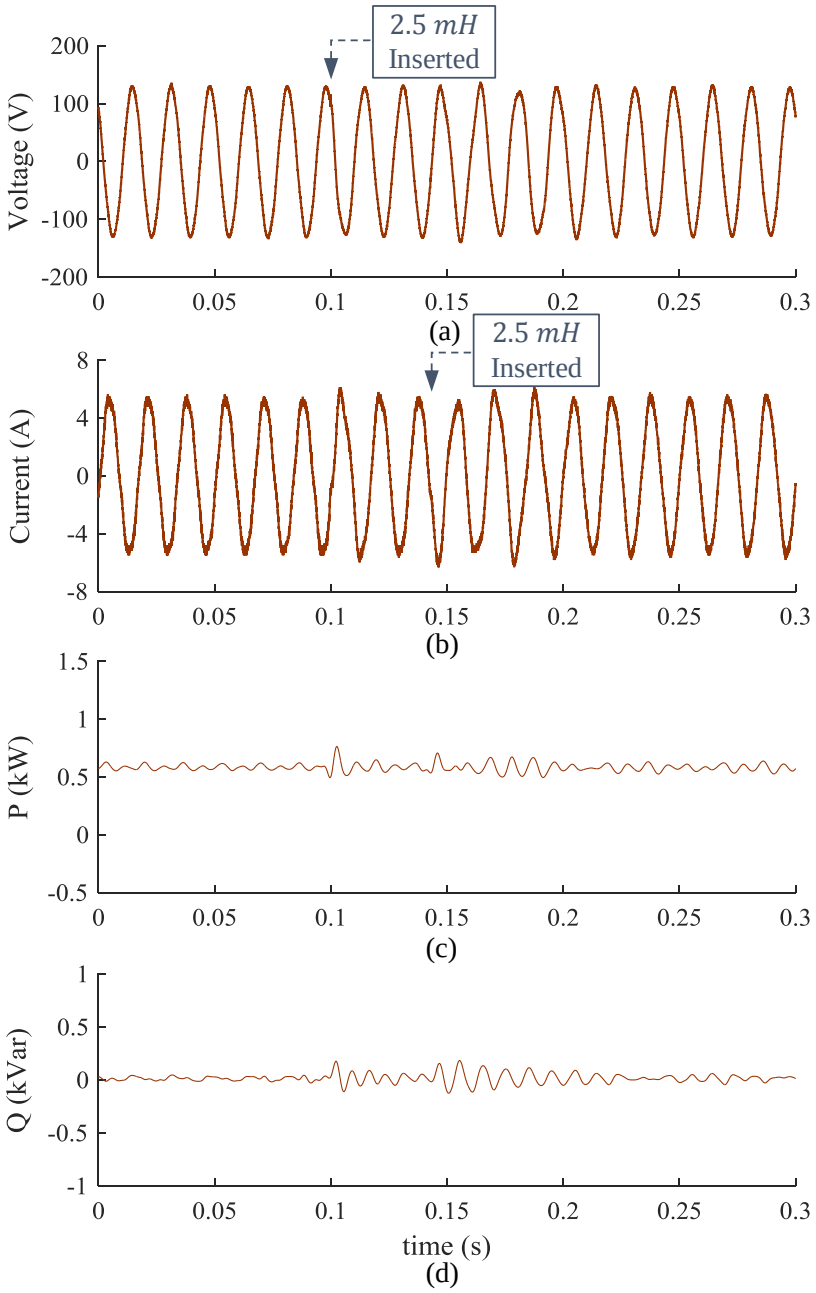


Figure 5.8: *(a) Voltage at the PCC, (b) grid current, (c) active power of the VSI, and (d) reactive power of the VSI at* $L_g = 2.5mH$ *as a grid inductance of* $2.5mH$ *is inserted at instant* $0.1s$ *followed by the insertion of an additional* L_g *of* $2.5mH$ *at instant* $0.14s$ *with the developed adaptive virtual inductance feedforward scheme enabled.*

by making the virtual inductance adaptable to various system operating conditions and thus making it more suitable for practical applications.

5.5 Conclusion

In this chapter, an adaptive virtual inductance feedforward scheme has been developed combining the virtual inductance scheme derived in the previous chapter with a direct MRAC scheme, to adaptively choose the virtual inductance value for enabling stable operation under various weak grid conditions. The critical grid inductance value that makes a grid-tied system unstable depends on the operating conditions of the system, thereby making the selection of a virtual inductance for stability difficult to perform, both manually and through grid impedance estimation techniques. In this chapter, a direct MRAC scheme has been integrated with the virtual inductance feedforward scheme to adaptively tune the virtual inductance such that the response of the system follows a stable reference model. The efficacy of the presented adaptive virtual inductance scheme has been verified through hardware tests performed on a grid-tied experimental setup.

Chapter 6

Atypical Pulse Width Modulation Scheme

In this chapter, an atypical PWM technique is presented to maximize the dc-bus utilization of VSIs providing ancillary services. The linear modulation region of inverters are restricted by the dc-bus voltage, therefore providing symmetrical and asymmetrical ancillary services may drive the positive-sequence fundamental inverter voltage to the overmodulation region, resulting in low-order harmonics being introduced to the system. To operate in the linear modulation region while providing ancillary services, the positive-sequence fundamental voltage then has to be reduced that would, in turn, limit the active and reactive power a grid-tied VSI can supply. In this dissertation, an atypical PWM method is developed to maximize the active and reactive power a grid-tied VSI can supply while providing ancillary services by injecting a common-mode component to the PWM references computed based on instantaneous reference magnitudes. The proposed technique can be implemented with any control structure employing carrier-based PWMs.

The contents of this chapter are organized into five sections. In Section 6.1, the control scheme of a grid-tied VSI providing ancillary services is discussed. The atypical PWM technique for grid-tied VSIs is developed in Section 6.2. The presented technique is verified through simulation and experimental studies in Sections 6.3 and 6.4, respectively. Finally,

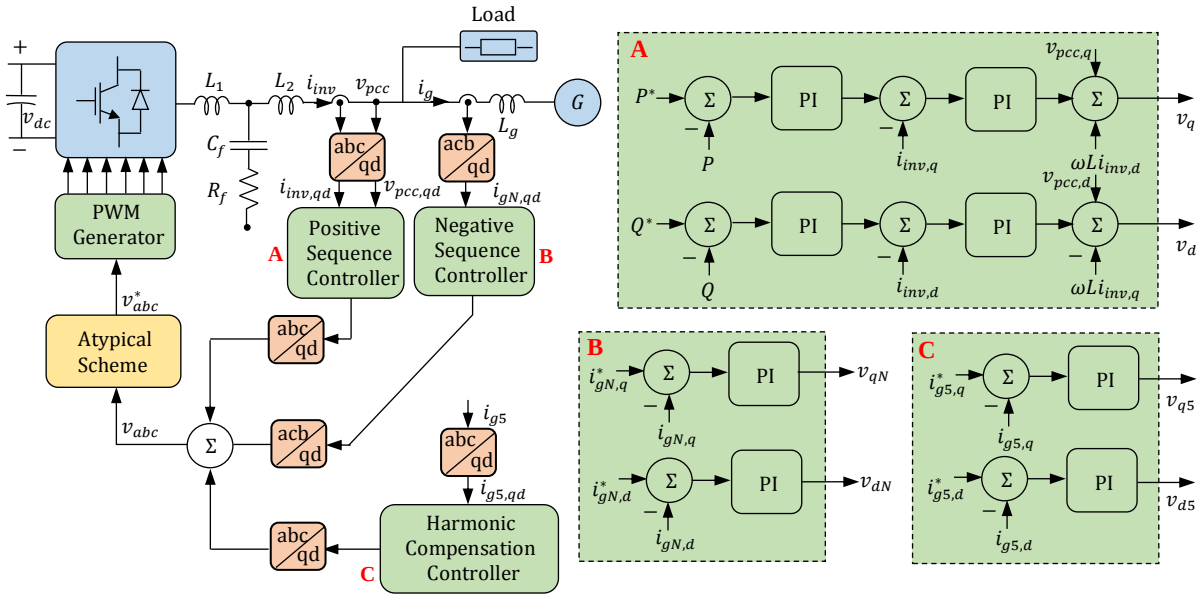


Figure 6.1: *Schematic diagram of a grid-tied VSI along with detailed block diagrams of positive sequence, negative sequence, and harmonic compensation controllers.*

concluding remarks are presented in 6.5.

6.1 Control Scheme for Ancillary Services

Two ancillary services are considered in this chapter. Harmonic compensation is considered as an instance of symmetrical services, while negative-sequence compensation is included as an instance of asymmetrical ancillary service. The control scheme of a grid-tied VSI supplying active and reactive power is illustrated in Fig. 2.6. The updated control scheme of a grid-tied VSI also providing negative-sequence and harmonic compensation is presented in Fig. 6.1. It can be seen from Fig. 6.1 that separate set of independent controllers are integrated into the control scheme to provide negative-sequence and harmonic compensation. The outputs of the controllers are then added to obtain the references for PWM generation [40].

The positive-sequence controller employed in Fig. 6.1 is the same one presented in Fig. 2.6. However, since an unbalanced system is considered in this chapter, the full three-phase form of the Park's transformation, shown in (6.1), is used to calculate the *dq* components of the

positive-sequence signals.

$$T^{+} = \frac{2}{3}\begin{bmatrix} cos(\theta) & cos(\theta - 2\pi/3) & cos(\theta - 4\pi/3) \\ sin(\theta) & sin(\theta - 2\pi/3) & sin(\theta - 4\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{6.1}$$

The instantaneous phase angle θ is obtained using a PLL with the voltage at the PCC as reference. Following controller operation, an inverse transform of the matrix provided in (6.1) is used to determine the positive-sequence components of the inverter voltage.

To compensate the negative-sequence component of the grid currents, three-phase grid currents i_g are sensed and their negative-sequence dq components are obtained using the negative-sequence dq transform expressed as follows:

$$T^{-} = \frac{2}{3}\begin{bmatrix} cos(\theta) & cos(\theta - 4\pi/3) & cos(\theta - 2\pi/3) \\ sin(\theta) & sin(\theta - 4\pi/3) & sin(\theta - 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{6.2}$$

Based on the calculated negative-sequence component of the grid currents, caused by the presence of an asymmetrical load or an asymmetrical grid fault, the inverter generates a negative-sequence voltage using the negative-sequence compensation controllers to provide the required negative-sequence current component, resulting in balanced grid currents.

Harmonic compensation is provided using a separate harmonic compensation controller operating in the dq frame of reference as shown in Fig. 6.1. The compensation of fifth order harmonics is considered in this chapter, while a distorted grid is considered as the source of fifth harmonics. Following the same principle, independent compensators of different order can also be introduced if necessary. To determine the q and d components of the grid current fifth harmonic, the positive-sequence dq transformation shown in (6.1) is used with a reference angle employing five times the fundamental frequency, i.e. 5θ. The acquired fifth harmonic components are then sent to the harmonic compensation controller, which produces a fifth harmonic voltage with magnitude and phase equal to that of the grid harmonic voltage. The

fifth harmonic voltage component is then superimposed on the fundamental inverter voltage to generate the final inverter voltage, thus eliminating any path for fifth order harmonic currents to flow. Due to the presence of negative-sequence voltage components, the generated references may become asymmetrical, which would make traditional common-mode injection techniques such as third-harmonic injection, unsuitable. A more flexible common-mode injection approach applicable to both symmetrical and asymmetrical references is presented in the next section.

6.2 Derivation of Atypical Scheme

In this section, the atypical PWM method for maximizing the dc-bus utilization of VSIs providing symmetrical and asymmetrical ancillary services is developed. The method is realized through injecting a common-mode component to the PWM references based on instantaneous reference magnitudes.

For a typical carrier-based PWM, which does not utilize any common-mode components, the reference signals can be expressed as follows:

$$v_x = \frac{m v_{dc}}{2} sin(\omega t - \varphi_x), x \in a, b, c \tag{6.3}$$

where, v_{dc} is dc-bus voltage, m is the modulation index, and φ_x is 0, $2\pi/3$ and $4\pi/3$ for phases a, b, and c, respectively. A VSI is operating in the linear modulation region if $|\hat{v}_x| \leq v_{dc}/2$, where $\hat{v}_x$ is PWM reference of peak phase-x. Therefore, while functioning in the linear modulation region a VSI's maximum line-to-line voltages are reached when $|\hat{v}_x| = v_{dc}/2$ for some $x \in a, b, c$, if no common-mode component is used to adjust PWM references. Accordingly, the maximum positive sequence component of the PWM references has to be reduced to operate in the linear modulation range, when additional components associated with different compensation services are required. To avoid this issue, a common-mode component can be defined, allowing adjusted references to be generated.

For a set of PWM references at an angle θ_0, a common-mode component is required for

operation in the linear modulation region when $|\hat{v}_x| > v_{dc}/2$ for some $x \in a, b, c$, i.e. when phase-x PWM reference has reached the overmodulation region. Denoting k as the phase for which over-modulation occurs as follows:

$$k = \underset{x \in a,b,c}{\text{argmax}}(|\hat{v}_x(\theta_0)|), \tag{6.4}$$

the minimum common-mode voltage required to place $v_k(\theta_0)$ in the linear modulation region can be computed as follows:

$$v_o(\theta_0) = \begin{cases} v_k(\theta_0) + v_{dc}/2, & v_k(\theta_0) < -v_{dc}/2 \\ v_k(\theta_0) - v_{dc}/2, & v_k(\theta_0) > v_{dc}/2 \\ 0, & \text{otherwise} \end{cases} \tag{6.5}$$

where, the common-mode component is defined as $v_o(\theta_0)$. It can be seen from (6.5) that the generated common-mode component is only functions of v_{dc} and $v_k(\theta_0)$. Therefore, the frequency spectrum of the common-mode component is that of $v_k(\theta_0)$, which consists of a large fundamental frequency component along with lower order harmonic components for harmonic compensation. Since, the sampling frequency of the control scheme is in the kHz range, which is much higher than the low-order harmonic components, potential effects of interaction between them is avoided. The modified PWM references following the injection of common-mode components can be expressed as follows:

$$v_x^*(\theta_0) = v_x(\theta_0) - v_o(\theta_0), x \in a, b, c. \tag{6.6}$$

Atypical PWM references generated using (6.6) when the VSI is providing negative-sequence compensation are plotted in Fig. 6.2, along with the unadjusted PWM references. From Fig. 6.2, the atypical references may appear distorted and clamped, however, the distortion does not appear in the line-to-line voltages and hence the currents, as the same common-mode component is injected into all three phases of the PWM reference. Inserting the common-mode component in all three phases can also be seen in min-max sequence

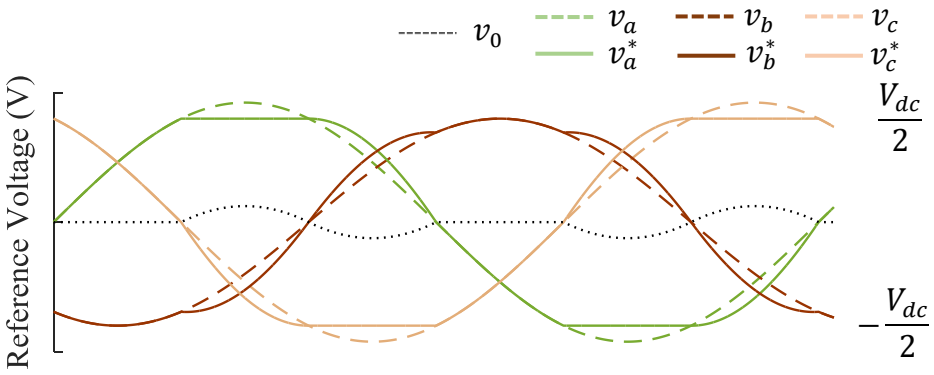


Figure 6.2: *Atypical PWM references, v_x^*, generated using the proposed technique and compared to the unadjusted references, v_x when providing negative-sequence compensation.*

common-mode injection techniques. However, the common-mode generation follows an entirely different procedure in mix-max sequence and more importantly, as opposed to the proposed technique the mix-max sequence injection is only applicable for symmetrical components [44, 85]. A common-mode injection technique applicable to symmetric and asymmetric components can be found in [86]. However, it is formulated for cascaded H-bridge multilevel inverters.

As one can see from Fig. 6.2, the conventional PWM references are in the overmodulation region, whereas the references generated using the proposed scheme remains clamped at $v_{dc}/2$, since for $|v_k(\theta_0)| > v_{dc}/2$, applying $v_o(\theta_0)$ as in (6.5) and (6.6) result in $|v_k(\theta_0) - v_o(\theta_0)| = |v_k^*(\theta_0)| = v_{dc}/2$.

The $v_x^*(\theta_0)$ are guaranteed to be in the linear-modulation region provided that:

$$|v_x(\theta_0) - v_y(\theta_0)| \leq v_{dc}; x, y \in a, b, c \tag{6.7}$$

To determine the increase in dc-bus utilization using the developed scheme for symmetrical references, different combinations of the PWM references from (6.3), multiplied by a factor F, are plugged in (6.7) as follows:

$$|F\frac{mv_{dc}}{2}sin(\omega t - \varphi_x) - F\frac{mv_{dc}}{2}sin(\omega t - \varphi_y)| \leq v_{dc}, \tag{6.8}$$

where, F is the increased utilization factor and $\varphi_x \in 0, 2\pi/3, 4\pi/3 \neq \varphi_y \in 0, 2\pi/3, 4\pi/3$. Performing trigonometric simplifications, the magnitude of the left-hand side of (6.8) for $m = 1$ comes out to be $Fv_{dc}(\sqrt{3}/2)$. Equating this term to the right-hand side of (6.8), the maximum value of the increased utilization factor comes out to be 1.155. In other words, the developed scheme enables up to a 15.5% increase in dc-bus utilization when providing symmetrical ancillary services such as harmonic compensation at rated power.

For asymmetrical references, assuming asymmetry is present in one phase, the asymmetrical reference can have a 30.1% increase for $m = 1$, which is a factor of 1.310 for the condition presented in (6.7) to hold. Now, the definition for voltage unbalance factor (VUF) recommended by IEC61000-4-27 [87] can be expressed as follows:

$$VUF = \sqrt{\frac{1 - \sqrt{3 - 6\beta}}{1 + \sqrt{3 - 6\beta}}}, \beta = \frac{V_a^4 + V_b^4 + V_c^4}{(V_a^2 + V_b^2 + V_c^2)^2}. \tag{6.9}$$

Replacing the PWM reference values in (6.9), i.e. $v_{dc}/2$ for two phases and $1.310v_{dc}/2$ for the other phase, the VUF in percentage comes out to be 20%. This value of VUF is also valid for different combinations of unbalance in multiple phases. The analysis herein is done for a modulation index of 1, whereas for a lower modulation index, the VUF can go higher and the proposed scheme can ensure operation in the linear modulation region for higher degrees of negative-sequence compensation.

Note that the proposed scheme does not influence inverter voltage generation through the controllers nor is it directly responsible for the generation of the gate pulses. It operates as an intermediate step between reference voltage and gate pulse creation. Therefore, the proposed atypical PWM scheme can be extended to work in conjunction with other control scheme and carrier-based PWM combinations of two-level VSIs.

6.3 Simulation Verification

In this section, the efficacy of the presented atypical PWM scheme is verified through simulations carried out in MATLAB/Simulink using the SimPowerSystems toolbox. The pa-

Table 6.1: *Simulation parameters for Section 6.3*

Parameter	Value
PWM carrier frequency	$10kHz$
Fundamental frequency	$60Hz$
$V_{LL,rms}$	$208V$
v_{dc}	$350V$
L_1	$1.0mH$
L_2	$1.0mH$
C_f	$10\mu H(\Delta)$
R_f	3.3Ω
C_d	$1800\mu F$

rameter values for simulation are provided in Table 6.1. The total inductance $(L_1 + L_2)$ of the filter is selected considering a voltage drop of $0.05p.u.$ across the filter, while $L_2 = L_1$ is selected for superior harmonic performance. To limit the decrease in the power factor of VSIs a commercially available standard capacitor value of less than 3% of its base impedance value was selected [77]. The resonance frequency f_{res} of the designed LCL filter also satisfies the stability criterion imposed on grid-tied VSIs with grid-side current feedback, i.e. $f_s/2 > f_res > f_s/6$, where f_s is the sampling frequency of the controller [88]. To mitigate the potential impact of resonance, a passive damping resistance is employed. For grid connection, a $208V_{rms}$ three-phase voltage source with a line impedance of 0.107Ω and a X/R ratio of 0.4 is used. An ideal dc voltage source is used as input to the VSI for a more general analysis. For all the scenarios presented in this section, the inverter is set to deliver its rated power of $18kW$ at unity power factor. The same analysis will be valid for lower power values with higher degrees of negative-sequence or harmonic compensation.

6.3.1 Negative-Sequence Compensation

The presented scheme is first tested under negative-sequence compensation scenarios. An asymmetry is introduced to the system in the form of an asymmetrical Δ connected $20kW$ resistive load with $R_{ab} = 5.408\Omega$, $R_{bc} = 5.408\Omega$, and $R_{ca} = 10.816\Omega$.

In the first scenario, the grid-tied VSI is supplying $18kW$ power to the asymmetrical load

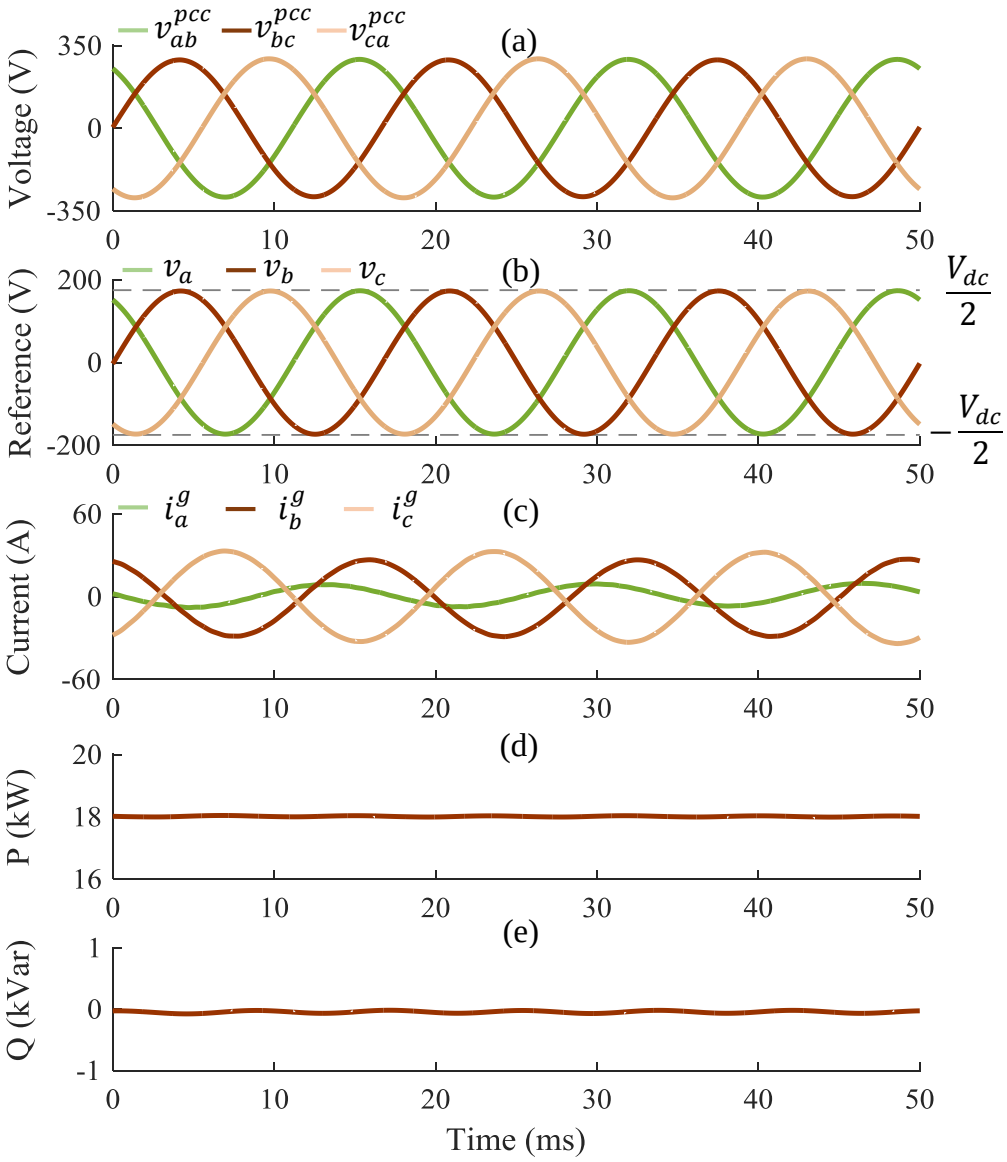


Figure 6.3: *(a) PCC voltages, (b) PWM references, (c) grid currents, (d) VSI active power, and (e) VSI reactive power when supplying 18 kW power to an asymmetrical load while no negative-sequence compensation is provided.*

without any negative-sequence compensation. The resulting PCC voltages, grid currents, PWM references, and the power supplied by the VSI are plotted in Fig. 6.3. It can be seen from Fig. 6.3 that the grid currents are significantly asymmetrical as the grid is supplying the negative-sequence components of the load currents. Alternately, the inverter references are symmetrical as only the positive-sequence component of the controller is operational.

The waveforms are plotted in Fig. 6.4 as the negative-sequence controller of the VSI

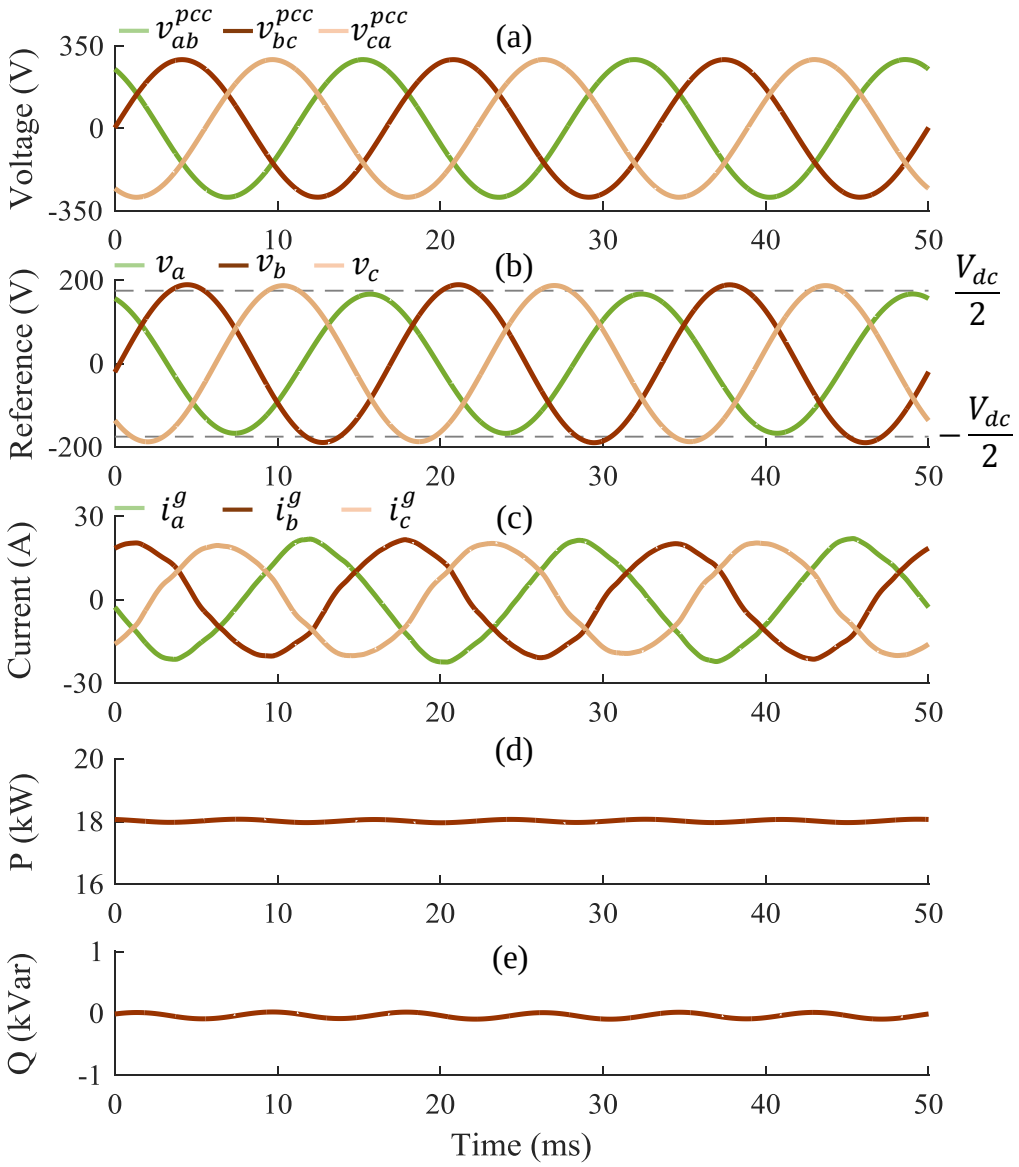


Figure 6.4: *(a) PCC voltages, (b) PWM references, (c) grid currents, (d) VSI active power, and (e) VSI reactive power when supplying 18 kW power to an asymmetrical load while providing negative-sequence compensation without employing atypical PWM.*

is activated while providing $18kW$ power at unity power factor as can be seen from the asymmetrical PWM references generated without the atypical scheme. However, providing negative-sequence compensation at rated power moves the peak of the PWM references to the overmodulation region. As a result, noticeably distorted grid currents can be observed due to the presence of low order harmonic contents, which is typical in the overmodulation region.

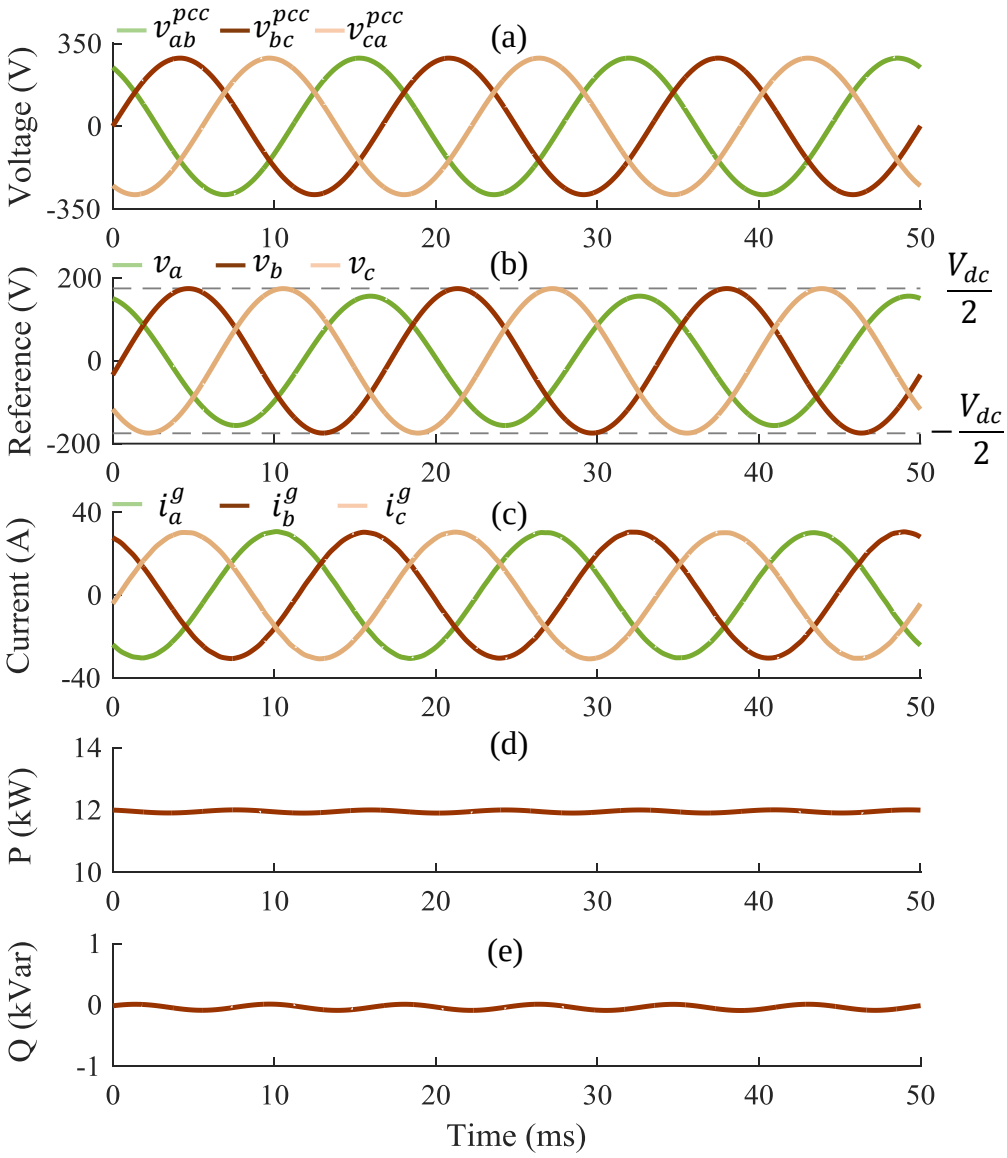


Figure 6.5: *(a) PCC voltages, (b) PWM references, (c) grid currents, (d) VSI active power, and (e) VSI reactive power when supplying 12 kW power to an asymmetrical load while providing negative-sequence compensation.*

To operate in the linear modulation region while providing negative-sequence compensation using conventional PWM, the inverter's positive-sequence component must be reduced, which in turn will reduce the active power output of the inverter. The PCC voltages, PWM references, grid currents, and the output powers of the inverter are shown in Fig. 6.5 as the active power of the VSI is reduced to $12kW$ at unity power factor to accommodate negative-sequence compensation services. It should be noted that the power supplied by the

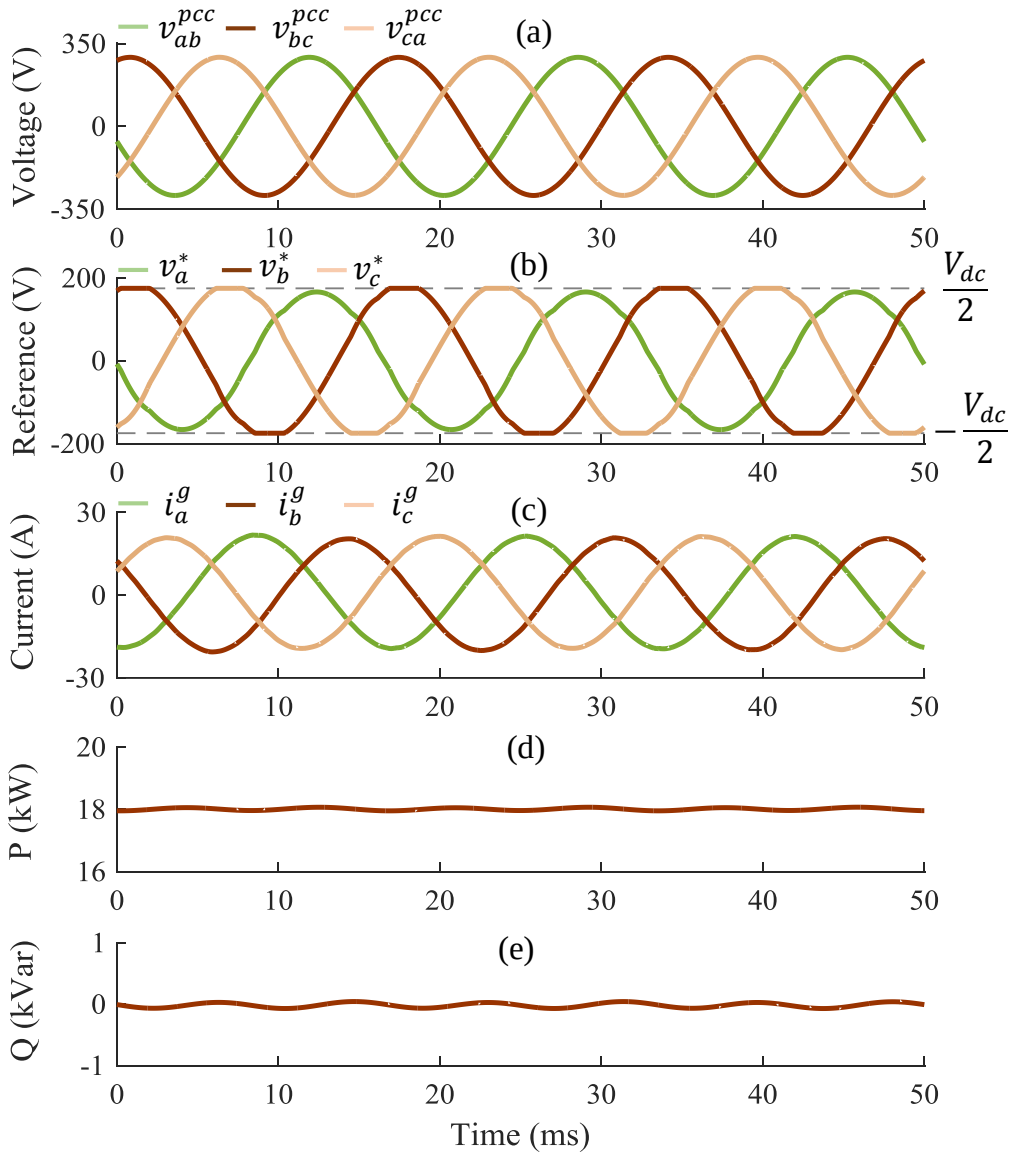


Figure 6.6: *(a) PCC voltages, (b) PWM references, (c) grid currents, (d) VSI active power, and (e) VSI reactive power when supplying 18 kW power to an asymmetrical load, while providing negative-sequence compensation employing the atypical PWM scheme.*

VSIs are shown in the figures in this subsection, while the currents being displayed are the grid currents. Therefore, as the inverter power output decreases the grid current increase to compensate for the load demand. The atypical PWM scheme developed in Section 6.2 can be utilized as an alternate technique to enable operation in the linear-modulation region while providing negative-sequence compensation without requiring this significant decrease in the supplied active power.

The waveforms displayed in Fig. 6.6 were obtained as the VSI is supplying $18kW$ power to an asymmetrical load at unity power factor while providing negative-sequence compensation utilizing the presented atypical PWM scheme. As one can see from Fig. 6.6, the resulting grid currents are symmetrical in this case and do not contain any low order harmonic content, as the atypical scheme ensures that the PWM references operate in the linear modulation region.

The performance of the atypical PWM scheme is then tested as delta-connected resistances R_{bc} and R_{ca} were independently varied up to 30% from a nominal resistance of 6.5Ω, selected to create a $20kW$ load with various degrees of asymmetry. Once again, for all the different unbalance conditions the VSI was set to deliver $18kW$ at unity power factor while also providing negative-sequence compensation employing the atypical scheme. For each asymmetrical configuration, the THD of all three phases of the grid currents were calculated and then averaged, and the results are displayed in Table 6.2. As one can see from the THD values presented in Table 6.2, the calculated THD values are within acceptable limits for all load unbalance cases considered, demonstrating the efficacy of the presented PWM scheme under asymmetrical ancillary services.

The developed atypical PWM scheme can also deliver superior performance while providing negative-sequence compensation under asymmetrical grid voltage sags, which typically result from single phase to ground faults. The three-phase voltage profile of a VSI, connected to the grid through a distribution transformer, is shown in Fig. 6.7(a) for a single phase to ground fault [9]. As one can see from Fig. 6.7(a), the voltages at the PCC are clearly

Table 6.2: *Grid current THD(%) for varying degree of load asymmetry*

R_{ca} \ R_{bc}	70%	85%	100%	115%	130%
70%	1.13	1.30	1.24	1.25	1.28
85%	1.48	1.34	1.62	1.41	1.33
100%	1.38	1.43	1.34	1.38	1.33
115%	1.45	1.43	1.26	1.31	1.22
130%	1.62	1.76	1.34	1.38	1.22

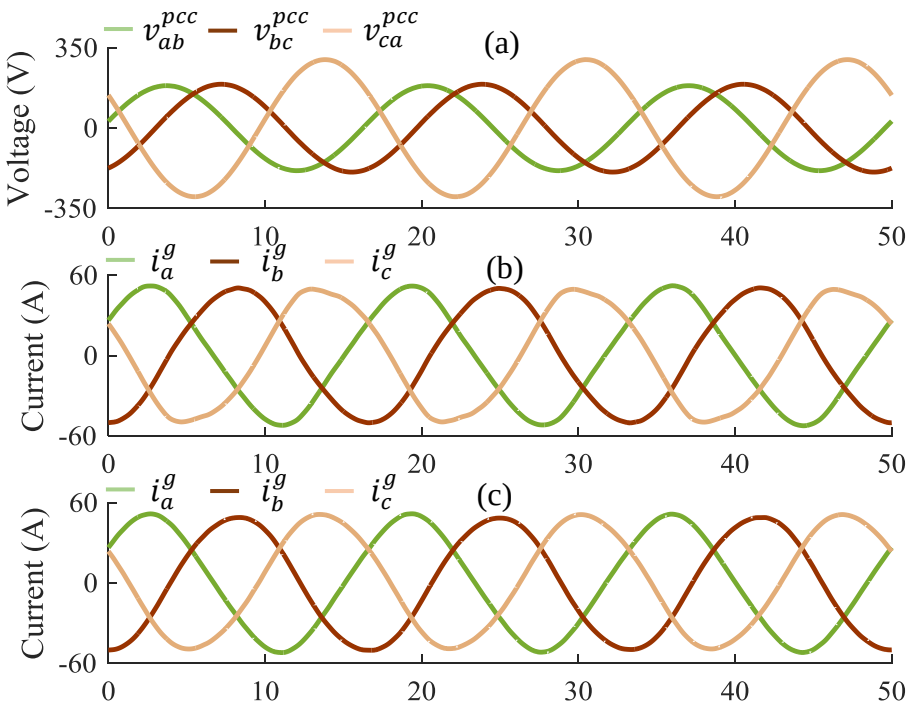


Figure 6.7: *(a) PCC voltages, (b) grid currents using conventional PWM, and (c) grid currents using proposed atypical PWM while providing negative-sequence compensation under asymmetrical grid voltage sags.*

asymmetrical, which would cause asymmetrical grid currents unless negative-sequence compensation is provided. The grid currents while providing negative-sequence compensation under asymmetrical grid voltage sags with and without employing the atypical PWM scheme are shown in Figs. 6.7(b) and 6.7(c), respectively. It can be seen from Fig. 6.7 that the grid currents without using the proposed scheme contain low-order harmonics due to overmodulation while the currents obtained using the presented scheme is balanced and clean.

6.3.2 Harmonic Compensation

To demonstrate the usefulness of the proposed scheme while providing harmonic compensation, a distorted grid voltage with a fifth harmonic component of $0.05pu$ is considered as an input to the grid-tied VSI. The applied distorted grid voltage will cause severely distorted grid currents with low-order harmonics. To eliminate the fifth harmonics associated with the

grid currents, a fifth harmonic compensation controller is employed by the VSI operating at the synchronously rotating dq frame of reference.

In the scenario presented in Fig. 6.8, the grid voltages, PWM references, grid currents, and VSI active and reactive power are shown as the VSI is supplying $18kW$ at unity power factor while providing fifth harmonic compensation using conventional PWM due to distortions

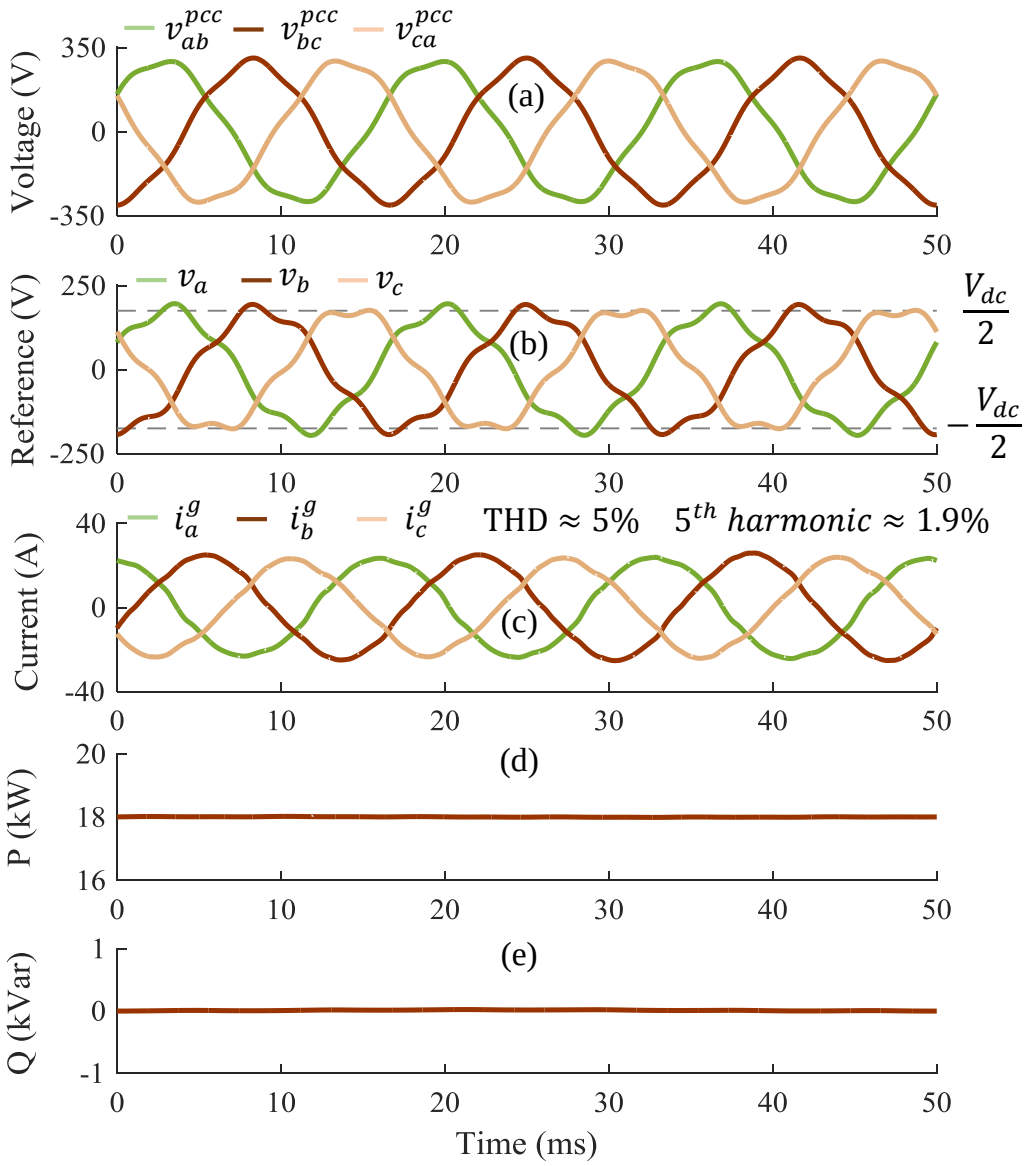


Figure 6.8: *(a) Grid voltages, (b) PWM references, (c) grid currents, (d) VSI active power, and (e) VSI reactive power when supplying 18 kW power to its load while providing fifth harmonic compensation without the atypical PWM scheme.*

resulting from a grid voltage with fifth order harmonics. As one can see from Fig. 6.8, the harmonic compensation controller reduces the fifth harmonic component of the currents to an acceptable limit, i.e. 1.9%, however, the THD of the currents is still at a large value, i.e. 5%. This results from the other lower order harmonics, e.g. third, seventh, eleventh, ninth, and thirteenth, being introduced to the grid currents as the PWM references reach the

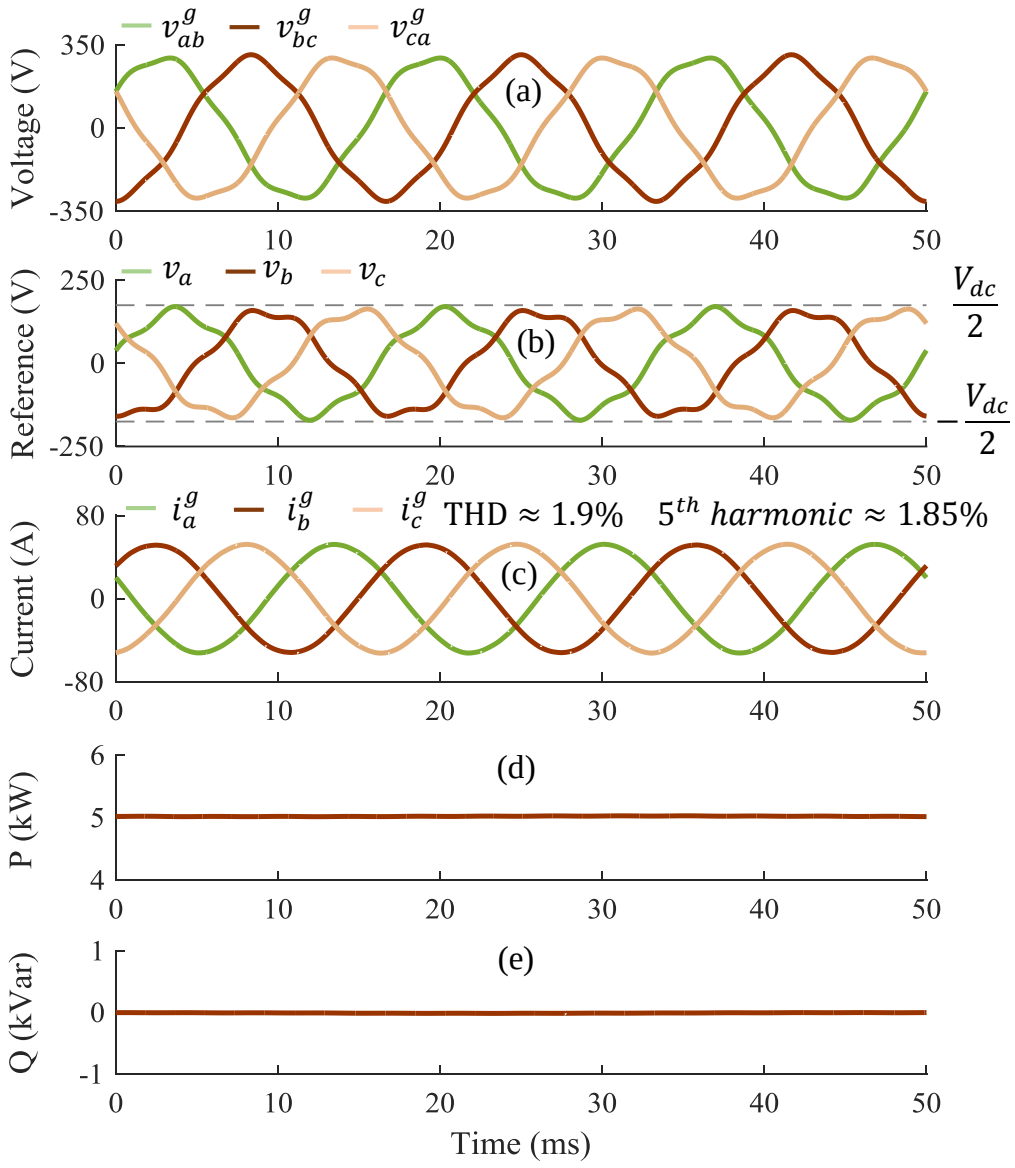


Figure 6.9: *(a) Grid voltages, (b) PWM references, (c) grid currents, (d) VSI active power, and (e) VSI reactive power when supplying 5 kW power to its load while providing fifth harmonic compensation.*

overmodulation region while providing harmonic compensation at rated power. Harmonic compensators of different orders can be added to the control scheme to eliminate the other dominant lower order harmonics, but this, in turn, will drive the PWM references further into the overmodulation region and the harmonic components of the remaining uncompensated lower order harmonics will increase even further.

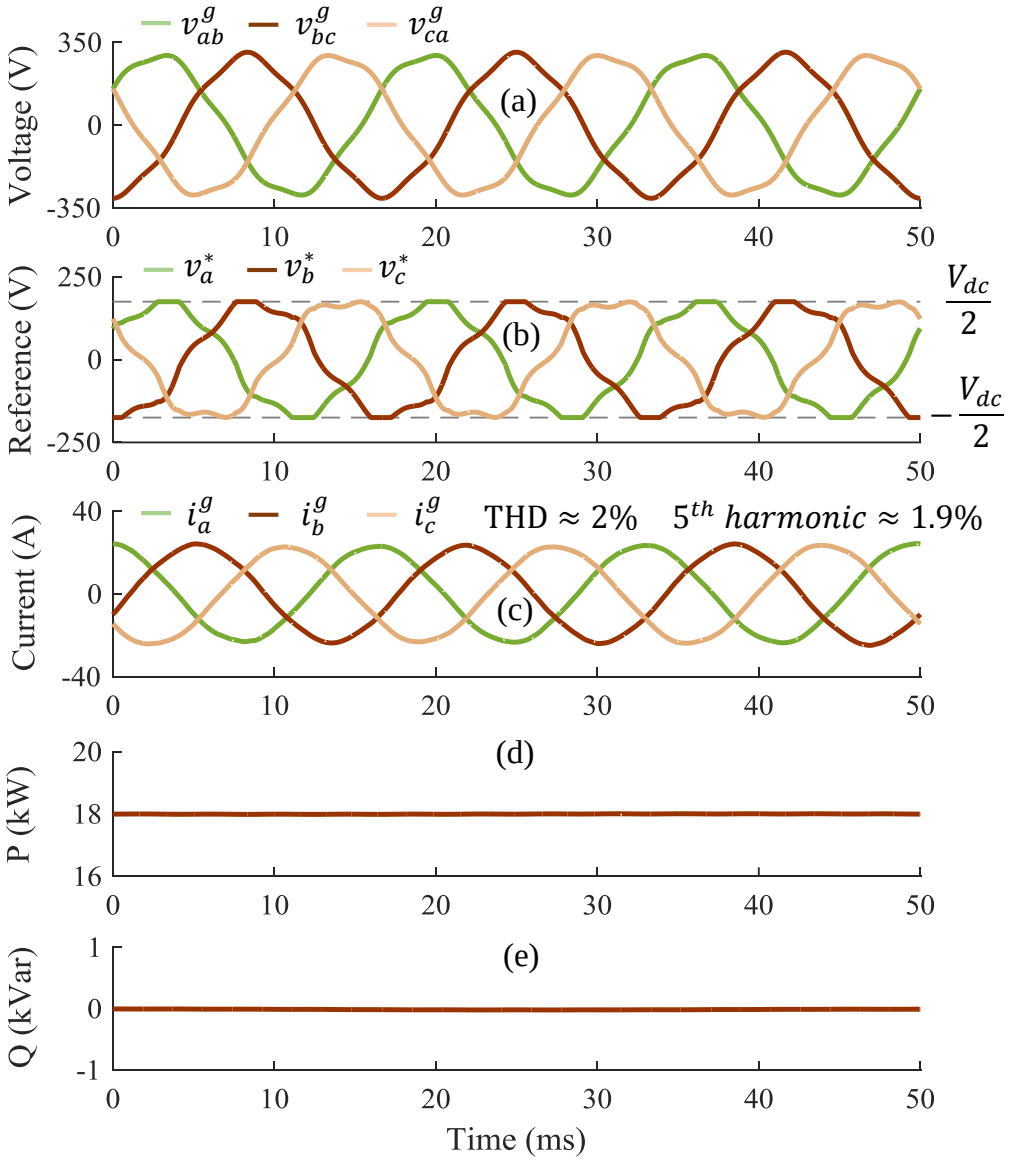


Figure 6.10: *(a) Grid voltages, (b) PWM references, (c) grid currents, (d) VSI active power, and (e) VSI reactive power when supplying 18 kW power to its load while providing fifth harmonic compensation utilizing the atypical PWM scheme.*

Similar to the case of negative-sequence compensation, the grid-tied VSI can be operated in the linear modulation region through conventional PWM by reducing the positive-sequence fundamental component as shown in Fig. 6.9. As one can see from Fig. 6.9, the VSI active power has to be reduced to $5kW$ to operate the inverter at linear modulation, which is significantly lower than its rated power of $18kW$. Alternatively, the developed atypical scheme can be employed.

The waveforms are presented in Fig. 6.10 as the VSI is supplying $18kW$ active power at unity power factor while providing fifth harmonic compensation using the atypical PWM scheme. Contrary to the case of Fig. 6.8, grid currents with THD well below the maximum limit is achieved through the use of the presented scheme while providing fifth harmonic compensation at $18kW$. The THD values shown in these scenarios is the average current THD of the three phases. In the scenario presented in Fig. 6.10, the fifth harmonic component of the grid currents is compensated through the fifth harmonic compensation controller while the atypical PWM scheme ensures that the VSI is operating in the linear modulation region, thereby eliminating the other lower order harmonics and validating the efficacy of the presented scheme.

6.4 Experimental Verification

In this section, the developed atypical PWM scheme is verified via data collected using a $208V$ three-phase grid-tied setup. A $12kW$ Primate Power grid simulator was used as the three-phase grid for the tests carried out in this section. Grid voltages with various harmonic components can be generated using the grid simulator, which was beneficial for the harmonic compensation studies. The gate signals for the VSI were generated making use of the slave I/O unit of a dSpace 1103 Controller Board. The experimental setup is shown in Fig. 6.11. More details on the experimental setup can be found in Section 2.1.2. The parameter values employed for the hardware tests are provided in Table 6.3. The LCL filter values were chosen following the same procedure outlined in Section 6.4. Although the VSI unit is capable of supplying $20kW$ power, for all tests performed in this section the inverter was set to deliver

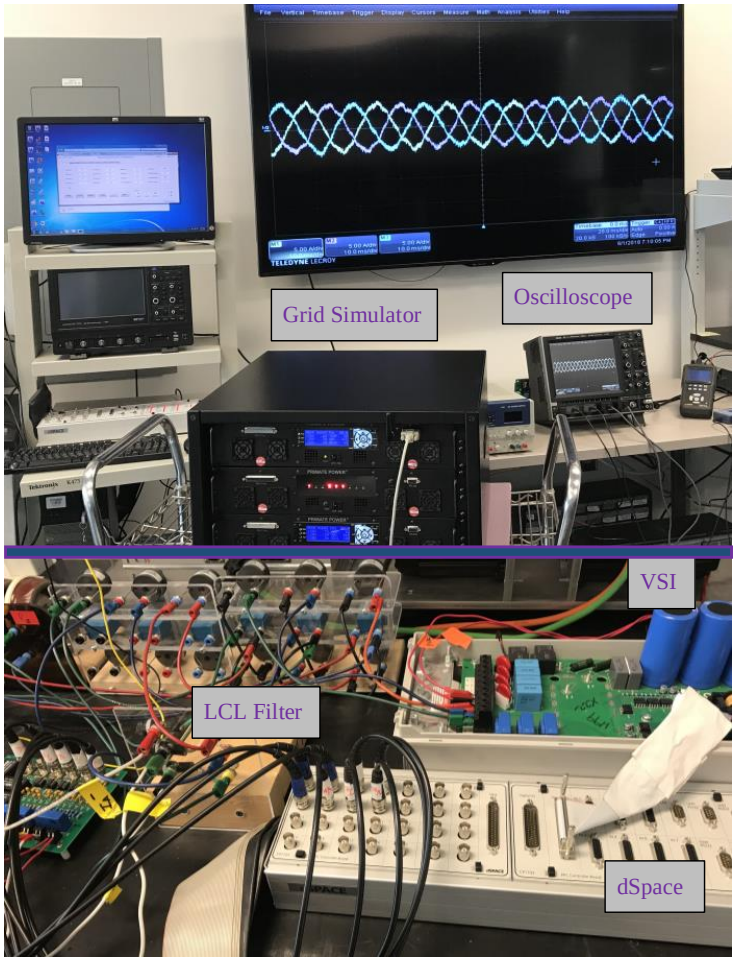


Figure 6.11: *Hardware setup used for the experimental scenarios in Section 6.4 with the scenario of Fig. 6.21 shown in oscilloscope.*

$500W$ at unity power due to constraints of the remaining laboratory equipment. The dc-bus voltage of the VSI was then varied to verify the increased dc-bus utilization property of the developed scheme.

6.4.1 Negative-Sequence Compensation

A $2kW$ asymmetrical load with $R_a = 24\Omega$, $R_b = 24\Omega$, and $R_c = 32\Omega$ was utilized as the source of asymmetry in the experiments carried out in this subsection. The three-phase grid voltages used for this subsection are shown in Fig. 6.12.

The grid currents shown in Fig. 6.13 were obtained as the VSI was providing $500kW$ to the asymmetrical load at unity power factor for a dc-bus voltage of $375V$, while no

Table 6.3: *Parameter values for Section 6.4*

Parameter	Value
PWM carrier frequency	$10kHz$
Fundamental frequency	$60Hz$
$V_{LL,rms}$	$208V$
L_1	$1.0mH$
L_2	$0.5mH$
C_f	$5\mu H(\Delta)$
R_f	3.3Ω
C_d	$1800\mu F$

negative-sequence compensation was provided. As one can see from Fig. 6.13, the grid currents are asymmetrical as they were providing the negative-sequence current required by the asymmetrical load, which can cause a deleterious effect in microgrid scale generators. The grid currents with negative-sequence compensation controller activated are shown in Fig. 6.14 as the VSI is providing $500W$ at unity power factor for the same dc-bus voltage. The developed atypical scheme was not used for the scenarios depicted in Figs. 6.13 and 6.14.

To demonstrate the improved performance of the presented scheme compared to traditional PWM schemes when providing asymmetrical ancillary services, the grid currents were measured as the inverter was providing $500W$ at unity power factor for a dc-bus voltage of $330V$. The results obtained without and with the atypical scheme applied is shown in Figs. 6.15 and 6.16, respectively. As one can see from Fig. 6.15, the grid currents without

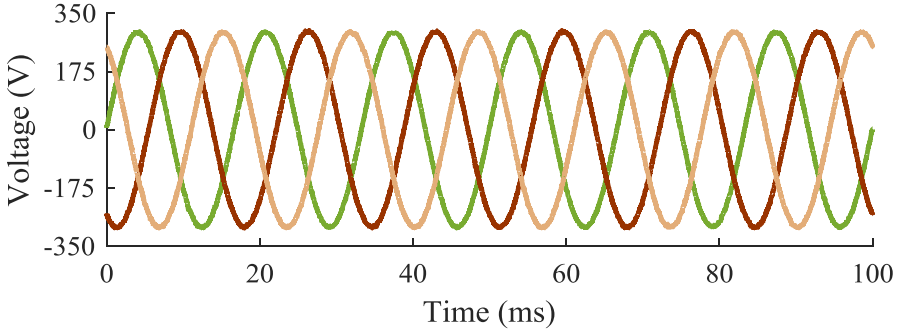


Figure 6.12: *Three-phase grid voltages for the hardware tests carried out in Subsection 6.4.1.*

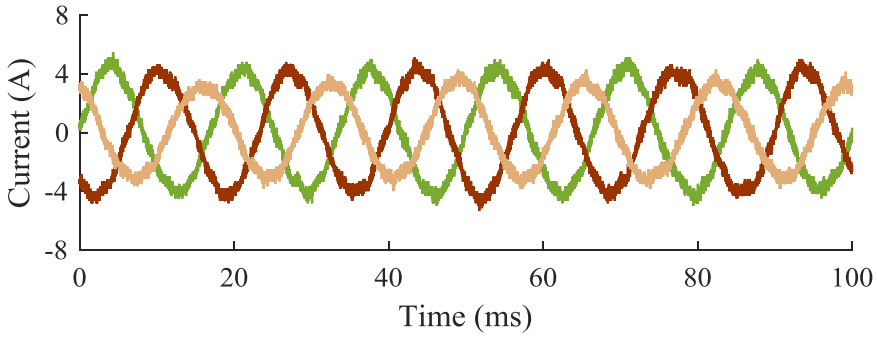


Figure 6.13: *Experimentally obtained grid currents without negative-sequence compensation when* $v_{dc} = 375V$.

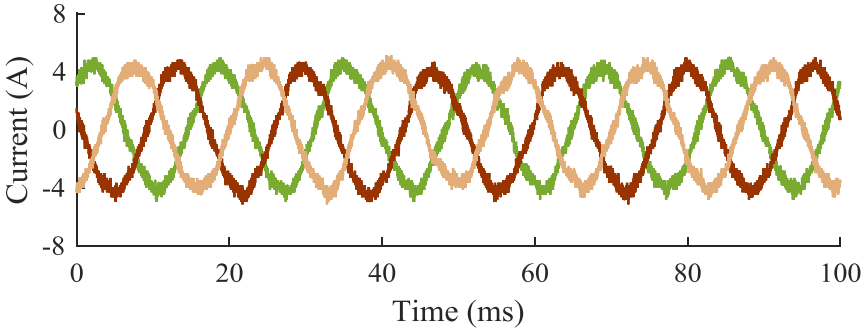


Figure 6.14: *Experimentally obtained grid currents with negative-sequence compensation provided by the inverter when* $v_{dc} = 375V$.

using the developed technique contain significant low-order harmonic content as the VSI has to operate in the overmodulation region to deliver the desired power while also providing negative-sequence compensation. On the other hand, the currents obtained using the atypical scheme is clean and balanced as can be seen from Fig. 6.16, since overmodulation is avoided for the same dc-bus voltage due to increased dc-bus utilization capability of the atypical scheme.

To further demonstrate the increased dc-bus utilization of the developed technique, the performance of the atypical scheme is compared with the conventional PWM scheme for a large range of dc-bus values when providing negative-sequence compensation. It should be noted that the dc-bus voltage was changed to demonstrate the effectiveness of the developed scheme, as constraints of the laboratory equipment ratings limited the maximum output

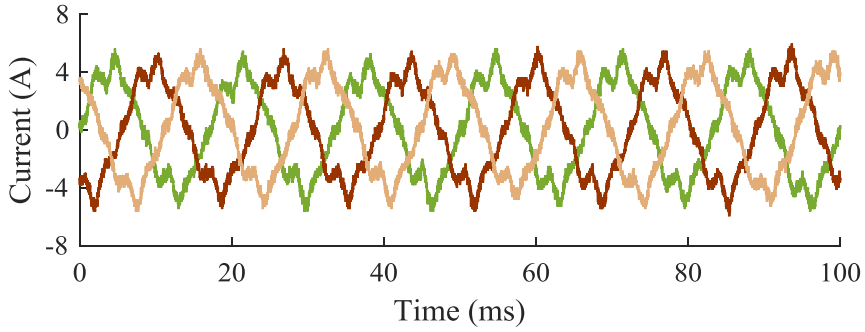


Figure 6.15: *Experimentally obtained grid currents with negative-sequence compensation when $v_{dc} = 375V$ and atypical PWM scheme is not used.*

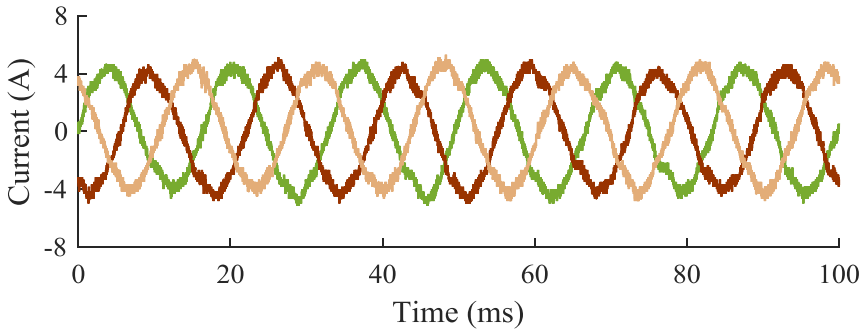


Figure 6.16: *Experimentally obtained grid currents with negative-sequence compensation when $v_{dc} = 375V$ and the atypical scheme is utilized.*

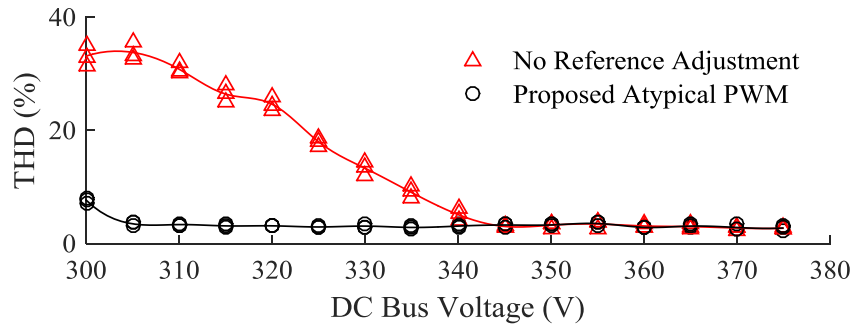


Figure 6.17: *Plot showing grid current THD vs. v_{dc} with and without using the atypical PWM scheme, with each dc-bus voltage tested at three different measurement times.*

power the inverter could provide. Grid currents drawn, while providing negative-sequence compensation both with and without the atypical scheme were measured at three separate occasions as the dc-bus voltage of the VSI was decreased in $5V$ steps from $375V$ to $300V$. The

average THD of the three phases of the grid currents were then calculated for both schemes. The results, which is illustrated in Fig. 6.17 show that the presented atypical scheme exhibit an acceptable THD value for a much larger range of dc-bus values, demonstrating that the atypical PWM scheme extends the linear modulation range of the VSI.

6.4.2 Harmonic Compensation

In this subsection, the efficacy of the atypical PWM scheme is validated when compensating fifth harmonic components of the grid currents caused by a $0.03p.u.$ fifth harmonic component present in the grid voltages, which are displayed in Fig. 6.18.

The fifth harmonic component of the grid currents, resulting from the distorted grid voltage, were compensated using a fifth harmonic compensation controller as shown in Fig. 6.19 while the VSI was delivering $500kW$ active power at unity power factor a dc-bus voltage of $375V$. It can be seen from Fig. 6.19 that the fifth harmonic content of the grid currents was effectively compensated through proper operation of the fifth harmonic compensator.

The grid currents when providing fifth harmonic compensation without the atypical PWM scheme for a dc-bus voltage of $320V$ is shown in Fig. 6.20. Although the fifth harmonic component of the grid currents was reduced to a low value (2%), the grid currents are still severely distorted as can be seen from Fig. 6.20, due to the presence of other lower order harmonic components, e.g. fifth, seventh, and eleventh, as the PWM references reach the overmodulation region. The grid currents obtained using the atypical PWM scheme for the

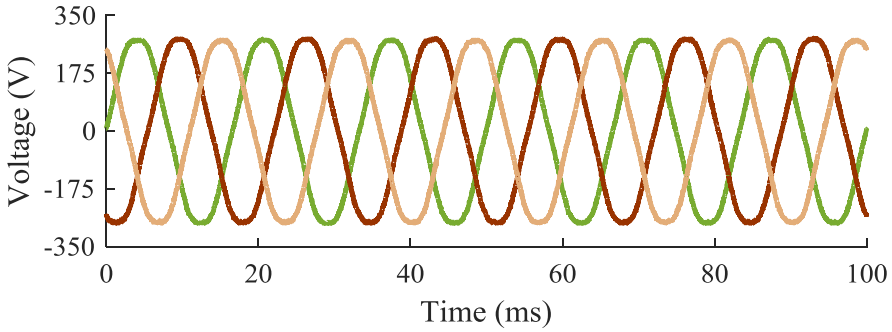


Figure 6.18: *Three-phase grid voltages with a fifth harmonic component of* $0.03p.u.$.

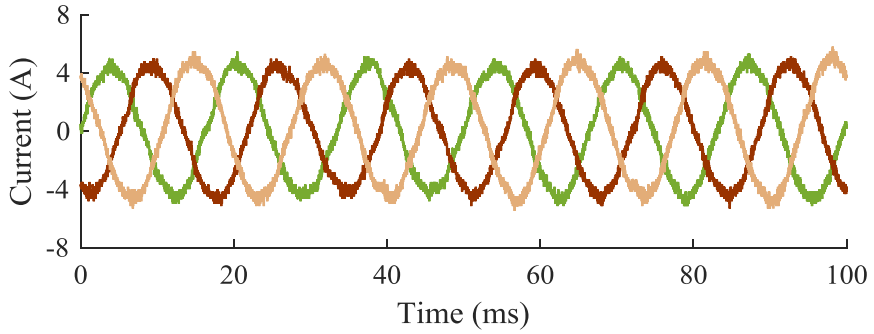


Figure 6.19: *Experimentally obtained grid currents with fifth harmonic compensation when* $v_{dc} = 375V$.

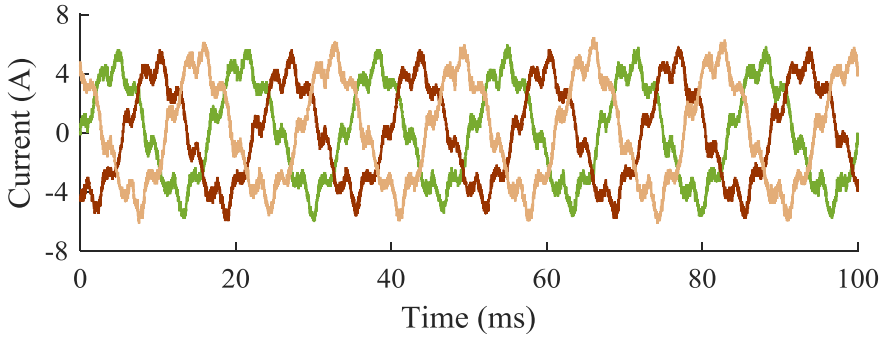


Figure 6.20: *Experimentally obtained grid currents with fifth harmonic compensation when* $v_{dc} = 320V$ *and the atypical scheme is not utilized.*

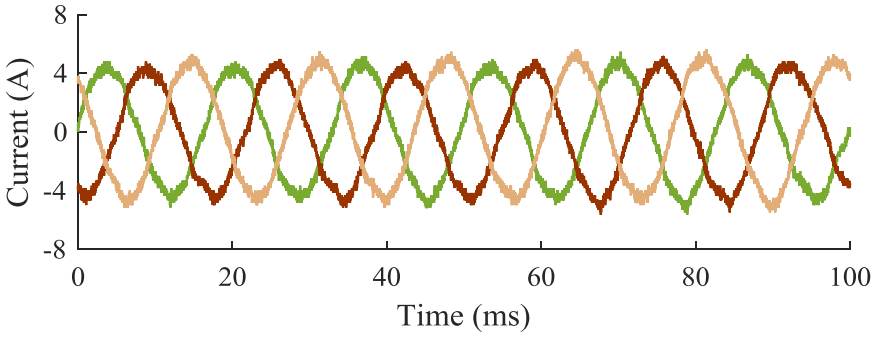


Figure 6.21: *Experimentally obtained grid currents with fifth harmonic compensation when* $v_{dc} = 320V$ *and the atypical scheme is utilized.*

same operating conditions are shown in Fig. 6.21. As one can see from Fig. 6.21, utilization of the presented scheme results in clean currents as operation in the overmodulation region is avoided while providing harmonic compensation, due to the increased dc-bus utilization

of the VSI. This increase in the linear modulation region means that the implementation of the atypical PWM scheme increases the maximum active and reactive power a VSI can provide for a given dc-bus voltage.

6.5 Conclusion

In this chapter, an atypical PWM method has been presented for grid-tied VSIs providing symmetrical and asymmetrical ancillary services. The presented technique increases the dc-bus utilization of the VSI by injecting a common-mode component in the PWM references computed based on instantaneous reference magnitudes. The presented scheme can be extended to any two-level VSI controller structure employing carrier-based PWMs. The validity of the atypical PWM scheme has been verified through tests carried out in simulation and in an experimental setup. It has been verified that the presented scheme facilitates the injection of maximum active power while the inverter is providing negative-sequence compensation and harmonic compensation services. The presented technique maximizes dc-bus utilization by maximizing the positive-sequence fundamental component the PWM references can contain without reaching overmodulation, thereby maximizing the power the inverters can deliver.

Chapter 7

Conclusions and Suggestions for Future Work

In this chapter, the contents of this dissertation are summarized with the contributions of the work highlighted. This chapter is organized into two sections. In Section 7.1, the summary of the dissertation is presented. In Section 7.2, suggestions for possible future work based are discussed.

7.1 Summary and Conclusions

In this dissertation, new control and switching techniques have been developed to enhance the stability and performance of grid-tied VSIs under abnormal grid conditions. The role of VSI as an essential interface for the grid integration of renewable energy sources has been discussed in Chapter 1. As has been discussed, along with extracting the maximum power from DG units, VSIs are capable of providing ancillary services such as negative-sequence compensation and harmonic compensation under grid abnormalities, which however could degrade the quality of the power being supplied to the grid. The grid-tied VSI could even become unstable due to the large impedance associated with a weak grid as depicted in many of the referenced works. The state-of-the-art regarding the aforementioned issues has also

been discussed in Chapter 1. The shortcomings of the existing techniques in literature and the necessity for new techniques to improve the stability and performance of grid-tied VSIs under abnormal grid conditions have also been emphasized.

A detailed full-order model of a grid-tied VSI equipped an LCL filter and a PQ controller has been developed in Chapter 2. The comprehensive nature of the developed model lends itself to be used for studies other than the ones carried out in this dissertation. The open-loop model and the controller model have been derived in separate steps. The open-loop model has a generalized structure, which allows it to be integrated with various controllers both in the grid-tied and islanded modes of operation. The open-loop model has been verified through both simulation and experimental results. The steps performed in this dissertation to integrate the open-loop and the controller model can also be recreated for the integration of different controllers.

The developed model has been utilized in Chapter 3 to study the effect of different system parameters on the stability of VSIs in weak grids. Through root locus of the model eigenvalues, it has been identified that increasing the passive damping resistance, controller time delay, and grid-side filter inductances can improve the stability of VSIs in weak grids. On the hand, the controller proportional gains and the filter capacitance have to be reduced for stability in weak grids. It should be noted that the effect of controller time delay and grid-side filter inductance is valid for systems with current measurements conducted after the LCL filter. The efficacy of some of the parameters in stabilizing the system in weak grids is validated through experimental studies. The tradeoff associated with redesigning the system parameters for stability has also been discussed.

A virtual inductance feedforward control scheme has been developed in Chapter 4 to enhance the stability of grid-tied VSIs in weak grids. The continued-fraction-expansion criterion has been applied on a simplified transfer function of the grid-tied VSI to verify the stabilizing impact of increased grid-side filter inductances in weak grids. A virtual inductance term has been derived emulating the effect of additional grid-side filter inductance to avoid the drawbacks associated with adding a larger inductor to the system. As has been discussed, the grid-side filter inductance is a good candidate to implement virtually as the current

flowing through the component is measured for normal controller operation. Therefore, the virtual inductance feedforward scheme can be implemented without requiring any additional sensors. The virtual inductance feedforward has been integrated with the PQ controller to develop a modified PQ controller that can extend the stability boundary of grid-tied VSIs in weak grids. The full-order model has also been modified to include the effect of virtual inductance. Root locus studies of the eigenvalues of the modified model have indeed shown that the virtual inductance feedforward scheme can extend the stability range of VSIs in weak grids. For the operating condition defined in Chapter 4, the presented scheme can ensure stable operation up to an SCR value of 2.1, whereas existing standards require stable operation up to an SCR of 10. The efficacy of the virtual inductance scheme has been validated through hardware tests carried out on a grid-tied experimental setup. The steady-state performance of the closed-loop system including virtual inductance feedforward has also been verified experimentally.

A direct MRAC method has been integrated to the virtual inductance feedforward scheme to adaptively vary the virtual inductance for changes in grid impedance in weak grids. As has been discussed, the direct MRAC method does not require a parameter estimation stage and can adapt the virtual inductance value according to a stable reference model. The balanced truncation technique has been employed to obtain a second-order model from the presented full-order model to select a reference model for the MRAC scheme. The adaptation law for a first-order system employing direct MRAC method has been derived first. It has then been updated for the grid-tied VSI system. The direct MRAC method is integrated to the PQ controller to develop a modified PQ controller with adaptive virtual inductance feedforward. The efficacy of the presented control scheme has been verified through hardware tests carried out for different weak grid conditions. The integration of the adaptive scheme in virtual inductance feedforward makes it more suitable for practical applications under varying operating conditions.

An atypical scheme has been presented in Chapter 6, to maximize the dc-bus utilization of grid-tied VSIs when providing ancillary services. As has been discussed, the presented scheme can extend the linear modulation range of VSIs, which allows maximum energy to be

extracted from the DG units while providing ancillary services. A control scheme containing negative-sequence and fifth harmonic compensators has been presented to achieve clean grid currents under distorted grid voltages and asymmetrical loads. The atypical PWM scheme has then been developed, which can be realized by injecting a common-mode component in the PWM references computed based on instantaneous reference magnitudes. The developed scheme can be integrated with other control schemes employing carried-based PWMs, as it only acts as an intermediary between the controller and the PWM generator. The efficacy of the developed scheme has been verified through simulation and experimental case studies while providing both negative-sequence compensation and harmonic compensation.

The simulation verifications of the developed techniques have been performed using MATLAB, while for circuit simulations the SimPowerSystems toolbox has been employed in this dissertation. The hardware tests have been carried out in a laboratory scale setup containing a commercial VSI drive.

In conclusion, an adaptive virtual inductance feedforward scheme and an atypical PWM scheme have been presented in this dissertation to improve the adaptability of VSIs under grid abnormalities, which would, in turn, allow more renewable energy based DG units to be integrated to the power grid. The limitations of existing techniques in handling concerns related to grid abnormalities have been discussed and the contributions of the developed techniques with respect to the state-of-the-art have been highlighted. The presented techniques are well suited to be employed for practical applications.

7.2 Suggestions for Future Work

The efficacy of the techniques presented in this dissertation has been thoroughly validated. There are, however, opportunities to build on the work presented herein.

The open-loop model presented in Chapter 2 has a generalized structure and therefore can be integrated with various controllers. The open-loop model can be integrated with a controller for the standalone mode of operation to obtain a standalone VSI model. Similar to the analysis carried out in this dissertation for a grid-tied system, the standalone model

can be also used to analyze the effect of different parameters on the stability of the system.

The adaptive virtual inductance feedforward scheme has been presented in this dissertation to improve the stability of VSIs in weak grids considering balanced grid impedances. A more uncommon phenomenon seen in practice is a weak grid with unbalanced impedances, which could result from non-uniformly distributed single-phase loads and non-symmetrical transformer windings. The presented virtual inductance scheme should still be able to improve the stability under asymmetrical weak grids, however, the power quality associated with the asymmetrical impedances would still remain. Therefore, a potential avenue of future research could be to update the virtual inductance scheme for asymmetrical cases.

The adaptive virtual inductance feedforward scheme is suitable for inductive and resistive-inductive grid impedances typical for transmission and distribution grids. On the other hand, for microgrids operating in standalone mode, the line impedances are predominantly resistive. Large line impedances in microgrids could deteriorate the stability microgrid-interactive VSIs. Therefore, another potential avenue of research could be updating the virtual inductance scheme for stability enhancement in resistive microgrids in the standalone mode of operation.

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Appendix A

Full-Order Model Matrix Equations

In this appendix, the grid-tied VSI state-space matrices, in the *abc* frame of reference, for all the SVPWM sectors are presented. In addition, the full-form of the block matrices introdcued in the full-order state-space models throughout the dissertation are also provided.

A.1 State-Space matrices for SVPWM sectors

As mentioned in Section 2.1, The A matrices for the state-space models are identical. The B matrix for switching states (000) and (111) is provided as follows:

$$\overline{B}_{000/111} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.1}$$

The B matrix for switching state (100) can be expressed as follows:

$$\overline{B}_{100} = \begin{bmatrix} \frac{2}{3L_1} & 0 & 0 \\ \frac{-1}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.2}$$

The B matrix for switching state (110) can be expressed as follows:

$$\overline{B}_{110} = \begin{bmatrix} \frac{1}{3L_1} & 0 & 0 \\ \frac{1}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.3}$$

The B matrix for switching state (010) can be expressed as follows:

$$\overline{B}_{010} = \begin{bmatrix} \frac{-1}{3L_1} & 0 & 0 \\ \frac{2}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.4}$$

The B matrix for switching state (011) can be expressed as follows:

$$\overline{B}_{011} = \begin{bmatrix} \frac{-2}{3L_1} & 0 & 0 \\ \frac{1}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.5}$$

The B matrix for switching state (001) can be expressed as follows:

$$\overline{B}_{001} = \begin{bmatrix} \frac{-1}{3L_1} & 0 & 0 \\ \frac{-1}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.6}$$

The B matrix for switching state (101) can be expressed as follows:

$$\overline{B}_{101} = \begin{bmatrix} \frac{1}{3L_1} & 0 & 0 \\ \frac{-2}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.7}$$

The B matrix of the averaged state-space model for Sector I, where the VSI alternates between switching states (000/111), (100), and (110) can be expressed as follows:

$$\overline{B}_I = \begin{bmatrix} \frac{2d_1+d_2}{3L_1} & 0 & 0 \\ \frac{-d_1+d_2}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.8}$$

The B matrix of the averaged state-space model for Sector II, where the VSI alternates between switching states (000/111), (110), and (010) can be expressed as follows:

$$\overline{B}_{II} = \begin{bmatrix} \frac{d_1-d_2}{3L_1} & 0 & 0 \\ \frac{d_1+2d_2}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.9}$$

The B matrix of the averaged state-space model for Sector III, where the VSI alternates between switching states (000/111), (010), and (011) can be expressed as follows:

$$\overline{B}_{III} = \begin{bmatrix} \frac{-d_1-2d_2}{3L_1} & 0 & 0 \\ \frac{2d_1+d_2}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.10}$$

The B matrix of the averaged state-space model for Sector IV, where the VSI alternates between switching states (000/111), (011), and (001) can be expressed as follows:

$$\overline{B}_{IV} = \begin{bmatrix} \frac{-2d_1-d_2}{3L_1} & 0 & 0 \\ \frac{d_1-d_2}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.11}$$

The B matrix of the averaged state-space model for Sector V, where the VSI alternates between switching states (000/111), (001), and (101) can be expressed as follows:

$$\overline{B}_{V} = \begin{bmatrix} \frac{-d_1+d_2}{3L_1} & 0 & 0 \\ \frac{-d_1-2d_2}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.12}$$

The B matrix of the averaged state-space model for Sector VI, where the VSI alternates between switching states (000/111), (101), and (100) can be expressed as follows:

$$\overline{B}_{VI} = \begin{bmatrix} \frac{d_1+2d_2}{3L_1} & 0 & 0 \\ \frac{-2d_1-d_2}{3L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-2}{3L_2} & \frac{-1}{3L_2} \\ 0 & \frac{1}{3L_2} & \frac{-1}{3L_2} \end{bmatrix} \tag{A.13}$$

A.2 Full-Form of Block Matrices

The full-form of the block matrices introduced in matrix A of (2.4) are provided below:

$$A_{11} = \begin{bmatrix} \frac{-3R_1-R_f}{3L_1} & -\omega \\ \omega & \frac{-3R_1-R_f}{3L_1} \end{bmatrix}, A_{12} = \begin{bmatrix} \frac{-1}{2L_1} & \frac{\sqrt{3}}{6L_1} \\ \frac{-\sqrt{3}}{6L_1} & \frac{-1}{2L_1} \end{bmatrix}, A_{13} = \begin{bmatrix} \frac{R_f}{3L_1} & 0 \\ 0 & \frac{R_f}{3L_1} \end{bmatrix},$$
$$A_{21} = \begin{bmatrix} \frac{1}{2C_f} & \frac{\sqrt{3}}{6C_f} \\ \frac{-\sqrt{3}}{6C_f} & \frac{1}{2C_f} \end{bmatrix}, A_{22} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}, A_{23} = \begin{bmatrix} \frac{-1}{2C_f} & \frac{-\sqrt{3}}{6C_f} \\ \frac{\sqrt{3}}{6C_f} & \frac{-1}{2C_f} \end{bmatrix}, \tag{A.14}$$
$$A_{31} = \begin{bmatrix} \frac{R_f}{3L_2} & 0 \\ 0 & \frac{R_f}{3L_2} \end{bmatrix}, A_{32} = \begin{bmatrix} \frac{1}{2L_2} & \frac{-\sqrt{3}}{6L_2} \\ \frac{\sqrt{3}}{6L_2} & \frac{1}{2L_2} \end{bmatrix}, A_{33} = \begin{bmatrix} \frac{-3R_2-R_f}{3L_2} & -\omega \\ \omega & \frac{-3R_2-R_f}{3L_2} \end{bmatrix}.$$

The full-form of the block matrices introduced in matrix B of (2.4) are provided below:

$$B_{12} = \begin{bmatrix} \frac{V_{dc}cos(\psi)}{\sqrt{3}L_1} & \frac{-MV_{dc}sin(\psi)}{\sqrt{3}L_1} \\ \frac{-V_{dc}sin(\psi)}{\sqrt{3}L_1} & \frac{-MV_{dc}cos(\psi)}{\sqrt{3}L_1} \end{bmatrix}, B_{32} = \begin{bmatrix} \frac{-1}{2L_2} & \frac{\sqrt{3}}{6L_2} \\ \frac{-\sqrt{3}}{6L_2} & \frac{-1}{2L_2} \end{bmatrix},$$
$$b_1 = \begin{bmatrix} -I_d^{inv} \\ I_q^{inv} \end{bmatrix}, b_2 = \begin{bmatrix} -V_d^c \\ V_q^c \end{bmatrix}, b_3 = \begin{bmatrix} -I_d^g \\ I_q^g \end{bmatrix}, \tag{A.15}$$

The block matrices introduced in matrix A of (2.16) can be expressed as follows:

$$A_{43} = \begin{bmatrix} \frac{-k_{i1}V_q^{pcc}}{2} & 0 \\ 0 & \frac{-k_{i3}V_q^{pcc}}{2} \end{bmatrix}, A_{53} = \begin{bmatrix} -k_{i2} - \frac{k_{p1}k_{i2}V_q^{pcc}}{2} & 0 \\ 0 & -k_{i4} - \frac{k_{p3}k_{i4}V_q^{pcc}}{2} \end{bmatrix}, A_{54} = \begin{bmatrix} k_{i2} & 0 \\ 0 & k_{i4} \end{bmatrix}. \tag{A.16}$$

The block matrices introduced in matrix B of (2.16) can be expressed as follows:

$$B_{41} = \begin{bmatrix} \frac{-k_{i1}I_{qL}}{2} & \frac{-k_{i1}I_{dL}}{2} \\ \frac{-k_{i3}I_{dL}}{2} & \frac{k_{i3}I_{qL}}{2} \end{bmatrix}, B_{43} = \begin{bmatrix} k_{i1} & 0 \\ 0 & k_{i3} \end{bmatrix},$$
$$B_{51} = \begin{bmatrix} \frac{-k_{p1}k_{i1}I_{qL}}{2} & \frac{-k_{p1}k_{i1}I_{dL}}{2} \\ \frac{-k_{p3}k_{i3}I_{dL}}{2} & \frac{k_{p3}k_{i3}I_{qL}}{2} \end{bmatrix}, B_{53} = \begin{bmatrix} k_{p1}k_{i2} & 0 \\ 0 & k_{p3}k_{i4} \end{bmatrix}. \tag{A.17}$$

The block matrices introduced in (2.23) can be expressed as follows:

$$A_{63} = \frac{1}{T_d}\begin{bmatrix} -k_{p2} - \frac{k_{p1}k_{p2}V_q^{pcc}}{2} & \omega L \\ -\omega L & -k_{p4} - \frac{k_{p3}k_{p4}V_q^{pcc}}{2} \end{bmatrix}, A_{64} = \frac{1}{T_d}\begin{bmatrix} k_{p2} & 0 \\ 0 & k_{p4} \end{bmatrix}, A_{65} = \frac{1}{T_d}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix},$$
$$B_{61} = \frac{1}{T_d}\begin{bmatrix} 1 - \frac{k_{p1}k_{p2}I_{qL}}{2} & -\frac{k_{p1}k_{p2}I_{dL}}{2} \\ -\frac{k_{p3}k_{p4}I_{dL}}{2} & 1 + \frac{k_{p3}k_{p4}I_{qL}}{2} \end{bmatrix}, A_{66} = -\frac{1}{T_d}\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, B_{63} = \frac{1}{T_d}\begin{bmatrix} k_{p1}k_{p2} & 0 \\ 0 & k_{p3}k_{p4} \end{bmatrix}. \tag{A.18}$$

The modified block matrices of (2.24) can be expressed as follows:

$$A_{13}^L = A_{13}T, A_{23}^L = A_{23}T, A_{31}^L = T^{-1}A_{31}, A_{32}^L = T^{-1}A_{32},$$
$$A_{33}^L = T^{-1}A_{33}T, B_{31}^n = T^{-1}B_{31}, b_3^L = T^{-1}b_3, \tag{A.19}$$

where, $T = \begin{bmatrix} \frac{1}{2} & -\frac{1}{2\sqrt{3}} \\ \frac{1}{2\sqrt{3}} & \frac{1}{2} \end{bmatrix}$. The full form of the matrix M introduced in (2.29) is

$$M = \begin{bmatrix} V_{dc}cos(\psi) & -MV_{dc}sin(\psi) \\ -V_{dc}sin(\psi) & -MV_{dc}cos(\psi) \end{bmatrix}. \tag{A.20}$$

The full form of the block matrices introduced in (2.32) are

$$G_1 = \begin{bmatrix} R_g & \omega L_g \\ -\omega L_g & R_g \end{bmatrix}, G_2 = L_g. \tag{A.21}$$

The modified block matrices of matrix A in (2.35) can be expressed as follows:

$$\begin{cases} A_{3n}^c = A_{3n}^L + B_{3n}^L (I - G_2 B_{31}^L)^{-1} G_2 A_{3n}^L, n \in 1, 2, \\ A_{33}^c = A_{33}^L + B_{31}^L (I - G_2 B_{31}^L)^{-1} (G_1 + G_2 A_{33}^L), \\ A_{n1}^c = B_{n1} (I - G_2 B_{31}^L)^{-1} G_2 A_{31}^L, n \in 4.5.6, \\ A_{n2}^c = B_{n1} (I - G_2 B_{31}^L)^{-1} G_2 A_{32}^L, n \in 4.5.6, \\ A_{n3}^c = A_{n3} + B_{n1} (I - G_2 B_{31}^L)^{-1} (G_1 + G_2 A_{33}^L), n \in 4, 5, 6. \end{cases} \tag{A.22}$$

The modified block matrices of matrix B in (2.35) can be expressed as follows:

$$\begin{cases} B_{31}^c = B_{31}^L (I - G_2 B_{31}^L)^{-1}, \\ B_{n1}^c = B_{n1} (I - G_2 B_{31}^L)^{-1} G_2 A_{31}^L, n \in 4.5.6 \\ b_3^c = b_3^L + B_{31}^L (I - G_2 B_{31}^L)^{-1} G_2 b_3^L, \\ b_n^c = B_{n1} (I - G_2 B_{31}^L)^{-1}, n \in 4, 5, 6. \end{cases} \tag{A.23}$$

The modified block matrices of (4.34) are provided below:

$$\begin{aligned} A_{53}^{vir} &= \begin{bmatrix} -k_{i2}(\frac{1}{2} k_{p1} V_q^{pcc} + 1) & -k_{i2} \frac{\omega L_{vir}}{R_{vir}} \\ k_{i4} \frac{\omega L_{vir}}{R_{vir}} & -k_{i4}(\frac{1}{2} k_{p3} V_q^{pcc} + 1) \end{bmatrix}, \\ A_{63}^{vir} &= \frac{1}{T_d} \begin{bmatrix} -k_{p2} - \frac{k_{p1} k_{p2} V_q^{pcc}}{2} & -k_{p2} \frac{\omega L_{vir}}{R_{vir}} + \omega L \\ k_{p4} \frac{\omega L_{vir}}{R_{vir}} - \omega L & -k_{p4} - \frac{k_{p3} k_{p4} V_q^{pcc}}{2} \end{bmatrix}. \end{aligned} \tag{A.24}$$

Appendix B

Reduced-Order Model

In this appendix, a second-order model is derived for a grid-tied VSI using the balanced truncation method. The use of a detailed full-order model for a DG unit may become cumbersome when modeling a distribution system or a microgrid with many DG units. One approach could be to represent each DG unit with a reduced-order model. An accurate reduced-order model would preserve the dominant behavior of the system while reducing computational complexity. The advantages of reduced-order models have been utilized in this dissertation when selecting a reference model required for updating the virtual inductance term through the direct MRAC method.

The contents of this appendix are presented in five sections. In Section B.1, the reasons behind using the balanced truncation method for model order reduction are outlined. In Section B.2, the principle of balanced truncation method is discussed. In B.3, a reduced-order model for a grid-tied VSI using the balanced truncation method is derived. The model is validated through time-domain simulations and eigenvalue analysis in B.4. Finally, concluding remarks for this appendix are presented in B.5.

B.1 Model Order Reduction Techniques

Model-order reduction techniques can be broadly divided into two categories. The first one is balanced realization (BR) methods such as balanced truncation technique and singular value perturbation (SVP) technique. The other category includes moment matching methods such as Krylov subspace technique.

In model-order reduction through the SVP technique, the states with faster modes, i.e. smaller damping constants, are eliminated while some of their information is retained through their projection onto the remaining slower states of the model [89–92]. In [89], the SVP technique is used to reduce the order a seventh order model of a droop-controlled islanded microgrid. The model can be reduced up to fifth order under some operating scenarios as any further order reduction can result in erroneous stability results. In [90], a fifteenth order model of an inverter is reduced to an eighth order model using SVP. In both cases, the need to preserve the slower modes using the SVP method restricted any further reduction in model order. In [91], a second order model using SVP was derived, but it is valid only for inverters in islanded microgrids. A second order model for a VSI using SVP is also derived in [92]; however, this model is developed from a simplified full-order model excluding the LCL filter dynamics.

In the Krylov subspace method, the reduced order model is developed by matching the leading coefficients of the power series expansion of the reduced order, to that of the full-order through iterative procedures [93–95]. In [93] and [94], the Krylov subspace method is used to reduce the order of traditional power systems excluding DG units. In [95], a reduced order model of an active distribution system with power electric converters is derived using the Krylov subspace method. The entire system is divided into two regions with the active power electronic components isolated in one region and the remaining passive components isolated in another region. Only the region with the passive components is reduced and as a result, such a procedure will not be applicable for an area with high penetration of DG units, since the system order will remain high even following the order reduction. Similar to the SVP method only the slower modes of the original system are

retained in the Krylov subspace method. For traditional power systems, such slower modes represent the dominant modes and as such are able to represent the stability of the system. However, this statement is not always true for systems with power electronic circuits as can be seen from the root locus analysis carried out in Sections 3.1 and 4.4 for grid-tied VSIs. As one can see from the root locus of the eigenvalues in the aforementioned sections, some of the slower eigenvalues, i.e. the real eigenvalues close to the origin, are non-responsive to system parameter VARiations. Therefore, these eigenvalues are the not the dominant ones as they do not affect system stability. However, model-order reductions performed using SVP and Krylov subspace methods will retain these states, which will restrict a worthwhile reduction in the model order.

In the balanced truncation method, the dominant eigenvalues of the system can be identified through their respective Hankel singular values. An accurate model with a significantly reduced number of orders can thus be obtained by retaining the system states with large Hankel singular values while eliminating the ones with smaller Hankel singular values [96–101]. The balanced truncation method is employed in this appendix to derive a reduced-order model for a grid-tied VSI.

B.2 Balanced Truncation Method

In this section, the principle of model order reduction using balanced truncation method is described. The method outlined in this section is used to derive a reduced-order model of a grid-tied VSI in the following section.

The full-order model of grid-tied VSI presented in (4.34) can be expressed using a more general state-space form as follows:

$$\dot{x} = Ax + Bu, y = Cx + Du, \tag{B.1}$$

where, $A \in \Re^{nxn}, B \in \Re^{nxm}, C \in \Re^{pxn}, andD \in \Re^{pxm}$. The goal is to derive a reduced-order model with $\tilde{A} \in \Re^{kxk}, \tilde{B} \in \Re^{kxm}, \tilde{C} \in \Re^{pxk}$, and $\tilde{D} \in \Re^{pxm}$ such that $k \ll n$. The other

requirement of the reduced-order model are that the mismatch between the full-order and the reduced-order model be negligible, the properties of the full-order model be preserved, and the method to obtain the reduced-order model be computationally stable and efficient [102]. The balanced truncation method is an attractive approach to obtain the reduced-order model since it preserves the stability of the system while providing a global computational error bound between the full-order and the reduced-order model [102, 103].

The first step in reducing the system order using balanced truncation method is to transform the system to a balanced form. A balanced form for linear systems is achieved when its controllability Gramian $\mathcal{P}$ and observability Gramian $\mathcal{Q}$ are equal and diagonal. The Gramians of the system can be calculated as follows:

$$\mathcal{P} = \int_0^\infty e^{At} B B^T e^{A^T t} dt, \tag{B.2}$$

$$\mathcal{Q} = \int_0^\infty e^{A^T t} C^T C e^{At} dt. \tag{B.3}$$

The Gramians can be made equal and diagonal through a basis change by applying the transformation matrix T, which should be of the same order as the system to be reduced, i.e. $T \in \Re^{nxn}$, and also should not be a singular matrix. Hence, T is chosen such that,

$$\tilde{\mathcal{P}} = T\mathcal{P}T^T = \tilde{\mathcal{Q}} = T^{T^{-1}}\mathcal{P}T^{-1} = \Sigma. \tag{B.4}$$

where, $\tilde{\mathcal{P}}$ and $\tilde{\mathcal{Q}}$ are the Gramians of the balanced system. Following the basis change the new balanced state-space form is found to be,

$$\dot{\tilde{x}} = TAT^{-1} + TBu, y = CT^{-1}\tilde{x} + Du. \tag{B.5}$$

The Gramians of the balanced state-space form is equated to Σ in (B.4), which is a diagonal matrix and its diagonal elements are the Hankel singular values. The Hankel singular values give an indication of which states of a system dominate its input/output behavior [102]. In other words, the larger the Hankel singular value associated with a state,

the more dominant its eigenvalue will be, and in turn the larger its impact will be on the dynamics of the system. As a result, a reduced-order model for the system in (B.5) can be derived by identifying its states with the smaller Hankel singular values and truncating them. To that end, the diagonal matrix Σ can be partitioned into two parts with respect to Hankel singular values such that,

$$\Sigma = \begin{bmatrix} \Sigma_1 & 0 \\ 0 & \Sigma_2 \end{bmatrix}, \tag{B.6}$$

where, Σ_1 and Σ_2 are diagonal matrices containing the larger and smaller Hankel singular values, respectively. Partitioning the system according to (B.6), (B.5) can be written as,

$$\begin{bmatrix} \dot{\tilde{x}}_r \\ \dot{\tilde{x}}_t \end{bmatrix} = \begin{bmatrix} \tilde{A}_{rr} & \tilde{A}_{rt} \\ \tilde{A}_{tr} & \tilde{A}_{tt} \end{bmatrix} \begin{bmatrix} \tilde{x}_r \\ \tilde{x}_t \end{bmatrix} + \begin{bmatrix} \tilde{B}_r \\ \tilde{B}_t \end{bmatrix} u$$
$$y = \begin{bmatrix} \tilde{C}_r & \tilde{C}_t \end{bmatrix} \begin{bmatrix} \tilde{x}_r \\ \tilde{x}_t \end{bmatrix} + \tilde{D}u \tag{B.7}$$

where, $\tilde{x}_r \in \Re^{kx1}$ are the dominant states and $\tilde{x}_t$ are the states to be truncated. By eliminating the states with the lower Hankel singular values, the reduced-order model for the system in (2) using the balanced truncation technique can be expressed as follows:

$$\dot{\tilde{x}}_r = \tilde{A}_{rr}\tilde{x}_r + \tilde{B}_r u, y = \tilde{C}_r\tilde{x}_r + \tilde{D}u \tag{B.8}$$

The technique outlined in this section is used to derive a reduced-order model for a grid-tied VSI in the following section.

Table B.1: *Parameter values for Section B.3*

Parameter	Value	Parameter	Value
L_1	$1.5mH$	k_{p1}, k_{p3}	0.02
L_2	$1.0mH$	k_{p2}, k_{p4}	0.5
C_f	$33\mu H(\Delta)$	k_{i1}, k_{i3}	8
R_f	0.1Ω	k_{i2}, k_{i4}	10
L_g	$0.5mH$	T_d	$300\mu s$

B.3 Reduced-Order Model

In this section, the balanced truncation method is applied to derive a second-order model for a grid-tied VSI. The parameter values for this section are provided in Table B.1. The definitions for the parameters listed in Table B.1 can be found in Fig. 2.6.

As mentioned in the previous section, the Hankel singular values are a reliable indicator of the information each state of a system holds regarding the system dynamics. The normalized Hankel singular values of the full-order model described in (4.34) are plotted in Fig. B.1. As one can see from Fig. B.1, two of the states have the largest Hankel singular values associated with them, while the Hankel singular values of the remaining ten states can be seen to be negligible. Hence, it can be concluded that two states of the grid-tied VSI have the largest impact on the system dynamics and as a result, a second-order model can represent the behavior of grid-tied VSIs.

The A and B matrices of the full-order state-space model is defined in (4.34). To deter-

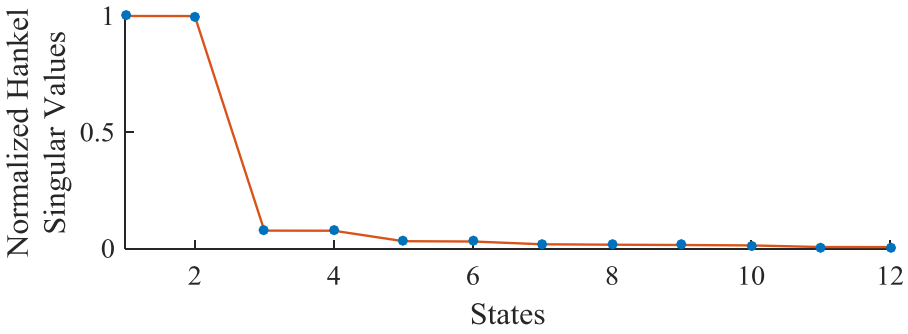

Figure B.1: *Normalized Hankel singular values of the full-order model presented in* (4.34).

mine the reduced-order model of the grid-tied VSI using the balanced truncation method described in the previous section, the C and D matrices of the full-order state-space model should also be defined. As the VSI is operating in the grid-tied mode equipped with a PQ controller, the output of the model should be P and Q, i.e.$y = \begin{bmatrix} P & Q \end{bmatrix}^T$. The expressions for P and Q in the dq frame of reference is provided in (2.10) and (2.11), respectively. Linearizing the expressions for P and Q, the output equations for the full-order model can be expressed as follows:

$$P = \frac{1}{2}V_q^{pcc} i_{qL} + \frac{1}{2}I_{qL} v_q^{pcc} + \frac{1}{2}I_{dL} v_d^{pcc}, \tag{B.9}$$

$$Q = \frac{1}{2}V_q^{pcc} i_{dL} + \frac{1}{2}I_{dL} v_q^{pcc} - \frac{1}{2}I_{qL} v_d^{pcc}. \tag{B.10}$$

Replacing the relationship between v^{pcc} and v^g provided in (2.33) in (B.9) and (B.10), the final output equations of the full-order model can be expressed as follows:

$$\begin{aligned} y = (D_D(I - G_2 B_{31}^L)^{-1} G_2 A_{31}^L) i_{qd}^{inv} + (D_D(I - G_2 B_{31}^L)^{-1} G_2 A_{32}^L) v_{qd}^c \\ + (C_C + D_D(I - G_2 B_{31}^L)^{-1}(G_1 + G_2 A_{33}^L)) i_{qdL}. \end{aligned} \tag{B.11}$$

The block matrices C_C and D_D introduced in (B.11) can be defined as follows:

$$C_C = \frac{1}{2}\begin{bmatrix} V_q^{pcc} & 0 \\ 0 & V_d^{pcc} \end{bmatrix}, D_D = \frac{1}{2}\begin{bmatrix} I_{qL} & I_{dL} \\ I_{dL} & -I_{qL} \end{bmatrix} \tag{B.12}$$

A second-order model of a grid-tied VSI with the operating point specified in Table I can then be found as follows:

$$\tilde{A}_{rr} = \begin{bmatrix} -29.77 & -4659.0 \\ 4667.52 & -36.81 \end{bmatrix}, \tilde{B}_r = \begin{bmatrix} -33.12 & -200.95 & -2.0 & -0.39 & -0.79 \\ -189.13 & 44.83 & -18.47 & -0.83 & 0.42 \end{bmatrix},$$
$$\tilde{C}_r = \begin{bmatrix} 54.20 & 198.76 \\ 201.68 & 15.57 \end{bmatrix}, \tilde{D} = \begin{bmatrix} 5.67 & 0 & 0 & 0 & 0 \\ 0 & -5.67 & 0 & 0 & 0 \end{bmatrix}, \tag{B.13}$$

where, $\tilde{A}_{rr}$, $\tilde{B}_r$, $\tilde{C}_r$, and $\tilde{D}$ are defined in (B.8). The derived reduced-order model is verified in the following section through time-domain simulations. This method of developing reduced-order models for grid-tied VSIs is also verified for different operating points through simulation studies and eigenvalue analysis in the following section.

B.4 Model Verification

In this section, the reduced-order technique presented for grid-tied VSIs in the previous section is verified through time-domain simulation and eigenvalue analysis.

Table B.2: *Parameter values for Section B.4*

Parameter	Case I	Case II	Case III
L_1	$1.5mH$	$1.5mH$	$1.5mH$
L_2	$1.0mH$	$1.5mH$	$1.5mH$
C_f	$15\mu H$	$10\mu H$	$10\mu H$
R_f	0.05Ω	0.05Ω	0.05Ω
L_g	$0.5mH$	$0.5mH$	$0.5mH$
k_{p1}, k_{p3}	0.02	0.02	0.02
k_{p2}, k_{p4}	0.5	0.5	0.5
k_{i1}, k_{i3}	5	5	10
k_{i2}, k_{i4}	5	5	10
T_d	$300\mu s$	$300\mu s$	$300\mu s$

B.4.1 Time-Domain Verification

The usefulness of the developed reduced-order model is dependent upon its effective operation for a wide range of input values and different operating points defined by different circuit and controller parameters. Therefore, to prove the validity of the model order reduction procedure outlined in Sections B.2 and B.3, reduced-order models are generated under three separate group of system parameters as shown in Table B.2 and compared against circuit simulation and its full-order model counterpart. Note that the first set of operation points presented in Table B.2 is the same as the one presented in Table B.1. Therefore, the reduced-order model derived in the previous section can be directly used for this case. For all the scenarios presented in this section, a dc-bus voltage of $380V$ and a grid rms voltage of $208V$ are used. The PWM frequency is set at $5kHz$. The simulations are carried out in MATLAB/Simulink using the SimPowerSystems toolbox.

The outputs of the reduced-order model for the first case study are compared against their full-order and circuit simulation counterparts in Fig. B.2. The inputs to the models are changed in two steps. Firstly, the desired active power P^* is decreased from $5kW$ to $3kW$ at instant $0.03s$, following which the desired reactive power Q^* is increased from $0VAR$ to $200VAR$ at instant $0.07s$. It can be seen from Fig. B.2 that the reduced-order model presented in the previous section is an accurate representation of the circuit simulation and full-order model.

For the second case study depicted in Fig. B.3, different circuit parameters for the grid-connected VSI are considered as provided in Case II of Table B.2. In the scenario depicted in Fig. B.3, the accuracy of the reduced-order model is verified as P^* is increased from $5kW$ to $7kW$ at instant $0.03s$, while the same VARiation in Q^* is considered. As one can see from Fig. B.3, the outputs of the second-order model can impressively track that of both the full-order model and the circuit simulation.

For the third case study, different controller parameters are considered for the system as can be seen from the last column of Table B.2. The results are plotted in Fig. B.4 for an increase in P^* from $5kW$ to $7kW$ at instant$0.03s$, followed by an increase in Q^* from $0VAR$

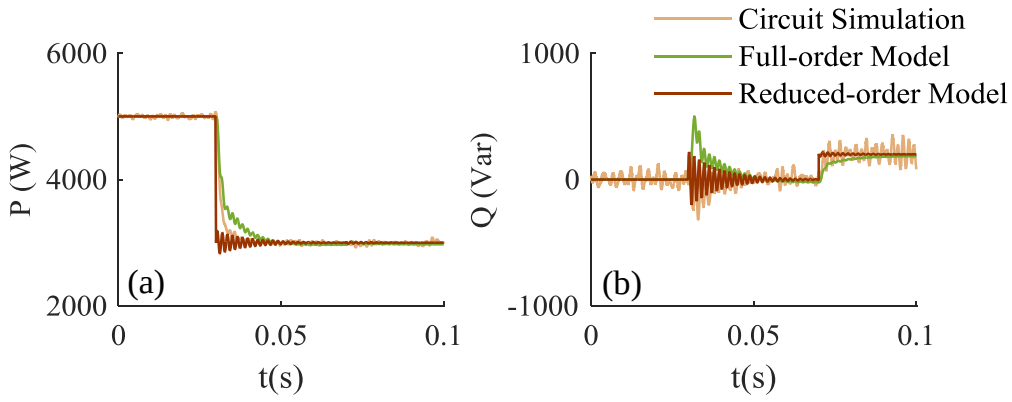

Figure B.2: *Reduced-order outputs obtained using* (B.13)*, plotted against their full-order and circuit simulation counterparts with* P^* *changing from* $5kW$ *to* $3kW$ *at* $0.03s$ *followed by a change in the reactive power from* $0VAR$ *to* $200VAR$ *at* $0.07s$*.*

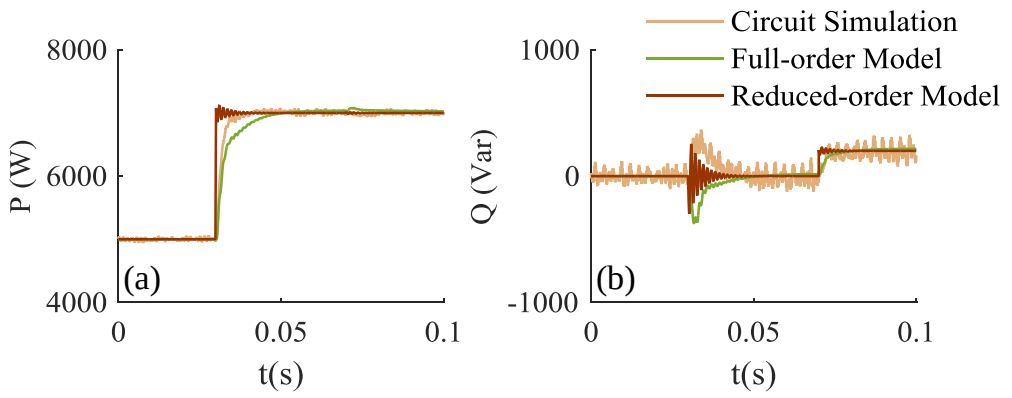

Figure B.3: *Reduced-order outputs under Case II parameters in Table B.2 plotted against their full-order and circuit simulation counterparts with* P^* *changing from* $5kW$ *to* $7kW$ *at* $0.03s$ *followed by a change in* Q^* *from* $0VAR$ *to* $200VAR$ *at* $0.07s$*.*

to $500VAR$ $0.07s$. Similar to the previous case studies, the reduced-order model for this case show good performance as can be seen from Fig. B.4. In all three scenarios, it can be observed that the slow dynamics of the outputs are not exactly represented by the reduced-order models. It could be due to the eigenvalues retained in the reduced-order models being high-frequency ones and as a result, low-frequency eigenvalues of the full-order model are truncated. This topic is analyzed further in the following subsection.

B.4.2 Eigenvalue Analysis

The second evaluation criteria for verifying the accuracy of the developed reduced-order models is the ability to faithfully analyze the stability of the grid-tied system. To that end, the root locus of the system eigenvalues is obtained for the reduced-order models and compared against its full-order counterparts. The analysis in this subsection is performed by observing the eigenvalues of the models as one system parameter is VARied at a time. The initial values of the system parameters used in this section can be found in Table B.1.

In the first scenario depicted in Fig. B.5, the eigenvalues of the full-order and reduced-order models are plotted as the grid inductance L_g is increased from $0.5mH$ to $4mH$. It can be seen from Fig. B.5 that as L_g increases the system goes from the stable to the unstable region, while for the entire range the reduced order eigenvalues provide a good representation of the dominant eigenvalues of the full-order model. This is achieved through the stability preservation property of the balanced truncation method. As expected from the analysis of the Hankel singular values in the previous section, two eigenvalues, which are a complex conjugate pair, dominate the stability of the grid-tied VSI. A zoomed-in version of the root locus of the eigenvalues focusing on one of the dominant eigenvalues is also shown in Fig. B.5 (right), where it can be seen that the reduced-order and the full-order eigenvalue are an exact match near the boundary of the stability region. Notice that the dominant eigenvalues of

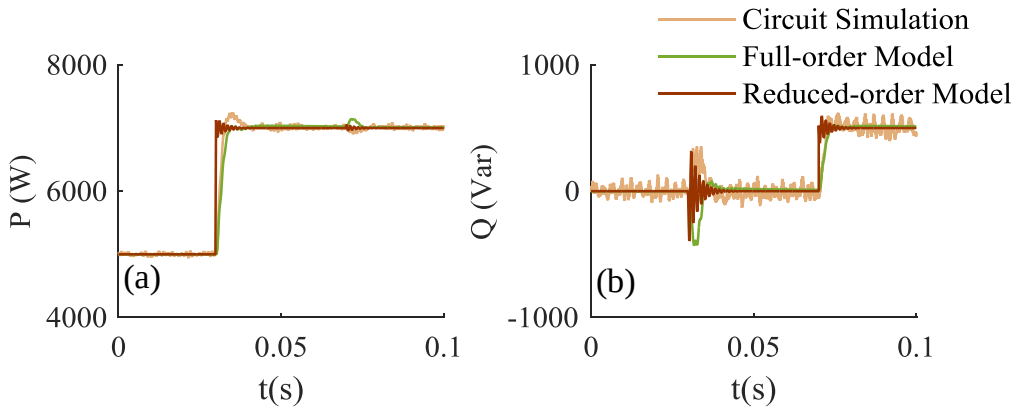

Figure B.4: *Reduced-order outputs under Case III parameters in Table B.2, plotted against their full-order and circuit simulation counterparts with P^* changing from $5kW$ to $7kW$ at $0.03s$ followed by a change in Q^* from $0VAR$ to $500VAR$ at $0.07s$.*

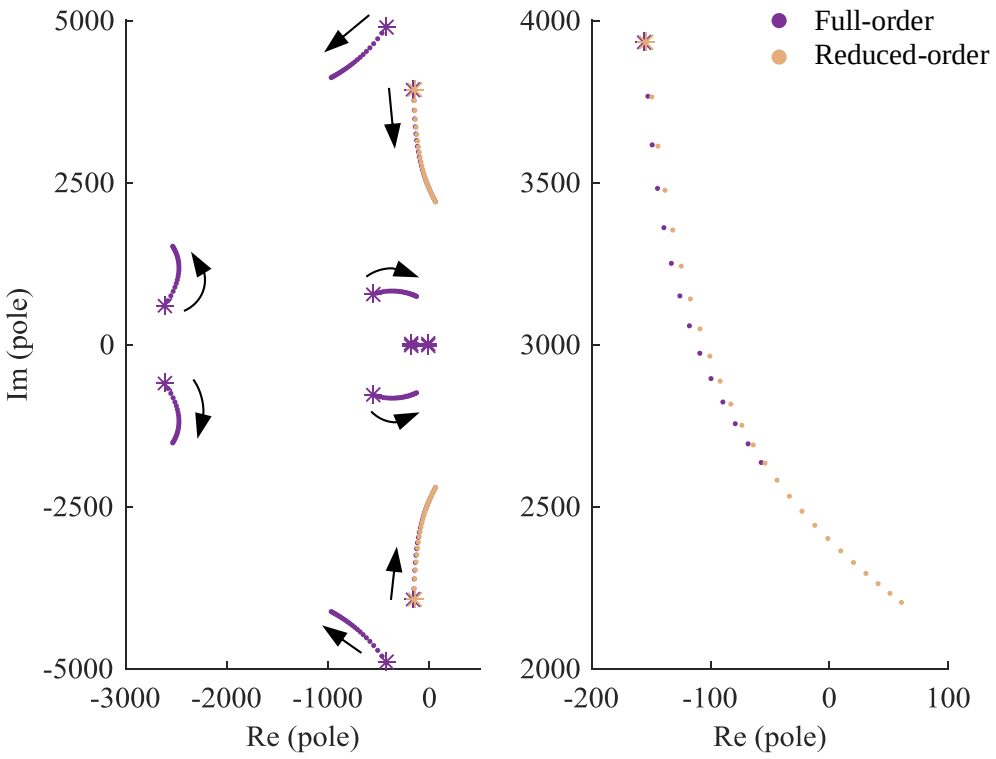

Figure B.5: *The root locus of the full-order and the reduced-order models as L_g is gradually increased from $0.5mH$ to $4mH$ (left) along with a zoomed-in plot of one of the dominant eigenvalues (right).*

the full-order model have a high undamped natural frequency. On the other hand, the non-dominant eigenvalues containing the low-frequency dynamics are eliminated using the balanced truncation method and are not present in the reduced-order model.

The eigenvalues are plotted for the next scenarios, as the controller proportional gains k_{p1} and k_{p2} are VARied in Figs. B.6 and B.6(b), respectively. The root locus of only the dominant eigenvalue of the full-order model is considered for the remaining scenarios presented in this subsection. As one can see from Fig. B.6, the reduced-order technique provides an accurate stability response for changes in both parameters.

The dominant eigenvalues of the models are then plotted in Fig. B.7 for VARiations in filter parameters L_1 and C_f. The presented model order reduction technique is a reliable indicator of system stability as further confirmed from the scenarios in Fig. B.7. For the scenarios presented in this subsection, the magnitude of the eigenvalues of the reduced-order

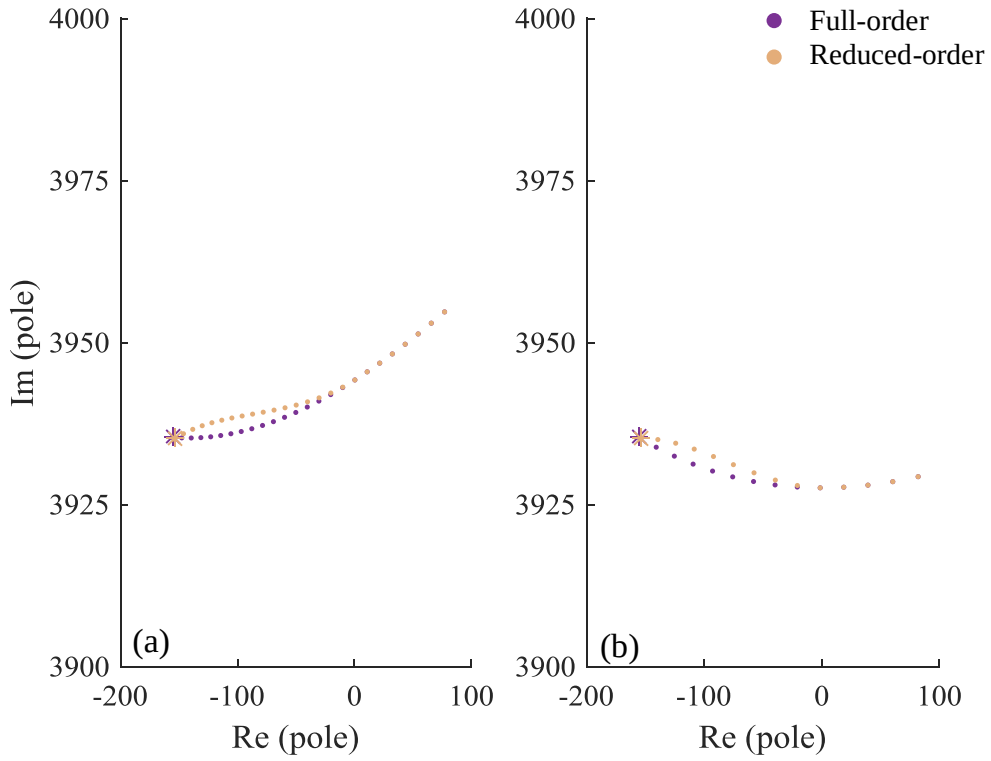

Figure B.6: *The root locus of a dominant eigenvalue of the full-order and the reduced-order models as (a) k_{p1} is increased from* 0.015 *to* 0.5 *and (b) k_{p2} is increased from* 0.5 *to* 2.

model slightly diverges from the dominant full-order eigenvalues as the system starts moving further to the stable region. This is due to the dominant eigenvalues entering the vicinity of the remaining eigenvalues of the system as they move further into the stable region. As a result, the contribution of the remaining eigenvalues on the system response of the full-order model begins to increase. On the other hand, the eigenvalues of both the models exactly superimpose in the unstable region and at the boundary of stability and instability, thus indicating good stability response for the reduced-order technique.

B.5 Conclusion

In this appendix, the balanced truncation method has been employed to develop a second-order model for a grid-tied VSI. The reduced-order model has been developed to accurately represent the twelfth-order state-space model of a grid-tied VSI under VARious operating

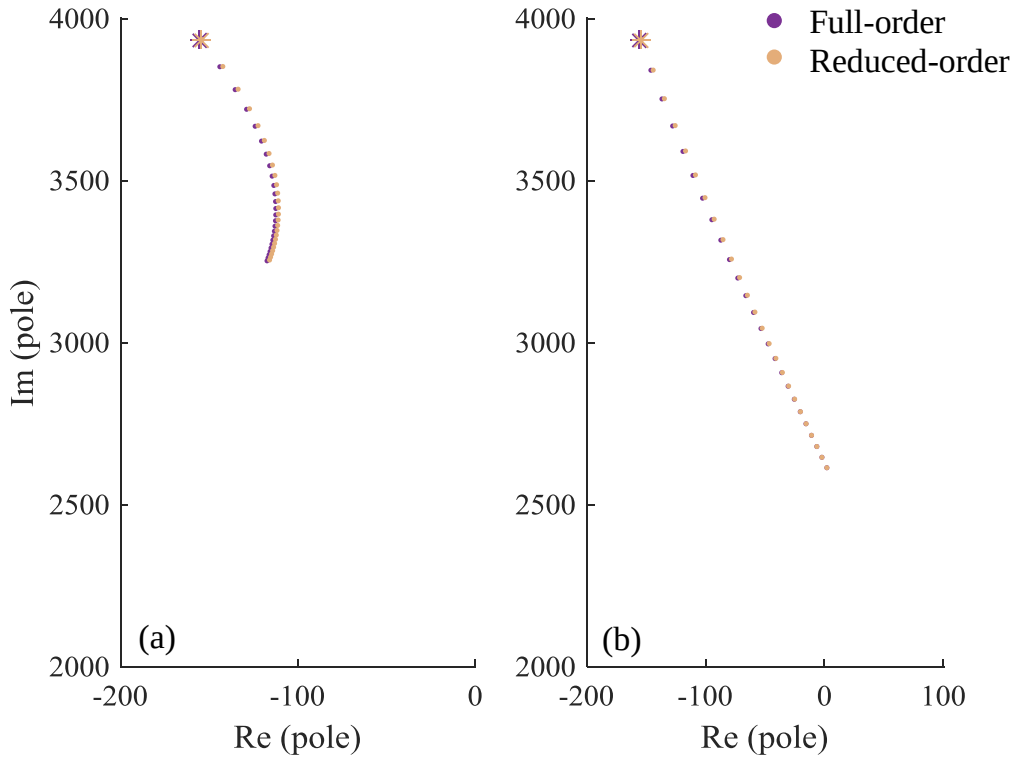

Figure B.7: *The root locus of a dominant eigenvalue of the full-order and the reduced-order models as (a) L_1 is increased from $1.5mH$ to $5mH$ and (b) C_f is increased from $15\mu F$ to $40\mu F$.*

conditions. Observation of the Hankel singular values of the full-order model showed that two dominant states contain most of the system information, which justified the development of a second-order model. Several time-domain simulation scenarios have been carried out to verify the accuracy of the developed model. As the balanced truncation method preserves the stability of the system, a second-order model can act as a reliable indicator of grid-tied VSI stability. The work presented in this appendix can be used as a base for the development of reduced-order model for a distribution grid with high penetration of DG units or a microgrid. In this dissertation, the presented reduced-order technique has been employed to select a second-order reference model for the direct MRAC method, which has been integrated to the presented adaptive virtual inductance feedforward scheme.