THE USE OF FIELD-EFFECT TRANSISTORS AT HF AND VHF AS TUNED AMPLIFIERS AND MIXERS

by

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I. AN INTRODUCTION TO FIELD-EFFECT TRANSISTORS

There are two categories of transistors, namely, bipolar (conventional) transistors and unipolar transistors. Almost everybody in electronics is aware of the bipolar transistors, but as aware of unipolar transistors. Therefore, it is perhaps instructive to discuss some aspects of the unipolar transistors.

The field-effect transistor (abbreviated to FET) is a type of unipolar device. It has a long history, much longer than that of the conventional bipolar transistor. In the early 1930's there were already some treatises (by Sommerfeld, Bethe, Frohlich and Wilson) and patents (by Heil[1]). In 1952, the unipolar FET with junction gate was proposed by Schockley[2]. The development of FETs has been considerably slower than that of bipolar transistors. First, publications on bipolar transistors have overshadowed the field-effect device and absorbed most of the technological effect; second, the range of possible applications is more limited than that of bipolar transistors; lastly, the technological difficulties concerned with quantitative manufacture have been encountered.

Recently there has been considerable effect expended in the development of this device so that there are now a number of commercially available types. This has occured for several

1. O. Heil, Brit. Pat. 439, 457, (Sept. 26, 1939).
2. W. Shockley, Proc. IRE 40, 1365 (1952).

reasons, one reason for this development is a better understanding of semiconductor physics and the related advance of semiconductor technology which now makes it possible to fabricate devices with predictable performance. Another reason is the addition of now technological features such as evaporated construction and insulated gates which promise much improved performance over the reverse-biased-junction gate construction. The third reason is the deficient performance of the bipolar transistors in some applications requiring high impedance or lateral symmetry.

II. THE PRINCIPLE AND CHARACTERISTICS OF FIELD-EFFECT TRANSISTORS

The field-effect transistor is far simpler to visualize than an ordinary transistor. Basically, it is a variable resistor whose value is controlled by an input potential. The operation of FETs may even be visualized in terms of rheostats with control knobs that are turned to vary their resistance. The input resistance may thus be much greater than a vacuum tube. There is in fact a considerable similarity between parameters of the FET and of the pentode vacuum tube, and many familiar old circuits are coming back in a new guise. This has brought some circuit designers and manufacturers an ever-increasing interest in the study of FETs.

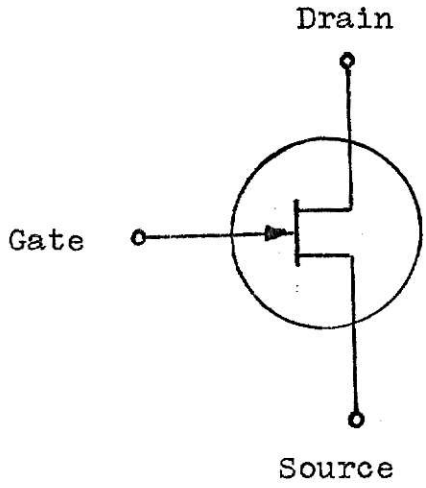
There are two basic forms of FETs, the Junction Field-Effect Transistor (JFET) and the Insulated Gate Field-Effect Transistor (IGFET). Both types achieve much the same result but by different means. They make use of a semiconductor resistor of constant length, which is subjected to a transverse modulation of the material resistivity. This modulation is so pronounced that the resistor may be regarded as varying in physical width. Such a result is made possible by using a fundamental property of a p-n junction in a semiconductor. This property is the increase of charge stored on both sides of the actual junction when the junction is back biased. This charge is stored by forcing mobile charge carriers away from the junction region, thus causing the large numbers of ionised impurity atoms to be no longer neutralised. The mobile carriers are, of cause, the means of conduc-

tion of charge through the semiconductor material; hence, if the resistor is bounded by a p-n junction, the effective boundary moves as the potential across the junction changes.

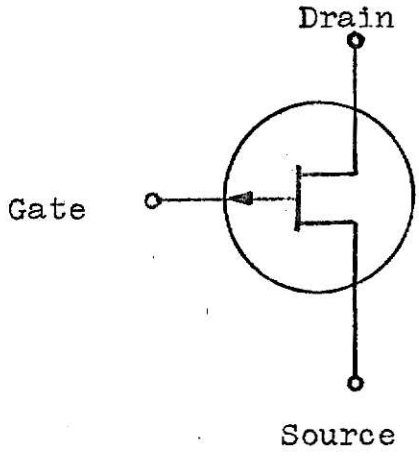
The mechanism of conduction for charge carriers along the resistor is drift under the influence of an electric field, the mechanism that gives rise to Ohm's law. The complicated diffusion mechanisms that are encountered in bipolar transistors do not play a significant part in the operation of field-effect transistors. Only one type of charge carrier need be considered; this will be the electron if the resistor is n-type. (majority carrier). This is why the FET may be described as a unipolar device. The device symbols of both JFET and IGFET for n-channel and p-channel are as shown in Figure 1.

1. Junction Field-effect Transistor

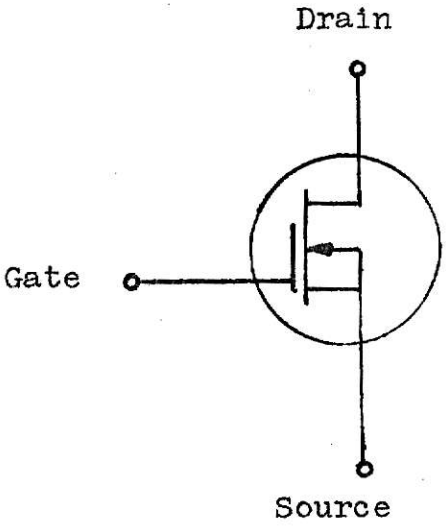
A Junction Field-effect Transistor is basicly constructed as a semiconductor bar with p-n junction for boundaries. Figure 2 shows the p-type silicon block with n-type impurities introduced into opposite sides, forming two p-n junctions on the semiconductor bar. The two n-type regions are electrically connected, and a reverse voltage V_{GS} is applied to the two junctions. Between the drain and source terminals a potential difference V_{DS} is applied. If the impurity concentration in then-type regions is purposely made very high compared to that in the bar, then the depletion layer (the region on either side of the junction from which mobile carriers have disappeared, termed by some space charge layer.) due to the contact potential (the potential that



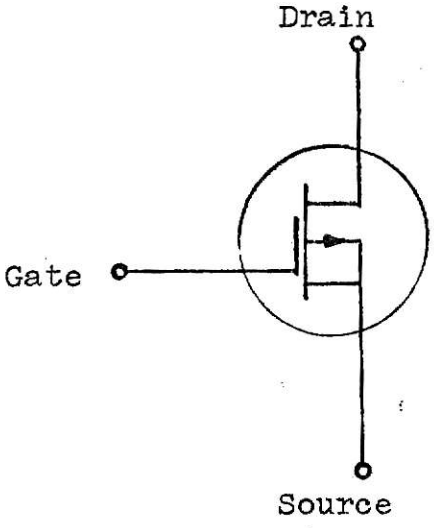
(a) n-channel JFET



(b) p-channel JFET



(c) n-channel IGFET



(d) p-channel IGFET

Figure 1. Device symbols for JFET and IGFET

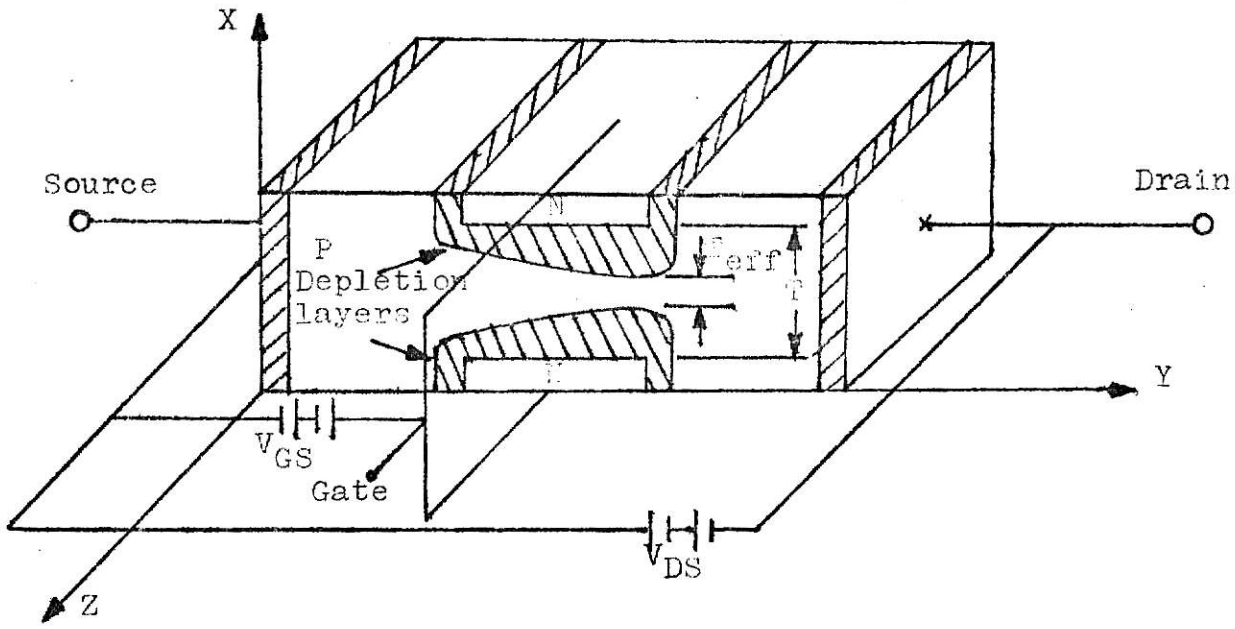


Figure 2. Basic construction of a p-channel JFET.

completely prevents movement of holes and electrons across the junction.) and external bias V_{GS} will extend into the region of the bar between the junctions. Now, since there are virtually no free carriers in the depletion layer (except those generated by heat), the conductance between the source and drain terminal is almost entirely determined by the region between the p-n junctions not depleted of free carriers by the reverse junction voltage. Thus it is easy to see how the applied voltage V_{GS} controls the conductance of our semiconductor bar.

In Figure 2, the shaded regions between junctions are the depletion layers; the parts of the bar between the ends of the channel and ohmic contacts can be considered as lumped bulk resistors. The effective thickness available for conduction at a point y along the channel is as shown in Figure 3, where X_p and X_n are the widths of the depletion regions in the p-type and n-type related to the impurity densities in both p-type and

n-type semiconductors[3]. It is obviously;

$$T_{eff} = T - 2X_p \qquad (1)$$

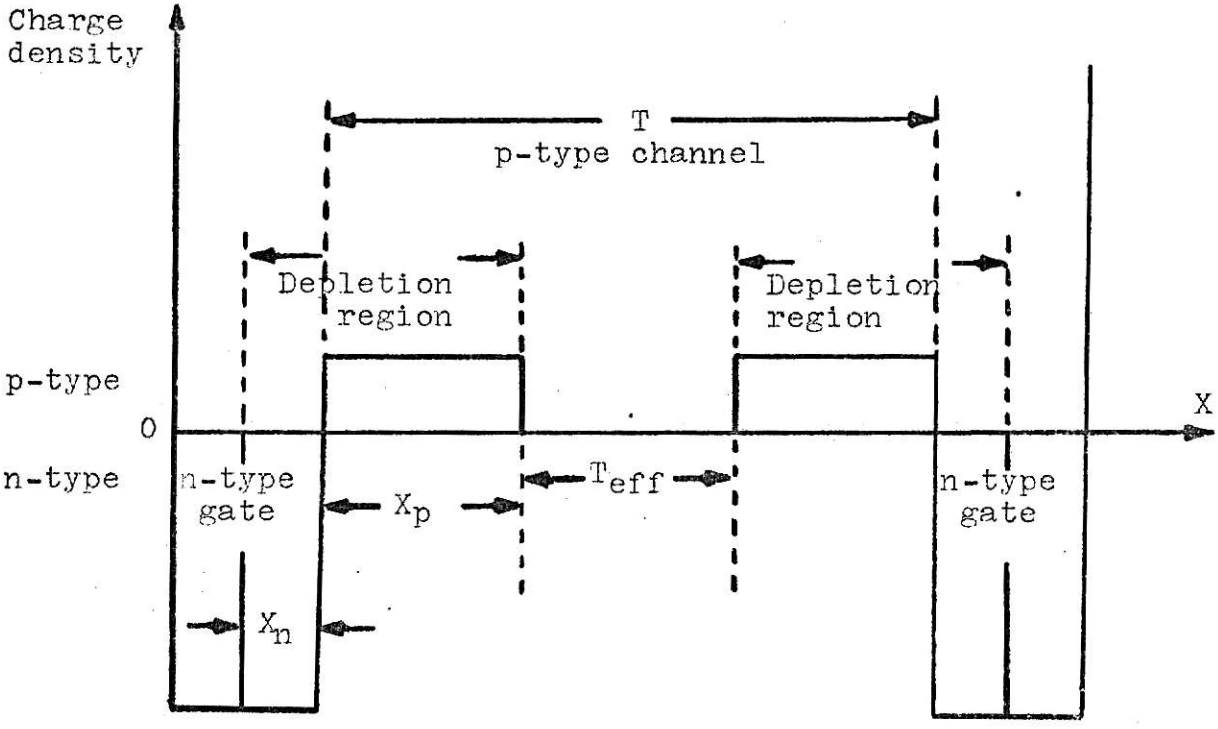


Figure 3. The effective channel thickness in the p-type channel.

The depletion region width will increase as the gate reverse bias is increased. When the reverse bias increases to a certain value V_p, all the free charge will be removed from the channel, i. e. the effective channel thickness will be reduced to zero. The value V_p is called the pinch-off

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3. M. S. Ghausi, "principles and Design of Linear Active Circuit." Sec. 7-3

voltage. Thus we have;

$$T_{eff} = T - 2X_p = 0 \quad \text{or} \quad X_p = T/2 \tag{2}$$

Under this condition, the resistance between source and drain is practically infinite, and the conductance of the channel is zero. Figure 4 shows the relationship between V_{GS} and the conductance G of the channel with zero source-to-drain voltage.

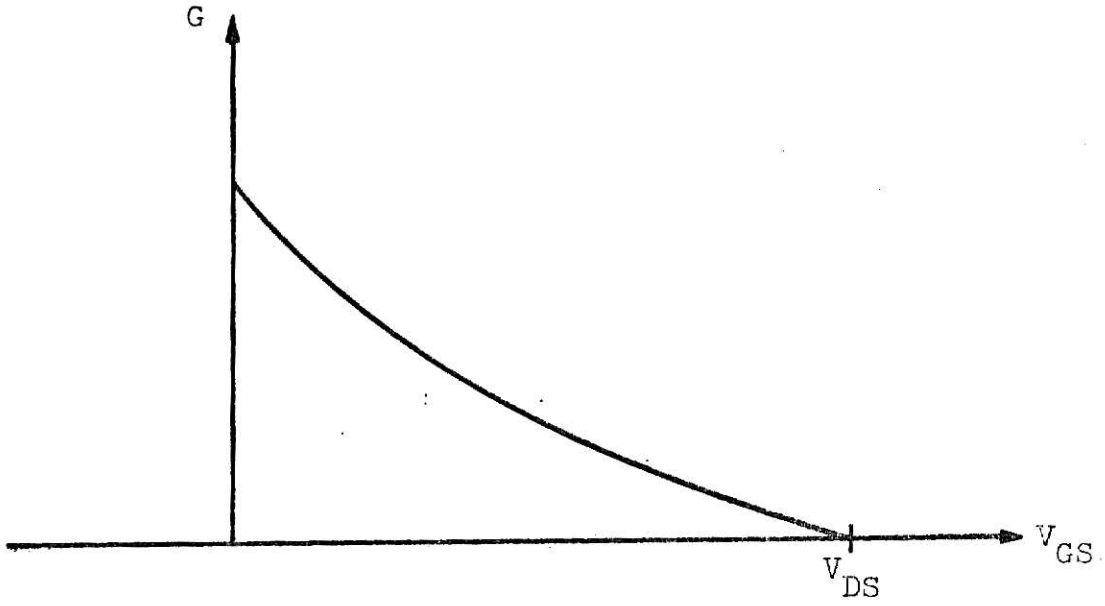

Figure 4. G versus V_{GS} with V_{DS}= 0.

Now if the gate-source voltage is zero and the drain is made negative with respect to the source, a current flow I_d will flow in the channel because of the potential difference between source and drain. As the voltage V_{DS} is increased from zero to small values, the drain current I_d rises linearly with V_{DS}, so that the channel between the drain and the source behaves as a linear resistor. However, as current I_d increases, the drain voltage drop reverse biases the p-n junction near the drain end of the channel, and the depletion regions are extended into the channel, decreasing the effective channel thickness

and lowering the channel conductance. As the drain-source voltage V_{DS} is increased to the pinch-off voltage, the effective channel thickness is reduced to zero at a point near the drain end of the channel. It is interesting to note that the drain current does not stop at pinch-off and beyond[4], since a voltage approximately equal to V_p still exists between the pinch-off point and the source. In this case the channel is pinched-off at the drain end and the drain current is no longer affected by the drain voltage. Thus, the drain current can only be controlled by the gate-source voltage V_{GS}. In the other words, as the drain voltage is increased beyond V_p, the depletion region thickness is increased between the gate and drain, but is practically unchanged between the pinch-off point and source, unless a reverse bias V_{GS} is applied. A complete operation with various values of V_{GS} and V_{DS} is shown in Figure 5. Once the drain-source voltage reaches pinch-off ($V_{DS} = V_p$), the drain current I_d saturates and stays relatively constant until drain to gate avalanche is reached. An expression for the drain current in the uniform channel as a function of gate-source voltage when the JFET is operated in the pinch-off region was originally derived by Shockley[5];

$$I_d = I_{DSS}\left[1 - 3(V_{GS}/V_p) + 2(V_{GS}/V_p)^{3/2}\right], \qquad (3)$$

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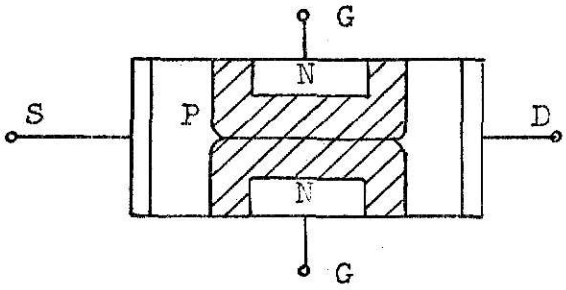
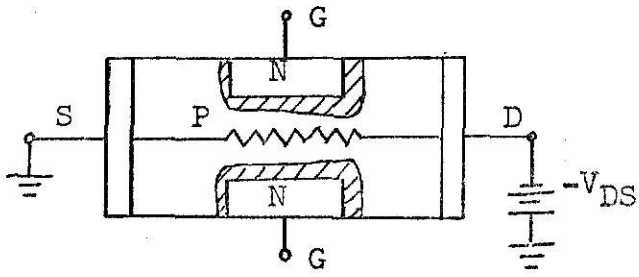
4. Leonce J. Sevin, Jr. "Field-Effect Transistors" page 11-17.
5. Shockley, W. "AUnipolar Field-Effect Transistor", Proc. IRE, Vol. 40, pp. 1365-1376, Nov. 1952.



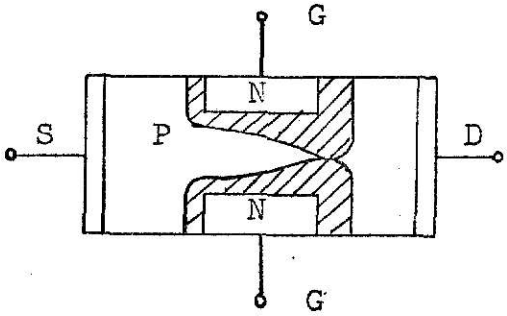
(a) $|V_{GS}| = |V_p|$

$V_{DS} = 0$



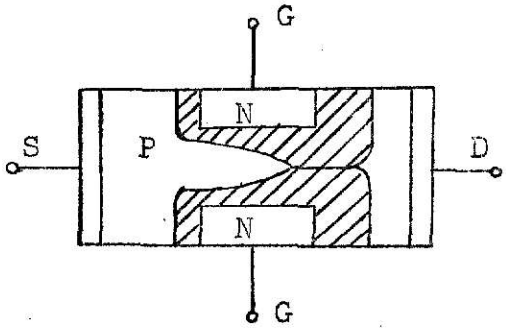
(b) $V_{GS} = 0$

$0 < |V_{DS}| << |V_p|$



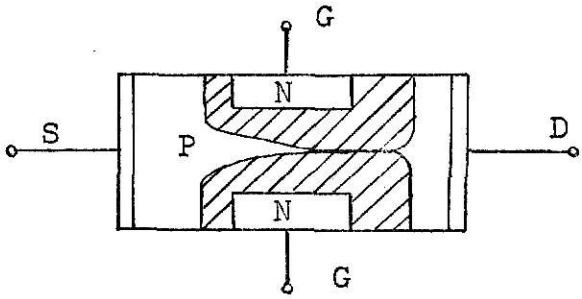
(c) $V_{GS} = 0$

$|V_{DS}| = |V_p|$



(d)* $V_{GS} = 0$

$|V_{DS}| > |V_p|$



(e)* $V_{GS} > 0$

$|V_{DS}| > |V_p|$

Figure 5. Depletion region in JFET with different V_{GS} and V_{DS}. (d)* shows the depletion region thickness is only increased between the gate and the drain. (e)* shows the depletion region is increased at both ends after a reverse bias is applied.

where I_{DSS} is defined as the drain current that flows when the external gate and source terminal are shorted together. Equation (3) is only valid for alloy FETS; another expression of drain current for diffused type channels was derived by G. C. Dacey and I. M. Ross[6], and has the form;

$$I_d = I_{DSS}(1 - V_{GS}/V_p)^2 \qquad (4)$$

When Equations (3) and (4) are plotted on the same graph as shown in Figure 6, that there is a surprisingly narrow range of possible transfer characteristics as indicated by the shaded region.

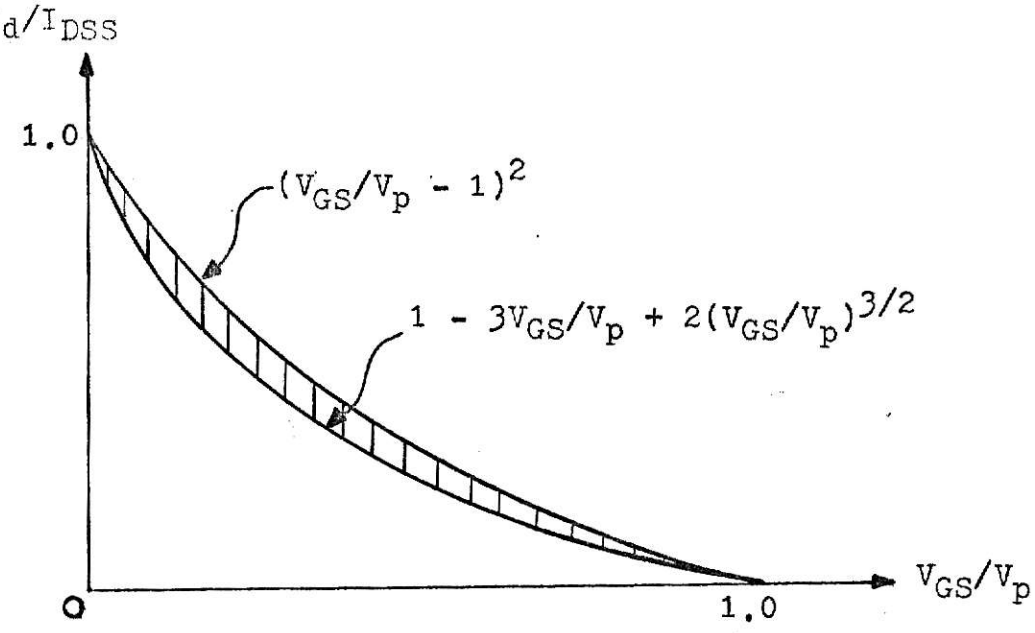


Figure 6. Limits on I_d versus V_{GS} transfer curve with normalized scale.

When an FET is made by some diffusion process (as a matter of fact, most p-n junction FETs are constructed in this manner

6. Dacey, G. C. and Ross, I. M. "The Field-effect Transistor" Bell System Tech. , Vol. 34, pp. 1149-1189, Nov. 1955.

nowadays), the free carrier profile must fall somewhere between the uniform profile and the diffuse profile, and hence approach the square law even more closely[7].

More characteristics can be seen from Figure 7, the drain current I_d versus source-drain voltage V_{DS} with different gate-source voltages V_{GS}. Since both the JFET and MOSFET have much the same drain characteristics, more details will be given in a following section on the MOSFET.

The channel on resistance, $r_{D(on)}$, is the value of the drain-to-source resistance when $V_{GS} = 0$, i. e., the slope of the zero bias output curve at the origin, and is defined as equal to $1/g_{max}$, which is also shown in Figure 7, where g_{max} is the conductance of a parallelepiped section of the channel bounded by the depletion layers at the source end.

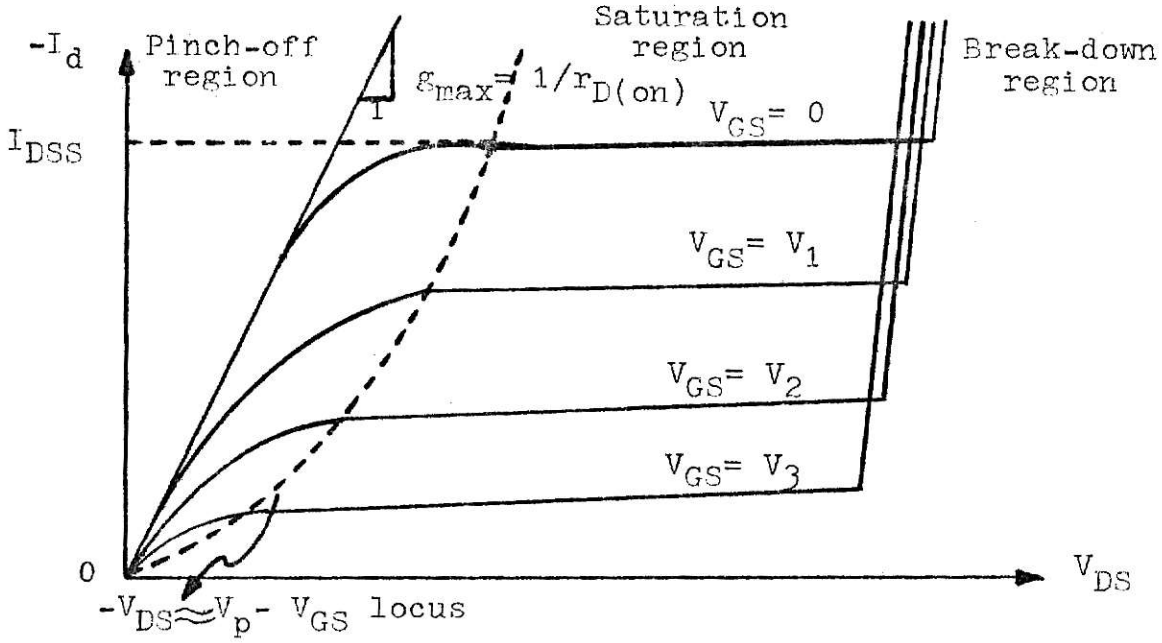


Figure 7. P-channel drain characteristics.

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7. Sevin, Leonce J. "Field-Effect Transistors" page 17-25

Figure 8 shows the input gate characteristics of the JFET, where BV_{GSS} refers to the breakdown gate-source voltage with drain tied to the source. In the normal operating mode, the gate is reverse biased to a voltage between zero and V_p. The input gate current is just the leakage current across a reverse biased p-n junction and is very small; the input impedance is therefore, extremely high. At room temperature the input impedance of a JFET is of the order of hundreds of megohms.

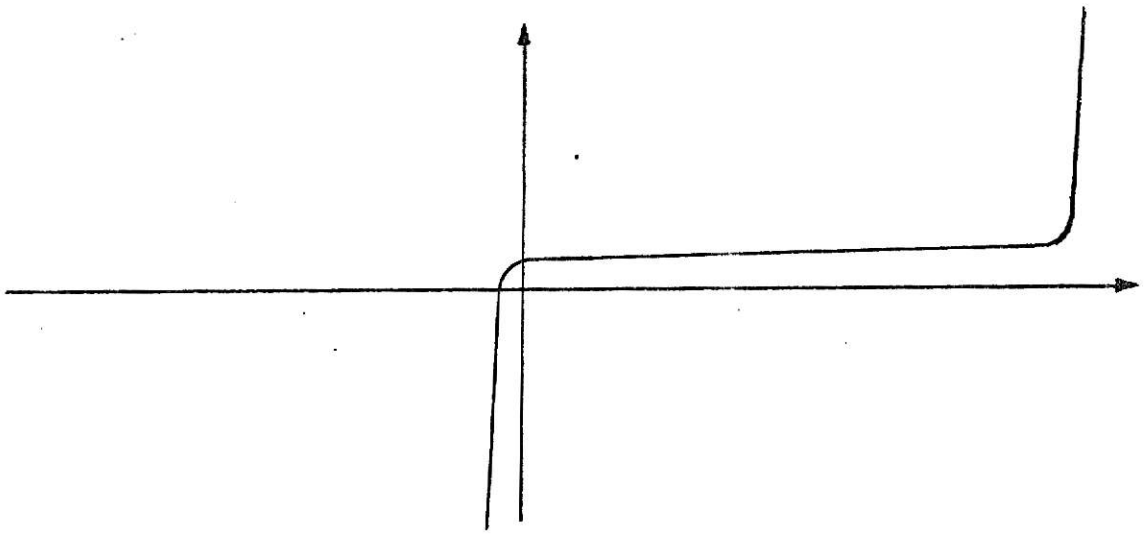

Figure 8. Input characteristics.

The breakdown mechanism in a FET is avalanche breakdown of the gate-to-channel diode, and the reverse voltage on this diode varies along the gate length, being highest at the drain end of the channel. This is why the actual breakdown occurs between the gate and drain terminals. Since the reverse bias between the gate and the source must be increased to reduce drain current, it follows that, for a fixed drain-source voltage, the apparent drain breakdown voltage must decrease monotonically with current.

2. Insulated Gate Field-effect Transistor

The Insulated Gate Field-effect Transistor operates with a different mechanism than the Junction Field-effect Transistor. The latter device uses two junctions as boundaries of the resistor, but the former one uses only one junction. Actually, the junction of the IGFET is formed by the potential difference applied to the gate. The basic structure of an IGFET is illustrated in Figure 9. It can be seen that two separate heavily doped n-type regions are produced in a thin lightly doped p-type silicon block by the planar process. A thin layer of insulating oxide (SiO_2) is formed over the gap region and three electrodes denoted as source, gate and drain are then positioned on top of the structure. Because of the three layers of metal, oxide and semiconductor, the IGFET is also known as the MOS transistor.

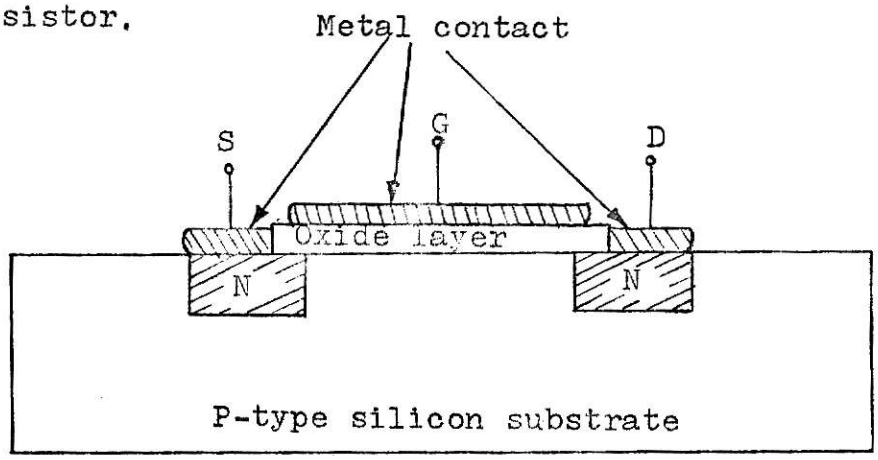

Figure 9. The n-channel MOS transistor structure.

The silicon dioxide gate insulation is made extremely thin (usually 200 Å or less) in order to provide extremely high electric field strengths across the oxide layer when a gate

voltage is applied. Now, if a positive voltage is applied at the gate electrode, an electric field will be directed perpendicularly through the oxide. Because the resistivity of the insulator is much greater than that of the semiconductor, it is reasonable to assume that the resulting electric field exists only in the oxide. This electric field in turn forms an n-type inversion at the surface of the silicon substrate, just below the oxide. The region is called the inversion layer since the surface channel, where electrons are the majority carriers, occurs within a p-type semiconductor. At the same time, because of the existance of the field, a surface charge must also be present there. Thus when a positive gate voltage is applied, a sheet of free electrons is created at the surface, enhancing the original inversion layer; beneath this other electrons rise and combine with the acceptor atoms in the p-type material to form a depletion layer. The charge distribution in the channel when a positive gate voltage is applied is shown in Figure 10. Similarly, a negative voltage will tend to deplete any initial surface inversion layer.

As a result, the gate potential controls the size of the n-surface channel, and thus determines the density of the conduction-band electrons in the gap between drain and source. The drain-to-source conductance will increase as the positive gate voltage increases. For sufficiently small drain-source voltage, this device plays the part of an electrically controlled variable resistor.

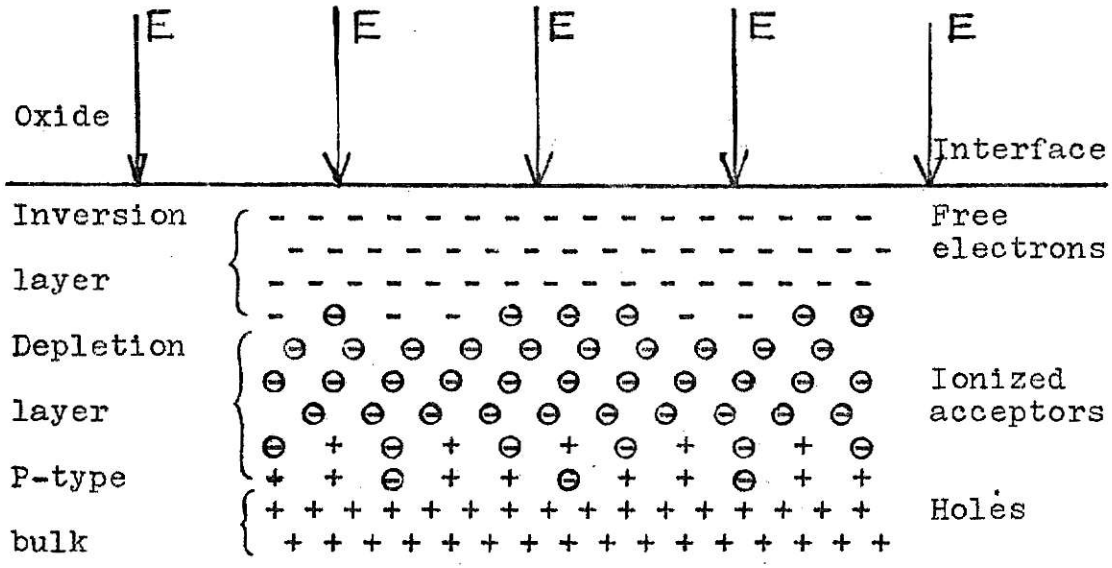

Figure 10. Charge distribution near the silicon surface

In essence, there are two possible modes of operation for an IGFET, the enhancement mode and the depletion mode. Operation in the enhancement mode is synonymous with operation with positive gate voltage (for an n-channel unit); the depletion mode comes into play when the gate voltage is negative. The depletion mode will only be possible when an initial inversion layer that can be depleted by the application of a negative gate voltage exists at zero gate potential. One way to achieve this requirement is to diffuse a moderately doped n-type layer into the p-type silicon substrate as shown in Figure 11.

As a rule, enhancement devices have no initial inversion layer present when the gate voltage is zero. The depletion devices do have an initial inversion layer present. Hence the conductance between the drain and the source for the former device is almost zero in the absence of the gate voltage. But for the latter device, current can flow in the channel when

the gate potential is zero. The depletion units have the advantage of operating with either positive or negative voltage applied to the gate.

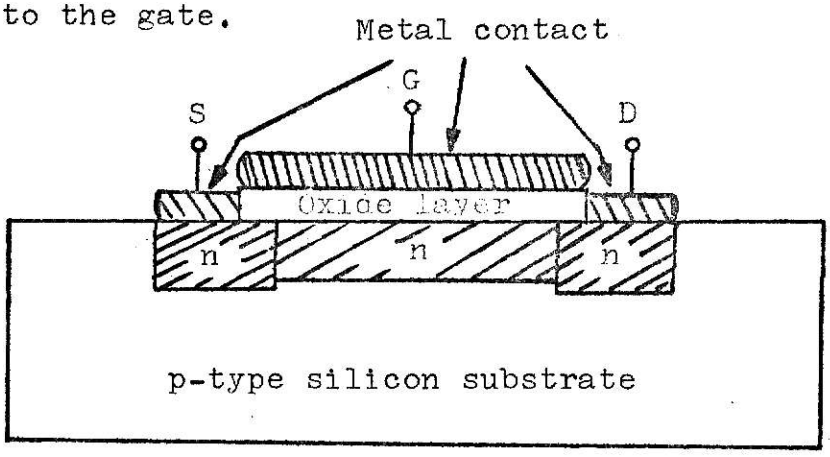

Figure 11. Depletion mode n-channel MOS transistor.

The drain current versus drain-source voltage characteristics of all MOSFETs are shown in Figure 12, and can be divided for discussion into three distinct regions.

As has already been seen, the conductance between the drain and source region in a MOSFET is a function of the gate voltage. In essence, the resistivity of the channel is varied with gate voltage. For small drain-to-source voltages, below the pinch-off voltage, the current path between drain and source will consist of conducting material only. For higher drain-source voltages, however, a depletion region will begin to form near the drain, and the channel will start to pinch-off, as shown in Figure 12, region 1.

At the pinch-off voltage, defined as that value of voltage impressed across the oxide at any point that will just cause the mobile charge concentration at that particular point in the

channel to go to zero, the inversion layer is no longer formed. For drain-to-source voltages above pinch-off, the current will saturate, and the device will be operating in region 2. Operation in this region results in an increase in the depletion regions together with a associated reduction in channel length at the drain end. Under normal operating conditions, the drain diode in a MOSFET is reverse-biased and the output resistance is very high, hence the current still remains almost constant for large changes in V_D. If the drain-source voltage keeps increasing, the current will rise sharply because of the occurance of avalanche breakdown, as in the region 3.

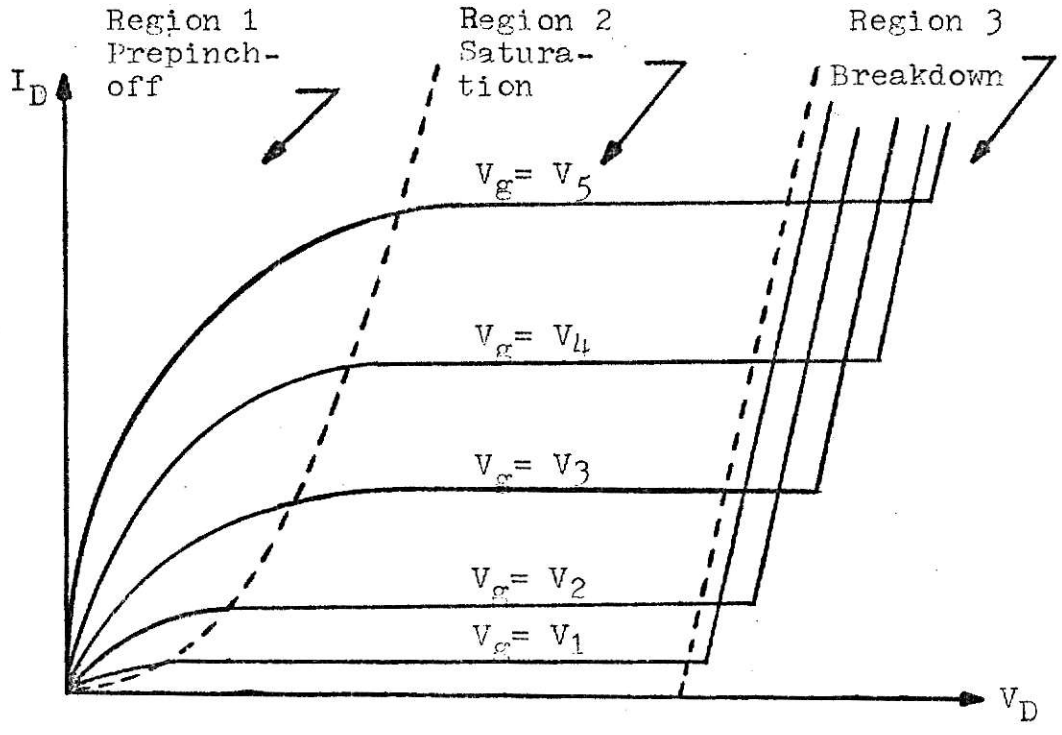

Figure 12a. I_D versus V_D for an enhancement n-channel MOSFET (subtrate grounded).

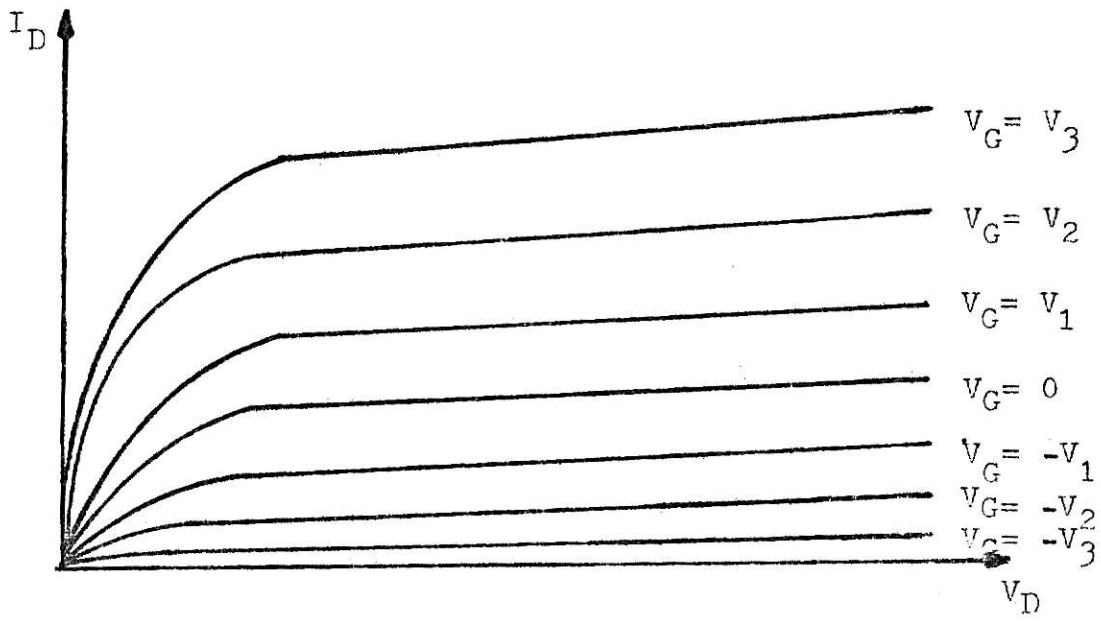

Figure 12b. I_D versus V_D of a depletion MOSFET.

Figure 13 shows the MOSFET transfer characteristic curve for both enhancement and depletion modes with drain-source voltage held constant. The threshold value of gate to source voltage, V_{th}, is defined as the voltage across the gate oxide layer just necessary to produce inversion in the channel. From the device depletion curve, one notes this device can not only be operated in the normal way (reverse characteristic region), but also may have usable forward characteristics for quite large gate voltages. Both modes exhibit behavior as a square-law device.

There are three important temperature effects in an FET. The first effect is that the reverse-biased gate-channel junction exhibits a leakage current having the usual exponential dependence on temperature. This effect is particularly important at high temperatures for a JFET. The second effect is

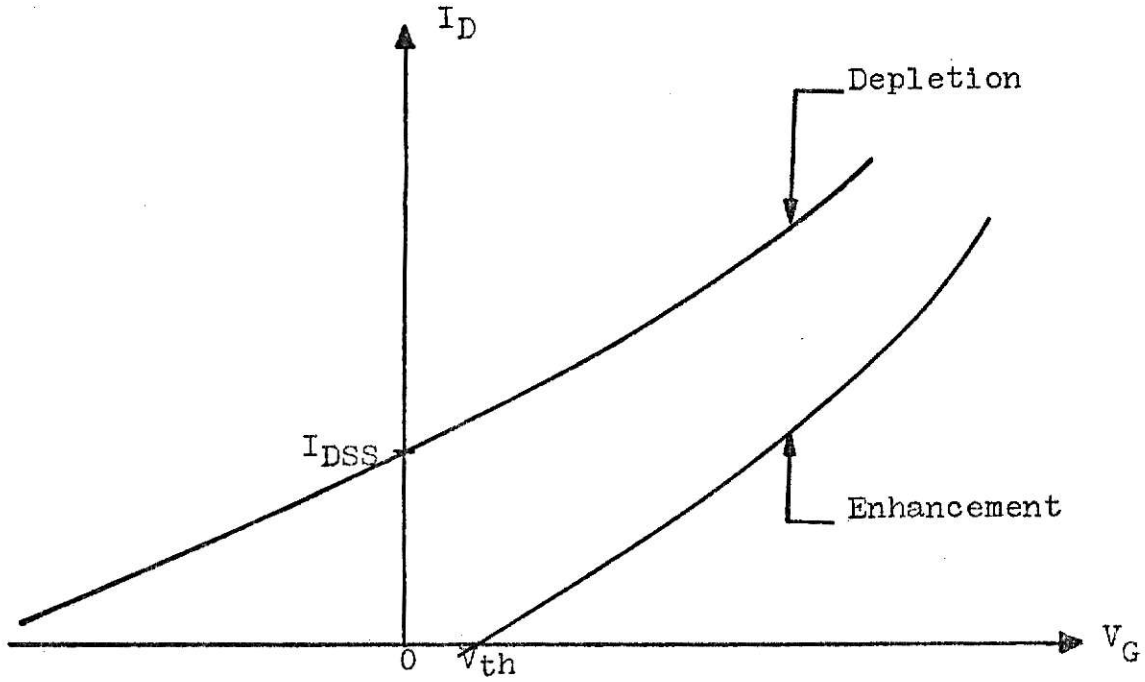

Figure 13. The MOSFET transfer characteristic curve.

involved with the drain current at fixed gate bias, and produces a negative dependence of drain current on temperature. The last effect is that mutual conductance shows a temperature dependence similar to that of the drain current. A more detailed discussion of temperature effects are given by Sevin[4], and Richman[8].

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8. P. Richman "Characteristics and Operation of MOS Field-Effect Devices."

III. HIGH FREQUENCY ANALYSIS

1. Tuned Amplifiers

The field-effect transistor is a majority carrier device and thus has the general capability of operating at high frequencies. Many FETs retain a relatively large transconductance up to near one GHZ. The FET also has some particular characteristics that permit performance superior to either bipolar transistor or tube; such as high input impedance, low cross modulation, good r-f selectivity and capability to withstand interfering signals. These considerations are of considerable significance in communication system design.

Parasitic interelectrode capacitances of the FET are similar to those for a triode vacuum tube. It is usually necessary to consider the input and output capacitances as a part of the tuned circuits. Although these capacitances are still associated with p-n junctions and thus are sensitive to bias voltage, the magnitude of the problem is uaually less severe than with bipolar transistors.

(a) Admittance parameters and the equivalent circuit

Because of the nature of its high input and output impedance characteristics, it is common practice to specify the FET by its equivalent short-circuit admittance parameters. The admittance specification of a two-port is illustrated in Figure 14, the relationship between the input and the output is given by:

$$I_1 = Y_{11}V_i + Y_{12}V_o \qquad (5a)$$

$$I_2 = Y_{21}V_i + Y_{22}V_o \qquad (5b)$$

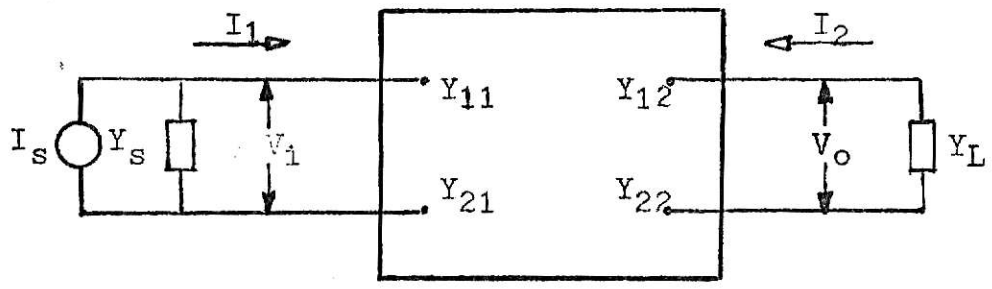

Figure 14. Two-port admittance representation of a network

The input admittance, Y_{11}, is the admittance of port 1 when port 2 is short-circuited($V_o = 0$). The reverse transfer admittance, Y_{12}, is the transfer admittance from port 2 to port 1 when port 1 is short -circuited($V_i = 0$). The forward transfer admittance, Y_{21}, is the transfer admittance from port 1 to port 2 when port 2 is short-circuited($V_o = 0$); it is also termed the forward transadmittance. The output admittance, Y_{22}, is the admittance of port 2 when port 1 is short-circuited($V_i = 0$).

The field-effect transistor, just like the other three terminal active network, can be operated in an amplifier circuit with any of its three terminals as the common terminal. Usually, the source is most frequently used as the common electrode, a connection analogous to the common cathode vacuum tube amplifier. The set of common source admittances can be written as:

Input admittance:

$$Y_{is} = g_{is} + jb_{is} \tag{6a}$$

Reverse transfer admittance:

$$Y_{rs} = g_{rs} + jb_{rs} \tag{6b}$$

Forward transfer admittance:

$$Y_{fs} = g_{fs} + jb_{fs} \tag{6c}$$

Output sdmittance:

$$Y_{os} = g_{os} + jb_{os} \tag{6d}$$

where g represents the conductive part, and b, the susceptive part of the admittance.

Using the matrix notation of circuit analysis, the common source admittance matrix can be written as,

$$Y_s = \begin{bmatrix} Y_{is} & Y_{rs} \\ Y_{fs} & Y_{os} \end{bmatrix}. \tag{7}$$

The high frequency equivalent circuit of an insulated gate field-effect transistor is shown in Figure 15.

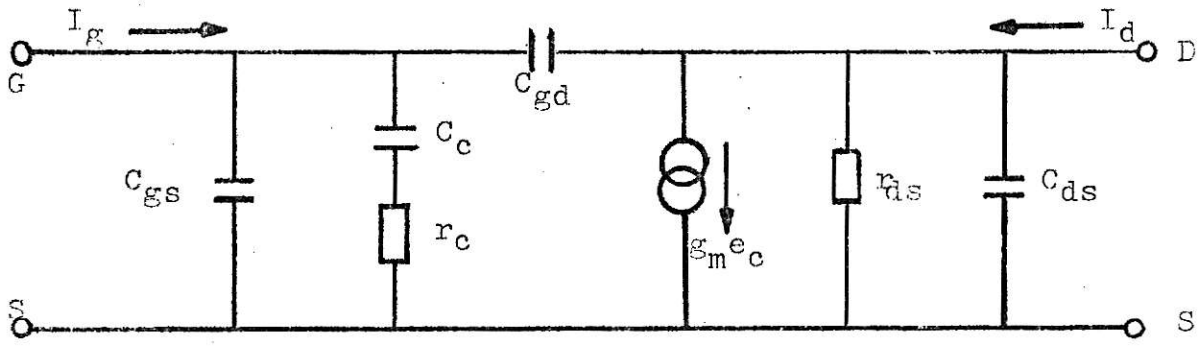

Figure 15. High frequency equivalent circuit of an IGFET

The elements C_{gs}, C_{gd}, and C_{ds} are the interlead capacitances between the elements designed by the subscripts. C_c and r_c in series are a lumped approximation of the actual distributed network formed between the active channel resistance and the metallized gate. Consequently, the high frequency performance is a function of the time constant associated with C_c and r_c. The generator $g_m e_c$ acts as a relatively constant

current source in the pinch-off region, where g_m is the transconductance and e_c, is the voltage across C_c. The resistance, r_{ds}, shown in shunt with the $g_m e_c$ generator represents the dynamic output resistance of the transistor.

By calculating the two-port admittances for this circuit we can express the frequency variation of the admittance parameters by,

$$Y_{is}=\frac{I_g}{V_{gs}} = \frac{r_c}{r_c^2+ (1/wC_c)^2} + jw\left[C_{gs}+ C_{gd}+\frac{C_c}{1 + (wr_cC_c)^2}\right] \quad (8a)$$

$$Y_{fs}=\frac{I_d}{V_{gs}} = \frac{g_m}{1 + jwr_cC_c} - jwC_{gd} \quad (8b)$$

$$Y_{rs}=\frac{I_g}{V_{ds}} = - jwC_{gd} \quad (8c)$$

$$Y_{os}=\frac{I_d}{V_{ds}} = \frac{1}{r_{ds}} + jw(C_{ds}+ C_{gd}) . \quad (8d)$$

The two-port common-source admittances for an typical insulated gate field-effect transistor are shown in Figures 16 to 19[9]. From these figures it is easy to see that the input admittance remains largely susceptive up to several hundreds MHZ, and that the reverse transfer admittance is dominated by the feedback capacitance from drain to gate. The forward transfer admittance is essentially constant and real up to about 60MHZ, so that the low-frequency concept of a real transfer admittance is applicable up to this frequency. The real

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9. D. M. Griswold, Unpublished work.

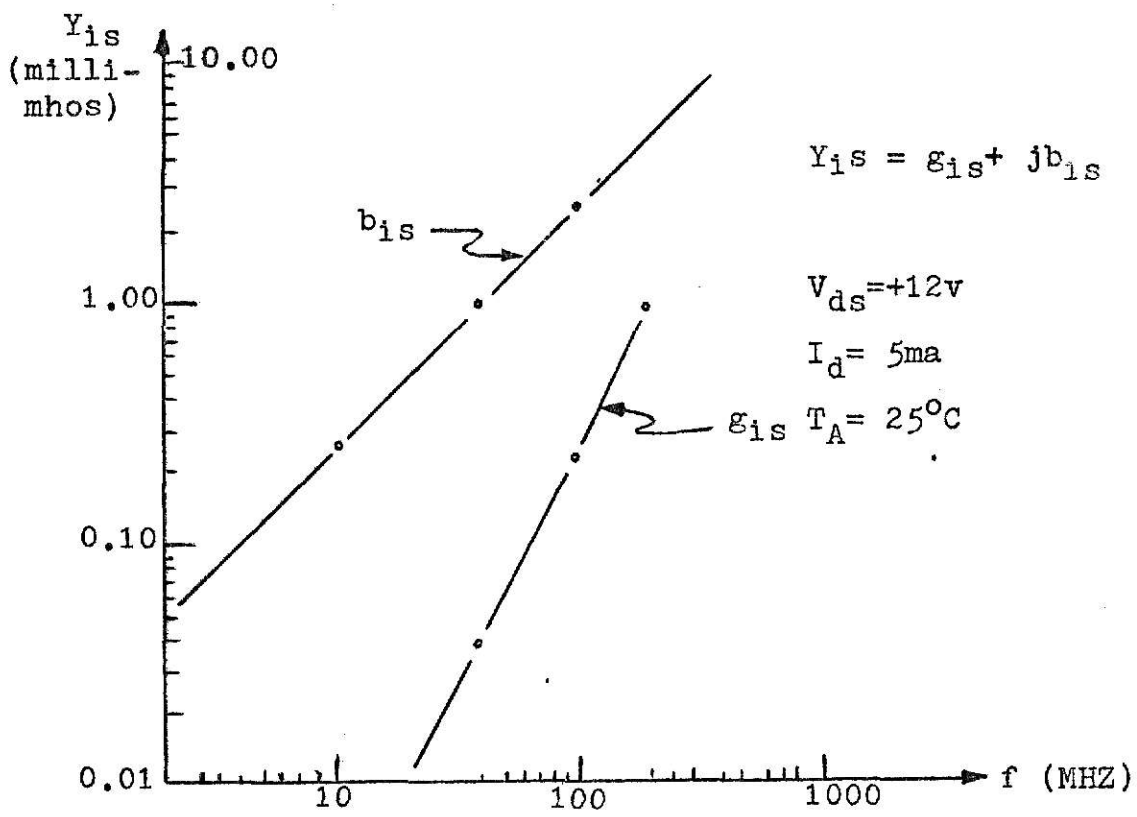

Figure 16. Input admittance

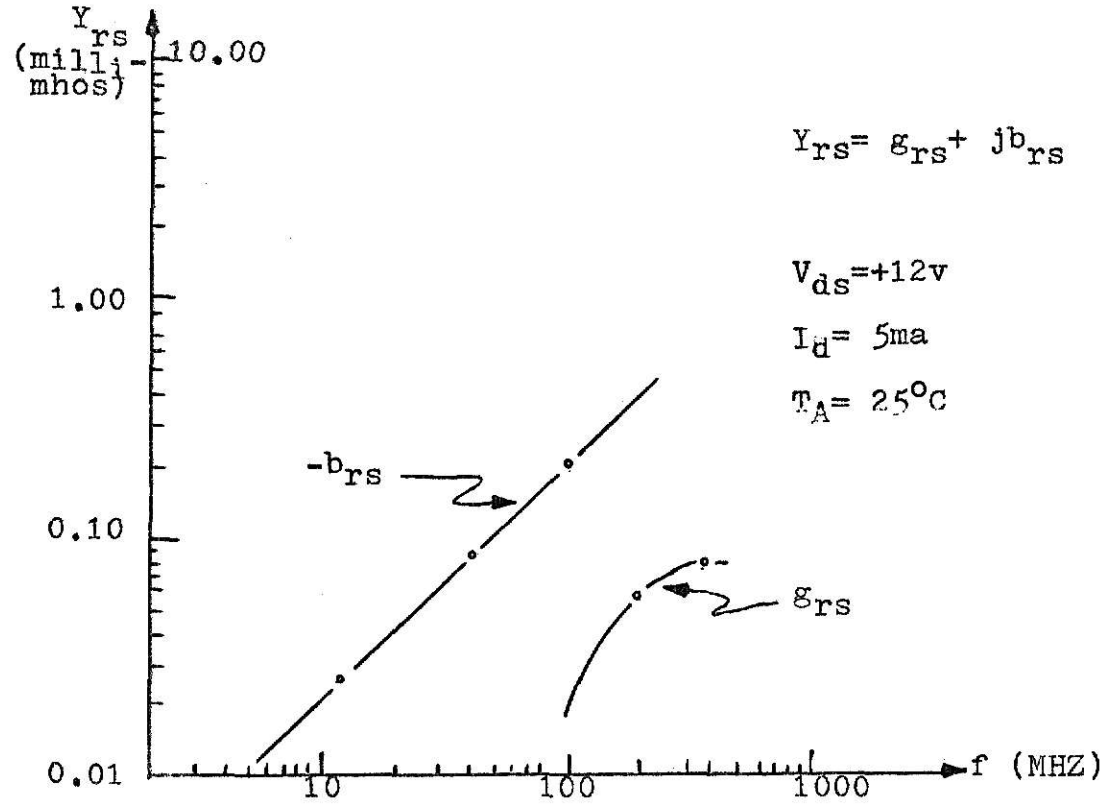

Figure 17. Reverse Transfer admittance

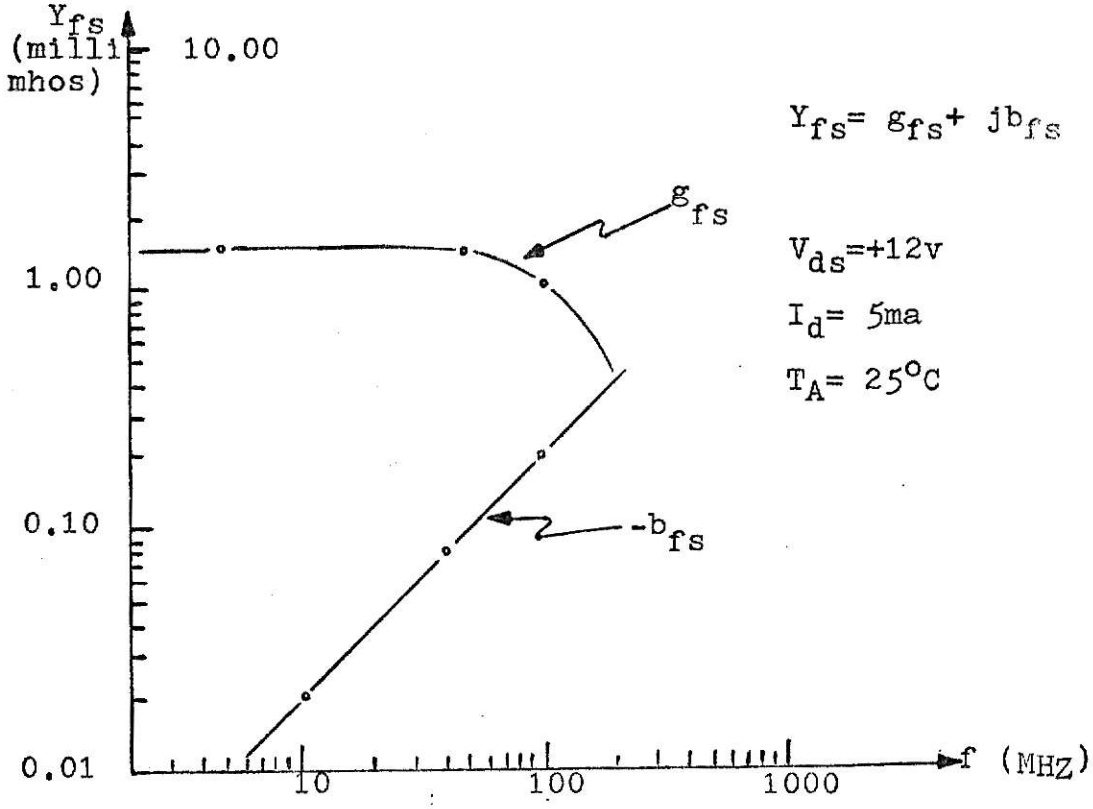

Figure 18. Forward transfer admittance

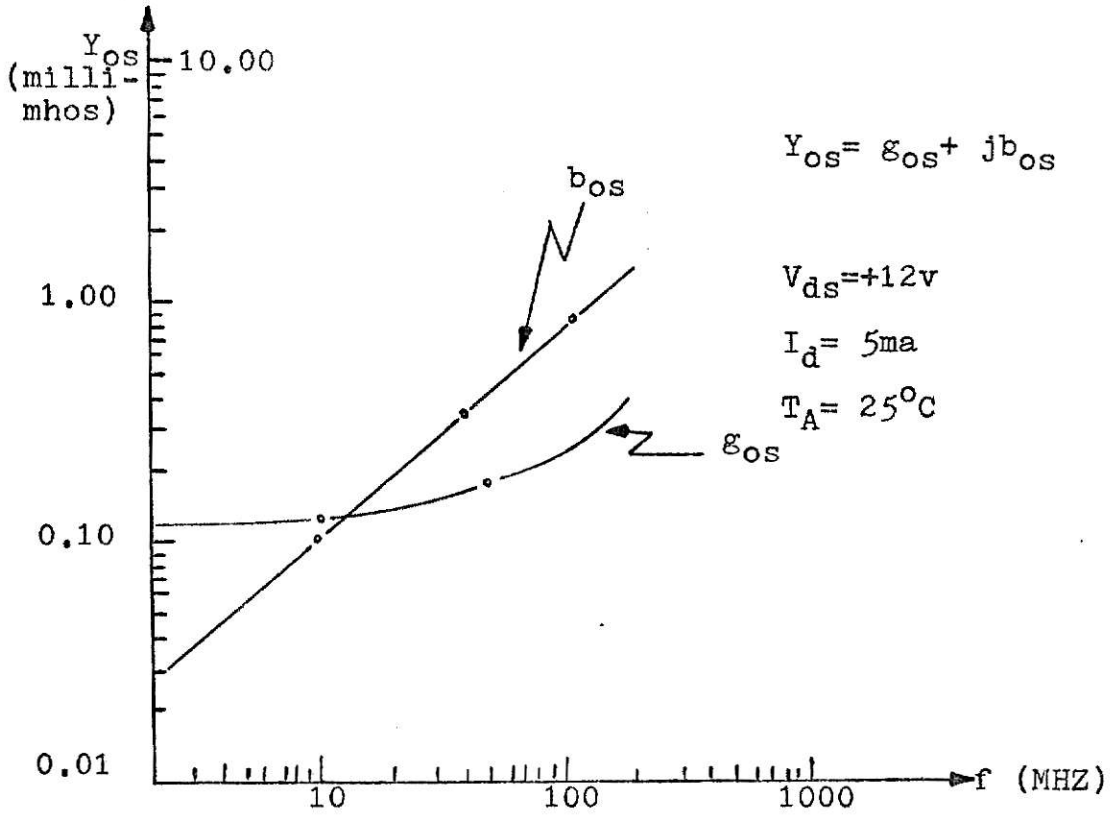

Figure 19. Output admittance.

and imaginary components become equal in magnitude at about 200 MHZ. Because the output resistance of a FET with its pentode-like characteristic is high, the conductive and susceptive components of the output impedance become equal near 10MHZ. The susceptive components of Y_{os} and Y_{rs} vary linearly with frequency as expected from Eq. (8d) and Eq. (8c). The susceptive components of Y_{is} and Y_{fs} vary somewhat differently as would be expected from the presence of the r_c terms in both Eq. (8a) and Eq. (8b).

Generally, the characteristics of a field-effect transistor at high frequencies are analogous to those for similar vacuum-tube configurations. The common-gate FET is analogous to a grounded-grid vacuum tube with its high input admittance. The common-drain FET has low input admittance and high output admittance as does the cathode follower. The common-source FET is analogous to a common-cathode vacuum tube; the input admittance is very low compared with the common-gate FET.

There are four popular types of FET tuned amplifiers named unneutralized common-source, neutralized common-source, cascode and common-gate. Since the unneutralized power gain is given by[10,11]

$$G_{oo} = \frac{Y_{rs}^2}{4\mathrm{Re}Y_{is}\mathrm{Re}Y_{os} - 2\mathrm{Re}Y_{fs}Y_{rs}} \qquad (9)$$

and the stability factor, C, is evaluted as

$$C = 2G_{oo}\left|\frac{Y_{fs}}{Y_{rs}}\right| \qquad \begin{array}{l}\text{stable if } C<1\\ \text{unstable if } C>1\end{array} \qquad (10)$$

10. R. F. Shea, Transistor applications.(John Wiley & Sons,Inc.)

11. W. Gartner, Transistors principles, design and applications.

For most unneutralized common-source FET tuned amplifiers, C is greater than unity at higher frequencies where the FET has usavle gain. Circuits in common-source connection in high frequency applications, therefore, must be neutralized.

Neutralization has come to be known as unilateralization among designers of solid-state circuits. The concept is that the solid-state device in a circuit is made to function in one direction only. A nonunilateral active network can be made unilateral by connecting it in parallel with a passive two-port network whose reverse transfer admittance is the negative of the reverse transfer admittance of the active two-port. When a FET amplifier is neutralized, the input and output admittances are independent of the source and load admittances. The input and output networks can therefore be designed independently of one another. It can be shown that the amplifier gain will be a maximum if the source and load admittances are the conjugates of the FET input and output admittances respectively. For a neutralized circuit, the maximum neutralized power gain is then given by,

$$G_{max} = \frac{|Y_{rs} - Y_{fs}|^2}{4(g_{is} + g_{fs})(g_{os} + g_{fs})} \qquad (11)$$

Figure 20 shows a typical neutralized common-source high frequency tuned amplifier. Neutralization components L_n and C_{n1}, C_{n2} provide an external feedback path that is made equal in magnitude, but opposite in phase, to that contained within the FET proper. Source impedance is 1K at the operating

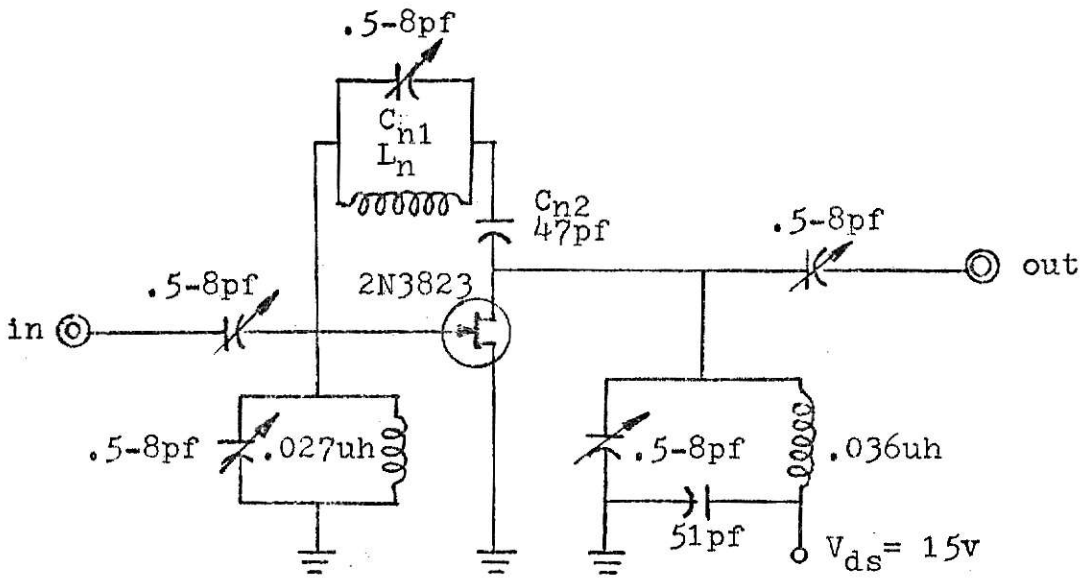

Figure 20. Common-source 200MHZ amplifier.[12]

frequency and load impedance is about 5K.

(b) Cross-modulation

Cross-modulation is the transfer of modulation from an undesired radio-frequency signal to a desired signal. This results in an undesired station or signal being heard on the desired signal to which a radio receiver is tuned.

One of the most important advantages of the FET in r-f circuitry is its low cross-modulation. Since cross-modulation is proportional to undesired signal voltage appearing between gate to source, the cross-modulation performance of a common-gate amplifier is superior to that of a common-source amplifier when each circuit is optimized for low-noise performance

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12. J. B. Compton, Junction FET HF amplifiers, Wescon 1966 Convention Record, Session 22/3.

at the operating frequency. This should be expected since optimum input impedance in a common-source circuit is very much higher than in a common-gate circuit, especially in high frequency ranges. At 100MHZ, for example, the optimum input impedance in common-gate circuit is only about 300 ohms, while that of common-source circuit reaches about 1K.

In order to get better insight into this problem, let us consider it mathematically. The FET transfer characteristic $i_d = f(v_i)$ can be developed in the neighborhood of the bias point I_{DP} into a Taylor series:

$$i_d = I_{DP} + S_1 v_i + \frac{1}{2!} S_2 v_i^2 + \frac{1}{3!} S_3 v_i^3 + \cdots\cdots\cdots\cdots \quad (12)$$

where i_d is the drain current, v_i, the input voltage, S_1, S_2, S_3 represent the first, second and third derivatives $d^n i_d / dv_i^n$ for (n= 1, 2, 3).

Introducing the voltage $v_i = V_1 \cos w_1 t + V_2 \cos w_2 t$, the wanted signal plus the interfering signal, into Eq. (12), and neglecting I_{DP}, which is a constant, and also v_i^4 and the higher terms,

$$i_d = S_1(V_1 \cos w_1 t + V_2 \cos w_2 t) + 1/2\ S_2(V_1 \cos w_1 t + V_2 \cos w_2)^2 + 1/6\ S_3(V_1 \cos w_1 t + V_2 \cos w_2 t)^3 \quad (13)$$

Since in a tuned circuit resonant at the angular frequency w_1, only those terms containing $\cos w_1 t$ are important , and using the formula:

$$\cos^2 A = \frac{1}{2}(1 + \cos 2A)$$

$$\cos^3 A = \frac{1}{4}(\cos 3A + 3\cos A)$$

the fundamental component of the current can be written:

$$i_{d1} = \left(1 + \frac{S_3}{8S_1} V_1^2 + \frac{S_3}{4S_1} V_2^2\right) S_1 V_1 \cos w_1 t. \qquad (14)$$

Cross-modulation mostly occurs when a weak transmission is being received, i.e. when V_1 is small compared with V_2; Eq. (14) may therefore be simplified to:

$$i_{d1} = S_1 V_1 \cos w_1 t\left(1 + \frac{S_3}{4S_1} V_2^2\right). \qquad (15)$$

This formula confirms the fact that the amplification of the wanted signal is dependent on the amplitude of the interference, unless the second term (S_3 term) in the progression can be neglected.

If the interfering signal is modulated, V_2 in Eq. (15) must be replaced by $V_2(1+ m_2\cos pt)$, where m_2 stands for the modulation depth and p the modulation frequency of the interfering. The result of this substitution is

$$i_{d1} = S_1 V_1 \cos w_1 t\left[1 + \frac{S_3}{4S_1} V_2^2 (1+m_2^2/2) + \frac{S_3}{2S_1} V_2^2 m_2 \cos pt\right] \qquad (16)$$

$$= S_1 V_1 \cos w_1 t\left[1 + \frac{S_3/2S_1 \; V_2^2 m_2}{1+S_3/4S_1 \; V_2^2(1+m_2^2/2)} \cos pt\right] \qquad (16a)$$

It is apparent that the wanted signal of frequency w_1 is modulated by the interference to a depth of m_k, thus,

$$m_k = \frac{S_3/2S_1 \; V_2^2 m_2}{1 + S_3/4S_1 \; V_2^2(1+m_2^2/2)}. \qquad (17)$$

For a small enough value of V_2, m_k reduces to:

$$m_k \approx \frac{S_3}{2S_1} V_2^2 m_2 = Km_2 \qquad (18)$$

In this equation, the interference which is transfered to the wanted signal is expressed as a fraction K of the modulation m_2 of the unwanted transmission. K is termed the cross-modulation factor and is dependent on the amplitude V_2 of the interfering signal. If equation (18) is rewritten as

$$K = \frac{m_k}{m_2} = \frac{S_3}{2\ S_1}\ V_2^2 \qquad (19)$$

it is apparent that the cross modulation factor is independent of the wanted signal, and directly proportional to the square of the interfering signal.

In order to compare devices for cross-modulation, it is desirable to compare the devices in comparable systems. An approach to a system comparison can be made considering signal power. Thus,

$$\text{interfering signal power} = V_{is}^2/R, \qquad (20)$$

where V_{is} is the input voltage (of the device) that causes 1% cross-modulation; and where $R = R_s R_i / R_s + R_i$, R_s is the source resistance and R_i is the input resistance of the device. As the input resistance for all these devices increases with increased gain control, at some gain-control point R approaches R_s. The 1% cross-modulation versus gain control is shown in Figure 21, a comparison of cross-modulation performance of an IGFET, a bipolar transistor and a vacuum tube at 216MHZ. The better performance of the IGFET is evident.

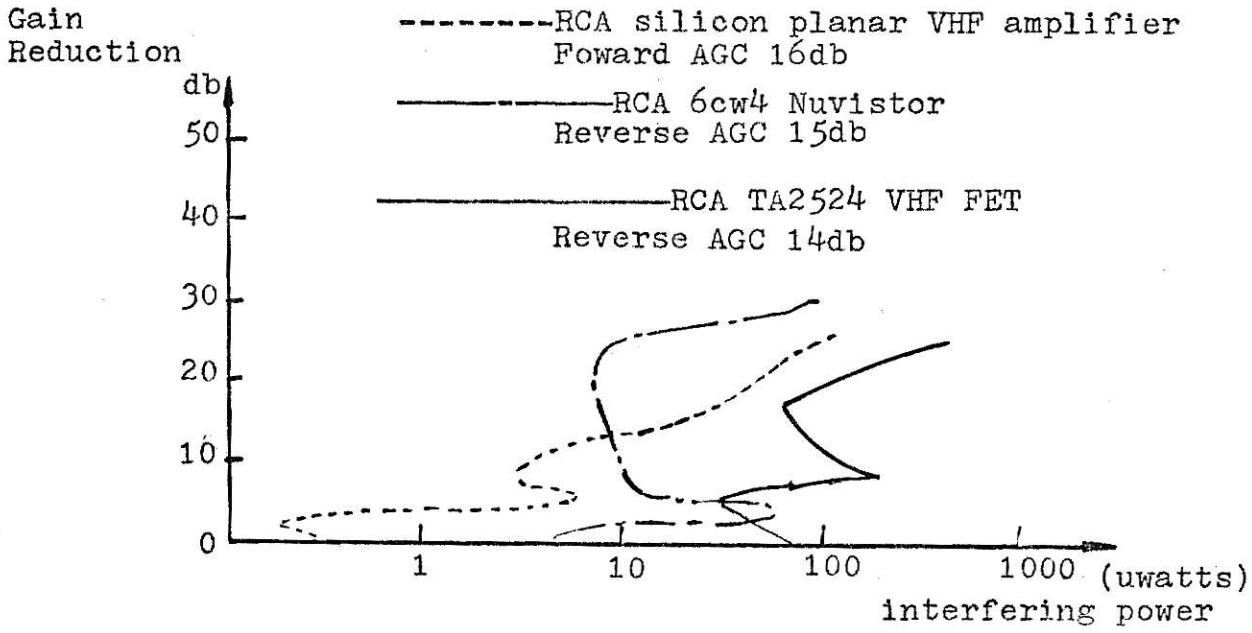

Figure 21. Comparison of cross-modulation performance of an IGFET, a bipolar transistor and a vacuum tube.[13]

(c) Automatic gain control

In field-effect transistors a facility for controlling gain can be achieved in two ways. One method uses an FET operated at drain voltage below pinch-off as a variable ohmic resistance in an attenuator circuit either in the foward or feedback path of the amplifier. The amount of gain variation obtainable depends on signal magnitude. Substantial distortion will result if large input signals are applied to an amplifier biased near the cut-off gate voltage.

A simple AGC circuit is constructed as in Figure 22. With the help of Figure 7, it can be seen that when the FET is pinched-off, (V_{AGC} greater than V_p) then the gain of the circuit

depends only the series resistor R_s and the loading at the output. If the load can be neglected, $V_o/V_i = 1$. When the FET is operated below the pinch-off, V_{AGC} less than V_p, the voltage attenuation ratio is given by

$$A_v = V_o/V_i = \frac{r_{ds}}{R_s - r_{ds}} \tag{21}$$

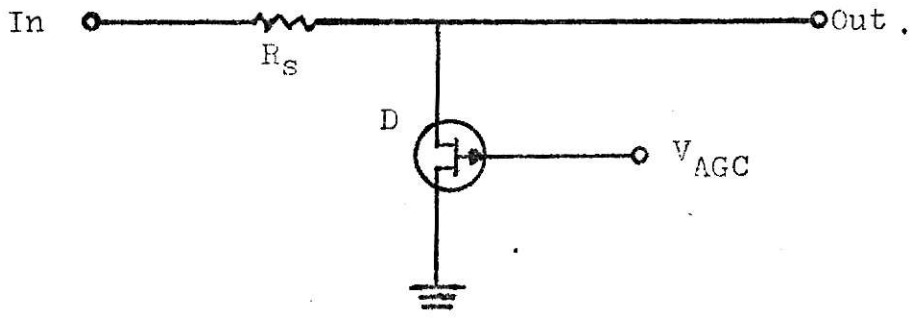

Figure 22. Simple AGC FET circuit.

since r_{ds} is controlled by gate voltage, provided the gate voltage is large compared with the drain voltage. Normally, $r_{ds} = 1/g_m$.

Now by rewriting Eq. (4) and by differentiating I_d with respect to V_{GS}:

$$I_d = I_{DSS}(1 - V_{GS}/V_p)^2 \tag{4}$$

$$dI_d/dV_{GS} = g_m = 2I_{DSS}/V_p (V_{GS}/V_p - 1), \tag{22}$$

so that for the case $V_{AGC} = V_{GS}$,

$$A_v = \frac{r_{ds}}{R_s + r_{ds}} = \frac{1}{1+g_m R_s} = \frac{1}{1+\frac{2I_{DSS}}{V_p}\left(\frac{V_{AGC}}{V_p} - 1\right) R_s}. \tag{23}$$

13. J. Torkel, Wallmark & Harwick Johnson "FETs Physics, Technology and Applications"

The minimum posible value of Eq. (23) occurs when $V_{gs}=-\phi$, i.e. let gate bias equal to contact potential (see page 4). Thus

$$(A_v)_{min} = \frac{1}{1 - \frac{2I_{DSS}}{V_p}\left(\frac{V_p + \phi}{V_p}\right) R_s} . \qquad (24)$$

It is possible to obtain a large AGC range this way; for example, if R_s= 500K, and I_{DSS}= 2ma, V_p= 2v, ϕ = 0.5v, the maximum AGC range is the reciprocal of Eq. (24) or about 1250, this is greater than 60db. It is also evident from Figure 7 that the signal should be kept fairly small because the nonlinearity of drain-source resistance can introduce large amounts of distortion. However, this circuit will be far more versatile than any comparable circuit using bipolar transistors. The disadvantage of this scheme is the circuit has no gain, it only attenuates.

Figure 23 shows a circuit that uses a FET as a variable emitter resistor in a bipolar transistor amplifier. The gain of such amplifier is very nearly

$$A_v = - R_c/r_{ds} = - g_m R_c . \qquad (25)$$

If the FET is assumed to be a good square-law device,

$$A_v = - \frac{2I_{DSS}}{V_p}\left(V_{AGC}/V_p - 1 \right) R_c . \qquad (26)$$

The voltage gain is a linear function of the AGC voltage at least so long as the FET transfer curve is a parabola. The advantage is, however, achieved at the cost of including a transistor, although this can contribute gain.

The second method of obtaining AGC depends on the variation of g_m, the mutual conductance, with I_d and hence V_{GS}.

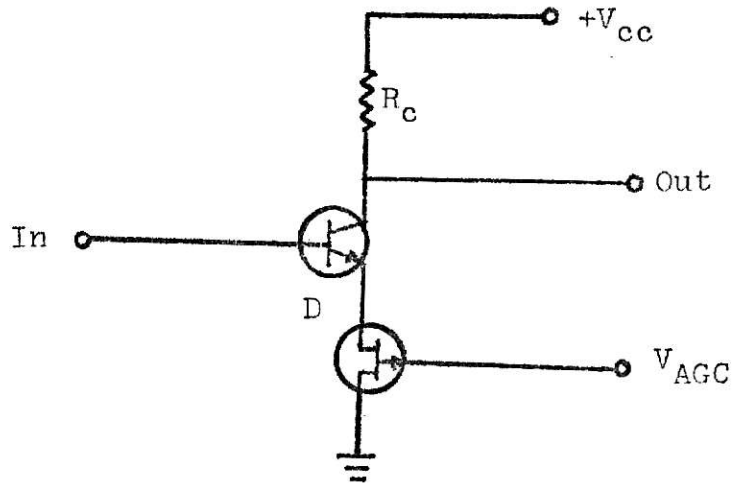

Figure 23. Amplifier stage with provision for AGC.

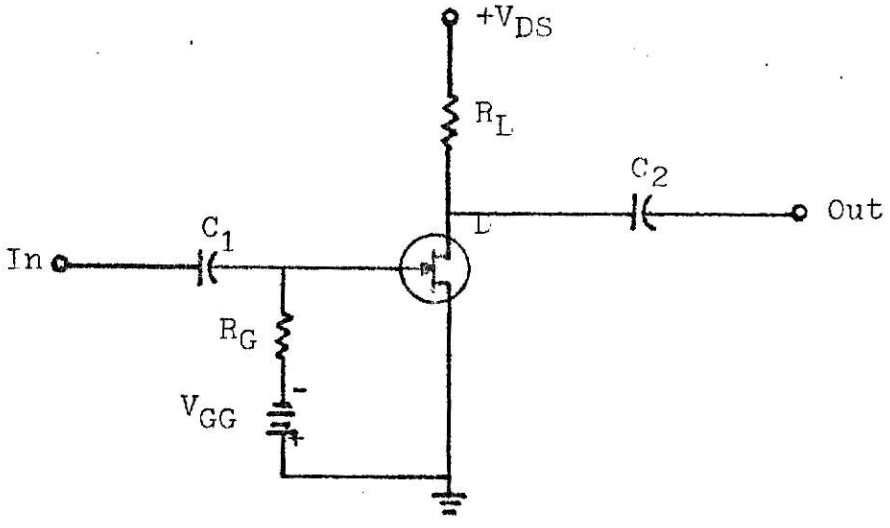

Figure 24. Simple common-source amplifier with fixed bias.

This can be shown by the simple common-source FET amplifier shown in Figure 24, where fixed-gate bias was used. As the value of V_{GG} (which will be very nearly equal to V_{GS} unless leakage current is high or R_G is very large) is increased in magnitude, the drain current will drop and g_m, the mutual conductance of the FET will decrease

from its zero-gate-bias value of g_{mo} in approximately the following manner if Eq. (4) properly describes the transfer characteristic:

$$g_m = g_{mo}(1 - V_{GS}/V_p). \tag{27}$$

Since the voltage gain is proportional to the transconductance, the value of A_v will vary from its zero-gate-bias value A_{vo} in roughly the following manner:

$$A_v = A_{vo}(1 - V_{GS}/V_p). \tag{28}$$

Using equation (28), a normalized form of A_v/A_{vo} versus V_{GS}/V_p is plotted as shown in Figure 25. The linearity of A_v as a function of V_{GS} is perfect only for the ideal case, since the value of the drain voltage is also changing as the control voltage is varied. The effect of V_{DS} on g_m will enter into the exact control relationship.

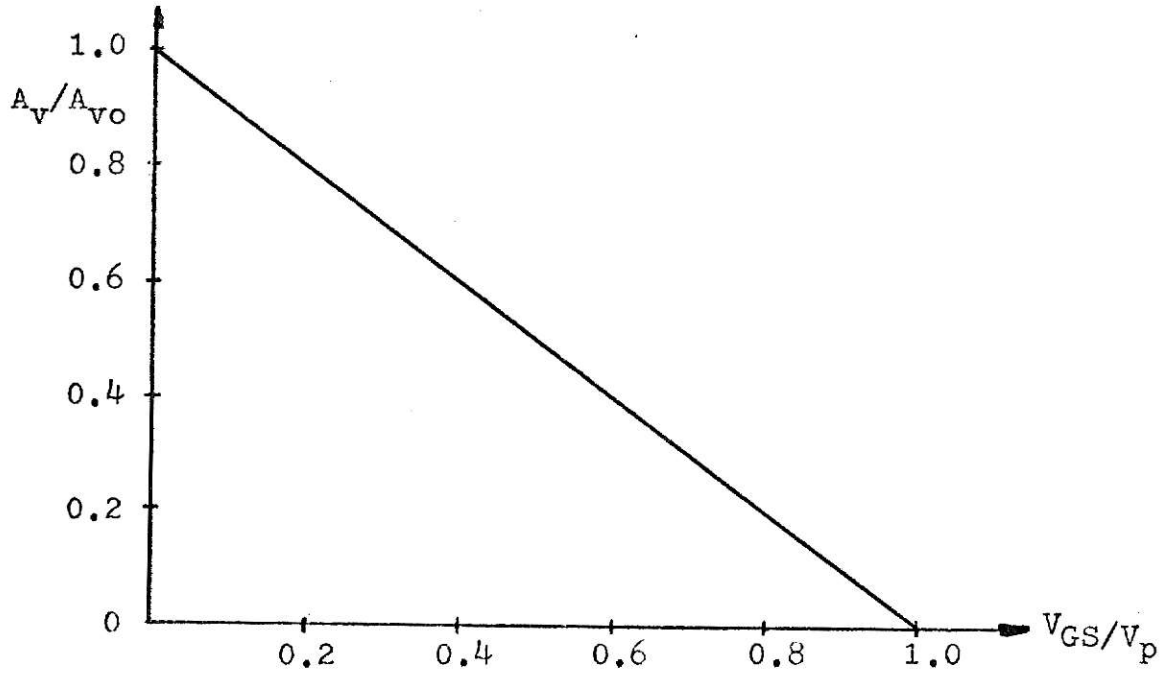

Figure 25. Theoretical AGC characteristic.

(d) Noise considerations

There are three basic noise sources in FET's: Thermal noise, Gate-leakage-current noise, and 1/f noise.

Thermal noise is produced by the channel resistance and by parasitic source and drain resistances. Because the gate junction is reverse biased, the fluctuations (caused by the random motion of charge carriers--it exists whenever there is current) in the current flow through a reverse biased p-n junction can be expressed as shot noise. The term 1/f noise refers to a type of noise whose power density varies inversely with frequency. The exact mechanisms that cause 1/f noise are still open to question. However, this noise has a relation to fabrication uniformity as well as to junction and circuit leakages.

Since shot noise is result of the random motion of charge carriers, and this random charge motion is uniform over the frequency spectrum, a mean-square noise current ($\overline{i_g^2}$) can be stated as an equation:[14]

$$\overline{i_g^2} = 2e(I_1 + I_2) B \qquad (29)$$

where,

e is the electron charge (1.602×10^{-19} coulombs),

I_1 and I_2 are the forward and reverse (leakage) current, respectively, in the gate-channel junction, and

B is the frequency bandwidth.

Thermal agitation of the carriers in the FET channel is

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14. Van der Ziel, "Thermal Noise in Field-effect Transistors" Proc. IRE 50 (1962) 1808-1812.

responsible for the electrical energy that creates the so-called thermal noise. Since it is temperature related, it does not exist at absolute zero. Like shot noise, it is uniform over the frequency spectrum, and its mean-squared noise current ($\overline{i_d^2}$) varies directly with the channel resistance, bandwidth, and temperature. Stated as an equation:[14]

$$\overline{i_d^2} = 4kTg_{ms}Q(V_g, V_d)\,B \tag{30}$$

where,

k is Boltzmann's constant (1.38×10^{-23} watt-second/degree)

T is absolute temperature, in degrees Kelvin,

g_{ms} is the transconductance in saturation region for the given gate bias V_g,

$Q(V_g, V_d)$ is a function of the operating points, usually less than unity, and

B is noise bandwidth.

Under practical operating conditions, the channel thermal noise can be expressed as an equivalent noise resistance:

$$R_{eq} = \frac{Q(V_g, V_d)}{g_{ms}} \qquad \begin{array}{l} Q = 1 \text{ for JFET} \\ Q = .67 \text{ for IGFET} \end{array} . \tag{31}$$

At higher frequencies, the gate noise of an FET increases rapidly with increasing frequency. This effect is attributed to the thermal noise of the conducting channel and is caused by the capacitive coupling between the channel and gate. A complete calculation for high frequency of an FET noise model represented by gate and drain noise generators has been developed by Van der Ziel,[15]

$$\overline{i_g'^2} = \overline{i_g^2} + \frac{4kTB}{g_{ms}} w^2 C_{gs}^2 \frac{g_1(y,z)(1-z^{1/2})}{f_1^3(y,z) f_2^2(y,z)} \tag{32}$$

$$\overline{i_d'^2} = 4kTBg_{ms} \frac{g_2(y,z)}{(1-z^{1/2}) f_2(y,z)} , \tag{33}$$

where $y = W_d/W_{oo}$, $z = W_s/W_{oo}$, $z \leq y \leq 1$, C_{gs} is the gate-channel capacitance and $\overline{i_g^2}$ is given by Eq. (29). If V_g is the gate bias, $-V_d$ is the drain bias and V_{dif}, the diffusion potential (the charge carriers that have enough energy to surmount the potential barrier at the junction, and have a sufficiently of velocity directed across the potential barrier, constitute the forward current) of the gate-channel junction, then $W_s = V_g + V_{dif}$ at the source side of the gate contact, $W_d = V_g + V_{dif} - V_d$ at the drain side of the contact, and W_{oo} is the bias needed for channel cutoff. Also,

$$f_1(y,z) = (y-z) - 2/3(y^{3/2} - z^{3/2}) \tag{34}$$

$$f_2(y,z) = \frac{1}{2q_o aL} C_{gs} W_{oo} , \tag{35}$$

where q_o is the space charge density in the space charge region, 2a is the thickness of p-type layer and L is the length of the conducting channel as shown in Figure 26. Also required in (32) and (33) are

$$g_1(y,z) = p^2 g_2(y,z) - 2ph_2(y,z) + h_3(y,z) \tag{36}$$

$$g_2(y,z) = (y - z) - 4/3(y^{3/2} - z^{3/2}) + 1/2(y^2 - z^2) \tag{37}$$

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15. "Gate Noise in Field-effect Transistors at Moderately High Frequencies" Proc. IEEE, 51(1963) 461-467

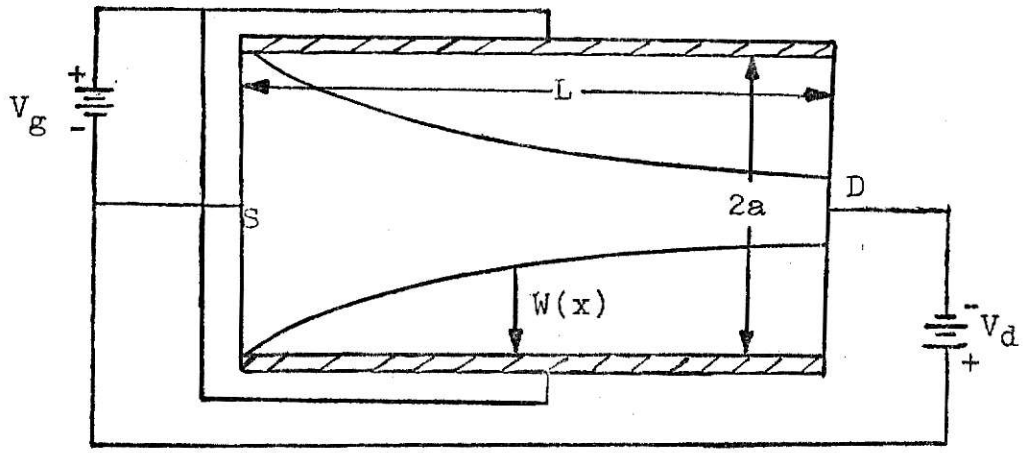

Figure 26. Cross section of an p-type FET conduction channel.

where,

$$p = \frac{1}{f_1(y, z)}\left[-1/3(y^{3/2} - z^{3/2}) + 1/6(y^2 - z^2) + (z - 2/3\, z^{3/2})(y^{1/2} - z^{1/2})\right] + y^{1/2} \quad (38)$$

$$h_2(y, z) = 2/3(y^{3/2} - z^{3/2}) - (y^2 - z^2) + 2/5(y^{5/2} - z^{5/2}) \quad (39)$$

$$h_3(y, z) = 1/2(y^2 - z^2) - 4/5(y^{5/2} - z^{5/2}) + 1/3(y^3 - z^3)\,. \quad (40)$$

Instead of representing the noise sources at positions in the small-signal equivalent circuits which are physically appropriate, it is often convenient for analytical work to consider a schematic representation of a device in which the noise generators have no direct physical significance.[16] Figure 27 illustrates this alternative representation of a noisy device. In the box of Figure (b) a similar equivalent circuit to that

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16. Rothe, E. I.R.E. Trans. ED-1, p.258 (1954)

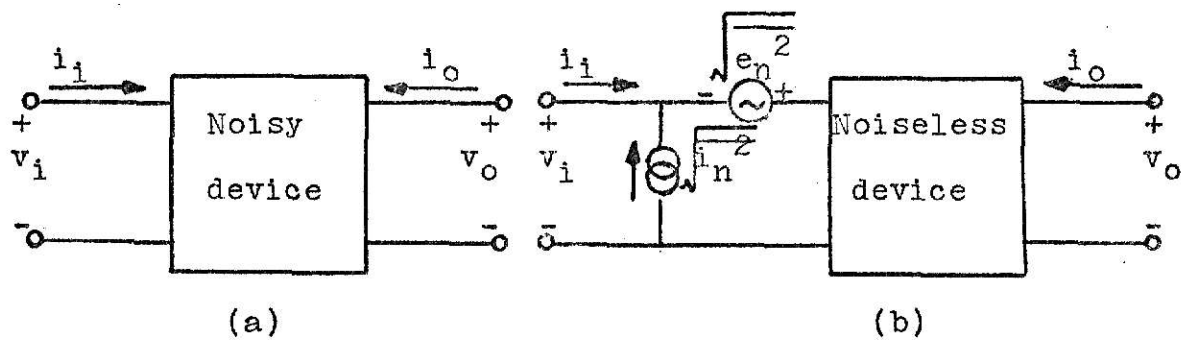

Figure 27. Schematic representation of a noisy device. (a) with regard to small-signal and noise current and voltages. (b) an alternative representation to that (a) in which the noise is completely represented by external noise generators.

postulated for Figure (a) may be found with the difference that it will contain no noise current or voltage generators. For an FET, because of the physical mechanisms, this alternative noise representation can be used quite satisfactorily, where

$$\overline{e_n^2} = \overline{i_d'^2}/g_{ms}^2 \tag{41}$$

and,

$$\overline{i_n^2} = \overline{i_g'^2} \quad . \tag{42}$$

There is a familiar way to express the noise performance, namely the noise figure[17], F. The noise figure of a two-port system is defined as:

$$F = \frac{S_i/N_i}{S_o/N_o} \quad , \tag{43}$$

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17. Friis, H. T. Proc. Inst. Radio Engrs. 32, p.419 (1944).

where S_i/N_i is the signal-to-noise power ratio at the input of the system and S_o/N_o is the signal-to-noise power ratio at the output. The equivalent definition of F is given by:

$$F = \frac{\text{Total noise power at the output}}{\text{Noise power at the output which is due to the source}}$$

Figure 28 shows a schematic representation of a noisy FET tuned amplifier, where $Y_s = g_s + jb_s$, the admittance of the signal source, and $\overline{i_s}$, the noise of the signal source with $\overline{i_s^2} = 4kTg_sB$. The values of $\overline{i_n^2}$ and $\overline{e_n^2}$ can be found from Equations (32), (42) and (33), (41) respectively:

$$\overline{i_n^2} = \overline{i_g^2} + \frac{4kTB}{g_{ms}} w^2 C_{gs}^2 \frac{g_1(y, z)(1 - z^{1/2})}{f_1^3(y, z) f_2^2(y, z)} \tag{44}$$

$$\overline{e_n^2} = \frac{4kTB}{g_{ms}} \frac{g_2(y, z)}{(1 - z^{1/2}) f_2(y, z)} \tag{45}$$

In order to calculate F, one can simply consider the net current flow in a short circuit between 1 and 1' at the input to the noiseless amplifier and then determine the ratio of the squares of the short-circuit current. In accordance with the definition, it is found that,

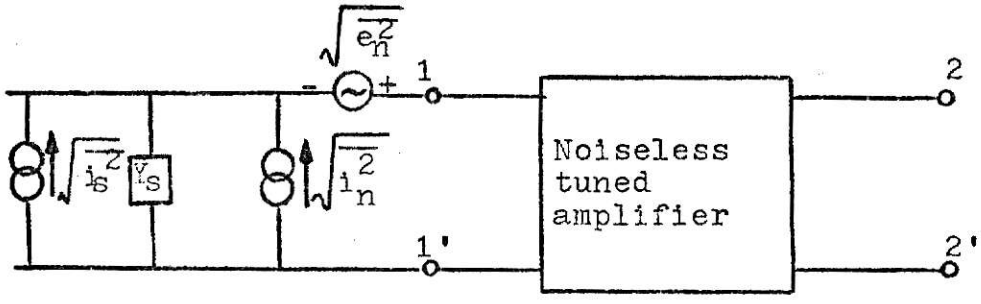

Figure 28. Schematic representation of a noisy FET tuned amplifier.

$$F = \frac{\overline{i_s i_s^*} + (\overline{i_n + e_n Y_s})(\overline{i_n + e_n Y_s})^*}{\overline{i_s i_s^*}}$$

$$= 1 + \frac{\overline{i_n i_n^*} + \overline{e_n e_n^*}\,(g_s^2 + b_s^2) + g_s(\overline{e_n^* i_n} + \overline{e_n i_n^*}) + Jb_s(\overline{e_n i_n^*} - \overline{e_n^* i_n})}{\overline{i_s i_s^*}} \qquad ----(46)$$

Clearly F depends on the real and imaginary parts of the signal source admittance and may be minimized if both are optimized to satisfy the relationship:

$$dF = \frac{\partial F}{\partial g_s} dg_s + \frac{\partial F}{\partial b_s} db_s = 0 \qquad (47)$$

The optimum values of g_s and b_s are found to be:

$$b_{opt} = \frac{j(\overline{e_n^* i_n} - \overline{e_n i_n^*})}{2\overline{e_n e_n^*}} \qquad (48)$$

and,

$$g_{opt} = -\frac{\overline{e_n^* i_n} + \overline{e_n i_n^*}}{2\overline{e_n e_n^*}}$$

$$= -\left[\frac{(\overline{e_n^* i_n} - \overline{e_n i_n^*})^2}{4(\overline{e_n e_n^*})^2} + \frac{\overline{i_n i_n^*}}{\overline{e_n e_n^*}}\right]^{1/2} \qquad (49)$$

the corresponding value of F_{min} is given by:

$$F_{min} = 1 + \frac{\overline{e_n^* i_n} + \overline{e_n i_n^*} + 2\left[(\overline{e_n^* i_n} - \overline{e_n i_n^*})^2/4 + \overline{i_n i_n^*}\,\overline{e_n e_n^*}\right]^{1/2}}{(\overline{i_s i_s^*})/g_s} \qquad (50)$$

where,

$$\overline{e_n e_n^*} = \overline{e_n^2} \quad , \quad \overline{i_n i_n^*} = \overline{i_n^2}$$

By using the relationship between Equation (44) and (45),

and letting

$$\frac{w^2 C_{gs}^2}{g_{ms}} \frac{g_1(y, z)(1 - z^{1/2})}{f_1^3(y, z) f_2^2(y, z)} = G_n$$

$$\frac{1}{g_{ms}} \frac{g_2(y, z)}{(1 - z^{1/2}) f_2(y, z)} = R_n \quad ,$$

then F_{min} becomes:

$$F_{min} = 1 + j\frac{2wC_{gs}}{g_{ms}} \frac{g_2(y, z)}{(1 - z^{1/2}) f_2(y, z)}$$

$$+2\left[\frac{g_2(y, z) g_1(y, z)}{f_1^3(y, z) f_2^3(y, z) g_{ms}^2} w^2 C_{gs}^2 + \frac{e(I_1 + I_2) g_2(y, z)}{2kTg_{ms}(1 - z^{1/2}) f_2(y, z)}\right.$$

$$\left. - \frac{b_{opt}^2 g_2^2(y, z)}{(1 - z^{1/2})^2 f_2^2(y, z) g_{ms}^2}\right]$$

$$= 1 + j2wC_{gs}R_n + 2R_n\left[\frac{G_n}{R_n} + \frac{e(I_1 + I_2)}{2kTR_n} - b_{opt}^2\right]^{1/2} \qquad (51)$$

The general expression for noise figure for any source admittance Y_s is

$$F = F_{min} + \frac{R_n}{g_s}\left|Y_s - Y_{opt}\right|^2 \quad , \qquad (52)$$

where $Y_{opt} = g_{opt} + jb_{opt}$.

The noise figure of a typical common-source amplifier as shown in Figure 20, is given in Figure 29.

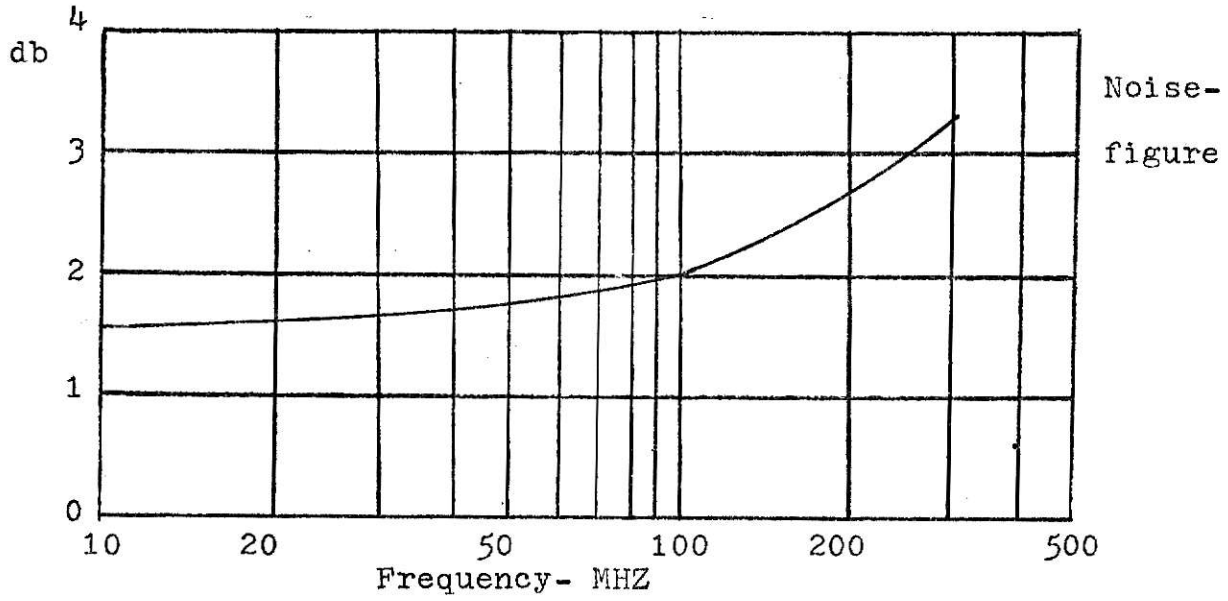

Figure 29. Noise figure versus frequency.

2. Mixers and Modulators

(2). Analysis in terms of FET characteristics

FET mixers operate much the same as vacuum tube types with injection of both local oscillator and input signal into the gate circuit. Because of the nonlinearity of the characteristic, the current through the device contains components at the intermediate frequency. By inserting a tuned circuit in the output lead, an output voltage of intermediate frequency is obtained.

Because the FET follows a square law almost perfectly, a minimum cross-modulation effect and less intermediate-frequency skewing (the output impedance of some mixers varies with changes in local oscillator signal to give i-f skewing) occurs in the circuit, as expected.

The mathematical expression for mixing can be developed in the following manner. From Eq. 4,

$$i_d = I_{dss}\left(1 - V_{GS}/V_p\right)^2$$

$$= I_{dss}/V_p^2\left(V_p^2 - 2V_{GS}V_p + V_{GS}^2\right) . \qquad (4')$$

If one applies both the input signal $v_i = V_i \cos w_i t$ and the local oscillator signal $v_s = V_s \cos w_s t$ with respective resonant angular frequencies w_i and w_s at the gate, then

$$V_{GS} = V_{GSO} + v_i \cos w_i t + v_s \cos w_s t , \qquad (53)$$

where V_{GSO} is the gate bias voltage. Substituting equation (53) in (4')

$$i_d = I_{dss} + \frac{I_{dss}}{V_p^2}\left[-2V_p(V_{GSO}+v_i\cos w_i t + v_s\cos w_s t) + V_{GSO}^2 \right.$$
$$\left. +2V_{GSO}(v_i\cos w_i t + v_s\cos w_s t)+(v_i\cos w_i t + v_s\cos w_s t)^2\right]$$
$$= I_{dss} + \frac{I_{dss}}{V_p^2}\left[V_{GSO}^2 - 2V_{GSO}V_p + 1/2\ (v_i^2 + v_s^2)\right]$$

(steady state drain current)

$$+ \frac{I_{dss}}{2V_p^2}(\ v_i^2\cos 2w_i t + v_s^2\cos 2w_s t\ )$$

(second harmonic terms)

$$+ v_i v_s \frac{I_{dss}}{V_p^2}\left[\cos(w_i + w_s)t + \cos(w_i - w_s)t\right] \qquad (54)$$

(sum and difference frequency terms).

Equation (54) consists of:

1. A dc component.
2. The second harmonics.
3. The sum frequency term and the difference frequency term.

Evidently, no higher harmonics are present in this equation.

For zero bias, i.e. $V_{GS} = 0$, equation (22) becomes,

$$di_d/dV_{GS} = g_{max} = -2I_{dss}/V_p = \text{constant}. \qquad (55)$$

This is the most important advantage of the FET over thermionic values and bipolar transistors with their nonlinear transconductances.

For the conditions with v_s much greater than v_i, $V_{GSO} = V_p$, and the difference frequency term becomes,

$$i_d = v_i v_s \frac{I_{dss}}{V_p^2} \cos(w_i - w_s)t, \tag{56}$$

while the instantaneous transconductance becomes

$$g_m' = di_d/dv_i = \frac{v_s I_{dss}}{V_p^2} \cos(w_i - w_s)t \ . \tag{57}$$

The average value of g_m', g_{mAV}', can be calculated by integrating over the half cosine wave (in this case $v_{s(peak)} = V_p$)

$$g_{mAV}' = \frac{1}{\pi} \int_{-\pi/2}^{\pi/2} \frac{I_{dss}}{V_p} \cos w_m t \, dw_m t$$

$$= \frac{2}{\pi} \frac{I_{dss}}{V_p} \ . \tag{58}$$

For the condition of equation (55), g_{mAV}' becomes

$$g_{mAV}' = \frac{1}{\pi} g_{max} \ . \tag{59}$$

In order to derive the full benefits of FET square-law behavior, the gate voltage excursion must be limited to a range over which the transconductance rises linearly with gate voltage. The maximum permissible voltage at the gate is given as[18]

$$V_{GS,max} = I_{d,max} I_{d,test} (2/g_{m,test}) \ , \tag{60}$$

where $g_{m,test}$ is the transconductance quoted by the manufacturer for a drain current $I_{d,test}$. If one assumes the input signals to be small, then the oscillator voltage may swing over the entire permissible gate voltage range. It has been established that the mixer transconductance g_m' is

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18. U. L. Rohde, "The FET at VHF" wireless world, Jan., 1966.

proportional to the voltage of the oscillator. This effect can be used for automatic gain control. By reducing the local oscillator signal the mixer gain can be reduced to zero. When v_s is small, v_i may occupy the entire range of the permissible gate voltage.

(b) Mixing noise

Noise in the mixing process depends on conversion loss because each decibel of this loss adds a decibel to the noise figure. The device achieves low noise when its transfer characteristic is most nearly square law. This occurs near the FET's pinch-off bias, where the drain current I_d is zero. Unfortunately, minimum drain current also results in minimum amplifier gain, since g_m increases as the drain current increases.

This dilemma, however, can be resolved by self-biasing the FET with a suitable source resistor, so that I_d is well below one ma, and then applying a large local oscillator signal to drive the FET on during the positive half cycles. In this way, an average I_d of 3 ma or more can be achieved. Noise is kept low, yet the effective g_m is sufficient to provide gain.

The theory of the noise figure of a mixer circuit is analogous to that of an amplifier circuit. The equivalent noise circuit of a mixer stage is shown in Figure 30, where R_a is the transformed antenna resistance, R_n is the tuned circuit impedance, and R_1 is the input resistance of the mixer circuit. Then $\sqrt{4kTB/R_a}$ is the noise current generator representing the

thermal noise of the antenna, the input noise current generator can be written as $\sqrt{2e(I_1+ I_2)B+ 4kTBG_n}$ [all these value I_1, I_2, and G_n were used in equation (51)], the current generator representing the thermal noise of the tuned circuit is $\sqrt{4kTB/R_n}$, and the mixer noise voltage generator is given by $\sqrt{4kTBR_{nc}}$.

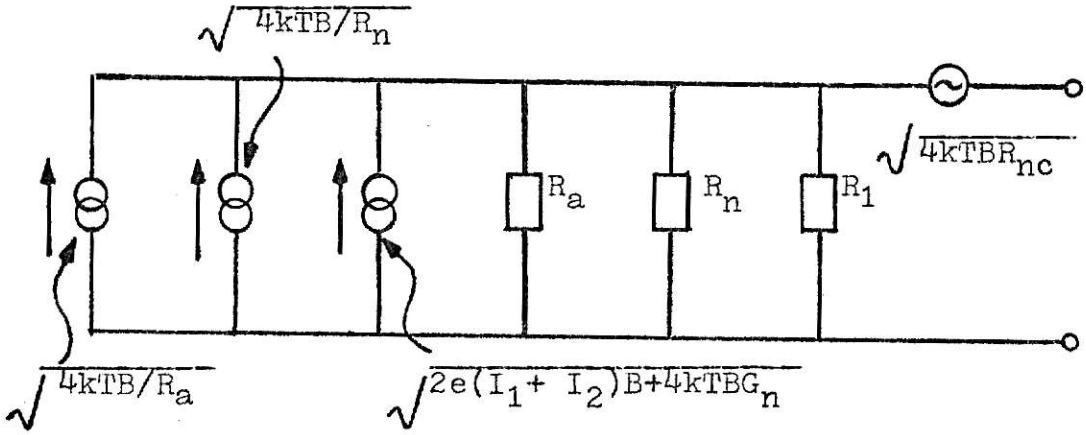

Figure 30. Equivalent noise circuit of an FET mixer.

It is sometimes more convenient to represent the input noise plus the thermal noise of R_n by a current generator $\sqrt{n4kTB/R_n}$. Obviously, n becomes

$$n = \frac{e}{2kT}(I_1+ I_2)R_n+ G_nR_n+ 1$$

$$= 20(I_1+I_2)R_n+ G_nR_n+ 1 \quad . \tag{61}$$

According to the equivalent circuit, the noise figure F is

$$F = 1+ nR_a/R_n+ R_{nc}R_a\left(1/R_a+ 1/R_n+ 1/R_1 \right)^2$$

$$=1+ 20(I_1+ I_2)R_a+ R_aG_n+ R_a/R_n$$

$$+ R_{nc}R_a\left(1/R_a+ 1/R_n+ 1/R_1 \right)^2 . \tag{62}$$

(c) Use as receiver converter

A converter can be constructed by using the mixer and a r-f amplifier. As mentioned before, the FET in r-f circuitry has very low cross modulation, especially when it operates as a common-gate amplifier (see page 29-30). Use of a common-gate amplifier before the mixer or receiver converter can reduce the reverse transfer admittance to a negligible value. The elimination of neutralization permits a wide-band input circuit and gives excellent bandpass characteristics coupled with ease and stability of alignment.

Figure 31[19] shows a typical circuit of a converter for use in the 144 MHZ amatuer band. The power gain of this converter is greater than 20 db with a noise figure of 2.5 db.

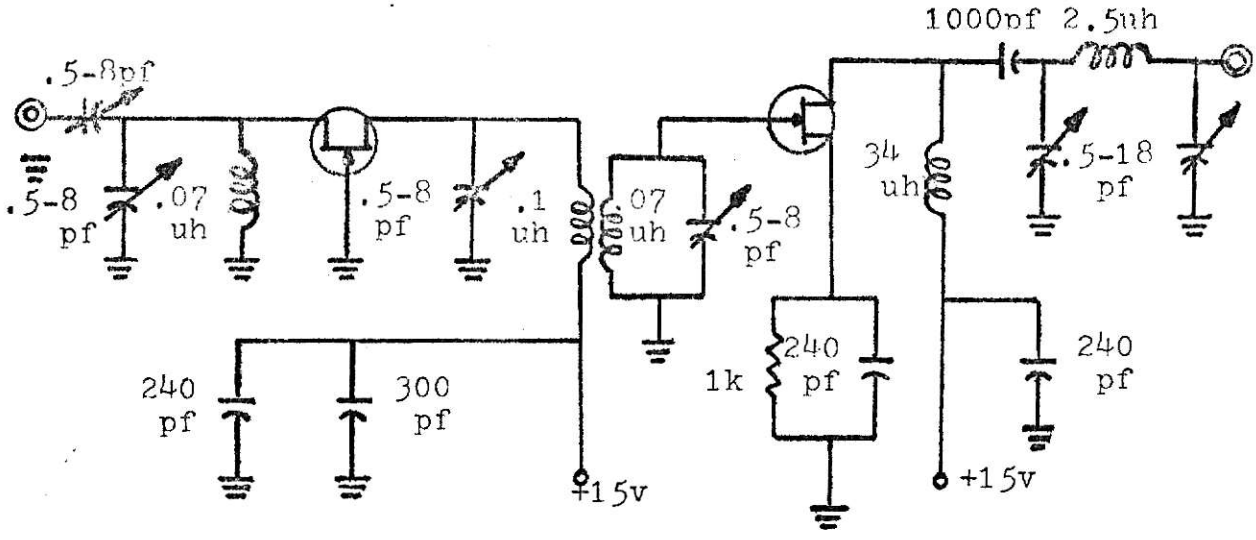

Figure 31. A typical converter circuit.

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19. J. B. Compton "Junction FET high frequency amplifiers" Wescon 1966 convention session 22/3.

(d) Use in single-side band (SSB)

Many modern transmitters, particularly in high frequency bands, use single-side band (SSB) techniques. Only one sideband is transmitted, together with a small "pilot" carrier (since complete suppression of carrier is not a practicable arrangement). This avoids the waste of power that would result when the carriers are transmitted at full strength, and also reduces the overall bandwidth with an improvement of the signal/noise ratio.

Balanced modulators are used in the generation of SSB phase modulated r-f carriers. The balabced mixer mixes an signal from the carrier generator with two out of phase signals from an audio frequency source. A more sophisticated way of looking at the phase-shift method of generating SSB is given by Figure 32.

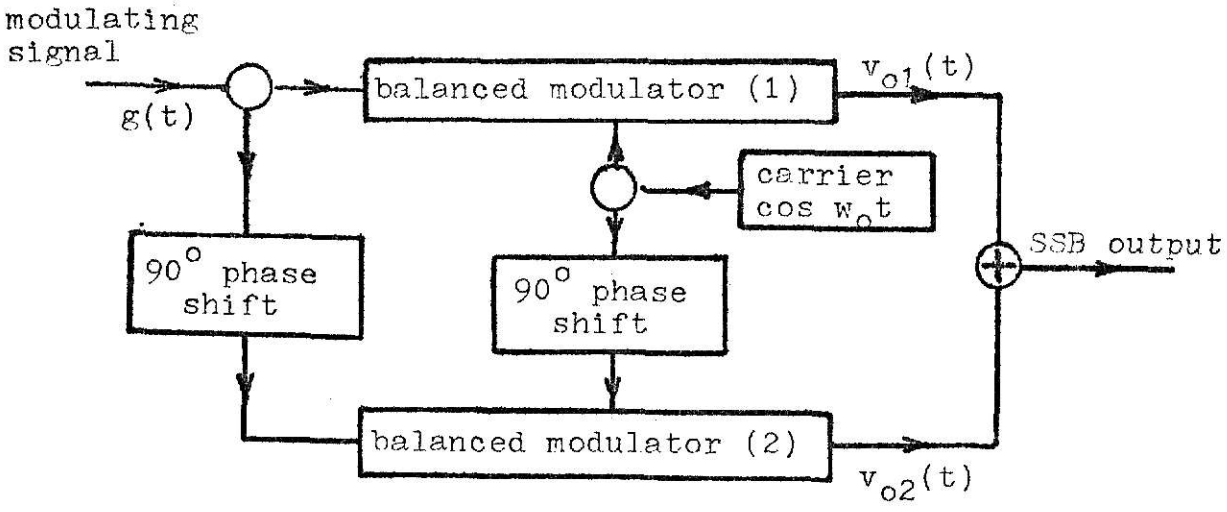

Figure 32. Phase shift method of generating SSB.

The mathematical approach is demonstrated in the following:

From equation (12), it is noted that,

$$i_d = I_{DP} + S_1 v_i + \frac{1}{2!} S_2 v_i^2 \qquad (63)$$

For balanced modulator (1), the inputs are,

$$v_1 = \cos w_o t + \sin w_n t \ ,$$

$$v_2 = \cos w_o t - \sin w_n t \ .$$

Omitting the constant bias, I_{DP}, the drain current i_{d1} of Q_1, and i_{d2} of Q_2 are given by,

$$i_{d1} = S_1(\cos w_o t + \sin w_n t) + \frac{1}{2!} S_2(\cos w_o t + \sin w_n t)^2 \ ,$$

$$i_{d2} = S_1(\cos w_o t - \sin w_n t) + \frac{1}{2!} S_2(\cos w_o t - \sin w_n t)^2 \ .$$

The output voltage is given by,

$$v_{o1}(t) = i_{d1}R - i_{d2}R$$

$$= 2S_1 R \sin w_n t + 2S_2 R \cos w_o t \sin w_n t \ . \qquad (64)$$

Since $\cos w_o t \sin w_n t = \frac{1}{2}\left[\sin(w_n + w_o)t + \sin(w_n - w_o)t\right]$,

$$\sin w_o t \cos w_n t = \frac{1}{2}\left[\sin(w_n + w_o)t - \sin(w_n - w_o)t\right] \ ,$$

a SSB signal of $\sin(w_n + w_o)t$ can be generated by letting balanced modulator (2) have an output voltage with the form,

$$v_{o2}(t) = 2S_1 R \cos w_n t + 2S_2 R \sin w_o t \cos w_n t \ ; \qquad (65)$$

the terms $2S_1 R \sin w_n t$ and $2S_1 R \cos w_n t$ can be filtered out by using a bandpass filter. A triode-type FET balanced modulator is shown in Figure 33. It should be noted that the modulating signal (audio frequency input) is applied to the gates in

push-pull through transformer T, and that the carrier (radio frequency) signal is applied to the sources in parallel through capacitor C_2. Cancellation of the carrier in the output circuit results from the symmetry of the circuit.

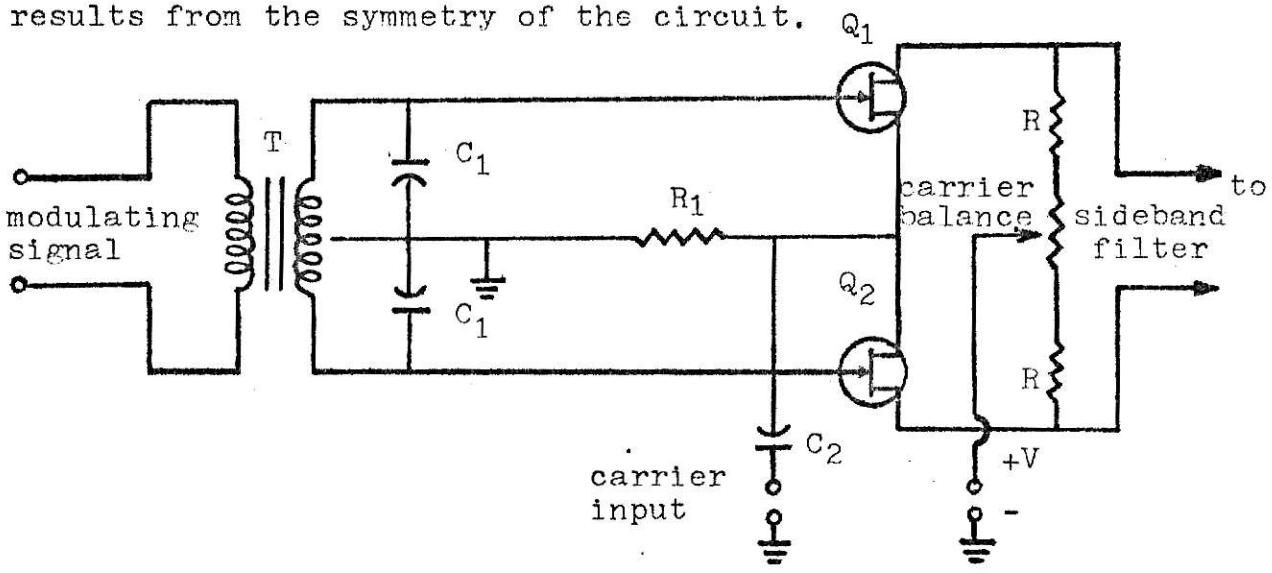

Figure 33. Balanced modulator

(e) Modulators (AM and FM)

In general, any waveform f(t) may be considered to be both an amplitude-modulated and an angle-modulated signal[20], such that

$$f(t) = A(t)\cos \phi(t). \tag{66}$$

If m(t) is a band-limited function such that $F[m(t)] = M(jw) = 0$ for $|w| \geq w_m$, then the signal,

$$f(t) = K\left[1 + m(t)\right] \cos w_o t\ , \tag{67}$$

is an ordinary amplitude-modulated signal, provided that $w_o \geq w_m$ and $|m(t)| \leq 1$. In above equations, the sinusoid $\cos w_o t$ is refered to as the "carrier", the frequency $f_o = w_o/2\pi$ is

20. Balth Van der pol. "The fundamental principles of FM" J. Inst. Elec. Enges,, Vol. 93, 1946.

called the "carrier frequency", and $f_m = w_m/2\pi$ is called the "modulating frequency". Comparison of Equation (66) with Equation (67) shows that in ordinary amplitude modulation $A(t) = K\left[1 + m(t)\right]$ and $\phi(t)=w_o t$. Since one defines $|m(t)| \leq 1$, it follows that for K positive $A(t) \geq 0$, and the function A(t) can be refered to as the modulation envelope.

The signal $f(t)= A_o \cos\left[w_o t + \phi(t)\right]$ is said to be an angle-modulated signal, since the angle of the cosine function $\phi(t)= w_o t + \phi(t)$ varies in accordance with $\phi(t)$, in addition to the linear variation of $w_o t$. If $\phi(t)$ is given as $k_f \int m(t)dt$, then the wave form,

$$f(t) = A_o \cos\left[w_o t + k_f \int m(t)dt\right] \quad , \tag{68}$$

is said to have frequency-modulation (FM).

In order to develop FM modulators, it is necessary to use equation (12) again,

$$i_d = I_{DP} + S_1 v_i + S_2 v_i^{2/2!} \quad . \tag{12}$$

By letting $v_i = V_1 \cos w_o t + Am(t)$,

then i_d becomes,

$$i_d = I_{DP} + S_1 V_1 \cos w_o t + S_1 Am(t) + \frac{1}{2} S_2 V_1^2 \cos^2 w_o t + \frac{1}{2} S_2 A^2 \left[m(t)\right]^2 + S_2 V_1 \cos w_o t \; Am(t) \quad . \tag{69}$$

Through using the identity,

$$V_1^2 \cos^2 w_o t = \frac{1}{2} V_1^2 + \frac{1}{2} V_1^2 \cos 2w_o t \quad ,$$

equation (69) can be defined as

$$i_d = i_o + i_1 + i_2 \quad ,$$

where

$$i_o = I_{DP} + S_1 Am(t) + \frac{1}{2} S_2 A^2 \left[m(t) \right]^2 + \frac{1}{4} S_2 V_1^2 \qquad (69a)$$

$$i_1 = V_1 \left[S_1 + S_2 Am(t) \right] \cos w_o t \qquad (69b)$$

$$i_3 = \frac{1}{4} S_2 V_1^2 \cos 2w_o t \ ;$$

it is also observed that

$$i_1(t) = V_1 S_1 + S_2 Am(t) \cos w_o t$$

$$= S_1 V_1 \left[1 + \frac{S_2 A}{S_1} m(t) \right] \cos w_o t \ .$$

Obviously, if $S_2A/S_1=+1$, then $i_1(t)$ is an ordinary amplitude-modulated signal, hence AM is produced.

Narrow-band FM can be generated by starting from equation (68) in exponential form,

$$\bar{f}_{FM}(t) = A_o e^{j\phi(t)}$$

$$= A_o e^{j\left[w_o t + k_f \int m(t)dt\right]}$$

$$= A_o e^{j\left[w_o t + \phi(t)\right]}, \qquad (70)$$

so that the real part of $\bar{f}_{FM}(t)$ can be written as,

$$f_{FM}(t) = A_o \cos\left[w_o t + k_f \int m(t)\, dt\right]$$

$$= \mathrm{Re}\left[\bar{f}_{FM}(t)\right]$$

$$= \mathrm{Re}\left[A_o e^{jw_o t} e^{j\phi(t)}\right]. \qquad (71)$$

Expanding $e^{j\phi(t)}$ in a power series gives,

$$f_{FM}(t) = \mathrm{Re}\left\{A_o e^{jw_o t}\left[1 + j\phi(t) - \frac{1}{2!}\phi^2(t) - j\frac{1}{3!}\phi^3(t) + \cdots\right]\right\}$$

$$= \mathrm{Re}\left\{A_o(\cos w_o t + j \sin w_o t)\left[1 + j\phi(t) - \frac{1}{2!}\phi^2(t) - \cdots\right]\right\} \qquad (72)$$

In the case of narrow-band FM, $|\phi|_{max} \ll 1$, so the exponential modulation is approximately linear, and equation (72) can be reduced to:

$$f_{FM}(t) = A_o \cos w_o t - A_o \phi(t) \sin w_o t$$

$$= A_o \cos \left[w_o t - A_o k_f \int m(t) dt \right]$$

$$= A_o \cos w_o t - A_o k_f g(t) \sin w_o t \ , \qquad (73)$$

where $k_f g(t) = \phi(t)$. Equation (73) contains two terms, the "carrier" and "side band", this, the so called narrow-band FM, is quite analogous with amplitude modulation. Figure 34 illustrates a method of generating FM signal.

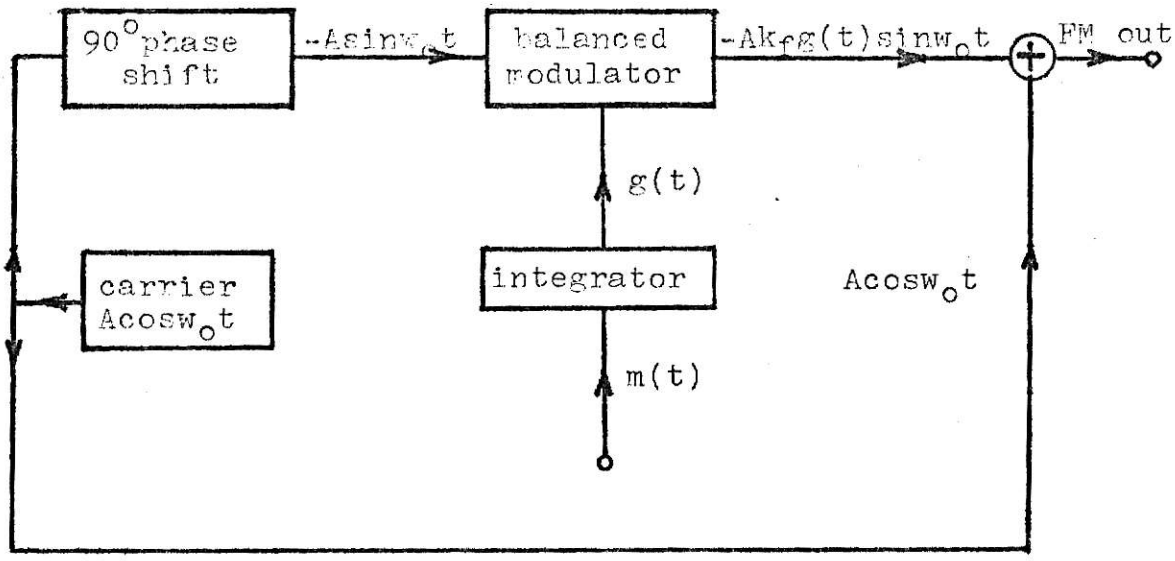

Figure 34. An example of FM signal generation.

IV. CONCLUSION

The high frequency performance of an FET is predictable from the geometry and tranconductance characteristics; it is quite similar to a vacuum tube (pentode).

A wide range of applications in FET circuits has been investigated. As this paper has pointed out, FETs have certain advantages in HF and VHF performance, such as high input impedance, low cross-modulation, low harmonic (second order) distortion and low noise figure. All of these are very important in r-f circuitry design. Furthermore, since the FET operates by controlling the flow of majority carriers, the problems encountered in the application of FETs are no more complex than those encountered with conventional bipolar transistors (which operate with minority carriers, and hence have a more complicated diffusion mechanism).

This paper is limited to the use of FETs as tuned amplifier and mixer circuits. Many other applications such as switching circuits and integrating circuits also play important roles in electronic industry. It is safe to say that as time goes by, more and more FET circuits will be used in engineering designs.

V. ACKNOWLEDGEMENTS

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THE USE OF FIELD-EFFECT TRANSISTORS AT HF AND VHF AS TUNED AMPLIFIERS AND MIXERS

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AN ABSTRACT OF A MASTER'S REPORT

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the requirements for the degree

MASTER OF SCIENCE

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1969

The purpose of this report is to analyze the field-effect transistor as HF and VHF tuned amplifiers and mixers. For completeness, the principle and characteristics of FETs are also introduced. From the FET's admittance parameters and equivalent circuit, there is no difficulty in finding the characteristics of an FET at high frequencies. The common-source FET is analogous to a common-cathode vacuum tube; the input impedance is very high. The common-gate FET is analogous to a grounded-grid vacuum tube with its low input impedance (compared with common-source). The common-drain FET has a high input impedance and low output impedance as does the cathode-follower.

It is noted that the FET has lower noise than that of bipolar transistors and vacuum tubes at frequencies ranging from 20 KHZ to 200 MHZ. The transfer characteristic follows a square-law almost perfectly--this keeps cross-modulation to a monimun and allows only second order harmonic distortion. These advantages place the FET as one of the most practical, necessary and efficient element in semiconductor r-f circuitry.

This report is limited to the use of FETs as amplifier and mixer circuits. Many other applications such as switching circuits and integrating circuits also play important roles in the electronic industry. It is safe to say that as time goes by, more and more FET circuits will be used in the engineering designs.