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I. Introduction

A common problem encountered in the design of portable, battery powered data acquisition or real time signal processing systems for field use is the high power consumption of the Analog to Digital Converter (ADC) and, in particular, the Sample and Hold (S&H). In higher speed applications involving sampling rates greater than a few kilohertz, power consumption can be reduced through careful selection of components, by using CMOS technology where possible, and by minimizing load currents. A large number of field systems, however, use much lower sampling rates. In these systems, other methods of reducing the power consumption are available in addition to those mentioned above. This paper will discuss two low speed, high resolution, minimal power systems designed for Sandia National Laboratories in Albuquerque, N.M. The first system was to be capable of performing a 12-bit bipolar conversion on each of two input channels sampled at 240 Hz. The phase difference between the two samples was to be kept to a minimum. In the second system, it was desired to expand the resolution of the ADC to 15-bits while reducing the sample rate to 128 Hz per channel. It was determined that the signal processing algorithms operating on the output of the systems, while requiring 12 or 15 bit sensitivity, did not require absolute accuracy in the conversions.

In order to accomplish these goals, two new techniques were applied to commercially available components. First, to reduce power consumption, low duty cycle "power switching",

that is, turning devices on and off as required, was employed on the higher power analog devices in the initial system. As a result the notion of "warm-up time" for integrated circuits had to be investigated. Second, to increase the resolution of the system, an iterative conversion technique which uses a "pre-conversion" to obtain a low resolution estimate of the input signal followed by a "post-conversion" to yield the necessary resolution, was applied to the second system. As a result, it is possible to obtain 12 to 15 bit resolution at low sample rates while consuming as little as 100 mW of power.

II. Overview

The systems designed consist of four major sections, as shown in Figure 1: 1) the microprocessor interface, 2) the control logic, 3) the S&H, and 4) the ADC. The interface to the microprocessor is the same on both systems, consisting of Tri-State latches used to store the results of the conversions, and since it consists only of discrete CMOS logic, the power consumption is negligible. The control logic for both systems consists of a counter used to generate the address for an EPROM, a CMOS EPROM containing the desired timing sequences, and some additional logic required to reset the counter or pause the sequence. The specifics of the controllers for each system will be discussed in more detail later. First, an overview of S&H's and ADC's will be presented.

A S&H is basically an analog memory device which stores a given input voltage until the ADC has finished performing its conversion. A typical S&H is shown in Figure 2. It consists of a unity gain input buffer to prevent the S&H from loading the source, an analog switch to select either the "sample" or "hold" mode, a high quality capacitor to store the input signal, and a unity gain output buffer to drive a load and to prevent the load impedance from affecting the stored voltage. A S&H is required in a system only if the input signal can change by more than $1/2$ LSB during the ADC's conversion time, which will depend on the ADC used and on the maximum slew rate of the input signal. Once it is determined that a S&H is required in a system, the selection of

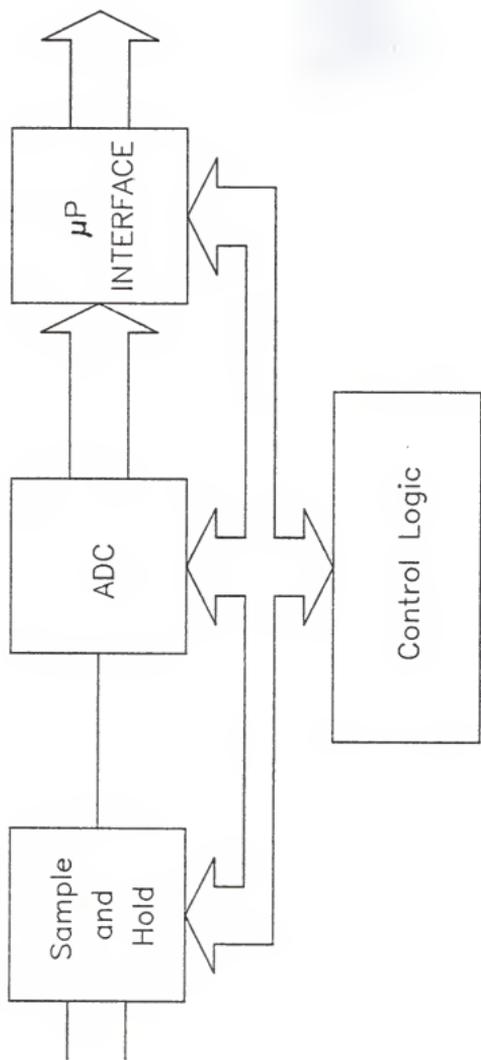


Figure 1. Typical System Block Diagram

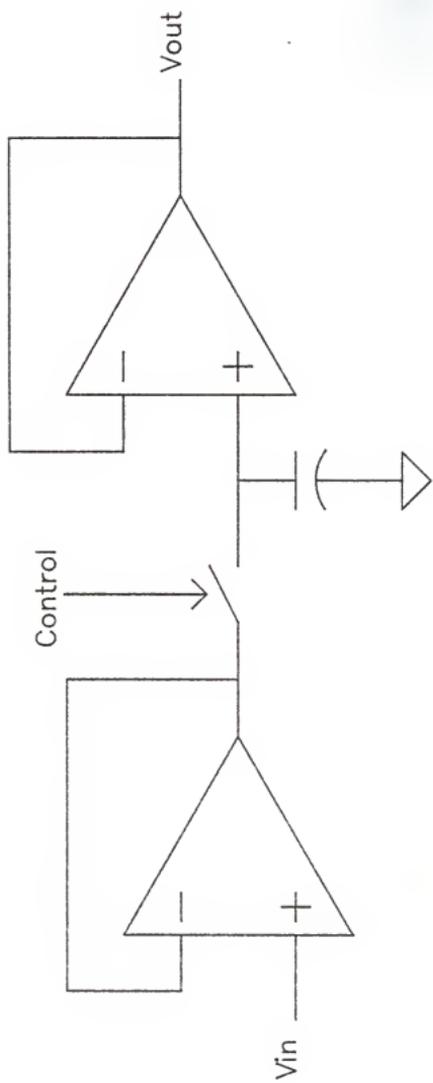


Figure 2. Typical Sample and Hold

the proper device is usually based on the following S&H characteristics: aperture time, aperture delay time, aperture uncertainty time, droop rate, acquisition time, and S&H amplifier slew rate. Although these parameters will be discussed here, a more detailed discussion is presented in [1].

There is a great deal of debate as to the importance of aperture time and aperture delay time in a sampled data system. Aperture time is defined as the time required for the switch to change state following the hold command. Aperture delay time is the time delay from the midpoint of the sample to hold command and the midpoint on the impedance curve of the switch as it changes states [1]. Aperture times are presented graphically in Figure 3. It is presented in [2] that the above aperture times must be minimized in a system in order to obtain a specified accuracy because of the fact that the input signal is changing during these delays. Actually, if the output of a sampled data system is represented as a series of impulse functions, each indicating a given sample value, the net effect of the aperture time and aperture delay time is to shift the samples in time by a constant, measurable amount, as shown in Figure 4. If absolute accuracy is required in a system, the effect of these delays can be compensated for by advancing the control timing by the appropriate amount. However, in a system in which the ADC output is used by a signal processing algorithm, aperture time has no significant effects, beyond that of delaying the signal, and generally can be ignored. The third aperture time mentioned

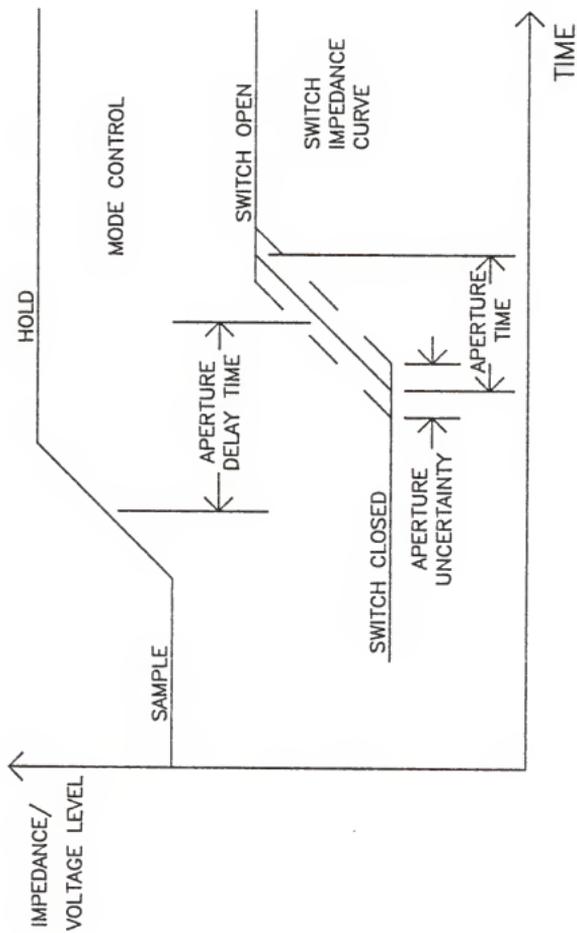


Figure 3. Aperture Times for Sample and Hold [1]

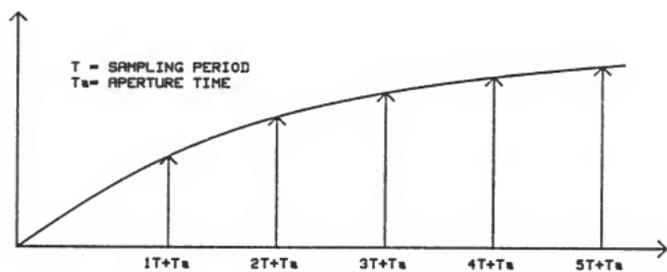
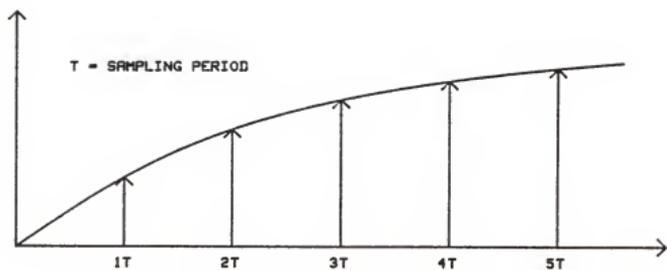


Figure 4. Effect of Aperture Time on Sampling

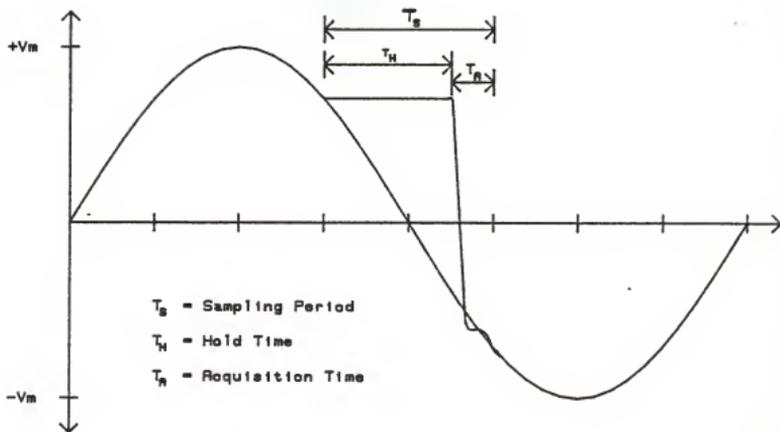
above, aperture uncertainty time or aperture jitter, is a lumped parameter encompassing the variations in both aperture time and aperture delay time caused by the uncertainty of the switch. As a result, the samples are not necessarily equally spaced in time. This has the effect of modulating the frequency spectra of the sampled data slightly, but since aperture uncertainty time is usually on the order of 1 to 10 ns, the effect on systems with low sample rates is negligible. Thus in the systems discussed in this paper, aperture time is not a consideration.

The next S&H characteristic which must be considered in designing a system is the Droop Rate of the S&H. Droop rate is the output drift, expressed in V/s, of the S&H amplifier when it is in the "hold" mode. The rate of output drift is a function of the hold capacitor value and results from switch leakage, capacitor leakage, and op-amp input bias currents. For a given S&H, the hold capacitor value must be made large enough to prevent the output drift of the S&H from exceeding 1/2 LSB during the ADC's conversion time. However, increasing the value of the hold capacitor beyond a certain point, which is device dependent, can reduce the slew rate and increase the acquisition time of the S&H, thus limiting the band of frequencies which can effectively be sampled with the device. Therefore, when determining the value of hold capacitor to use, the slew rate and acquisition time requirements must first be determined.

The final two parameters to be discussed are acquisition time and slew rate. Acquisition time is defined as the length of time between the sample command and the point at which the output

is tracking the input to a specified accuracy, usually 0.1% or 0.01% of full scale. The slew rate is the maximum rate of change of the input voltage which can be tracked by the S&H. Since acquisition time and slew rate are inversely related, both must be considered together when selecting a S&H to use for a specific application. The minimum slew rate or maximum acquisition time permissible for the S&H in a system is determined by the required hold time (or ADC conversion time), the sampling period, and the maximum full scale deflection of a sine wave of the highest frequency of interest in the input signal. This is illustrated in Figure 5. In a band limited system, the maximum slew rate occurs at the zero crossings of a full scale peak-to-peak sine wave at the maximum frequency of interest and is given by $2\pi f_{\max} V_m$. Since the required "hold" time is determined by the ADC chosen, the maximum permissible acquisition time for the S&H will be given by the difference between the sampling period and the "hold" time. The minimum slew rate required for correct operation of the S&H will be given by the change in voltage about the zero crossing during the acquisition time which is equal to the maximum slew rate of the input signal multiplied by the ratio T_S/T_A . Using the values given above for maximum S&H acquisition time and minimum amplifier slew rate, combined with the acceptable droop rate computed from the resolution and conversion time of the ADC, the correct S&H and required hold capacitor for a given single channel system can be determined.

However, in multi-channel systems where a single S&H is



Maximum Slew Rate of Signal = $2\pi f_{\text{MAX}} V_m$

Maximum T_A Allowed = $T_S - T_H$

Minimum Slew Rate Required = $V/T_A = 2\pi f_{\text{MAX}} V_m T_S / T_A$

Figure 5. Computation of S&H Acquisition Time and Amplifier Slew Rate Requirements

being used to sample multiplexed inputs, the above analysis does not apply because the S&H will require a higher slew rate than that of the input signal since the S&H input is switching between inputs which could be at opposite rails. In this situation, acquisition time becomes the dominant design consideration in determining which S&H to use. In this case, the maximum permissible acquisition time will be given by the difference between the sampling rate per channel divided by the number of channels, and the "hold" time required by the ADC (assuming each channel is sampled at the same rate). The maximum droop which can be permitted in such a system will be computed in the same way as discussed above, however, the slew rate used in determining the hold capacitor value will be computed from a full scale voltage change occurring during the acquisition time. Another situation in which the maximum permissible acquisition time of the S&H is the dominant factor and must be reduced even further is when the phase difference between the samples from each input channel must be minimized. In this situation, two options exist. First, a single S&H can be used and the acquisition time can be computed from the maximum acceptable phase error, or secondly, multiple S&H's can be used and the design parameters can be determined by treating each S&H as if it were in a single channel system. The main difference between these approaches is that of power consumption.

The power consumption of a S&H is directly related to the amplifier's slew rate, and thus inversely related to the S&H's acquisition time. The first option presented above would require

a S&H with a much higher slew rate than each individual S&H's in the second option. In order to break even or improve the power consumption of a multi-channel system by using the first option, there would need to be in excess of 5 to 10 input channels in the system, depending on the selection of lower power S&H's used to implement the second option. However, this is the case only if the S&H's are continuously powered. In the case where power switching is used, the first option has several distinct advantages which will become evident when the effects of "power switching" are discussed.

The final section of the analog to digital conversion system to be discussed is the ADC itself. In determining which ADC to use in a specific application, the first decision to be made is which conversion scheme to use. The most common analog to digital conversion schemes implemented in monolithic or hybrid devices are Flash converters, Successive Approximation ADC's, and Integrating ADC's, although other methods exist. A detailed discussion of analog to digital conversion appears in [3]. The decision as to which method to use is based on four considerations; conversion speed, accuracy or resolution, power consumption, and cost. Flash ADC's are the fastest, with typical conversion times of 20 ns to 150 ns, but with the high speed comes increased power consumption. Also, since an n-bit flash converter requires 2^n comparators, the resolution of flash converters is limited to 7 or 8 bits. One method of achieving higher resolution in a flash converter without an exponential

increase in the number of comparators is to use a two stage parallel converter as shown in Figure 6. As shown, an 8-bit flash converter can be obtained by using two 4-bit stages. The results of the first four bit conversion are converted back to an analog voltage and subtracted from the input signal. The difference signal is then converted by the second 4-bit flash ADC, and the results are accumulated in an 8-bit register [4]. Actually, this method can be applied to increase the resolution of other types of ADC's, and will be discussed later. The cost of a flash ADC is also a limiting factor in the design of a system, since the price of an 8-bit flash ADC can range from \$100 to \$1000. Successive approximation ADC's are slower than flash ADC's, with typical conversion times of 1 μ s to 1 ms, depending on the resolution and clock rate. They are in a medium price range of \$20 to \$200 and are typically available with 12 to 14 bit resolution. Although successive approximation ADC's offer relatively high speed and resolution at a reasonable cost, they do suffer from potential missing code errors. The power consumption of successive approximation ADC's depends upon the fabrication technology used and the conversion speed, and ranges from roughly 10 mW to several watts. Integrating ADC's are the slowest with conversion speeds of 1 ms to 300 ms or more, and are available with as much as 18-bit resolution. They are the lowest priced, and in the case of a dual-slope integrating ADC, the most accurate. They have excellent noise immunity and, unlike the successive approximation type of ADC, do not suffer from missing code errors. However, the long conversion times, or prohibitively high clock rates required

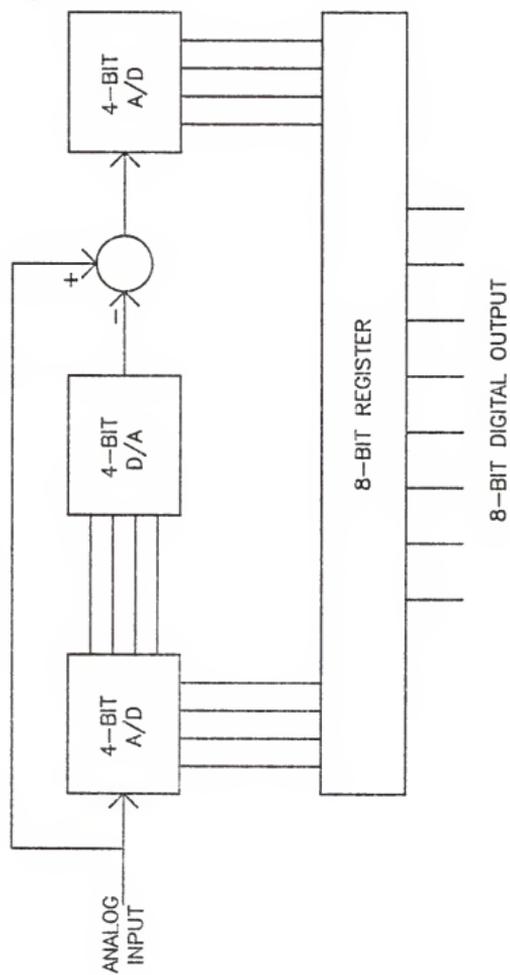


Figure 6. Two-Stage Flash ADC

to reduce the conversion time, associated with integrating ADC's, eliminate them from consideration in many applications. This is especially true if high resolution is required.

Once the type of converter is determined, individual ADC's may be compared using a variety of criteria which are discussed in [5]. It should be noted at this point that ADC errors that would be fatal to a recording type data acquisition system in which absolute accuracy is required will have little or no effect in a signal processing environment where only relative accuracy is needed. Absolute accuracy is determined by the degree of correspondence between the actual device input-output characteristics and the ideal characteristics. Relative accuracy is determined by the linearity of the input-output characteristic and is unaffected by gain or offset errors. The distinction between absolute and relative accuracy is shown in Figure 7. Offset error, the degree to which the output characteristic fails to pass through the origin, can sometimes be ignored, depending on the application, or can easily be corrected using the following method. Ground the input to the system and perform a conversion. This conversion yields the value of the offset error, which can be stored in memory and subtracted from all subsequent readings to yield the corrected values. Gain error, the difference between the slope of the actual and ideal ADC output, can almost always be ignored, or if necessary, can be corrected in a manner similar to that used to compensate for the offset error. To correct the gain error, a second conversion is

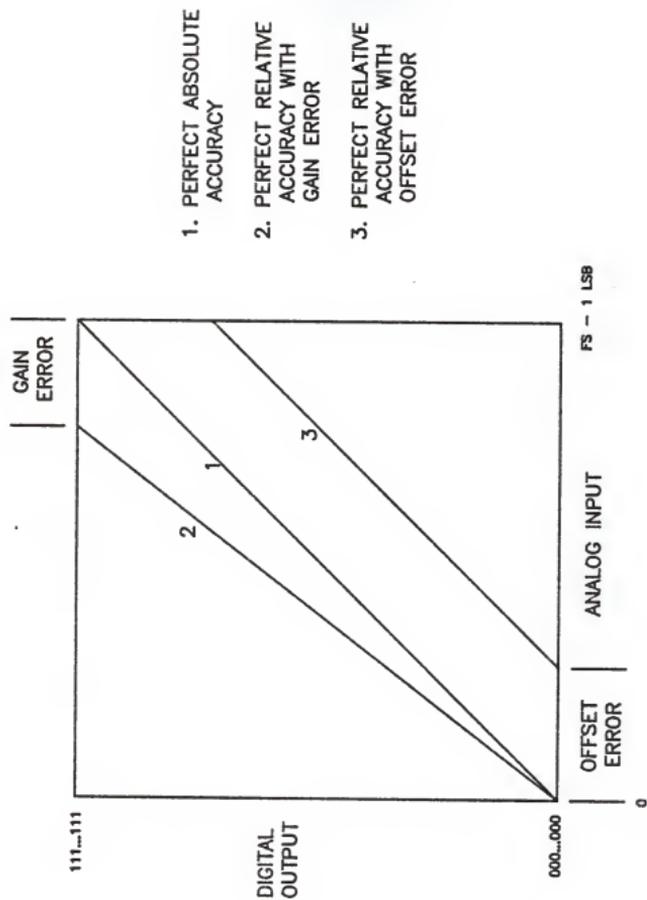


Figure 7. ADC Accuracy, Gain and Offset Errors [5]

performed with a known input voltage of 50% to 75% of full-scale. This, combined with the value used to correct for the offset error, can be used to determine the slope of the ADC output characteristic. The slope can then be used to compute the scale factor required to correct the output. The addition and multiplication operations required for these corrections can be performed by the microprocessor which is running the signal processing algorithm. The same processor can also perform the required switch closures to determine the values to be used in the error correction process. In the systems designed for Sandia Laboratories, these errors had no effect on the signal processing algorithms and were, for all practical purposes, ignored.

The main parameter affecting the relative accuracy or linearity is the differential nonlinearity, which determines whether an ADC is monotonic or has any missing code errors. Differential nonlinearity is defined as the maximum deviation of any bit size from the theoretical value of 1 LSB over the entire conversion range [5]. If the differential nonlinearity is zero, as in the ideal case, then each bit size is equal to 1 LSB and the ADC is perfectly linear. A differential nonlinearity of +1 LSB or greater will result in missing code errors, while a differential nonlinearity of -1 LSB or greater will result in non-monotonic operation. Some of the errors due to variations in differential nonlinearity are shown in Figure 8 and should be considered when determining which ADC to use.

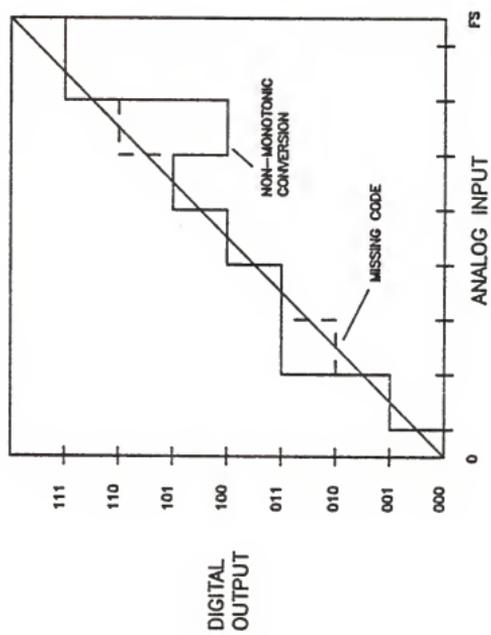


Figure 8. Errors Due to Differential Nonlinearity [5]

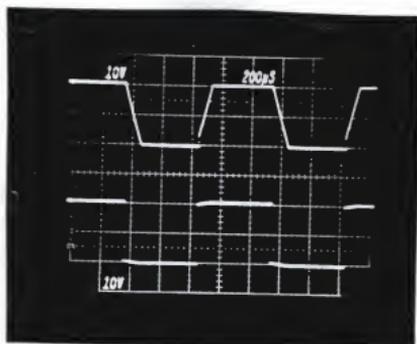
III. Power Switching

Switching the power to a device on and off as required is not a unique concept. Devices already exist on the market which go into a quiescent mode when not in use, consuming only a few hundred microwatts of power. Power switching devices which are not internally designed for such use, however, introduces several problems for the designer. First, a low power method of switching the device must be determined or the advantages of power switching are lost. Secondly, all of the inputs to the device must be disconnected before the power is switched off in order to prevent damaging the device. Also, substantial noise can be introduced on the analog signal and ground lines by the switching action, so the effect of this noise on the other parts of the system must be determined and steps taken to eliminate it if necessary. Finally, the "warm-up" time for each switched device must be measured and included in the "on" time.

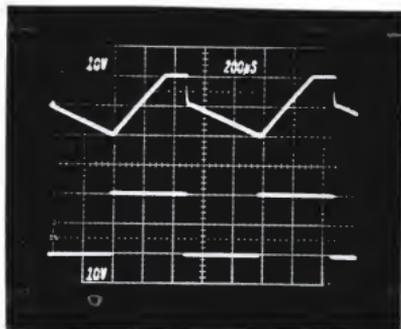
The method used in switching the power to a device on and off depends on the supply current the device requires and on the switching frequency. Original efforts used BJT's, but the control voltages were not easily generated and the circuitry consumed too much power. The second approach used opto-couplers to do the switching. This corrected the control voltage problem, but the opto-couplers ended up consuming more power than the device being switched. The final solution to the problem was to use overvoltage protected analog switches, such as the Siliconix DG211CJ, to do the power switching. The DG211 is a quad CMOS SPST

analog switch which consumes 20 mW of power per package. Each switch is capable of handling 20 mA of current continuously, and up to 70 mA peak. The DG211 also uses standard 0 to 5V CMOS logic levels, so interfacing to the control logic is not a problem. The DG211 can also be used to switch the inputs to a device into a high impedance state while the power is off, thus protecting the switched device from damage. Also, since the DG211 has a low "on" resistance and was designed for low transient switching, such as that required for a S&H, the switching action will introduce a minimal amount of noise into the system.

The "warm-up" time for a system is loosely defined as the amount of time from power-up to the point where the device can be effectively used to perform its function, to some specified accuracy, which is determined by the requirements of the system. The warm-up times for several op-amps were measured in an effort to establish a relationship between warm-up time and amplifier slew rate. When performing these tests, the input to the op-amp was connected to a -10 V source. A negative input voltage was used because the slew rate for a negative signal is typically less than or equal to the slew rate for a positive signal and thus would yield the worst case warm-up time. This phenomenon is illustrated in Figure 9. The bottom trace shows a 20 volt peak-to-peak input signal applied to the op-amps in a unity gain configuration, with a 10k ohm load. The top trace shows the output waveform of the op-amp. The results obtained using a PMI OP-07 show that the positive and negative slew rates are nearly



(a)



(b)

Figure 9. Slew Rate Measurements for (a) OP-07 and (b) OP-20

equal, with the negative slew rate being slightly slower. The results for a PMI OP-20 show a dramatic difference in the two slew rates, with the positive slew rate being 1.5 times faster than the negative slew rate. This phenomenon would cause a significant error in the measured values of warm-up time if not taken into consideration.

The circuit used to measure warm-up time is shown in Figure 10. The amplifier under test was connected in a unity gain configuration with a 10k ohm load. The power switching was performed using Siliconix DG211 switches, which were also used to switch the input signal in conjunction with the supply voltages to the device. The input and output of the op-amp were connected to the differential input of an oscilloscope. The control signal to the switch was also monitored on the oscilloscope. Representative samples of the results obtained are shown in Figure 11. The warm-up time was taken to be the amount of time for the error signal, given by the difference between the input and output voltages, to stabilize at or near zero volts. As can be seen in the photographs, the OP-07, which has a typical slew rate of $0.3 \text{ V}/\mu\text{s}$, took $50 \mu\text{s}$ to stabilize, while the OP-01, which has a higher typical slew rate of $18 \text{ V}/\mu\text{s}$, took $12 \mu\text{s}$. These results imply that the warm-up time for a device is directly related to the slew rate of the amplifiers making up the device. In general this comparison is valid, however there are other factors involved, the most important of which is the internal design of the amplifier. A more detailed summary of the results of the warm-up time tests are shown in Figure 12.

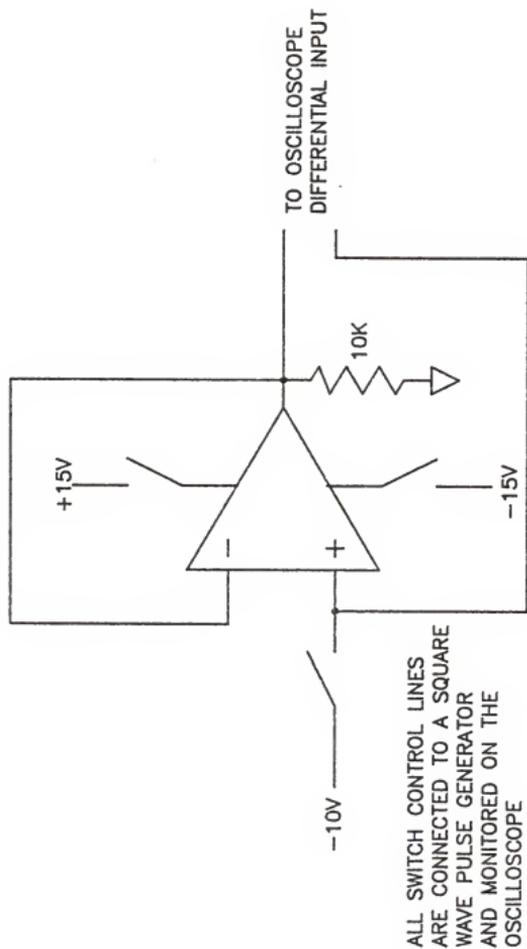
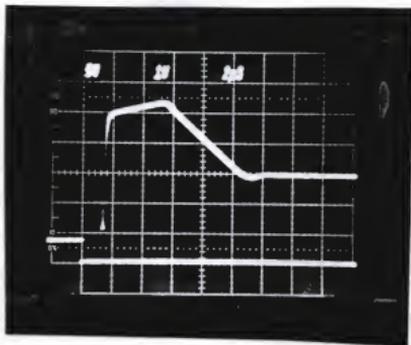
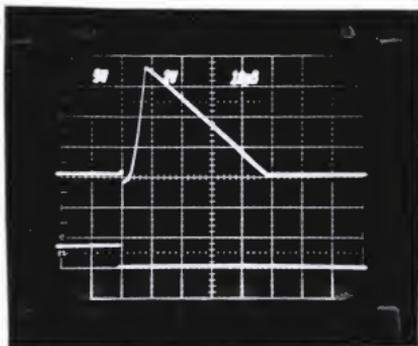


Figure 10. Op-amp Warm-up Time Test Circuit



(a)



(b)

Figure 11. Warm-up Time Measurements for (a) OP-01 and (b) OP-07

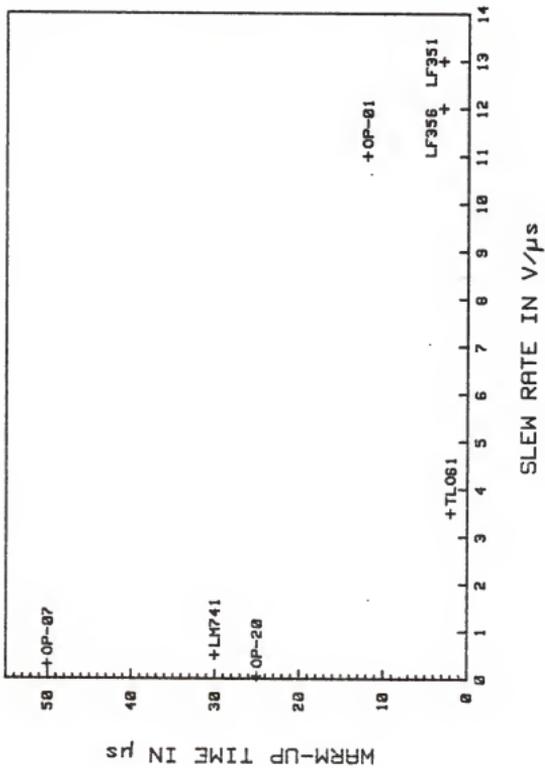


Figure 12. Op-amp Warm-up Time Test Results

The power switching of analog devices realizes the greatest advantage when applied to devices having short warm-up times. This allows the designer to use fast, high performance devices in place of low power devices which are often too slow for a given application, and also minimizes the "on" time in a system, providing a greater reduction in the power consumption. In the case of the 12-bit system designed for Sandia Laboratories, a S&H with a short acquisition time was required in order to minimize the phase difference between the samples obtained from each channel. The Analog Devices AD583 IC S&H was chosen because of its low acquisition time (4 μ s) and high slew rate (5 V/ μ s). However, according to the data sheet, the power consumption of the AD583 is in the 75 mW to 150 mW range. Thus it was decided to attempt to power switch the device and measure the amount of degradation in its response.

First, the circuit shown in Figure 13 was built and used to measure the warm-up time and the power consumption of the switched system. With the DG211 control inputs grounded (switches closed), the supply currents through the 10 ohm sense resistors were measured to be 6.16 mA @ +15V and 2.32 mA @ -15V, corresponding to a power dissipation of 127.2 mW. In order to determine the power consumption of the switched system, the voltage across the 10 ohm sense resistors was monitored using the differential input on an oscilloscope. The results for the positive supply to the device are shown in Figure 14. Figure 14a shows the switch control signal (lower trace) and the voltage

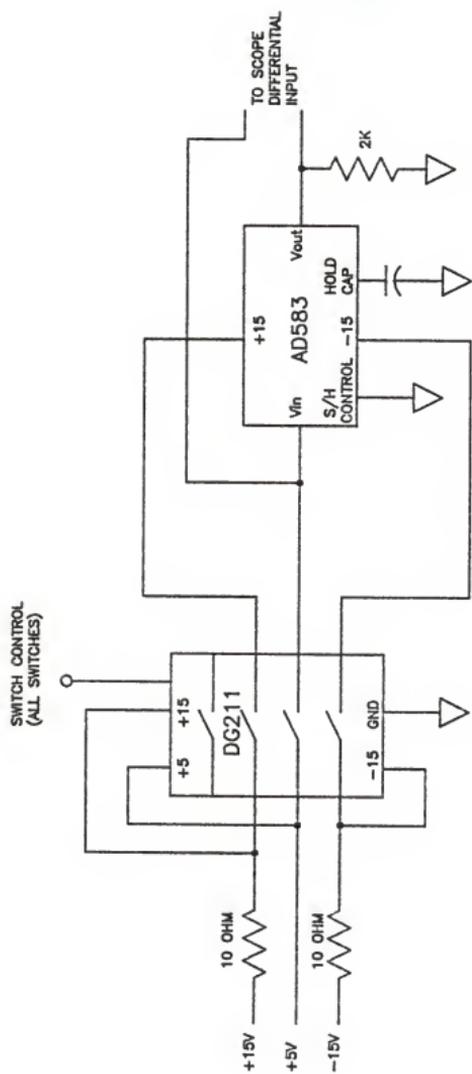
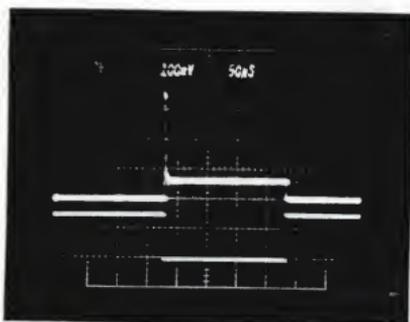
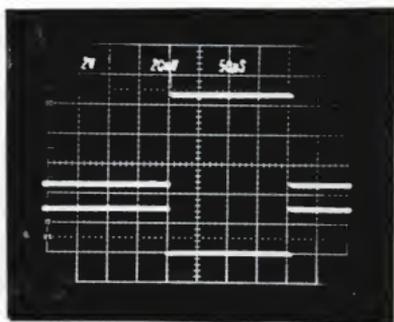


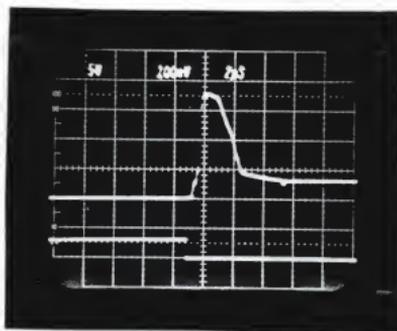
Figure 13. AD583 Test Circuit



(a)



(b)

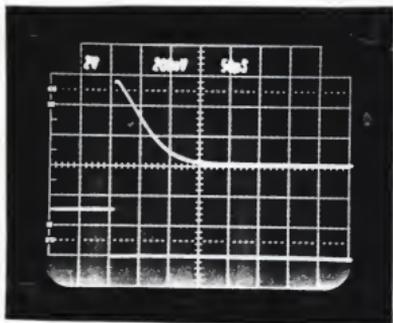


(c)

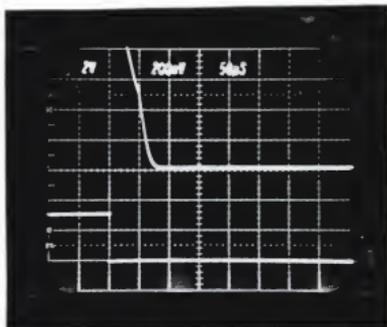
Figure 14. Current in Positive Supply of Switched AD583

across the positive supply line sense resistor (upper trace). Notice that there is a brief, 36 mA pulse when the switch closes, followed by a constant dc current. Figure 14b is a blow-up of the waveform and shows a current through the resistor of approximately 6.6 mA when the AD583 is turned on, and a current of roughly .6 mA due to the analog switch when the AD583 is turned off. Figure 14c shows that the 36 mA turn on spike has a duration of only 3 μ s. Similar results were obtained using the sense resistor in the negative supply lead. As a result, if the turn-on spike is neglected, the power dissipation of the switched device is equivalent to its continuous power dissipation multiplied by the fraction of time that the device is on in one cycle. Such an estimation is quite accurate, especially if the duration of the turn-on spike is very short in comparison to the switching period. Naturally, as in the continuous operation case, the power consumption of the switched device will depend on the output load impedance, input voltage, etc.

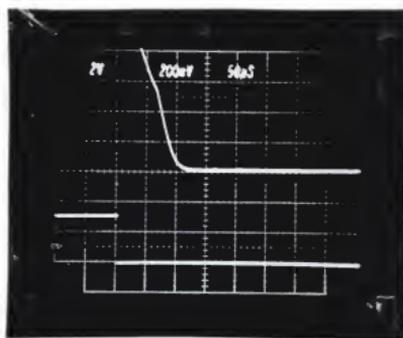
Now that the feasibility of power switching the AD583 had been demonstrated, the final parameter to be measured was the warm-up time necessary for accurate operation. Using the same circuit as shown in Figure 13 except with a -10 V input, the warm-up time was measured in a manner similar to that used for the op-amps mentioned above. However, in this case, it was realized that the warm-up time would be a function of the value of hold capacitor used, so measurements were made with an increasing series of capacitor values. These results are shown in Figure 15. Again, the bottom trace shows the switch control



(a)



(b)



(c)

Figure 15. Warm-up Time Measurements for AD583 with (a) $0.033 \mu\text{F}$
 (b) $0.0047 \mu\text{F}$ and (c) $0.01 \mu\text{F}$ Hold Capacitors

signal and the top trace shows the input-output error signal. For a holding capacitance of $.0047 \mu\text{F}$, a warm up time of $90 \mu\text{s}$ is required. Capacitor values of $.01 \mu\text{F}$ and $.033 \mu\text{F}$ show warm-up times of $130 \mu\text{s}$ and $180 \mu\text{s}$, respectively. Obviously this result is not unexpected, since the hold capacitor acts as a load on the output of the first op-amp in the S&H and would act to dampen or slow the response of the amplifier.

The final step was to measure the overall effect of power switching the S&H in the system. This will be discussed in the next section.

IV. Design and Testing of the 12-bit System

Since the requirements for the operation of the power switched S&H were known, the next step was to determine which ADC to use. It was decided that the Datel-Intersil ADC-HC12B 12-bit successive approximation ADC be used for the following reasons. First, the ADC-HC12B can be operated from a single positive supply voltage. Second, the ADC-HC12B is a complete ADC requiring only a few external resistors for offset and gain adjustments. Third, and most importantly, the ADC-HC12B is hybrid integrated circuit fabricated using CMOS technology, noted for very low power consumption, which includes a built-in interrupt power mode which results in even lower power dissipation. The interrupt power mode functions in the following manner. With the END-OF-CONVERSION (EOC) pin tied to the POWER MODE pin on the device, when the START CONVERSION command is received, EOC goes high causing the internal analog circuitry to be energized. After 50 μ s the circuitry stabilizes and the conversion begins. At the end of the conversion, 350 μ s later, EOC goes low, returning the analog circuitry to its quiescent state. The resulting power dissipation at a conversion rate of 480 conversions per second (240 conversions per second on two channels) is approximately 30 mW.

The disadvantage of such a long conversion time is that the S&H would have to be on for 800 μ s (two conversions) plus a warm-up time and a second acquisition time, or approximately 950 μ s. Also, using the S&H in this fashion eliminates the benefit gained

from having a fast acquisition time to reduce the phase error between the samples from the two channels. To correct this situation, the AD583 was used in conjunction with two low speed "slave" S&H's constructed using OP-20's, as shown in Figure 16. Using this configuration, the AD583 can be turned on, allowed to warm-up, take two fast samples and transfer them to the slave S&H's, and then turned off. The slave S&H's, which are continuously powered, use only 5.5 mW of power. The slave S&H's, however, are very slow to respond due to the low slew rate of the OP-20's. As a result, a delay of 200 μ s between the time that the sample from the first channel is stored on the hold capacitor of the slave S&H and the start of the first conversion must be included in the system timing. Also, since the second slave S&H has to hold its sample for a period equaling two ADC conversion times, the hold capacitor on the second slave must be increased to compensate for the droop.

The dual S&H configuration was tested and it was determined that it was operating as expected. It was realized, however, that the AD583 was being turned off with as much as 10V on the hold capacitor, and that the hold capacitor was discharging through the unpowered device. Since it was uncertain as to the effect this would have on the AD583, the situation was corrected by including a third switch on the input to the S&H which was connected to the analog ground. After transferring the two samples to the slave S&H's, the AD583 was placed in the "sample" mode with the input grounded, thus allowing the hold capacitor to

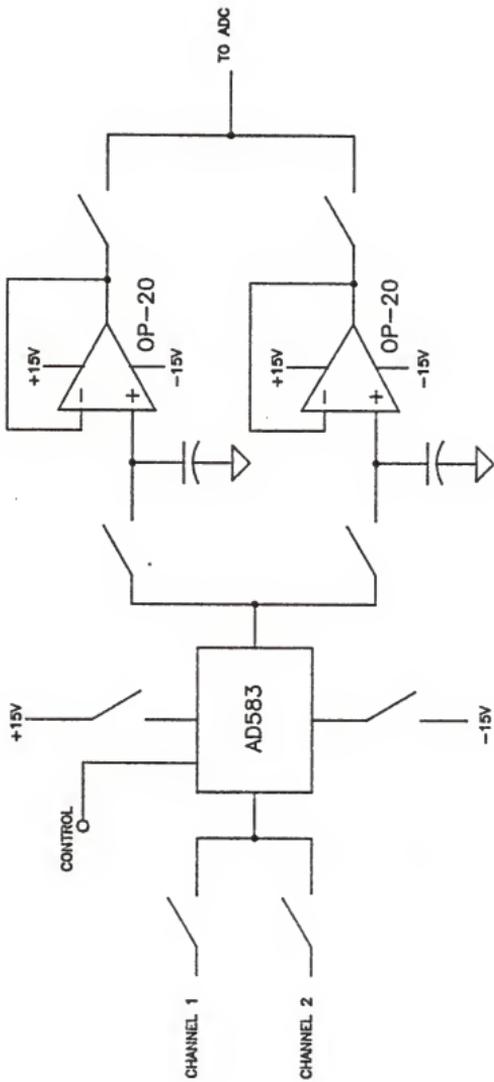


Figure 16. Sample and Hold Module

discharge before turning the device off.

The next step was to determine the timing required for the control signals to the S&H and the ADC and design the control logic. Since a 4 MHz clock signal was provided from the system microprocessor, a CD4060 binary counter was used to divide the clock down to obtain a 244 Hz sample rate clock. This was within the 5% tolerance specified by Sandia. The counter was also used to obtain a 125 KHz clock to drive the control logic, which would yield 8 μ s resolution in the control signals. Also, to reduce noise during the conversion, it was decided to disable the control logic during the conversion and to use the EOC signal from the ADC to restart the controller. Using this information, and the warm-up time measurements made earlier, the timing diagram for the system shown in Figure 17 was determined. To implement this timing, the circuit shown in Figure 18 was used. The 244 Hz sample rate clock was used to clock a flip-flop which controlled the 125 Hz logic clock. The logic clock was used to advance a counter which, in turn, was connected to the address lines of an EPROM used to store the desired system timing sequence. The output of the EPROM was latched using the same signal used to clock the address counter. The falling edge of the START CONVERSION pulse was used to clock a second flip-flop which would disable the 125 KHz logic clock. The falling edge of the EOC signal, inverted to provide a rising edge to clock a third flip-flop, was used to reset the second flip-flop and restart the idle logic. This sequence is repeated for the second conversion. When the address counter reaches the value \$43, the first flip-flop

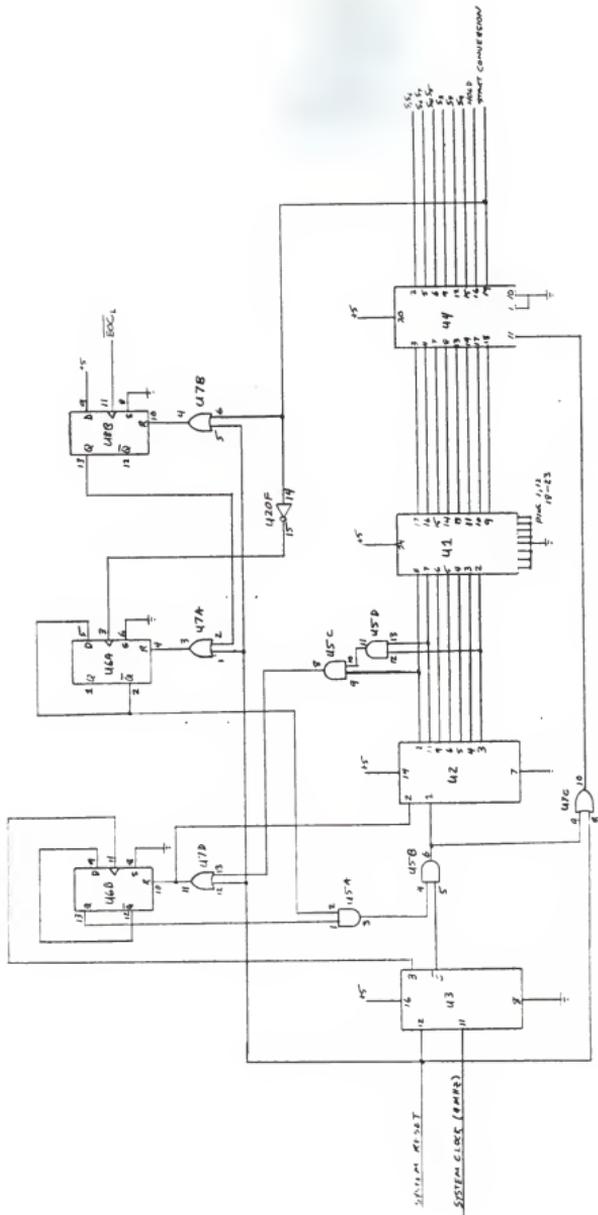


Figure 18. Schematic of 12-bit ADC, Control Logic

and the address counter are reset and the system is ready to perform another pair of conversions on the next rising edge of the sample rate clock.

To interface the ADC to the system microprocessor, a set of Tri-State latches were used. The EOC signal from the ADC is used to toggle a flip-flop which alternately clocks each pair of latches to store the results of each conversion. The signal used to store the results of the second conversion is also used to clock another flip-flop which asserts an interrupt flag to the microprocessor. To enable the processor to read the data, four register control signals, designated R0 through R3, were provided and connected to the Tri-State control on each latch. Also, R3 is used to reset the interrupt flag, so when the system is initially powered-up, a dummy read of R3 is required. The analog portion of the system, along with the interface to the system processor, is shown in Figure 19. One problem encountered in using the ADC-HC12B is that the logic levels required by the device are equal to the supply voltage which, in this case, is +15V. Reducing the +15V levels out of the device to +5V was accomplished by using CD4050 CMOS inverters which are capable of handling overvoltage signals on the inputs. To pull the START CONVERSION signal up to +15V, a spare switch in one of the DG211 packages was used.

The system was tested using a Hewlett Packard test system consisting of an HP9845B computer, an HP3455A digital voltmeter, an HP3325A function generator, and a 6940B multiprogrammer. The function generator was used to provide a programmable DC input

signal to the S&H. The signal was measured using the digital voltmeter. The digital output from the ADC was read by the computer via an isolated input card in the multiprogrammer. Data acquisition and plotting was performed by the 9845B computer. The first test on the system was to determine the linearity of the ADC. With the S&H module bypassed, the input signal was applied directly to the ADC and the device characteristic was recorded by the computer. A plot of output code as a function of input voltage is shown in Figure 20. It can be seen from the graph that the ADC characteristic is highly linear, with only a slight deviation from the ideal slope. The second test performed was to compare the warm-up time for the AD583 measured using the oscilloscope and the results obtained using the ADC on the S&H output. Figure 21 shows the outcome of the tests performed using a 0.0047 μF hold capacitor. The data obtained using a 0.033 μF hold capacitor are shown in Figure 22. The results obtained using this method agree quite well with those obtained earlier. The warm-up time for the 0.0047 μF capacitor is shown to be between 50 μs and 100 μs , while the value measured earlier was 90 μs . The warm-up time required for the 0.033 μF capacitor is shown to be between 150 μs and 200 μs . The value measured earlier was 180 μs . It can also be seen from these graphs that the linearity of the overall system is not affected by the inclusion of the S&H module, if the correct warm-up time is used.

Once it was known that the system was functioning properly, the last area to be examined was the power consumption. The breakdown for the analog portion is as follows:

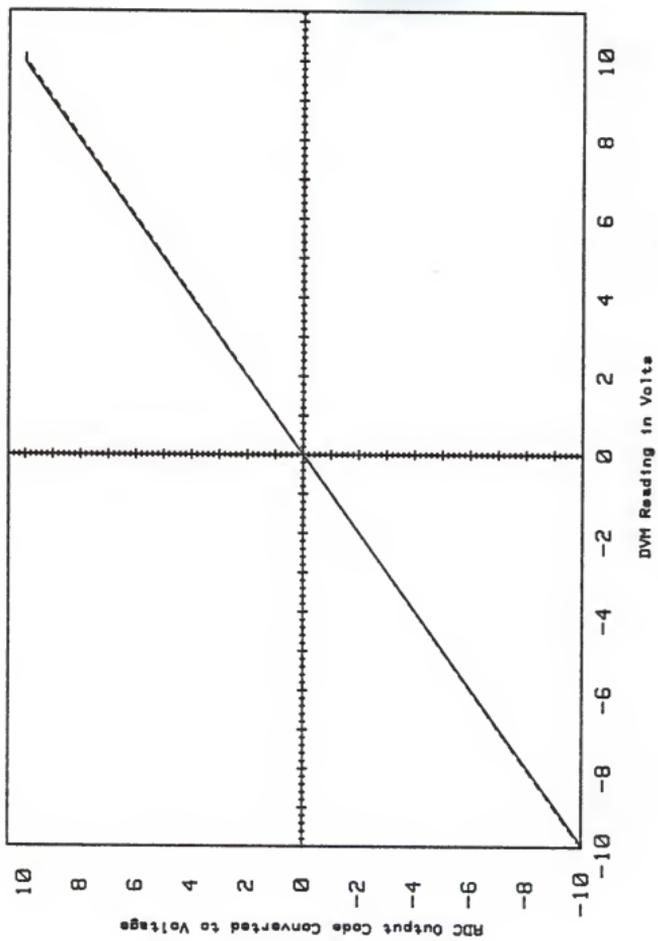


Figure 20. ADC-HC12B Device Characteristic

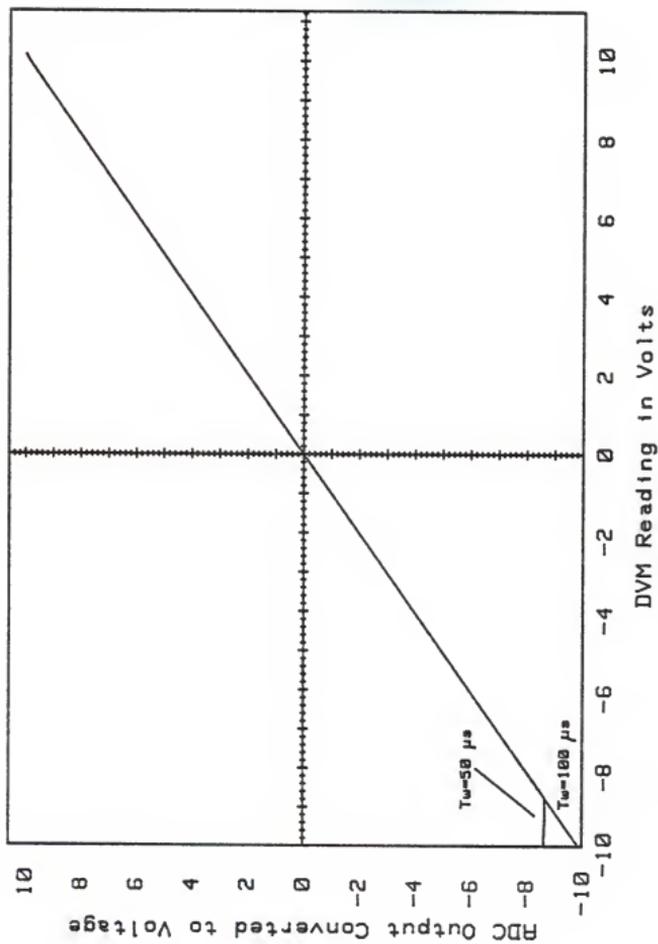


Figure 21. System Response as a Function of S&H Warm-up Time using a 0.0047 μF Hold Capacitor

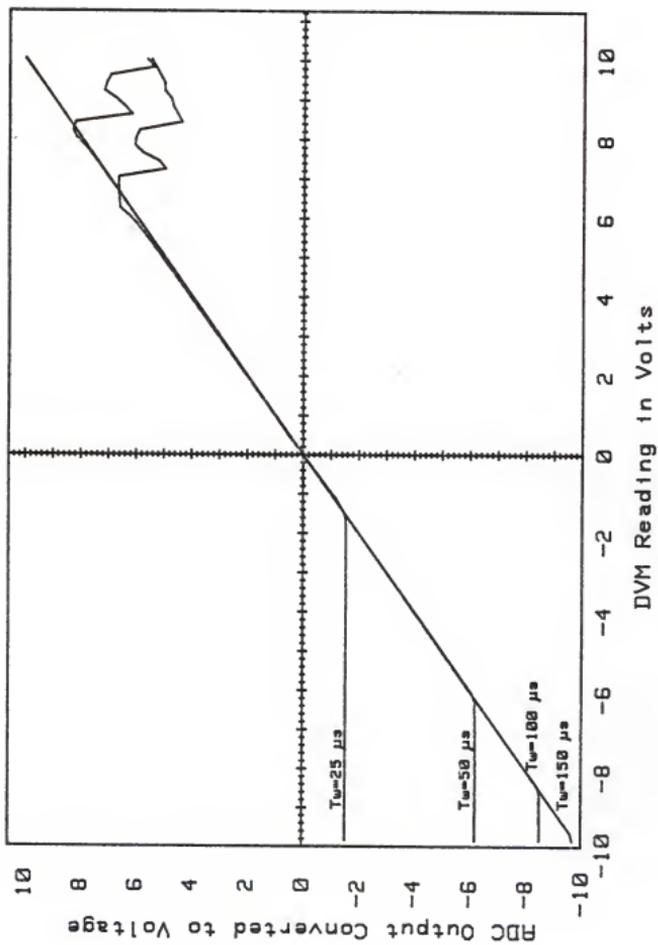


Figure 22. System Response as a Function of S&H Warm-up Time using a $0.033 \mu F$ Hold Capacitor

<u>Device</u>	<u>Power Dissipation</u>
ADC-HC12BMM	30 mW
AD583	6.5 mW
OP-20 (x2)	5.5 mW
<u>DG 211 (x3)</u>	<u>60 mW</u>
TOTAL	102 mW

The figures above use maximum continuous power dissipation. The value obtained for the AD583 uses the maximum continuous power dissipation multiplied by $176 \mu\text{s}/4098 \mu\text{s}$, the ratio of "on" time to switching period. The total power dissipation of the S&H module comes to 72 mW, a reduction of 66% over that of operating the components continuously. This could be reduced even further by using the DG211 switches only for power switching, where overvoltage protection is required, and on the inputs to the slave S&H's, where low charge transfer is required. Replacing the other two packages of DG211 switches with DG308 switches would reduce the power dissipation of the S&H module by an additional 39 mW, to a total of 33 mW. This would make the total dissipation of the analog portion 63 mW. The digital portion of the system consumes slightly more than 25 mW. This is broken down into two areas, the discrete logic, and the EPROM. The discrete logic, being all CMOS, consumes only 350 μW of power. The EPROM, however, consumes 25 mW, contributing greatly to the overall system dissipation, which would total 88 mW if the DG308 switches are used.

V. Design of the 15-bit ADC

Increasing the resolution of the ADC to 15 bits while maintaining a low power consumption presented several new problems. In the first system, a very low power 12-bit ADC was available, so the only area of difficulty was in reducing the power consumption of the S&H. However, there is no low power commercial ADC available which yields 15 bit resolution required for the second system. As a result, the technique of performing iterative conversions on an input sample with one or more ADC's was investigated. This method was discussed earlier as a way to obtain an 8-bit flash converter by using two, four bit flash ADC's and a Digital to Analog Converter (DAC), and was presented by Zuch [3]. In actuality, the method is more difficult than is indicated by Zuch, especially in higher resolution applications.

To investigate this method, the Telmos TML 1070 7-bit Flash ADC was used. The TML 1070 is a CMOS device having a continuous power dissipation of 10 mW for low speed operation (< 100 KHz). The configuration shown in Figure 23 was used in an effort to obtain 14-bit resolution from the 7-bit flash ADC. The system works in the following manner. First, the input signal, presumably from the S&H, is converted by the flash. This 7-bit "pre-conversion" is input to the upper 7-bits of a 14-bit DAC to obtain a 7-bit estimate of the input signal. The 14-bit DAC is required because, in order to obtain a 14-bit result, the analog estimate must have 14-bit linearity. The estimate of the input signal is then subtracted from the actual input signal to obtain

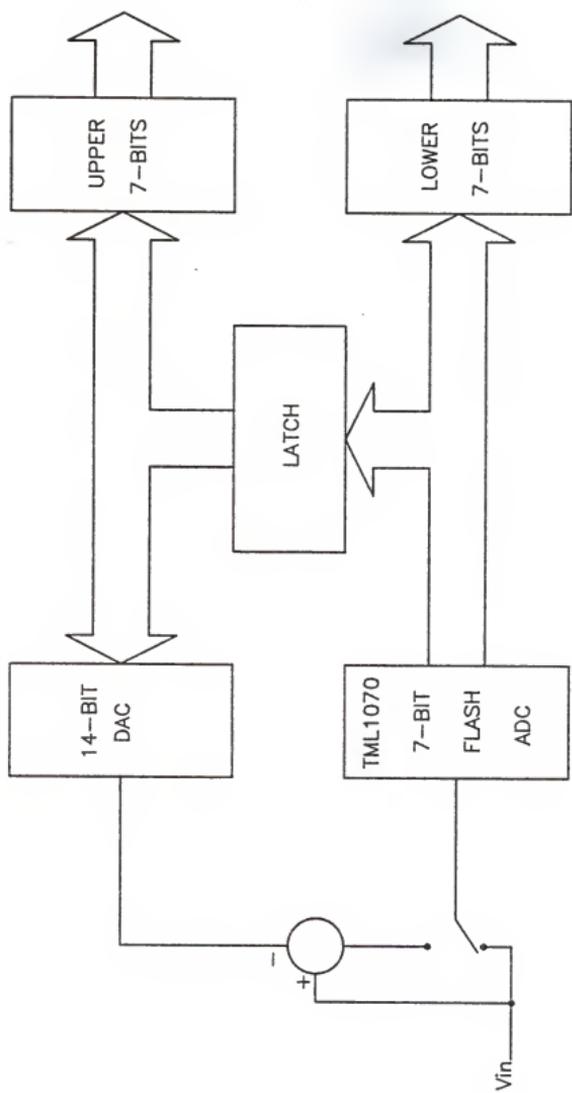


Figure 23. 14-bit Iterative Flash Converter

an error signal. Ideally, the error signal has a magnitude of $1/2$ LSB or less. This error signal is then amplified by 128, which makes a $1/2$ LSB error a fullscale input to the flash. The amplified error signal is then converted to digital form by the flash. This "post-conversion" yields the lower 7 bits of the 14-bit result, while the "pre-conversion" yields the upper 7 bits.

The system described above was built and tested manually using an HP3325A function generator as a DC signal source, and an HP1600A logic state analyzer to monitor the digital output. The schematic diagram of the system tested is shown in Figure 24. The system uses a $\pm 2.5V$ reference which gives the LSB a value of $305 \mu V$. This indicates a common problem with high resolution systems, noise. The noise level in the system must be kept below $1/2$ LSB, or $152 \mu V$. Since it is difficult to accurately measure the noise level in a system using an oscilloscope, an easier method is to operate the ADC and check the stability of the lower bits, and the repeatability of the output code. This was done on the 14-bit flash system and it was concluded that the noise level was below the $1/2$ LSB level, since the digital output was stable for a given input voltage, the output code would respond correctly to a $305 \mu V$ change in the input voltage, and, no matter what input voltage had been applied previously, whenever a preselected input voltage level was returned to, the output code would be the same. However, in the process of performing these tests, it was discovered that a "dead zone" existed between the fullscale output on the "post-conversion", and the next bit

change on the "pre-conversion". Further investigation showed that for input voltages resulting in "dead zone" operation, the magnitude of the error signal was exceeding the $1/2$ LSB limit imposed by the system design. The reason the error signal is able to exceed the limit is due to the differential nonlinearity of the TML 1070.

In order for the error signal to remain within the $\pm 1/2$ LSB limits proposed, the ADC used would need to have a differential nonlinearity of zero. This is because each output code step of the ADC is ideally 1 LSB wide, and the DAC output voltage would ideally be the voltage at the center of the ideal step, thus leaving $1/2$ LSB of variation on each side of the DAC estimate. Such a value of differential nonlinearity cannot be obtained. A more common value would be $\pm 1/2$ LSB. In this case, the maximum magnitude of the error signal would be 1 LSB. To amplify this value to a full scale input for the "post-conversion" would require a gain of 64. This would result in the LSB of the "pre-conversion" having the same value as the MSB of the "post-conversion", thus yielding a 1-bit overlap between the conversions. The two bits could be OR'ed together to form the final result since, due to the design of the system, only one of the bits can be set at a time.

In the case of the TML 1070, the differential nonlinearity has a maximum value of $+4/5$ LSB. With this value, an error signal as large as 1.3 LSB's may occur. To accommodate this large a signal, the gain in the feedback loop must be reduced to 32, resulting in a 2-bit overlap between the two conversions. To

obtain the correct digital output code, the "post-conversion" must be sign extended to 12-bits and added to the "pre-conversion" followed by five zeros to allow for the 2-bit overlap. As a result, the maximum resolution which can be obtained using the TML 1070 in this fashion is 12-bits.

In order to obtain 15-bit resolution using the iterative conversion technique, either the resolution of the ADC used must be increased to allow for the overlap, or a second ADC with a higher resolution must be used to perform the "post-conversion". It was decided to pursue the second option using the Datel-Intersil ADC-HC12B to perform the "post-conversion" since it had already been proven in the first system. Such a system would use the top 5 bits of the "pre-conversion" performed using the TML 1070, and all 12 bits of the "post-conversion", with a two bit overlap to correct for the differential nonlinearity errors. At present, research on this system is being done by Doug Doerfler, who is working at Kansas State University as part of a research contract with Sandia National Laboratories.

In an iterative system such as the one described above, there are a variety of sources for error, mainly due to resistor tolerances and resistor matching. For example, to obtain absolute accuracy in the feedback loop, the error signal formed from the difference between the input signal and the DAC estimate must be accurate to 15 bits. This requires 15-bit matching between both the input resistors to the difference amplifier and the difference amplifier feedback resistor which controls the system

feedback loop gain. This is not very practical since 0.001% tolerance resistors are very expensive. Also, DAC and op-amp offsets in the feedback loop will affect the accuracy of the system as well. To determine the overall effects of these errors, we will have to wait for Mr. Doerfler's research to be completed.

VI. Conclusion

The motivating force behind the research leading up to the design of the systems presented in this paper was the lack of commercially available systems offering high performance coupled with low power consumption. However, industry is slowly becoming attuned to the specialized needs of persons designing real time signal processing systems for field use. The two approaches to power consumption reduction presented in this paper, low duty cycle power switching and iterative analog-to-digital conversion, offer substantial increases in system performance without sacrificing low power consumption. To realize the maximum advantage, these methods should be incorporated in large scale systems fabricated on hybrid integrated circuits. Since both methods have already seen limited, small scale exposure in industry, such a future for these methods is expected. In fact, at the time of this writing, Datel-Intersil has just released the ADC-868, an ultra high speed 12-bit modular ADC which uses an iterative flash conversion method similar that discussed in this paper. Unfortunately, the ADC-868 was designed with high speed, high resolution conversions in mind, operating at 2 MHz and consuming over 9 watts, but it does demonstrate the feasibility of the iterative conversion method. The feasibility of power switching has already been demonstrated by devices such as the Datel-Intersil ADC-HC12B ADC discussed in this paper.

Acknowledgements

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A note to my wife:

Honey - I'll be home soon.

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4. Eugene L. Zuch, "Principles of Data Acquisition and Conversion," Data Acquisition and Conversion Handbook, p. 3, Datel-Intersil, 1980.
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APPENDIX I

Test Programs for Analog to Digital Converters

```

10 ! Program Title: "ADC/SH" [ADC test and Sample & Hold test]
20 !   Programmer: Tim J. Sobering and Kirk D. Scarbrough
30 !       Date: 9/10/82
40 !       Version: 1.2
50 ! Description:
60 !           This program is designed for testing any 12-bit
70 !           ADC or S&H/ADC module. It supplies a DC stimulus under
80 !           computer control to the module via an HP 3325A
90 !           Synthesizer/Function Generator, mentions the stimulus
100 !          using an HP 3455A DVM, and reads the ADC output data
110 !          back to the computer via an HP 6948B Multiprogrammer
120 !          and an HP 59500A Multiprogrammer Interface. The computer
130 !          then stores the data on a mass storage device and plots
140 !          the output using an HP 9872A type plotter.
150 ! Revisions:
160 !       9/11/82 - Added capability of storing Hold Capacitor value
170 !               and S&H warmup time in data file.
180 !
190 !
200 !
210 !
220 ! *****
230 !
240 !
250 !
260 !
270 !
280 !           Declare and Initialize Variables
290 !
300 OPTION BASE 0
310 DIM Vin(100,2),Month$(12)(5),Mer$(2),Records$(22),Mass$(5),File$(11)
320 DIM Day$(2),Hour$(2),User$(4),P$(1),Q$(1),T$(1),Time$(2),Mow$(6)
330 DIM Holdcap$(8)
340 INTEGER Month,Hour,Stat,Dvm,Fgn,Mux,I,H,Day,Octal,Name_entered,File_entr
350 REAL X_label,Y_label
360 Fgn=717 ! Set HP-IB Bus Addresses
370 Dvm=722 ! for Digital Voltmeter.
380 Mux=723 ! Function Generator, and
390 ! Multiprogrammer
400 Mass$=":F8,0" ! Set data mass storage
410 ! device
420 PRINTER IS 16 ! Declare CRT as printer
430 PRINT "*" ! Clear CRT
440 !
450 !
460 !
470 INPUT "Do you want to print out an old file?(Y/N)" P$
480 IF UPC$(P$)="Y" THEN 520
490 IF UPC$(P$)="N" THEN 570
500 BEEP
510 GOTO 470
520 GOSUB Get_file

```

```

530   GOSUB Print_file
540   !
550   !
560   !
570   INPUT "Do you want to plot an old file?(Y/N)",Q$
580   IF UPC$(Q$)="Y" THEN GOTO Plot
590   IF UPC$(Q$)="N" THEN GOTO Take
600   BEEP
610   GOTO 570
620   !
630   !
640   !
650 Plot: GOSUB Get_file
660       GOSUB Plot_start
670       GOTO End
680   !
690   !
700   !
710 Take: INPUT "Do you want to take Data:(Y/N)",T$
720   IF UPC$(T$)="Y" THEN 760
730   IF UPC$(T$)="N" THEN End
740   BEEP
750   GOTO 710
760   Name_entered=0
770   GOSUB Take_data
780   GOSUB Store_data
790   GOSUB Plot_start
800   !
810   !
820   !
830 End: DISP " NORMAL PROGRAM TERMINATION "
840   END
850   !
860   !
870   !
880 Filename: IF Name_entered THEN RETURN
890       PRINT "Data File Name on Device "&Mass$&"?(max. 6 char.)"
900       INPUT File$
910       PRINT ""
920       File$=File$&Mass$
930       Name_entered=1
940       RETURN
950   !
960   !
970   !
980 Take_data: GOSUB Filename
990       GOSUB Real_time
1000      INPUT "SM Hold capacitor valuetmax. 8 characters)?",h0lccap$
1010      LINPUT "Monostable Pulse Width?",hpwt
1020      PRINTER IS 7,1
1030      PRINT PAGE;
1040      PRINT "           Filename: ";File$
1050      PRINT

```

```

1060 PRINT Record$
1070 PRINT
1080 PRINT "Sample & Hold warm up time: ";mpw$
1090 PRINT
1100 PRINT "Holding Capacitance: ";Holdcap$
1110 PRINT
1120 PRINT "XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX"
1130 PRINT "XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX"
1140 PRINT "***          ***          ***          ***          ***"
1150 PRINT "          FGN          DVM          ***          ADC          ***"
1160 PRINT "          OUTPUT          ***          INPUT          ***          OUTPUT          ***"
1170 PRINT "          (Volts)          ***          (Volts)          ***          (Volts)          ***"
1180 PRINT "          ***          ***          ***          ***          ***"
1190 PRINT "XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX"
1200 PRINT "XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX"
1210 !
1220 FOR I=0 TO 100 STEP 1
1230     Vin(I,0)=(I-50)/10
1240     Vset$=VAL$(Vin(I,0))
1250     OUTPUT Fgn;"FU00F"&Vset&"VO"
1260     GOSUB Digivolt
1270     OUTPUT Mux;"00140TDT"
1280     WAIT 500
1290     ENTER Mux;Octal
1300     IF DECIMAL(Octal)>2048 THEN Positive
1310     Vin(I,2)=DECIMAL(Octal)-4096
1320     GOTO Loopend
1330 Positive: Vin(I,2)=DECIMAL(Octal)
1340 Loopend:Vin(I,2)=.0048852*Vin(I,2)
1350     PRINT USING 1360;"***";Vin(I,0);"***";Vin(I,1);"***";Vin(I,2):"***"
1360     IMAGE 3A,4X,DD.DDD,5X,3A,4X,DD.DDD,5X,3A,3X,DDD.DDD,5X,3A
1370     NEXT I
1380     OUTPUT Fgn;"OF0VO"
1390     PRINT "XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX"
1400     PRINT "XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX"
1410     PRINT PAGE
1420     PRINTER IS 16
1430     RETURN
1440 !
1450 !
1460 !
1470 Digivolt: RESET Dvm
1480     OUTPUT Dvm;"F1R7T2D1"
1490     TRIGGER Dvm
1500 Erases. STATUS Dvm;Stat
1510     IF Sta=65 THEN Get_value
1520     IF Sta=0 THEN Status
1530     DISP "DVM Error ",Stat
1540     BEEP
1550     STOP
1560 Get_value:ENTER Dvm;Vin(I,1)
1570     RETURN
1580 !

```

```

1590 !
1600 !
1610 Store_data:CREATE Files,78,32
1620     ASSIGN #1 TO Files
1630     PRINT #1;Vin(*)
1640     PRINT #1;Record$
1650     PRINT #1;mpw$
1660     PRINT #1;Holdcap$
1670     ASSIGN > TO #1
1680     RETURN
1690 !
1700 !
1710 !
1720 Get_file: IF File_entered THEN RETURN
1730     GOSUB Filename
1740     ASSIGN #1 TO Files
1750     READ #1;Vin(*)
1760     READ #1;Record$
1770     READ #1;mpw$
1780     READ #1;Holdcap$
1790     ASSIGN #1 TO *
1800     File_entered=1
1810     RETURN
1820 !
1830 !           Subroutine to plot data
1840 !
1850 Plot_start:INPUT "CRT or the 9872B Plotter?(CRT=0,Plotter=1)".H
1860 IF H=0 THEN 2040
1870 IF H=1 THEN 1930
1880 BEEP
1890 GOTO 1850
1900 !
1910 !           Declare 9872B as plotter and set limits
1920 !
1930 DISP "Set up PLOTTER and press CONT"
1940 PAUSE
1950 DISP
1960 PLOTTER IS 13,"GRAPHICS"
1970 GCLEAR
1980 PLOTTER IS 7,5.0,"9872A"
1990 LIMIT 0,350,0,260
2000 GOTO 2110
2010 '
2020 !           Declare CRT as plotter and set limits
2030 '
2040 PLOTTER IS 13,"GRAPHICS"
2050 LIMIT 0,1E+4 0,145
2060 !
2070 '           Locate and frame graph area
2080 !
2090 GCLEAR
2100 GRAPHICS
2110 LOCATE 32,124.2,32,98

```

```

2120 CLIP 32,130,32,100
2130 SCALE -10,10,-10,10
2140 PEN 1
2150 LINE TYPE 1
2160 FRAME
2170 FRAME
2180 AXES ,2,,2,0,0,5.0,5.0,1      ! Draw axes
2190 UNCLIP                          ! Enable to draw outside graph area
2200 !
2210 !                               Label X axis
2220 !
2230 FOR X_label=-10 TO 10 STEP 2
2240   CSIZE 3
2250   MOVE X_label,-11
2260   LORG 4
2270   LABEL X_label
2280 NEXT X_label
2290 !
2300 !                               Label Y axis
2310 !
2320 FOR Y_label=-10 TO 10 STEP 2
2330   CSIZE 3
2340   MOVE -11,Y_label
2350   LORG 5.0
2360   LABEL Y_label
2370 NEXT Y_label
2380 !
2390 !                               Title X axis
2400 !
2410 MOVE 0,-12.4
2420 CSIZE 3
2430 LORG 4
2440 LABEL "DVH Reading in Volts"
2450 !
2460 !                               Title graph
2470 !
2480 MOVE 0,-14.4
2490 CSIZE 3.3,.6,13
2500 LABEL "ADC OUTPUT vs DVH INPUT READING"
2510 !
2520 MOVE 0,-16.4
2530 CSIZE 2.5
2540 LABEL "FILE: ",Files
2550 !
2560 !
2570 MOVE 0,-17.2
2580 LABEL Record$
2590 !
2600 !
2610 MOVE 0,-18.2
2620 LABEL "S&H warm up time: ",tpwt
2630 !
2640 !

```



```

3180 PRINT "*****"
3190 FOR I=0 TO 100 STEP 1
3200 PRINT USING 3210;"**";Vin(I,0);"**";Vin(I,1);"**";Vin(I,2);"**"
3210 IMAGE 3A,4X,DD.DDD,5X,3A,4X,DD.DDD,5X,3A,3X,DDD.DDD,5X,3A
3220 NEXT I
3230 PRINT "*****"
3240 PRINT "*****"
3250 PRINT PAGE
3260 PRINTER IS 16
3270 RETURN
3280 !
3290 !
3300 !
3310 Real_time: OUTPUT 9.0;"Request time" ! Request real time
3320 ENTER 9.0;Month,Day,Hour,Time$ ! Read real time
3330 RESTORE 3370 ! Place pointer at start of data
3340 FOR I=1 TO 12
3350 READ Month$(I) ! Read data into string array
3360 NEXT I
3370 DATA JAN,FEB,MARCH,APRIL,MAY,JUNE,JULY,AUG,SEPT,OCT,NOV,DEC
3380 Mer$="AM" ! Start by assuming "AM"
3390 IF Hour>11 THEN Mer$="PM" ! Use "PM" if past noon
3400 IF Hour>12 THEN Hour=Hour-12 ! Convert to 12-hour format
3410 IF Hour=0 THEN Hour=12
3420 Day$=VAL$(Day)
3430 Hour$=VAL$(Hour)
3440 Record$=Month$(Month)&" "&Day$&" at "&Hour$&":"&Time$&" "&Mer$
3450 RETURN

```

The Design of Low-Power, High-Resolution, Analog to Digital
Conversion Systems with Sampling Rates less than 1 KHz

by

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Abstract

In recent years, there has been an increased usage of microprocessor-based, real-time, signal processing systems in field applications. In such systems, which operate off limited power sources, the high power consumption of the analog to digital converter and associated sample and hold has severely restricted the duration of operation due to short battery lifetimes. The need for a high resolution analog to digital conversion system which could operate at moderate speeds with low power consumption is apparent.

This paper discusses the design and evaluation of two systems incorporating techniques which partly solve this problem. The techniques are low duty-cycle power switching to reduce power consumption, and performing iterative conversions to obtain increased resolution. First, a discussion of relevant system characteristics and design procedures is presented. Then, power switching is discussed and results demonstrating its effectiveness are included. Thirdly, material relating to a system constructed to evaluate this method is presented. Finally, a discussion of a second system which utilizes an iterative flash conversion technique is included.

The test results for both systems are presented, along with a discussion of potential system problems.