SIMULATION OF PHASE-LOCKED LOOPS WHICH USE A PHASE-FREQUENCY DETECTOR

by

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TABLE OF CONTENTS

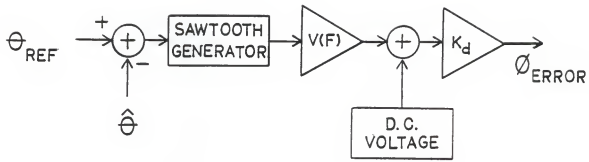
LIST OF FIGURES

I. INTRODUCTION

Computer simulations of Phase Locked Loop acquisition times are easily accomplished for loops using a product type Phase Detector by treating the detector as a balanced mixer.

Substituting a Phase-Frequency Detector, which has an output voltage proportional to frequency as well as phase, poses a more difficult challenge. This paper develops a method for simulating the output of a Motorola MC12540 Phase-Frequency Detector, and compares its behavior with the old standard, the phase detector, in a type Two Phase-Locked Loop.

A block diagram of the proposed model for the phase-frequency detector is shown in Figure 1. The phase difference between the reference and feedback phase is input into a sawtooth generator whose magnitude is frequency dependent. This sawtooth wave is then added to a frequency dependent DC term to yield the detector output error voltage. Arguments leading to this model are presented in the next section. The model is based on both analysis and experimental work.



θ_{REF} - reference input phase

$\hat{\theta}$ - phase of the Voltage Controlled Oscillator

V(F) - frequency dependent magnitude function

K_d - detector gain

FIGURE 1) Block Diagram of the Phase-Frequency Detector Model

II. DEVELOPMENT OF A MATHEMATICAL MODEL FOR THE PHASE FREQUENCY DETECTOR.

The MC12540 has the logic diagram shown in Figure 2 [1]. With two inputs and two outputs, this circuit can assume up to sixteen possible states. Analysis has revealed that only twelve of these states are stable, as shown in Figure 3.

The inputs to the circuit may change in any one of three ways:

R6 may change state

V9 may change state or

both R6 and V9 may change simultaneously.

The state diagram of Figure 4 shows all of the possible transitions of this circuit. A computer program used to verify this data is listed in Appendix A. Simultaneous changes of the input may be determined using Figure 4 by first changing one input and then the other. In all cases except two, the order in which V9, and R6 are changed using this chart is unimportant. The circuit always ends up in the same state. These two exceptions are observed with states '2' and '1'. Here a simultaneous change always results in a change to state '12'.

From this diagram some clues begin to emerge as to the behavior of the detector. If V9 changes at a much higher rate than R6, the circuit will end up spending most of the time in loops 1-5 and 9-13 regardless of the state it initially started in. In this instance, output D11 will be high most of the time. Similiarly, if input R6 changes much more rapidly than V9, the circuit will spend a large amount of time in loops 2-10 and 6-14.

A plot of output voltage vs. phase difference for the case of coherent frequency lock can be derived using the state diagram of Figure 4.

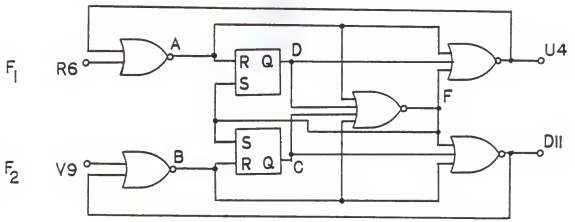


FIGURE 2) Logic Diagram of the Motorola MC12540 Phase-Frequency Detector

STATE	R6	V9	U4	D11	A	B	C	D	F
0	0	0	0	0	1	1	0	0	0
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	0	1	0	0	0
3	0	0	1	1	UNSTABLE				
4	0	1	0	0	1	0	1	0	0
5	0	1	0	1	1	0	0	0	0
6	0	1	1	0	0	0	1	0	0
7	0	1	1	1	UNSTABLE				
8	1	0	0	0	0	1	0	1	0
9	1	0	0	1	0	0	0	1	0
10	1	0	1	0	0	1	0	0	0
11	1	0	1	1	UNSTABLE				
12	1	1	0	0	0	0	1	1	0
13	1	1	0	1	0	0	0	1	0
14	1	1	1	0	0	0	1	0	0
15	1	1	1	1	UNSTABLE				

FIGURE 3) States of the MC12540

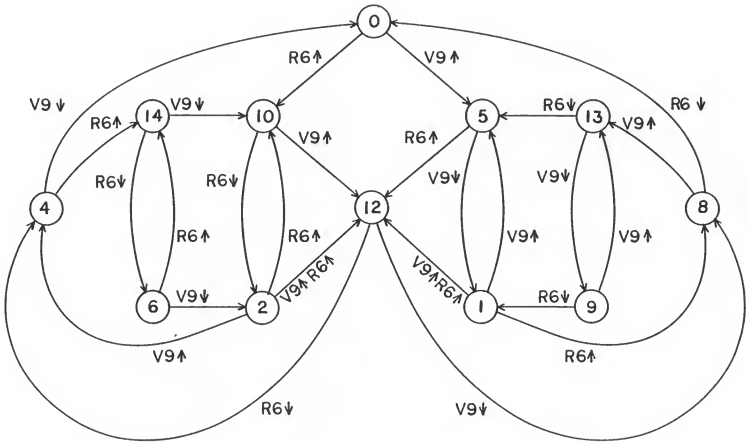


FIGURE 4) State Diagram of the MC12540

Assume that the input to R6 is exactly in phase with the input at V9. This situation is shown in Figure 5a. At time t=0- the circuit could be in any one of three states. But from the state diagram of Figure 4 it can be seen that no matter the initial situation, the circuit will oscillate between states '0' and '12'. No corrective voltage will be outputed. If the input at R6 were to lag by 90°, Figure 5b shows that the output at pin D11 would be high for 25% of the input cycle. As the delay at R6 approaches a 180° lag, state '5' (pin D11 high) appears close to 50% of the time. Note that the circuit is in state '8' before it drops momentarily into state '0'. At a phase difference of 180° (Figure 5d) the circuit cycles between state '5' and '8'. D11 is high 50% of the time. When the input at R6 approaches a phase delay of 2π, D11 approaches a 100% duty cycle as shown in Figure 5e. Note that state '1' is approaching the reference at t=0. When the delay reaches exactly 2π, D11 has a 100% duty cycle for one cycle (Figure 5f) but then shuts off as the circuit assumes the original conditions per Figure 5a.

The graph of Figure 6, showing the output voltage vs. phase difference for the coherent case, is directly derived from the preceeding explanation. It should be noted that at any point $\theta=n2\pi$ ($n=\pm1, \pm2, \ldots$) the state of the detector (after it 'goes over the top') is indistinguishable from the state at $\theta=0$. Therefore if the phase difference continues to increase, an output similar to the solid lines (to the right of zero in Figure 6) will occur. However should the phase difference then begin to decrease, the output will 'slide below' the x axis at any point which is a multiple of 2π. A continual decrease in the phase difference will result in an output similar to the negative

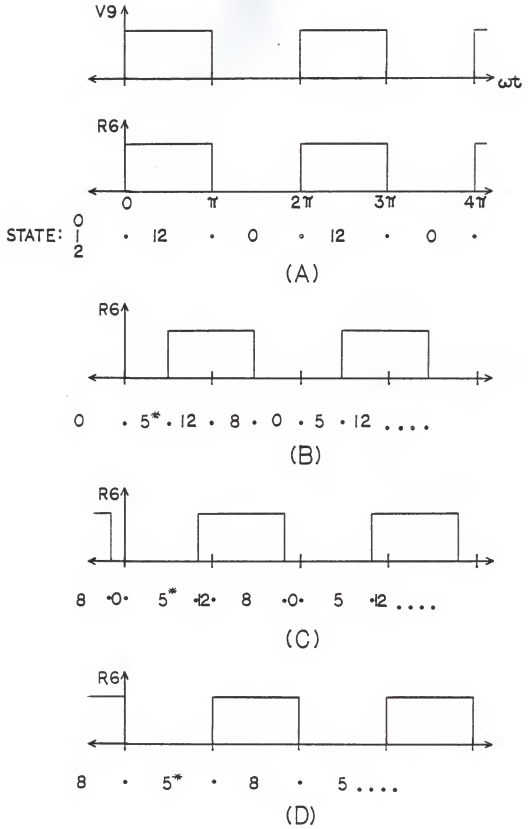


FIGURE 5) Output States over a Phase Lag of 2π

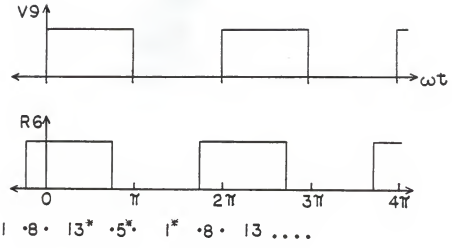


FIGURE 5) (CONTINUED)

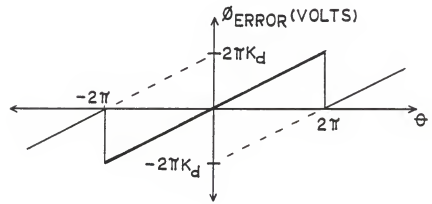


FIGURE 6) Coherent Output

going peaks of Figure 6 -- even if the total phase difference is still positive. This has been verified experimentally using the circuit shown in Figure 7.

This bench test also showed that the sawtooth output from the phase frequency detector completely disappears if the frequency at one of the inputs of the detector is much greater than the frequency at the other input. A DC voltage appears in its place. During the transition from a large frequency difference to a small one, the sawtooth output is observed to increase in magnitude, and to ride on a decreasing DC voltage until a low ratio of f_1/f_2 (or f_2/f_1) exists.

A plot of the observed normalized sawtooth magnitude vs. the frequency ratio f_2/f_1 is shown in Figure 8. With the exception of the spikes at the harmonics, the magnitude decreases in a relatively smooth curve.

In order to verify that the curve of Figure 8 was not a fluke caused by the testing set-up, and that the state diagram of Figure 4 will predict this behavior, a computer simulation of this test (see Appendix B) was developed. This program picks its initial state and phase delay at random, and then runs through a ten cycle simulation. The output of the detector is then run through a low pass filter, and the detected high and low values are stored. The results agree quite well with the observed behavior, and are also plotted in Figure 8.

Observations were also recorded of the normalized average value of the output as the frequency ratio was varied. These values are plotted in Figure 9. Comparison with information given by Rohde [2] shows a high degree of correlation.

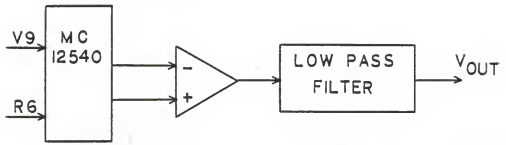


FIGURE 7) Block Diagram of Circuit used for Bench Test

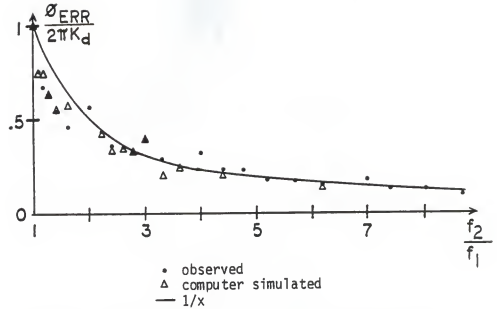


FIGURE 8) Sawtooth Magnitude - Simulated vs. Observed

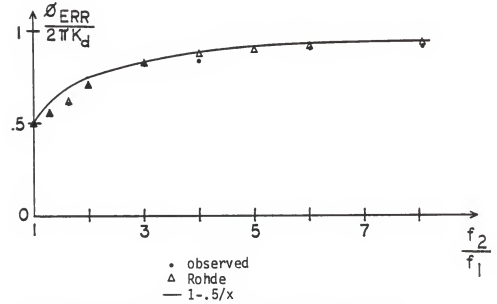


FIGURE 9) Average Value of Detector Ouput Voltage

The curves of both Figure 8 and Figure 9 vary according to the frequency ratios. The actual frequencies involved are immaterial so long as they do not cause 'racing' problems within the Phase Detector IC.

A recap notes the following observed behavior of the detector output:

1) A phase-difference dependent sawtooth waveform (see Figure 6) may be used to represent the detector output.
2) The magnitude of the sawtooth depends on the ratio of frequencies at the inputs of the detector (see Figure 8).
3) The average value of the output varies with the ratio of f_2/f_1.

Since the sawtooth magnitude decreases while the average value increases, a DC voltage term must be included to account for the increase in average value. The DC term should equal the difference between the sawtooth average and the total average value.

Figures 8 and 9 provide sufficient information to derive simple formulas for both the sawtooth multiplication factor V(f) and the DC voltage of Figure 1.

The normalized sawtooth average (half of the peak-to-peak value) closely approximates

$$v_{saw} = .5/x \text{ where } x = f_2/f_1 \ (f_2 > f_1). \qquad (1)$$

The normalized average value of the detector output (half of the sawtooth peak-to-peak voltage plus the DC term) closely follows the following equation:

$$v_{ave} = 1-.5/x \quad \text{where } x = f_2/f_1 \ (f_2 > f_1). \qquad (2)$$

Thus, the normalized DC voltage term, V_{dc}, may be written as

$$V_{dc} = V_{ave} - V_{saw} = 1 - 1/x \qquad (3)$$

It should be noted that the preceeding discussion is based on the frequency at V9 (f_2) being greater than, or equal to the frequency at R6 (f_1). A similar analysis for $f_1 > f_2$ shows that the plots of Figures 8 and 9 are valid, except that a negative voltage is outputed.

III. A SIMULATION OF PHASE LOCKED LOOP ACQUISITION CHARACTERISTICS

A Second Order, Type Two (and Three) Phase Locked Loop has been used to compare the lock acquistion capabilities of the Phase Detector with the Motorola Phase-Frequency Detector, in a noiseless environment. This PLL (see Figure 10) was designed to have a natural frequency, f_n, of 18 KHz and a damping factor of .707, when T_3=0.

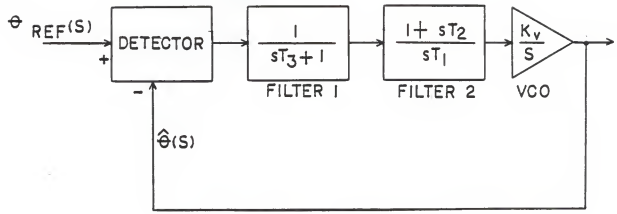
Breaking the block diagram down further into small pieces suitable for computer simulation results in the diagram of Figure 11. This diagram, along with previously discussed information, has been used to write the computer program of Appendix C. This program can simulate the behavior of both a phase detector, and a phase-frequency detector, in a phase locked loop.

Two parameters have been varied, and simulations run, in order to observe their effects on the two types of detectors.

The time constant T_3 represents an extraneous pole that is often introduced by physical construction techniques. It has been varied from 0 (resulting in a 2d Order Loop), to .1, .25, and .5 times T_2 (making a 3d Order Loop). Figure 12 shows the peaking in the locked closed loop power spectrum evident as T_3 changes the damping factor while moving towards the origin (see Figure 13).

The frequency of the reference input at time t=0 has been varied by a frequency step function. Steps of f_n, $2f_n$, $4f_n$, and $10f_n$ have been simulated.

The graphs of the detector error voltage from Figure 14 to 21 tell the story. A PLL with a phase-frequency detector has far superior acquisition properties, especially at high values of Δf (compare Figure 17 with Figure 21). Two factors account for this. First, the average



K_v - VCO Gain = 2 MHZ/Volt

T_1 - 9.824E-04

T_2 - 1.250E-05

T_3 - is derived in terms of T_2

FIGURE 10) Block Diagram of the 3rd Order Phase Locked Loop

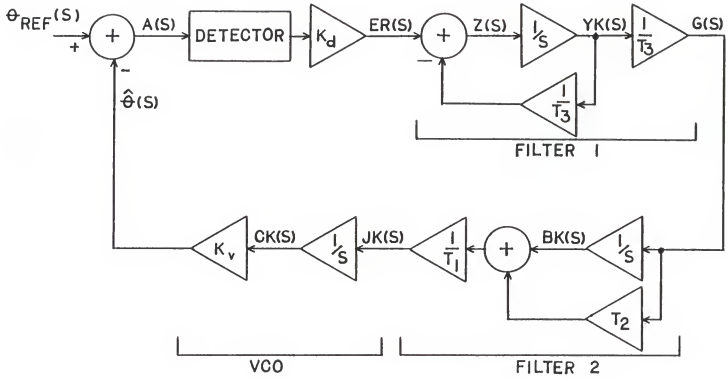


FIGURE 11) Block Diagram of the Computer Simulation
(low pass equivalent circuit in the 'S' domain)

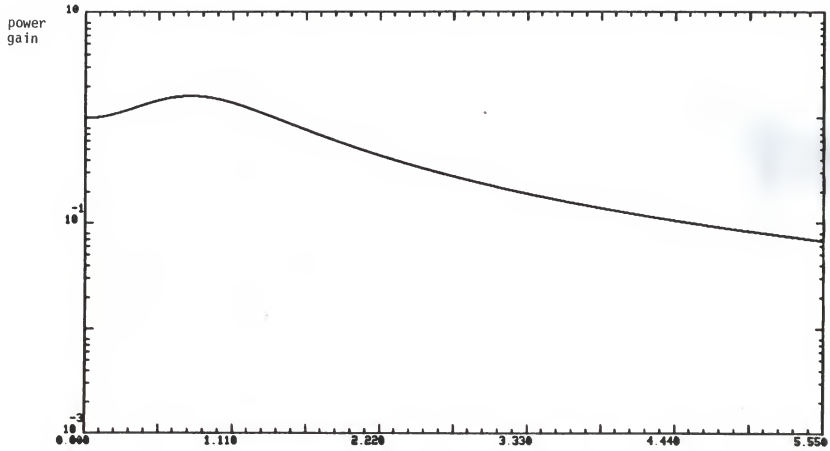


FIGURE 12a) Power Response of the Closed Loop System (T_3=0)

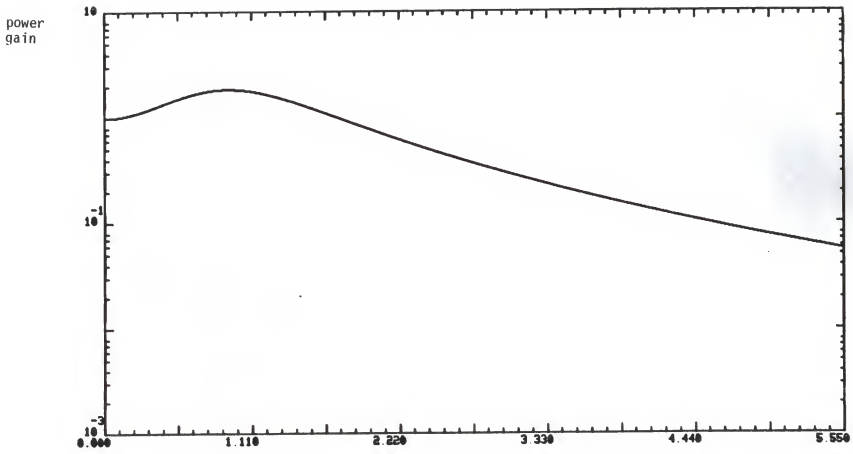


FIGURE 12b) Power Response of the Closed Loop System (T_3=.1T_2)

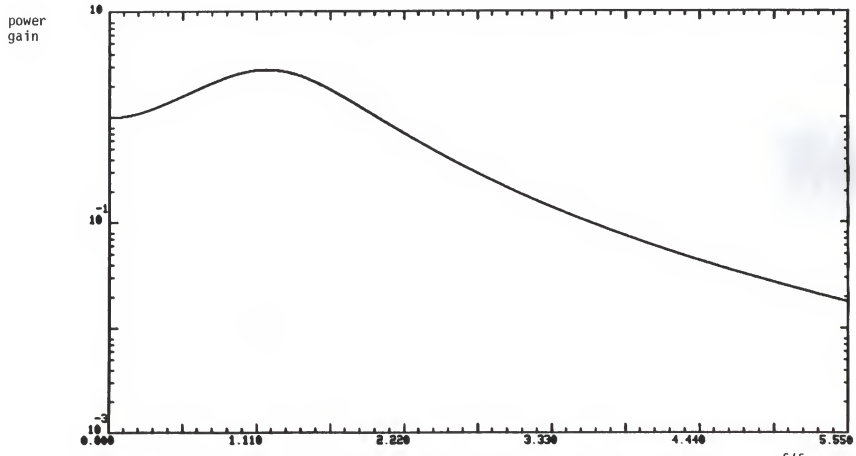


FIGURE 12c) Power Response of the Closed Loop System (T_3=.25T_2)

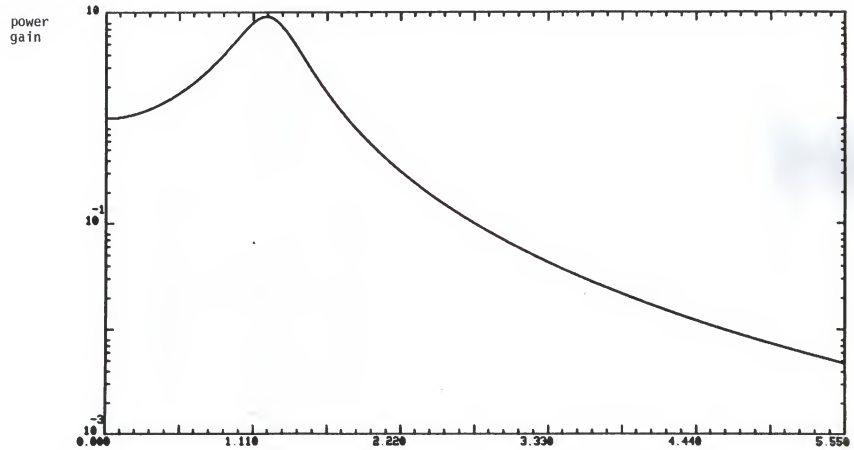


FIGURE 12d) Power Response of the Closed Loop System (T_3=.5T_2)

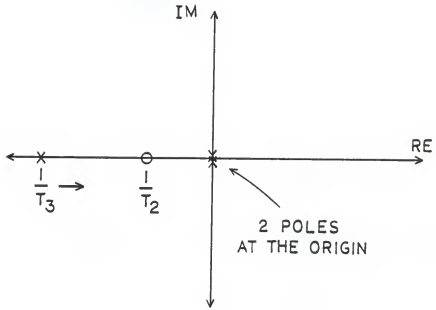


FIGURE 13) Pole and Zero Locations - Forward Loop Gain

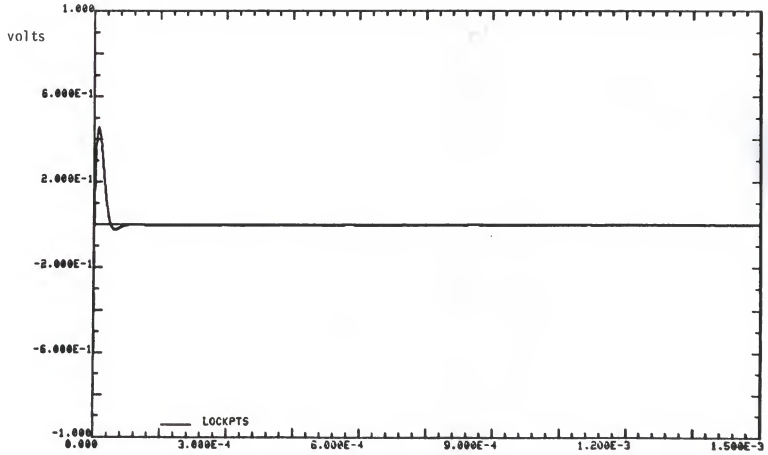


FIGURE 14a) Output of the Phase Detector $\Delta f = f_n$ (T_3=0)

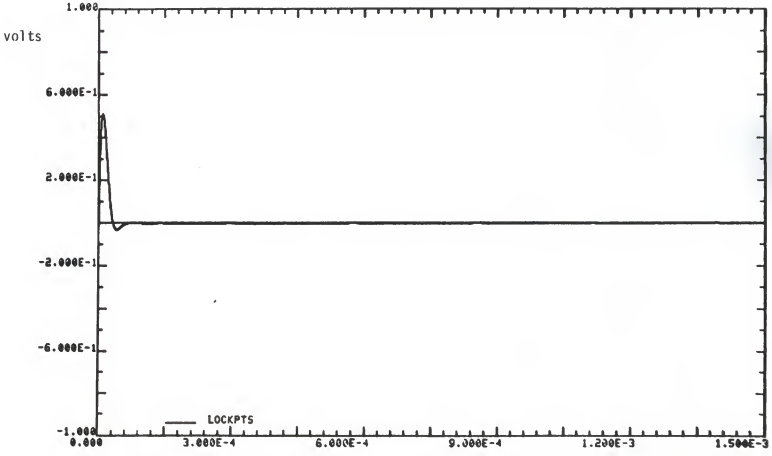


FIGURE 14b) Output of the Phase Detector $\Delta f=fn$ $(T_3=.1T_2)$

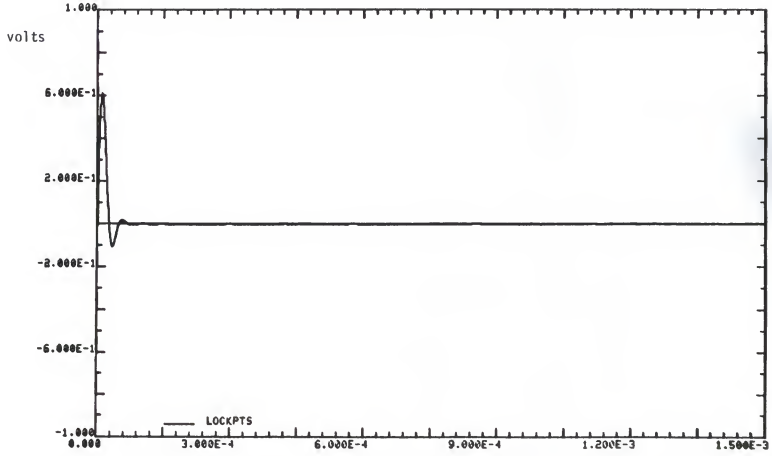


FIGURE 14c) Output of the Phase Detector $\Delta f=f_n$ $(T_3=.25T_2)$

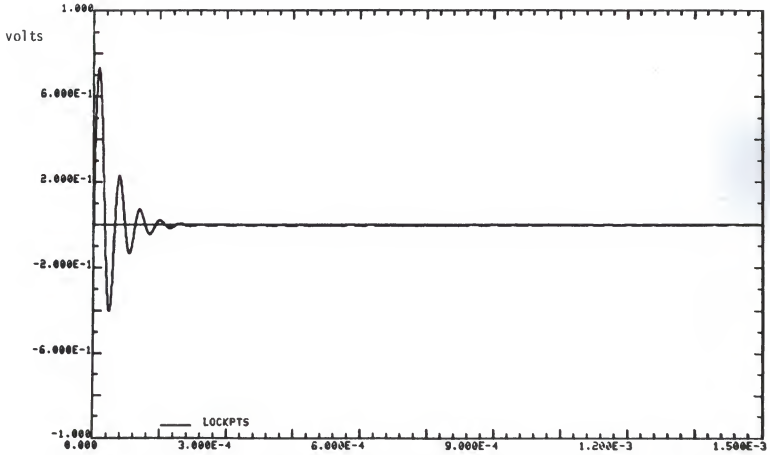


FIGURE 14d) Output of the Phase Detector $\Delta f = f_n$ $(T_3 = .5T_2)$

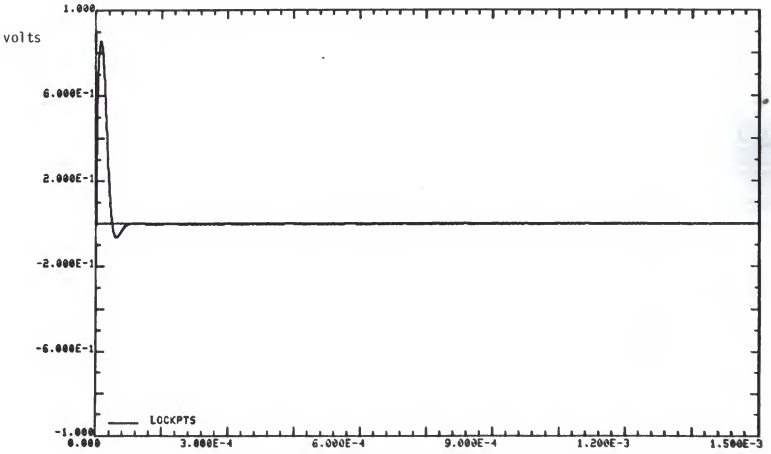


FIGURE 15a) Output of the Phase Detector $\Delta f=2f_n$ $(T_3=0)$

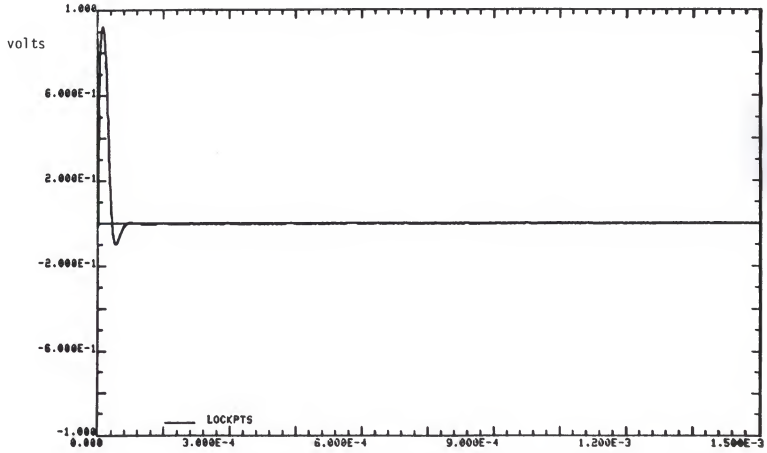


FIGURE 15b) Output of the Phase Detector $\Delta f=2f_n$ $(T_3=.1T_2)$ seconds

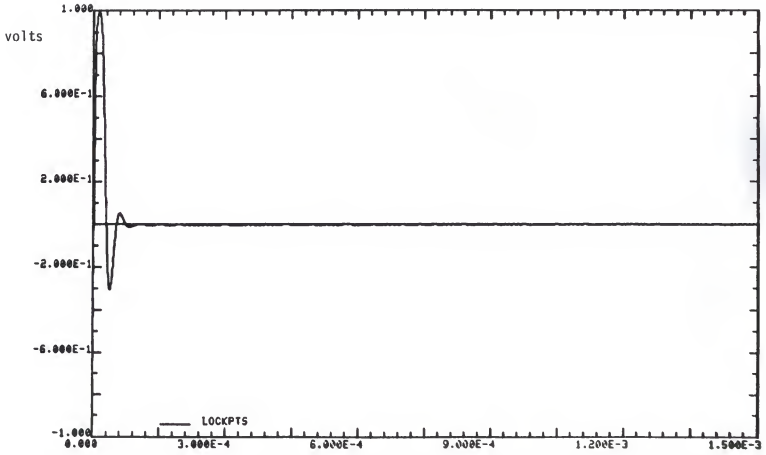


FIGURE 15c) Output of the Phase Detector $\Delta f=2f_n$ $(T_3=.25T_2)$ seconds

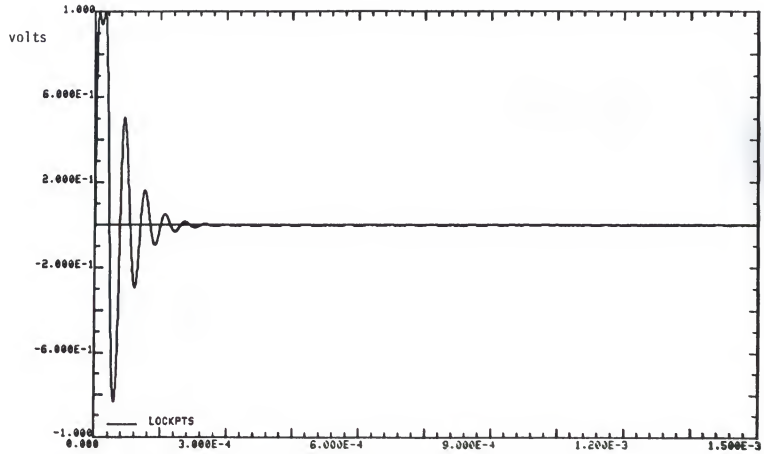


FIGURE 15d) Output of the Phase Detector $\Delta f=2f_n$ $(T_3=.5T_2)$

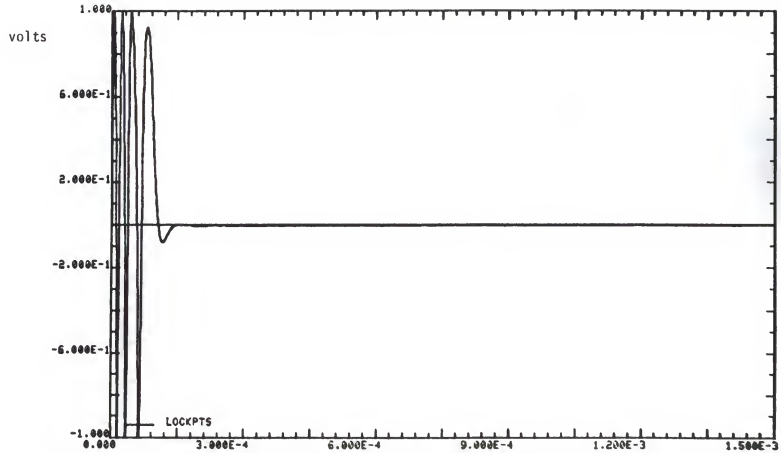


FIGURE 16a) Output of the Phase Detector $\Delta f = 4f_n$ (T_3=0)

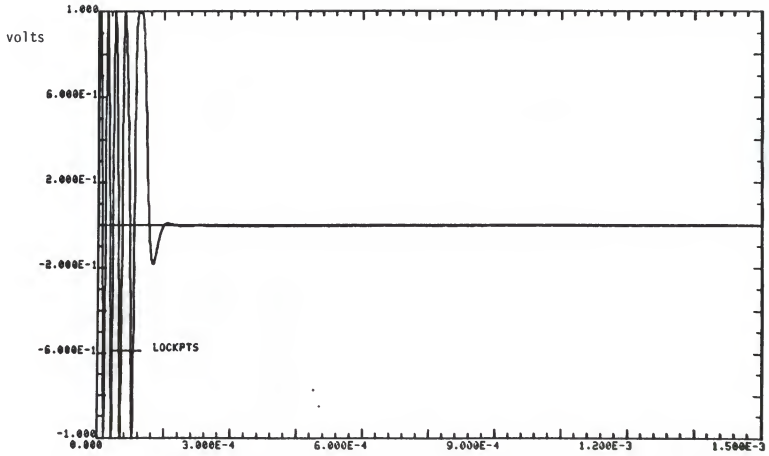


FIGURE 16b) Output of the Phase Detector $\Delta f=4f_n$ ($T_3=.1T_2$) seconds

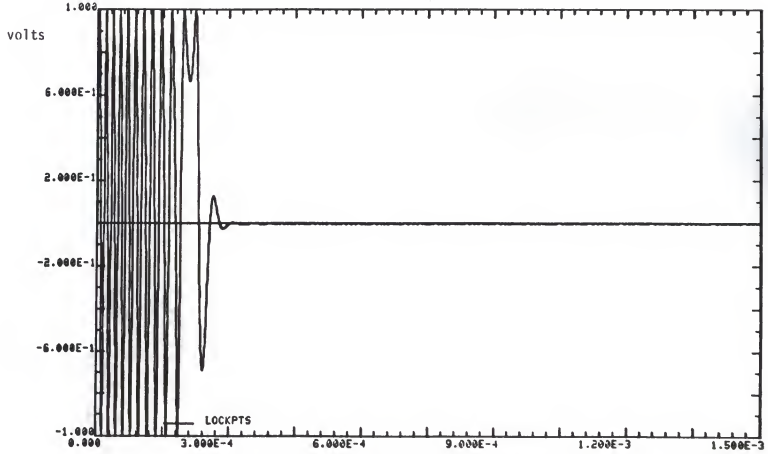


FIGURE 16c) Output of the Phase Detector $\Delta f=4f_n$ ($T_3=.25T_2$) seconds

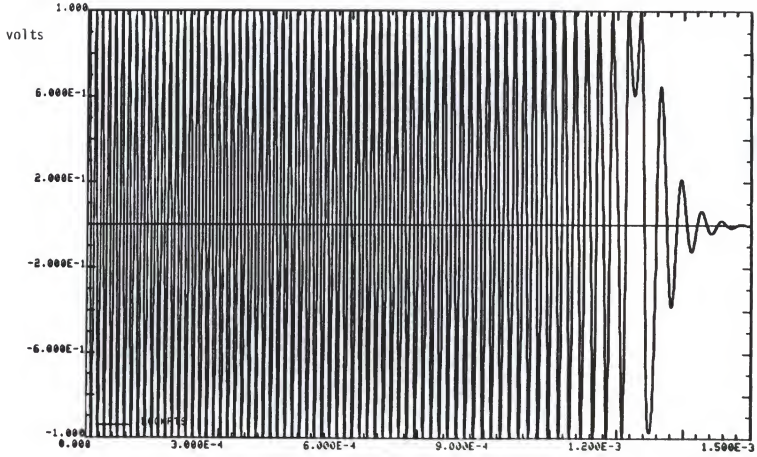


FIGURE 16d) Output of the Phase Detector $\Delta f=4f_n$ $(T_3=.5T_2)$

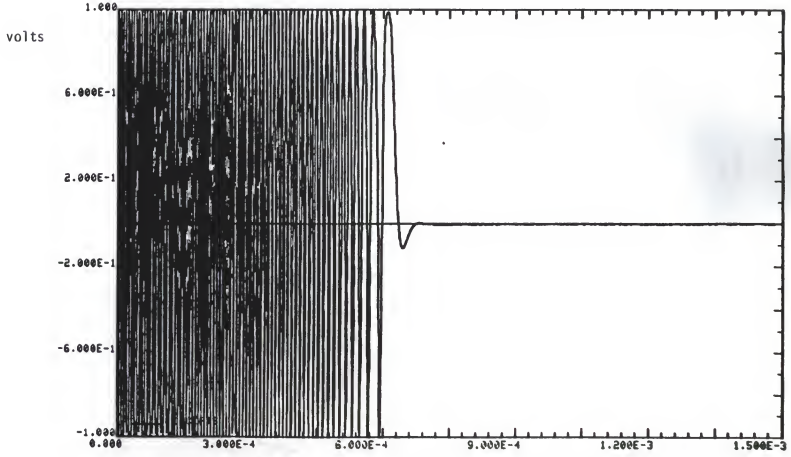


FIGURE 17) Output of the Phase Detector $\Delta f=10f_n$ (T_3=0)

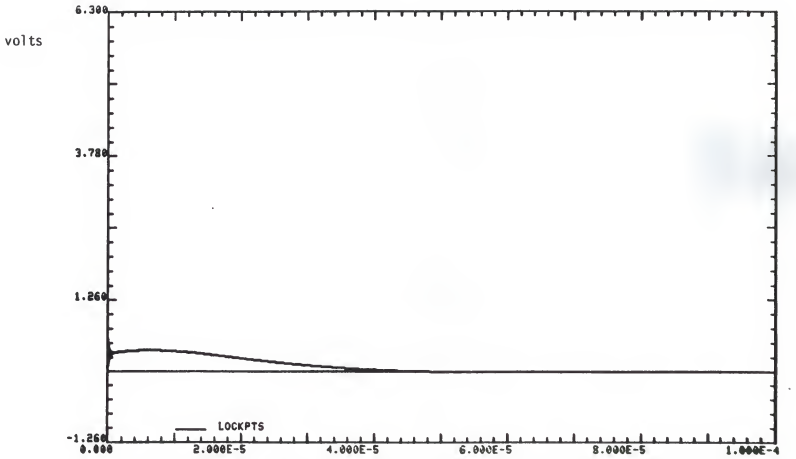


FIGURE 18a) Output of the Phase-Frequency Detector $\Delta f = f_n$ $(T_3 = 0)$

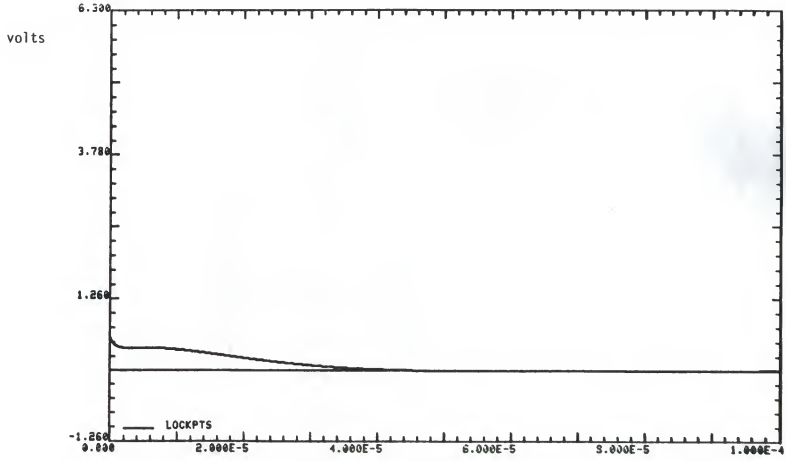


FIGURE 18b) Output of the Phase-Frequency Detector $\Delta f=f_n$ $(T_3=.1T_2)$

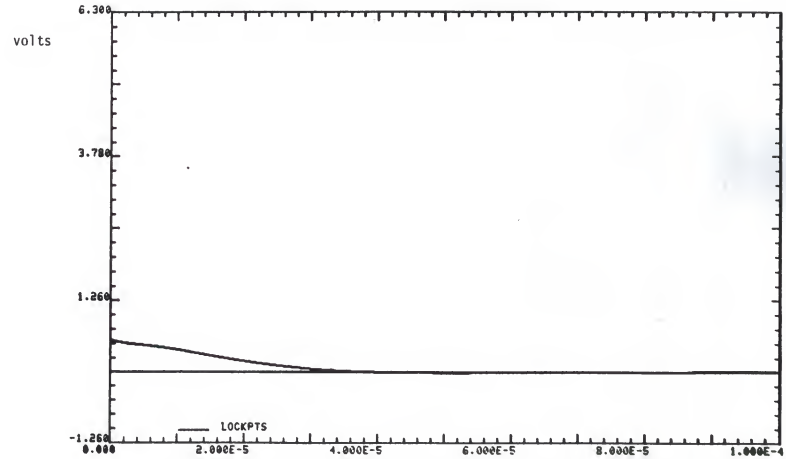


FIGURE 18c) Output of the Phase-Frequency Detector $\Delta f=f_n$ $(T_3=.25T_2)$

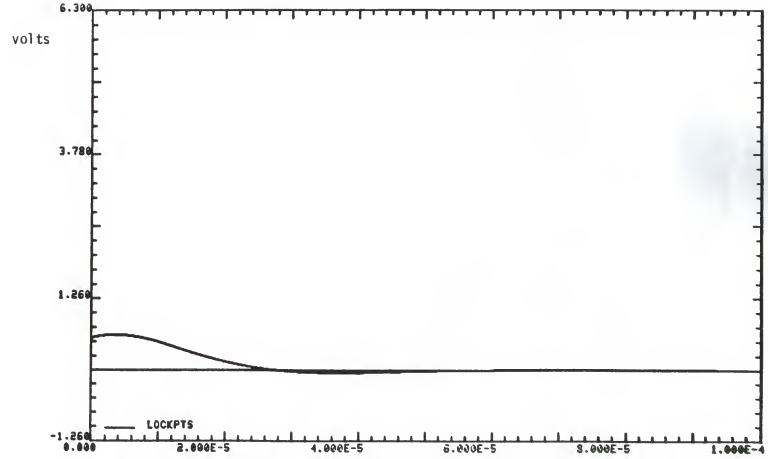


FIGURE 18d) Output of the Phase-Frequency Detector $\Delta f=f_n$ $(T_3=.5T_2)$

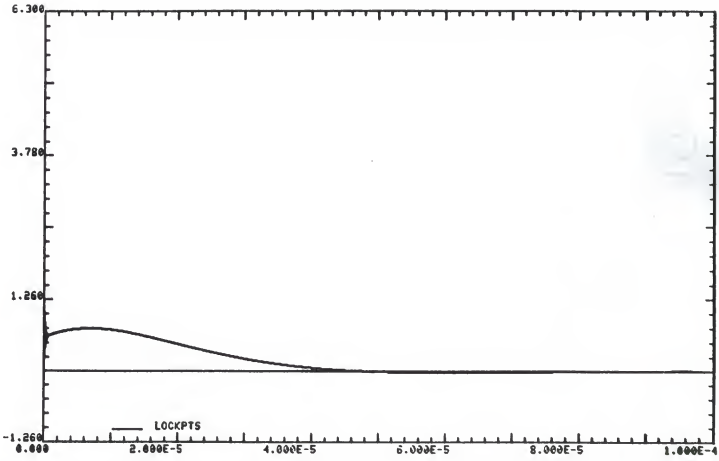


FIGURE 19a) Output of the Phase-Frequency Detector $\Delta f = 2f_n$ (T_3=0)

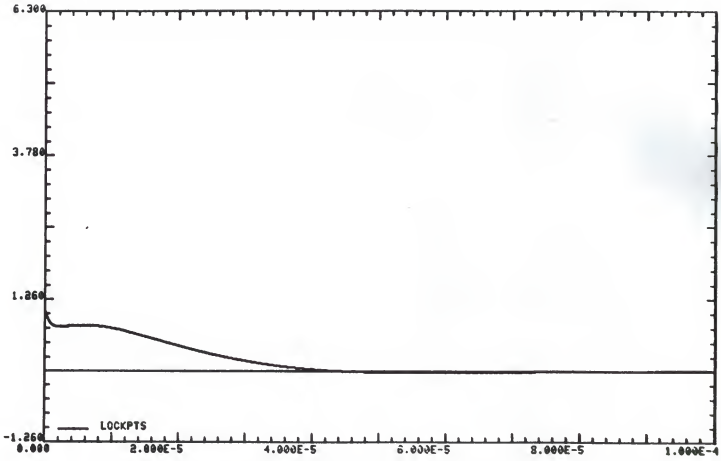


FIGURE 19b) Output of the Phase-Frequency Detector $\Delta f = 2f_n$ $(T_3 = .1T_2)$

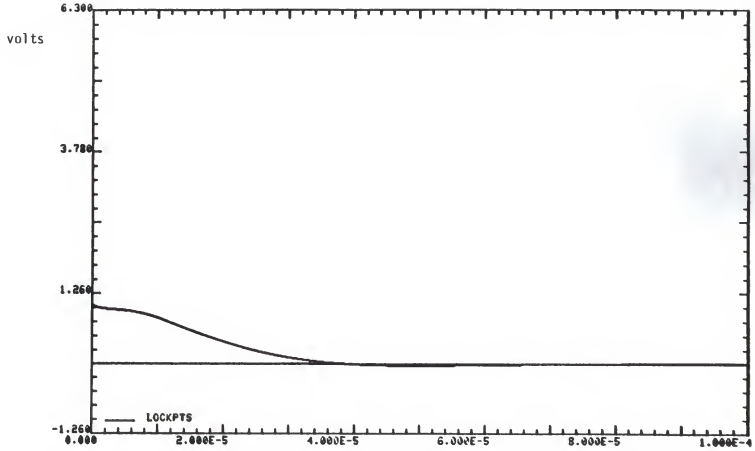


FIGURE 19c) Output of the Phase-Frequency Detector $\Delta f=2f_n$ $(T_3=.25T_2)$

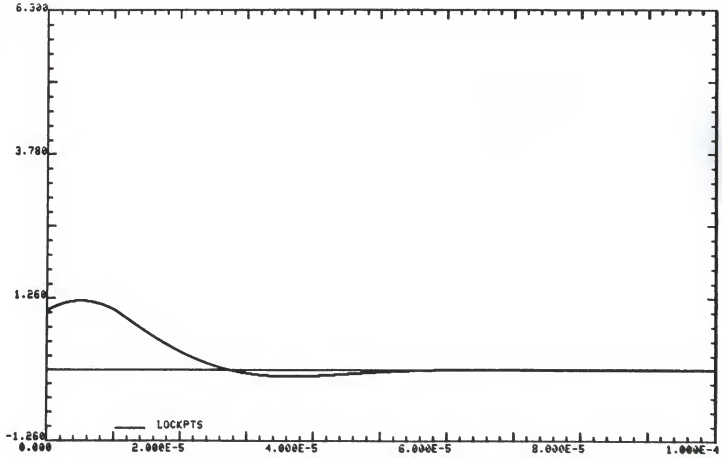


FIGURE 19d) Output of the Phase-Frequency Detector $\Delta f=2f_n$ $(T_3=.5T_2)$ seconds

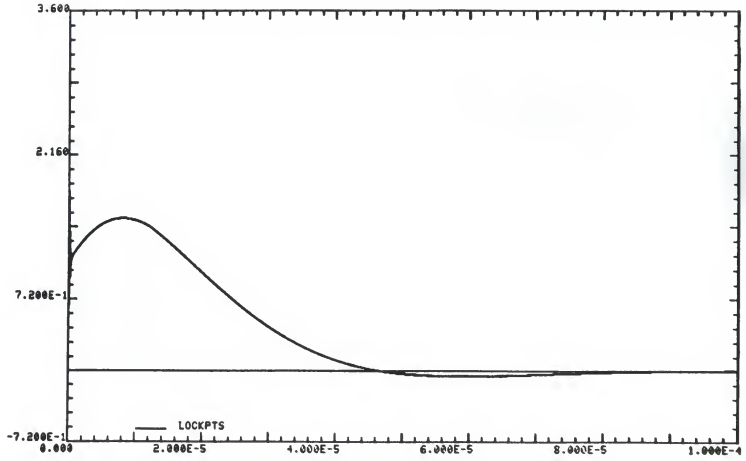


FIGURE 20a) Output of the Phase-Frequency Detector $\Delta f=4f_n$ $(T_3=0)$

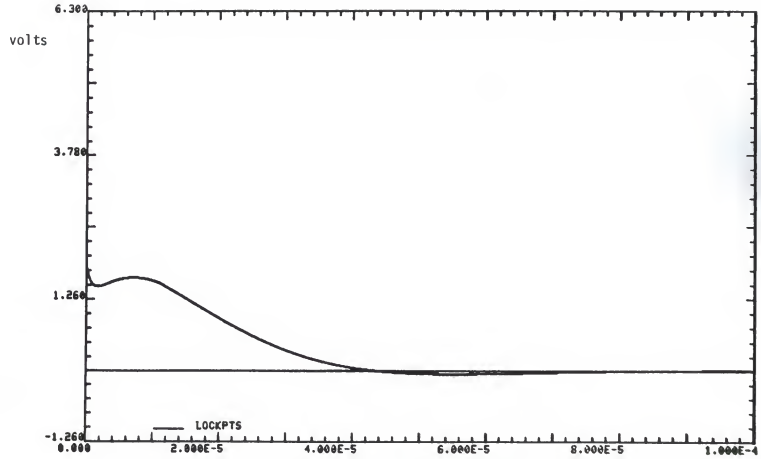


FIGURE 20b) Output of the Phase-Frequency Detector $\Delta f=4f_n$ $(T_3=.1T_2)$

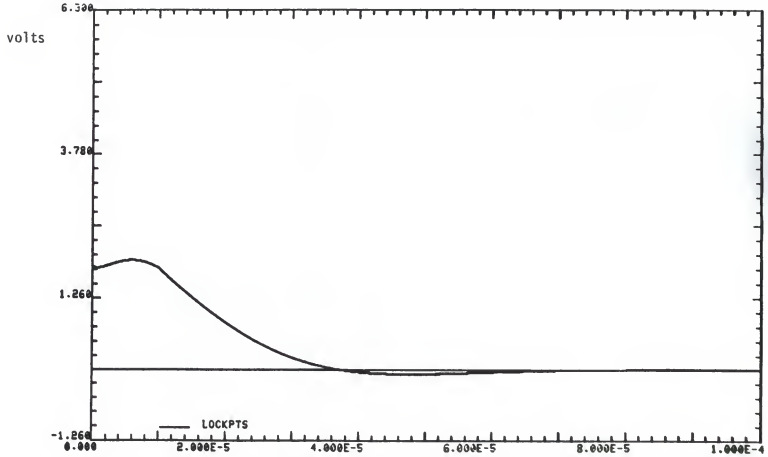


FIGURE 20c) Output of the Phase-Frequency Detector $\Delta f=4f_n$ $(T_3=.25T_2)$

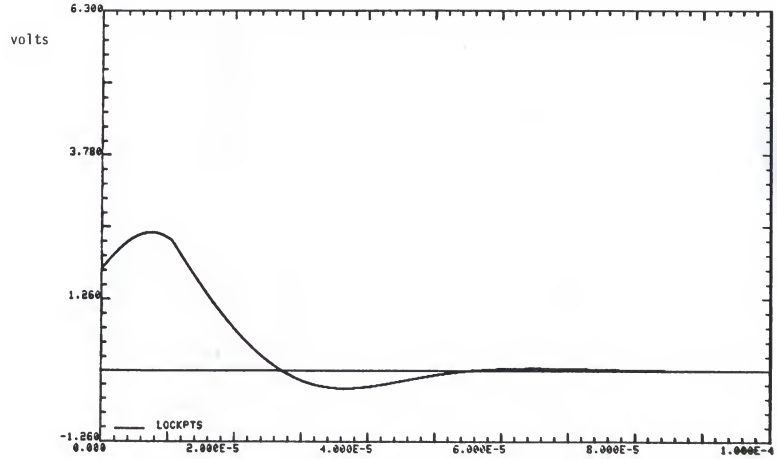


FIGURE 20d) Output of the Phase-Frequency Detector $\Delta f=4f_n$ $(T_3=.5T_2)$

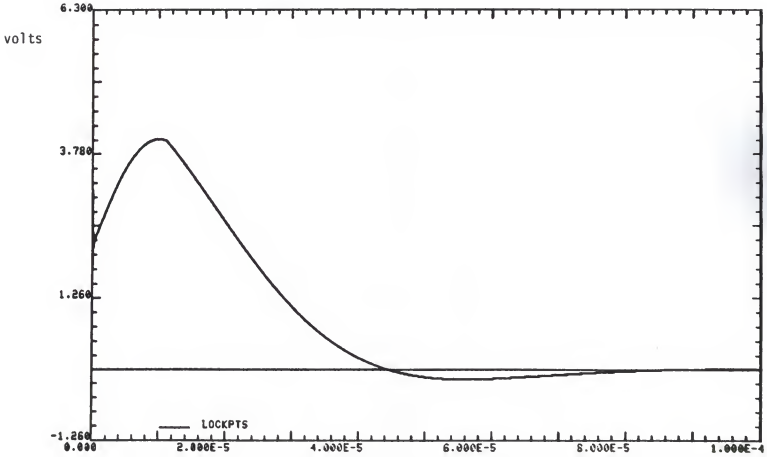


FIGURE 21a) Output of the Phase-Frequency Detector $\Delta f = 10 f_n$ $(T_3 = 0)$

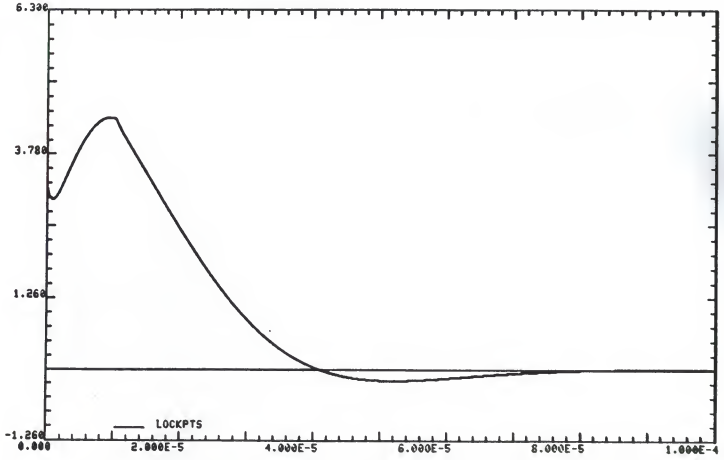


FIGURE 21b) Output of the Phase-Frequency Detector $\Delta f = 10 f_n$ $(T_3 = .1T_2)$

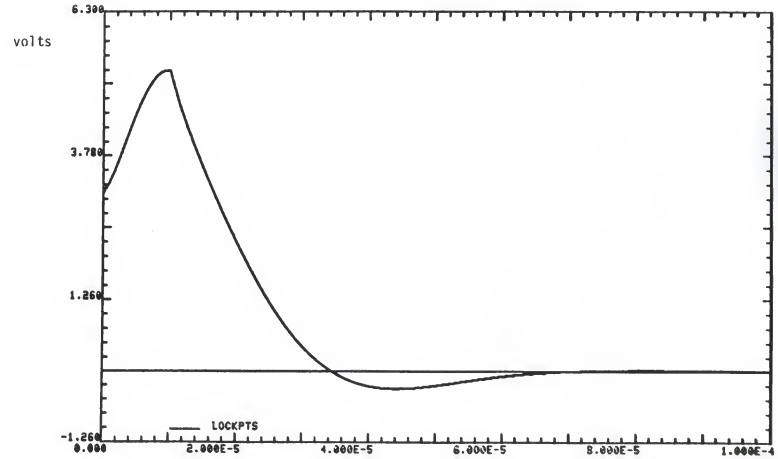


FIGURE 21c) Output of the Phase-Frequency Detector $\Delta f=10f_n$ $(T_3=.25T_2)$ seconds

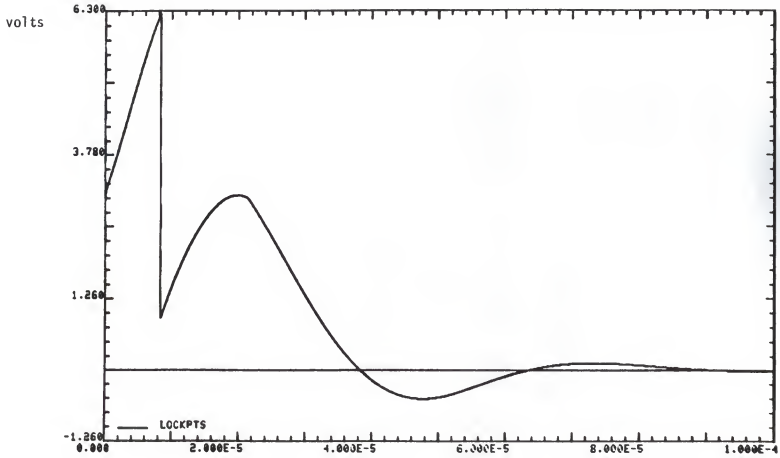


FIGURE 21d) Output of the Phase-Frequency Detector $\Delta f=10f_n$ $(T_3=.5T_2)$ seconds

value of the phase detector output is approximately zero, and its negative incursions tend to slow it down. The phase-frequency detector can have an average value of 50% of full scale (πK_d) even with an offset frequency of only 1 hertz. Additionally, the phase-frequency detector is capable of higher peak voltages given equal values of detector gain, K_d.

The phase-frequency detector is also much less susceptible to factors affecting loop stability--in this case, a third pole approaching the origin. The phase-frequency detector, with its higher peak voltage capability, compensates by increasing its output voltage swing, whereas the phase detector, which in many cases is already outputing voltage peaks at its maximum, may often only compensate by increasing acquisition time.

The computer simulation of Appendix C is capable of providing accurate data so long as a few points are not ignored.

First, with a phase-frequency detector installed, this loop will eventually lock to <u>any</u> finite frequency step. If a very large jump occurs, the phase-frequency detector will output a DC voltage near $2\pi K_d$. The ideal integrators (Figure 11) will, given a long enough period of time, reach high enough values so that the voltage provided to the voltage controlled oscillator will be sufficiently high enough to drive it to its new value. In practice, power supply considerations would dictate a limit as to the allowable error voltages that may be applied to the VCO.

This effect can be easily included in the simulation by placing a ceiling on the allowable output values of the integrators.

Second, this simulation assumes both VCO gain (K_v), and detector gain (K_d) are linear over all frequency ranges concerned (from 180 KHz--the reference input--to 360 KHz for the graphs shown). Any nonlinearities as the frequencies change, would need to be included for a more accurate model.

Computer induced roundoff errors may begin to appear if the simulation is run over long time periods. Steps have been included in the program to reduce these errors (taking advantage of the periodicity of the detectors, and using double precision variables). However it should be noted that the values of the intermediate integrators may not be changed during the program run without disrupting the simulation. Over a long run, as the values in the integrators continue to increase and are continually added to a small relatively decreasing increment, a point will eventually arrive at which the precision deteriorates. Runs of up to 10 msec have been simulated without the above phenommenon becoming evident.

Finally, it should be realized that the plots of the phase-frequency detector error voltages (Figures 18-21) derived from the proposed model are <u>not</u> what one would view if an oscilloscope was connected to an actual phase-frequency detector. Physical observation would reveal positive and negative going pulses at the output of the differential amplifier (Figure 7). However, as the model represents the average value of the detector output, the lock acquisition times shown will be accurate.

IV. CONCLUSIONS

A mathematical model of the behavior of a MC12540 phase-frequency detector has been derived in Section III. This model has been used in a low pass equivalent circuit to simulate the behavior of a PLL during acquisition and tracking modes. Plots of the detector error voltage clearly show that a PLL utilizing a phase-frequency detector acquires frequency and phase lock much faster than a similar PLL using a product type phase detector.

Using the phase frequency detector simulator developed here, lock acquisition times, and the effects of circuit changes to PLL's may be accurately predicted for loops using an MC12540.

V. REFERENCES

1) Motorola MECL Data Book, Motorola, Inc., Phoenix, Arizona, 1982.

2) Ulrich L. Rohde, Digital PLL Frequency Synthesizers, Prentice-Hall, Inc., Englewood Ciffs, New Jersey, 1983.

VI. APPENDICES

APPENDIX A

This computer program was used to predict the state diagram of the MC12540 PF detector.

The user inputs the initial values of R6 and V9. The program will then output the current state of the circuit, return to the start, and ask for the situation after the first change.

```
1 OPEN4,4:CMD4:LIST:PRINT#4:CLOSE4
10 A=1:B=1
20 INPUT"R6,V9";R6,V9
30 A=NOT(R6 OR U4)AND 1
40 B=NOT(V9 OR D1)AND 1
70 IFA=0 AND F=1 THEN D=1
80 IFA=1 AND F=0 THEN D=0
90 IFA=1 AND F=1 THEN D=INT(RND(0)+.5)
100 IFB=1 AND F=1 THEN C=INT(RND(0)+.5)
110 IFB=1 AND F=0 THEN C=0
120 IFB=0 AND F=1 THEN C=1
130 F=NOT(A OR B OR C OR D)AND 1
140 U4=NOT(A OR D OR F)AND 1
150 D1=NOT(B OR C OR F)AND 1
160 IFAT=A AND BT=B AND CT=C AND DT=D AND FT=F AND UT=U4 AND RT=D1 THEN 180
170 AT=A:BT=B:CT=C:DT=D:FT=F:UT=U4:RT=D1:GOTO30
180 U0=U4+U0:D0=D1+D0:N=N+1
190 PRINT"STATE"R6+8+V9*4+U4*2+D1;"*"A;B;C;D;F:GOTO20
```

APPENDIX B

This program is designed to precisely model the circuit of Figure 7.

The input (f_2) at V9 has a frequency of 1 KHz and a 100 step cycle. By varying the number of steps of the input at R6, its input frequency -- equal to:

(100 steps/cycle)(1000 cycles/sec)/(# of steps at R6)

can be user selected. The initial state of the MC12540, and the phase lag twixt the two inputs, are randomly selected. The computer then begins iterating, switching the inputs (R6 and V9) at the appropriate times. The output of the PF detector is fed to an ideal Differential Amplifier (line 190) which outputs a +10, 0, or -10 voltage depending upon the output of the detector. The differential amp output is then fed to a low pass filter (200-230). After an appropriate 'settle down' time--in case the initial randomly chosen state is in the wrong place--the output is monitored and the high and low values stored (lines 250 and 260).

So long as the input square waves 'slide across' each other so that the phase delay between the two varies over 2π, accurate readings of the sawtooth peaks can be obtained. Choosing a multiple of 100 or a number that divides into 100 without a remainder (such as 50) will 'freeze' the phase difference to that initially selected by the computer, and result in misleading data.

```
6 M=1:LP=5:HP=-5
8 DIMS(12),R(12),V(12),U(12),D(12),AA(12),BB(12),CC(12),DD(12),FF(12)
10 DIM RS(1000),VS(1000),US(1000),DS(1000),IO(1000)
12 FORJ=1TO12:READS(J),R(J),V(J),U(J),D(J),AA(J),BB(J),CC(J),DD(J),FF(J):NEXT
13 REM PICK INITIAL STATE AT RANDOM
14 SS=INT(RND(0)*12)+1
16 S1=S(SS):R6=R(SS):V9=V(SS):U4=U(SS):D1=D(SS):A=AA(SS):B=BB(SS):C=CC(SS)
18 D=DD(SS):F=FF(SS)
20 PRINT"NUMBER OF STEPS OF R6 INPUT----100 STEPS IS ONE CYCLE OF V9"
22 INPUT NS:PRINT"THE R6 INPUT (F1) HAS A FREQUENCY OF  "1E+05/NS" HERTZ"
24 N2=NS/2:PD=INT(RND(0)*N2)+1:PRINT"PHASE LAG= "PD" STEPS"
39 IFF2=50THENF2=0:V9=NOT(V9) AND 1:SK=1
40 IFF1=PDTHEN R6=NOT(R6)AND 1:PD=1000*PD:F1=0:SK=1
45 IFF1=N2THEN R6=NOT(R6)AND 1:F1=0:SK=1
47 IF SK=1THENSK=0:GOTO50
48 GOTO180
50 A=NOT(R6 OR U4)AND 1
60 B=NOT(V9 OR D1)AND 1
70 IFA=0 AND F=1 THEN D=1
80 IFA=1 AND F=0 THEN D=0
90 IFA=1 AND F=1 THEN D=INT(RND(0)+.5)
100 IFB=1 AND F=1 THEN C=1NT(RND(0)+.5)
110 IFB=1 AND F=0 THEN C=0
120 IFB=0 AND F=1 THEN C=1
130 F=NOT(A OR B OR C OR D)AND 1
140 U4=NOT(A OR D OR F)AND 1
150 D1=NOT(B OR C OR F)AND 1
160 IFAT=A AND BT=B AND CT=C AND DT=D AND FT=F AND UT=U4 AND RT=D1 THEN 180
170 AT=A:BT=B:CT=C:DT=D:FT=F:UT=U4:RT=D1:GOTO50
180 N=N+1:F1=F1+1:F2=F2+1
185 REM INTEGRATOR SIMULATION
190 V1=D1*10-U4*10
200 AK=VI-9.5*BL
210 BK=AL*10E-6+BL
220 VO=BK*488.3
230 AL=AK:BL=BK
240 UO=UO+U4:DO=DO+D1
250 IFN>1500AND VO>HPTHENHP=VO
260 IFN>1500AND VO<LPTHENLP=VO
270 GETL$:IFL$="("?)"THEN GOSUB7000
275 VA=VA+VO:REM USE TO FIND V.AVE
280 TE=N/100
286 IFTE=INT(TE)THENIO(M)=VO:PRINTM;UO;DO;VO:M=M+1
288 IFN=100000THENGOSUB7000
290 GOTO39
```

```
5000 DATA 0,0,0,0,0,1,1,0,0,0
5010 DATA 1,0,0,0,1,1,1,0,0,0
5020 DATA 2,0,0,1,0,0,1,1,0,0
5030 DATA 4,0,1,0,0,1,0,1,1,0
5040 DATA 5,0,1,0,1,1,1,0,0,0
5050 DATA 6,0,1,1,1,0,0,0,1,0
5060 DATA 8,1,0,0,0,0,1,0,1,0
5070 DATA 9,1,0,0,1,0,0,0,1,0
5075 DATA 10,1,0,1,1,0,0,1,0,0,0
5080 DATA 12,1,1,0,0,0,0,1,1,0
5090 DATA 13,1,1,0,1,1,0,0,0,1,0
5100 DATA 14,1,1,1,0,0,0,1,0,0
7000 GETG$:IFG$<>""(??)"THEN7000
7010 FORA3=1TO10000:PRINTA3;IO(A3):NEXT
7015 IFN=100000THENEND
7020 RETURN
```

APPENDIX C

This program simulates a high frequency PLL via its low pass equivalent circuit.

The system under test starts in an ideal phase and frequency locked condition. The perfect phase matchup between the VCO and the reference input results in no corrective output voltage from the phase or phase-frequency detector. As a result, all the integrators of Figure 11 have zero values.

The reference frequency (line 40) is at 180 KHz unless another value is desired.

After the user selects the type of detector, the frequency step at t=0, and the value of the time constant, T_3, the required sampling interval is calculated (around line 680). The smallest of the following becomes the sampling interval T_s:

1. runlength/4000 sample points
2. .1/frequency offset (this insures a minimum of 10 samples per cycle—well above the Nyquist rate--are taken)
3. a value ten times smaller than the T_3 time constant
4. a value 100 times smaller than the T_2 time constant.

Number 3 is important because $1/T_3$ is the feedback gain of filter 1 (see Figure 11). If the feedback is too large, the incoming error voltage will be completely obliterated, resulting in Z(s) alternately becoming a large negative and larger positive number each iteration.

Check number 4 establishes the maximum allowable sampling interval, sufficiently small to insure the $1/T_1$ gain in filter 2 does not cause any wild swings.

Line 800 calculates the ratio of:

(reference freq. at t=0+)/[(VCO freq. at t=0-)+(any changes to VCO freq.)] in other words, f_2/f_1. The value of the DC voltage 'black box' (see Figure 1) is then calculated.

The sawtooth waveform of Figure 6 is periodic over 2π. The sawtooth alogrithm operates over a $\pm 2\pi$ range (the darker part of Figure 6). The phase difference is divided by 2π to yield a number (S1) which represents the number of revolutions the phase difference has advanced (line 855). If the phase difference has advanced past 2π, it is reduced by 2π. S1 (at this point always less that $|1|$), is then multiplied by $2\pi K_d$ to yield the value of the sawtooth under coherent (frequency locked) conditions. If frequency lock has not yet been achieved, the sawtooth value is decreased proportionally to the frequency ratio (line 990). The PF detector error output, which is the sum of the DC term and the sawtooth term, is then calculated (line 1010) and applied to the remainder of the PLL.

After processing by the filters and the VCO (compare Figure 11 with page 65, BL, CL, and YL are values of BK(s), CK(s), and YK(s) respectively, one turn ago) the current VCO frequency offset from time t=0 is calculated via the equations:

$$\Delta\hat{f} = \frac{\Delta\hat{\theta}}{2\pi\Delta t} = \frac{\hat{\theta}_n - \hat{\theta}_{n-1}}{2\pi\ T_s} \tag{4}$$

If the VCO phase has advanced past 10π it is shifted to zero, and the reference input also reduced accordingly. A(s) is not affected by this operation, which is designed to keep the phase values manageable so roundoff error will not affect line 780.

At any point in the simulation $\hat{\theta}_n(s) = \hat{\theta}_{n-1}(s) + \Delta\hat{\theta}_{n-1}$ where $\Delta\hat{\theta}_{n-1} = K_v T_s J K_{n-1}(s)$. If at iteration n, $\hat{\theta}_n(s)$ is reduced to zero, the value of

$\hat{\theta}_{n+1}(s)$ at the next iteration is computed by $\hat{\theta}_{n+1}(s) = \hat{\theta}_n(s) + \Delta\hat{\theta}_n(s) = \Delta\hat{\theta}_n(s)$. The value of the integrator at CK(s) must be reduced accordingly (see line before 1140).

```
C
C
C
      DIMENSION ES(4000)
      REAL KO,KV,KD,K2,K
      DOUBLE PRECISION REFIN,JK,YL,BL,CL,YK,BK,CK
C
C
      REFIN=0.
      T=0.
      THETAHAT=0.
      DH=0.
      A=0.
      AL=0.
      TT=0.
      BL=0.
      CL=0.
      DL=0.
      YL=0.
      TL=0.
      P2=2.*3.1415927
      SI=1.
      T1=9.824E-04
      T2=1.25E-05
      K2=2.E+06
      KV=P2*K2
      TEMP1=P2*5.
      B1=KV/T1
      N=1
      K=1
      YM=P2
      NN=1
C
C
40    TYPE *'INPUT REFERANCE FREQUENCY AT T=0-'
      TYPE *'ENTER A '0' FOR 180KHZ REFERANCE, OR.......'
      TYPE *'ENTER A '1' FOR SOMETHING DIFFERANT'
      ACCEPT IREF
      IF(IREF.GT.1.OR.IREF.LT.0)GOTO40
      IF(IREF.EQ.1)GOTO45
      FR=180000.
      GOTO50
45    TYPE* '
      TYPE*'ENTER DESIRED REFERANCE (I VCO) FREQUENCY'
      ACCEPT FR
50    FR=FR
      TYPE*'PHASE (1) OR PHASE-FREQUENCY (2) DETECTOR DESIRED'
      ACCEPT DT
      IF(DT.NE.1..AND.DT.NE.2.)GOTO50
185   TYPE*'INPUT FREQUENCY STEP AT T=0-'
      ACCEPT DF
      IF(DF.LT.-FR)GOTO185
      FR=FR+DF
      TYPE*'ENTER VALUE OF T3 IN TERMS OF THE RATIO OF T3/T2'
      TYPE*  A '0' IMPLIES NO T3'
      TYPE*  A VALUE <1 IMPLIES T3'S ROOT LIES TO THE LEFT OF T2'S'
      TYPE*  A VALUE >1 IMPLIES T3'S ROOT LIES TO THE RIGHT OF T2'S'
570   ACCEPT RT
      IF(RT.LT.0.)GOTO570
      T3=T2*RT
650   W=DF*P2
C
C
C
C
```

```
C
C
C
C
C
C
C       CALCULATE CORRECT SAMPLING INTERVAL BASED ON VALUE OF
C       OF FREQUENCY STEP (DF), T2'S ZERO, AND T3'S POLE.
C       4000 SAMPLE POINTS ARE TO BE STORED AND PLOTTED.
C
        TV=.1
        TYPE*INPUT DESIRED LENGTH OF RUN IN SECONDS*
        ACCEPT RL
680     TS=RL/4000.
        D2=ABS(TV/DF)
        IF(D2.LT.TS)N=TS/D2+1.
        IF(D2.LT.TS)TS=D2
        IF(T3.GT.(2.*TS).OR.T3.EQ.0.)GOTO748
        TS=T3/10.
        N=RL/TS/4000.+1.
        TYPE' '
748     IF(TS.LT.1.25E-07)GOTO750
        TS=1.25E-07
        N=RL/TS/4000.+1.
C
C
750     TYPE*SAMPLING INTERVAL IS*,TS
        TYPE*WHAT IS LOWER THAN F. REFERANCE BY*,DF,*HERTZ*
760     TYPE*THERE ARE*,N,*   SAMPLES PER POINT*
        B2=1./TS/P2
C
C
C       SIMULATION COMMENCES HERE
C
C
770     DO 1150 J=1,N
780     IF(K.GT.1)REFIN=REFIN+W*TS
790     A=REFIN-THETAHAT
        IF(DT.EQ.1.)GOTO850
C
C       CALCULATE VALUE OF DC TERM
C
800     FF=FR/(FM+DM)
810     IF(FF.LT.1.)GOTO840
        VD=(1.-1./FF)*VM
        GOTO850
840     VD=-(1-FF)*VM                                          .
C
        SAWTOOTH ALGORITHM: THE PHASE DIFFERENCES ARE KEPT
C       WITHIN +- 2PI HERE

850     TT=A-AL+TT
855     S1=TT/P2
        IF(S1.LT.0.)S1=-1.
        RV=INT(S1*S1)
        IF(RV.LT.1)GOTO885
        TT=TT-S1*P2
        GOTO855
885     IF(DT.EQ.2.)GOTO890
        ER=SIN(TT)
        GOTO940
890     UU=S1*VM
C
C
C
C
```

```
C
C
C
960     SI=1.
        AL=A
        IF(DT.EQ.1.)GOTO1012
990     IF(FF.GT.1.)OU=OU/FF
        IF(FF.LT.1.)OU=OU*FF
1010    ER=OU+VD
C
C       INTEGRATION SIMULATION STARTS HERE
C
1012    IF(RT.EQ.0.)GOTO1019
        Z=ER-YL/T3
        YK=YL+Z*TS
        GS=YL/T3
        GOTO1020
1019    GS=ER
1020    BK=GS*TS+BL
        JK=(BL+T2*GS)/T1
        CK=CL+TS*JK
        THETAHAT=CL*KV
        DH=(THETAHAT-TL)*B2
        BL=BK
        CL=CK
        YL=YK
        T=TS*K
        K=K+1
C
C       MODIFY VALUES OF THETA TO MINIMIZE ROUND-OFF ERROR
C
        IF(ABS(THETAHAT).LT.TEMP1)GOTO1140
        TOTAL=THETAHAT
        THETAHAT=0.
        REFIN=REFIN-TOTAL
        CL=JK*TS
1140    TL=THETAHAT
        IF(NU.EQ.1)GOTO1160
1150    CONTINUE
C
C
C       OUTPUT
C
C
1160    ES(NU)=ER
        NU=NU+1
        IF(NU.GT.4000)GOTO1200
        GOTO170
1200    TYPE*,'TIME OF RUN =',T
        TYPE*,'ERROR AT ABOVE TIME IS',ES(4000)
        CALL OPEN(3,'LOCKPTS.',3,16000,IERR)
        CALL WRITRW(3,1,ES,1,IERR)
        CALL CLOSE(3,IERR)
        END
```

APPENDIX D

This program finds the closed loop power response $s_\theta(f)$. The spectrum of the input signal is flat with magnitude 1.

The user selects the value for the constant T_3 and the desired portion of the spectrum to observe. The program uses the closed loop response, which is of the form:

$$\frac{\hat{\theta}(jw)}{\theta(jw)} = \frac{jw\,\frac{K_v T_2}{T_1} + \frac{K_v}{T_1}}{(jw)^3 T_3 + (jw)^2 + \frac{K_v T_2}{T_1} + \frac{K_v}{T_1}}$$

by squaring and determining the magnitudes of the numerator and denominator. The quotient of the two yields the value of the power spectrum at the particular frequency.

```
C
C
C       MAGNITUDE/PHASE RESPONSE OF PLL V.6
        INTEGER DF
        REAL MAG(3000)
        REAL LFB,KD,KV,KO,MNU,MDN,K
        COMPLEX NU,DN, CMPLX, S
        T1=9.824E-04
        T2=1.25E-05
        KV=2.*3.14159*2.E+06
        TYPE'ENTER VALUE OF T3 IN TERMS OF THE RATIO OF T3/T2'
        TYPE'A '0' IMPLIES NO T3'
        TYPE'A VALUE <1 IMPLIES T3'S ROOT LIES TO THE LEFT OF T2'S'
        TYPE'A VALUE >1 IMPLIES T3'S ROOT LIES TO THE RIGHT OF T2'S'
10      ACCEPT RT
        IF(RT.LT.0.)GOTO10
        T3=T2*RT
        TYPE'T3 =',T3
22      TYPE'INPUT LOW FREQUENCY BOUNDARY'
        ACCEPT LFB
        TYPE'INPUT HIGH FREQUENCY BOUNDARY'
        ACCEPT HFB
        DF=(HFB-LFB)/3000.
25      K=KV/T1
        A1N=K*T2
        A1D=A1N
        F=LFB
        N=0
30      W=F*2.*3.14159
        N=N+1
        S=CMPLX(0.,W)
        NU=(S*A1N+K)**2
        MNU=SQRT(REAL(NU)**2+AIMAG(NU)**2)
        DN=(T3*S**3+S**2+A1D*S+K)**2
        MDN=SQRT(REAL(DN)**2+AIMAG(DN)**2)
        MAG(N)=MNU/MDN
        F=F+DF
        IF(N.EQ.1)TYPE MAG(1),MNU,MDN
        IF(N.EQ.1000)TYPE MAG(1000)
        IF(N.LT.3000)GOTO30
        CALL OPEN(3,'PLLPLOT.*',3,12000,IERR)
        CALL WRITRW(3,1,MAG,1,IERR)
        CALL CLOSE(3,IERR)
        END
```

SIMULATION OF PHASE-LOCKED LOOPS WHICH USE A PHASE-FREQUENCY DETECTOR

by

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B. S., United States Military Academy, 1975

AN ABSTRACT OF A MASTER'S THESIS

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ABSTRACT

A model is developed for the phase-frequency detector commonly used in phase-locked frequency synthesizers. The model is based on both analytical and experimental results obtained for the Motorola MC-12540 integrated circuit detector.

This thesis presents the supporting arguments which lead to the mathematical model and shows the results obtained when the model is used in a computer simulation of a phase-locked loop (PLL). The examples given show a comparison of the acquisition and tracking characteristics of a PLL which uses a phase-frequency detector with those of a PLL which uses a conventional product type phase detector.