THEORY AND APPLICATIONS OF FIELD-EFFECT TRANSISTORS

by 149

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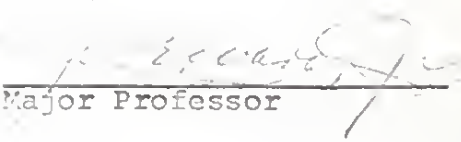

Major Professor

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INTRODUCTION

In 1952, shortly after the invention of the junction transistor, Shockley (18) described theoretically a new active device based on the modulation of a majority-carrier current. The principle of operation of this device, which he termed a unipolar field-effect transistor, is radically different from that of the junction transistor in that the majority - rather than minority-carrier current is modulated by altering the width of a conducting channel through the narrowing or widening of a p-n junction depletion layer. At that time, probably the principle attraction of this device over the junction transistor was the high input impedance of the control electrode, which behaves essentially as a reverse-biased p-n junction. However, the difficulties of making the device with the techniques then available were considerable, and, although both silicon and germanium (7) devices were described shortly after Shockley's paper was published, the device in its practical form did not appear very attractive. It was not until the techniques of masking, diffusion and epitaxial growth using silicon were sufficiently developed that field-effect devices could be manufactured with a reasonable degree of reproducibility and with characteristics which offered considerable advantages over the junction transistor for certain applications. In fact, it is only in the last few years that the devices have become readily available through commercial channels.

The theory of the device, as originally formulated by Shockley, can be considered as a first-order theory. It assumed an abrupt p-n junction with a uniformly graded channel along which the change in potential is gradual enough to allow the use of the charge-neutrality condition. Furthermore, Shockley assumed that the carrier mobility was independent of the electric field. Dacey and Ross (7) modified this theory to include the effects of variable mobility. In addition, they considered in some detail the high-frequency performance of the device. By comparison with experimental measurements on transistors constructed by the alloy process, they showed that the general features of the d-c characteristics of some units were adequately explained by the first-order theory of Shockley, while for others some modified theory was necessary.

Modern field-effect transistors (FET) are constructed by methods which result in junctions of both the abrupt and graded types. Recently there has been renewed interest in the solid-state field in both the conventional junction field-effect transistor and in the more recently developed surface or metal-oxide-semiconductor (MOS) device.

While the details of carrier motion and control are different for the several types of field-effect devices, basic equations describing all types of devices have the same mathematical form and can thus be treated in a unified approach. The purpose of this report is to discuss and solve a gener-

alized model of an abrupt junction field-effect transistor by developing the basic relations among its parameters. An attempt is also made to present its most important features as an active device by including device application.

CONSTRUCTION OF FIELD-EFFECT TRANSISTORS

In order to compare the performance of a practical field-effect transistor with theoretical predictions, it is necessary to assume a suitable structural model. Such a model and an assessment of its validity can be best obtained by considering the methods by which the devices are made.

The techniques of alloying, diffusion and epitaxial growth, or combinations thereof, can be used for device fabrication. This discussion will be restricted to the diffusion processes, since it and the epitaxial process enable the best control over impurity density and dimensions to be obtained.

The structure illustrated in Fig. 1 can be achieved by using double-diffusion techniques similar to those employed in making silicon n-p-n transistors. Either simultaneous or sequential double diffusion can be used. If sequential diffusion is employed, a suitable acceptor impurity is first diffused into an n-type silicon slice, producing a p-type layer. A "photoresist" procedure is then used to produce a silicon-oxide mask over all the surface, except where it is desired to produce a channel. Diffusion of donor impurities then converts the selected region of the p-layer into an n-type gate, the depth of which is controlled by the diffusion time and temperature. The doping profile that may be expected to result from such a procedure is shown in Fig. 2.

Another technique (15) which can yield field-effect transistors with a high transconductance and cutoff frequency

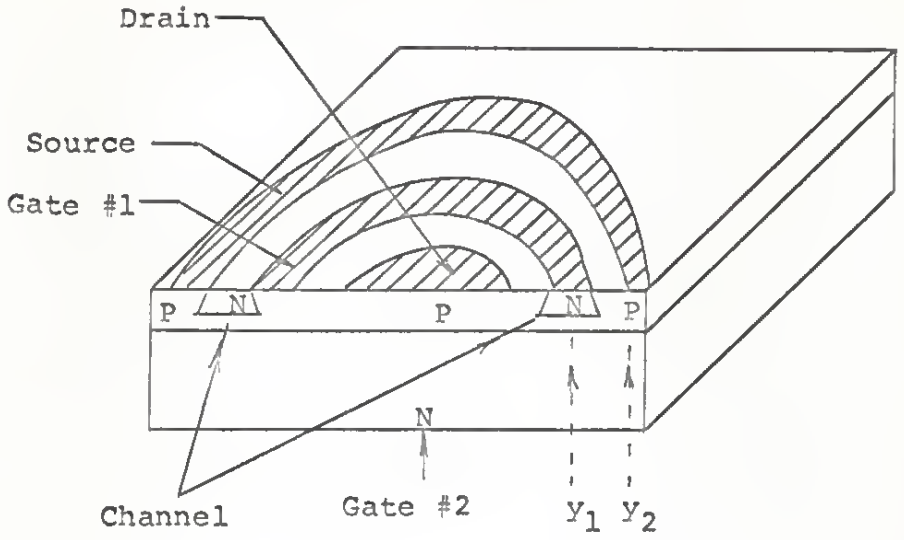


Fig. 1. Construction of a double-diffused transistor. The p channel is formed by diffusing acceptors into the n substrate, which forms the second gate. A second diffusion through the masked surface forms gate 1.

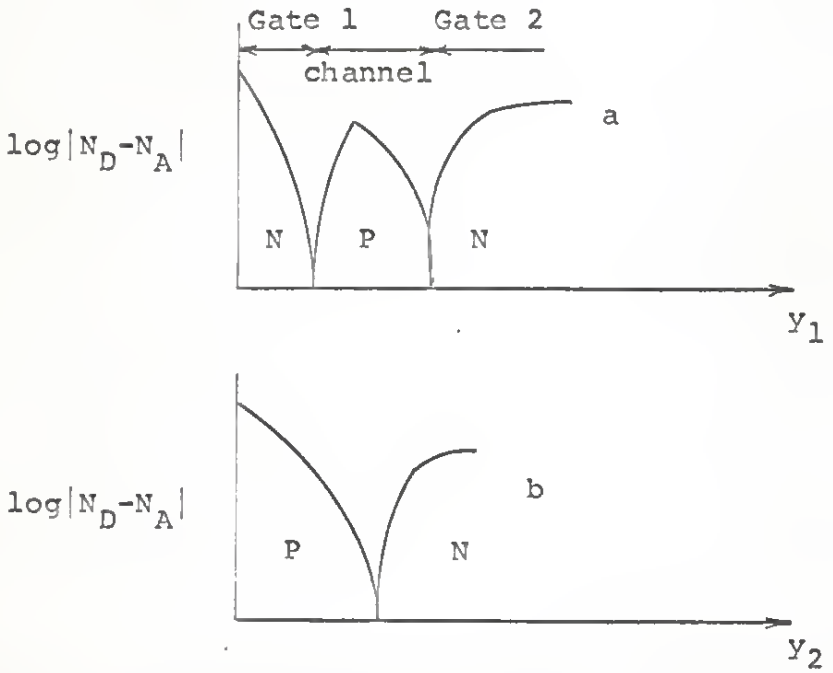


Fig. 2. Approximate form of the doping profile for the double-diffused structure shown in Fig. 1. Net impurity density: a Along y_1; b Along y_2.

utilizes the fact that diffusion can occur laterally beneath a masked area to produce a channel region. The junctions of this structure are diffused, and it might be expected that, since both gate regions are of the same resistivity, this device should exhibit symmetrical gate characteristics (9).

THE FIELD-EFFECT TRANSISTOR

Illustrated in Fig. 3 is an example of a junction gate field-effect transistor. It is shown to be a three terminal device formed by introducing two n-type impurities into opposite sides of the p-type material. The two n-type regions are shown to be electrically connected and form the gate (grid) terminal. The interesting part of the field-effect transistor is the region between the two junctions which is called the conductive channel. The conductive channel is provided with two ohmic contacts, one acting as the source (cathode) and the other as the drain (anode) with an appropriate voltage (drain voltage) applied between drain and source terminals. If the impurity concentration in the n-regions is purposely made much higher than that of the p-region, then a space-charge layer due to the external bias V_{GG} will extend almost entirely into the channel between junctions, thus controlling the thickness of the channel. If the bias potential at the source and drain differ, then under operating conditions there will be a narrowing of the channel at the terminal that has the larger potential.

In a field-effect transistor, the current flow is carried by one type of carrier only. The changed conductance of the field-effect transistor input and output terminals results from changing numbers of carriers of this one type. For this reason the field-effect transistor is some times refered to as a "unipolar transistor".

It is perhaps well to point out at this point that the field-effect transistor of Fig. 3 is in some ways analogous to a vacuum tube. Suppose that it be imagined that a small time varying signal is applied between source and gate terminals, then the effect will be to widen and narrow the channel which carries current between source and drain terminals. This is closely analogous to the action of a grid which controls the current flow between cathode and plate.

If in Fig. 3 the impurities diffuse through the p-region in a plane parallel to the n-regions, then the conductance of the channel can be calculated from the following expression:

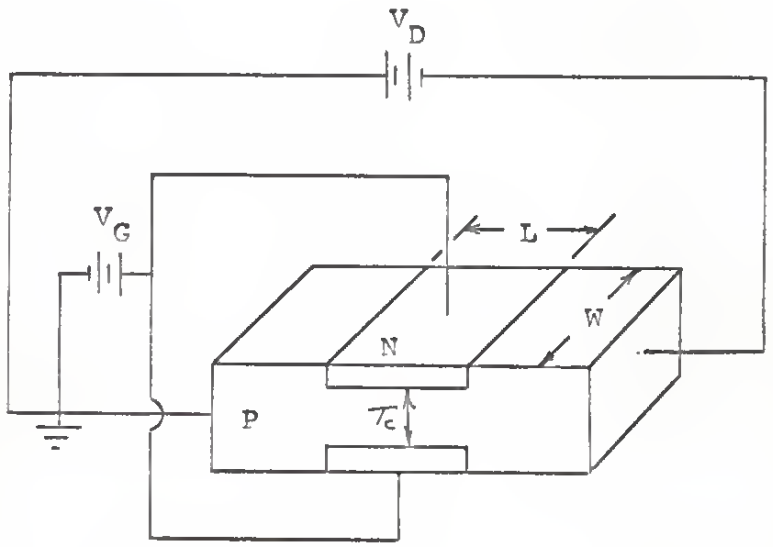


Fig. 3. The field-effect transistor.

$$G = \frac{\mu q W}{L} \int_0^{T_c} p(y)\,dy \qquad (1)$$

where p = the impurity density in the p-region $(N_A - N_D)$.

q = the electronic charge.

μ = carrier drift mobility.

Referring to equation (1), it is seen that the conductance between source and drain terminals depends on the effective channel thickness T_c. The effective channel thickness is entirely determined by the region between p-n junctions not depleted of free carriers by the reverse bias junction gate voltage. Thus, it is easy to see how the applied voltage V_G controls the conductance of the semiconductor body.

FIELD-EFFECT TRANSISTOR THEORY

A mathematical representation of field-effect transistors provides a basis for predicting transistor performance and the influence of various design and material parameters. Published analyses (18) and (7) have been limited to specific device geometries and impurity distributions.

The solutions of the field-effect transistor equations presented here are general in that both the free carrier density and space-charge density may vary arbitrarily with distance from the gate junction (1). However the solutions are limited to cases where the one dimensional Poisson-equations can be employed in rectangular form. The gradual approximation originated by Shockley (18) is employed. Solutions based on this approximation have been shown to agree favorably with experimental results (7). Many of the relationships derived here have been previously noted in analyses of specific impurity distributions. However, this report will show that many of these relationships are independent of distribution.

The amplifying properties of a field-effect transistor are best characterized by its mutual transconductance. Both mutual transconductance and output current approach constant maximum values (g_m and I_p) when the output terminal voltage reaches a particular value V_p. The value of V_p also represents the magnitude of the input terminal voltage required to reduce the output current to zero. In the following sections general expressions for mutual transconductance, output transconductance, junction

capacitance, and current amplification are derived as functions of the depletion layer thickness at the device boundaries. These expressions are not explicitly dependent on charge distribution (1).

The Conductive Channel

The physical structure for this analysis is illustrated in Fig. 4. Note that only the lower half p-n junction of the field-effect transistor of Fig. 3 is shown. Also, only the active channel is shown in Fig. 4., and it has length L, width W, and thickness T_{hc}. T_{hc} is the half channel thickness.

In Fig. 4, the space-charge region is represented as lying entirely in the p-region. This is only an approximation; but it is a good one (18) since the impurities in the n-region are much greater than that of the p-region. The lower surface (gate) represents a junction boundary. When this junction is reverse biased a depletion layer forms which extends a distance t into the channel. The value of t depends on the reverse bias voltage and increases with distance x in as much as the potential in the conducting channel increases with that distance when a drain current I_d is flowing (18). A current I_d between source and drain contacts results when a voltage V_D is applied between the source and drain terminals. This current is restricted to the region beneath the depletion layer boundary. A field-effect transistor may have either an n-type channel or a p-type channel. From a circuit point of view, the structures are the same except

that the terminal voltages and currents are of opposite polarities. In Fig. 4 all voltages are measured with respect to the source terminal. The values of T_s and T_d are the extent of the depletion layer at the source and drain respectively.

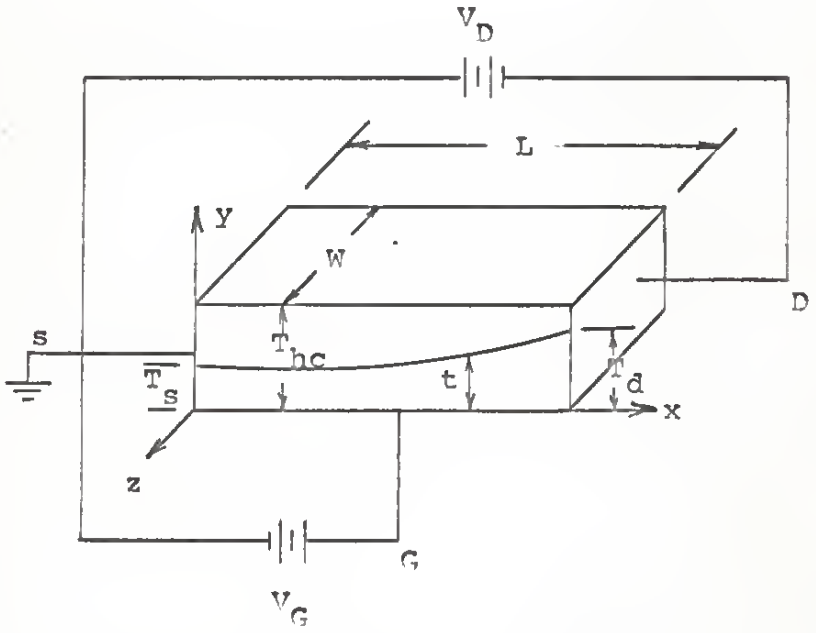


Fig. 4. The active channel of the field-effect transistor.

Free carriers constitute a mobile charge density in the region above the depletion layer boundary. Although a one-to-one correspondence usually exists between free and space-charge densities, certain exceptions occur (2). Therefore free and space-charge densities are represented independently by $\rho_s(y)$ and $\rho_f(y)$, (coul/cm^3) in order to maintain the generality of this analysis (1).

Depletion Layer Potential

In this section, the solution for the potential distribution across the depletion layer is carried out under the assumption that the reverse bias at both the gate and drain terminals are the same so that the channel has substantially uniform thickness (18). As was previously mentioned, the thickness of penetration of the depletion layer into the n-region is neglected. Therefore, it is assumed that the potential drop occurs wholly in the p-region.

To simplify the following analysis, it will prove useful to consider the integral form of the volume charge density.

$$Q(y) = A \int_0^y \rho(y)\,dy \tag{2}$$

where A is the effective area of the gate junction and has unit dimension in the x and z directions.

If the electric field E in the region $0 \leq y \leq t$ is assumed to exist in the y direction only, then the dependence of the depletion layer thickness t (see Fig. 4) on the reverse-bias voltage V(t) may be derived from the one-dimensional Poisson equation.

$$\frac{d^2V}{dy^2} = \frac{dE_y}{dy} = \frac{\rho_s(y)}{\varepsilon} \tag{3}$$

where ε is the dielectric constant of the material (farads/cm). The use of ε in farads/cm permits the use of dimensions in cm, mobilities in cm^2/volt sec and conductivities in ohm/cm, while

retaining currents and voltages in amp and volt. Also $\rho(y) = qp$ (space-charge density); p = impurity density $(N_A - N_D)$.

Integration of equation (3) yields

$$E_y = \frac{1}{\varepsilon} \int_0^y \rho_s(y)\,dy + C_1 \tag{4}$$

Near y = t there is an abrupt transistion region at which $p_s(y)$ is zero. Consequently, it is assumed that at the edge of the depletion layer $E_y = 0$. Thus using the boundary condition to evaluate the constant of integration yields

$$C_1 = -\frac{1}{\varepsilon} \int_0^t \rho_s(y)\,dy \tag{5}$$

therefore

$$E_y = \frac{1}{\varepsilon} \int_0^y \rho_s(y)\,dy - \frac{1}{\varepsilon} \int_0^t \rho_s(y)\,dy \tag{6}$$

When equation (2) is substituted into equation (6) then

$$E_y = \frac{1}{\varepsilon} [Q(y) - Q(t)] \tag{7}$$

The voltage across the depletion layer can now be obtained by integrating equation (7) between $0 \leq y \leq t$.

$$V(t) = -\frac{1}{\varepsilon}\int_0^t [Q(y) - Q(t)]\, dy \tag{8}$$

Hence,

$$V(t) = \frac{1}{\varepsilon}\left[yQ(t) - \int_0^t Q(y)\, dy\right] \tag{9}$$

The terms in the brackets of equation (9) are an integral of a product and can be expressed as

$$V(t) = \frac{1}{\varepsilon}\int_0^t y\rho_s(y)\, dy \tag{10}$$

Therefore the voltage across the depletion layer as a function of t is given by equation (10).

Equation (10) has an important limit in the form of a pinch-off voltage V_p when the upper limit of integration is allowed to go to T_{hc}. Remembering that advantage of the symmetry of the field-effect transistor has been taken, this limit then yields the reverse bias voltage that removes all the free charge from the conducting channel; thus the current path has been pinched-off i.e., the channel no longer has the ability to conduct current. The pinch-off voltage V_p is defined then as the magnitude of the input gate voltage, V_G, required to reduce the output current to zero. Hence,

$$V_p = \frac{2}{\varepsilon} \int_0^{T_{hc}} y \, \rho_s(y) \, dy \tag{11}$$

The junction capacitance of the field-effect transistor can now be evaluated. The differential of equation (10) is

$$dV(y) = \frac{2}{\varepsilon} (y\rho_s(y)dy) \qquad 0 \leq y \leq t \tag{12}$$

When equation (2) is substituted into equation (12), equation (12) becomes

$$dV(y) = \frac{2ydQ(y)}{A\varepsilon} \qquad 0 \leq y \leq t \tag{13}$$

where

$$dQ(y) = A\rho_s(y)dy \tag{14}$$

therefore,

$$\frac{dQ}{dV} = C_j = \frac{\varepsilon A}{2t} \qquad (y = t) \tag{15}$$

Equation (15) defines the junction capacitance and shows that the space-charge layer thus acts as a parallel plate capacitor with plate separation t.

Channel Current

An expression relating the drain current, I_d to the physical parameters of the transistor and to the applied voltages can be derived from Ohm's law. When a current flows in the plus x direction in the channel of Fig. 4, an electric field with a component E_x must be present. This requires that the potential changes along the channel. Since the gate terminals carry no current they are equipotentials. Hence the reverse voltage between channel and the n-regions varies with distance x and therefore the channel thickness varies (18). In the previous section, the derivation of the relationship between depletion layer thickness t and reverse-bias voltage V assumed that

$$\frac{\partial^2 V}{\partial x^2} = 0 \quad , \tag{16}$$

so that a one-dimensional Poission equation could be used. However when current flows,

$$E_x = \frac{\partial V}{\partial x} \neq 0 \quad , \tag{17}$$

in general $\frac{\partial^2 V}{\partial x^2}$ will not vanish. However, if $\frac{\partial^2 V}{\partial x^2}$ is very small compared to $\rho_s(y)/\varepsilon$, then the one dimensional approximation can be used for channel potential V(y) and the reverse bias channel potential V(x) will be the same as in the case of $I_d = 0$ (18). The approximation that V(x) and t(x) change gradually with distance

x is referred to by Shockley (18) as the gradual case. The gradual case will be assumed in the following discussion.

Ohm's law in terms of current density in the x direction J_x, electric field E_x and conductivity $\sigma(x)$ is

$$J_x = E_x \sigma(x) \tag{18}$$

where $\sigma(x) = qp_f(y)\mu$.

Now $\rho_f(y) = qp_f(y)$ is the free space charge density.

Substituting these relations and the expression for the electric field from equation (17) into equation (18),

$$J_x = \mu \rho_f(y) \frac{dV}{dx} \tag{19}$$

from which the total current through any cross section of the channel can be obrained i.e.,

$$I_x = 2 \int_t^{T_{hc}} J_x dS \tag{20}$$

where $dS = Wdy$, so that equation (20) becomes

$$I_x = 2\mu \frac{dV}{dx} W \int_t^{T_{hc}} \rho_f(y)\, dy \tag{21}$$

The factor of 2 occurs because of symmetry. Equation (21) can be simplified somewhat by replacing dV by $\frac{1}{\epsilon} y\rho_s(y)dy$ as given

by equation (12). Hence,

$$I_x dx = \frac{2W\mu y\rho_s(y)\,dy}{\varepsilon} \int_t^{T_{hc}} \rho_f(y)\,dy \tag{22}$$

From equation (2) assuming unit dimensions in the x and z directions then,

$$Q(T_{hc}) - Q(t) = \int_t^{T_{hc}} \rho_f(y)\,dy \tag{23}$$

Substituting this relationship into equation (22), it then becomes

$$I_x dx = \frac{2\mu W}{\varepsilon} [Q(T_{hc}) - Q(t)]y\rho_s(y)\,dy \tag{24}$$

When equation (24) is integrated from x = 0 to x = L, the corresponding limits on the right-hand side are from y = T_s to y = T_d. Therefore the total drain current is given by,

$$I_d = \frac{2\mu W}{\varepsilon L} \int_{T_s}^{T_d} [Q(T_{hc}) - Q(t)]y\rho_s(y)\,dy \tag{25}$$

An examination of equation (25) shows that when T_s equals zero and T_d approaches T_{hc}, then the drain current becomes a maximum current called I_p.

From equation (25) it is quite apparent that the current is a function of the space-charge layer heights at both the source and drain ends of the channel which in turn are functions of the voltages across the depletion layer at each end of the channel: i.e.

$$T_s = F(V_{GS}) \tag{26}$$

$$T_d = G[V_{DS} - V_{GS}] \tag{27}$$

At this point it is convenient to define I_p, as the drain current that flows when the external gate and source terminals are shorted together. By this definition, I_p is the drain current for any value of voltage between source and drain V_{DS}, but will be restricted to the current that flows when V_{DS} has a value that causes T_d to equal T_{hc} (5). That value of voltage was shown to be V_p in the previous section. Hence,

$$I_p = \frac{2\mu W}{L\varepsilon} \int_0^{T_{hc}} [Q(T_c) - Q(t)]y\rho_s(y)\,dy \tag{28}$$

This is abnormal of course, since if T_d equals T_{hc}, the conducting channel thickness is zero and no current can flow. Or what is more likely, if the conducting channel thickness goes to zero, then the current density must go to infinity, since when $V_{GS} = 0$ it is not possible to cause I_p to go to zero by increasing V_{DS}. The answer to this dilemma is that T_d cannot equal T_{hc},

because there is a fundamental limit on how narrow the conducting channel can be (1). If the limiting value of the current density is J_{max}, then $I_p = WJ_{max}\ \Delta T_{hc}$ where ΔT_{hc} is the narrowest possible conducting channel. Equation (28) is therefore only an approximation. The real upper limit on the integral is $(T_{hc} - \Delta T_{hc})$, but the approximation given is a good one because T_{hc} is much greater than ΔT_{hc} (5).

Characteristics of the Field-Effect Transistor

There are two distinctly different modes of operation of the field-effect transistor. First, for zero or small voltages across the channel, where the conductance of the channel (see Fig. 5) is not markedly changed by the current flow, and second, operation in pinch-off (or saturation) where the channel conductance is affected by the flow of current. The current of the device in this latter mode of operation becomes virtually independent of the drain voltage as depicted by the device's output characteristics of Fig. 5. In the first mode of operation, the device can be considered as a passive element-variable conductance controlled by the gate voltage. In the second mode of operation, it appears as an active device with characteristics similar to those of a vacuum pentode.

An examination of Fig. 5 shows that beyond the pinch-off voltage V_p, further increases in V_{DS} (up to the junction reverse-bias breakdown, BV_{DGS}) causes little change in I_d. For this reason, this portion of the field-effect transistor characteristics

is referred to as the pinch-off or constant current region (13). Note pinch-off is shown to occur with $V_{GS} = 0$. Another region of importance as shown by Fig. 5 is the so called triode region. These two regions are separated by the dashed curve, which is the locus of pinch-off points, i.e., the points where $V_{DS} = V_p + V_{GS}$.

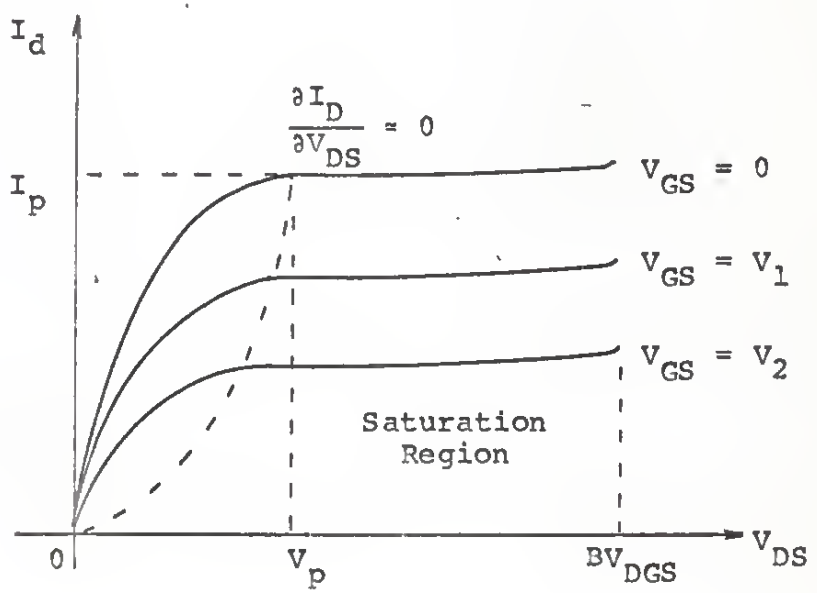


Fig. 5. Output characteristics of a field-effect transistor.

Mutual Transconductance

The most active and useful parameter of the field-effect transistor is its mutual transconductance, g_m. The amplifying properties of a field-effect transistor are best characterized by

its mutual transconductance. It has been previously shown that the drain current is a function of the small increments of gate-to-source voltage and the drain-to-source voltage, i.e.,

$$I = f(V_{GS}, V_{DS}) \tag{29}$$

Equation (29) can be written as

$$\Delta I_d = \frac{\partial I_d}{\partial V_G} \Delta V_G + \frac{\partial I_d}{\partial V_D} \Delta V_D \tag{30}$$

therefore

$$\Delta I_d = g_m \Delta V_G + g_d \Delta V_D \tag{31}$$

where

$$g_m = \frac{\partial I_D}{\partial V_G} \tag{32}$$

and

$$g_d = \frac{\partial I_D}{\partial V_D} \tag{33}$$

so that

$$g_m = \frac{\partial I_d}{\partial V_G} = \frac{\partial I_d}{\partial T_S} \frac{\partial T_s}{\partial V_G} + \frac{\partial I_d}{\partial T_D} \frac{\partial T_d}{\partial V_G} \tag{34}$$

The partial derivatives $\frac{\partial I_d}{\partial T_s}$ and $\frac{\partial I_d}{\partial T_d}$ can be evaluated from equation (25). Thus,

$$\frac{\partial I_d}{\partial T_s} = \frac{2\mu W}{\varepsilon L} [Q(T_{hc}) - Q(T_s)] T_s \rho_s(T_s) \tag{35}$$

and

$$\frac{\partial I_d}{\partial T_d} = \frac{2\mu W}{\varepsilon L} [Q(T_{hc}) - Q(T_s)] T d \rho_s(T_d) \tag{36}$$

Now, from equation (10), the rate of change of voltage across the depletion layer with respect to y is given as

$$\frac{dV(y)}{dy} = \frac{qy\rho_s(y)}{\varepsilon} \qquad 0 \leq y \leq t \tag{37}$$

Using equation (37) and the relationship in equation (26) and (27) with the consideration that $V(T_s) = -V_{GS}$ and $V(T_d) = (V_{DS} - V_{GS})$, then the following partials are obtained.

$$\frac{\partial V_{GS}}{\partial T_s} = \frac{qT_s\rho_s(T_s)}{\varepsilon} \tag{38}$$

and

$$\frac{\partial V_{GS}}{\partial T_d} = \frac{qT_d\rho_s(T_d)}{\varepsilon} \tag{39}$$

Substituting equations (35), (36), (38) and (39) back into equation (34), then the mutual transconductance is obtained.

$$g_m = \frac{\mu W}{L} [Q(T_d) - Q(T_s)] \tag{40}$$

The implication of equation (40) is extremely interesting; it shows that the transconductance of the field-effect transistor is simply the conductance of the rectangular section of the device extending from $y = T_s$ to $y = T_d$. Maximum g_m is obtained when $T_d = T_{hc}$ and $T_s = 0$. This occurs when $V_G = 0$ and $V_D = V_p$. Hence,

$$g_{m_{(max)}} = \frac{\mu W}{L} Q(T_c) = g_o \quad , \tag{41}$$

where g_o is the bulk conductance of the entire semiconductor body. This value is independent of the space-charge density (1). The small-signal output conductance g_d at the drain terminals of the device can be obtained from equations (23) and (37) in a similar manner.

$$g_d = \frac{\partial I_d}{\partial V_D} = \frac{\mu W}{L} [Q(T_c) - Q(T_d)] \tag{42}$$

Equation (42) is the conductance of the rectangular parallelpiped portion of the channel bounded by T_d and T_c in the y direction. According to equations (28) and (42), when $I_d = I_p$, $g_d = 0$ and the drain terminal of the device behaves as a constant-current source; these results are shown graphically in Fig. 5. At $V_{DS} = V_p$, g_d is zero, and further increases in V_{DS} produces no increase in I_d. This is only a first-order approximation, of course (1). When T_d approaches T_c, other effects influence the behavior of the output characteristics of Fig. 5 such that g_d really never gets to zero before the gate-to-drain diode goes into avalanche breakdown (5).

Determining the Field-effect Pinch-off Voltage

The preceeding analysis defined the pinch-off voltage of the field-effect transistor as the drain voltage which separates the triode region from the pinch-off region with zero gate bias. Because pinch-off is not a sharply defined phenomena itself it becomes necessary to define somewhat arbitrarily how the pinch-off voltage of a field-effect transistor is measured.

Richer and Middlebrook (14) in a recent communication showed that FET transfer characteristics as illustrated by Fig. 6 are represented remarkably well by the following simple relation;

$$I_D = I_p \left(1 - \frac{V_{GS}}{V_p}\right)^n \tag{43}$$

where n is a constant surprisingly close to 2.

Equation (43) is called the square law approximation. The square law with its delightful simplicity, is not a bad approximation of the transfer curve of any FET and is quite an accurate approximation for FET's with narrow channels (low pinch-off voltages) no matter how they are manufactured. (6)

The values of I_p and V_p are necessary to completely describe the forward transfer characteristics, and should be given by a manufacturer's data sheet. When equation (43) is differentiated with respect to V_{GS} one obtains

$$g_m = \frac{nI_p}{V_p} \left(1 - \frac{V_{GS}}{V_p}\right)^{n-1} \tag{44}$$

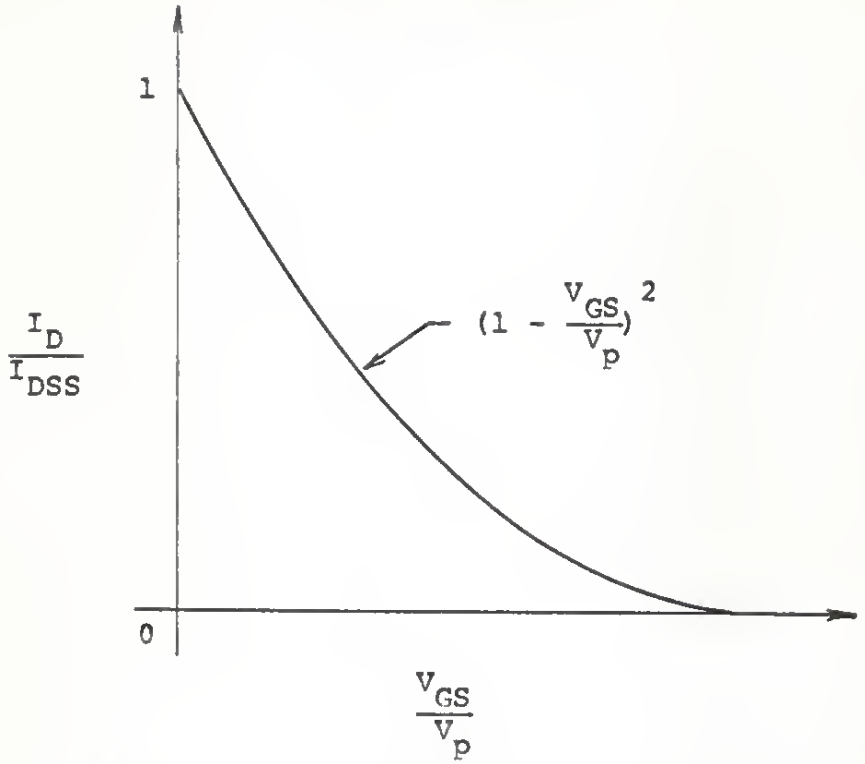


Fig. 6. Transfer curve with limits.

From equation (44) transconductance at zero-gate voltage is obtained as follows:

$$g_m \Big|_{V_{GS}=0} = g_d = \frac{nI_p}{V_p} \tag{45}$$

Equation (45) also equals the channel conductance $1/R_o$ for $V_{GS} = 0$ and $V_{DS} < V_p$. From these facts, the following expressions are then valid (6).

$$V_p = \frac{nI_p}{g_d} \tag{46}$$

or

$$V_p = nI_p R_o \tag{47}$$

Both of these equations give V_p a fairly precise meaning. The terms on the right hand side of equation (45) are measured in the pinch-off region and for all practical purposes are independent of the drain voltage. Equation (46) has the advantage that V_p is obtained quite simply from the static output characteristics. In either case the value obtained for V_p by these methods characterize the field-effect transistor in a broader sense than a value obtained in the usual manner (6). These equations developed above have shown that all field-effect transistors have a fixed relationship between pinch-off voltage V_p, zero-bias current I_p, and zero-bias forward transconductance. Thus it is possible, given a single set of reference values, to determine specific parameter values for a select device.

What has been said indicates that when making calculations for the design of field-effect transistor circuits, I_p and V_p give most of the information necessary. Other FET characteristics (except for breakdown voltages) can be regarded as causing only second-order effects; for the most part they can be ignored (6).

Temperature Dependence of I_p

Although I_p is not greatly dependent on the drain-to-source voltage as was pointed out in its derivation, it is a very strong

function of temperature as Fig. 7 attests. The temperature dependence of I_p can quickly be derived from equation (28). Differentiation of this equation with respect to temperature (T_A) yields

$$\frac{dI_p}{dT_A} = \frac{2W}{\varepsilon L}\frac{du}{dT_A}\int_0^{T_{hc}} [Q(T_c) - Q(t)]y\rho_s(y)\,dy \qquad (48)$$

The left hand side can be reduced to $1/\mu(du/dT_A)I_p$ where $1/\mu(du/dT_A)$ is by definition the temperature coefficient of the mobility. The temperature coefficient and the variation of drain current will be discussed further in the following section.

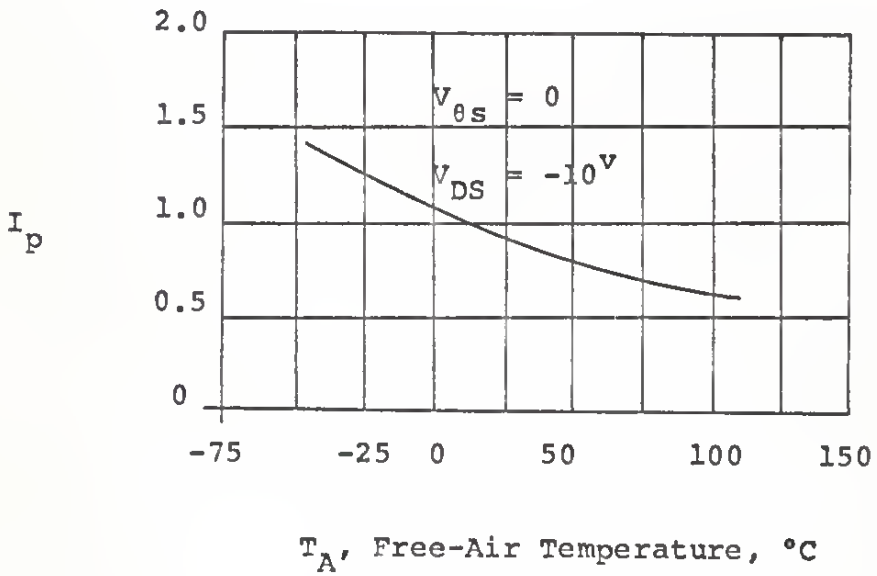


Fig. 7. Normalized zero-gate-voltage drain current vs. free air temperature.

BIASING FIELD-EFFECT TRANSISTORS

In field-effect transistors, the variation of drain current with temperature can be held to very low levels by proper selection of the bias point. This zero bias point depends on the physical size and pinch-off voltage of the field-effect transistor.

The variation of drain current with temperature in a field-effect transistor is determined by two factors. One factor is the change in majority carriers mobility. As temperature increases, majority carriers move less freely in the crystalline structure. For a given field strength, their velocity is reduced (10). This tends to make drain current I_d decrease as temperature increases. The rate of decrease for most FET's is between 0.6 and 0.8 per cent/deg C (3).

The second factor is the change in width of the thermally generated depletion layer at the gate-channel junction. Any p-n junction, even with no voltage applied, has this depletion layer. As was shown in the first part of this report, it is identical to the depletion region generated by reverse-biasing the gate-to-channel diode with an external voltage. The width of the thermally generated barrier decreases as temperature increases, tending to make I_d increase with increasing temperature, at a rate equivalent to a change of 2.2 mv/deg C at the gate (10). This is the same phenomenon, incidentally, that causes the base-emitter voltage in bipolar transistors to change by 2.2 mv/deg C when the collector current is held constant.

Note that these two factors act in opposite directions. The change in majority-carrier mobility tends to decrease I_d; the change in depletion-layer thickness tends to increase I_d. If conditions can be found at which the two effects cancel, the FET will have no net change of I_d with temperature. If the mobility factor is -0.7 per cent/deg C and the thermal barrier factor is 2.2 mv/deg C, the condition for zero thermal drift is

$$0.007 I_{dz} = 0.0022 g_{mz}$$

$$\frac{I_{dz}}{g_{mz}} = 0.315 \text{ volts} \tag{49}$$

where g_{mz} and I_{dz} are the transconductance and the drain current respectively at the zero-drift bias point.

To proceed further, other expressions for I_d and g_{mz} must be developed. For a double-diffused FET, (see Fig. 3) the drain current for any value of gate-to-cource voltage between zero and pinch-off voltage V_p is:

$$I_d = I_p \left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{50}$$

where I_d is the drain current at $V_{GS} = 0$. Equation (50) is called the square-law approximation (14).

A similar expression for g_{mz} was derived in equation (30) i.e.

$$g_{mz} = \frac{\partial I_d}{\partial V_{GS}} \tag{51}$$

or

$$g_{mz} = \frac{\partial I_p}{V_p}\left(1 - \frac{V_{GS}}{V_p}\right) \tag{52}$$

Dividing equation (50) by equation (52) gives

$$\frac{I_d}{g_{mz}} = \frac{V_p}{2}\left(1 - \frac{V_{GS}}{V_p}\right) \tag{53}$$

substituting equation (53) into equation (49) gives

$$0.315 = \frac{V_p}{2}\left(1 - \frac{V_{GSt}}{V_p}\right)$$

or

$$V_{GSz} = V_p - 0.63 \tag{54}$$

This equation shows the value of V_{GS} which will give zero drift. It also shows that for a FET with $V_p = 0.63$ volts, the point of zero drift occurs at $V_{GS} = 0$, or $I_d = I_p$. More important, these equations allow prediction of I_{dz} and g_{mz} at zero drift for devices with V_p above 0.63 volts (3). Thus, at zero drift,

$$I_d = I_p \left(\frac{0.63}{V_p}\right)^2 \tag{55}$$

$$g_{mz} = \frac{2I_p}{V_p} \left(\frac{0.63}{V_p}\right) \tag{56}$$

Equation (55) reveals that devices with a large V_p must operate at an I_{dz} very much below I_p to achieve zero drift. For example, if V_p is 6.3 volts, I_{dz} must be one per cent of I_p.

For a given device type, unit-to-unit variations of I_p and V_p are interrelated by the empirical equation (10),

$$I_p = KV_p^{1.6} \tag{57}$$

where K is a function of the device geometry.

Substituting equation (57) into equation (55) gives

$$g_{mz} = K_1 \left(\frac{1}{V_p}\right)^{0.4} \tag{58}$$

and substituting equation (57) into equation (56) gives

$$g_{mz} = K_2 \left(\frac{1}{V_p}\right)^{0.4} \tag{59}$$

Equations (58) and (59) show that, when a field-effect transistor is biased for zero drift, both I_{dz} and g_{mz} are inverse functions of V_p. Therefore, low V_p devices are perferable for most applications (10).

If a FET is biased at other than the zero-drift bias, what effect will the temperature-induced change in I_d have on V_{GS}? It has already been found that the change in depletion layer thickness causes V_{GS} to change at a rate of -2.2mv/deg C. Assuming that the change in mobility causes I_d to change 0.7 per cent/deg C, then the quantity $0.007\ (I_d/g_{mz})$ represents the corresponding change, in volts/det C, of V_{GS} (3). Thus, the net drift is

$$D = 0.0022 - 0.007\left(\frac{I_d}{g_m}\right) \tag{60}$$

in volts/det C.

Dividing equation (50) by equation (52) reveals that

$$\frac{I_d}{g_m} = \frac{V_p}{2}\left(1 - \frac{V_{GS}}{V_p}\right) \tag{61}$$

Substituting equation (61) into equation (60),

$$D = 0.0022 - 0.007\ \frac{V_p}{2}\left(1 - \frac{V_{GS}}{V_p}\right) \tag{62}$$

Rearranging equation (50), it can be seen that

$$\left(1 - \frac{V_{GS}}{V_p}\right) = \left(\frac{I_d}{I_p}\right)^{1/2} \tag{63}$$

Substituting equation (63) into equation (62),

$$D = 0.0022 - 0.007 \frac{V_p}{2}\left(\frac{I_d}{I_p}\right)^{1/2} \tag{64}$$

But, from equation (52)

$$(I_p)^{1/2} = \frac{V_p}{0.63}(I_{dz})^{1/2} \tag{65}$$

Then

$$D = 0.0022 - 0.0022\left(\frac{I_d}{I_{dz}}\right)^{1/2} \tag{66}$$

Converting to millivolts per deg C,

$$D = 2.2\left(1 - \sqrt{\frac{I_d}{I_{DSS}}}\right) \tag{67}$$

Thus for any bias current I_d, the change of V_{GS} with temperature can be calculated if the zero-drift bias current I_{dz} is known. The test circuit used to verify the drift-compensation concept is shown in Fig. 8. Source resistor R_s is large enough to keep I_d constant. A zero-drift bias point can be found by adjusting R_s until V_p at 100°C is equal to V_{GS} at 25°C (10).

To confirm equations (58) and (59) field-effect transistors with various pinch-off voltages have been tested in a circuit like that of Fig. 8. I_{dz} and g_m were measured for each. The measured points shown in Figs. 9 and 10 are sufficiently close to the calculated curves to justify the equations (10).

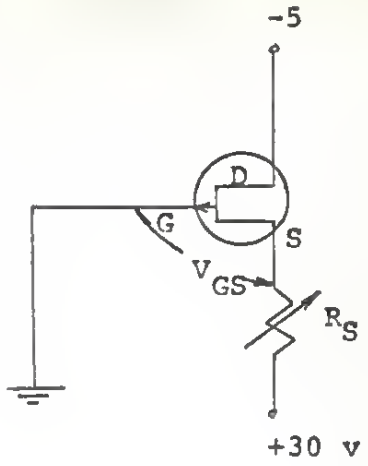


Fig. 8. Test circuit for finding zero-drift bias point.

The simplest circuit for zero-drift is the source follower, illustrated by the test circuit of Fig. 8. This circuit has no voltage gain, but can be used as an impedance transformer. The thermal drift of this circuit is comparable to that of a high-quality differential amplifier (10). Since voltage and current drift can be reduced to very low levels, field-effect transistors permit design of d-c amplifiers which exhibit little change in operating point even with generator impedances greater than one megohm (10).

Selecting the Best FET

As might be expected, values of I_{dz} and g_m are proportional to the size of the field-effect transistor. Also, as in pointed out previously, field-effect transistors with low V_p have higher I_{dz} and g_m.

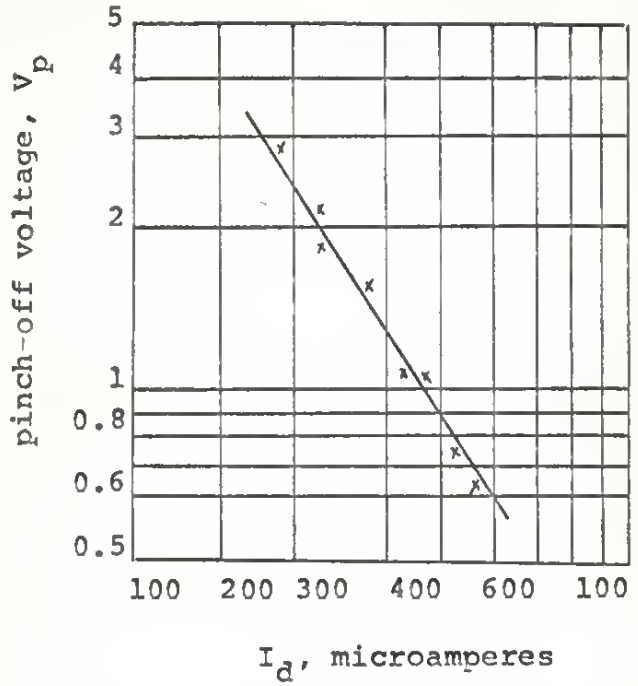


Fig. 9. Drain current at zero drift for various values of pinch-off voltage. The cross represent measurements made in the circuit of Fig. 8. The line represents values calculated from eq. (58).

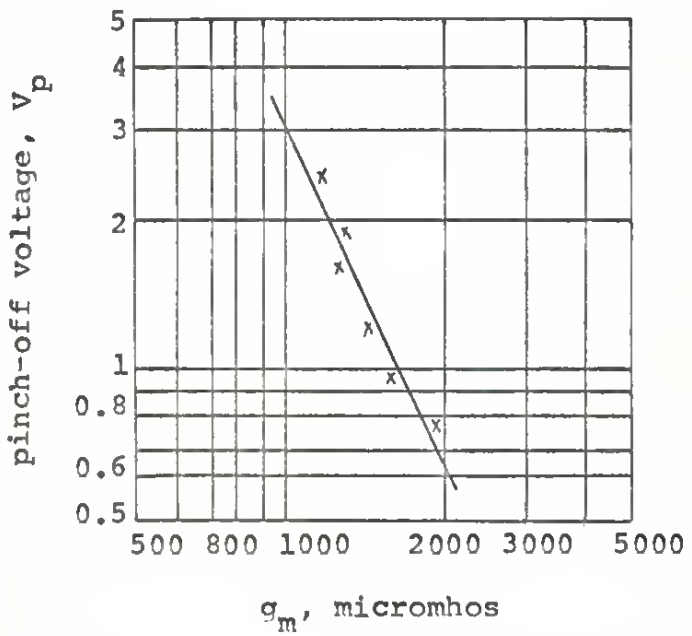


Fig. 10. Transconductance at zero drift for various values of pinch-off voltage. The line represents calculated values from eq (59).

Field-effect transistors with higher I_{dz} are desirable for amplifiers in which a junction transistor is used in the second stage. Field-effect transistors with low I_{dz} are more seriously affected by the loading of a junction transistor, here, a second field-effect transistor, with its very low current drift, is the ideal choice for the second stage.

In selecting the best type of field-effect transistor for an application, a compromise must be made between the very large input impedance and the low input current drift of the small-geometry field-effect transistor and the ease of circuit design afforded by the higher drain current of large field-effect transistors.

Circuit Design

As any given FET type may have as much as 5:1 spread in I_p and 4:1 spread in g_m, particular attention must be given to circuit design to ensure that any device within specifications will perform satisfactorily (16). Consider a common-source self-biased amplifier design of Fig. 11. It is helpful to have a plot available of the approximate minimum and maximum transfer characteristics of the device. The d-c operating point for any device within the range may be determined by constructing a source load line from the origin with a slope of $1/R_s$ intersecting with the two curves. It is desirable to operate with a small R_s for minimum distortion, but with a large R_s for constant drain current I_d. The range of the quiescent I_d has now been determined; however, the peak signal current $i_{D_{max}}$ must be added. This is determined by superimposing

the gate signal voltage on the operating point. To maintain a reasonably low distortion level, the signal swing as projected on the minimum transfer curve must be small compared with the curvature of that characteristic (16). The peak signal current $i_{d_{(max)}}$ has been determined; the maximum allowable R_L may be determined. Remembering that the V_{DG} should not drop below about 1.5 V_p, then

$$V_{DG} = V_D - i_{D_{(max)}} R_L \tag{68}$$

and

$$R_{L_{(max)}} = \frac{V_D - 1.5V_p}{i_{D_{(max)}}} \tag{69}$$

Stage gain may be increased only be increasing R_L. To do this it is necessary to increase V_D, reduce i_d and/or V_p or select a field-effect transistor with a smaller spread in I_p (17). As some field-effect transistors are typed with I_p spreads of 3:1 their use may be of some advantage (17).

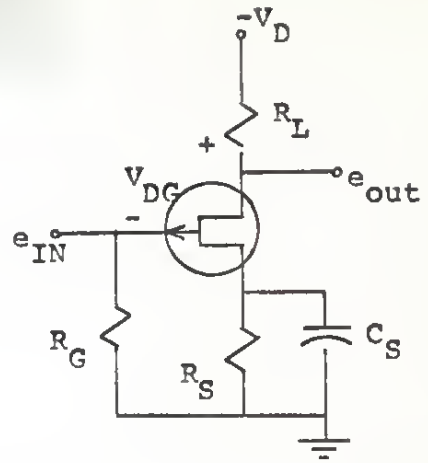


Fig. 11(a). Self-biased amplifier.

Fig. 11(b). Transfer characteristics.

SMALL-SIGNAL LOW FREQUENCY-PROPERTIES

The channel current of a field-effect transistor actually flows in a nonlinear distributed RC transmission line, but for low frequency work it is sufficient to treat the device as if it were a lumped nonlinear electrical network. An equivalent circuit showing the lumped parameters necessary for low frequency calculations is given in Fig. 12. Capacitances C_{DG} and C_{SG} and conductances g_{DG} and g_{SG} are a lumped-element representation of the reverse-biased gate-to-channel diode. In a well designed

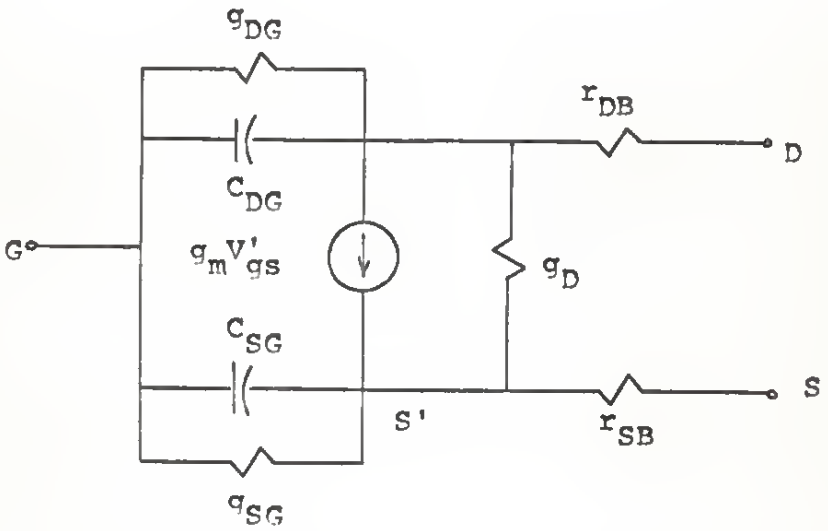


Fig. 12. Low frequency equivalent circuit for FET.

field-effect transistor, g_{DG} and g_{SG} will be quite small and can be considered open circuits. VAlues r_{DB} and r_{SB} are the bulk resistances of the semiconductor path from the channel edges to the drain and source respectively; they will be in the order of 100

ohms or less, depending somewhat on the geometry and manufacturing process (9). At low frequencies, the effect of r_{DB} is quite negligible; it can be considered as only a very small part of any practical load resistance (9). The value of r_{SB} has a slight, generally negligible effect on the apparent transconductance of the device; the small signal voltage v'_{gs} in Fig. 12, is related to the input terminal voltage v_{gs} by

$$v'_{gs} = \frac{v_{gs}}{1 + g_m r_{SB}} \tag{70}$$

The value of g_m is the slope of the output characteristics in the pinch-off region and is generally small compared to practical load conductances.

For linear small signal-operation, the common-source configuration is probably the most useful. Because of the nature of its characteristics, i.e. high input and output impedances, use of the admittance parameters is recommended (9). They are defined by the equations

$$i_g = y_{is} v_{gs} + y_{rs} v_{ds} \tag{71}$$

$$i_d = y_{fs} v_{gs} + y_{os} v_{ds} \tag{72}$$

The two-generator equivalent circuit based on the use of these parameters is shown in Fig. 13. The terminal conditions for determining the parameters are

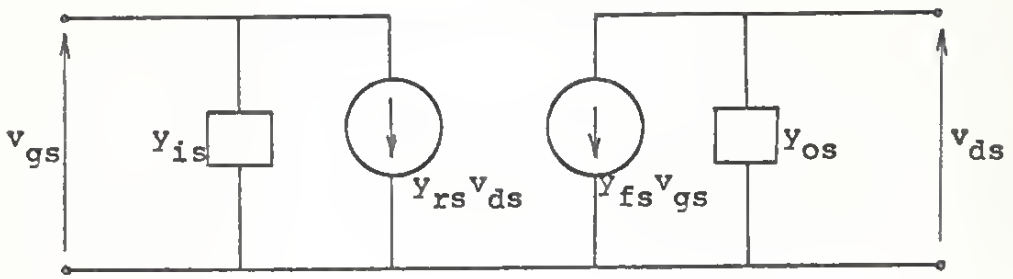


Fig. 13. Two-port y-network.

Output shorted: $$y_{is} = \frac{i_g}{v_{gs}}$$

$$y_{fs} = \frac{i_d}{v_{gs}}$$

Input shorted: $$y_{rs} = \frac{i_g}{v_{ds}}$$

$$y_{os} = \frac{i_d}{v_{ds}}$$

When these conditions are applied to the physical equivalent circuit of Fig. 12, the y parameters can be written in terms of the lumped physical elements. If all the diode conductances and bulk resistances of Fig. 12 are neglected, the y parameters (9) are:

$$y_{is} = j\omega(C_{DG} + C_{SG}) \tag{73}$$

$$y_{rs} = -j\omega C_{DG} \tag{74}$$

$$y_{fs} = g_m - j\omega C_{DG} \tag{75}$$

$$y_{os} = g_{DS} + j\omega C_{DG} \tag{76}$$

These parameters are all bias dependent (9). It has been shown previously that the bias dependence of g_m in the pinch-off region is given by equation (44).

SMALL-SIGNAL EQUIVALENT CIRCUIT

It is now possible to develope a low frequency circuit for the field-effect transistor by using equations (71) and (72). Both equations (71) and (72) have dimensions of current, and thus the right hand side of each equation suggest the summing of currents entering a junction. Figure 13 illustrates the simplest and the most obvious two-current-generator equivalent circuit that can be developed from equations (71) and (72).

A small equivalent low frequency circuit of Fig. 13 can be used to describe the incremental linear behavior of the field-effect transistor. Because the input-gate current I_g is assumed to be negligible (let $I_g = 0$), both y_{is} and y_{rs} in equation (71) are equal to zero. Hence,

$$0 = 0\ v_{gs} + 0\ v_{ds} \tag{77}$$

$$i_d = g_m v_{gs} + g_d v_{ds} \tag{78}$$

redefining,

$$y_{fs} = g_m \quad \text{and} \quad y_{os} = g_d$$

where g_m is the small-signal low frequency transconductance of the device and g_d is the small-signal output conductance of the device.

Thus equation (78) is the only equation of any importance in field-effect transistor small-signal equivalent circuit analysis.

The equivalent small-signal circuit for the field-effect transistor is shown in Fig. 14.

The assumption that $I_g = 0$ greatly simplifies the equivalent circuit of Fig. 13. This assumption also emphasizes that a field-effect transistor is not necessarily a current amplifier but also a voltage amplifier.

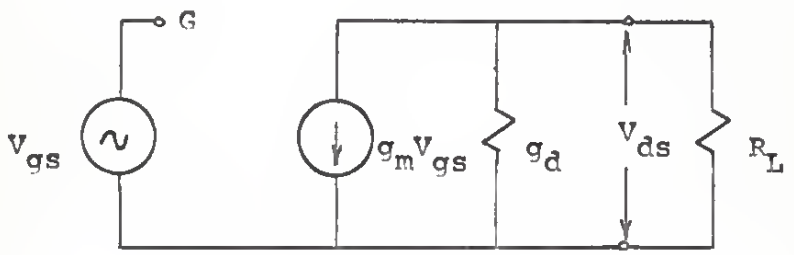


Fig. 14. Small-signal low frequency equivalent circuit of the field-effect transistor.

From this equivalent circuit the voltage gain of the device can be easily obtained if the device is operated in the pinch-off region of its characteristics (20). If a load R_L is applied to the output of Fig. 14, the expression for the gain is

$$A_v = \frac{V_{gd}}{V_{gs}} \tag{79}$$

$$v_{gs}\left[\frac{g_m}{g_d + \frac{1}{R_L}}\right] = -V_{ds} \tag{80}$$

$$\frac{v_{ds}}{v_{gs}} = -\frac{g_m R_L}{1 + g_d R_L} \tag{81}$$

therefore

$$A_v = -\frac{g_m R_L}{1 + g_d R_L} \tag{82}$$

As long as $g_d R_L << 1$ then $A_v \simeq g_m R_L$. The value of A_v varies linearly with R_L and can be made quite large by making R_L large (20). When R_L becomes extremely large, so that $g_d R_L >> 1$, $|A_v| \simeq \frac{g_m}{g_d}$, (20). This ration of the two parameters is known as amplification factor μ of the field-effect transistor. The value of μ is quite small in the non-pinch-off region of the characteristics but it becomes appreciable in the pinch-off region of the characteristics. This is the main reason that the device is operated in the pinch-off region of the characteristics (20).

The input impedance for the small-signal application of the common source field-effect transistor amplifier is particularly easy to obtain, since the gate current is assumed to be zero in theory, or

$$Z_{in} = \frac{V_{GS}}{I_g} = \infty \tag{83}$$

However for most devices the gate current is of the order of nanoamperes. So for all practical purposes when calculating the input impedance it is very large and may often be considered an open circuit.

FIELD-EFFECT TRANSISTOR AMPLIFIERS

Basic FET Amplifier Configurations

The field-effect transistor, like the other three-terminal active networks, can be operated with any of its three terminals common in an amplifier circuit. The three basic amplifier configurations are shown in Fig. 15 a-c, which are common-source, common-gate, and common-drain amplifiers respectively. In each of these connections it is possible to reverse the input and output terminals pairs, giving altogether six possible combinations, but the three connections shown are the only ones that have any major applications.

The field-effect transistor symbol shown in Fig. 15, indicates the interchange-ability of the drain and the source terminals. Without some special marking, the drain is indistinguishable from the source. Hereafter, the drain will be designated by the symbol D as in Fig. 15. The symbol shown indicates a P-channel FET; for an N-channel FET, the arrow on the gate terminal is reversed.

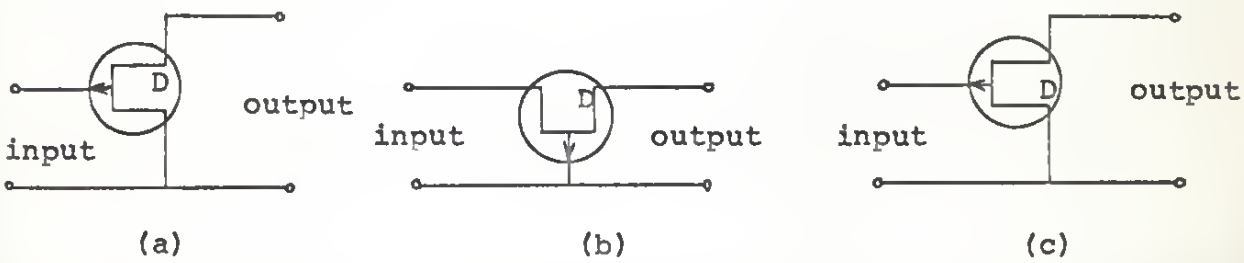


Fig. 15. Basic amplifier configurations: (a) common source, (b) common gate, (c) common drain.

Voltage Amplifier Circuit

In the past, high input impedances in amplifiers could only be obtained using vacuum tubes. Today, less complicated and more reliable designs are possible with high-quality field-effect transistors. A relatively high-input impedance solid-state amplifier will be discussed in this section and some insight into biasing techniques is provided to show that field-effect transistors are compatible with and complementary to conventional transistors. The amplifier analyzed here is built around a p-channel field-effect transistor and an npn bipolar transistor in the following stage.

In the design of a high-input-impedance amplifier, biasing at the input must be carefully considered as has been pointed out previously. Although the input impedance of the FET is very high as compared to the conventional bipolar transistor, it is necessary, if reasonably stable operation is to be achieved, to provide a d-c current path from the gate to source. The d-c gate current of the type 2N2606 field-effect transistor has been shown to be less than 10^{-9} amps at room temperature; at 100° C, however, it may increase to about 5×10^{-8} amps (8). This current must be considered in setting up the bias for the FET.

In the voltage amplifier circuit in Fig. 16a, the gate bias is

$$V_{GS} = V_G - I_g R_G \tag{84}$$

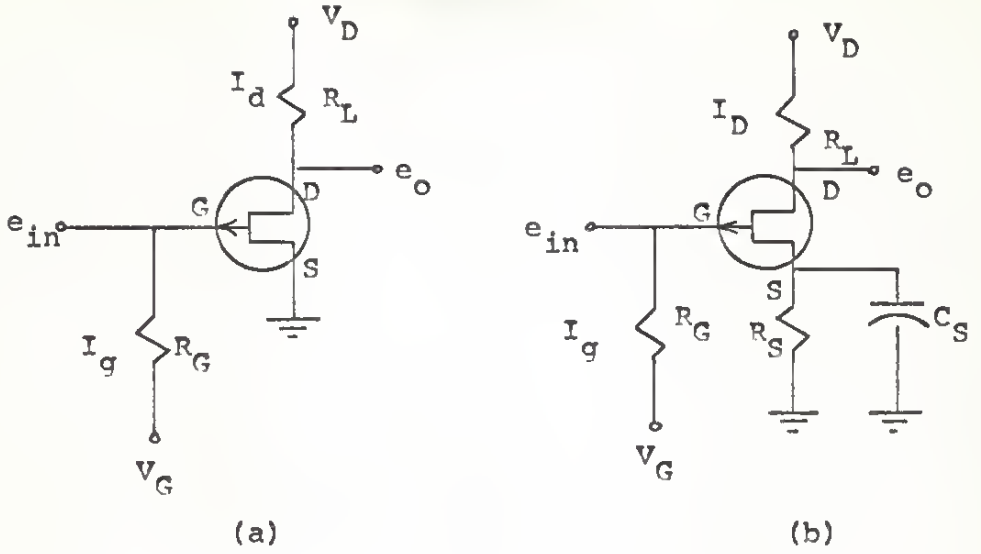


Fig. 16. Single-state amplifier
(a) Unstabilized, (b) source stabilized

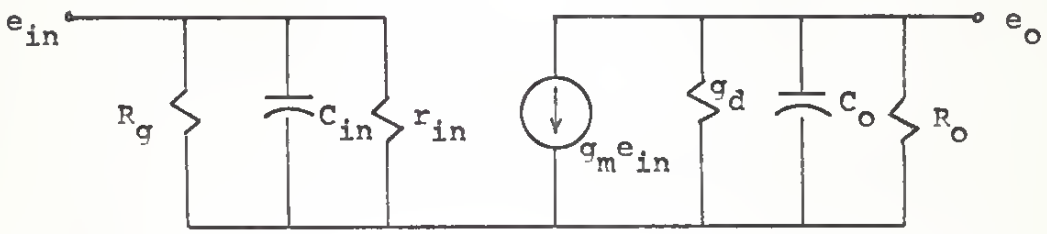


Fig. 17. Amplifier equivalent circuit.

If, for example, an input impedance of 10^7 ohms is desired, the value of R_G must be at least 10^7 ohms since it shunts the input (8). In this case, the gate bias V_{GS} may change as much as 0.5 v, due to $I_G R_G$. When the temperature is raised from 25° C to 100° C. For some applications this may be tolerable; however, this change will result in considerable variation in drain current and transconductance (8).

Another undesirable aspect of the circuit of Fig. 16a is the dependence of drain current I_d upon temperature. If V_{GS} is held constant, I_d will decrease as the device temperature increased. Since transconductance g_m is a function of drain current, it will also decrease. If the amplifier is to operate over a reasonable ambient temperature range and with a reasonable production spread of device parameters, some form of bias stabilization must be used (8).

Bias stabilization for the circuit of Fig. 16b is achieved by negative feedback, due to the I-R drop across source resistor R_S. This is the same type of current feedback provided by the emitter resistor in a conventional transistor circuit and the cathode resistor in a vacuum tube circuit. A change in source current will result in a change in source voltage, and thus ΔV_{GS} is such as to oppose the initial source-current change. Capacitor C_S serves to bypass R_S for a-c signals.

The voltage amplification of the circuits in Fig. 16 is given by equation (82).

$$A_v = \frac{g_m R_L}{1 + R_L g_d} \tag{85}$$

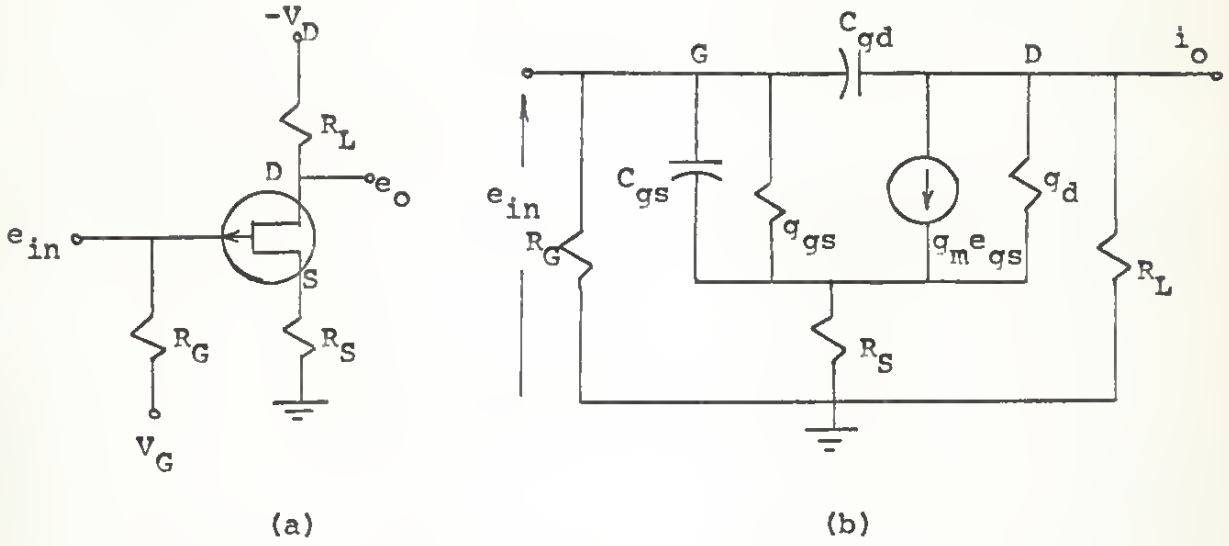


Fig. 18. (a) Amplifier with unbypassed source resistor, (b) Equivalent circuit.

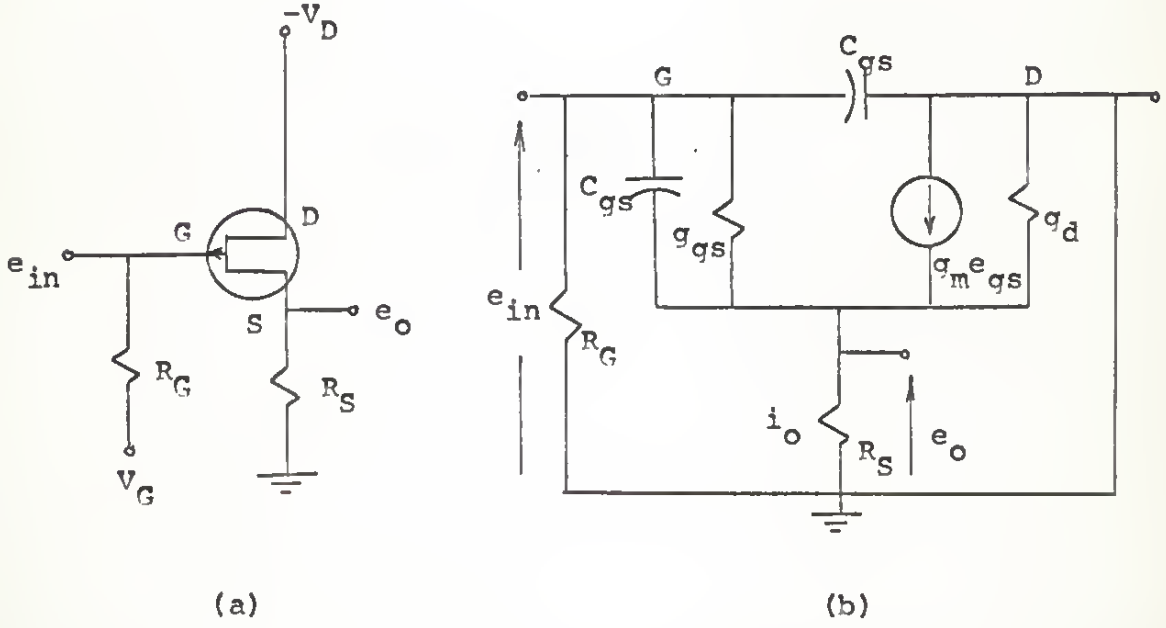
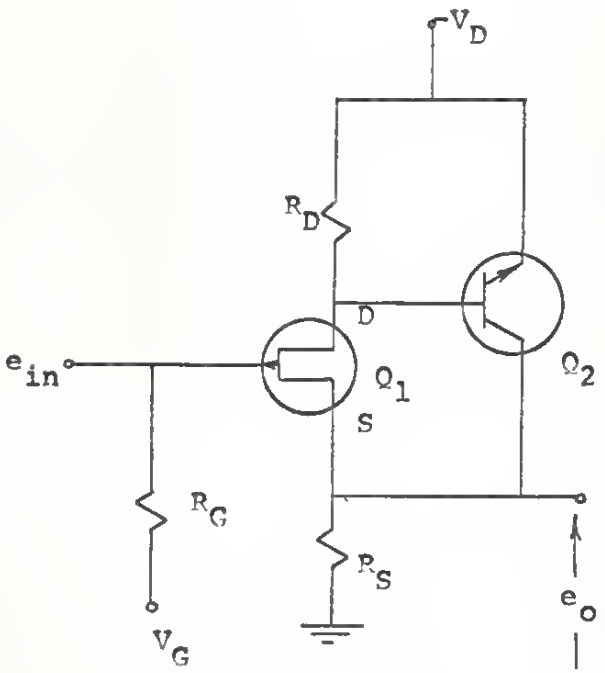
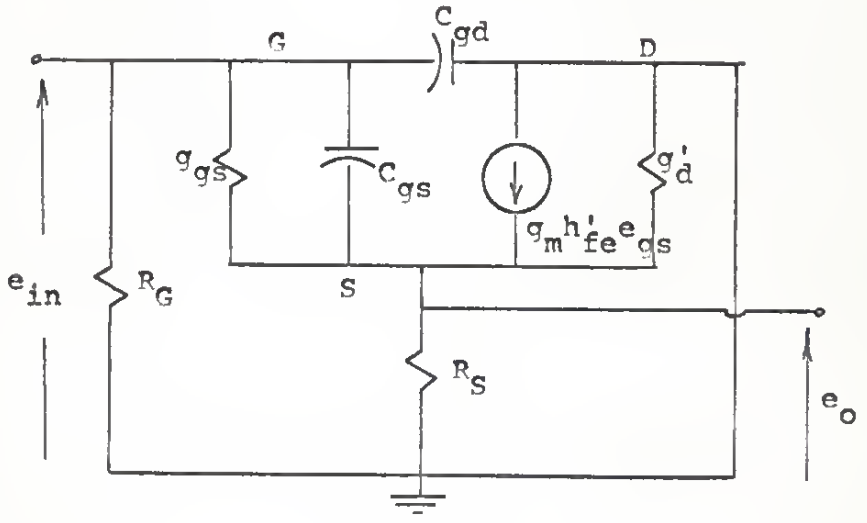


Fig. 19. (a) Source follower circuit, (b) Equivalent circuit.



(a)



(b)

Fig. 20 (a) Unipolar-bipolar cascade amplifier
(b) Equivalent circuit.

Typically, the product $R_L g_d$ will be much less than unity so that equation (85) reduces to the approximation (8)

$$A_v = g_m R_L \tag{86}$$

which is quite familiar to vacuum-tube engineers as the approximate gain of a pentode stage.

In general, the amplifier input admittance is complex and is made up of the sum of $1/R_G$, plus the gate-source admittance, plus the amplifier gain times the gate-drain admittance. This can be simplified and reduced to an equivalent input admittance as shown in Fig. 17. For the circuits of Fig. 16a the input resistance of the field-effect transistor will usually be greater than the value of R_G.

The output resistance, as shown in Fig. 17 is the parallel combination of R_L and the output resistance of the FET.

$$R_o = \frac{R_L}{1 + R_L g_d} \tag{87}$$

In the circuit of Fig. 16b, the source bypass capacitor C_S is considered to have negligible reactance at signal frequencies of interest (8). If this component is omitted (Fig. 18a), negative feedback results since R_S is common to the input and output circuits. From the equivalent circuit shown in Fig. 18b neglecting gate current, the input voltage is

$$e_{iN} = e_{gs} + i_o R_S \tag{88}$$

$$e_{iN} = e_{gs} + \frac{R_S}{R_L} e_o \tag{89}$$

The feedback factor ß is the ratio of R_S to R_L, thus the voltage amplification is given by

$$A_v' = \frac{A_v}{1 + \frac{A_v R_S}{R_L}} \tag{90}$$

substituting equation (86) into equation (90) yields

$$A_v' = \frac{g_m R_L}{1 + g_m R_S} \tag{91}$$

If $g_m R_S$ is made large with respect to unity, equation (91) becomes

$$A_v' = \frac{R_L}{R_S} \tag{92}$$

The Source Follower Circuit

If, in Fig. 19a the load resistor R_L is eliminated and the output voltage is taken from the feedback resistor R_S, a source-follower circuit is obtained. The equivalent circuit is shown in Fig. 19b. This will be recognized as being equivalent to the emitter follower and cathode follower circuits and has the same types of advantages.

Following the equivalent circuit of Fig. 19a and neglecting FET capacitances, the output current can be written as

$$i_o = \frac{e_{gs} g_m}{(1 + g_d R_S)} \tag{93}$$

the output voltage

$$e_o = i_o R_s = \frac{e_{gs} g_m R_s}{(1 + g_d R_s)} \tag{94}$$

and the input voltage

$$e_{in} = e_{gs} + e_o = e_{gs} \left[1 + \frac{g_m R_s}{(1 + g_d R_s} \right] \tag{95}$$

Dividing equation (94) by equation (95) leads to the voltage amplification:

$$A_v = \frac{e_o}{e_{in}} = \frac{g_m R_s}{(1 + R_s (g_m + g_d)} \tag{96}$$

The output impedance of this circuit is greatly reduced from that of the circuit in Fig. 16b, as indicated by

$$R_o = \frac{R_s}{1 + R_s (g_m + g_d)} \tag{97}$$

Another important characteristic of the source-follower is a reduced input admittance. The gate-source component of the effective input capacitance is reduced as shown below:

$$C'_{gs} = C_{gs} (1 - A_v) \tag{98}$$

where C_{gs} = gate-to-source capacitance.

FET Cascade With Bipolar Transistor

Where it is desired to couple a very high-impedance source to a low-impedance load, a unipolar-bipolar cascade transistor stage is a good circuit. Such a circuit is shown in Fig. 20a. The similarity between this circuit and the source follower of Fig. 18a should be noted. To a first approximation, the improvement in performance (8) can be determined by multiplying the g_m of FET Q_1 by the h_{fe} of the npn bipolar transistor Q_2. If the output admittance of the combination of Q_1 and Q_2, g'_d, is assumed to be small compared to $g_m h'_{fe}$ and $1/R_S$, the voltage amplification of Fig. 20b can be written

$$A_v = \frac{e_o}{e_{in}} = \frac{g_m h'_{fe} R_s}{1 + g_m h'_{fe} R_s} \tag{99}$$

In equation (99) and in the equivalent circuit of Fig. 20b,

$$h'_{fe} = h_{fe} \frac{R_D}{R_D + h_{ie}} \tag{100}$$

where h_{fe} = current gain of Q_2

and h_{ie} = input impedance of Q_2.

Equation (99) is similar to Equation (96) except that g_d has been neglected and the factor h'_{fe} has been introduced to account for the additional current gain of the bipolar transistor. The cascade circuit is useful for video amplifiers or RF amplifiers up to about 100 MHz. Noise figures of less than 2DB are realized at 100-200 MHz. (8).

THE POWER FIELD-EFFECT TRANSISTOR

Junction power field-effect transistors have some provocative characteristics for applications through VHF. Currently available units exhibit an output current (I_d) of one amp with an input current (I_g) of 1 nA, making them easier to drive than (17) their bipolar counterparts. (power supply regulators?). These new FETs can be turned on (5 ohms) and off (5000 megohms) in less than 20 nanoseconds (core drivers?), and they have zero offset voltage. (store and hold circuits?) (D-to-A ladder switches?) (17).

Conventional bipolar transistors suffer from a conflict of interests when it comes to power and frequency, because high current dictates large junction area and high feedback capacitance, while high voltage means large base width and reduced gain. In the FET, junctions can be kept small because current flows between the junctions rather than through them. Also, maximum voltage is determined by gate diode breakdown, and has no first order effect on gain.

The power FET looks pretty good as an RF amplifier. For one of the newest types, the calculated F_t is 1.5 GH_z (17). As a result of the low intermodulation distortion inherent in FETs in general, and the low noise resistance of these new high current devices in particular, an evaluation unit has demonstrated over 140 DB of dynamic range operating as an RF front end (17).

While currently available power FETs are not about to obsolete their bipolar predecessors, they are certainly worthy of investigation.

CONCLUSIONS

The field-effect transistor, or FET, as discussed in this report is an excellent choice for amplifier circuit applications requiring; high input impedance, low d-c input current, low harmonic distortion, low noise and zero d-c drift.

The characteristics which suit the field-effect transistor to these applications requirements are: reverse-biased diode input characteristic providing 10^9 to 10^{13} ohms d-c input resistance; square law transfer characteristic allowing only second order harmonic distortion; noise levels as low as $\overline{e}_{in}$ = 20 nv$\sqrt{Hz}$ at 10 Hz and NF < db, and d-c drift as low as 1 μv/°C when properly biased.

Those amplifier applications where field-effect transistors are now, or are destined to be widely used are (17) electrometer and charge sensitive amplifiers, low drift d-c amplifiers, RF and mixer circuits requiring low cross-modulation levels, low-noise audio, video, and RF applications, low distortion audio circuits, and high-impedance audio or video applications. Each amplifier application may be considered individually relating to pertinent field-effect transistor characteristics.

The field-effect transistor has been principally known for its high input impedance characteristic. The gate input impedance is a function of the physical size and quality of the gate junction. The d-c leakage current I_g of the junction FET may be below 1 pA at 30 volts (17); this is equivalent to 10^{13} ohms input impedance.

In biasing a field-effect transistor for extremely low gate current applications, the source follower configuration is best, as the gate-source voltage may be minimized over the range of input signal swing. Drain-gate voltage V_{DG} should also be the lowest practical value in order to reduce gate-drain leakage to a minimum. The operating gate current I_g is then less than I_p by an order of magnitude depending upon the gate-source V_{GS} and drain-gate V_{DG} voltages.

A single field-effect transistor connected in a common-source or common-drain configuration may be biased to operate with a true zero temperature coefficient. This characteristic is unique to field-effect transistors and is due to two counteracting temperature effects. One effect is, by now, well known in transistors as a temperature sensitive base-emitter voltage V_{BE}. The gate junction of a field-effect transistor exhibits the same approximate -2.2 mV/°C temperature dependence which causes the drain current to exhibit a positive temperature coefficient. Another effect is a negative temperature coefficient drain current due to decreasing carrier mobility. At one certain value of drain current, these two effects exactly cancel, and drain current and gate-source voltage remain constant with temperature.

A field-effect transistor is free of the noise generated in a conventional bipolar transistor; the source of noise in the latter is due to carrier recombination in the base. In the field-effect transistor, the current flow is simply majority

carrier flow just as in a metal conductor. Radiation reduces minority carrier lifetime thus degrading conventional transistors (13). The transconductance of field-effect transistor is independent of this lifetime and is therefore insensitive to this type of radiation damage (12).

Finally, due to such applications as have been described of the field-effect transistor, it is reasonable to say that had industry first concentrated on perfecting the field-effect transistor rather than the bipolar injection type now so prevalent, most circuits would be using field-effect transistors. Injection types would play a special role only-a complete reversal of the actual situation today.

REFERENCES

(1) Bockemuehl, R. R.
Analysis of field-effect transistors with arbitrary charge distributions, IEE Trans. on Electron Devices, Vol. ED-10, pp. 31-34, January 1963.

(2) Bockemuehl, R. R.
Field-effect modulation of photoconductance, J. Appl. Phys., Vol. 31, pp. 2256-2259, December 1960.

(3) Buckholz, W.
Biasing a FET for low drift, Electronics, p. 92, May 30, 1966.

(4) Bruncke, W. C.
Noise measurement in field-effect transistors, Proc. IEEE, Correspondence, Vol. 51, p. 378, February 1963.

(5) Cobbold, R. S. C. and Trofimenkoff, F. N.
Theory and application of the field-effect transistor, Proc. IEEE, Vol. III, No. 12, pp. 1981-1991.

(6) Cowles, Laurence G.
Measurement of FET pinch-off voltage, Proc. IEEE, p. 200, February 1964.

(7) Dacey, G. C. and Ross, I. M.
The field-effect transistor, Bell System Tech. J., Vol. 34, pp. 1149-1189, November 1955.

(8) Evans, A. D.
Analyzing high-input-impedance FET amplifiers, Electronic Equipment Eng., Vol. 11, p. 72, March 1963.

(9) Evans, A. D.
Characteristics of unipolar field-effect transistors, Electronic Industries, Vol. 22, p. 99, March 1963.

(10) Evans, L. L.
Biasing FETs for zero D-C drift, Electro-Technology, p. 94, August 1964.

(11) Gibbons, J. F.
Semiconductor Devices, McGraw-Hill Book Company, 1966. Chapter 6.

(12) Phillips, Alvin B.
Transistor engineering, McGraw Hill Book Company, 1962, Chapter 4.

(13) Radeka, V.
Field-effect transistor-its characteristics and applications, IEEE Trans. on Nuclear Science, pp. 358-364, June, 1964.

(14) Richer and Middlebrook.
Power law nature of field-effect transistor, Proc. IEEE, p. 1145, August 1963.

(15) Roosild, S. A., Dolan, R. P., and O'Neil, D.
A unipolar structure applying lateral diffusion, Proc. Inst. Electrical Electronics Engrs., p. 1824, 1963, 51.

(16) Sevin, S.
A simple expression for the transfer characteristics of a FET, Electronic Equipment Engineering (EEE), p. 59, August 1963.

(17) Sherwin, J. S.
Field-effect amplifiers, Electronic Communicator, p. 3, January/February 1967.

(18) Shockley, W.
A unipolar field-effect transistor, Proc. IRE., Vol. 40, pp. 1365-1376, November 1952.

(19) Uzunoglu, Vasil
Semiconductor network analysis and design, McGraw-Hill Book Company , p. 68, 1964.

(20) Van der Ziel, Albert
Electronics, Allyn and Bacon, Inc., p. 103, 1966.

(21) Wang, Shyh
Solid State Electronics, McGraw Hill Book Company, 1966, Chapter 3.

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List of Principal Symbols

BV_{dgs}	reverse-bias breakdown voltage
C_{DG}	gate-drain depletion capacitance of intrinsic device
C_{SG}	gate-source depletion capacitance
D	drain terminal
E_x, E_y	x and y components of electric field
F_T	cutoff frequency
G	gate terminal
g_m	mutual transconductance
g_d	output conductance of undepleted channel
I_{dz}	drain current for zero drift
i_g	small-signal gate current
I_p	pinch-off (saturation) current with gate shorted to source
I_g	gate input current (also input leakage current)
I_s, I_d	channel current
i_d, i_s	small signal drain and source current
L	length of active channel
N_A, N_D	doping densities of abrupt-junction
p(y)	impurity density $q(N_A-N_D)$
Q(y)	total channel charge when channel is entirely depleted
Q(t)	charge stored in channel depletion regions
q	electronic charge
SS	source terminal
t	depletion layer thickness
T_c	effective channel thickness

T_{hc}	half-thickness of channel
T_s	depletion layer thickness at the source
T_d	depletion layer thickness at the drain
V_D	drain-bias voltage (relative to source)
V_{DS}, v_{ds}	drain-to-source voltage
V_G	gate-bias voltage (relative to source)
V_{GS}, v_{gs}	gate-to-source voltage
W	width of channel
ε	dielectric constant
μ	mobility of majority carriers in the channel
ρ_f	free charge density of channel
ρ_s	space charge density (fixed)

THEORY AND APPLICATIONS OF FIELD-EFFECT TRANSISTORS

by

JOE WILLARD TOLIVER

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AN ABSTRACT OF A MASTER'S REPORT

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The junction field-effect transistor (FET) has a conducting channel that connects its source and drain terminals. The conductivity of this channel can be modulated by the electric field of the reverse biased gate-to-channel junction diode; thus the name junction field-effect transistor. Three characteristics of the junction field-effect transistor make it very attractive as an active semiconductor device. (1) Low gate current and thus high input impedance, (2) Low noise, and (3) Excellent stability.

The d-c theory and small signal properties of the junction field-effect transistor are presented analytically. The analysis is based upon an active transmission line analogy to the conductive channel of the FET. Within limitation of the gradual channel approximation, general expressions for the channel current, pinch-off voltage, mutual transconductance, output conductance, and junction capacitance are derived as functions of the depletion layer thickness at the device boundaries. Equivalent small signal circuits are obtained which describe the junction field-effect transistor characteristics in the region below pinch-off as well as in the pinch-off region.

The effects of temperature on the device are considered in detail. It is shown that provided certain conditions are fulfilled, the device can be biased so as to operate with almost zero drift over a wide temperature range.