AUTOMATIC TUNING OF Q-ENHANCED INTEGRATED DIFFERENTIAL BANDPASS FILTERS IN A SILICON-ON-SAPPHIRE PROCESS

by

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Abstract

In microchip circuitry, the tiny size of inductors creates low Q values, limiting a bandpass filter's ability to have narrow bandwidths at RF frequencies. To counter this problem and also compensate for losses, Q-enhancement can be implemented to facilitate narrower bandwidths and boost gain.

With Q-enhancement, temperature sensitivity of the circuitry causes the filter parameters to drift over time, making it necessary to adjust the filter periodically in order to keep the filter centered at the desired frequency. With the proper additional on-chip circuits used with a microprocessor, a tuning algorithm makes it possible to automatically tune the filter in-situ. The algorithm is based on increasing Q-enhancement until the filter begins to oscillate, reading the frequency of oscillation, adjusting to the desired frequency, and then decreasing Q-enhancement until the filter no longer oscillates.

A 500MHz single-pole differential filter was designed with an on-chip amplitude detector and frequency prescaler to facilitate tuning. The filter was made adjustable across frequency with banks of binary weighted switchable capacitors. Q-enhancement adjustment was achieved via banks of cross-coupled FETs, also binary weighted. The circuit was fabricated in 0.5μm silicon-on-sapphire technology. The finished filter chip was controlled with a PIC microprocessor which had been programmed in C with the tuning algorithm.

With the tuning algorithm in place, the filter was successfully able to align itself to within ±1MHz of the desired 500MHz center frequency. Q-enhancement levels were also able to self-adjust to maintain a desired bandwidth.

An improved design based around an off-chip coupled-resonator two-pole filter has also been designed. This filter includes adjustable coupling capacitance between the two poles, which also must be tuned. A new method of tuning is proposed for such applications. The properties of a two-pole filter cause it to oscillate at two frequencies with Q-enhancement. A modified amplitude detector is capable of reading the beat frequency which results from the two oscillations, a value which relates directly to and allows tuning of the bandwidth of the filter.

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Acknowledgements

In the Spring semester of 2008, the RFIC Design class at Kansas State University (class number ECE 765) set out to design a tunable single-pole Q-enhanced filter system. Proposed by Dr. William Kuhn, the system included three circuit sections: a differential filter core with Q and frequency tuning, an amplitude detector and a frequency prescaler. Each member of the 10-person class designed one section of the circuit and then compiled the designs into three full systems (with one extra filter core design). The author of this paper, a member of that class, originally designed a frequency prescaler section.

All three completed systems were compiled by the author and were fabricated. One of these prototype designs was chosen for testing, featured here in Chapters 3 and 4. This design was created by Thomas Weston Burress (filter core), Keith Albers (amplitude detector), and Joel Schonberger (frequency prescaler). The author would like to thank them for their contributions to the project.

Additional thanks are also due to Joel Schonberger for his help in programming the PIC and assisting with the tuning algorithm documented in section 4.2, and to Sandia National Laboratories for their encouragement and support of this research.

The author would like to extend many thanks to major professor Dr. William Kuhn, for passing on his extensive knowledge and passion about this field and this work in particular.

Thanks also to committee members Dr. Andrew Rys and Dr. Balasubramaniam Natarajan.

Dedication

For my grandpa, Lawrence Strouts,
who gave me a love of the science in the world around me
and made me a third-generation Wildcat.

CHAPTER 1 - Introduction

1.1 Objective

The objective of this research is to further the study of tuning in Q-enhancement in the hope that it will one day be used in industry. This goal is addressed in this thesis by fabricating, testing and automatically tuning a Q-enhanced filter, and by designing a next-generation Q-enhanced two-pole filter.

1.2 Why this research is necessary

With ever advancing technology, a continuing goal is to make circuits smaller and faster by making them as integrated as possible. One of the problems with integrated circuit (IC) processes is that the very tiny size of traces creates high resistances relative to non-integrated circuitry. When inductors are created from these tiny traces, the inherent resistance in the lines causes the inductors to have low quality (Q). The Q of an inductor is directly related to the achievable bandwidth of a filter using those inductors by the equation:

$$Bandwidth = \frac{f_0}{Q} \tag{1}$$

To achieve desired narrow bandwidths at radio frequencies (RF), one solution is to boost the Q of these inductors. This can be done by placing a pair of cross-coupled field effect transistors (FETs) in parallel with the inductor [5], as shown in Figure 1-1.

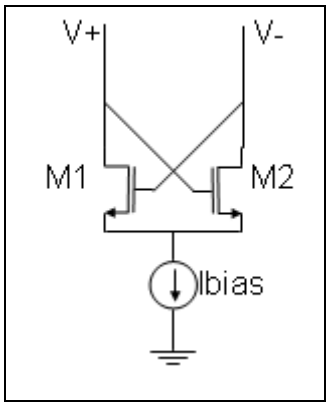

Figure 1-1: Cross-coupled FETs

These cross-coupled FETs behave as a negative resistance, counteracting the power losses within the physical resistance of the inductor.

The low fractional bandwidth achievable with these techniques in addition to the temperature sensitivity of the Q-enhancement circuitry creates a need for frequency tuning. Although there have been several publications in the last two decades on tuning techniques [2, 6, 7, 8], this area is still partially unexplored. In particular, there has been little work on tuning of multi-pole Q-enhanced filters. Therefore, this thesis concentrates on the problem of tuning, and a new technique for tuning two-pole filters is presented.

There are several known issues with Q-enhanced filters, such as low noise figure and limited dynamic range [13]. For these reasons, the filters presented here may not be suitable for preselect, image or other front-end filters. In this work, the filters are intended as IF filters, since lower noise figures are acceptable in that application.

CHAPTER 2 - Tuning in Prior Art

In order to counter process variations and adjust across temperature changes, it has long been acknowledged that Q-enhanced filters require some sort of tuning mechanism to regulate frequency and Q-enhancement.

In [6], a tuning setup requiring a second on-chip copy of the filter which is used as a VCO is demonstrated. This method involves tuning the copy, sampling and then holding the control signals until an idle space between transmit and receive cycles. The main filter can then be updated with new control signals as the copy is turned off to keep the VCO signal from leaking into the transmissions. The downsides here are that the second copy uses twice the space and additional power.

In [7], second-order RF Q-enhanced bandpass filters are reported which function in the 5GHz band. The filter is digitally tuned by performing a Fast Fourier Transform (FFT) on the output of the filter while in oscillation. The FFT is analyzed and the frequency is adjusted. After the frequency is set, the FFT continues to run while Q is decreased in order to account for any changes in frequency due to the Q components. Finally, amplitude is measured to further adjust for Q. A possible problem with this method is that it requires the filter to be disconnected from transmitting or receiving during the tuning process. However, the authors of [7] also declare that digital transmissions can accommodate the necessary disconnection time. The tuning setup required downconversion of the output signal, conversion from analog to digital format, and GPIB linkage to a PC which ran the FFT. The tuning was implemented using an Altera FPGA. The FFT process was reported to take 52 μS on the PC.

In [2], a self-tuning technique for a single-stage Q-enhanced filter is described. This utilizes the same disconnect-during-downtime method as described above, but employs a simpler tuning method based in analog circuitry.

In [8], Nakaska et.al. utilize this simpler technique, with some modifications, to tune a series-coupled shunt-resonator filter. Here, a three-pole cascaded filter was tuned, with one pole at a time undergoing tuning according to the algorithm. The algorithm was run on an FPGA. The filter also required manual tuning of the coupling capacitors between stages for optimal frequency response. In [9], the same author theorizes that tuning time for that application would be just over 1 mS. Analog tuning of varactors was used.

This work also bases a tuning algorithm around the simpler analog solution proposed in [2]. To adapt this technique for automatic tuning of a two-pole coupled filter, the algorithm must be expanded to include tuning of the coupling capacitors in the filter, an approach which is new to this field. Automatic tuning of this capacitance allows a user to tune the filter for a wide variation of bandwidths in-situ, making it ideal for applications such as software defined radio.

CHAPTER 3 - Automatically-Tuned Q-Enhanced Single-Pole Filter

3.1 Q-Enhanced Filter Prototype

In the spring of 2008, the 10 members of the EECE 765 class at Kansas State University class designed three Q-enhanced filters and the additional circuitry necessary to facilitate automatic tuning. The author, a member of this class, fixed problems with the circuits, made them more robust, and collected all the designs into one die for fabrication. The design was fabricated in the 0.5µm FC Peregrine Semiconductor Silicon-on-Sapphire (SOS) process.

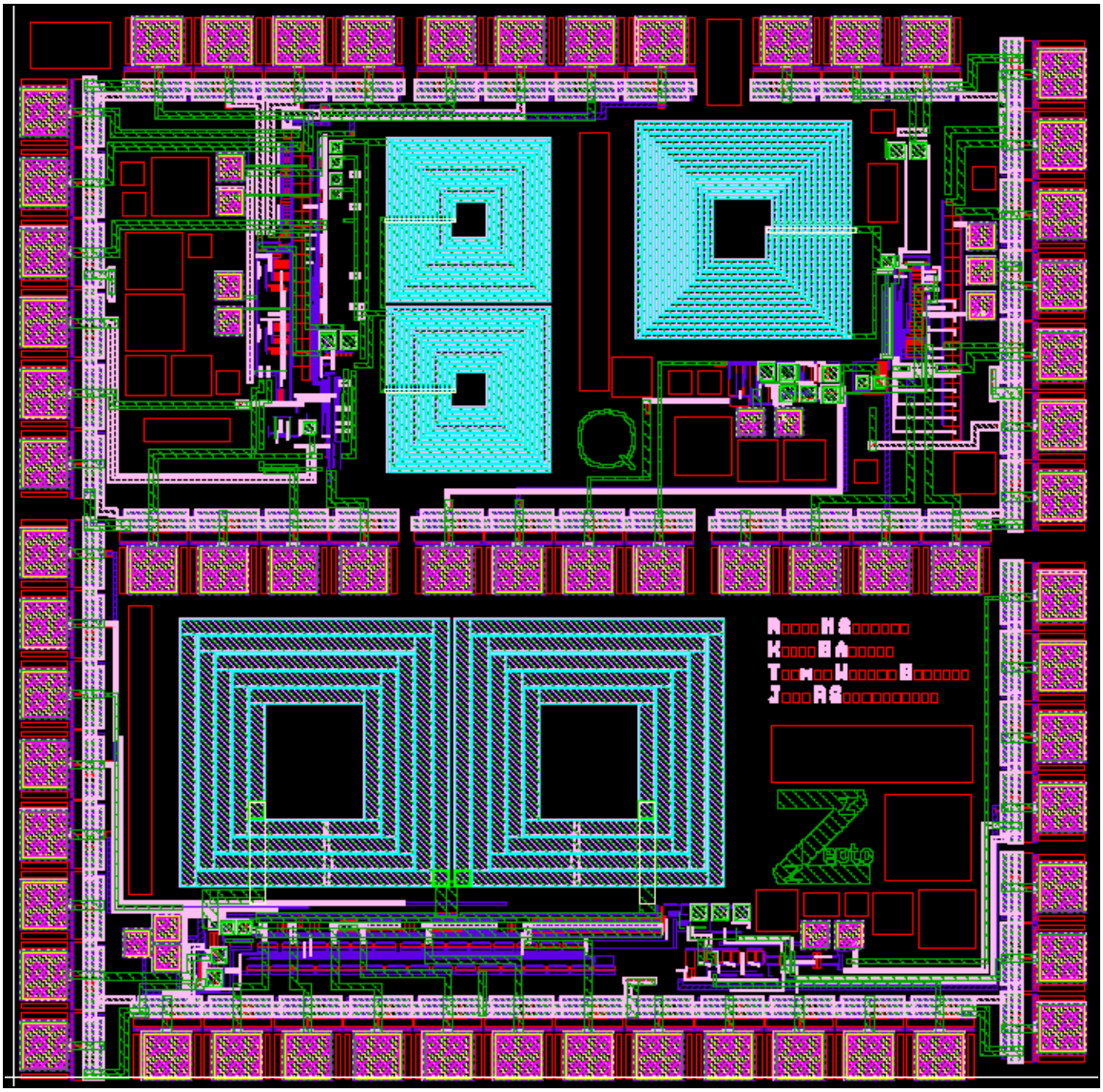

Figure 3-1: Design Layout

All three designs were tested and the best performing one was chosen for further testing and application of the tuning algorithm. This design was originally created by Keith Albers, Thomas Weston Burress and Joel Schonberger.

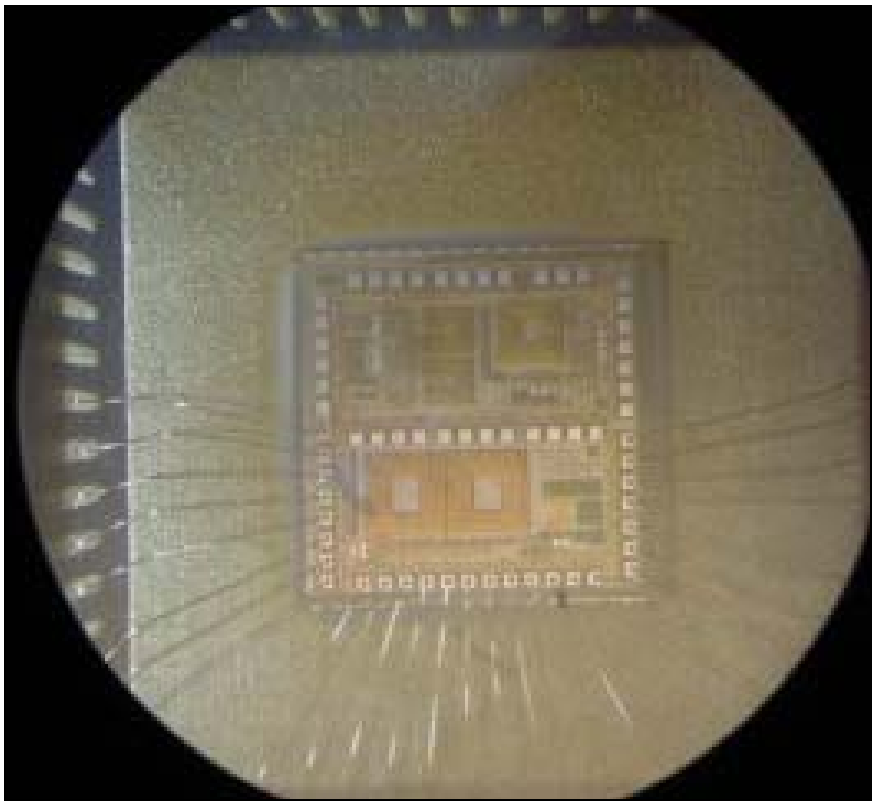

Figure 3-2: The fabricated chip

A picture of the fabricated and bonded chip can be seen in Figure 3-2. All three designs fit into a 3mm x 3mm chip space. The design used in the majority of testing in this research can be seen in the lower half of the die and occupies approximately 4.7mm^2, though this includes 0.6mm^2 of filler space.

This filter was designed to operate at a 500MHz center frequency with a bandwidth of 10MHz. The relationship between bandwidth B, center frequency f_o, and quality factor Q is given by the well-known expression:

$$B = \frac{f_0}{Q} \tag{2}$$

A Q value of 50 is needed for this bandwidth. Since achievable Q values for inductors in the selected process are on the order of 10 at this frequency, some enhancement is clearly needed. The sections below detail the Q-enhancement circuits employed and the related tuning elements.

3.2 Operational Overview

The system is composed of three distinct circuits: a differential filter with Q- and frequency tuning circuitry, a frequency prescaler, and an amplitude detector. An off-chip microprocessor is also necessary in order to run the tuning algorithm.

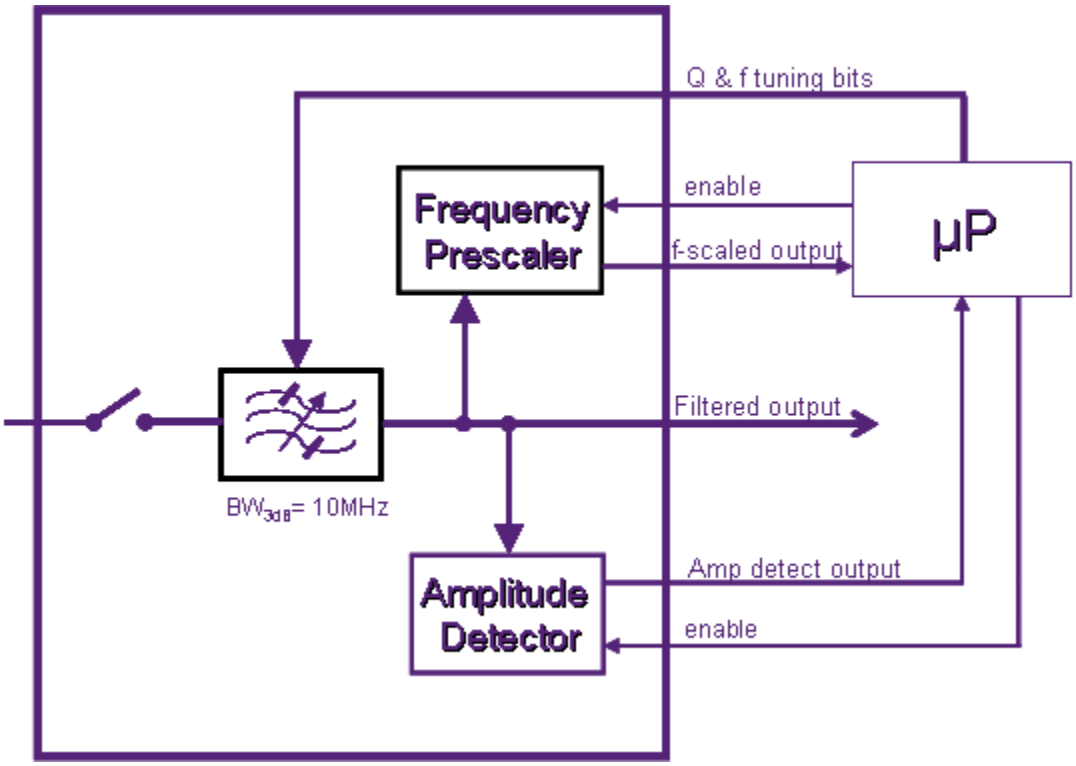

Figure 3-3: Block Diagram of self-tuned filter

The overall block diagram is shown in Figure 3-3. The tunable filter is at the center of the diagram. The differential output of the filter feeds into both the amplitude detector and the frequency prescaler. Each of these parts has outputs which feed signals necessary for the tuning algorithm to the microprocessor. The microprocessor runs the algorithm and updates the Q and

frequency tuning control bits as necessary, as well as enabling and disabling the frequency prescaler and amplitude detector when a tuning cycle begins or ends.

The principles of the algorithm run as follows:

1) Disconnect the input to the filter
2) Turn on the amplitude detector and frequency prescaler
3) Have the microprocessor adjust the Q until an oscillation is detected by the amplitude detector
4) Read the frequency from the prescaler
5) Adjust the frequency control inputs to get the correct frequency
6) Repeat steps 3 and 4 until the frequency is correct
7) Decrease the Q until the amplitude detector no longer detects an oscillation
8) Decrease Q by an additional fixed amount to achieve the desired bandwidth
9) Shut off the amplitude detector and frequency detector
10) Reconnect the input to the filter and resume normal operation

3.2.1 Q-Enhanced filter core

A simplified schematic of the filter core is shown in Figure 4. At the core of the filter is a basic cascoded differential long-tail amplifier. Designed by Thomas Weston Burress, this section of the circuit is based on the design described in [2]. Inputs come in at the gates of M2 and M3 and the signal is amplified through the two legs of the circuit. At the top of the amplifier is an LC tank circuit.

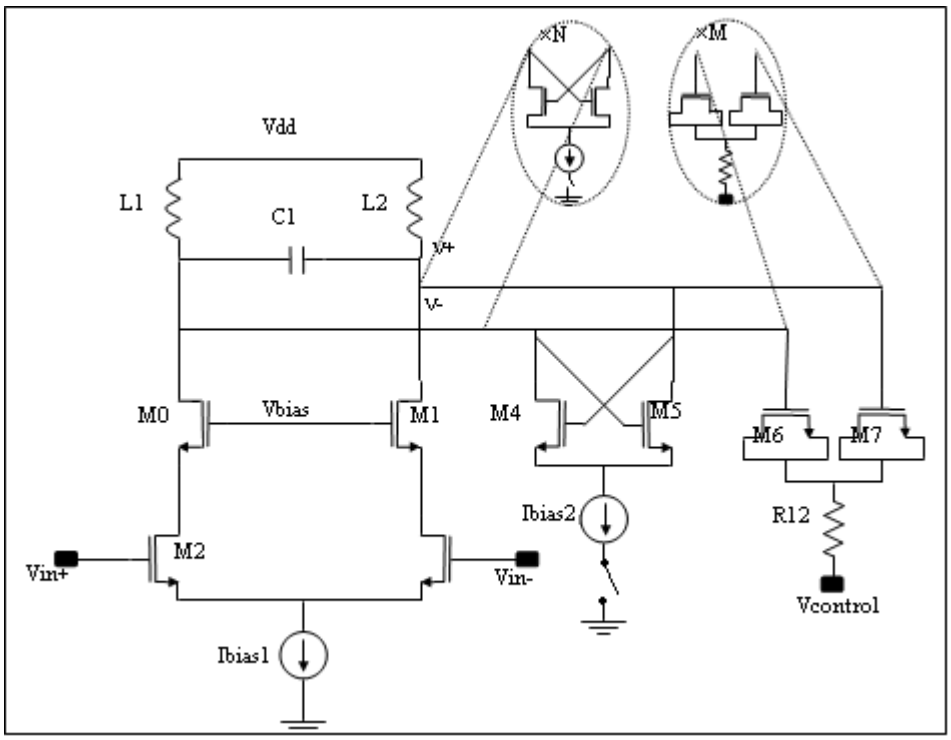

Figure 3-4: Filter core schematic

In parallel with the inductors are frequency-tuning cells and Q-tuning cells. The frequency tuning cells work on the principle of adding more capacitance in parallel with the fixed C1 to increase total capacitance and change the resonance frequency of the filter. For this reason, C1 is designed with less capacitance than necessary to achieve 500MHz. The frequency tuning may then add capacitance, allowing for tuning both above and below the desired center frequency. As these tuning cells must be switchable, they are created from two series connected MOScaps with a center tap. The gates of these FETs have a DC voltage of vdd. When a voltage of 0 is placed on the sources/drains of these FETs via R12, the resulting gate-source voltage forms channels which become the lower-plates of the capacitors. The differential topology causes them to act like a single capacitor with a value of half the capacitance of one FET. To shut off these capacitors, a vdd voltage is placed at the sources/drains, causing the gate-to-channel voltage to be below threshold and the channel is not formed. In this state, there is a minimum capacitance present, determined by component parasitics – particularly gate-to-source/drain fringing and overlap elements.

The Q-tuning cells are created from pairs of cross-coupled FETs. This arrangement behaves as if it were a negative resistance. The amount of negative resistance generated by one of these cross-coupled pairs is given by the equation:

$$R = \frac{-2}{gm} \tag{3}$$

where *gm* is the transconductance of the FETs involved. This circuit partially cancels the equivalent series resistance inherent in the inductors and boosts the Q factor, where Q is related to series resistance R_s and reactance X by the equation:

$$Q = \frac{X}{R_s} \tag{4}$$

These cells are controlled by switching on and off the current source at the tail of the cross-coupled pairs.

Both Q and frequency tuning cells are set up with binary weighting. The frequency tuning has 7 bits of tuning, so the 7^{th} cell has 64 times the capacitance of the first, providing 128 tuning steps. The Q tuning has 5 bits of tuning, providing 64 steps.

3.2.2 Frequency Prescaler

Based on the prescaler in [4], this circuit was designed by Joel Schonberger. The frequency prescaler exists to divide the oscillating frequency down to a frequency that is detectable by a microprocessor. Since available microprocessors need an input on the order of 20MHz or less, this frequency prescaler features a division of 40. A 500MHz frequency will then be scaled to 12.5MHz.

At frequencies within the UHF band, such as 500 MHz, typical digital flip-flop circuitry will not work. To achieve division at 500MHz, the frequency prescaler makes use of current

mode logic (CML) latched comparators. These can be made to have very similar operation to a standard D latch, but they function at the higher frequencies and have constant current draw.

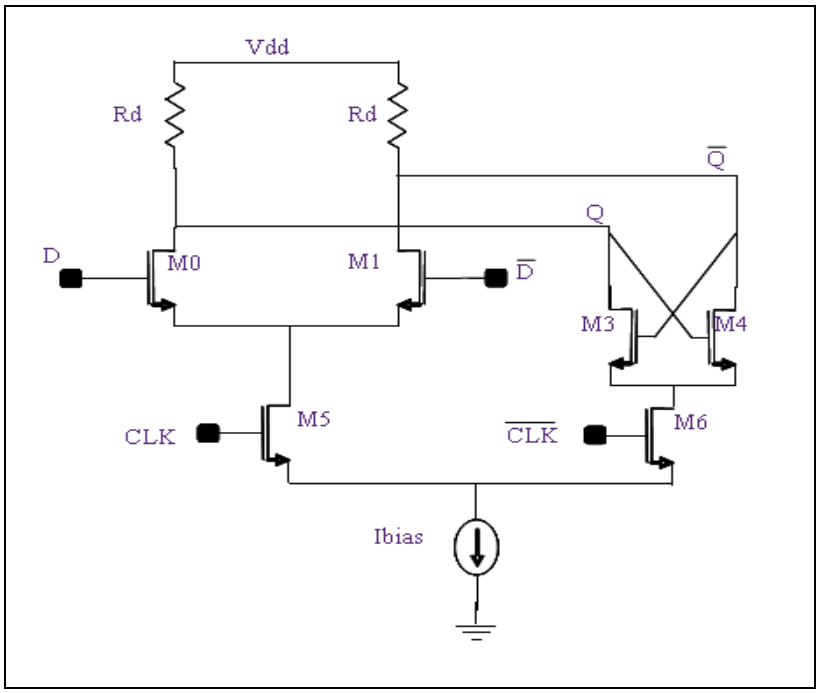

Figure 3-5: CML latched comparator schematic

The latched comparator in Figure 3-5 is a combination of a common-emitter differential pair amplifier made with M0 and M1 and the cross-coupled pair of M3 and M4. The differential pair is controlled by the "clk" signal, and the cross-coupled pair is controlled by "clknot", the inverse of "clk". When "clk" is high, the amplifier side of the circuit is enabled and current flows through M0 or M1, depending on the state of the input signal D. Hence, one drain will be high and the other low, and the latch can be considered to be in its pass-through mode. When "clk" is low, the cross-coupled pair switches on, and the circuit enters the latching mode. Though this piece of the circuit has the same arrangement as the Q-tuning cells mentioned above, it serves a different purpose here. When presented with a signal where one side is higher than the other, it exaggerates this difference. Given the previous analog value of the Q outputs, it quickly raises or lowers the voltage in each leg to the corresponding rail. To this extent, the circuit acts much like a comparator, indicating which leg of the circuit is higher at the time when the cross-coupled pair is enabled. The "clk" signal here is not actually a clocking line, but the

oscillating output of the filter. By suitably selecting Vgs overdrive values for the differential pair during design, the circuit can latch with very small input amplitudes.

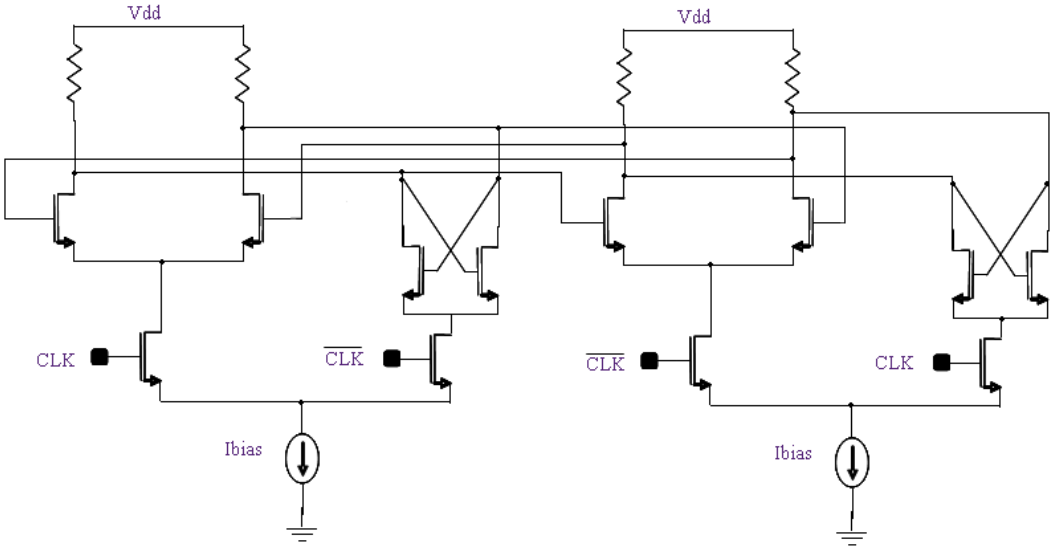

Figure 3-6: CML master-slave divide-by-two circuit

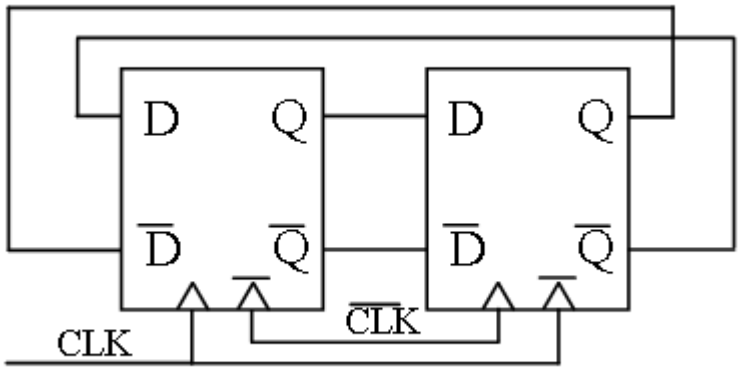

Figure 3-7: Digital master-slave divide-by-two

When two of these latched comparators are connected in a configuration as shown in Figure 3-6, they behave like a traditional digital master-slave divide-by-two circuit, such as that shown in Figure 3-7.

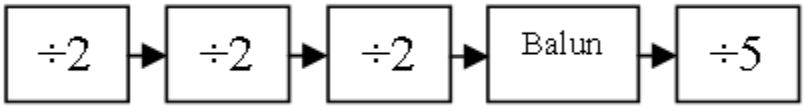

Figure 3-8: Frequency Prescaler division flow

In the present system application, three divide-by-two stages are connected together by feeding the differential outputs of the previous stage into the clock lines of the next, to form a divide-by-8 prescaling operation. Now that the signal is 1/8 its original frequency, it is a sufficiently low frequency to function with normal digital circuitry. Digital master-slave flip-flops have no need of the differential signal, so in order to maintain the full signal swing of the original signal, the outputs of the latched comparator stages are first fed into a balun, shown in Figure 3-9. Once turned into a single-ended signal, it is given a final division of 5 using the circuit shown in Figure 3-10.

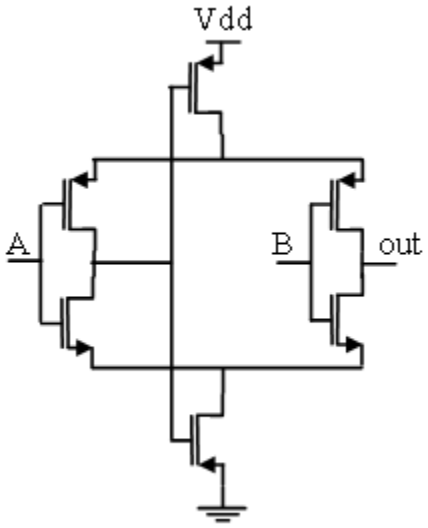

Figure 3-9: Balun

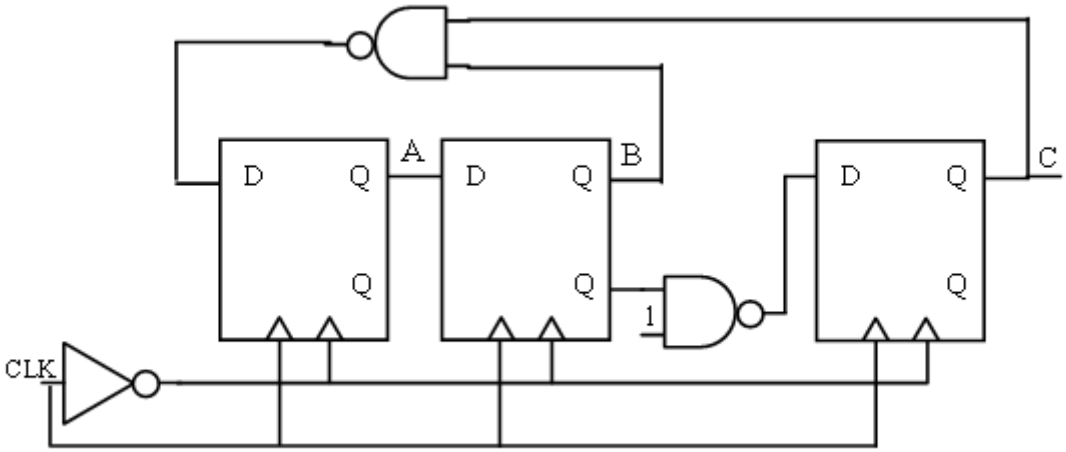

Figure 3-10: Digital divide-by-5 block diagram

To provide low output resistance to the microprocessor inputs, the final signal is fed through a buffer comprised of four cascaded, exponentially scaled inverters with a scaling factor of 4.

3.2.3 Amplitude Detector

The purpose of the amplitude detector is to provide a measureable output to determine when the filter is oscillating. In this case, a steady DC voltage is provided which has a negative relationship to the amplitude of the oscillation.

Designed by Keith Albers, this design was a modification of the amplitude detector described in [3].

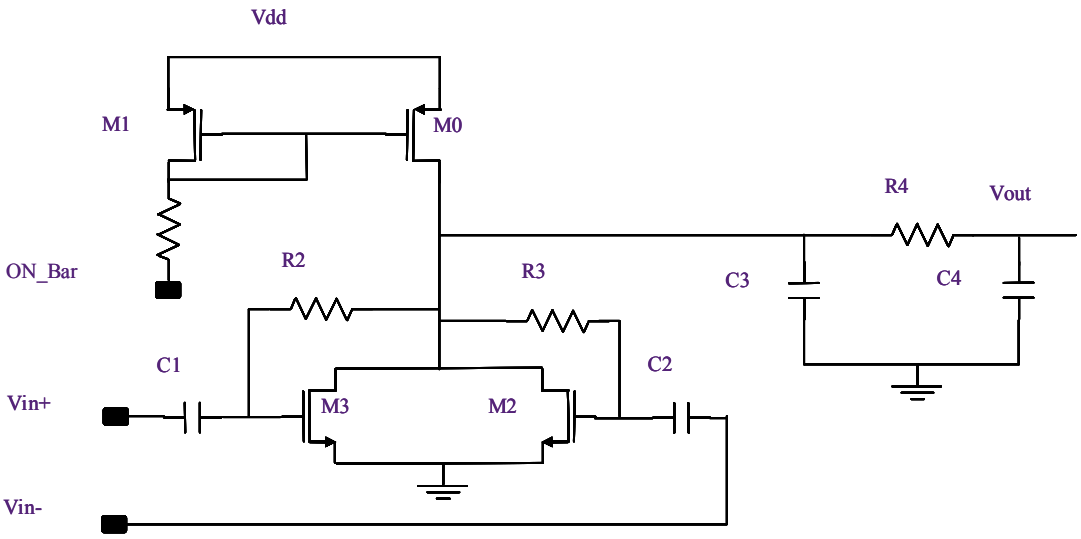

Figure 3-11: Amplitude detector schematic

A schematic of the amplitude detector is shown in figure 3-11. In design, the gates of M3 & M2 are biased near threshold for good sensitivity. Initially the current from M0 is split evenly by M2 and M3, and the threshold voltage plus Vgs overdrive of these devices at this current sets the DC output value. When the input signal on one side swings down, that FET begins to cut off. As the voltage on the opposite side swings upward, current through that leg increases to compensate. However, due to the square-law characteristic of drain current versus Vgs, the resulting output voltage will be less at the drain (since the component from V_{in} cancels from the differential structure). The simulated graph of the input amplitude vs. the output DC level is shown in Figure 3-12.

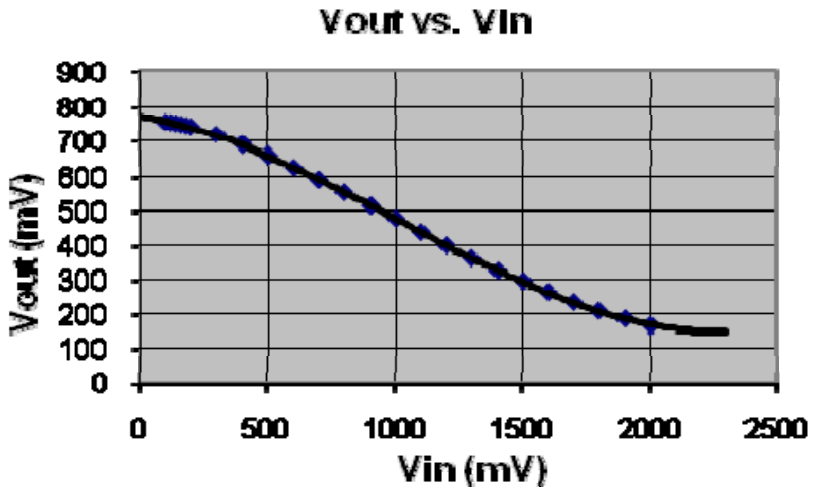

Figure 3-12: Amplitude Detector output curve

A basic lowpass RC filter at the output removes the 500MHz signal, passing the DC level through to the off-chip microcontroller.

CHAPTER 4 - Testing of Single-Pole Filter

The filter from the ECE765 class described in the previous chapter was tested by the author of this thesis, in collaboration with Joel Schonberger. It was first tested using manual tuning to assess the performance of the sub-blocks. A board was created using DIP switches as controls for all frequency and Q tuning inputs, as well as the enable pins, as shown in Figure 4-1.

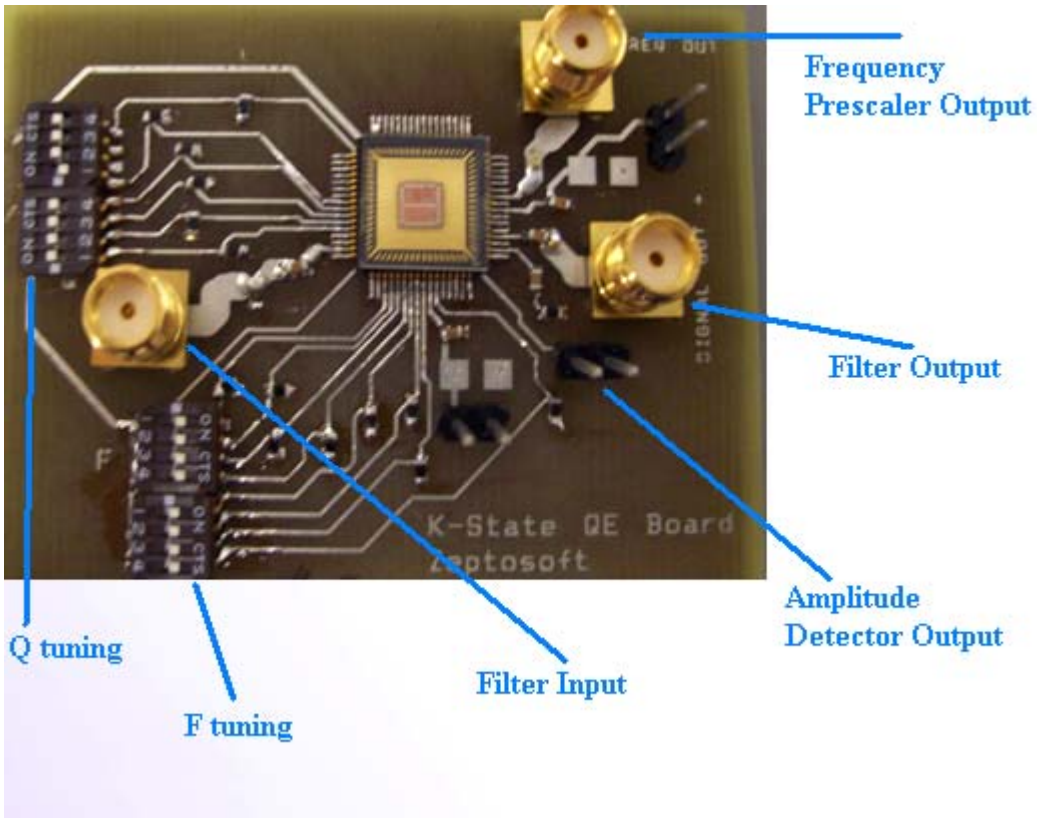

Figure 4-1: Manual testing board

This allowed for direct manual tuning of the filter over the entire achievable range of frequencies and Q-enhancement levels.

It was discovered during this initial test that the oscillations out of the filter were compressing at a much lower power level than needed or expected. The fault was determined to be the final stage of the filter's output buffer – biased at too high a voltage and not sourcing enough current, the oscillations from the filter were clipping and not providing enough power. This output was insufficient to run either the amplitude detector or the frequency prescaler.

At this point, it became a major advantage that the output of the filter and the inputs to the amplitude detector and frequency prescaler were all the same node. The filter outputs were able to be used as inputs to test the functionality of the amplitude detector and frequency prescaler, a process which also allowed for testing over the full range of the supporting circuits and not just the oscillations available from the filter.

4.1 Results

Switching on the Q-enhancement banks caused the bandwidth of the filter to narrow and gain to increase as expected, as shown in Figure 4-2. The upper left frame shows the filter shape with no Q-enhancement, with the lower right frame showing the shape with the most Q-enhancement possible without causing the filter to oscillate.

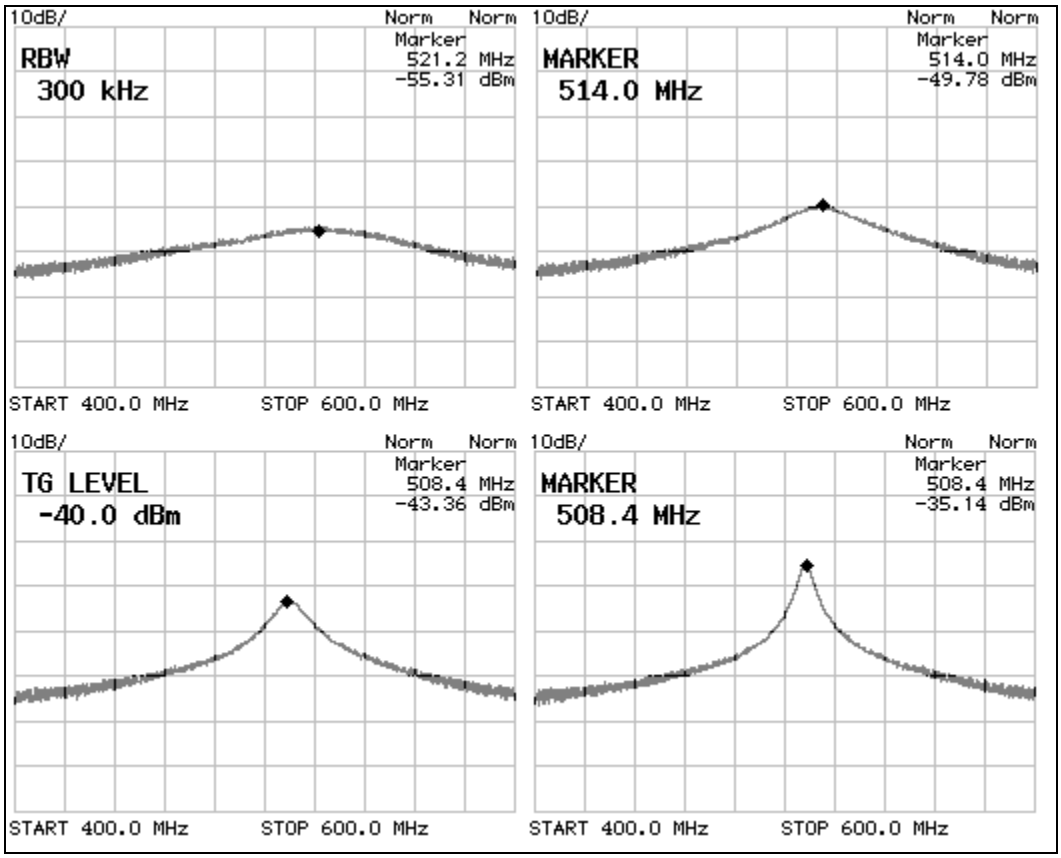

Figure 4-2: Filter shape with various levels of Q-Enhancement

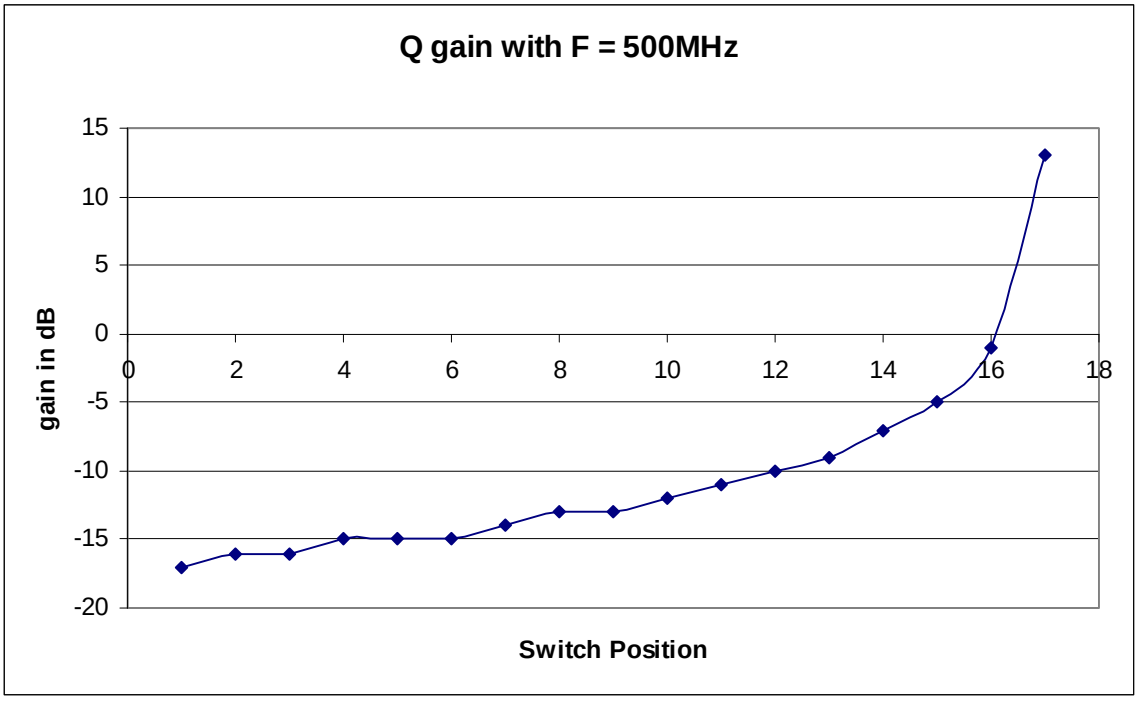

Figure 4-3: Gain achieved from Q-Enhancement

As seen in figure 4-3, Q-enhancement boosts the gain of the filter. Gain here is measured with a -40dBm input signal from a tracking generator. The peak on the right at switch position 17 is not truly a gain, but actually where oscillation begins. Data here was recorded with the frequency setting necessary for a 500MHz center frequency.

Figure 4-4 shows this oscillation with Q-enhancement at maximum. It was discovered during testing that the filter can be made to oscillate at any frequency by engaging just the MSB of the Q-enhancement. This is important for the robustness of the filter. At higher temperatures, the Q of the inductors and the effectiveness of each Q-tuning cell decreases, requiring more banks of Q-tuning to be turned on in order to achieve the same enhancement. Since the MSB represents half the available enhancement, the filter should be able to function over the necessary range of temperatures and process variations.

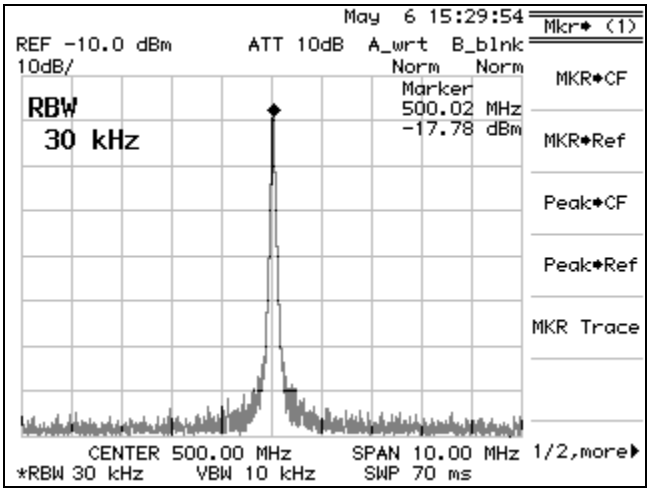

Figure 4-4: Oscillation with frequency tuning set for 500MHz

Figure 4-5 illustrates the output level from the oscillation. The -40dBm point is not true oscillation. At this point, there is significant gain in the filter, amplifying the noise in the circuit to a -40dBm level. The next Q-enhancement setting allows the signal to truly oscillate to a level where the circuit saturates at above -25dBm. At maximum Q-enhancement, the signal saturates near -18dBm.

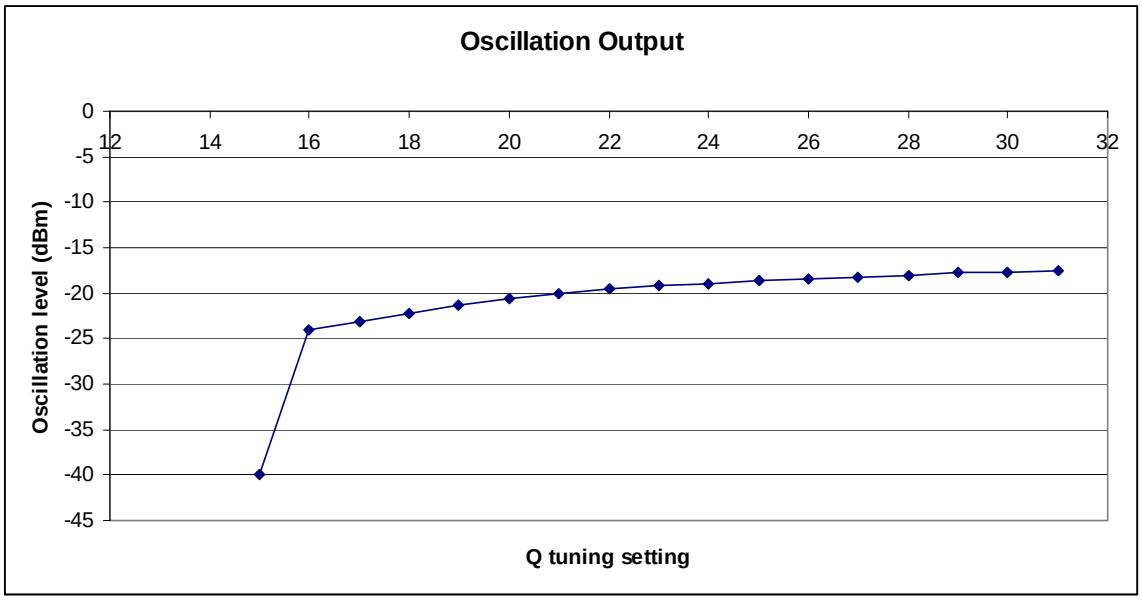

Figure 4-5: Oscillation level over range of Q-Enhancement

As seen in Figure 4-6, frequency tuning controls have a negative relationship to the output frequency. When more tuning bits are switched on, more capacitance is added to the filter, decreasing the frequency of operation. The desired center frequency was 500MHz. This is achievable, as the final output tunes between approximately 475 MHz and 595 MHz. This is not an exact range, because the actual frequency value is also affected by the Q setting. The tuning is very close to linear as seen in Figure 4-6, with the 500MHz setting marked in red. Frequency tuning steps are approximately 1 MHz apart.

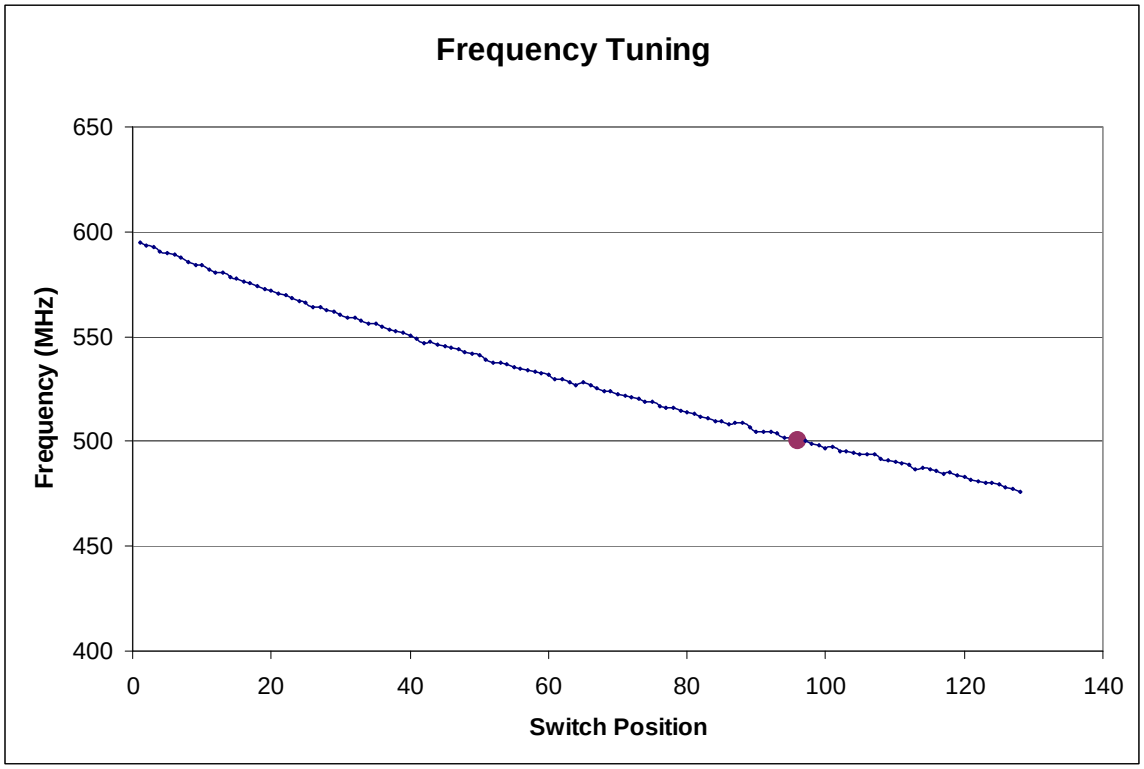

Figure 4-6: Frequency Range

Figures 4-7 and 4-8 show the filter response at opposite ends of the tuning range. It is important to realize that the frequency and Q tuning are not independent and that getting a specific bandwidth may require different settings at different frequencies. Here, the Q-enhancement was set to the maximum level without causing oscillation, which required a different setting for each frequency. The Q-enhancement setting for the lower frequency was 15, while the higher frequency required less Q-enhancement at setting 10.

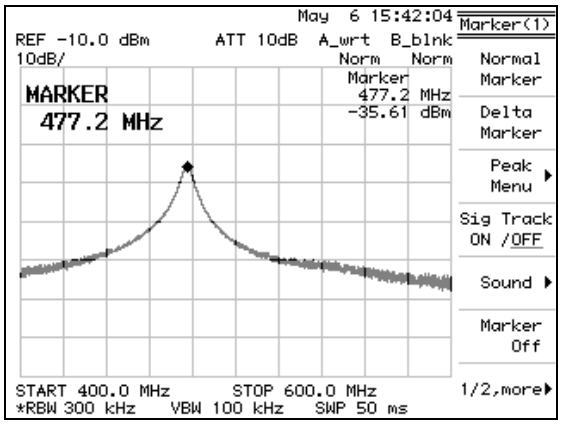

Figure 4-7: Filter response at low end of frequency tuning with Q level = 15

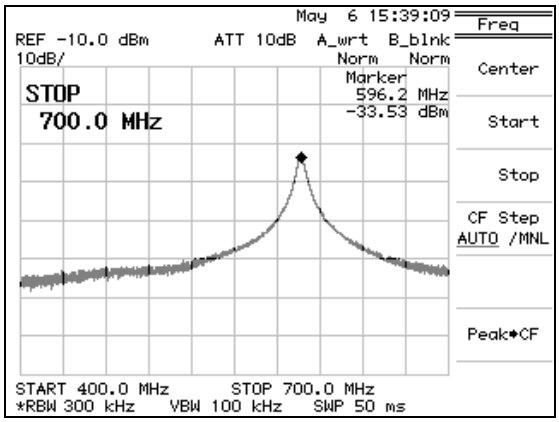

Figure 4-8: Filter response at high end of frequency tuning with Q level = 10

The fact that these settings change over frequency makes the function of the amplitude detector critical. When the amplitude detector signal drops, the microprocessor will know it can read the center frequency. Figure 4-9 shows the response of the amplitude detector's output to a 500MHz injected signal.

It is worth noting that the microprocessor does not need the amplitude detector output to have a specific voltage. Since the inputs are disconnected when running the algorithm, the ambient noise in the filter is below the detection range of the amplitude detector. Any sufficient oscillation will cause the output of the detector to drop, and it is only necessary that the microprocessor be able to recognize a change in the output. It is also important to note here that the amplitude detector implemented on this chip requires an input of at least -5dBm before any recognizable drop occurs. With the current oscillation saturation of -18dBm, the filter stage is

unfortunately not capable of tripping the amplitude detector. A workaround to this problem was developed, however, as explained in Section 4.2.

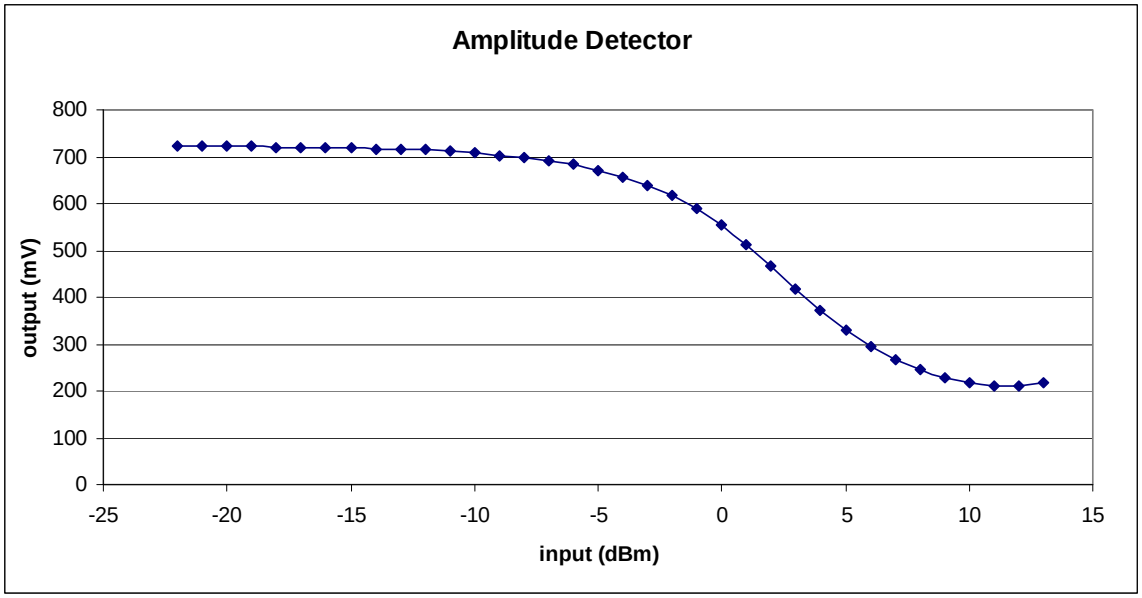

Figure 4-9: Amplitude detector output

Figure 4-10: Frequency prescaler output

The output of the frequency prescaler is shown in Figure 4-10. Given a strong enough input signal, the frequency prescaler properly demonstrated a divide-by-40 operation, displaying a 12.5MHz signal for an input of 500MHz. With insufficient input power, the frequency

prescaler will output a very noisy oscillatory signal. In this design, all parts of the frequency prescaler circuit – both analog differential sections and digital single-ended sections – were placed on the same power supply. This power supply was isolated from the main power in order to prevent the rail-to-rail signal swings from interfering with the main filtering circuit. However, it is likely that the frequency prescaler interfered with itself due to large signal swings in the single-ended output dividers feeding back to the low-level CML dividers to cause the oscillatory signal. A signal of +6dBm was required to override this self-oscillating tendency. Given the necessary input power, the frequency prescaler is capable of dividing signals up to 600MHz.

4.2 Self- Tuning Algorithm

In order to run a complete algorithm, it became necessary to boost the power out of the filter. With the oscillating output of the filter at -18dBm and the amplitude detector and frequency prescaler needing at least -5dBm and +6dBm respectively, a single chip was incapable of supporting the full algorithm. A second test board was designed using two copies of the microchip, shown in Figure 4-11.

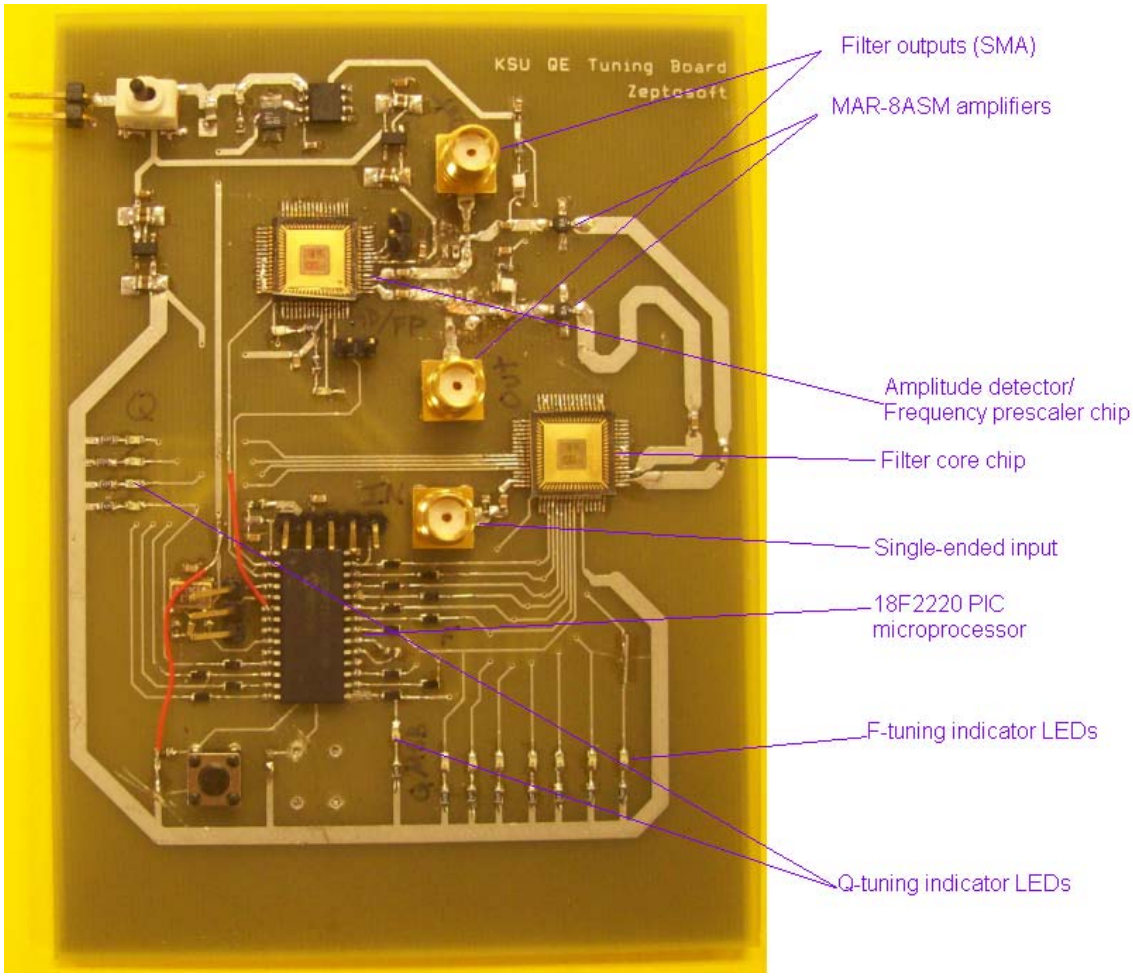

Figure 4-11: Test Board for running algorithm

The first chip in the line acted as the filter and was controlled by the frequency and Q-tuning inputs. The differential output from the first copy was amplified by approximately 26 dB

using MAR-8ASM amps from Minicircuits, and fed to the filter output/amplitude detector and frequency prescaler inputs of the second chip. The frequency prescaler and amplitude detector outputs were fed to an 18F2220 PIC microprocessor to use as inputs for the tuning algorithm which controlled the first copy. Code for the algorithm was written in C code and the PIC was programmed via a PIC Kit 2.

Because Q and frequency tuning settings were now chosen by the PIC and not selected manually, banks of LEDs were placed on the frequency and Q tuning lines so that a user could visually determine what the final settings were.

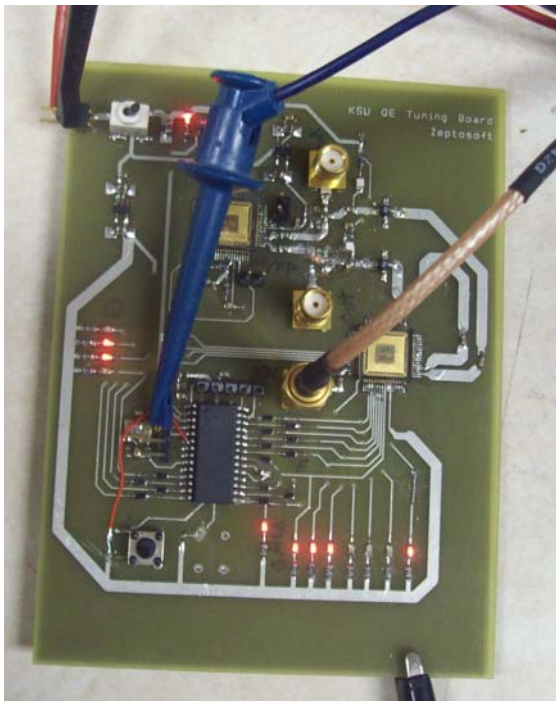

Figure 4-12: Test board connected to equipment, showing LED indicators

It was discovered on this new board that the MSB of the q-tuning did not engage. Since the lower frequencies of operation require more Q-enhancement to oscillate than do the higher frequencies, the circuit could no longer be made to oscillate at frequencies less than about 560MHz while at room temperature. Due to an extremely limited number of available chips, the decision was made to not try to replace or otherwise switch the chips on the board, as everything

else was working as expected. A new center frequency of 578MHz in the middle of the operable range was therefore chosen for purposes of demonstrating the algorithm.

Because of timing limits in this particular PIC, the divided frequency out of the frequency prescaler was brought in on the PIC's internal prescaler and scaled again by a factor of 8. This brought total division of the original frequency up to 320.

To fully demonstrate the algorithm, the inputs of the filter were hooked up to a spectrum analyzer with tracking generator through an RF switch. In addition to directly plotting the shape of the filter, the tracking generator's sweeping input also emulated signals in an actual application of the filter. The PIC controlled the RF switch, disconnecting the inputs from the filter at specified times in order to run the algorithm. In this way, the PIC was able to demonstrate a real-world application, where the algorithm is only allowed to run during a specified down-time.

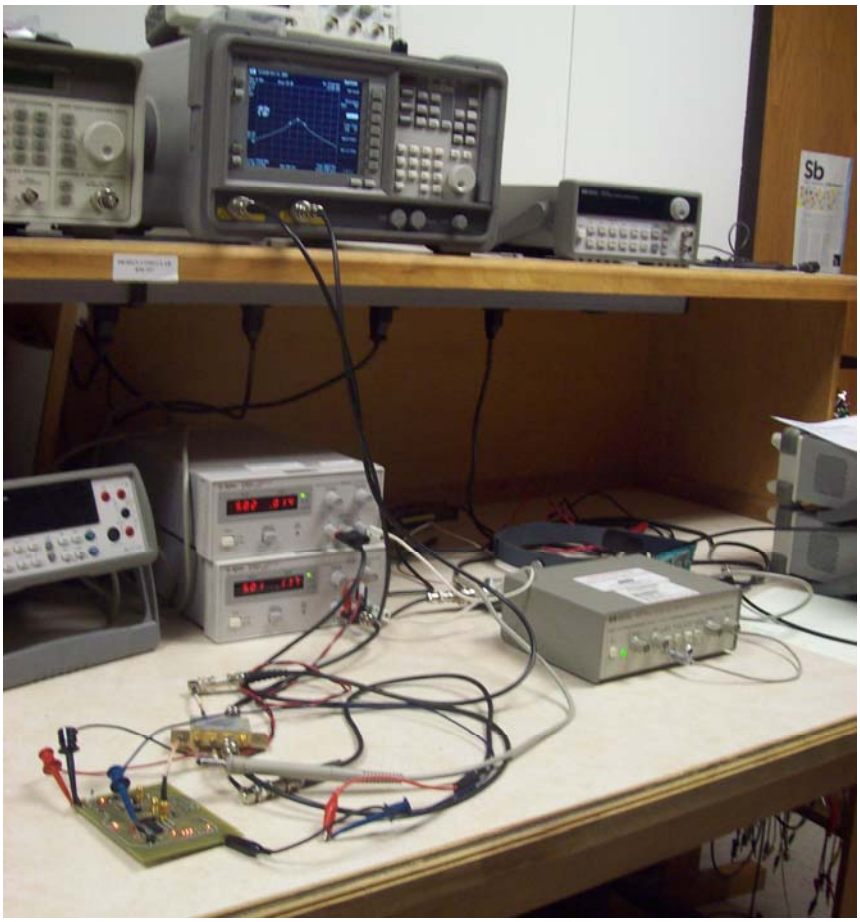

Figure 4-13: Bench setup

A binary search was used to determine necessary Q-enhancement and frequency settings. At the beginning of an oscillation check cycle, all Q-enhancement is set to zero, ensuring that the filter is not oscillating. The value of the amplitude detector's output is recorded at this point as a "non-oscillating" reference. When increasing Q to make the filter oscillate, the algorithm runs through the Q-tuning settings in a binary search manner until a setting is found where the output of the amplitude detector is between 15 and 25 mV less than the non-oscillating reference value. The algorithm then records the Q-tuning setting as the "lowest oscillating" level.

Once the critical oscillation point has been located, the zero-crossings from the frequency prescaler output can be counted. In the final version of the algorithm, the PIC counts for 500μS. Once the PIC has this count, it compares it to the stored count for the desired frequency. If the frequency is more than 10MHz away from the desired frequency, a coarse-tuning loop is run; otherwise a fine-tuning loop is used. Like the oscillation loop, this coarse tune is also a binary

search. The fine-tuning loop also runs after a coarse tuning. The fine loop is an incremental loop, stepping values up one at a time.

When the algorithm has tuned the filter to the proper center frequency, it returns the Q-enhancement level to a setting two levels less than the "lowest oscillating" level recorded earlier to ensure that the filter no longer oscillates, and to set the bandwidth to the desired amount.

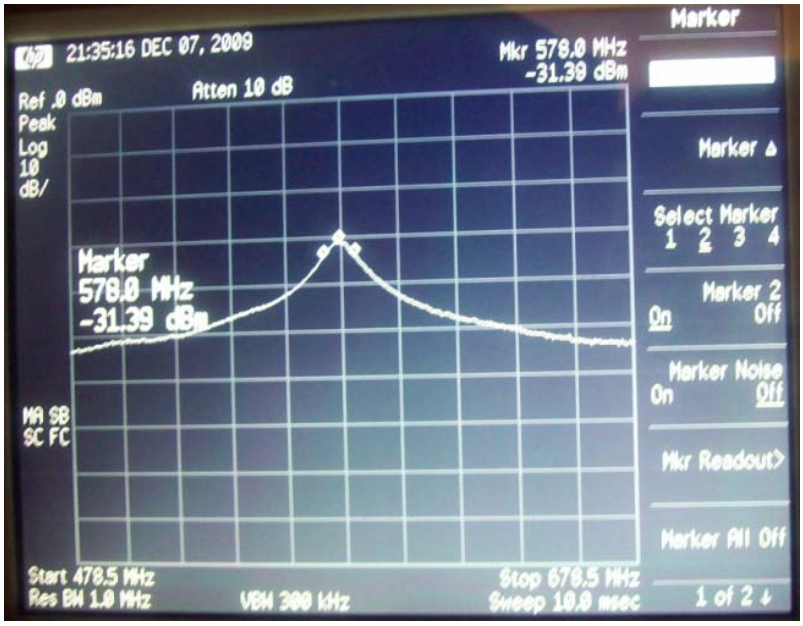

Figure 4-14: Filter shape after automatic tuning

After running the tuning algorithm, the filter was correctly tuned to a center frequency of 578MHz, with a 3dB bandwidth of 12MHz. When testing over temperature, the upper limit for which the filter was also able to successfully tune to the proper center frequency and bandwidth was 29°C. The nonfunctional Q-enhancement MSB is main reason the circuit was unable to tune at higher temperatures. With increasing temperature, the gm of the FETs decreases, lowering the effectiveness of the cross-coupled Q-enhancement pairs. So, with higher temperatures, more bits of Q-enhancement are required to achieve the same overall Q value. With the MSB broken, the circuit was already operating near the upper threshold of achievable Q values. On an identical board with a functioning MSB, the upper temperature threshold will be much higher. The circuit was tested to a low temperature of 19°C, the lowest temperature achievable with available equipment, but is capable of functioning at much lower temperatures. At decreasing temperatures, the circuit requires less Q-enhancement. There is a theoretical lower limit of

tuning functionality; it will occur either when the center frequency drifts so far as to be out of the tuning range, or when engaging the LSB of the Q-tuning causes the filter to oscillate, undercutting the necessary tuning thresholds.

The final version of the algorithm flows as follows:

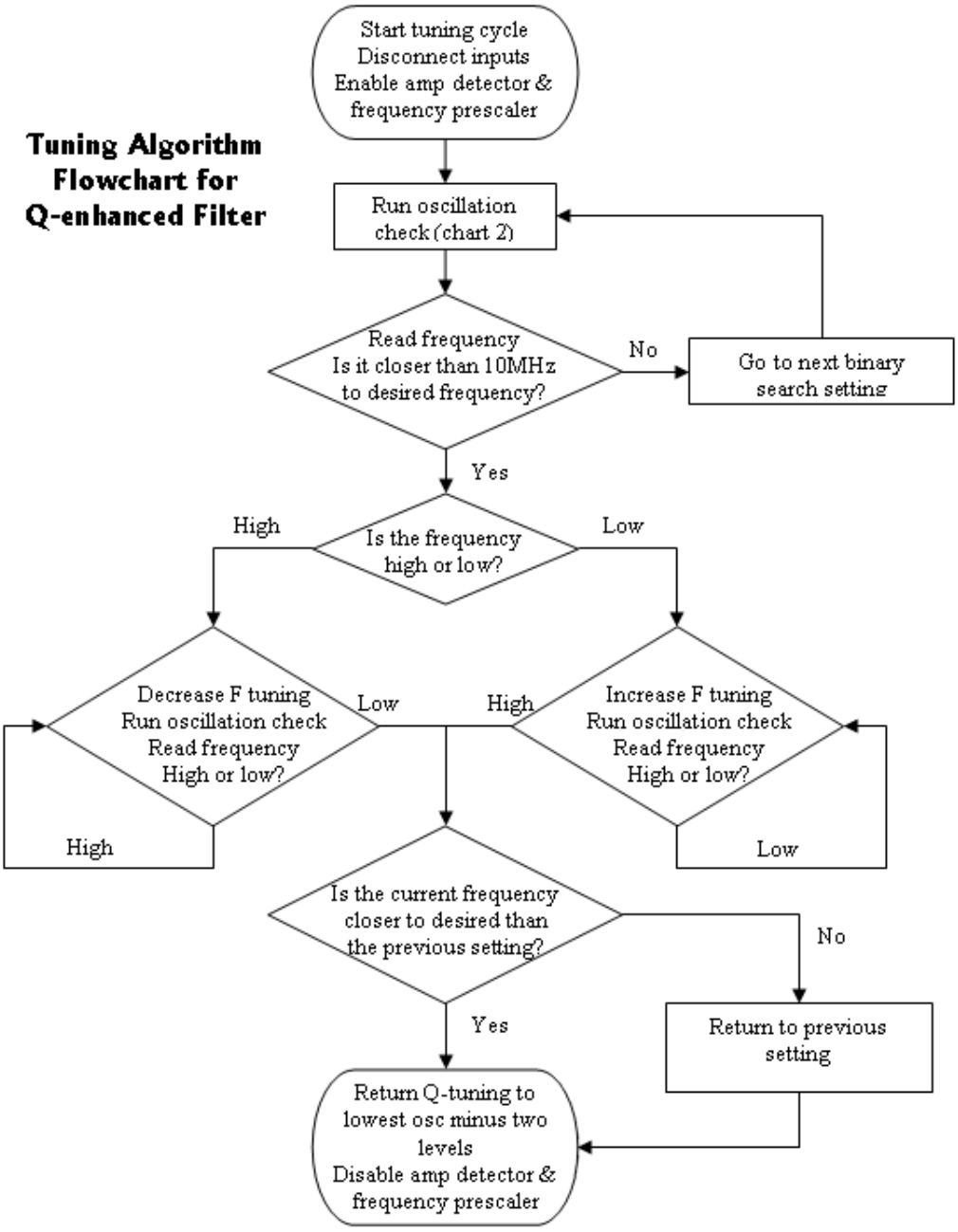

Figure 4-15: Tuning Algorithm Flowchart-Main Chart

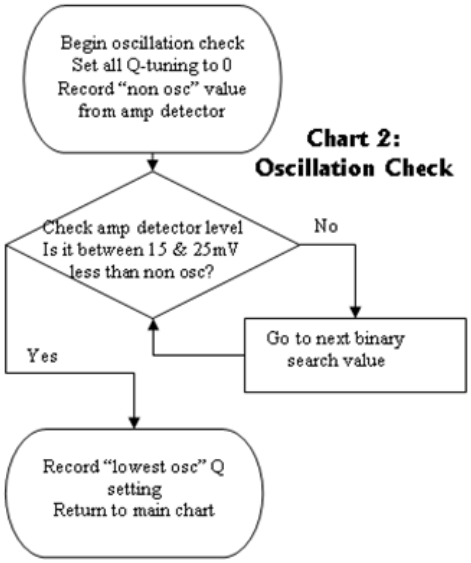

Figure 4-16: Tuning Algorithm Flowchart – Oscillation Chart

4.3 Tuning time

The time required to re-tune the filter is an important factor in determining whether or not a filter is usable in industry. Since the inputs must be disconnected during tuning, any system utilizing this filter must be able to accommodate this "down-time". For example, a system using time-division-multiplexing would be appropriate if and only if the tuning time is less than the duration between assigned timeslots.

4.3.1 Counting time

The longest delay encountered during tuning arises from the time it takes the microcontroller to count zero crossings to determine the frequency. The equation used to describe this is:

$$Accuracy = \frac{div}{t_c} \tag{5}$$

Where *Accuracy* is the frequency accuracy in Hz, t_c is the counting duration in seconds, and *div* is the factor by which the original signal was divided. For an accuracy of 1MHz (10% of our desired bandwidth setting), the counting duration for a divisor of 320 is 320μS. In actual tuning of the filter, 500 μS was used. Significantly shorter times could be achieved if the prescaling ratio is decreased.

4.3.2 Ring-up

Each time the frequency or bandwidth of the filter is adjusted, the circuit requires a finite amount of time to adjust to the change. This is much like when a filter is hit with an impulse and ring-up or ring-down time can be used as an approximation.

A transfer function of the filter with midband gain H_o, bandwidth B in radians/second and center frequency ω_o in radians/second is given by:

$$H(s) = \frac{H_o B s}{s^2 + Bs + \omega_o{}^2} \tag{6}$$

The inverse Laplace transform of this equation is the impulse response of the filter, which has the shape of a damped cosine. The damping coefficient ζ of that impulse response is given by:

$$\zeta = \frac{B}{2\omega_o} \tag{7}$$

One time constant, τ, can be found using the equation:

$$\tau = \frac{1}{\zeta\omega_o} \tag{8}$$

In this system with a bandwidth of 10MHz and a center frequency of 500MHz, the damping coefficient is equal to 0.01. This creates a time constant of approximately 32ns. The system will be 95% adapted to its new settings after 3 time constants, creating at delay of at least 95ns every time a parameter is changed.

With the binary search in place, the worst-case number of iterations to achieve the correct frequency is $\log_2(n)$. The n value here is 2^7, or 128, making the algorithm take up to 7 iterations before finding the correct frequency. However, every time the frequency is changed, the system runs through an oscillation check as well, requiring another binary search. The oscillation check is done over 32 bits, making a worst-case iteration of 5.

Assuming the worst for every possible search, the total delays incurred in the system are:

$$delay = (7 \times 5) \times 95ns + 7 \times 320\mu s = 2.24ms \tag{9}$$

While this is somewhat long in comparison with typical system timeslots, it is not a lower-bound and can be improved. For example, the 320us multiplier can be decreased through improved frequency counting circuitry.

CHAPTER 5 - Design of Two-Pole Coupled Filter

5.1 Overview

A next-generation version of the filter has been designed. This filter represents an improvement over the previous design in that it utilizes a capacitively-coupled two-pole resonator. In addition to providing a two-pole shape with a "flat" passband, this design also presents the opportunity to automatically tune the filter for a specified bandwidth. This filter has been designed within the Peregrine Semiconductor 0.25μm GC process, a smaller process than the previous design. A block diagram of the new filter is shown in Figure 5-1.

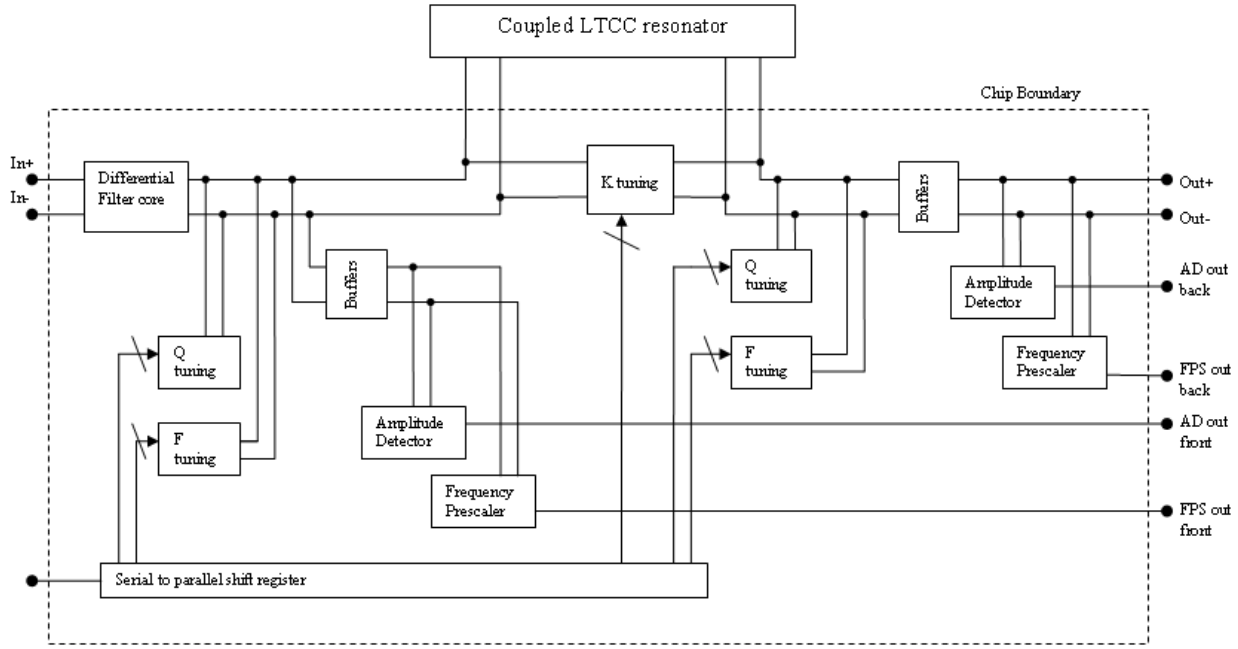

Figure 5-1: Block Diagram

Intended for a center frequency of 500MHz, this filter design will also have adjustable bandwidth from 10MHz to 1MHz, requiring Q values of 50 to 500. Like the previous filter, the input signal first comes into a differential amplifier that feeds to a resonator. The new resonator here is an off-chip differential center-tapped two-pole capacitively-coupled design to provide improved starting Qs.

This two-pole design adds an additional layer of difficulty to the algorithm in the form of the coupling capacitors between the sides of the resonator, which also must be tunable (marked

as “K tuning” on the diagram). As there are two sides of the resonator, the need arises to Q-enhance and frequency-tune each side. To that end, there are separate binary-weighted banks of Q and frequency tuning cells on each side of the filter (referred to from this point on as the “front” and “back” sides.) Because front and back sides will need to be tuned separately, each side also has its own amplitude detector and frequency prescaler. Not only is this separate tuning a critical functionality for the algorithm, but it provides for the ability to adjust for inherent mismatch between the off-chip components for better balance between the two sides. Due to the large number of control pins required for all the tuning capability, a serial to parallel shift register is used to reduce total pin count.

5.2 Advantages of the Two-Pole Resonator

This filter is designed to work with the resonators described in [10]. With an expected Q of 40 in the process from this reference, the low-temperature co-fired ceramic (LTCC) inductors start at a higher Q value than the expected Q of 10 for on-chip inductors, requiring less on-chip enhancement and achieving better dynamic range [13]. However, there is sufficient enhancement available with the new design to be able to handle lower Q values. The prototype of this filter will be capable of being tested using commercial-off-the-shelf (COTS) surface mount components. The external resonator also allows for the possibility of switching the inductors and capacitors to different values in order to achieve a different center frequency or other different desirable traits.

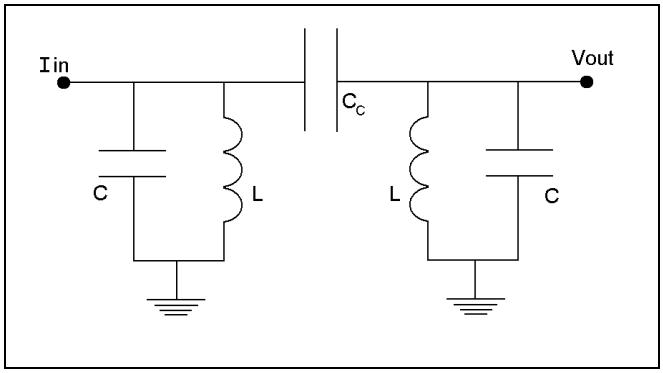

Figure 5-2: Single-ended two-pole coupled resonator

A basic two-pole single ended capacitively coupled filter is shown in Figure 5-2. In a single-pole filter such as the filter tested earlier in this work, Q-enhancement causes the filter to oscillate at the center frequency of the filter. With this coupled filter, increasing values of Q-enhancement beyond the necessary value causes something much like over-coupling of the filter, creating the characteristic shape with passband ripple, as seen in Figure 5-3.

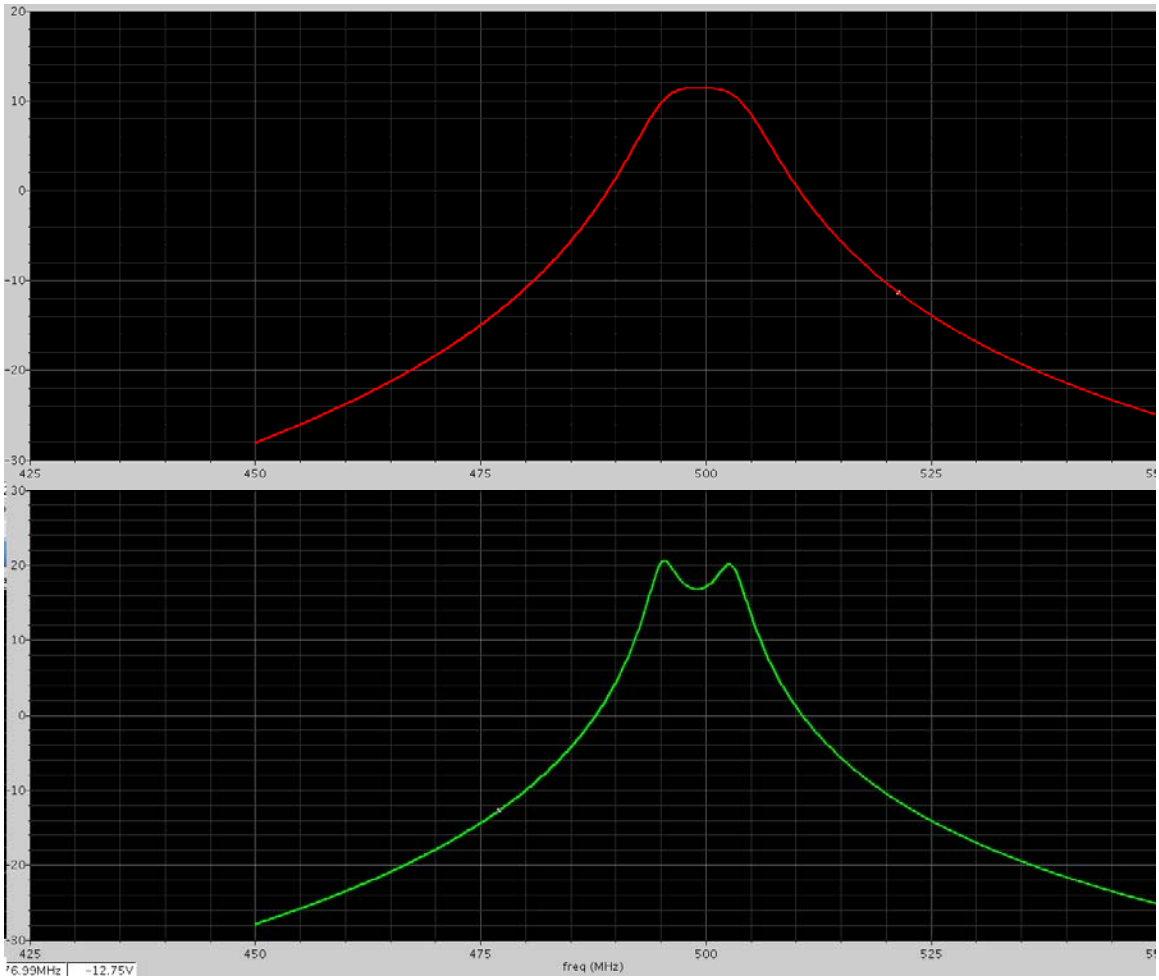

Figure 5-3: Normal coupled filter response (top), over-coupled filter response (bottom)

Further Q-enhancement causes the filter to oscillate at two frequencies situated near the edges of the bandwidth, as seen in Figure 5-4. When these two frequencies add together during oscillation, it creates a signal with a beat, also shown in Figure 5-4. The amplitude detector, a piece of the circuit already in place to perform part of the algorithm, can be very simply modified

to track this beat frequency. Therefore, by reading the frequency from the output of the amplitude detector, an estimation of the bandwidth of the filter can be determined without the need to inject any signals.

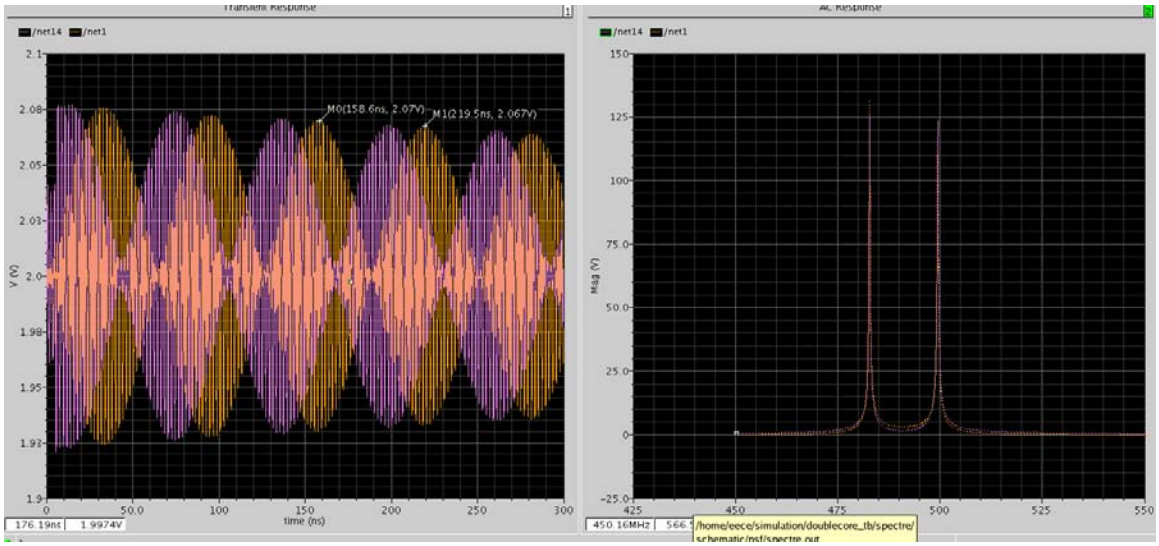

Figure 5-4: Beats created from two oscillating frequencies (left), over-Q-enhanced filter response (right)

In order to have a "flat" passband in a coupled filter, the capacitance between the two sides must fulfill a critical coupling criterion [11]. For a single-ended capacitive-only coupled filter, the equation with C_{crit} as the critical coupling value, Q_{eff} as the enhanced Q value, ω_o as the center frequency in radians and L as the inductance value is given by:

$$C_{crit} = \frac{\sqrt{2}}{2Q_{eff}\omega_o^2 L} \tag{10}$$

In the present design, the impedance of each tank circuit at resonance was chosen to be 1k Ohm, giving an inductance value of 6.4 nH. For a bandwidth of 10MHz and a corresponding effective Q of 50, the coupling between the sides must be approximately 0.18pF. It is important to note that the coupling here is not independent from the capacitance in parallel with the inductors. For a resonator at a given frequency, the coupling capacitance added to one parallel capacitor must add up to the total capacitance needed if one side were a single LC filter.

The capacitors are not the only mechanism which couples the filter together. There is also magnetic coupling created between the inductors, traces on a circuit board, or other components. The capacitive coupling must be able to cancel out the magnetic coupling and then re-couple the filter to a critical level.

By tuning the capacitive coupling so that it nearly cancels out the magnetic coupling, the two sides are effectively decoupled, essentially creating two separate filters. The sides can then be enhanced to oscillation and tuned separately.

For the purposes of Q-enhancing the resonator, a differential center-tapped resonator is used, shown in Figure 5-5. The differential resonator has other advantages, such as the advantages derived from attaching capacitors corner-to-corner across the resonator as discussed in the next section.

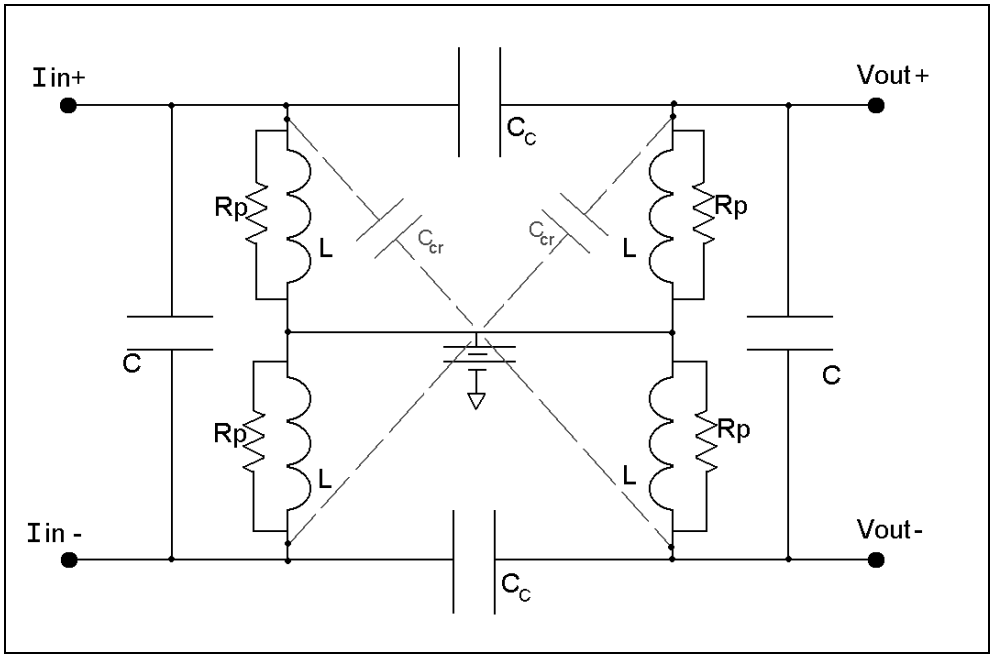

Figure 5-5: Differential coupled resonator with corner-to-corner capacitors

5.3 Adjustments in the Circuit Components for Two-Pole Design

5.3.1 K-tuning cells

Four binary-weighted banks of capacitors are used in this design: two banks connected directly across the resonator (C_C) and two corner-to-corner banks (C_{cr}) as shown above in Figure 5-5. Connected as they are to opposite sides of the differential filter, these corner-to-corner banks of capacitors have the ability to feed signals of opposing polarity back through the normal signal paths, effectively decreasing or cancelling resonator coupling in various ways.

The corner-to-corner capacitive banks are useful for several reasons. First, in the event that the capacitance between sides is higher than expected to the point where the minimum capacitance for the directly coupled banks is still too high, the corner-to-corner banks can be used to "subtract" capacitance from the coupling capacitance. This is important for the lower bandwidths (i.e. 1 MHz), when the two sides of the filter must be very loosely coupled. Second, the four banks of capacitors are designed with identical widths, lengths and layouts. The inherent parasitic capacitances in the different banks will be very similar after fabrication. With the corner-to-corner capacitors feeding back an opposite signal, the corner-to-corner banks cancel out the parasitic capacitances in the directly coupled banks, allowing for a truer "zero" capacitive coupling.

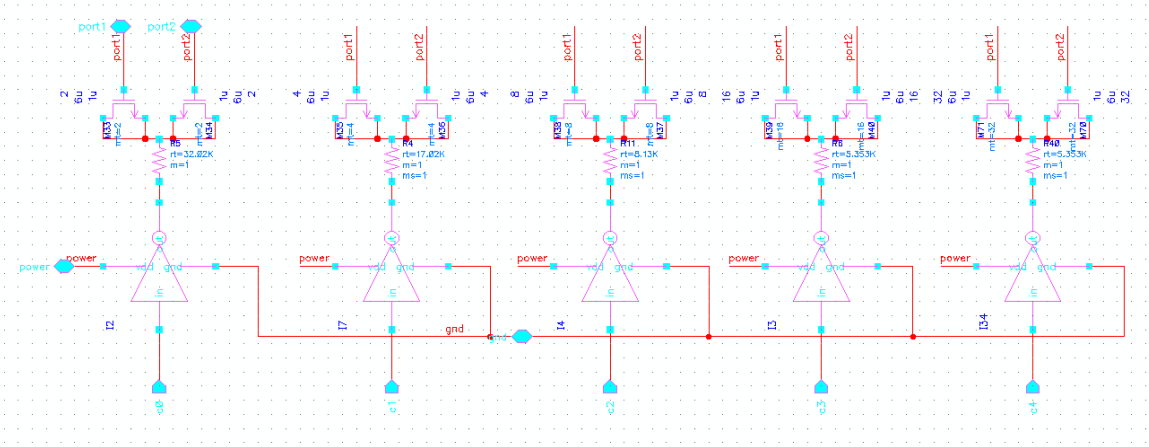

Figure 5-6: Capacitive bank schematic

Created as switchable capacitors, each individual binary-weighted capacitor is made up of two MOScaps, center tapped and switched on and off by an external high or low signal. The schematic is shown in Figure 5-6. Binary weighting is achieved by doubling the width of each pair of successive FETs. The gates of the FETs are all connected to the "ports": the off-chip connections to the inputs and outputs of the resonator. With a center tap on the resonator at 2V, there is a constant DC value of 2V at the gate of each FET in the capacitive bank. To turn on a capacitive "bit", a high signal is applied to the control line. Passing through the inverter, the corresponding low signal applied to the drain & source of each FET creates a voltage drop from the gate, activating the capacitor. The "off" state is achieved when a low signal is applied to the control, creating a high signal at the drains & sources. With 2.5V at the source/drain and 2V at the gate, the circuit can tolerate up to 1Vpp signal levels without inadvertent capacitor formation on signal peaks.

5.3.2 Q-Enhanced filter core

The differential amplifier core, very similar to the design used in the single-pole filter design, is shown in figure 5-7. The amplifier was designed for an unenhanced gain of approximately 10. This circuit draws about 6mA.

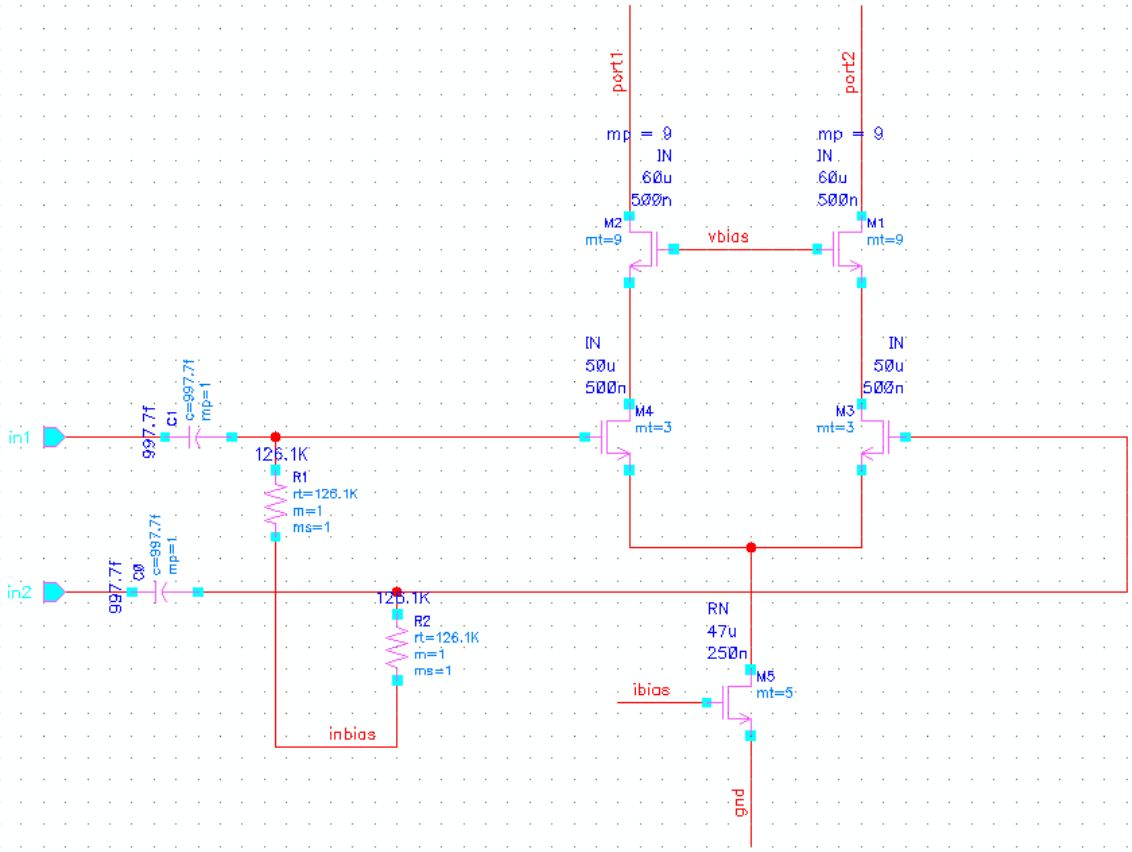

Figure 5-7: Differential amp schematic

The gain of the amp is given by:

$$A_v = 2 \times gm \times R_p' \tag{11}$$

where gm is that of the core FETs' gm and Rp` is the total resistance in parallel with the filter along one leg of the amplifier. Q is related to Rp` by the equation:

$$Q = \frac{R_p'}{X} \tag{12}$$

Increases in Q correspond to increase in Rp`, raising the overall gain of the filter.

The value of the parallel resistance is given by

$$R_{p'} = R_p \,//\, -\frac{1}{g_{m(QE)}} = \frac{R_p}{1 - g_{m(QE)} R_p} \tag{13}$$

where gm here is that of the Q-enhancement FETs in the cross-coupled pairs. A single cross-coupled pair is shown in Figure 5-8. Banks of Q-tuning are created by making binary-numbered multiple copies of the single pair. There are 7 bits of binary-weighted Q-tuning, meaning first bit controls one copy of the cross-coupled pair and the 7^{th} bit controls 64 copies of

the cross-coupled pairs. Bits are controlled by placing either a high or low voltage at the gate of M13: a high voltage at the "qbias" value pulls current through the cross-coupled FETs. A low voltage below threshold shuts off the current flow and doesn't allow the pair to Q-enhance. In addition to the binary-weighted banks, there is also one cell of analog tuning, comprised of two copies of the cross-coupled pair. The "qbias" pin of the analog cell is brought directly off-chip, allowing for analog control of the current and hence the gm value in the cross-coupled pairs.

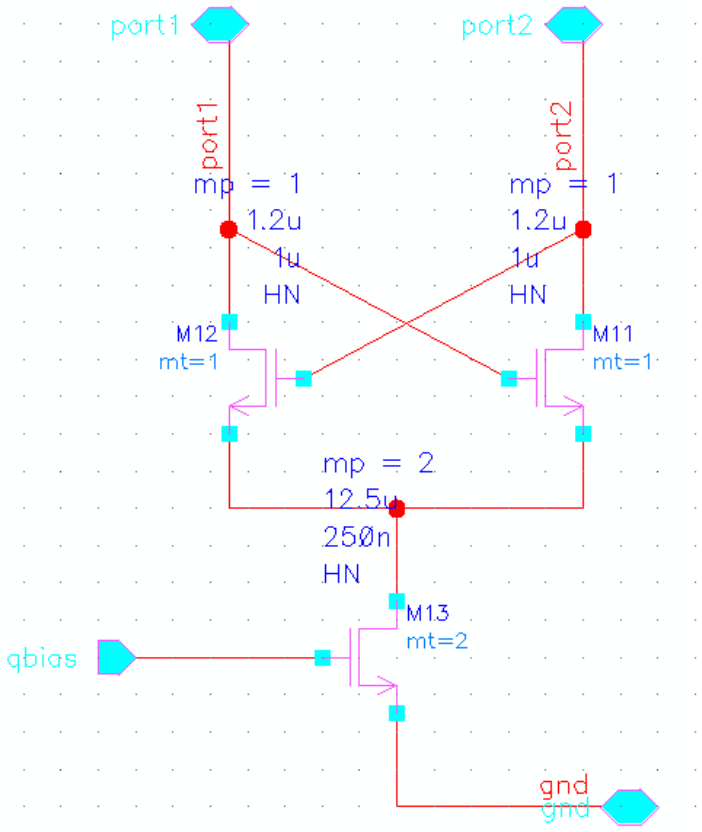

Figure 5-8: Cross-coupled pair for Q-Enhancement

The frequency tuning caps are designed to carry up to 10% of the total capacitance of the filter when at the center frequency, with the remaining 90% existing as an off-chip component. Banks of frequency tuning cells are set up in a manner nearly identical to that of the coupling caps discussed above in Figure 5-6. The sizes of the FETs are somewhat different to fulfill the capacitive needs of the frequency tuning, and each frequency tuning bank has 8 bits to support a broader range of values. Like the Q-enhancement banks, the frequency tuning also incorporates

analog tuning. One capacitive cell of twice the minimum size has its control pin brought off-chip for analog control.

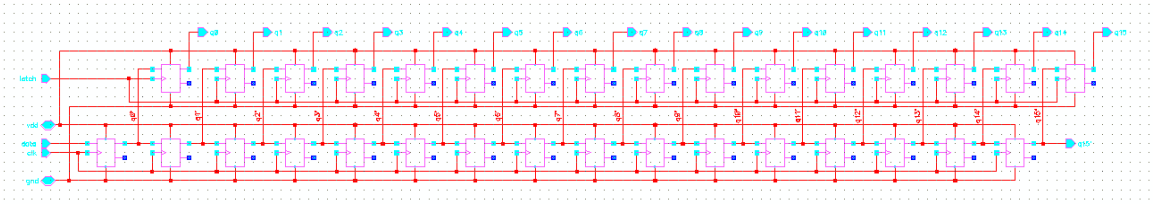

Figure 5-9: Serial-to-parallel shift register schematic

All capacitive coupling, frequency and Q-tuning digital controls are placed on a basic serial-to-parallel shift register with latch shown in Figure 5-9. Enable pins are also controlled via the shift register. The shift registers are designed for "words" of 16 bits. With 54 bits to control, four shift registers in series are used.

5.3.3 Amplitude/Bandwidth Detector

The amplitude detector used in this design is very similar to that used in the previous design (see section 3.2.3). The new design can be seen in Figure 5-10. Small adjustments were made to adapt the design to the new fabrication process. The only real change that was made was to the lowpass filter formed by R3 and C3, to adapt the circuit to read the beat frequency.

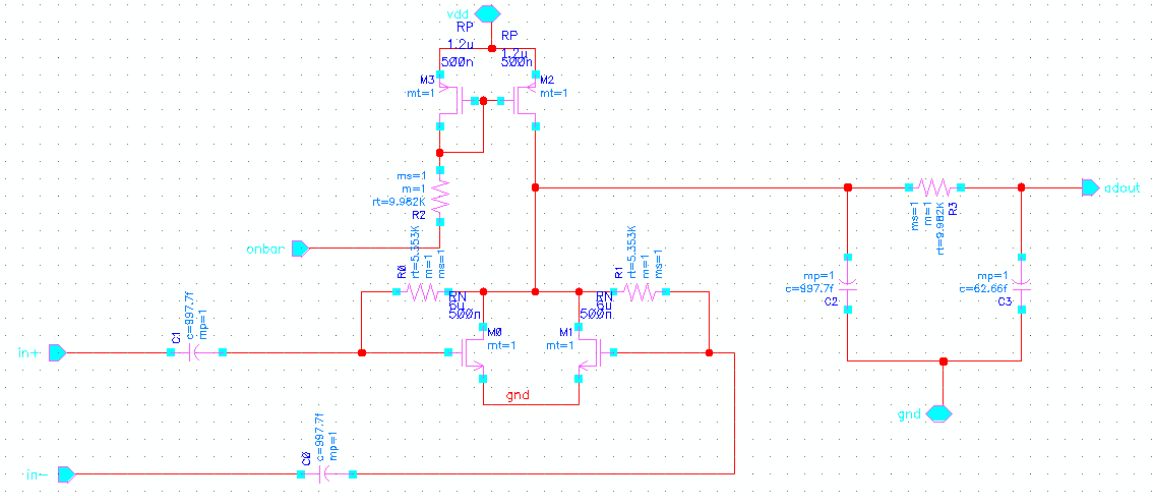

Figure 5-10: Amplitude detector schematic

For a relatively slow change in amplitude, such as when the oscillation saturates in Figure 5-11, the amplitude detector outputs a DC signal between approximately 700mV and 350mv. When used to determine the bandwidth of the filter, the amplitude detector is essentially used as an envelope detector. Capable of tracking the amplitude of the oscillating signal, the amplitude detector outputs a signal at the frequency of the beat as shown in figure 5-12.

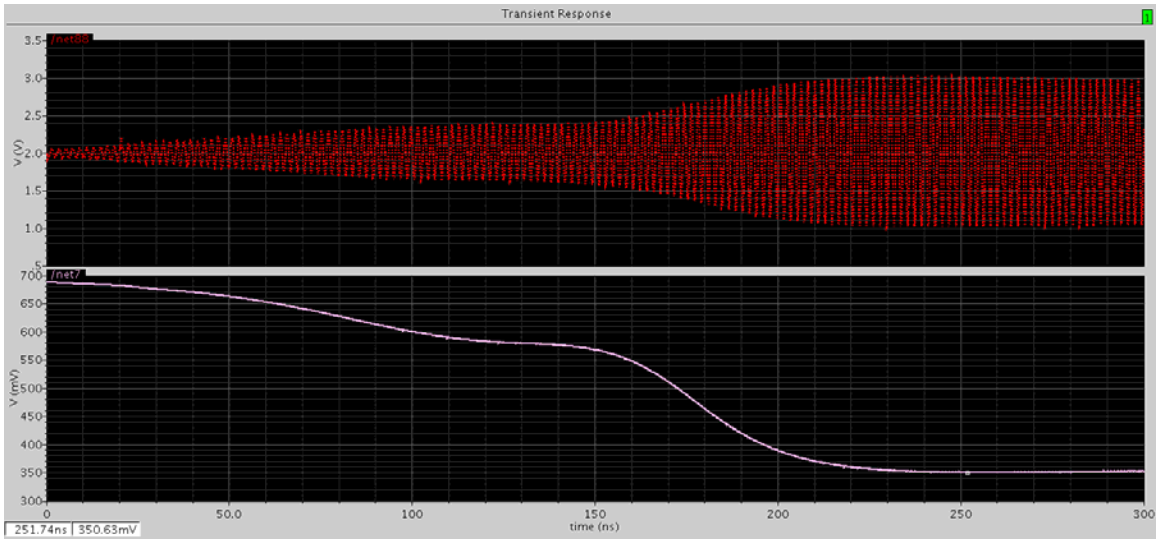

Figure 5-11: Amplitude detector tracking oscillation amplitude

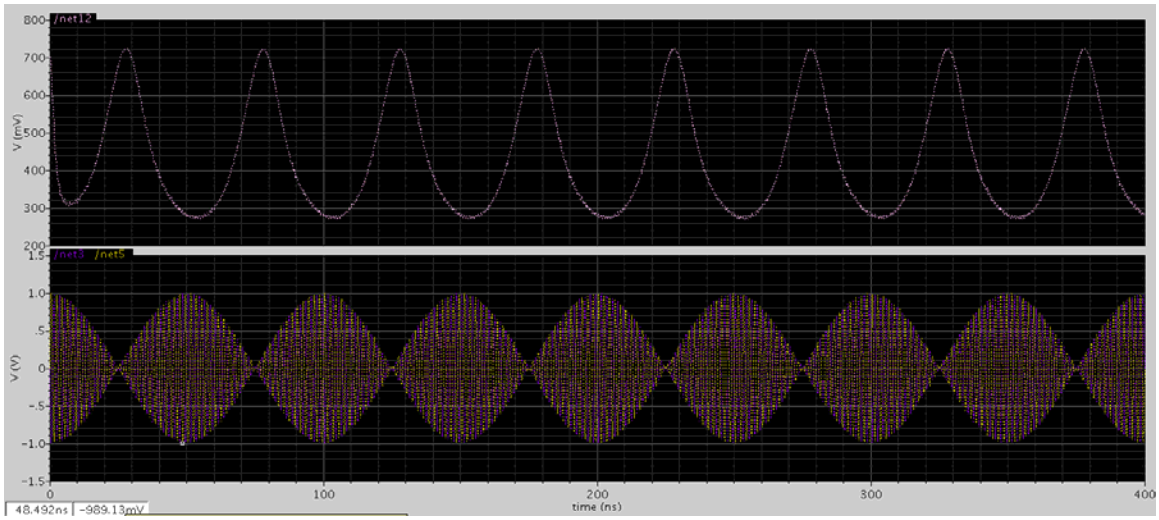

Figure 5-12: Amplitude detector tracking beat frequency

The lowpass RC filter formed by R3 and C3 at the output of the amplitude detector removes the 500MHz signal while letting the DC and low-frequency beat frequencies through. As the beat frequency is in the range of 1 – 20 MHz, a corner frequency of 250MHz was chosen for the lowpass filter.

5.3.4 Frequency Prescaler

The frequency prescaler used in this design is very similar to the prescaler used in the earlier design (see section 3.2.2).

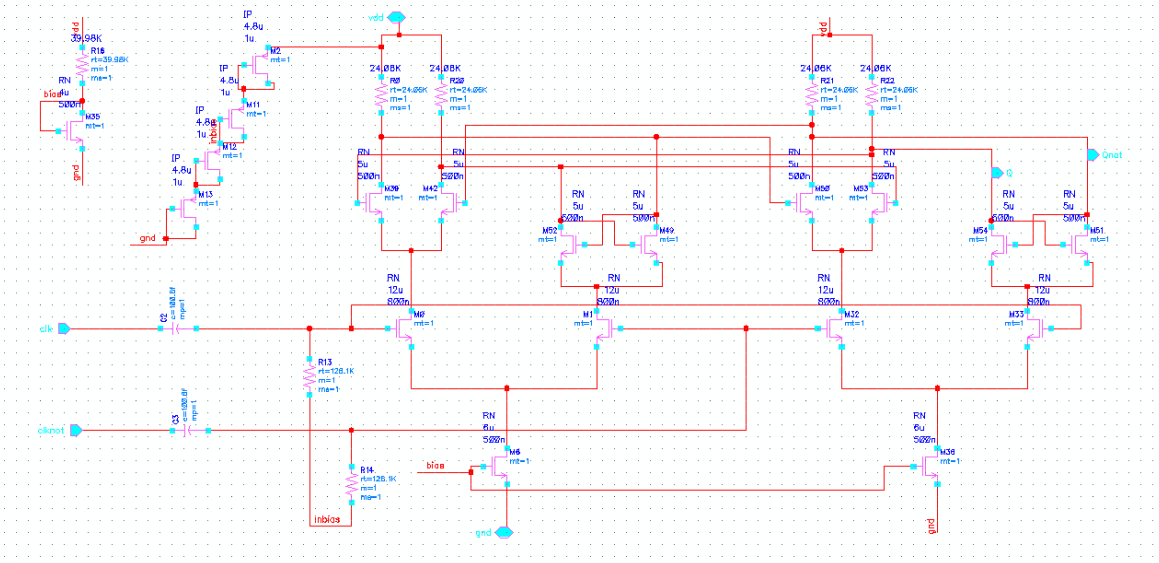

Figure 5-13: Frequency Prescaler schematic

Key design considerations for the frequency prescaler revolve around the gm for the cross-coupled pairs in the CML latches. In order to latch sufficiently quickly, the FETs must follow the equation

$$R_D \times gm \geq 2 \qquad (14)$$

Since problems occurred with the previous design where the frequency prescaler required a much higher input power than the amplitude detector to function, this design was adjusted to latch with much lower input amplitudes. As discussed in section 4.1, the earlier prescaler

displayed a self-oscillating problem that was hypothesized to be the fault of analog and digital circuitry being on the same power supplies. For this design, the analog circuitry shares a power supply with the main circuit, and only the digital circuitry is placed on its own power supply as shown in Figure 5-14 in an attempt to avoid this problem. PFET switches allow the divider to be disabled under software control to avoid crosstalk when in filtering mode.

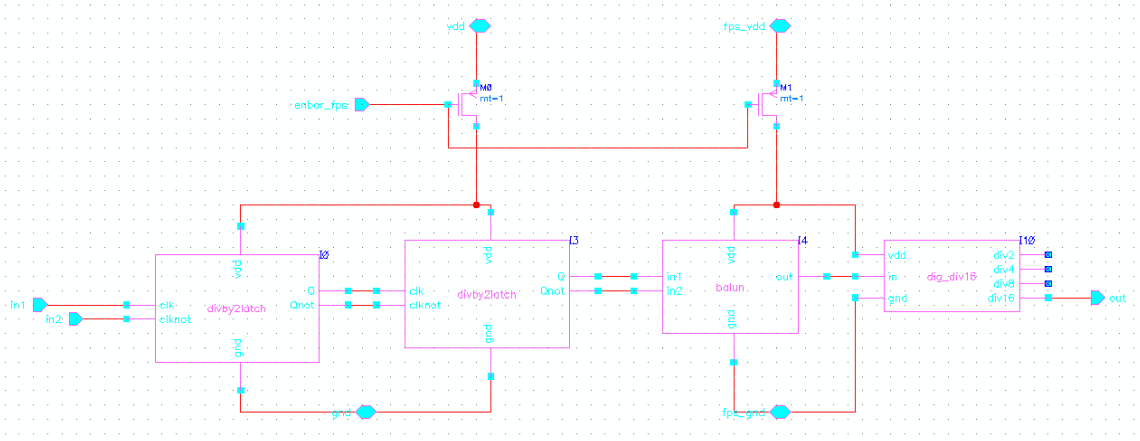

Figure 5-14: Frequency prescaler top-level

In simulations, the prescaler properly divides a sinusoidal signal with input amplitudes as low as 50mV pk-to-pk and up to frequencies of 1GHz.

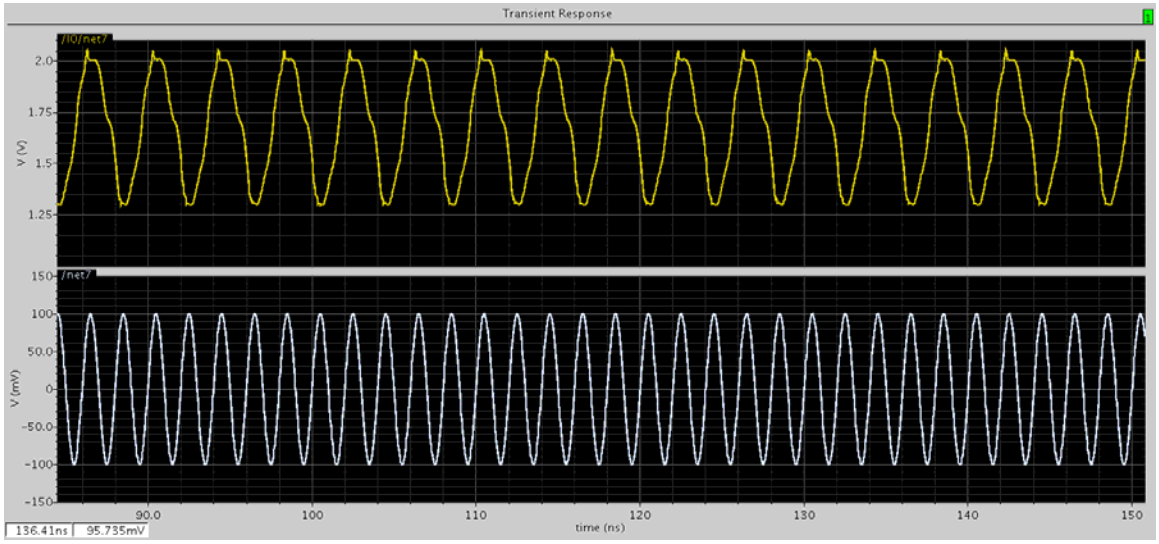

Figure 5-15: Frequency prescaler divide-by-2 operation

5.3.5 Output Buffers

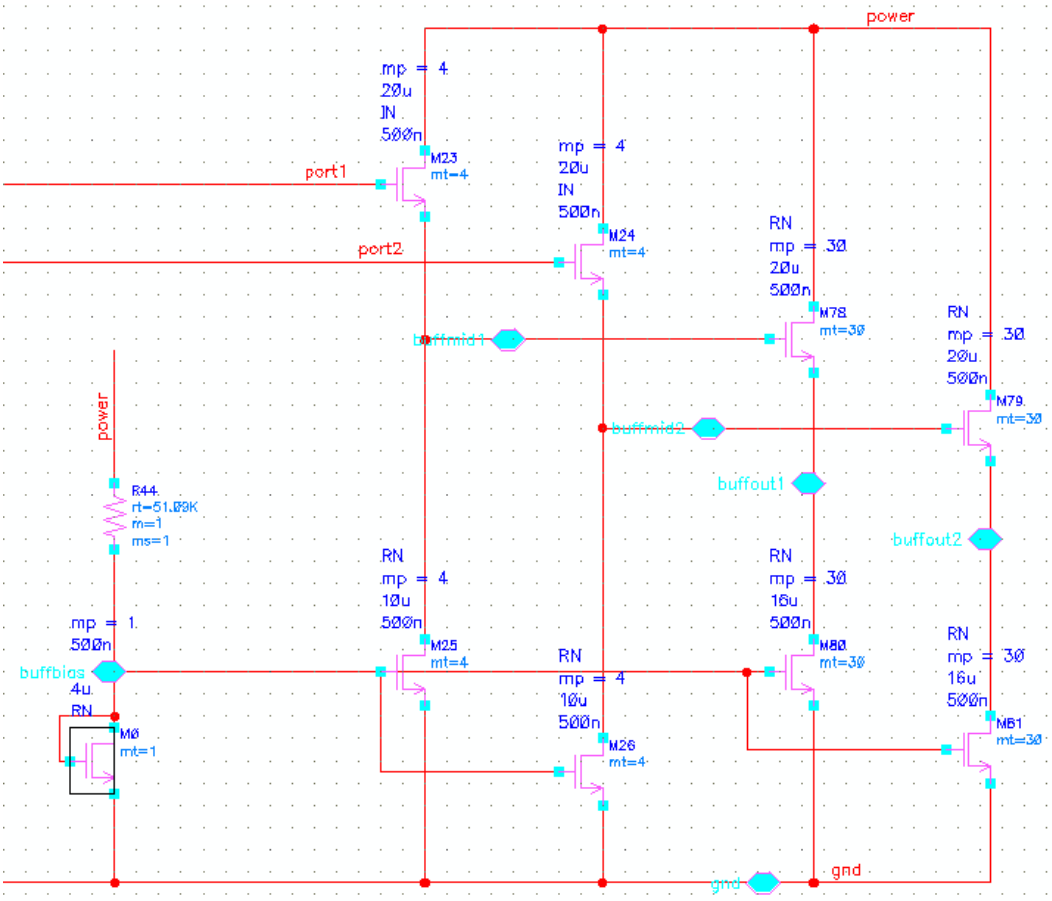

Figure 5-16: Output buffer schematic

One of the major failings of the earlier filter was due to improper design of the output buffers. The problems of low sourcing current and improper biasing have been fixed in this design.

Identical buffers are placed on both the front and back of the filters for balance. The frequency prescaler and amplitude detector inputs are taken from the last stage of the buffers.

Output buffers are constructed with simple source-follower topology. The first stage is designed with much smaller FETs to put low capacitive loading on the filter. The second stages of the output buffers were designed to be able to drive into 50Ω off-chip. To this end, each leg of the buffer draws 4.6mA. The output resistance of each leg is approximately 18 Ω. A bondable pin was placed on the gate of the current mirror FETs of the buffers. In the event that

the buffers need to be adjusted, an external DC voltage can be placed on this pin to override the original bias voltage and change the gain of the buffers.

5.4 Considerations of Bondwire Parasitics

One possible problem that arises when dealing with an off-chip resonator is from the impedances incurred in the bondwire and bondpad parasitics. At 500MHz, the frequency of interest, the bondwire/ bondpad system for the selected process presents as a 5.9nH series inductor and 590fF capacitor to ground, as shown in figure 5-17.

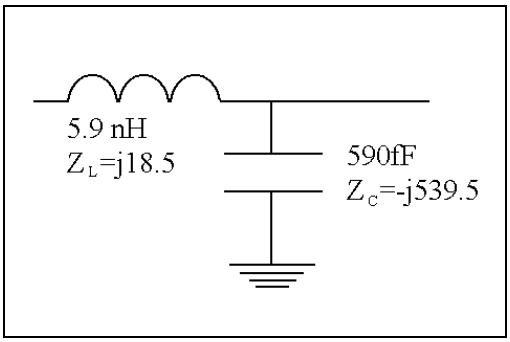

Figure 5-17: Model of bondwire parasitics at 500MHz

The j18.5 from the inductors is negligible in this case. However, the –j539.5 from the capacitors appears to be a problem until the AC circuit is examined, as shown in Figure 5-18. Here the parasitic capacitance is in parallel with the differential resonator capacitances, and can be absorbed into them during tuning.

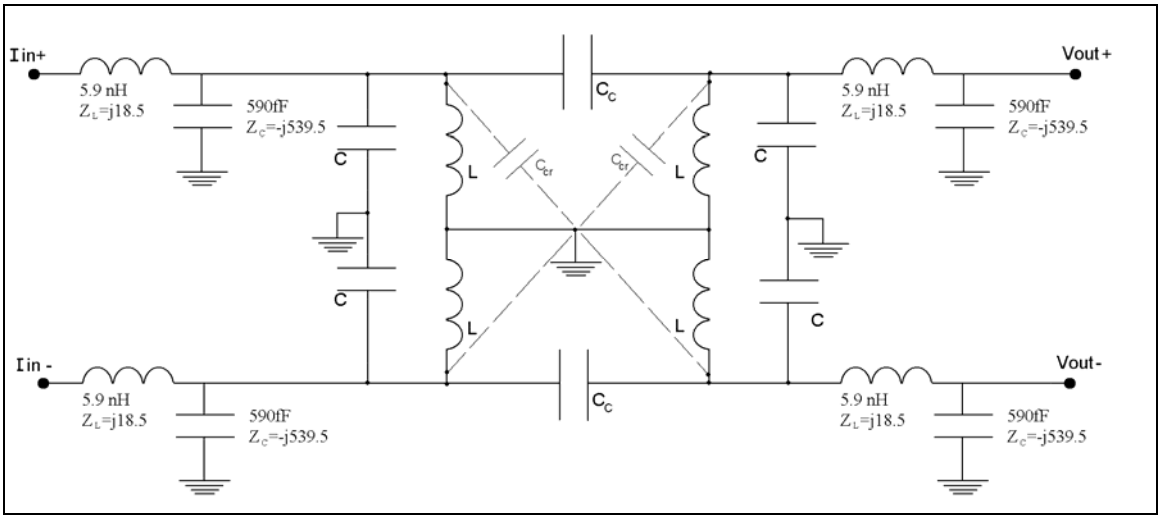

Figure 5-18: Off-chip resonator with bondwire parasitics

5.5 Layout

The finished layout occupies a space of approximately 3mm x 1.45mm for a total area of 4.2mm^2. A total of 29 bondable pins were used, with two additional test points for probing.

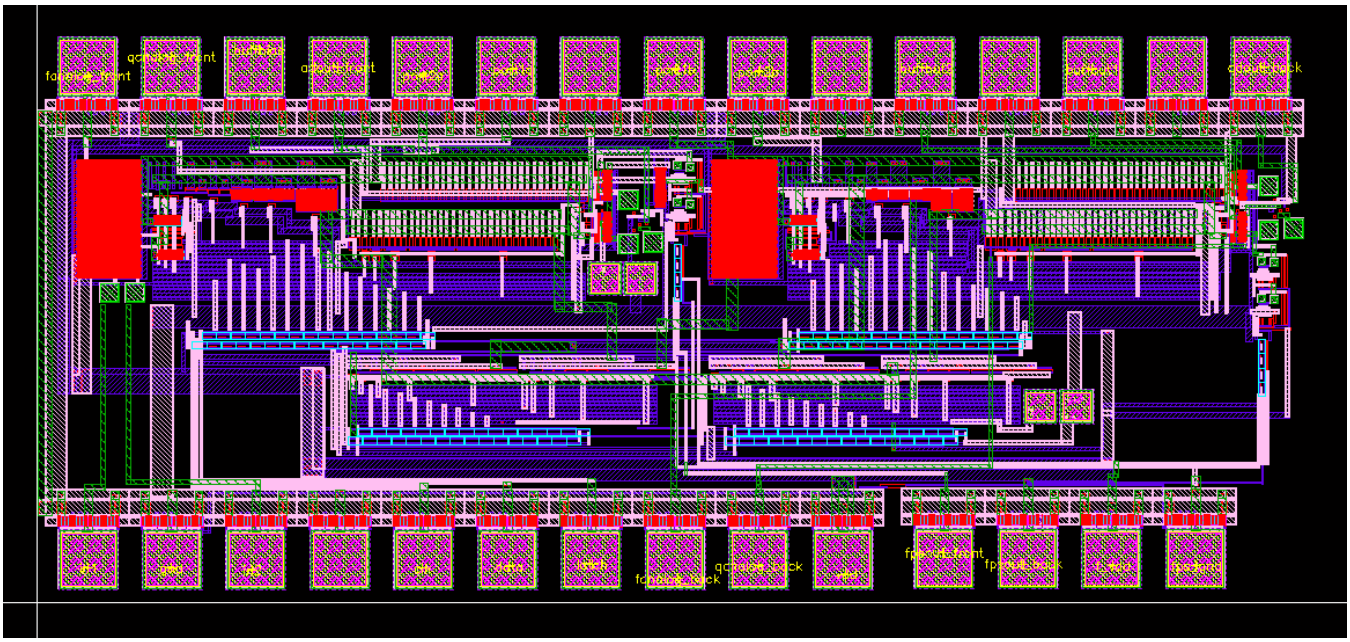

Figure 5-19: Full circuit layout

CHAPTER 6 - Conclusions

In the course of this work, an automatically-tuned single-pole Q-enhanced filter was designed, fabricated and tested. It was demonstrated here that the filter was able to tune itself to a desired frequency without the aid of any external signals or manual adjustment.

A novel two-pole q-enhanced filter design was also explored, and an expanded tuning algorithm was presented. This two-pole design allows for automatic self-tuning of the filter to a designated bandwidth, functionality not available in earlier versions of q-enhanced filters. To our knowledge, this is the first multi-pole q-enhanced filter design which allows for automatic tuning of specified bandwidth.

6.1 Future Work

Several of the ideas presented in this work will need to be expanded upon before the filters presented here are ready for use in industry.

Most obviously, the two-pole q-enhanced filter will need to be fabricated and tested. As of this writing, the design has been sent for fabrication, and will return for the next researcher to test. A fully fleshed-out version of the algorithm will need to written, programmed and run.

The algorithm itself is simple enough that it does not require the full processing power of a computer or microprocessor. It would be possible in future work to design the specific digital circuitry necessary to run the algorithm and to place that circuitry directly on the 3mm x 3mm die with the filter. This would eliminate the need for an external controller and would integrate the whole system more fully.

Currently, the system is intended to automatically re-tune itself at regular intervals. If a temperature sensor were added to the system, the filter might only need to be re-tuned when the temperature fluctuates by a certain amount. This is an idea worth exploring, although temperature differences in on-chip and off-chip components may be an issue.

6.1.1 Proposed Tuning Algorithm

A number of issues must be addressed when attempting to adapt the algorithm used earlier in this work for use with the more complex two-pole coupled filter.

First, there is the obvious issue that the new filter possesses two distinct "sides" to the filter. Each of these sides must be tuned to the same frequency in order to produce the desired shape of the filter. The design allows for this to be accomplished in more than one possible way. First, each side of the filter incorporates its own enable/disable pin, shutting off the current through that side, killing the gain and preventing that side of the filter from oscillating. To prevent any signal from feeding back through to the other side of the filter, the total magnetic and capacitive coupling between the sides must be minimized. If the external components are sufficiently far apart to render the magnetic coupling negligible, then the capacitive coupling can simply be set to zero. Each side of the filter is equipped with its own amplitude detector, frequency prescaler, q-enhancement and frequency tuning cells. One the two sides are isolated from each other, they can essentially each be separately tuned in frequency according to the algorithm described in section 3.5.

Since this new design incorporates some analog fine-tuning elements where the previous design does not, an additional analog-tuning loop will need to be added to the algorithm.

Finally, since the two-pole filter incorporates the ability to tune the bandwidth via controlling the coupling capacitance, the algorithm must be expanded to include this entirely new facet. This will likely be the most difficult part of the algorithm. First, the two poles of the filter must be Q-enhanced in tandem to a point of "critical oscillation": where the filter oscillates at two frequencies, but is neither dampened so that it dies down nor saturates so that the beat frequency is lost. The analog Q-tuning will be very useful for finding this point, particularly at the narrower bandwidths. Once this point is found and the beat frequency is established, the amplitude detector at the output of the filter can be used to read the frequency of the beat. The coupling between sides can then be adjusted until the bandwidth is reached. Finally, the "Q-backoff" from the critical oscillation point must be done, to achieve a proper passband shape. With the ability to oscillate one side only, it is believed that this can be achieved.

The algorithm should flow approximately as follows:

1. Disconnect inputs
2. find minimum coupling/ disable back side
3. oscillate front side
4. tune front side to desired frequency

5. de-oscillate front / disable side
6. oscillate back side
7. tune back side to desired frequency
8. oscillate front side too
9. find critical oscillation
10. increase coupling until desired BW
11. de-oscillate both sides by the necessary amount to achieve a flat passband
12. reconnect inputs

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