STUDY OF HIGH DIELECTRIC CONSTANT OXIDES ON GAN FOR METAL OXIDE SEMICONDUCTOR DEVICES

by

DAMING WEI

B.S., Dalian University of Technology, 2009

AN ABSTRACT OF A DISSERTATION

submitted in partial fulfillment of the requirements for the degree

DOCTOR OF PHILOSOPHY

Department of Chemical Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2014

Abstract

Gallium nitride is a promising semiconductor for fabricating field effect transistors for power electronics because of its unique physical properties of wide energy band gap, high electron saturation velocity, high breakdown field and high thermal conductivity. However, these devices are extremely sensitive to the gate leakage current which reduces the breakdown voltage and the power-added efficiency and increases the noise figures. To solve this problem, employing a gate dielectric is crucial to the fabrication of metal insulator semiconductor high electron mobility transistors (MISHEMTs), to reduce the leakage current and increase the magnitude of voltage swings possible. For this device to be successful, imperfections at the oxide-semiconductor interface must be suppressed to maintain the high electron mobility of the device.

This research explored multiple high dielectric constant gate oxides (Al_2O_3, TiO_2, and Ga_2O_3), deposited on different crystalline orientations and polarities of GaN by atomic layer deposition (ALD) to form metal oxide semiconductor capacitors, including effects of pretreatment on N-polar GaN, ALD TiO_2/Al_2O_3 nano-laminate on thermal oxidized Ga-polar GaN and ALD Al_2O_3 on *c*- and *m*-plane GaN Surface pretreatments were shown to greatly alter the morphology of reactive N-polar GaN which is detrimental to the electrical properties. 14 nm thick ALD Al_2O_3 films were directly deposited on N-polar GaN without thermal or chemical pretreatments which yield a smooth surface (RMS=0.23 nm), low leakage current (2.09×10^{-8} A/cm^2) and good Al_2O_3/GaN interface quality, as indicated by the low electron trap density (2.47×10^{10} cm^{-2}eV^{-1}). In the nano-laminate study, a high dielectric constant of 12.5 was achieved by integrating a TiO_2/Al_2O_3/Ga_2O_3 oxide stack layer, while maintaining a low interface trap density and low leakage current. There was a strong correlation between the surface morphology and electrical properties of the device discovered from comparing the ALD Al_2O_3 on *c*- and *m*-plane GaN, namely smooth surface lead to small hysteresis. These results indicate the promising potential of incorporation gate dielectric for future GaN devices.

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Major Professor
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Acknowledgements

I would like to thank my committee members who spent their precious time to train me on equipment and teach me knowledge during my doctoral research. Special thanks to Professor James Edgar, my major advisor and my role model for continuous supporting and inspiring me throughout the entire process. He also encourages me to continually explore the unknown and provide me valuable opportunities to lean in national laboratories. I feel very fortunate to work under his supervision. I also want to thank Professor Andrew Rys for guiding me into the electrical characterization of semiconductors and letting me use the oxidation furnace; Thank you Professor Vikas Berry for teaching me AFM and thank you Professor Keith Hohn for teaching me XPS.

I am grateful for numerous CV and IV measurements done by my co-worker and my friend Dr. Tashfin Hossain which is very important to this research. I also want to acknowledge Professor Daniel Higgins, Professor Takashi Ito for training me on the AFM, Dr. William Kuhn for trouble shooting electrical problems and Dr. Dan Boyle for teaching me SEM. I also want to thank all the professors, staffs and graduate students in chemical engineering who are always willing to help me out whenever I need them.

I would like to acknowledge Naval Research Laboratory for the collaborated work in this dissertation and Oak Ridge National Laboratory for providing user facilities to make partial of the device fabrication and characterization possible. Special thanks to Dr. Harry Meyer for training me operating the state-of-the-art XPS and Dr. Andrew Payzant, Dr. Melanie Kirkham for training me on XRD. I am also grateful for Dayrl Briggs who spends countless time writing recipes for processing my samples and training me on several semiconductor fabrication tools.

Dedication

This dissertation is dedicated to my family and friends. Especially to my parents Bai Wei and Hongna Shen and grandparent Guichun Zhou.

Chapter 1 - Introduction

Prologue to the thesis

GaN based devices have successfully demonstrates its superior performance of high frequency, high power handling capability and high device efficiency in power electronic applications such as hybrid electric vehicles, controllers for electric grids, wireless networks and compact radars. This is owing to the unique physical properties of GaN for a wide band gap energy and high saturation electron mobility. In the past decade, the dimension of GaN based devices have been scaled down to achieve higher frequency performance which bring some drawbacks such as the increasing gate leakage current.

In this dissertation work, multiple high dielectric constant oxides has been deposited on GaN substrates forming metal oxide semiconductor capacitors to reduce the leakage current and increase the magnitude of voltage swing possible. These devices were tested by correlating the composition, chemical bonding states, impurity concentrations, structure and morphology of gate oxides, to the electrical properties of the device such as leakage current density, interface states and breakdown strength. These were also related to the process conditions under which the oxide was prepared to better control the performance of the device

Introduction of power electronics:

To manipulate electrical energy itself, power electronics are the vital components to convert and control the flow of electrical energy.[1] A more complete illustration of power electronic system includes an energy source, an electrical load, and a power converter.[2] A power converter consists switches, energy storage elements and transformers, which is used to change the characteristics including current, voltage and/or frequency of electrical power to serve certain application (electrical load).[3]

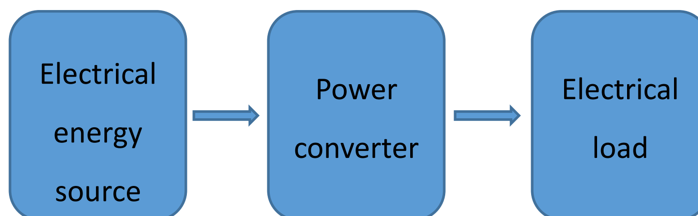

Figure 1.1 Schematic picture of power electronic system[2]. The source energy is converted to serve an electrical load.

Ever since the invention of the transistor at Bell Laboratory in 1947,[4] this invention can be found in most modern electronic technologies as well as the power electronic circuit. The development of a commercial thyristor by General Electric Company in 1958 opened a new era of power electronics. Since then, many different types of power semiconductor devices have been developed such as power metal oxide semiconductor field effect transistor (IR 400V 25A) and insulated gate bipolar transistor (IGBT).

The unique property of semiconductors is that its electrical conductivity can be controlled over a wide range by introducing impurities which are atoms contain either one more (electrons) or one fewer (holes) electrons in their outermost shell than the host semiconductor atoms.[5] This process is called doping by which different regions of the semiconductor with excessive electrons or holes could be formed, subsequently, those regions can be either positive (*p*-type) or negative (*n*-type). Solid state devices such as transistors are fabricated by forming junctions of these regions.

The function of a transistor is to control a large output with a small input. Based on how the electron flow is controlled when a bias voltage is applied between the terminals, transistors can be divided into two groups: bipolar (junction) transistors (BJT) and field effect transistors (FET). In a BJT, a potential profile controls the electron flow, while in a FET gate bias is used to control the flow.[6] There are many kinds of FETs such as Metal Semiconductor Field effect transistor (MESFET), Heterojunction Field Effect Transistor (HFET), and Metal Oxide Semiconductor Field effect transistor (MOSFET) or Metal Insulator Semiconductor Field effect transistor (MISFET). Since the first introduction of commercial MOSFETs, they have replaced BJTs and became the most extensively used solid-state device,[7] due to its simple fabrication technologies, excellent thermal stability and no secondary breakdown. These properties are favorable in high power applications.[8]

The MOSFET is a three terminal device with a source as an input, the drain as an output and the gate as a control terminal.[5] A MOSFET has a conducting semiconductor channel with two ohmic contacts (the source and the drain) on the end of each side of the channel as illustrates in Fig. 1.2. The number of charge carriers in the channel is controlled by the gate terminal through capacitive coupling (field effect),[9] and the insulator under the gate plays an important role of electrically separating the gate to the channel in order to minimize leakage current.

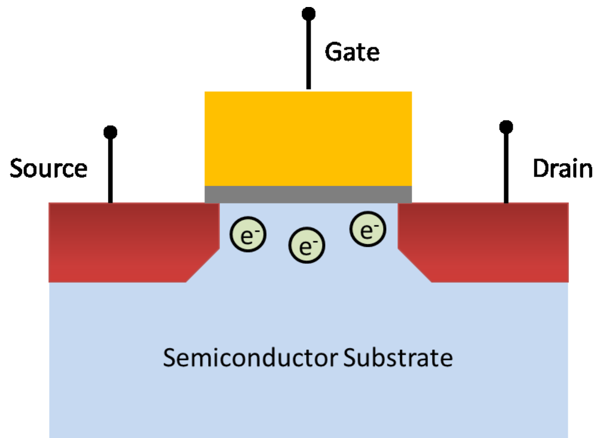

Figure 1.2 Schematic picture of a generic MOSFET

MOSFETs can be made from a wide variety of semiconductors including Si, GaAs, InP, InGaAs, GaN, SiC, etc.,[10–15] among which GaN are prevalent for power electronic devices for high frequency, high temperature and high power applications[16,17] due to its advantageous physical properties shown in table 1.1.

Table 1.1 Physical properties of common semiconductor materials. GaN has superior saturated electron velocity and breakdown field comparing to other semiconductors.[18]

Semiconductor		silicon	Gallium arsenide	Indium phosphide	Silicon carbide	Gallium nitride
Characteristic	Unit					
Bandgap	eV	1.1	1.42	1.35	3.26	3.49
Electron mobility at 300 K	cm^2/Vs	1500	8500	5400	700	1000-2000
Saturated (peak) electron velocity	$\times 10^7$ cm/s	1.0	2.1	2.3	2.0	2.5
Critical breakdown field	MW/cm	0.3	0.4	0.5	3.0	3.0
Thermal conductivity	W/cm·K	1.5	0.5	0.7	4.5	> 1.5

Although silicon has dominated electronic device since the 1950s because of its purity and the superior interface quality of Si/SiO_2,[19] the increasing need of higher frequency and lower cost per device has pushed silicon to its limits. Also, the dimensions of the transistor has been dramatically reduced. Imagine the size of a 1960s transistor was as big as a three-bedroom house, and it shrank by the same factor that the transistor has over 50 years. Today, the house could be held on people's hand.[20] With the reduction in device size, there are several problems that need to be addressed including larger power density per chip, increasing heat dissipation, and shrinking thickness of gate oxide.[21] All these factors make GaN an important alternative to high speed Si electronics.

At high temperature, Si devices stop working at about 140°C due to its small bandgap (1.1 eV), which nullifies the effect of external dopant.[22] In contrast, with a larger bandgap of 3.4 eV GaN devices have been tested up to 300°C and worked very well.[18] In addition to bandgap, another crucial properties affecting the performance of the device is the carrier drift velocity which determines how fast a transistor can switch.[23] The maximum drift velocity of an electron in a semiconductor when an electrical field is applied is the saturation drift velocity.[22] GaN can achieve a very high saturation velocity due to the polarization generated from its unique crystalline structure.

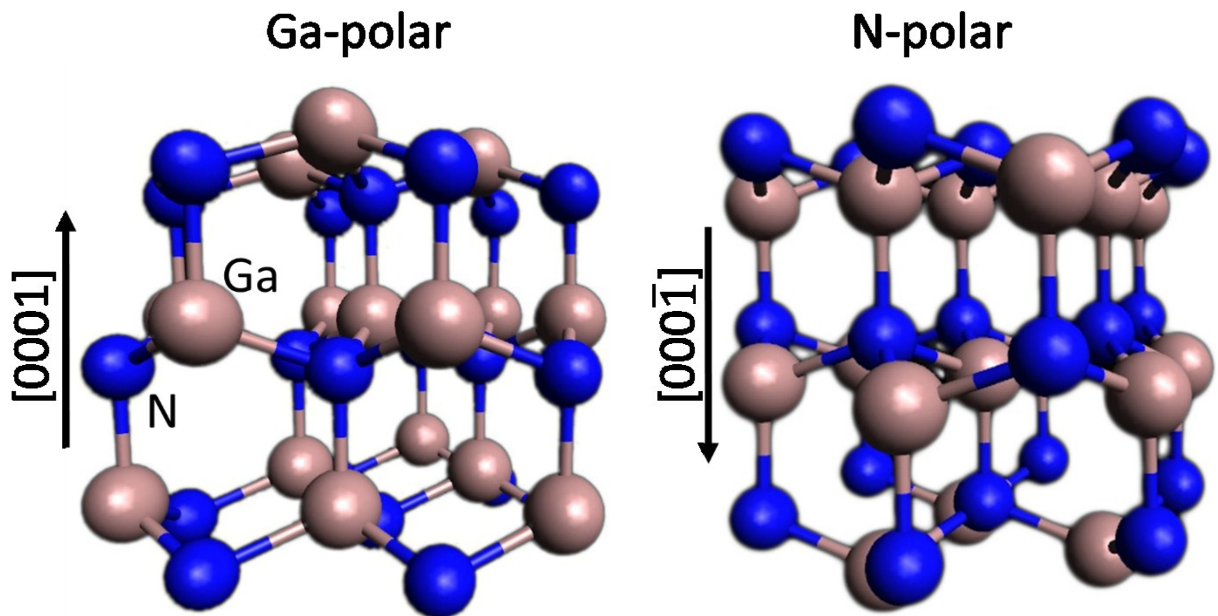

Figure 1.3 Crystal structure of wurtzite GaN.[24]

GaN exists in two crystal structures: wurtzite and zinc-blende. The most stable and commonly used phase is wurtzite. Due to the inversion asymmetry along the *c*-axis in the wurtzite phase, its structures along the (0001) [Ga-polar] and $(000\overline{1})$ [N-polar] have distinctive properties (Fig 1.3).[25] This makes possible the fabrication of the GaN-based High electron mobility transistors (HEMTs) which are a derivation of a FET. Take the AlGaN on Ga-polar GaN HEMT as an example (Fig 1.4). In GaN crystal, the ionized gallium and nitrogen atoms greatly differ in size and settled irregularly with respect to each other, which naturally generates electrical polarization within the crystal. Due to the neutralization of opposite charged regions, this polarization does not accumulate until it reaches the boundary with another crystal (AlGaN). Furthermore, the lattices mismatch of the two crystals at this AlGaN/GaN heterojunction can generate piezoelectric polarization.[26] This combination of two polarizations produces a high concentration of free charge carriers in a narrow region parallel to the interface in GaN, commonly known as two dimensional electron gas (2DEG), which is the critical part of HEMTs. Unlike most other semiconductors, the GaN HEMTs can form the mobile electron gases without doping with impurities.[18] This is advantageous because the electron mobility is reduced as the impurity concentration increases due to scattering. Until recently, all AlGaN-GaN HEMTs were made on Ga-polar GaN rather than N-polar semiconductors.[27–29]

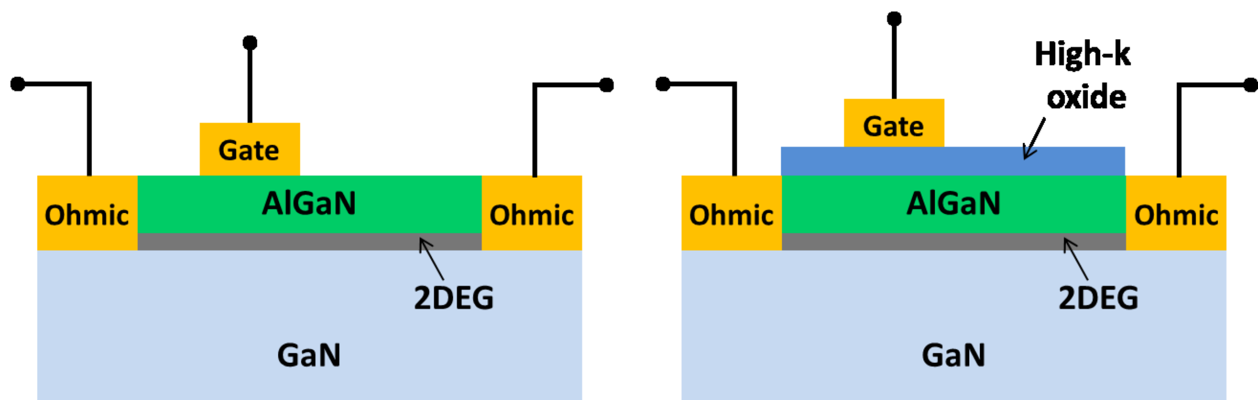

Figure 1.4 Structure of AlGaN/GaN HEMT (left) and MOSHEMT (right)

In contrast to an ordinary silicon based FET, which requires a gate bias to turn on the transistor (enhancement-mode operation), the source and drain of a GaN HEMT is always connected by the 2DEG. This is specifically true for a Ga-polar GaN-based HEMT. So when a voltage is applied to the drain, it can instantly draw electrons from the source. A negative gate voltage is required to adjust the amplitude of the current and even cut it off. This type of device is called normally-on transistor or depletion-mode transistor.[30] However, in the field of power

electronic applications, a normally-off type transistor is preferred for fail-safe operation and to minimize energy consumption.[31] For the normally-off transistor, a positive gate voltage is necessary to create a region of mobile electrons which connects the source and drain, and when the voltage is retrieved, the transistor is open (off). This is also called enhancement mode transistor.[30]

There are several ways of making a GaN enhancement transistor. First of all, is to use N-polar GaN as the substrate.[29] The switch of polarity of GaN crystal could adjust the amount of electrons in the 2DEG, and complete depletion of the electron turns it into an enhancement transistor. Secondly, 2DEG could also be controlled by fluoride-based plasma treatment,[32] in which fluorine ions act as immobile negative charges that deplete the 2DEG.[33] But implantation of the highly energetic fluorine ions leads to a defect formation in the 2DEG region, and consequently scarifies the electron velocity. An alternative structure to achieve the normally-off condition is to employ a GaN MOSFETs, but this structure also compromise the enhanced electron mobility.[34]

Another important factor in GaN transistor is a good insulation between the gate and channel, because the maximum forward voltage that can be applied to the gate is restricted by the Schottky barrier height. This would be the bottleneck if high positive gate voltage is required to generate significant drain current flow for the enhancement mode transistor. Adding a high dielectric constant [high-k] oxide ($k > 3.9$)insulator between the transistor gate and substrate helps to address the problems. It can significantly lower the leakage currents through the gate and increase the magnitude of voltage swings possible, thereby greatly increasing the device efficiency.[35,36]

Reference

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Chapter 2 - Review of High-k Dielectrics on GaN

Introduction of high-k oxides

Using high-k materials as the gate stack traces back to the fabrication of integrated circuit (IC) using silicon based MOSFETs where the SiO_2/Si was the most common insulator/semiconductor system until 21st century since the development of the first MOSFET.[1] To keep up with Moore's Law, the physical size of the transistor needs to be reduced by half every two years.[2] This leads to the shrinking of the gate dielectric thickness; the SiO_2 decreased from a few hundred nanometers to a few atomic layers (~1-2nm).[3] As the thickness approaching 1 nm, SiO_2 loses its insulating properties, as significant numbers of electrons tunnel through the energy barrier,[4] turning into unwanted heat and draining out of battery quickly.

To solve this problem, new materials are required to replace SiO_2. They should be able to form an insulating film that is thick enough to prevent electrons tunneling while at the same time being permeable enough to allow the gate electric field into the channel to accumulate enough electrons so that the transistor could be turned on.[1] The technical name for this material is high-k dielectric, which refers the dielectric constant of the material should be larger than that of SiO_2 (3.9).

Similar concepts are also applied to GaN-based transistors. A good compatible dielectric to GaN semiconductor requires a high dielectric constant, large conduction band offset, thermodynamic stable, low oxygen diffusivity, low leakage current and high interface quality with low interface state density.[5–8] However, the much inferior structural quality of the GaN/oxide interfaces in comparison to the Si/SiO_2 interface of Si-based MOS devices has remained a major obstacle [9]. In this chapter, previous studies of high-k dielectrics on GaN are reviewed, among which more attention was cast on Al_2O_3, HfO_2 and Ga_2O_3 due to their outstanding properties. Other oxides are also briefly reviewed and compared. A summary of the best candidate high dielectric for GaN is made.

Al_2O_3 as gate dielectric on GaN based transistor

Al_2O_3 has been widely studied as a gate oxide due to its suitable physical properties and many methods by which its thin layers can be deposited. The dielectric constant of Al_2O_3 ranges from 8 to 10,[10,11] which yields an effective oxide thickness ~0.4 times of the SiO_2 thickness. The

band gap of Al_2O_3 ranges from 6.8 to 9.4 eV.[11–14] This gives a high conduction band offset with GaN of ΔE_c=2.1 eV.[15,16] A large breakdown field of Al_2O_3 of 10MV/cm,[13] and good thermal stability (amorphous up to at least 1000°C) make it suitable for scaling devices and in high power applications. Many methods have been reported for depositing Al_2O_3 including sputtering,[10] metal-organic chemical vapor deposition (MOCVD),[17,18] oxidation of molecular beam epitaxial (MBE) of aluminum layer,[16] and atomic layer deposition (ALD).[19–22]

In all cases, adding an Al_2O_3 insulator improved the transistor performance, enabling a great increase in the drain current density and a two to three orders of magnitude of lower leakage current compared to the GaN HFET counterpart. However, the interface quality was not reported by MBE method,[16] and an additional Si_3N_4 layer was required before sputtering Al_2O_3 on GaN based transistor to achieve a good quality interface.[10] MOCVD reduces the current collapse by decreasing the interface trap density, and has the advantage of forming crystalline and amorphous Al_2O_3 by adjusting the reaction temperature,[17] but hysteresis on the capacitance-voltage measurement were not resolved, and quantitative studies of Al_2O_3 /GaN interface state were not presented. ALD of Al_2O_3 films were the most studied and offer better control over the oxide thickness. For Al2O3 deposited by ALD on GaN, the as-deposited interface trap density was between 10^{12} and 10^{13} cm^{-2}. This could be reduced by an order of magnitude by post-metallization annealing (PMA) in forming gas (5% H_2, 95% N_2) for 5 min at 500°C.[20] Consequently, ALD has become the most widely accepted Al_2O_3 deposition method.

HfO_2 as gate dielectric on GaN transistor

HfO_2 has also been widely used in GaN based transistors due to its large dielectric constant (ε=25),[13] large band gap (5.6~5.8 eV)[3] and low state density at the oxide semiconductor interface. Most studies of HfO_2/AlGaN/GaN focus on the device performance rather than the physical and electrical properties of the oxide-nitride interface.[23–29] The main finding from HfO_2 studies is that the density of surface states could be passivated by all the following reviewed deposition methods which relief the depletion in the 2DEG channel leading to an increasing of sheet carrier density (n_s).[30,31] Consequently, the drain current was increased and current collapse was reduced.

Deposition studies of HfO_2 for gate dielectrics includes ALD, reactive sputtering and pulsed laser deposition (PLD), among which ALD has better uniformity, better nano-scale

thickness control and low defect densities.[24,25] Shi *et al.* [25] grew a 15 nm HfO_2 film on AlGaN/GaN HEMT by ALD. The device demonstrated an off-state breakdown voltage V_{DS} of 1035 V with on resistance of 0.9mΩ cm^2, a maximum drain current ($J_{DS,\ max}$) of 575 mA/mm at the gate voltage of +1 V and a peak transconductance ($g_{m,max}$) of 160mS/mm, which has the best performance of HfO_2/AlGaN/GaN HEMT ever reported. A 20 nm HfO_2 reported by Liu *et al.* [24] showed an increase of the sheet carrier density from $8.53x10^{12}$ cm^{-2} to $1.12x10^{13}$ cm^{-2} as expected, but the mobility (μ_n) was decreased from 1140 cm^2(Vs)$^{-1}$ to 1015 cm^2(Vs)$^{-1}$. This reduced Hall mobility associated with the increased carrier concentration was proposed to be caused by an increased interface-roughness scattering as a result of 2DEG shifting towards the AlGaN/GaN interface at higher carrier concentration.[32] This is not observed with HfO_2 on GaN deposited by the ALD method. Thicker HfO_2 of 100 nm could be grown by pulsed laser deposition on a normally off device [29] with a $I_{DS,max}$ of 730 mA/mm at V_G of +10 V and gm max of 185 mS/mm which is very promising for simplicity of circuit design and fail safe power switching system.

Compared to Al_2O_3, HfO_2 has a larger dielectric constant, which helps further scaling of the EOT. But Al_2O_3 has a larger band gap than HfO_2, and its conduction band offset with GaN was 1 eV higher than that of HfO_2,[33] which provides a sufficient barrier for carriers in the GaN. Furthermore, Al_2O_3 has stronger adhesion to many surface and better chemical and thermal stabilities than HfO_2.[34,35] So a gate stack of HfO_2 on a Al_2O_3 passivation layer would be beneficial.

More thorough studies of the device physics are still needed. As shown in the papers summarized above, the dielectric constant of HfO_2 varies from 16.5 to 24,[24,28,36] and no explanation was provided for the change. Quantitative D_{it} analysis is also needed to correlate the deposition condition to better control the performance of the device.

Ga_2O_3 as gate dielectric on GaN transistor

Ga_2O_3 is a native oxide of GaN with the dielectric constant of 10.2-14.2 and band gap of 4.8eV.[37] Although the conduction band offset with GaN is 0.46 eV which is smaller than most of the other high k oxides,[15] Ga_2O_3 can be formed thermally and it is a chemically stable oxide on GaN. It also prevents the introduction of contamination from foreign oxide deposition and is expected to form high quality interface with GaN.[38–41]

The commonly used methods to grow Ga_2O_3 are photoelectrochemical oxidation,[40,41] pulsed laser deposition,[39] oxygen plasma oxidation,[42] saturated water vapor oxidation[43] and thermal oxidation.[44–47] Among all the above techniques, the lowest interface trap density of 10^{10} cm^{-2} eV^{-1} was achieved by dry thermal oxidation.[44,45] This is also one order of magnitude lower than the lowest achieved D_{it} with deposited insulator/GaN interface. It is worthwhile exploring a bit more about thermal oxidation of GaN due to this record low D_{it} and simple experimental setup.

The thermal oxidation of GaN usually yields β-Ga_2O_3 which is the most thermodynamically stable phase of all possible allotropes of gallium oxide.[48] The oxidation rate of GaN is extremely slow when the temperature is lower than 750°C.[49] The oxidation is a first order reaction for temperatures above 900°C. However, the surface roughness increased with increasing temperature. The following figures showed morphology of oxide surface (Fig. 2.1) and oxide/GaN interface (Fig. 2.2) at different temperatures. As shown in Fig 2.2, there are bubble shaped areas presented for samples oxidized at 950°C and 1000°C which suggests that GaN simultaneously thermally decomposed and was oxidized at these high temperatures.[46] This increasing roughness could deteriorate the interface quality and consequently increase the D_{it}. The lowest D_{it} of Ga_2O_3/GaN ever achieved (1×10^{10} $cm^{-2}eV^{-1}$) was conduct at an oxidation temperature of 880°C,[44] followed by one order of magnitude higher D_{it} of produced at 850°C [47] and 900°C [46] respectively. So the optimal oxidation temperature range is between 850 and 900°C in which the oxidation rate is significant and the interface quality is high.

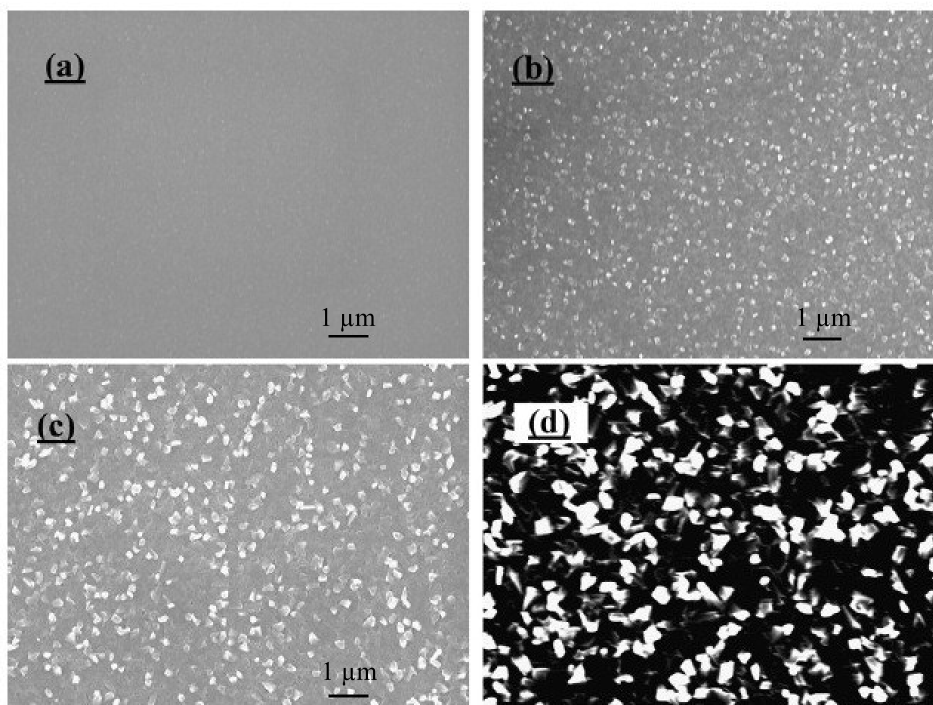

Figure 2.1 SEM images of Ga_2O_3 surfaces form at different temperatures (a) 850°C, (b) 900°C, (c) 950°C, (d) 1000°C.[46]

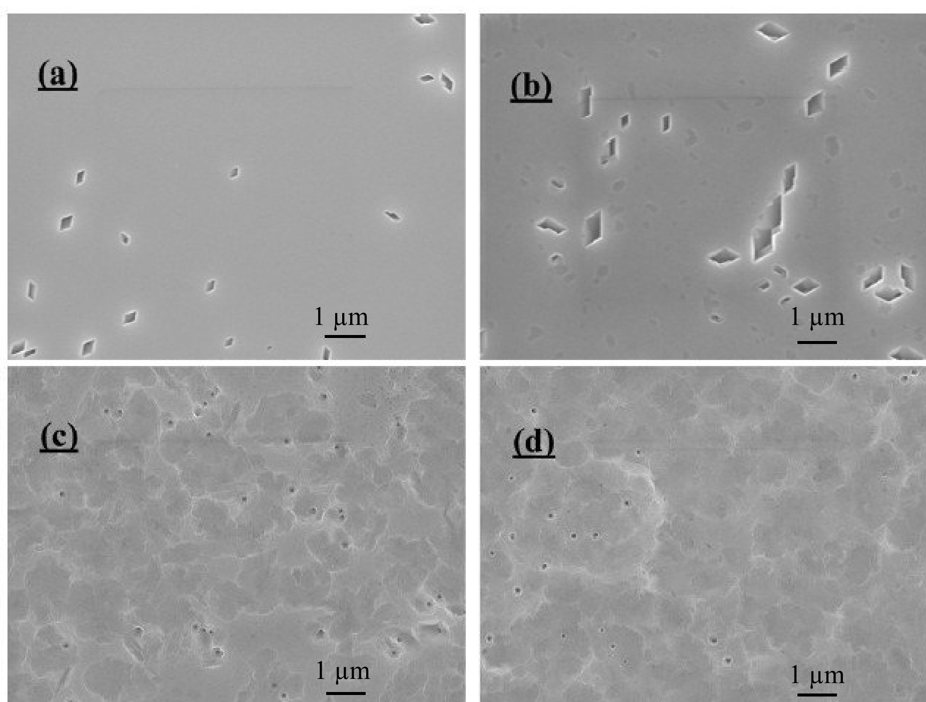

Figure 2.2 SEM images of the underlying GaN surface after the Ga_2O_3 layer was removed. The original oxidation temperatures were: (a) 850℃, (b) 900℃, (c) 950℃ (d) 1000℃ all for 6 hr. [46]

Other oxides as Gate dielectric

Chang *et al.*[50,51] deposited 10nm Gd_2O_3 with a moderate high dielectric constant of 17 on GaN by electron beam evaporation. With a relative small band gap (5.8 eV) of Gd_2O_3, 1100°C annealing for 5 min was conducted to refine the crystallinity of monoclinic Gd_2O_3, which reduce the leakage current from 7.9×10^{-6} to 4.6×10^{-9} A/cm^2 at 1 MV/cm. Capacitance-voltage measurements (C-V) showed a small frequency dispersion between 500 and 10 kHz indicating a low interface trap density, but no quantitative interface calculation was performed. Gd_2O_3 might be suitable gate oxide for high temperature processing of GaN.

Chui *et al.*[52] reported on the properties of 10 nm La_2O_3 deposited by electron beam evaporation on GaN. The dielectric constant was 13.1 which is much smaller than its static bulk dielectric constant of 30. The leakage current was suppressed by only 1 order of magnitude. A similar current suppression was also observed by Jur *et al.*[53] A 5 nm La_2O_3 was put down by evaporation of La and subsequently oxidized, the leakage current was 10^{-2} A/cm^2 at positive bias, which proves La_2O_3 does not efficiently of reduce the leakage current for GaN transistor. $LaAlO_3$ was promising for Si based transistor,[54–57] and a large band offset has been proposed on GaN (shown in Table 2.1), but more research is needed to verify this proposal.

Perovskite oxides such as $SrTiO_3$, TiO_2, $PbTiO_3$ usually have very large dielectric constant (up to 2000 for $SrTiO_3$),[11] and are excellent high k dielectric candidates for the application of dynamic random access memory (DRAM) [58]. Such high dielectric constants are achieved because of these oxides' crystal structures, usually cubic or tetragonal. Take $BaTiO_3$ as an example (fig 2.3), the Ti ions reside about the center of the Ti–O octahedral. A displacement of Ti ions causes great polarization, which can give rise to very large dielectric constants of 2000–3000. Since ions respond more slowly than electrons to an applied field, the ionic contribution begins to decrease at high frequencies.[13] Also, since the crystal structure of GaN is hexagonal, buffer layers such as MgO and TiO_2 might be needed to maintain the crystallinity of the Perovskite oxides.[59] Furthermore, Perovskite oxides usually have small band offsets with GaN. Improving the electrical breakdown strength and suppressing the leakage current on wide band gap GaN based transistor are still challenging. So more research on the application of perovskite oxide to GaN transistor for high frequency application is greatly needed.

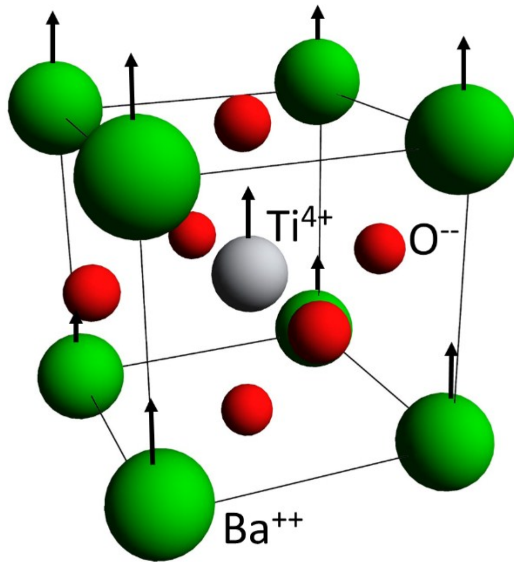

Figure 2.3 The unit cell of $BaTiO_4$. The displacement of the cation lattice with respect to the anion lattice induces a static dipole moment and thus, a spontaneous polarization in the perovskite crystal.

Ta_2O_5 has been deposited on GaN by ALD and EBE respectively.[60,61] EBE deposited 30 nm Ta_2O_5 film reduced the leakage current by 3 order of magnitude, but the interface traps was not measured. A 6nm thick Ta_2O_5 on AlN/GaN grown by ALD increased the drain current and transconductance. However, the interface trap density of above 10^{13} $cm^{-2}eV^{-1}$ was quite high.

SiN_x has the potential of achieving good SiN/GaN interface quality, but the device having PECVD SiN gate dielectric showed high leakage current.[62–64] So SiN coupling with other high band offset oxide such as Al_2O_3 should be more promising.

Sc_2O_3 has been deposited on GaN both as passivation layers and gate dielectrics by RF plasma assisted MBE and pulsed laser deposition.[65–67] Drain current slightly increased about 6% by MBE method.[66] A high interface quality with D_{it}=4x10^{11} $cm^{-2}eV^{-1}$ was achieved by pulsed laser deposition, and a low current density of 1x10^{-6} A/cm^2 at 30V gate bias.[67]

ZrO_2 has similar physical properties as HfO_2 such as a high dielectric constant of 23 and band gap of 5.8 eV.[11] Electron beam evaporation was applied as the deposition method to grow ZrO_2 on GaN.[63,68] There was a ~50% increase of the drain current and four-order of magnitude decrease of the leakage current. But, the intermixing with GaN was unexpected and further studies are needed to overcome this problem.

Summary

In general dielectrics with large k-value such as $SrTiO_3$ have small E_g (Fig. 2.4) leading to a small breakdown strength and less efficient of suppressing the gate leakage current. On the other hand, Al_2O_3 has the largest band gap of all the reviewed high-k oxides, and it has a moderate dielectric constant limiting the further scaling of the device. HfO_2 with a complimentary properties of slightly bigger band gap comparing to $SrTiO_3$ and a larger dielectric constant comparing to Al_2O_3 makes it a promising high k dielectric. Ga_2O_3 forms the best interface quality with GaN which could be realized by a simple deposition method. So combining the advantages of different high-k oxides would have great research potential to accelerating the development of GaN based power electronics.

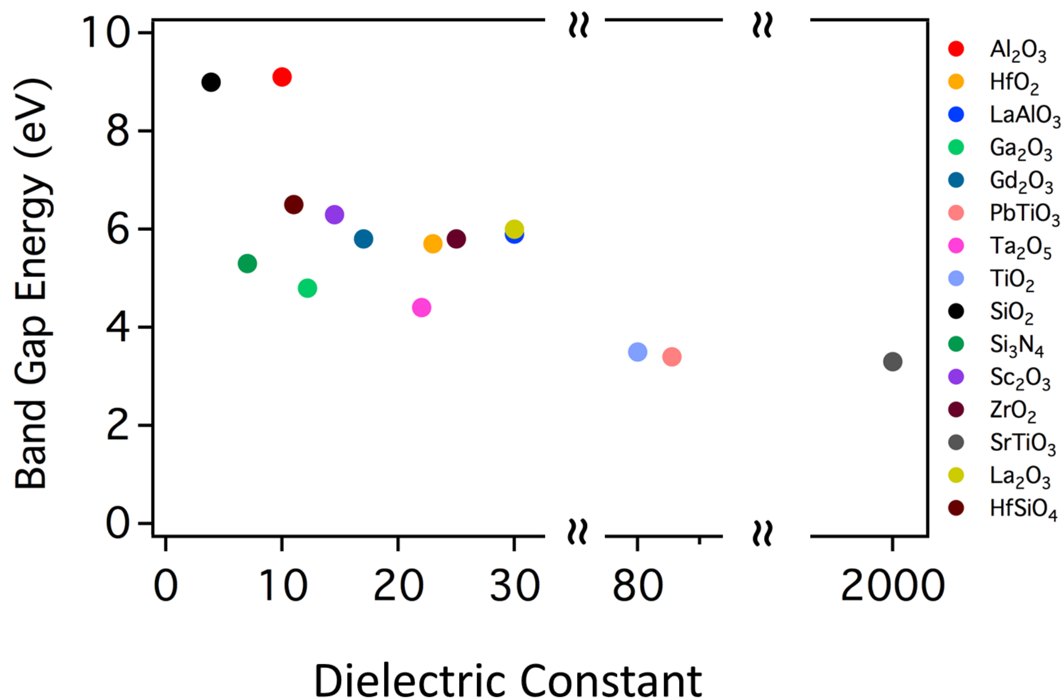

Figure 2.4 Distribution of the high-k dielectrics and their band gap.

Table 2.1 Summary of the reviewed oxides and their properties including band gap, dielectric constant and band offset with GaN.

Material	Band Gap E_g(eV)	Dielectric Constant ε	Conductance Band offset ΔE_c (eV)	Valence Band offset ΔE_v (eV)
Al_2O_3	8.8-9.4	9.0-11	2.1	3.4
HfO_2	5.6-5.8	21-25	1.09	1.6
$HfSiO_4$	6.5	11	1.57	
$LaAlO_3$	5.6-6.2	30	1.13	1.3
La_2O_3	6	30	1.97	0.8
Ga_2O_3	4.8	10.2-14.2	0.46	1.1
Gd_2O_3	5.8	17	1.9	0.7
$PbTiO_3$	3.4	78-104 (91)	0.4	
$SrTiO_3$	3.3	2000	-0.1	0.2
Ta_2O_5	4.4	22	0.1	0.9
TiO_2	3.5	80		
SiO_2	9	3.9	2.56	3.2
Si_3N_4	5.3	7	1.3	0.6
Sc_2O_3	6.3	14.5	1.97	0.8
ZrO_2	5.8	25	1.1	1.6

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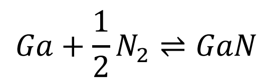
Chapter 3 - Device Fabrication

This chapter introduces growth of GaN crystal and the procedures necessary to make semiconductor devices. These deposition and fabrication techniques are also applied in the GaN MOS capacitor fabrication that will be discussed in Chapters 5, 6, 7 and 8.

Growth of bulk GaN

Early attempts to experimentally synthesize GaN started in the 1930s.[1,2] Only small GaN crystals were formed by passing ammonia over hot gallium.[3] GaN has a high melting temperature of 2500°C, and the nitrogen vapor pressure at melting point of GaN is ~45,000 atm.[4–6] So GaN cannot be grown from its stoichiometric melt due to these extreme conditions. Meanwhile, the free energy of GaN and its constituents Ga and N_2 are close because of the strong bonding between Ga-N and N-N (N_2).[7] Since N_2 is thermally stable even at elevated temperatures, ammonia (NH_3) is frequently employed instead, as a more reactive form at nitrogen. This will be discussed later in this chapter. At elevated temperatures, the free energy of Ga and N_2 decreased faster than that of GaN crystal (Fig 3.1), which makes GaN become thermodynamically unstable. As shown in reaction equation,



$$Ga + \frac{1}{2}N_2 \rightleftharpoons GaN$$

GaN tends to decompose to Ga and N_2 at high temperature (reverse reaction dominated), and it is hard to keep N_2 in the GaN without applying high pressure. This limits the production of bulk GaN from the melt, and alternative growth methods are being developed to form crystalline GaN.

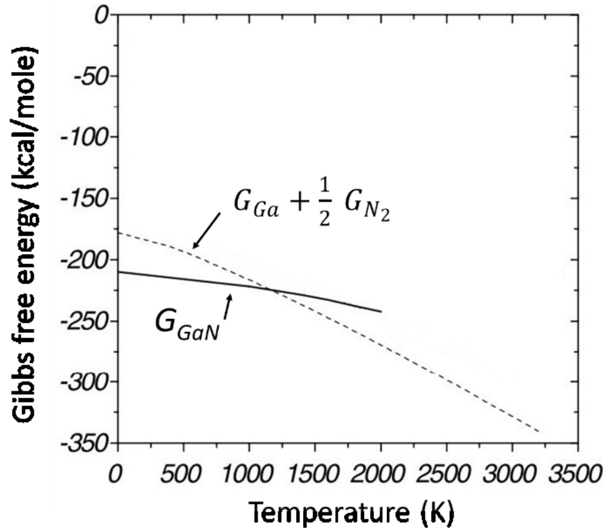


Figure 3.1 Gibbs free energy of 1 mole GaN and the (Ga + $\frac{1}{2}$ N_2) system as a function of the temperature at the pressure of 1 bar.[7]

GaN thin film growth

The first large area GaN layers were grown on sapphire by Maruska *et al*. in 1969 through chemical vapor deposition (CVD).[8] But the quality of crystal was low due to the high background impurity and nitrogen vacancy concentrations, which makes GaN n-type.[9,10] This problem was settled in 1983 by Yoshida *et al*.,[11] who developed the two-step method of growing GaN on sapphire. A thin AlN buffer layer was deposited in the first step followed by the epitaxial growth of GaN. This two-step method great improved the GaN crystal quality and formed the foundation of fabricating high speed GaN based transistor and laser diode in the 1990s and 21st century.

GaN is usually present in electronic devices as thin films, which are grown by metal organic chemical vapor deposition (MOCVD),[12–15] hydride vapor phase epitaxy (HVPE),[16,17] molecular beam epitaxy (MBE)[18–20], and pulsed laser deposition,[21] among which MOCVD and MBE are the most widely applied method in fabricating GaN thin films, and will be briefly introduced in the following paragraphs.

MOCVD

The source materials for growing GaN by MOCVD are usually trimethlgallium (TMGa) or triethyl-gallium (TEG) for Ga, and ammonia for N.[22] The dopants of making *n*- and *p*-type GaN are group IV elements and group II elements respectively. For example, methyl silane ($MeSiH_3$) or most commonly silane (SiH_4) works as a source of Si for *n*-type doping, and bis (cyclo-pentadienyl) magnesium (Cp_2Mg) works as a source for *p*-type doping.[23] H_2 is used as a carrier gas which flows through the liquid phase of metal organic and transports it in gas phase into the growth chamber (fig 3.2). GaN layers starts to grow on top of the substrate when the precursors of Ga and N are introduced to the chamber under a moderate pressure (10-760 Torr). The by-product of the reaction will be pumped out together with the H_2 carrier gas. Usually the substrate spins at a high speed to achieve a uniform deposition. Reaction temperature, chamber pressure, surface of the substrate, flow ratio and flow rate of the precursors are important parameters in determining the quality of deposited crystal.

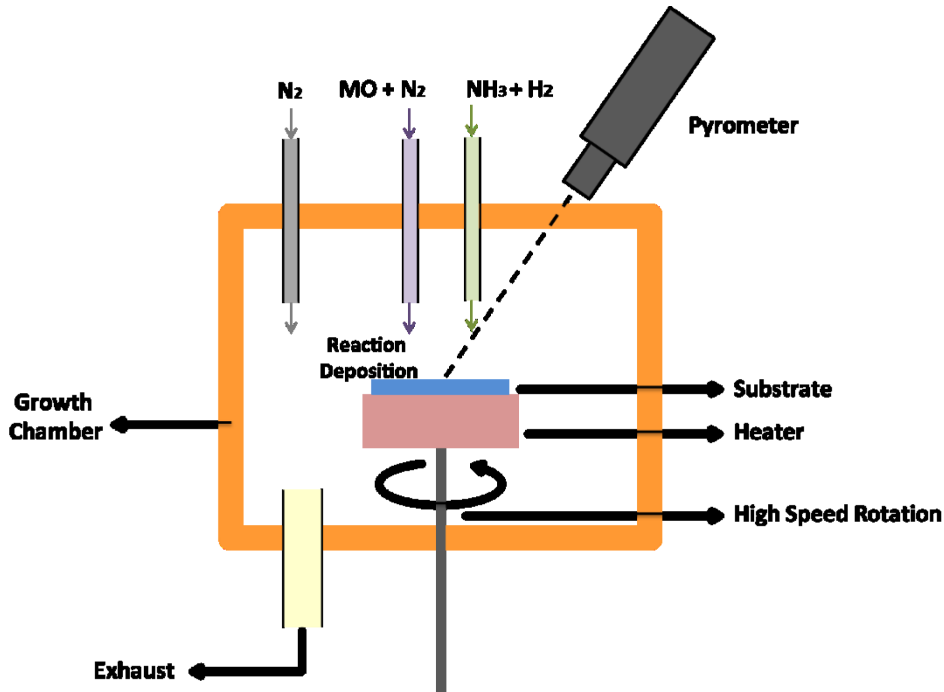
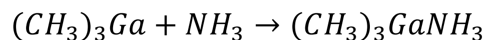


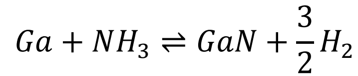
Figure 3.2 Schematic diagram of a MOCVD reaction system.

The reaction of MOCVD GaN involves adduct formation, decomposition of the adduct, reaction with NH_3 and forming GaN on the substrate.[13,14] The reaction equation of adduct formation is:



$$(CH_3)_3Ga + NH_3 \rightarrow (CH_3)_3GaNH_3$$

Subsequently, the $(CH_3)_3GaNH_3$ will decompose at the growth temperature forming $GaCH_3$ in gas phase. Then gaseous gallium species reacts with NH_3 follows the equation:[14]



$$Ga + NH_3 \rightleftharpoons GaN + \frac{3}{2}H_2$$

with a free energy ΔG of -42 kcal/mol at 1040°C.[14] Although the absolute value of ΔG is higher at lower temperature, meaning the forward reaction is favored, the formation of GaN is kinetically limited. [15] This enables the formation of only a very thin layer of polycrystalline and/or amorphous GaN on the substrate, and no further growth of GaN will occur at low temperature. This thin layer acts as a buffer layer that minimizes the lattice constant mismatch of GaN and the substrate.[24] By increasing the growth temperature, the reaction rate of GaN increases, and low defect crystalline GaN could be deposited on top of the buffer layer. Both AlN and GaN are used as buffer layers depending on the device application. For example, the big band gap of AlN makes it transparent to UV light and could be applied to detectors in the UV range.[25] Meanwhile, GaN buffer layer exhibited better electrical properties than AlN buffer and could be applied to fabricating electronic devices.[26]

MBE

Different from the MOCVD system, MBE uses pure Ga metal as group III source, and ammonia or reactive species of N_2 as nitrogen source.[19,20] Ga is heated in a Knudsen effusion cells (Fig 3.3). The evaporated gaseous Ga then condenses on the substrate and reacts with the nitrogen source. MBE requires an ultra-high vacuum (UHV) reaction condition, to enable a long mean free paths of the vaporized atoms. Meanwhile, many characterization methods that require UHV condition such as reflection high-energy electron diffraction (RHEED) and scanning electron microscopy (SEM) could be integrated in the MBE system and the quality of crystal growth could be monitored in situ. There is no carrier gas in MBE system which also reduce the potential contamination of the product. Another key advantage to MBE is that GaN can be grown without the use of hydrogen, which compensates the electrical acceptors.

The development of GaN MBE was slow in the 1980s, and one of the reasons was that ammonia as a precursor of nitrogen source decomposes at high temperature, and the low temperature has to be applied which limits the epitaxial rate. Alternative nitrogen sources had to be developed due to the difficulty of N incorporation using ammonia at low temperature. Electron cyclotron resonance (ECR) and radio frequency (RF) plasma were used to generate

reactive nitrogen species. However, the high energetic ions produced by the plasma are detrimental to the deposited crystal, and the energy of ECR or RF has to be well controlled.[27]

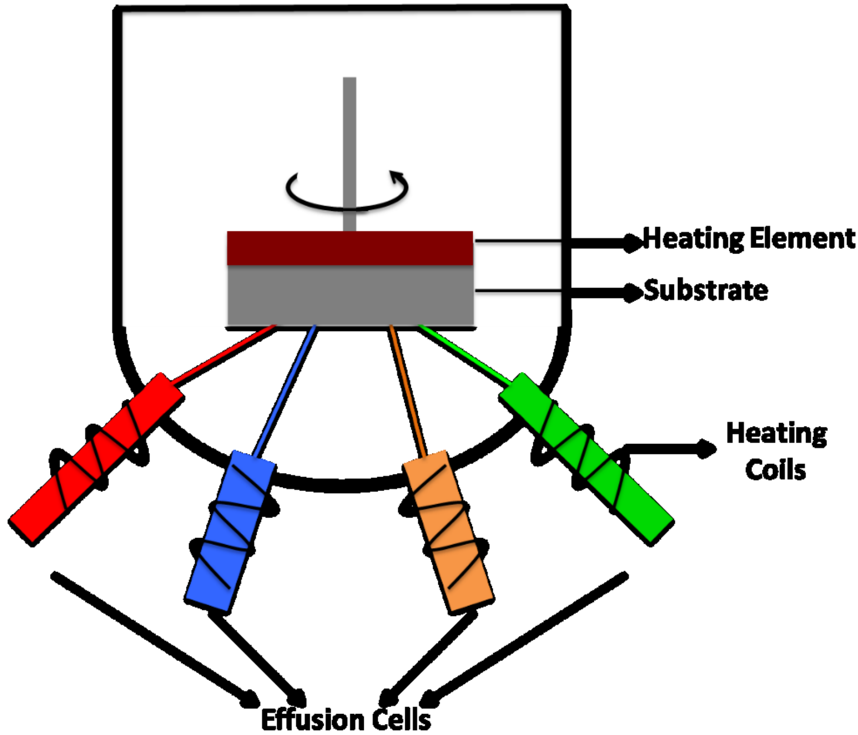


Figure 3.3 Schematic picture of MEB reaction system

Gate dielectric deposition

The gate insulator of GaN based MOS device had been deposited by several different methods such as atomic layer deposition (ALD),[28–35] MOCVD,[36,37] plasma enhanced CVD[38,39] and RF sputtering.[40,41] Among these deposition techniques, ALD has been the most extensive developed because of the IC chip processing, and the International Technology Roadmap for Semiconductors (ITRS) also has ALD included for growing high-k gate insulators in the silicon MOSFET structures.[42] As the continuous scaling of semiconductor device, the thickness control of the gate oxide needs to be on the atomic level. Also, a conformal thin film is desired for the high aspect ratio structures. ALD has demonstrated its capabilities and produces the best conformality comparing to all other thin film deposition methods.[42]

ALD

Generally speaking, high-k oxide are formed through a binary reaction in ALD. As shown in figure 3.4, one cycle of the reaction could be divided into four steps: exposure to metal precursors, inert gas purge, exposure to oxygen precursors and a second purge. During the first step, metal precursors are introduce to the reaction chamber and will deposit on each available surface site of the substrate. Although, some of the surface sites might react with the precursors first and accumulate multiple layers of precursor molecules, the unreacted molecules will subsequently desorb from the surface where the reactions are completed, and travel to the available open surface sites. The technical term of this phenomena is self-limiting, and can only be realized when the precursor is not self-reactive. Then the purging gas is introduced to the chamber to remove the excess metal precursor molecules leaving a sub-monolayer of the deposited film. In this way, precise thickness control at nano-scale level is achieved. A similar mechanism is used with the oxygen precursors in the next step. The oxygen precursors will react with metal precursors to complete the formation of the desired compound. A second purge is introduced to remove the excess oxygen precursor and the by-product, leaving a monolayer of the deposited film. This self-limiting character yields excellent step coverage and conformal film even on high aspect ratio structures such as trench capacitors for DRAM.[43] Meanwhile no surface sites are left uncovered during the ALD process; the films are usually pinhole free, which is crucial for application of gate insulation.

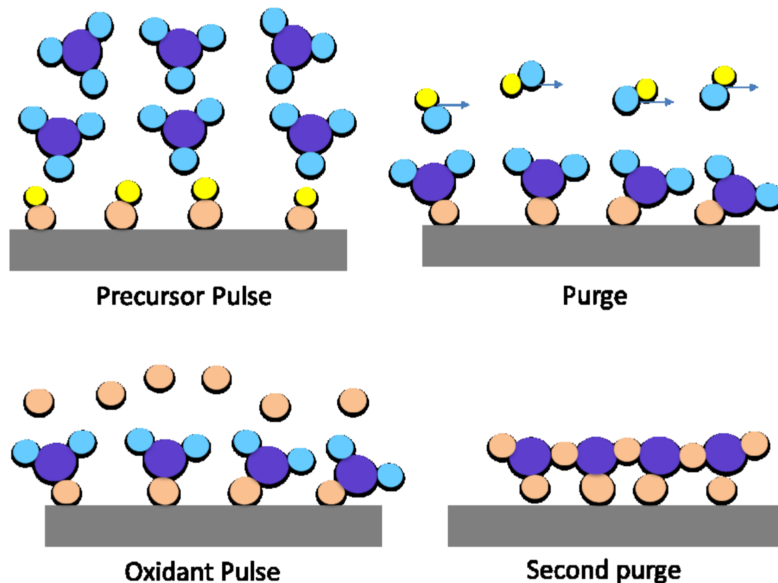


Figure 3.4 Schematic picture of one cycle ALD processing

Thermal ALD

In thermal ALD system, the precursor for oxygen is usually H_2O and the reaction does not involves the aid of plasma or free radicals.[42] The binary reactants of thermal ALD are the same as their counterpart CVD. The difference is that reactants are introduced individually in ALD while both reactants are present simultaneously in CVD. Thermal ALD does not require a high reaction temperature. Deposition temperature as low as 150°C was reported for Al_2O_3 ALD,[44] and 150°C for TiO_2 ALD.[45]

Plasma assisted ALD (PA-ALD)

Plasma ALD was firstly developed for single-element film deposition in which H_2 plasma was used to reduce the metal or semiconductor precursor such as ALD of Ti, Ta and Si.[46–48] In addition to depositing single-element films, high-k oxide could also be grown by PA-ALD where the oxygen precursor is O_2 plasma. This highly reactive precursor initiates the deposition at a lower temperature. Compare to H_2O, an O_2 plasma is easier to remove by the inert gas purge, which reduces time of ALD cycles and increases the overall deposition rate.[49]

Metal contacts

Schottky contact

There are two types of metal-semiconductor contacts: Schottky and Ohmic.[50] A Schottky contact has a rectifying effect which makes the current-voltage curve across the junction asymmetric or non-linear (Fig. 3.5 a). Take an *n*-type semiconductor as an example, when the metal has a work function Φ_m that is larger than that of semiconductor (Φ_s), the Fermi level of the semiconductor is higher than that of metal before contacting. As the metal and semiconductor are brought into contact, electrons are transferred from the semiconductor to the metal until their Fermi levels are aligned.[51] With the migration of electrons, an electric field is created called the equilibrium contact potential V_0, which prevents further net electron diffusion from the semiconductor into the metal, and the magnitude of V_0 is the difference of the work function (Φ_m-Φ_s).[51] Also, there will be a depletion region formed in the semiconductor with the width of W and a barrier height formed at the metal-semiconductor interface Φ_B which is $\Phi_{m-\chi}$, where q χ is the electron affinity of semiconductor measured from the vacuum level to the conduction band.[51]

When a positive voltage is applied to the metal, the contact potential is decreased by the magnitude of the applied voltage. Consequently, the electric field is weaker and electrons flow from semiconductor to the metal. The current is given by:[51]

$$I = I_0(e^{\frac{qV}{kT}} - 1)$$

where V is the applied voltage, k is the Boltzmann constant and T is the absolute temperature.

Ohmic contact

An Ohmic contact does not have the rectifying effect; the current is symmetric and linear (Fig. 3.5 b). An ideal Ohmic contact should have no voltage drop in theory when current passes. As shown in figure 3.5b, the work function of metal is small than semiconductor, so electrons will flow from metal to semiconductor when they are brought in contact. Electron will not stop flowing until the Fermi levels are aligned. In this configuration, no depletion region exists in the semiconductor, because majority carriers accumulate at the junction corresponding to the electrostatic potential difference.[51] An alternative method of making Ohmic contact is to heavily dope the semiconductor to reduce the width of depletion layers. In this way, electrons can tunnel through the barrier without going over it.

Due to a large band gap of 3.4 eV, it is hard to find a metal with work function large enough to form an Ohmic contact on *p*-type GaN while for *n*-type GaN, several studies have been reported methods to make low resistivity contacts. A resistivity of $8 x 10^{-6}$ ohm cm^2 was prepared by Lin *et al*.[52] by applying Ti/Al metal alloys. Continuous reduction of resistivity has been achieve by Feng et al.[53] by using Ti/Al/Ni/Au. With the same alloy, using a reactive ion etching of GaN before metal deposition and a high temperature annealing as a post-treatment further decreased the resistivity by additional order of magnitude.[54] This probably due to a removal of oxide insulating layers while Ti forms TiN on the Ti/GaN interface generating N vacancies and increased free moving electrons.[54]

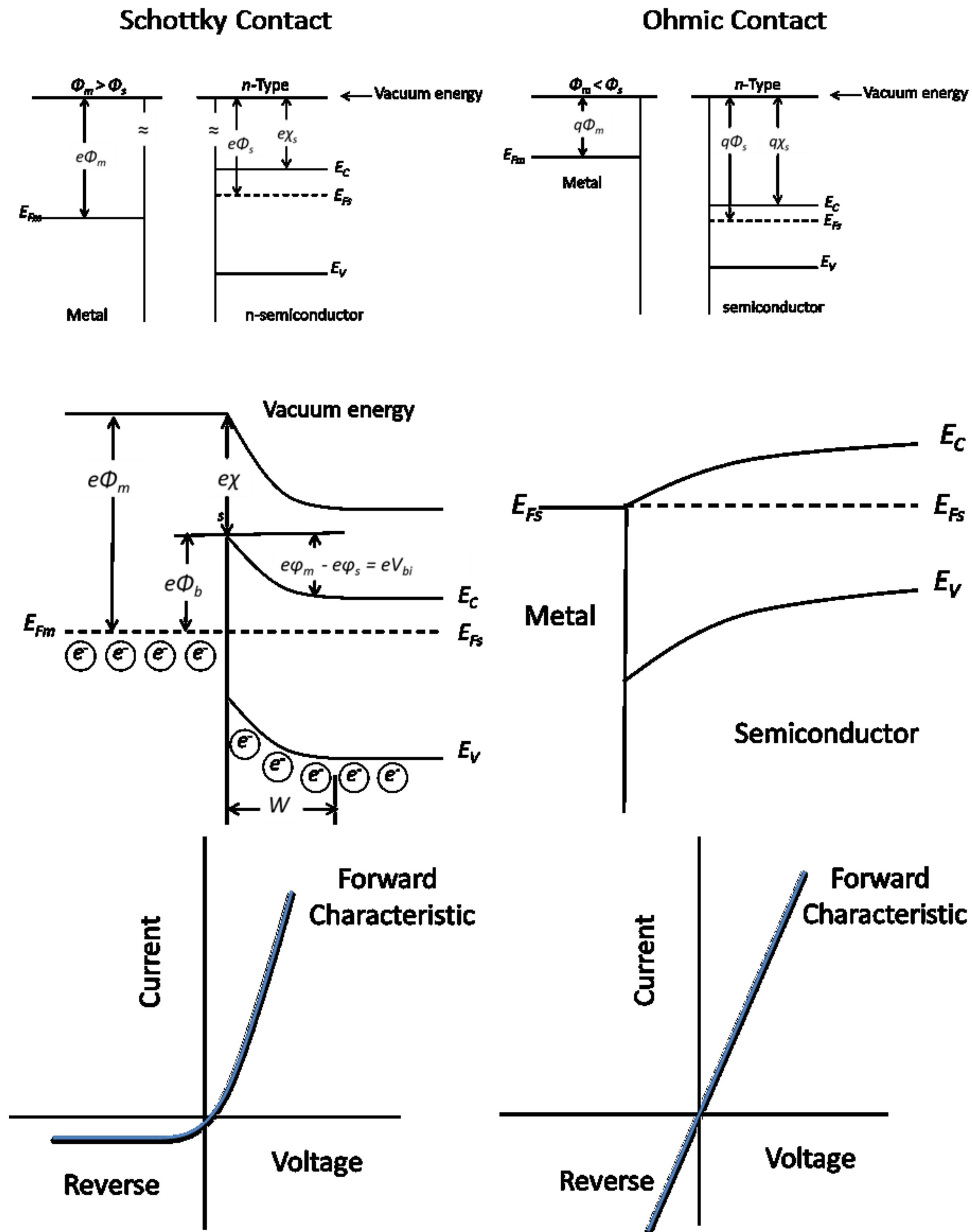


Figure 3.5 (a) Schottky contact of metal and n-type semiconductor junction (b) Ohmic contact of metal and n-type semiconductor junction.[51]

Metal contacts deposition

The main techniques of metal deposition include vacuum evaporation and sputtering, with the system setup for the former being simpler than that of later.[55] Vacuum evaporation can be further divided in to regular evaporation in which the sources are heated through contact with a resistance heater to raise their vapor pressure and electron-beam (e-beam) evaporation where an electron beam with intensive energy is used to locally heat up and evaporate the metal source. All the metal contacts in this study were fabricated by e-beam evaporation.

The setup of e-beam evaporation is shown in figure 3.6. From the bottom to top, a high energy electron beam is generated with high voltages (>10kV). Subsequently, the beam is bent and focused by a magnetic field to the surface of metal source. Evaporation happens at the highly localized hot point of the metal source while the rest area remains cold in a solid phase. This arrangement reduces contamination from the crucible because it remain at room temperature. Different metal sources are set on multiple hearths to achieve a multilayer film deposition without opening the deposition chamber and breaking the vacuum. This configuration also reduces the chance of impurity incooperation. The chamber pressure is pumped down to ~10^{-7} torr to minimize the residual contamination in the system and ensure the mean free path of the evaporated elements is long enough to reach the surface of the substrate.

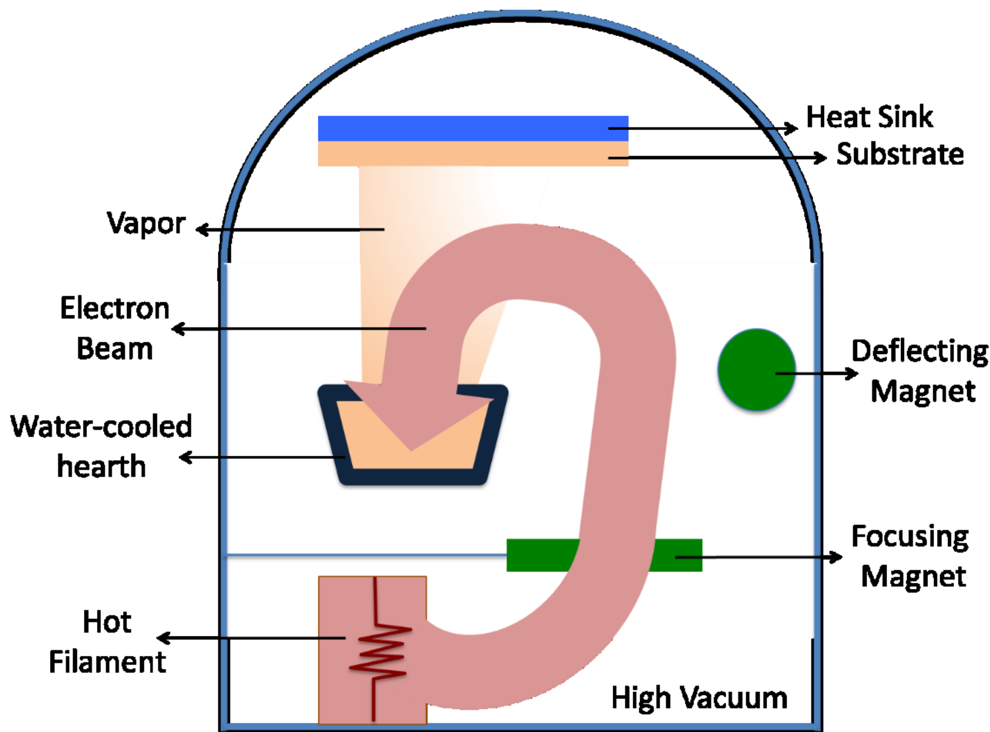


Figure 3.6 Schematic diagram of an e-beam evaporation system.

In this dissertation, the ohmic and gate contact of GaN metal oxide semiconductor capacitors (MOSCAPs) were deposited by electron beam evaporation with the composition of Ti/Al/Ni/Au for the ohmic contact and Ni/Au for the gate contact.

Lithography

Lithography enables printing patterns of different materials on the semiconductor substrate. The concept of lithography is straight forward. After a light sensitive photoresist is spun on its surface, the wafer is subsequently exposed by shining light through a mask.[56] The mask contains the desired patterns which allows light to pass through some area while blocking the rest. The exposed areas of the photoresist become soluble (or insoluble) in a developer solution. Then the whole wafer is transferred to a developing bath to complete the feature patterning. The resist may be used as a mask for ion-implantation, etching protection or metal liftoff in the following processes.

As the technology for fabricating modern device advances, the increasing demands could push the lithography to an expensive and complex system. The precision of the state-of-the-art lithography tool is better than 22nm which makes it a crucial part of today's chip manufacturing. An increasing the number of integrated device per chip requires making smaller structures. So the resolution needs to be very high (<22nm). The wafer size is also increasing from 12 inch to 18 inch (for Si IC manufacturing), which requires a larger exposure area. Placement accuracy is also important because each mask layer needs to be carefully aligned with respect to the existing pattern.[56] Moreover, fast throughput and low defect densities are crucial to improve the yield and quality of the fabrication device. Those requirements make lithography one of the most expensive tools in IC manufacturing.

In the studies of N-polar GaN pretreatment and comparison of ALD on c- and m-plane GaN, negative and positive photoresists were applied to develop circular patterns for the deposition of gate contact. To fabricate a top-to-bottom structure for MOSCAPs, accurate mask alignment was performed before applying photolithography for ohmic contact deposition.

Etching

After the pattern is developed on the surface, the underneath films are removed by etching with the protection of photoresist or hard masks (oxides or nitrides) to leave the desired pattern of the film.[56] There are two etching methods: wet and dry etching so named depending on

the etch environment. In wet etching, the wafers are immersed in chemical solutions where the film could be attacked by the etchant leading to an isotropic etch. In contrast in dry etching, gas-phase etchants (usually plasma) are used and accelerated to the wafer to remove the every exposed material on the surface. This leads to a lower selectivity but higher directionality than wet etching.

For the high-k nano-laminate studies, Ga_2O_3 was sputtered by Ar plasma in a dry etcher. The reason for removing the thermal oxide of GaN is to form lower resistive contacts, and consequently improve the electrical examination.

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Chapter 4 - Device Characterization

To evaluate the properties of the high-k oxides prepared in this study, their composition, chemical bonding state, impurity concentration and surface morphology were characterized by several microscopic and spectroscopic techniques. The electrical properties of the metal oxide semiconductor capacitors (MOSCAPs) integrated with the high-k materials were also characterized by capacitive-voltage (CV) and current voltage (IV) measurements. The results of the electrical, chemical and physical characterizations were further compared and correlated with their processing conditions, to provide feedback on the device fabrication. In this way, the process condition of oxide could be optimized and the performance of the device could be better controlled.

In this chapter, all the techniques used in this study are briefly introduced.

Microscopy

Microscopy contains a wide variety of methods to visualize features, monitor the device surface morphology and structure that are too small to resolve by the unaided human eye. In this study, optical microscopy, atomic force microscopy (AFM) and scanning electron microscopy (SEM) were the main techniques to characterize the high-k surface.

Optical Microscopy

Optical microscopy is the oldest form of microscopy, which can be dated back in the 1590 when Hans and Zacharias Janssen built the first compound microscope.[1] In optical microscopy, lights from the object usually travel through lens (or multiple ones) and a magnified real image was either “formed” in front of human eyes or detected by charge coupled device (CCD) cameras. This technique is handy in resolving micro-level features due to a relatively straight forward system and easy-to-load sampling without complicate sample preparation. However, features smaller than one micron are hard to be observed because of the resolution limitation of the optical microscope.

The resolution of an optical microscope is given by the equation:[2] [Equ 4.1]

$$\delta_{min} = \frac{0.61\lambda}{NA}$$

where δ_{min} is the resolution, NA is the numerical aperture and λ is the wavelength of the light source. With visible light as the illuminating source, this equation yields a resolution somewhere around 200 and 300nm in the air. This resolution could be applied to resolve the photolithography pattern in this study, but the thickness of the high-k layer employed in this study is usually below 30nm, which requires other microscopy techniques with higher resolutions to accurately measure.

Scanning Electron Microscopy (SEM)

In SEM a beam of electron is generated, accelerated and focus on the surface of sample by magnetic coils. The image is generate by a raster scanning of the focused beam, which generates electrons emitted from the sample containing information on the topography, composition and electrical conductivity of its surface. Two kinds of electrons can be are detected: backscattered electrons and secondary electrons. These electrons will be collected by the detector combining the beam position to reproduce the surface of the samples like duplicating keys.

The resolution of a SEM also obeys equation 4.1. In an SEM, the source is energetic electrons, and the de Broglie wavelength of an electron with certain accelerating voltage can be defined as: [3]

$$\lambda = \frac{h}{mv}$$

where h is Plank's constant, mv is the momentum of electron which equals:

$$mv = \frac{1}{c}\sqrt{(eV + m_p c^2)^2 - (m_p c^2)^2}$$

where m_p is the electron rest mass, c is the speed of light. So for an accelerating voltage of 100kV, the wavelength of the electron is 3.7pm.

In this research, the FEI FE-SEM was used to observe the morphology of GaN substrates and the deposited high-k gate oxides. In this system, the field effect was applied to the tungsten tip generating a strong electric field which allow electron to escape into the vacuum through tunneling. Compared to thermal emission, the field effect source generates more electrons with a smaller current, and consequently achieves a longer source lifetime. An energy dispersive detector is also integrated with SEM, which enables identification of elements within the same

system. This makes FE-SEM a handy tool for characterizing the microstructure and compositions of sample surfaces.

Atomic Force Microscopy (AFM)

AFM operates by measuring attractive or repulsive forces between the AFM tip and surface atoms. The tip is usually a Si or Si_3N_4 pyramid mounting at the end of a Si spring or "cantilever", which may be fabricated by a series of semiconductor processes including CVD, photolithography, reactive ion etching (RIE) and anisotropic wet chemical etching.[4] There are generally two modes in AFM: contact and tapping. In contact mode, the tip works under the repulsive force; while in tapping mode, the tip vibrates at a high frequency and the force between tip and sample is either repulsive or attractive. The resolution of both modes are determined by the tip radius (usually in the nanoscale range ~5nm). Either the tip or the sample is attached to a piezo scanner which can accurately control the raster scan with a high scan rate. The tip does not stay at a constant height above the sample during the scan, because it could result in a crash of the tip or loss of connection with the surface if the height of surface topography change dramatically. A feedback loop is integrated into the system to adjust the tip height instantaneously. The force between the tip and surface atoms is small, so its movement (bend up and down) induced by the chemical bonding is magnified by using the optical lever. Typically, a low power laser shines on the back of the cantilever and is reflected to the position sensitive photodiode. By adjusting distance of the reflected laser beam to the cantilever, a magnification of 200 could be achieved. So an angstrom bending of the tip could make a 20nm movement of the laser beam on the photodiode detector. This setup ensures an accurate and sensitive monitor of surface topography.

A Veeco Multimode Scanning Probe Microscope was used to characterize the topography of the ALD high-k gate oxides and the initial and cleaned GaN surfaces. This gives a better resolution of the surface morphology than SEM, because the high-k materials are usually insulating, which causes a surface charging effect that limits the beam voltage in SEM, subsequently lowering the resolution of SEM. Beside resolution, AFM can also provide the roughness of the deposited film and straight forward three-dimension view of the surface. Moreover, the AFM images reflect the top most surface. In contract, the electrons used to form an image in an SEM actually come from a certain depth. Hence the image of the surface is

generally not nearly as detailed as an AFM image. In general, AFM image accurately reflected the surface quality and could be correlated to with the electrical properties analysis such as density of interface traps and hysteresis.

X-ray Diffraction (XRD)

XRD is a technique to determine the crystal structure of a sample. A crystalline array of atoms (long range order of atoms) in the material causes x-ray beam to diffract. By measuring the angles and intensities of the diffract beam, the crystal structure of material can be depicted. The correlation of the spacing between planes of atomic lattice (d) and the incident angle of the x-ray beam (θ) is:[5]

$$\lambda = 2dsin\theta$$

A Rigaku desktop Powder X-ray diffraction and a grazing incidence x-ray diffraction (GID) were used to characterize the crystallinity of the GaN substrate and the ~20nm ALD TiO_2 high-k films respectively. As the incidence angle increases from 0.3 to 0.5°, the penetration depth of x-rays inside the material is increase by three orders of magnitude, typically from 1-10 nm to 1-10 μm.[6] In this study, the configuration of 20nm high-k on 5 μm GaN single crystalline substrate, the GaN peak intensity could be so strong that it washed out the peaks of thin crystalline high-k film. The advantage of GID is to keep the incident x-ray at a small angle and confine the penetration within 10nm. So the results will solely contain information of the thin film without interference of the substrate.

X-ray photoelectron spectroscopy (XPS)

XPS is an extremely surface sensitive technique that determines the surface elemental composition, bonding and chemical state. In XPS system, a beam of x-ray was focused on the sample surface, and subsequently generating photoelectrons which would travel through the UHV XPS chamber to the detector. The energy and intensity of the photoelectrons are dependent on the elements that are present and their surface concentrations, and their chemical bonding state, so XPS represents different elements with their unique spectrums. Because the mean free path of electron in solids is very small, the photoelectrons that finally make it to the detector originate from only the top few atomic layers, which makes XPS surface sensitive.[7] Quantitative data can be obtained from peak intensity and identification of chemical states can be determined from the peak position.

A K-alpha x-ray photoelectron spectrometer from Thermo Scientific was used to characterize the chemical composition, chemical state and stoichiometry of the ALD dielectrics. Al Kα was used as the x-ray source due to its narrow line width of 0.85eV and a moderate energy of 1486.6eV. Although 1500V would be high enough to generate x-rays, 15kV was usually applied (one order of magnitude higher) to ensure a massive x-ray photon flux which provides a good resolution and compatible sensitivity.[8] The relationship of a photon interacting with a core level electron is governed by the Einstein equation:[8]

$$KE = h\upsilon - BE - e\phi$$

where KE is the kinetic energy of the ejected photoelectron; $h\upsilon$ is the characteristic energy of incident x-ray photon (1486.6eV); BE is the binding energy of core level electron and ϕ is the work function of the material. Ar ion sputtering was used to clean the carbon and oxygen elements from the surface which are ubiquitous from the absorption of the CO_2, O_2 and hydrolysis in the atmosphere. An Ar ion sputtering was also applied in performing the depth profile of elemental distribution throughout the high k material.

Electrical characterization

The advantages of electrical characterization are simple sample preparation, accurate and non-destructive in assessing material quality and device reliability.[9] Several important parameter could be directly derived from the characterization results such as carrier doping density, type and mobility of carriers, interface quality, oxide trap density, contact resistances and so on.

The above parameters of the GaN MOS capacitors were determined through capacitance voltage (CV) and current voltage (IV) measurement using a Keithley 4200 semiconductor characterization system. These characterization techniques provide information on the interface quality including defects, interface states and the roughness, so as to monitor the changing of carrier mobility, low frequency noise and device reliability. Also, a high quality oxide is crucial in preventing currents from flowing between the gate and substrate. So both interface qualities and gate dielectric qualities need accurate and easy-to-use assessment to keep the device performance as ideal as possible.[9]

Capacitance voltage (CV)

The following description of CV was mainly taken from the electrical measurements section of MOS capacitors reported in Plummer *et al*.'s book.[10] For CV measurements, an MOS

capacitor is needed, consisting of a semiconductor substrate, a dielectric layer and a gate contact as a conducting electrode. CV can provide detailed information about the dielectric film and dielectric/semiconductor interface. This study employed GaN MOS capacitors so the following explanation of CV will take an ideal (very small interface defects) metal/oxide/n-GaN MOSCAP as an example.

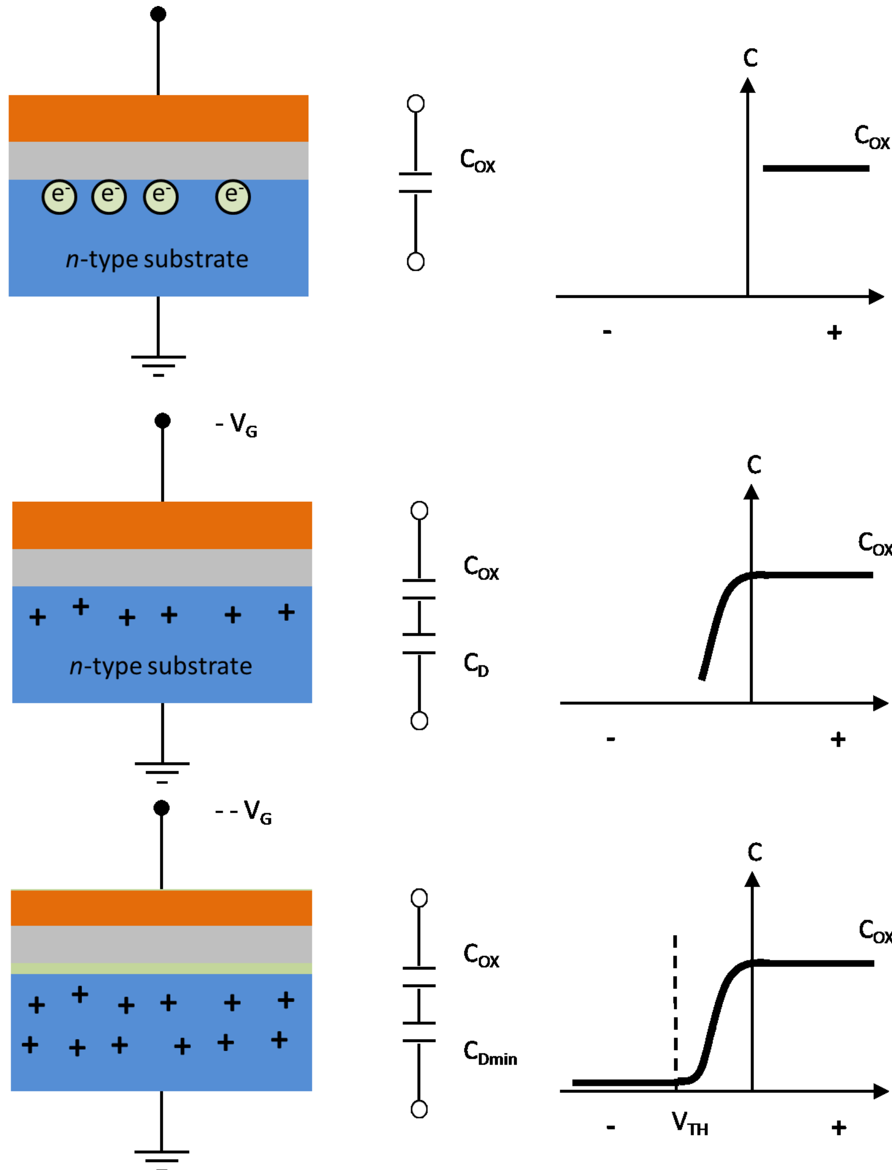

Figure 4.1 MOS capacitor structure with the equivalent circuit and its operation at (a) accumulation region, (b) depletion region, (c) inversion region.[10]

Generally speaking, a CV sweep consists three regions of operation: accumulation, depletion and inversion. The voltage applied to the gate is usually a DC voltage (V_G) to attractive the majority carrier (electrons) or minority carrier (holes) close to the interface of the oxide/*n*-

GaN. Consider a positive voltage $+V_G$ applying to the gate corresponding to the accumulation region in Fig 4.1 (a), the electrons in the *n*-type GaN substrate are attracted close to the gate until they got stopped by the insulating dielectric layer. If a small AC signal is superimposed on V_G, the capacitance of the dielectric oxide (C_{ox}) could be measured. Subsequently, the dielectric constant and thickness of the oxide could be calculated by:

$$C_{ox} = \varepsilon_0 \varepsilon_{ox} \frac{A}{d}$$

where ε_0 is the permittivity of the vacuum, ε_{ox} is the dielectric constant of the oxide, A is the area under the metal contact and d is the thickness of the oxide.

Applying a negative DC gate voltage (Fig 4.1b) repels electrons from the *n*-GaN surface creating a depleted region. The electric field generated by the $-V_G$ needs to be terminated by the holes in *n*-GaN substrate to maintain charge neutrality. As a result, the density of gate charge Q_G should be equal to the density of charge in depletion region Q_D, and the measured capacitance C is a result of the Cox and C_D in series. The mathematical expressions are:

$$|Q_G| = |Q_D| = N_D x_D$$

$$\frac{1}{C} = \frac{1}{C_D} + \frac{1}{C_{ox}}$$

$$C_D = \frac{\varepsilon_0 \varepsilon_s}{x_D}$$

where N_D is the doping concentration in GaN, x_D is the depth of depletion region (assuming a uniform doping), ε_s is the dielectric constant of GaN. C_D is a function of V_G, because as V_G becomes more negative, x_D grows wider. This yields a smaller capacitance.

For larger values of negative DC gate voltage, more holes will gather at the oxide-semiconductor interface to terminate the stronger electric field. If the concentration of holes is large enough to form an inversion layer, the gate voltage at which this occurs is called threshold voltage and it is also the voltage required to turn on a MOS transistor.[10] Once the inversion layer forms, x_D stops growing and reaches its maximum value (Fig. 4.1c). A charge balance equation is:

$$Q_G = N_D x_D + Q_I$$

where Q_I is the charge density in the inversion layer. However, in GaN, the carrier lifetime is very long. In other words, the generation of holes is slow and does not occur fast enough to meet

the increasing rate of negative V_G. So gate charge still needs to be balanced by expanding the width of depletion layer. Thus a *deep depletion* region is observed on the CV curve.

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Chapter 5 - Influence of Atomic Layer Deposition Temperatures on TiO_2/n-Si MOS Capacitor

Abstract

This study reports on the influence of deposition temperature on the structure, composition, and electrical properties of TiO_2 thin films deposited on *n*-type silicon (100) by plasma-assisted atomic layer deposition (PA-ALD). TiO_2 layers ~20nm thick, deposited at temperatures ranging from 100 to 300°C, were investigated. Samples deposited at 200°C and 250°C had the most uniform coverage as determined by atomic force microscopy. The average carbon concentration throughout the oxide layer and at the TiO_2/Si interface was lowest at 200°C. Metal oxide semiconductor capacitors (MOSCAPs) were fabricated, and profiled by capacitance-voltage techniques. The sample prepared at 200 °C had negligible hysteresis (from a capacitance-voltage plot) and the lowest interface trap density (as extracted using the conductance method). Current-voltage measurements were carried out with top-to-bottom structures. At -2V gate bias voltage, the smallest leakage current was 1.22×10^{-5} A/cm^2 for the 100°C deposited sample.

*This chapter serves as a preliminary test study of ALD high k oxide on a more widely known semiconductor substrate silicon. This work was collaborated with Naval Research laboratory and contributed by Daming Wei and Tashfin Hossain from Dr. James Edgar's group.

Published as

D. Wei, T. Hossain, N.Y. Garces, N. Nepal, H.M. Meyer, M.J. Kirkham, C.R. Eddy, and J.H. Edgar, ECS J. Solid State Sci. Technol. 2, N110 (2013) DOI: 10.1149/2.010305jss

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Introduction

Titanium oxide thin films have many applications such as photocatalyst,[1] solar cells,[2] gate insulators,[3] and dielectrics.[4] With the potential of achieving an extraordinarily high dielectric constant [up to 130 for rutile TiO_2,[5, 6] 2000 for $SrTiO_3$[7]], TiO_2 is also an appealing dielectric for capacitors in the dynamic random access memory (DRAM), the main memory device in modern computers. Since the capacity and performance of DRAM greatly affects the working speed of a computer, much attention has been given to optimize DRAM. As proposed by the International Technology Roadmap for Semiconductors (ITRS),[8] DRAM capacitors with higher capacitance, thinner equivalent oxide thickness (EOT)[9] and smaller leakage current density are highly desirable. The insulator deposition temperatures should be below 500 °C, because capacitors are expected to be deposited after transistors formation.[10] However, further research on the high dielectric materials is needed to fulfill those requirements.

In the present study, plasma-assisted atomic layer deposition (PA-ALD) was employed to deposit thin insulating TiO_2 films, because it offers excellent atomic level control of layer thickness with good uniformity and conformality.[11] With an O_2 plasma, the deposition can be conducted at a lower temperature and with a shorter purge time in cold-wall reactors than a conventional thermal ALD system.[12] These characteristics are particularly suitable for growing capacitor dielectrics for use in DRAM, as it uses a three dimensional structure with a high aspect ratio to increase the effective surface area.[13]

The present work reports on the impact of the deposition temperature on the properties of TiO_2 films prepared by PA-ALD and on the performance of said films in silicon MOSCAPs. By correlating the oxide structure, surface morphology and impurity concentration with electrical properties (hysteresis, interface trap density and leakage current), an optimal deposition temperature is identified.

Experimental Procedure

A. TiO_2 ALD Film Growth and Metal Contact Deposition

Before deposition, the *n*-type Si (100) substrates were cleaned with acetone and isopropyl alcohol (IPA) for 5 minutes at 40°C. TiO_2 was deposited by PA-ALD in an Oxford Instruments FlexAL ALD reactor with tetrakisdimethylamino titanium (TDMAT) kept at 39°C as the titanium precursor, and oxygen plasma as the oxidizing agent. The ALD growth temperatures

were 100°C, 150°C, 200°C, 250°C and 300°C. All ALD depositions consisted of 400 cycles and each ALD cycle included a 0.4 second dose of TDMAT followed by a 4 second purge with Ar gas, and a 3 second exposure to the oxygen plasma followed by a 3 second purge. The plasma power and pressure during exposure was set to 400 Watts and 15 mTorr, respectively, with an O_2 flow rate of 60 sccm. Circular capacitors (50-300 μm diameter) with Ni/Au (20/100 nm) metal contacts on top of the oxide were created by standard photolithography and e-beam evaporation methods. The current-voltage test structures consisted of the top capacitor contact and the bottom contact which was bare silicon held on the conductive measuring stage with constant vacuum pumping at the center of the sample.

B. TiO_2 Film Characterization

The TiO_2 film morphology was measured by atomic force microscope (AFM, Digital Instrument MultiMode SPM from Veeco Instruments Inc) operating in tapping mode.

Elemental compositions of the oxides were measured as a function of depth by x-ray photoelectron spectroscopy (XPS) with argon ion sputtering using a K-Alpha XPS from Thermo Scientific. The K-Alpha XPS uses monochromatic Al k-alpha x-rays to generate photoelectrons that pass through a double-focusing hemispherical electron energy analyzer onto a 128-channel detector. Depth profiling was carried out using 3 KV Ar-ions and set to a known sputtering rate for SiO_2, which is 6nm/min, as calibrated on a SiO_2 standard.

The thickness and refractive index of the TiO_2 films was measured using a spectroscopic ellipsometry (alpha-SE model from J.A.Woollam Co. Inc.) at three incident angles, 65°, 70°, and 75°. The spectral range of the ellipsometry was from 380-900nm (1.3-3.25eV), and measured data were fitted with the Cauchy layer model[14] to determine the thickness of the ALD films.

The structure of the thin films was characterized by x-ray diffraction (XRD, PANalytical X'Pert Pro MPD) using a Cu-Kα radiation source. Measurements were taken over the range of 5-80° with a step size 0.0167° and a count time of 2 seconds. To avoid the high intensity peak of the Si (100) substrate, the samples were offset by 2° in omega.

C-V measurements were taken on the TiO_2/Si MOS capacitors using a Keithley 4200 semiconductor characterization system operating at 1 MHz at room temperature. To evaluate charge trapping in the oxide layers from the hysteresis behavior of the oxide, the bias was applied by sweeping the dc voltage back and forth between +10V and -10V at a sweep rate of

0.1V/sec. The same results were obtained regardless of the sweep direction. The interface trap density, D_{it}, (at the oxide-dielectric interface) was determined by the ac conductance method[15] using an HP 4284A precision LCR meter, and conductance was measured from 20Hz to 1MHz with a long integration time at room temperature. The I-V measurements were taken by sweeping the voltage from +4V to -4V, and leakage current densities of each sample were compared at -2V gate bias voltage.

Results and Discussion

The surface of the TiO_2 film deposited at 200°C was the most uniform, as it had the highest density of nucleation sites as determined by AFM. The next most uniform samples were those prepared at 250 and 300°C (Fig. 5.1). By contrast, random, isolated islands formed at 150°C and 100°C, indicating a lower nucleation density at lower temperatures. The root mean square (RMS) surface roughness decreased with the growth temperature. Lee *et al.*[16] reported a similar trend for TiO_2 grown on amorphous Si by metal-organic chemical vapor deposition (MOCVD).

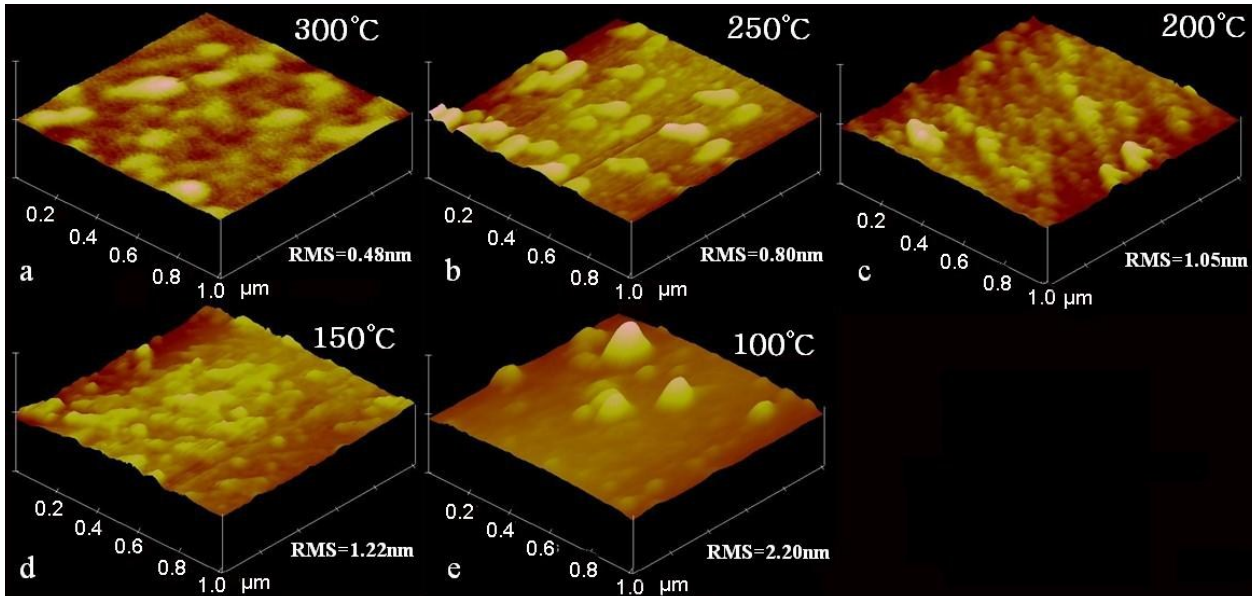
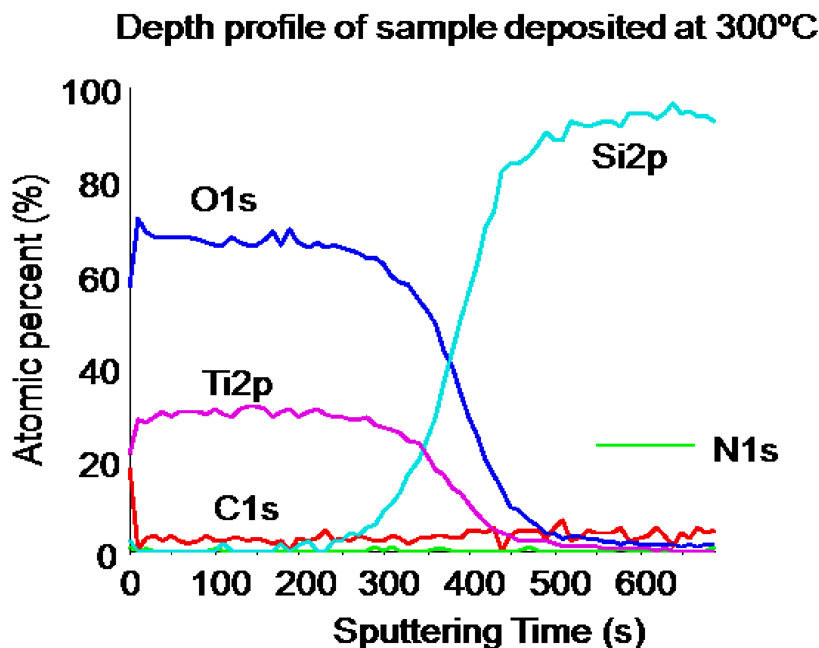
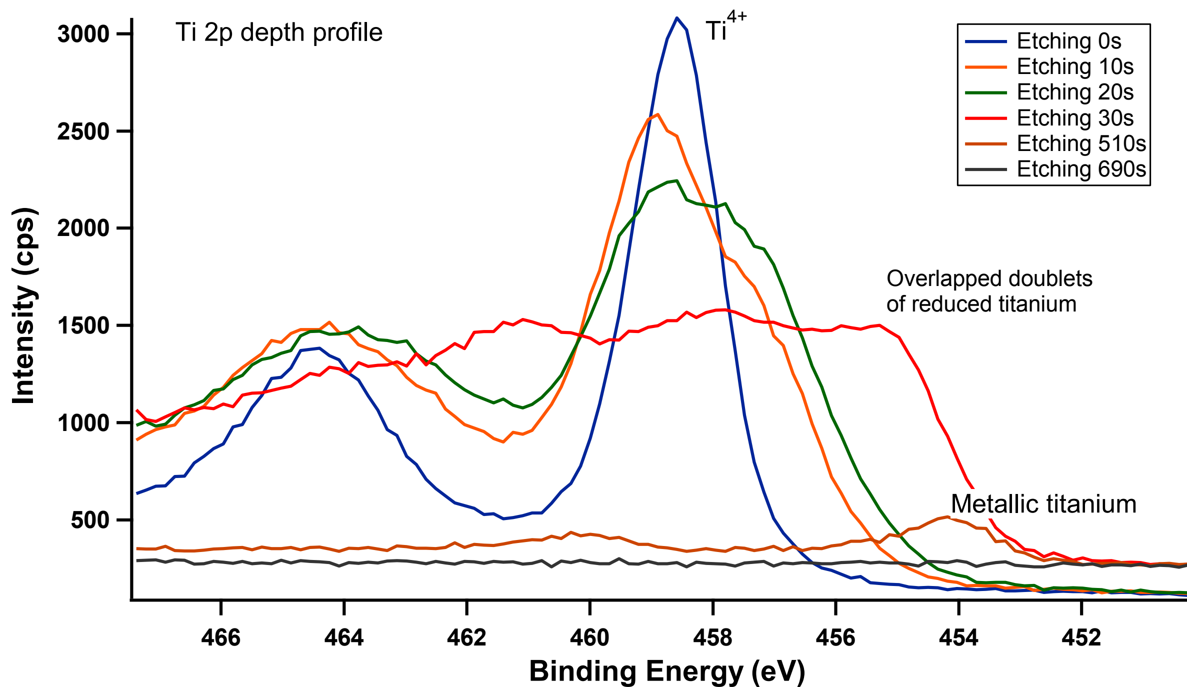


Figure 5.1 Three-dimensional AFM images of TiO_2 on Si deposited at different ALD temperatures. The Z height is 30nm for all images. (a) 300°C (RMS=0.48 nm), (b) 250°C (RMS=0.80 nm), (c) 200°C (RMS=1.05 nm), (d) 150°C (RMS=1.22 nm), and (e) 100°C (RMS=2.202 nm).

On all TiO_2 sample surfaces, nitrogen was detected by XPS. However, it disappeared after sputtering for 30 seconds, suggesting it was solely surface contamination. At the interface, silicon oxide was also observed. The average ratio of oxygen and titanium was calculated (Table 1) in the steady region in depth profile (Fig. 5.2a). The sample deposited at 200ºC had the O/Ti stoichiometry closest to 2/1 of TiO_2 followed by the 100 and 150ºC samples. 250 and 300ºC deposition temperatures lead to oxygen-rich titanium oxide films. The signal from the Ti 2p transition was also monitored in the depth profile (Fig. 5.2b). A single doublet, suggesting the presence of metallic titanium, was present at the oxide/Si interface for all samples, then disappeared away from the interface into the film. The observation of metallic titanium could be from the reduction during Ar^+ sputtering. Carbon was detected throughout the oxide films. Figure 5.3 plots the average carbon concentration in the oxide layers as a function of the ALD deposition temperature. The minimum carbon concentration (2.6 %) occurred at 200 °C (Table 5.1).



a)



b)

Figure 5.2 (a) XPS depth profile of sample deposited at 300°C. (The shape of the depth profiles is similar for all the samples. Only one is demonstrated.) (b) XPS depth profile of Ti2p at different sputtering times. The 2p3 of Ti^{4+} and metallic Ti peaks are 458.5eV at 0 seconds and 454.2eV at 510 seconds.

The TiO_2 thickness was similar for all samples, 19±1.2nm (Table 5.1), as measured by ellipsometry. However, the time to sputter through the oxide layers increased with increasing deposition temperature (Fig.5.3). This suggests that the oxide film increased in density and was more resistant to sputtering as the deposition temperature was increased.[17] The TiO_2 films were amorphous, since no TiO_2 crystalline peaks were detected by x-ray diffraction.

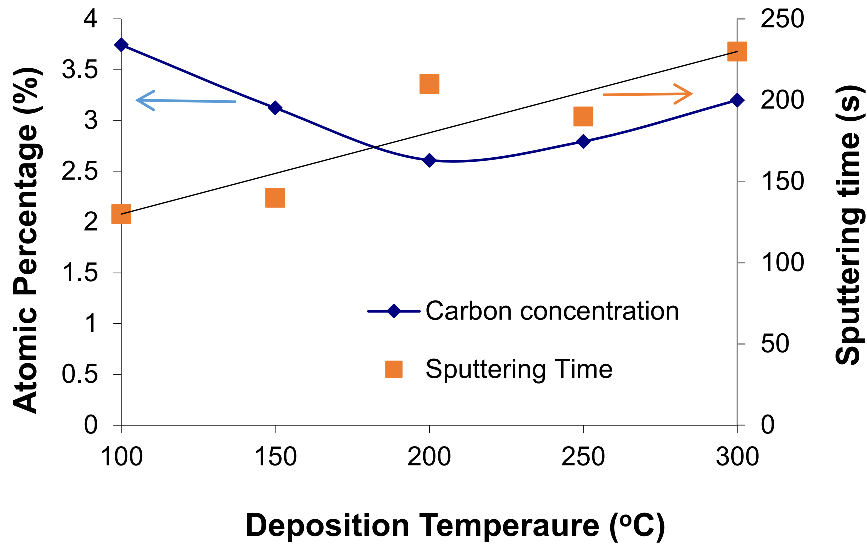


Figure 5.3 (Left axis) Average atomic carbon concentration in the TiO_2 layers versus ALD temperature. (Right axis) Sputtering time to remove the oxide layer and expose the Si substrate versus ALD deposition temperature.

The dielectric constant was calculated using the relationship $C = \varepsilon_r \varepsilon_0 {}^{A}/_{d}$, where C is the capacitance of the material, ε_r is dielectric constant, ε_0 is permittivity of free space and d is layer thickness. The TiO_2 and SiO_2 thin films were treated as capacitors in series, and it was assumed that the ε_r and thickness of SiO_2 are 3.9 and 1.9nm respectively. The dielectric constant of TiO_2 (Table 1) was calculated from C-V plots using the equation:

$$\frac{1}{C_m} = \frac{1}{C_{TiO_2}} + \frac{1}{C_{SiO_2}} \qquad (1)$$

where C_m is the measured capacitance in the accumulation region. A wide range of ε_r for amorphous TiO_2 [ε_r =16-86] has been reported,[18, 19] and our values [ε_r =29-56] were similar to those reported by Alexandrov *et al.*[18]

Table 5.1 Oxygen and titanium ratio, average carbon concentration, thickness, dielectric constant of TiO_2 and calculated values of D_{it} for TiO_2/Si samples prepared at different ALD temperatures.

ALD temperature (°C)	O:Ti Ratio	Average C concentration (%)	TiO_2 thickness (nm)	Dielectric constant	D_{it} (1×10^{13} $eV^{-1}cm^{-2}$)
300	2.24	3.20	19.7	29.6	1.7-4.0
250	2.32	2.79	19.0	42.5	3.8-4.7
200	2.08	2.61	19.2	55.6	1.1-1.5
150	2.12	3.12	17.9	47.1	2.5-3.9
100	2.10	3.74	19.3	41.3	1.5-2.2

All TiO_2/Si samples had negligible hysteresis, similar to the observations of Fuyuki *et al.*[19] for TiO_2 grown on Si by chemical vapor deposition (CVD) between 200 and 400°C. For the 200°C sample, the oxide saturation capacitance (C_{ox}) was observed and the transition from accumulation to depletion region was sharp compared to the rest of the curves (Fig.4), which is indicative of having a better interface quality. At 250 and 300°C, a bump at approximately 1.0 V is seen in the C-V plot, due to drift in mobile charge.[20] At different bias voltages, the samples deposited at 100, 150 and 300°C did not show saturation of oxide capacitance (C_{ox}). An explanation of this phenomenon will require further examination.

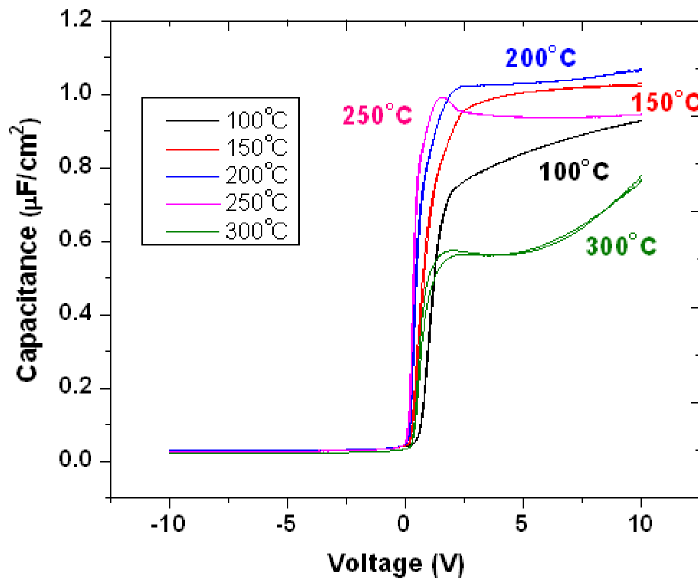


Figure 5.4 C-V measurement for TiO_2/Si MOS capacitors at different ALD temperatures

To calculate D_{it} as a function of energy in the bandgap of Si, the series resistance and interface state conductance $G_P(\omega)$ were extracted as a function of angular frequency at a fixed voltage within the depletion region using an ac equivalent parallel circuit model as shown in Figure 5.5a. The parallel conductance (G_P) represents an energy loss due to interface traps and is a function of measured capacitance (C_m), angular frequency (ω), series resistance (R_s), measured conductance (G_m) and oxide capacitance (C_{ox}). Capacitance and conductance data were corrected due to inclusion of series resistance. The series resistance was calculated using the relation[15]

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \qquad (2)$$

Here G_{ma} and C_{ma} are the measured conductance and capacitance in the strong accumulation region respectively. Calculated values of R_s are similar to previously published results (i.e. 2000-2500Ω) by Pakma *et al.*[21] Corrected capacitance, C_c, and corrected equivalent parallel conductance, G_c, are given by[15]

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2} \qquad (3)$$

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2} \qquad (4)$$

where a is given by

$$a = G_m - (G_m + \omega^2 C_m^2)R_s \qquad (5)$$

G_P can be expressed after inclusion of corrected conductance and capacitance as

$$G_p = \frac{\omega^2 C_{ox}^2 G_c}{G_c^2 + \omega^2 (C_{ox} - C_c)^2} \qquad (6)$$

The characteristic trap response time (τ=2π/ω) is expressed by the Shockley-Read-Hall statistics of capture and emission rates by the following equation:[22]

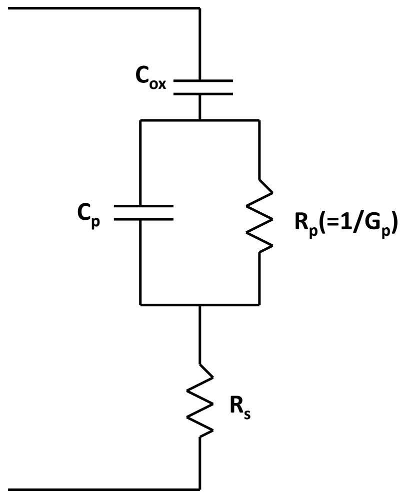
$$\tau = \frac{\exp[\frac{\Delta E}{k_B T}]}{\sigma v_{th} D_{dos}} \qquad (7)$$

where ΔE is the energy difference between the majority carrier band edge energy (E_{CB}) and the trap level E_T, k_B is the Boltzmann constant, v_{th} is the average thermal velocity of the majority charge carriers ($v_{th} = \sqrt{(3k_B T/m^*)}$ =2.68×10^7 cm/s), D_{dos} is the effective density of states of

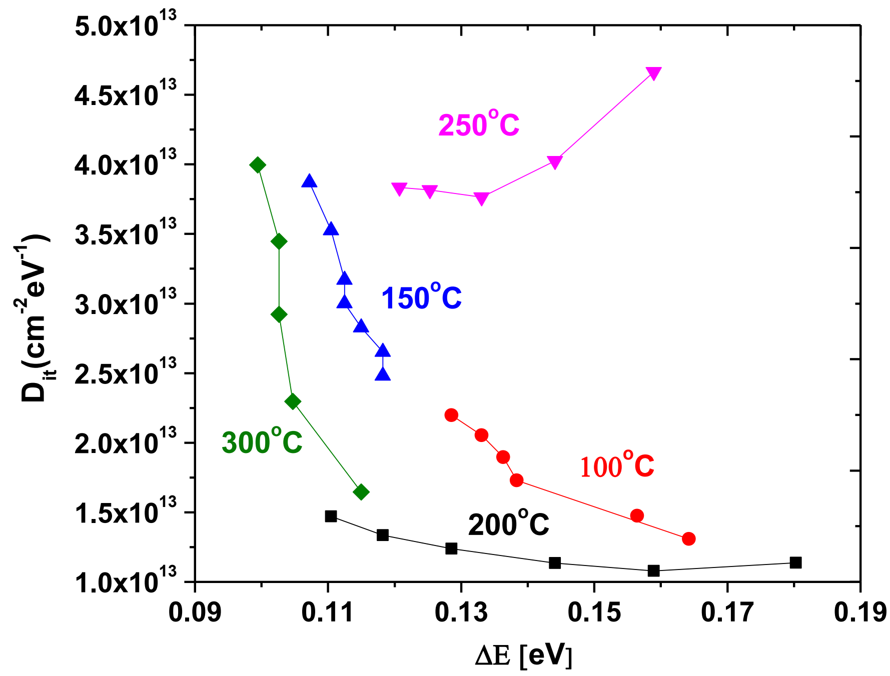
the majority carriers ($D_{dos} = 2(2\pi m^* k_B T/h^2)^{3/2} = 2.07\times10^{18}$ cm^{-3}), and T is the temperature. σ is the capture cross section of the trap (1×10^{-16} cm^{-2})[23], which is assumed to be constant due to the dominance of the exponential term of Equation 7.Errors in the capture cross section by three orders of magnitude only made 0.18eV energy difference within the bandgap of the semiconductor.[24] The trap level can be identified as the energy position from the frequency at which G_p/ω is maximum. Also, based on the maximum conductance from the measurement, an approximate equation to calculate interface trap density is given by:[25]

$$D_{it} = \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{max} \qquad (8)$$

where A is the capacitor area. The calculated values of interface trap density are on the order of 10^{13} $eV^{-1}cm^{-2}$ (Table 5.1) and are distributed between 0.09eV to 0.18 eV energy range from the conduction band edge of the Si bandgap. They were similar to the results of Kumar et al.[26] in which a single value $D_{it}=1.2\times10^{13}$ $eV^{-1}cm^{-2}$ was reported. The D_{it} distribution of the 200°C ALD sample is lower than that of the rest of samples (Fig. 5.4 b). Results also show that $qD_{it}>Cox$. In this case the conductance method becomes insensitive to the trap density and D_{it}, and it could be overestimated by an order of magnitude.[27] Figure 6 shows that the capacitance of the sample deposited under 200°C increases in the accumulation region when the frequency is decreased due to the effect of series resistance and localized interface states at the Si/TiO_2 interface.[21] Similarly, the capacitance also increases in the depletion region with decreasing frequency due to recombination and generation from the interface states.[28] This frequency dispersion in C-V characteristics is negligible in the inversion region.



a)



b)

Figure 5.5 (a) Simplified circuit of MOS capacitor including series resistance. (b) Interface trap density distributions of ALD samples at different deposition temperatures.

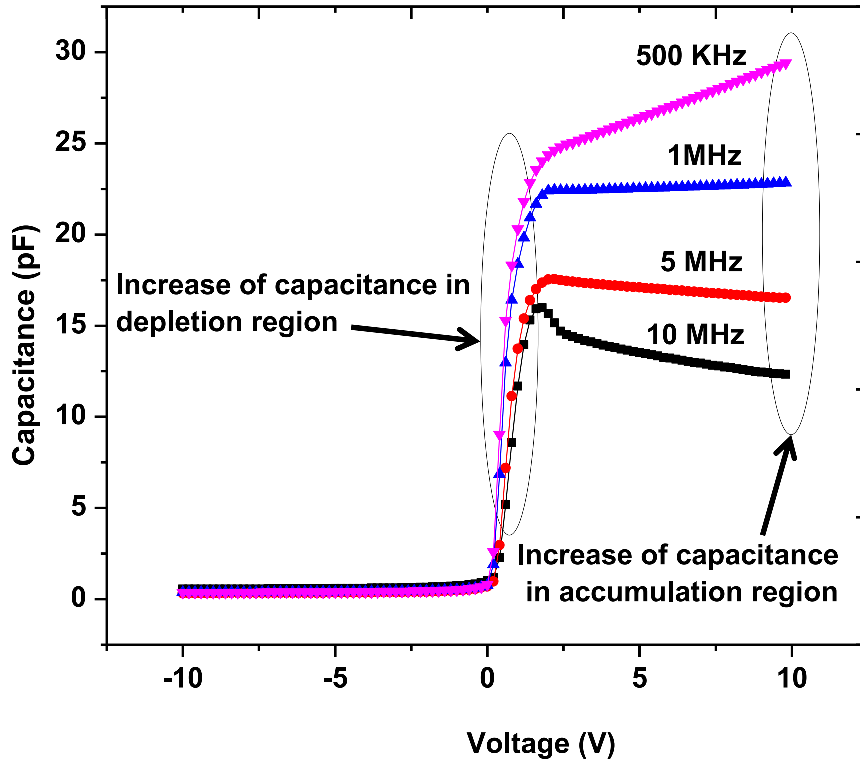


Figure 5.6 Measured capacitance vs gate voltage as a function of frequency for the TiO_2/Si at 200°C deposition temperature.

Figure 5.7 shows the current-voltage characteristics under positive and negative biases at room temperature for samples prepared at different ALD temperatures. The plots in Figure 5.7 (semi-logarithmic scale) are linear at low gate bias voltages, but deviate from linearity at high voltages, which is attributed to the series resistance effect on the TiO_2 film.[21] The leakage current densities were on the order of 10^{-5}~10^{-4} A/cm^2 at -2V, which is 2 orders of magnitude lower than that of the reactive sputtered TiO_2 film [58nm] reported by Albertin *et al*.[29] and CVD grown TiO_2 film [20nm] reported by Bae *et al*.[30]

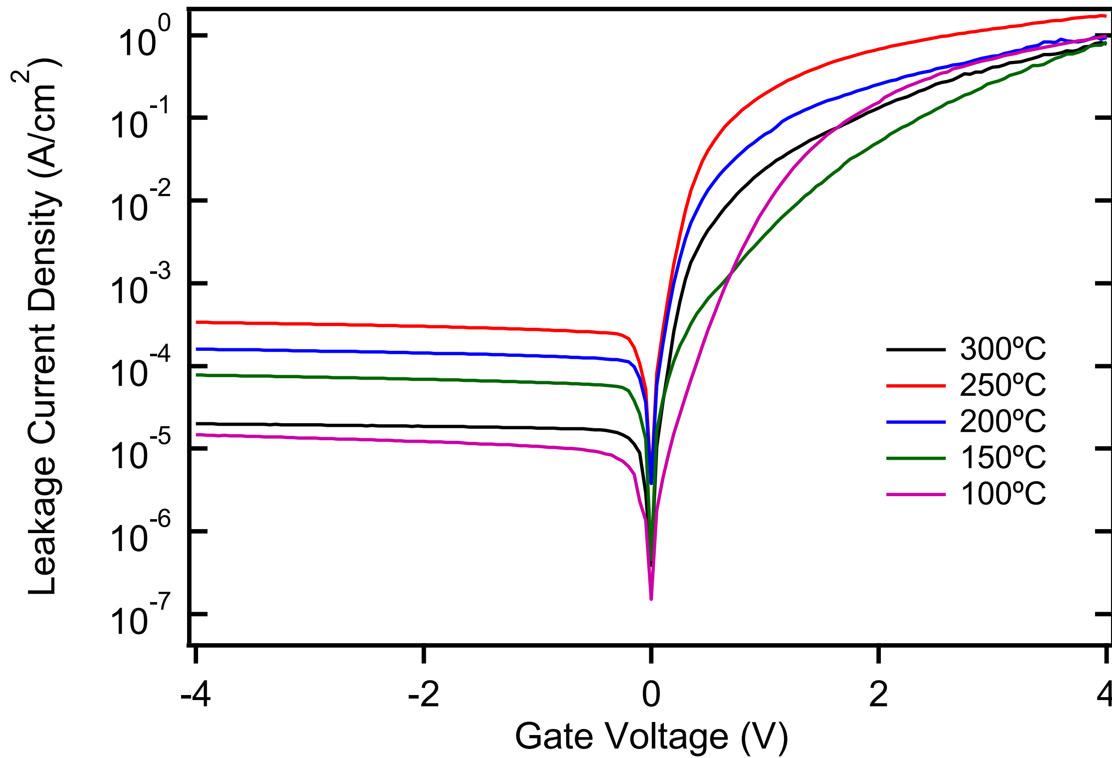


Figure 5.7 I–V characteristics of TiO_2/Si MOS capacitor at different ALD temperatures.

Conclusion

In this work, the influence of substrate temperature during plasma-assisted ALD on surface morphology, stoichiometry, impurity concentration and electrical properties of TiO_2/Si MOS capacitors is reported. Both surface morphology and roughness of the oxide layer were affected by the growth temperature. The impurity concentration at the oxide-silicon interface varied randomly with temperature. The TiO_2 dielectric constants are between 29 and 56, as obtained from C-V measurement, but the hysteresis in C-V plot did not change with temperature. The current density improved by two orders of magnitude compared to previous studies. Comparing the results of the TiO_2 film with different ALD temperatures, the optimal deposition temperature of TiO_2 is 200°C as this produces the highest dielectric constant, most uniform coverage and stoichiometry. This ALD temperature also has the lowest impurity concentration and lowest D_{it} at the interface, indicating a better quality sample. These results confirm that TiO_2 is a promising high k material for silicon devices.

Acknowledgements

We are grateful for the support for this project from the Office of Naval Research, grant N00014-09-1-1160, Paul Maki, program manager. XPS and XRD were conducted through the Oak Ridge National Laboratory's High Temperature Materials Laboratory User Program, sponsored by the U. S. Department of Energy, Office of Energy Efficiency and Renewable Energy, Vehicle Technologies Program. Work at the U.S. Naval Research Laboratory is supported by the Office of Naval Research.

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Chapter 6 - Effects of surface pretreatments on N-polar GaN for atomic layer deposition of Al_2O_3

Abstract

A systematic study of the effect of surface pretreatments on N-polar GaN for atomic layer deposition of ALD is reported. 14-20 nm Al_2O_3 was deposited on bulk n-type GaN pretreated with 30 min, 5 min pre-etching+epitaxy; 800 and 850°C thermal oxidation, HF (HF:H_2O=1:1); HCl (HCl:H_2O=1:1); base piranha (H_2O:NH_4OH:H_2O_2=3:1:1); H_2 plasma and no pretreatment for comparison. Subsequently, the device was fabricated into metal oxide semiconductor capacitors (MOSCAPs) and characterized by atomic force microscopy (AFM), capacitance-voltage (C-V) and current voltage (I-V) measurement. The surface morphology and electrical performance was greatly affected by different pretreatments due to the reactive nature of N-polar GaN. Al_2O_3 deposited on the non-pretreated sample displayed the best performance with the smallest hysteresis (0.03V), lowest leakage current density (2.09 x 10^{-8} A/cm^2) and total trap density (2.47 x 10^{10} cm^{-2}eV^{-1}) correlating to the smoothest surface morphology (0.23 nm).

Introduction

Gallium nitride (GaN) based materials are of great interest not only for optoelectronic devices such as blue LEDs,[1] laser diodes,[2] and UV detectors but also for electronic devices operating under high frequency, temperature and power with high efficiency. After years of study, Ga-polar GaN based high electron mobility transistors (HEMTs) have demonstrated great performance with high RF output power.[3,4] As the maximum frequency increases by scaling down the GaN HEMT dimensions to reduce electron transit time, the contact resistance and capacitive elements need to be well controlled to prevent device delay times and to ensure the frequency performance of the device.[5] N-polar GaN has the advantage over Ga-polar for high-frequency applications such as the potential to achieve very low contact resistance and a natural back barrier to improve electron confinement.[6–8] An extremely low contact resistance of 23 Ω-μm was reported by Mishra *et al*.[9] However, to date most of the N-polar GaN HEMT devices nowadays adapt the structure with a Schottky barrier as the gate contact.[6,10,11] For better performance a metal-oxide-semiconductor structure is desirable as it provides a higher input impedance, larger gate voltage swings and lower gate leakage current.[12]

Al_2O_3 has become a suitable gate dielectric for III-nitride based device due to its large band gap, relatively high dielectric constant and high thermal stability.[13–17] To grow Al_2O_3 on the highly scaled-down device feature, a precise thickness control of the growth film is necessary to maintain the aspect ratio between the gate length and oxide thickness for the frequency performance. This can be realized by atomic layer deposition (ALD).[18] But the initial condition of the substrate surface is crucial for the nucleation of oxide layer and could subsequently affect the surface morphology. A surface treatment prior to ALD might be beneficial to deposit high quality oxide film, and multiple studies have been conducted on the Ga-polar GaN surface pretreatment.[19–25] However, there are no published studies reporting the effects of different pretreatments on N-polar GaN.

In this work, a series of pretreatments before ALD Al_2O_3 were conducted on N-polar GaN. Metal-oxide-semiconductor capacitors (MOSCAPs) were fabricated to investigate the electrical properties. The electrical results were also compared with respect of different pretreatment and correlated with the surface morphology of the ALD oxide. An optimal processing condition was determined.

Experimental procedures

MOS capacitor fabrication

The single crystals used in this study were bulk *n*-type (1×10^{18} cm^{-3}) GaN wafers grown by HVPE, with a thickness of ~400μm and diced into 10×10 mm^2 chips after growth. Chemical mechanical polishing (CMP) was applied on Ga-polar (0001) and N-polar ($000\bar{1}$) GaN to achieve a smooth surface of less than 1nm root mean square (RMS) roughness. Chips were treated individually with different cleaning methods before ALD. Based on the purpose of cleaning, the methods of pretreatment could be divided into three groups: (1) Pre-epitaxy to remove the CMP defects; (2) Thermal oxidation to reduce interface defects; and (3) Chemical cleaning to remove carbon absorbed from the air and to improve the nucleation of the ALD oxide layer.

In Group one, to remove the sub-surface damage caused by CMP, N-polar GaN chips were etched by ramping to 1050°C in a metal organic chemical vapor deposition chamber under an ammonia condition. Specifically, this was accomplished at 70 Torr with 2 slm of ammonia. Two chips were then kept at 1050°C under these conditions for 30 and 5 min, respectively. Then samples were cooled to room temperature while continuing to flow ammonia. To regrow polish damage free GaN, 100nm-thick GaN was deposited by MOCVD using trimethyl gallium (TMG) and ammonia as precursors at a growth temperature of 1050°C, a pressure of 150 Torr, and with a V/III ratio of 2200.

In Group two, thermal oxidation was performed on two GaN chips under 800 and 850°C respectively to grow a thin layer of Ga_2O_3. The temperature of oxidation was 30 minutes and the O_2 flow rate was 120 sccm for both chips.

In Group three, surface pretreatments studied included: [1] etching HCl (H_2O:HCl=1:1) at room temperature for 1min; [2] HF (H_2O:HF=1:1) at room temperature for 1min; [3] Base piranha (H_2O:NH_4OH: H_2O_2=3:1:1) at 80°C for 10 min [4] treating in a H_2 plasma with forward power of 400W for 10 min; [5] A sample without any surface pretreatment was also included in this set for comparison. After surface pretreatment, Al_2O_3 was deposited on the surface of N-polar GaN by ALD at 150°C in an Oxford FlexAL Plasma Atomic Layer Deposition System. Each cycle of Al_2O_3 included a 30 ms TMA dose followed by 1500 ms Ar purge; and 2000ms O_2

plasma dose followed by 800 ms post plasma. This yields a growth rate of 1.35Å per cycle, and a total 112 cycles were conducted.

To pattern the circular MOSCAPs (Fig 6.1), primer P20 and negative photoresists NFR were spin coated at 3000RPM for 45 sec followed by 3 sec UV light exposure in Quintel Contact Lithography Tool. Before metal deposition, the samples were loaded into Oxford Plasmalab 100 RIE/ICP Etcher to descum the photoresist for 30 sec to further clean the sample surface and to improve the adhesion of the metal contact. A Ni/Au (20/50 nm) alloy was evaporated on the chip and subsequently liftoff in acetone.

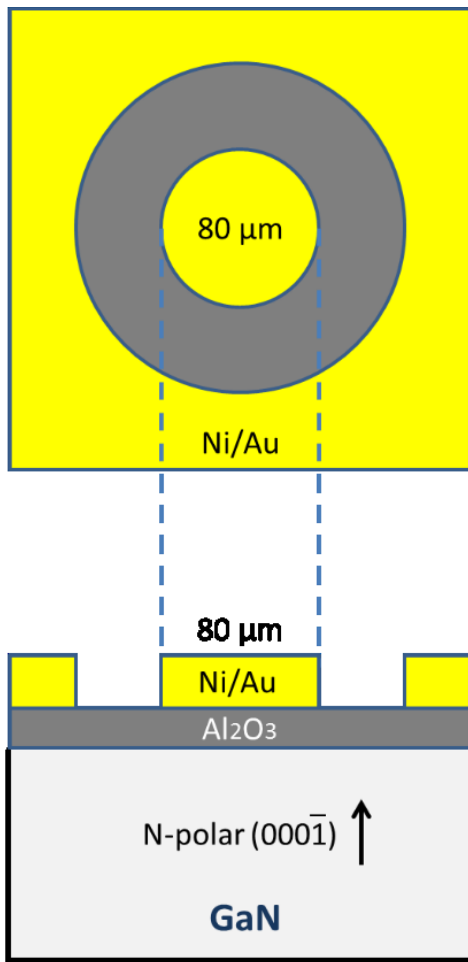

Figure 6.1 Schematic illustration of the N-polar GaN MOS capacitor with a top view (upper) and a side view (lower).

High-k film and device characterization

Atomic force microscopy (AFM, Digital Instrument MultiMode SPM from Veeco Instruments Inc.) was used to inspect surface morphology changes caused by the surface

pretreatments. The thickness and refractive index of ALD Al_2O_3 was measured using a spectroscopic ellipsometry (JA Wollam M-2000U) on silicon witness sample, and the thickness of photoresist was monitored by Veeco Optical Profilometer. C-V measurements were taken on the Al_2O_3/GaN MOS capacitors using a Keithley 4200 semiconductor characterization system operating at 1 MHz at room temperature. To evaluate charge trapping in the oxide layers from the hysteresis behavior of the oxide, the gate was biased in the accumulation region for 2 sec and then swept back and forth from the accumulation to the depletion regions (A to D), and from depletion to the accumulation region (D to A) with a sweep rate lower than 0.1V/sec to let the interface traps further react with the bias voltage. I-V measurements were taken by sweeping the voltage from +4V to -4V, and leakage current densities of each sample were compared at +4V gate bias voltage.

Results and discussion

Transformation of surface morphology by AFM Observation

Comparing surface morphology of the sample before and after 30 min ammonia etching (Fig. 6.2a, b), the surface roughness of N-polar GaN increased by a factor of 3 (from 0.54 to 1.94 nm). The vertical distance of the bumps on the etched sample were about 5 nm, which is similar to the sample before annealing, but the density of the bumps greatly increased. Surface roughness of the sample etched for 5 min was not decreased due to a partial etching on the surface as shown in Fig. 6.2c) in which the upper part of the surface (area X in Fig. 6.2c) is relatively smooth (not etched) while the lower part (area Y in Fig. 6.2c) was attacked by the etchant. The height difference of the unreacted surface and etched trench was larger than that of a uniformly etched surface where the height difference of a lightly etched bump and heavily etched trench was small. This suggested 5 min etching was in the transition stage, which also explained why a higher roughness was observed for 5 min etched sample than 30 min etched sample.

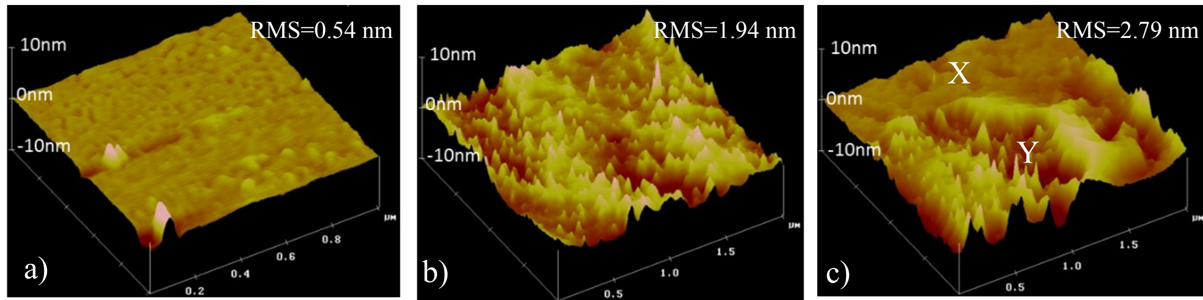

Figure 6.2 Three dimensional AFM pictures of the N-polar GaN surface morphologies of sample with a) no etching b) 30 min etching c) 5 min etching. The examined area was 1 x 1 μm^2 for the not etched sample and 2 x 2 μm^2 for two etched samples all with the Z-height of 20nm. The RMS roughness of surfaces were 0.54, 1.94 and 2.79 nm respectively.

To achieve a uniform surface with a lower roughness, 100nm N-polar GaN was deposited by MOCVD. After this epitaxial growth of thin GaN on the pre-etched surface, the roughness prominently decreased, and the surface features were significantly altered for both the 5-min and 30-min etched samples (Fig. 6.3). The bumps and trenches were uniformly covered by the epitaxial layer. This great change indicated that the nature of reactive N-polar could be very responsive to the epitaxy and quickly covered the rough areas produced by etching.

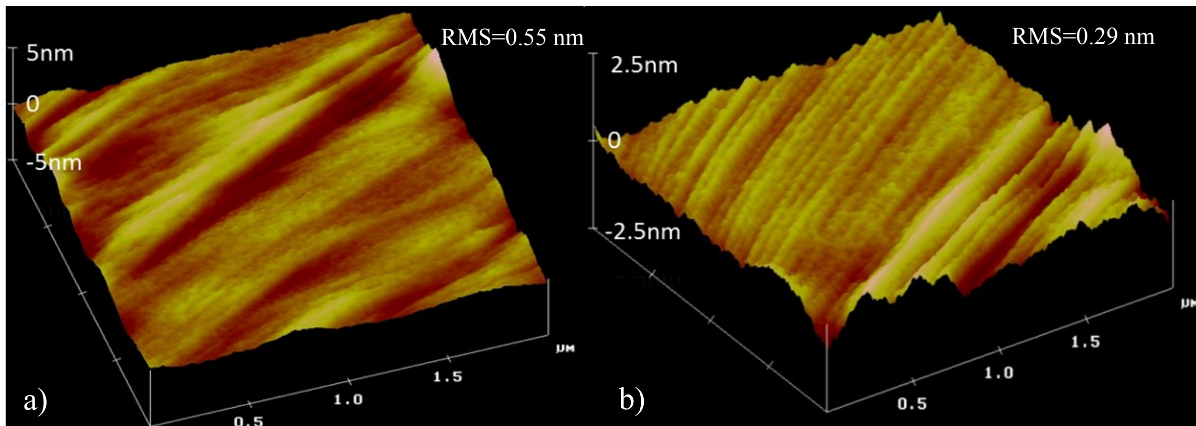

Figure 6.3 Three dimensional AFM picture of a) 30 min etched sample; b) 5 min etched sample after epitaxial growth of 100nm GaN.

After thermal oxidation at 800°C, bumps about 1.5 nm high formed on the N-polar surface (Fig. 6.4b) while bumps less than 0.5 nm were formed on the Ga-polar (not shown), which proved the N-polar surface was more reactive than the Ga-polar. The newly formed bumps increased the surface roughness from 0.14 to 0.51 nm on the N-polar surface. The surface morphology of the sample oxidized under 850°C was more aggressively roughen; higher bumps

around 5.5nm were formed. A possible explanation to this phenomena is that preferential oxidation happened at the dislocations on GaN to form the bumps;[26] plus relatively larger flow rate of oxygen at top of the bump enables a vertical growth of higher bumps while the bumps near the surface formed slower, leading to a non-uniformity of surface feature. This could be detrimental for electrical performance of the device, so ALD Al_2O_3 was not performed on the 850°C sample.

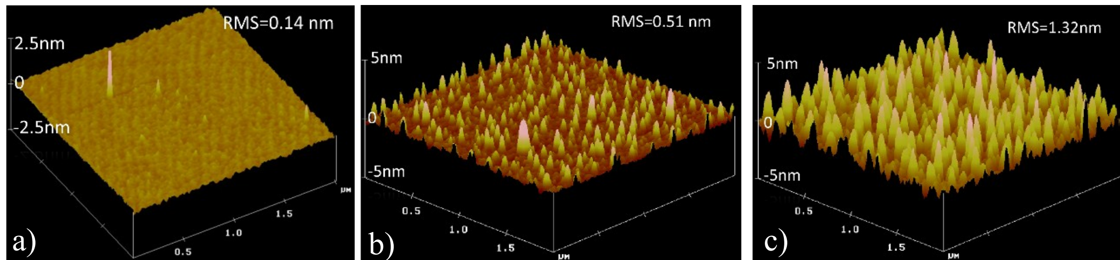

Figure 6.4 Three dimensional AFM pictures of sample (a) before oxidation, (b) oxidized at 800°C and (c) oxidized at 850°C

For the samples in group one and two, after Al_2O_3 deposition, the surface morphology was not dramatically changed under the AFM (not shown). For most samples, the surface roughness was slightly increased except for the sample etched for 30 min, which had a lower roughness (listed in Table 6.1). A possible reason for smaller roughness number was that the deposited thin Al_2O_3 on both sides of the trenches decreased the height difference of the gap.

Figure 6.5 showed morphology changes before and after surface pretreatment in group three. Fig. 6.5a is an AFM image representing the N-polar surface of all five samples prior to ALD Al_2O_3 due to the similarity of morphology before the pretreatment. Figure 6.5 also showed the AFM results of Al_2O_3 deposited at 150°C on N-polar GaN pretreated with (b) HCl, (c) HF, (d) base piranha, (e) H_2 plasma and (f) no pretreatment. The Al_2O_3 deposited on HF and H_2 plasma pretreated samples were smooth as well as the non-pretreated samples. ~20 nm bumps were observed on the HCl pretreated sample, and over 50 nm deep trenches were found on base piranha samples which indicated that HCl and base piranha pretreatments were very aggressive for the reactive N-polar GaN surface. Specifically, after piranha treatment, the bulk transparent GaN chip was visually cloudy on the N-polar surface, and this rough surface features could lead to high interface trap density and could be detrimental for the device performance.

Table 6.1 Surface roughness of N-polar GaN before and after ALD of Al_2O_3

Group number	RMS roughness before surface treatment (nm)	Surface pretreatment	RMS roughness after etching (nm)	RMS after pretreatment (nm)	RMS roughness after ALD (nm)
1	0.69	30 min Etching+epitaxy [a]	1.94	0.55	0.3
	0.52	5 min Etching+epitaxy [a]	2.79	0.29	0.5
2	0.14	800°C thermal oxidation [a]	NA	0.51	0.56
	0.18	850°C thermal oxidation [b]	NA	1.32	1.41
3	0.34	HCl [c]	NA	NA	4.73
	0.31	HF [c]	NA	NA	0.33
	0.26	Base Piranha [c]	NA	NA	26.51
	0.3	H_2 Plasma [c]	NA	NA	0.37
	0.27	No pretreatment [c]	NA	NA	0.23

[a] ALD of 20 nm thick Al_2O_3. [b] No ALD. [c] ALD of 14nm thick Al_2O_3.

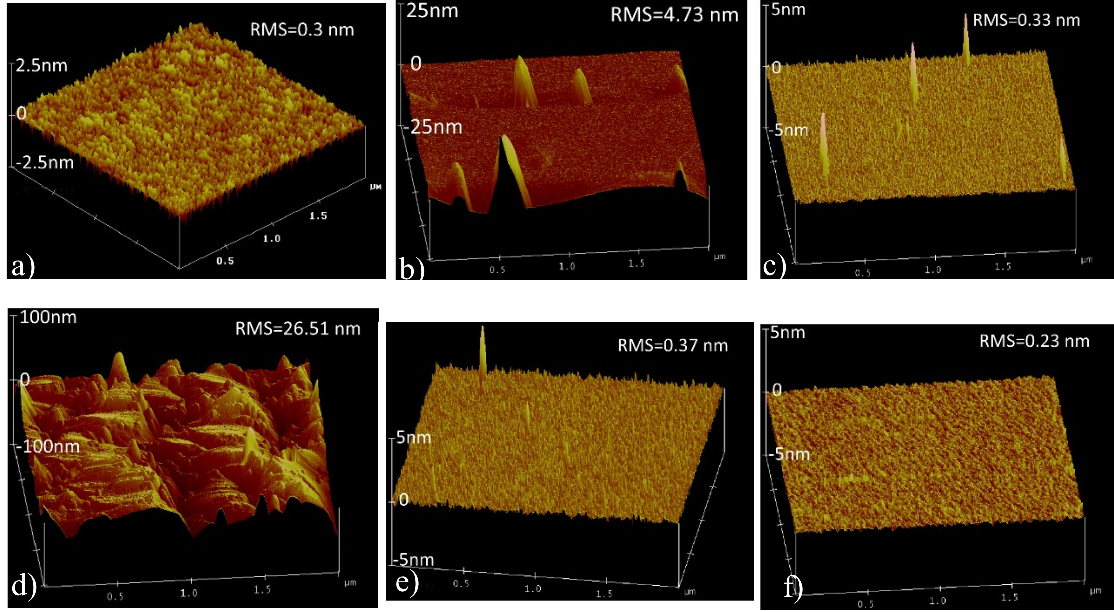

Figure 6.5 Three dimensional AFM images of N-polar GaN a) before ALD and after ALD pretreated with b) HCl, c) HF, d) Base piranha, e) H_2 plasma, f) No pretreatment

C-V and I-V measurements for Al_2O_3 on GaN MOSCAPs

In this section, the MOSCAPs are named according to their respective surface pretreatment method. The hysteresis of all the samples is presented in Figure 6.6 and calculated from the voltage difference (ΔV_{FB}) at the flat-band capacitance (C_{FB}) at each pair of sweeps[27]

$$C_{FB} = \frac{C_{ox}\varepsilon_0\varepsilon_s A/\lambda}{\varepsilon_0\varepsilon_s A/\lambda + C_{ox}}$$

where C_{ox} is the oxide capacitance assumed to be the accumalation capacitance; ε_0 is the vacuum permitivity; ε_s is the dielectric constant of GaN (ε_s=8.9); A is the area under the gate contact; and λ is the Debye length calculated from[27]

$$\lambda = \sqrt{\varepsilon_s kT/q^2 N_D}$$

where k is the Boltzmann constant, and N_D is the doping concentration ($N_D=1\times10^{18}cm^{-3}$). A rough estimation of average density of interface traps and oxide traps (Q_T) was perform using the hysteresis and C_{ox} as

$$Q_T = \frac{C_{ox}\Delta V_{FB}}{E_{BG}}$$

as E_{BG} is the band gap of GaN (E_{BG} =3.4 eV). The dielectric constant of the ALD Al_2O_3 was also determined by

$$\varepsilon_{ox} = \frac{C_{ox} d}{\varepsilon_0 A}$$

where d is the thickness of Al_2O_3 determined on silicon wittness samples, and the thickness of SiO_2 was subtracted from the result. The calculated results are listed in Table 6.2.

Because the deposited oxide thickness was the same for the samples in group 1 and 2, their hysteresis was compared as parallel. The smallest hysteresis was for the 30 min etched sample, which leads to the lowest total trapped charge density. The 5 min etched sample had the second lowest total trap density followed by the 800°C oxidation sample. This correlated well with the trend of surface roughness; specifically smoother surface leading to lower trap densities.

The same trend was found for samples in group three where the sample with no pretreatment had the lowest surface roughness, and the lowest trap density of 2.47×10^{10} cm^{-2} eV^{-1} among all the reported samples. In contrast, a rough surface could destroy a device. For example, the piranha etch had the roughest surface on which the metal/ Al_2O_3 stack failed to exhibit MOSCAP behavior but the Schottky behavior at positive gate bias (Fig. 6.6). The capacitance should have reach a saturated value rather than exponentially increasing with an unreasonable large value.

Besides surface morphology, hysteresis could also be affected by the crystalline quality of the GaN substrate. As the roughness of HF etched and H_2 plasma treated sample were similar, the hysteresis of H_2 plasma is almost 6 times higher than that of HF. The high energetic H_2 plasma could be effective to remove absorbed carbon and hydroxides on the surface. Meanwhile, it could also genertate defect such as vaccancies and intersitials among GaN crystal array especially with the reactive N-polar surface and eventually form interface traps.

So the origin of hysteresis could be explained as a conbination effects of the interface states of Al_2O_3/GaN and oxide traps in the ALD Al_2O_3.[28,29] The interface states distributes within the band gap of GaN and electrons could be captured by these states when the voltage is changed. However, those electrons captured in the deep-lying states (further away from the conduction band) cannot emit to the conduction band at room temperature due to an exponentially increasing emmission time constant and form negative fixed charges.[30] So if a deep-lying state is empty before the forward sweep (A to D) and filled after the forward sweep, it is unlikely to be emptied during the following backward sweep (D to A), which contributes to part of the hysteresis of the CV.

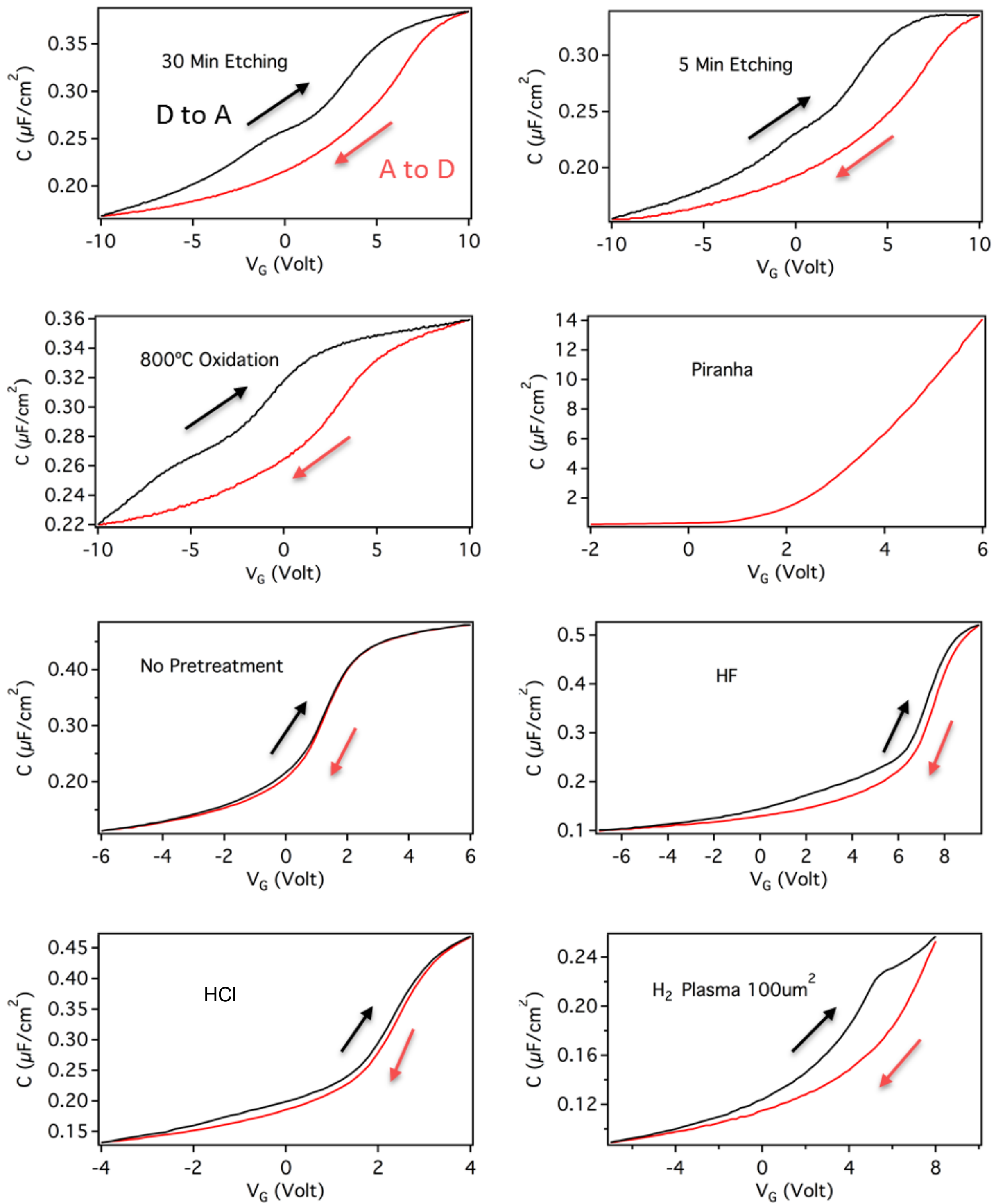

Figure 6.6 C-V sweeps from accumulation to depletion (red) and from depletion to accumulation (black) for samples with different pretreatment methods.

Table 6.2 Summary of electrical properties of ALD Al_2O_3 on N-polar GaN with different pretreatments.

Group Number	Surface pretreatment	C_{ox} (μF/cm^2)	ε_{ox}	C_{FB} (μF/cm^2)	Hysteresis ΔV_{FB} (V)	Total trapped charge density (cm^{-2} eV^{-1})	Leakage current density at VG=4V (A/cm^2)	Breakdown Field (MV/cm)
1	30 min Etching+epitaxy	0.38	8.7	0.33	2.55	1.80E+12	7.11E-06	NA
	5 min Etching+epitaxy	0.34	7.6	0.29	3.31	2.05E+12	6.67E-05	NA
2	800°C thermal oxidation	0.36	8.1	0.31	3.96	2.61E+12	5.22E-03	NA
3	HCl	0.45	7.2	0.38	0.11	8.81E+10	5.33E-02	3.2
	HF	0.51	8.2	0.42	0.33	3.10E+11	8.19E-05	6.7
	Base Piranha	NA	NA	NA	NA	NA	NA	NA
	H_2 Plasma	0.25	4.0	0.23	1.87	8.62E+11	2.09E-05	6.4
	No pretreatment	0.48	7.6	0.39	0.03	2.47E+10	2.09E-08	6.4

The other part of hysteresis is from the oxide traps that are filled and emptied through electron tunneling.[28] According to the location of the traps as a distance to the Al_2O_3/GaN interface, oxide traps could be divided to bulk traps (further from the interface) and border traps (close to the interface).[31] Bulk traps have almost no effects on the hysteresis as the probability of electron capture is low because of an exponetial decay of their capture cross section with increasing distance from the interface.[28] The border traps will respond to C-V sweeps, and thoeretically contribute to every hysteresis.[28,29] A schemetic illustrating the motion of electrons interacting with oxide traps in a single loop of CV sweeps is shown in Figure 6.7. Before the A to D sweep, the gate bias attracts electrons close to the interface which are injected and captured by the oxide traps causing a positive shift of the V_{FB}.[19] During the D to A sweep, oxide traps were emptied and became positive or neutural, which required more negative bias voltage to compensate. Consquently, a negative shift of CV curve was observed leading to the origin of hysteresis.

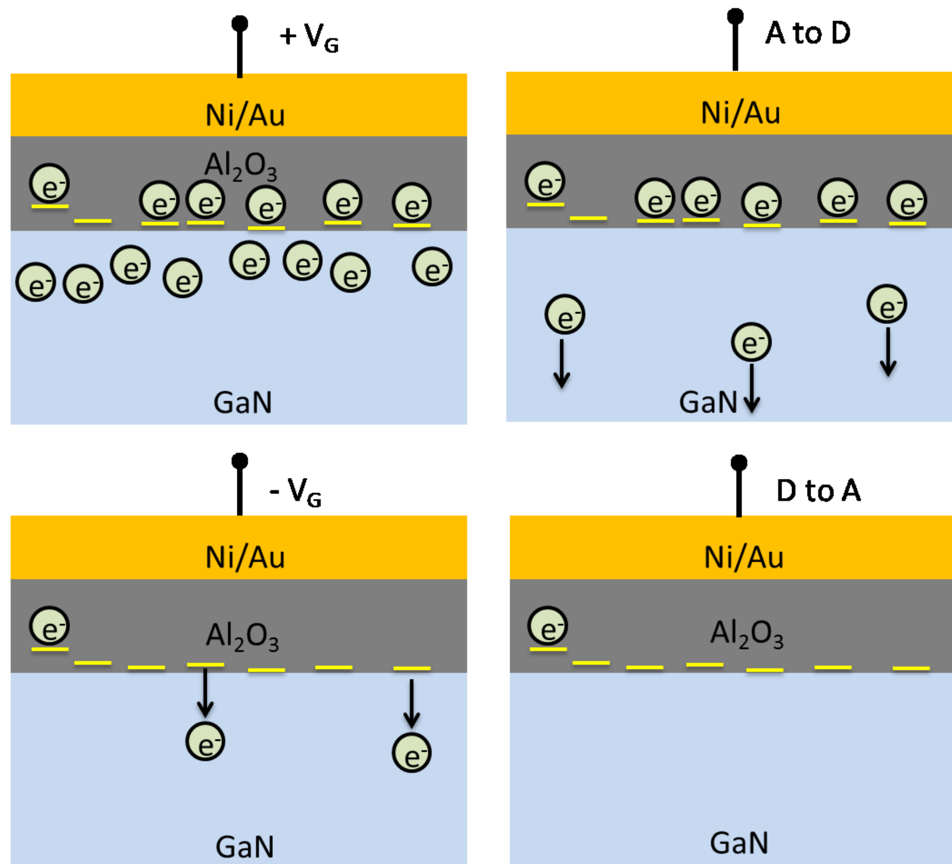

Figure 6.7 Schematic picture of electron motion in a single loop of C-V sweeps with the respect of oxide traps.[19]

The V_{FB} shift for the pretreated samples varied considerably in group three. Specifically the H_2 plasma treated sample had the largest positive V_{FB} shift followed by HF and HCl treated samples. This phenomena was observed in deposition high-k on Si based MOS sturctures.[32,33] The H_2 plasma may have attacked the N in GaN leaving a great amount of N vaccancy which could act as negative fixed charges and cause the positive shift of V_{FB}. The HF and HCl pretreatment yielded a F and Cl terminated GaN surface. The high eletronegativity of F and Cl could also act as negative fixed charges and shift the V_{FB}. A quantative study about the correlation of electronegativity of surface termination elements and the V_{FB} shift could be valuable, but is beyond the scope of this study.

All the samples exhibited deep depletion feature without inversion capacitance characteristics, which agrees well with the wide band gap semiconductor MOSCAPs.[34,35] Because the generation of minority carriers is very low at room temperature, it might take tens of years to achieve inversion in C-V measurement at room temperature as proposed by Wang *et al*.[36] on the SiC MOS structure.

The leakage current density was compared at a positive gate bias of +4V (Table 6.2). A good corelation of the Al_2O_3 roughness and current density was observed, namely smoother surface gives lower leakage current density. For example, the leakage current density of the rough HCl and 800°C samples were about 3 to 5 orders of magnitude higher than the smoother no pretreated and 30min etched samples.

Conclusion

N-polar GaN surface had been pretreated with different methods prior to ALD Al_2O_3 including: etching/pre-epitaxy, oxidation and various of chemical pretreatments. The electrical properties showed a strong correlation with the surface morphology as smoother surface yields better electrical performance. Surface pretreatments would severly affect the morphology of N-polar GaN surface due to its reactive nature, which could be detrimental for the device performance. HCl and HF surface pretreatment terminated the N-polar surface with high eletronegativity Cl and F atoms which performed as negative fixed charges and shifted the flat band voltage.Non-pretreated sample preserve the best crystal quality of GaN substrate with a smooth surface morphology leading to the lowest Q_T among all the pretreated samples.

Acknowledgement

This work was supported by Office of Naval Research (ONR) with grant number N00014-09-1-1160. Sepecial thanks to Naval Research Lab and Center for Nanophase Materials Sciences in Oak Ridge National Laboratory for the device fabircation with the proposal ID: CNMS2013-334.

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Chapter 7 - Characterization of ALD TiO_2-Al_2O_3 Laminated Gate Dielectrics on Ga-polar GaN MOSCAPs

Abstract

This research focuses on the benefits and properties of TiO_2-Al_2O_3 nano-laminate thin films deposited on Ga_2O_3/GaN by plasma-assisted atomic layer deposition (PA-ALD) for gate dielectric development. Correlations were sought between the films' structure, composition, and electrical properties. The gate dielectrics were approximately 15 nm thick containing 5.1 nm TiO_2, 7.1 nm Al_2O_3 and 2 nm Ga_2O_3 as determined by spectroscopic ellipsometry. The interface carbon concentration, as measured by x-ray photoelectron spectroscopy (XPS) depth profile, was negligible for GaN pretreated by thermal oxidation in O_2 for 30 minutes at 850°C. The RMS roughness slightly increased after thermal oxidation and remained the same after ALD of nano-laminate, as determined by atomic force microscopy. The dielectric constant of TiO_2-Al_2O_3 on Ga_2O_3/GaN was increased to 12.5 compared to that of the pure Al_2O_3 (8~9) on GaN substrate. In addition, the nano-laminate deposited on the Ga_2O_3/GaN showed small hysteresis in capacitance-voltage (C-V) characteristics yielding a total trap density of 8.74×10^{11} cm^{-2}, corresponding to a negligible carbon concentration from the XPS depth profile. The gate leakage current density ($J=2.81\times 10^{-8}$ A/cm^2) was low at +1 V gate bias. These results indicate the promising potential of plasma ALD deposited TiO_2/Al_2O_3 serving as the gate oxide on Ga_2O_3/GaN based MOS devices.

Introduction

GaN-based high electron mobility transistors (HEMTs) for power devices can operate at high frequencies, power and temperatures due to its unique physical properties like a wide band gap energy (3.4eV), high thermal conductivity (1.5 W/cmK), high electron saturation velocity (2.5×10^7 cm/s) and high dielectrical breakdown strength (3 MV/cm).[1] The metal-oxide-semiconductor (MOS) structure could further improve the performance of GaN HEMT with a larger gate voltage swing and lower leakage current which is an extremely important parameter in the radio frequency power amplifier and power switches.[2] An ideal gate dielectric for the MOS device should have: a large band offset with GaN to prevent thermal emission of electrons; a large dielectric constant to achieve a high drive current and prevent tunneling; and the ability to form a high quality interface with the GaN substrate for a lower interface trap density. However, a single dielectric material with all of these properties has not yet been discovered.

An alternative way to make such dielectric material is to combine the properties of different oxides by fabricating laminate gate stacks. Previous studies showed that thermally grown Ga_2O_3 on GaN forms a low trap density interface,[3–5] and could thus serve as a good initial layer for GaN MOS devices. Al_2O_3 is a great insulator with a wide band gap of 6.8eV but a moderate dielectric constant around 9.[6] TiO_2 processes a high dielectric constant [ε=25-80], but it has small band offset with GaN[7] The TiO_2/ Al_2O_3 laminate layer on thermally oxidized GaN takes advantages of the three oxides, which combines the high dielectric constant, high band edge discontinuity and high interface quality.

In this study, GaN metal oxide semiconductor capacitors (MOSCAPs) were fabricated with atomic layer deposition (ALD) TiO_2/ Al_2O_3 nano-laminates on Ga_2O_3 as the gate dielectric. Correlations were sought between the structure, composition, and electrical properties of the deposited oxide. Promising electrical properties of GaN MOSCAPs were observed, in terms of small hysteresis, low interface trap density and low gate leakage current.

Experiment

To evaluate the nano-laminates, GaN MOSCAPs were employed. The GaN was a 10-µm thick *n*-type c-plane (0001) layer on sapphire (0001) produced by HVPE. First, a ~2 nm Ga_2O_3 native oxide was formed by dry thermal oxidation at 850°C for 30 mins with an oxygen flow rate of 130 sccm. To expose Ga_2O_3 for patterning the Ohmic contact, Quintel Contact Lithography

Tool was used to conduct UV photolithography on the spin coated 955-2 µm photoresist. 20 sec Ar ion sputtering was used to remove Ga_2O_3 in the Oxford Plasmalab100 RIE/ICP Etcher before metal deposition. Ohmic contact Ti/Al/Ni/Au (25/20/40/50 nm) was deposited by e-beam evaporation and subsequently liftoff. To attain a low contact resistance, the Ti/Al/Ni/Au was annealed in the First Nano Rapid Thermal Processor system at 400°C for 3min and 800°C for 40s under N_2 atmosphere. This multiple stage annealing has the advantage of achieving smoother surface morphology of the metal contact reported by Feng *et al*. and Liu *et al*.[8,9]

An Oxford FlexAL Plasma Atomic Layer Deposition System was used to grow the Al_2O_3 and TiO_2 stack. The cycle of Al_2O_3 includes 30ms TMA dose followed by 1500 ms Ar purge; and 2000 ms O_2 plasma dose followed by 800ms post plasma. This yields a thickness of 1.35 Å per cycle. Then TiO_2 was deposited on top of Al_2O_3 with the recipe of 1000 TTIP dose followed by 3000ms Ar purge and 3000 ms O_2 plasma dose followed by 2000ms Ar purge. This yields a thickness of 0.43 Å per cycle. 56 cycles of ALD Al_2O_3 was conduct first to ensure a large band offset with the substrate followed by 114 cycles of TiO_2.

The sample was aligned and patterned for gate contact by the Quintel Contact Lithography Tool. A Ni/Au (20/40 nm) gate contact was deposited after 20 sec of descum photoresist to achieve good adhesion. A schematic structure of the device is shown in Fig. 7.1.

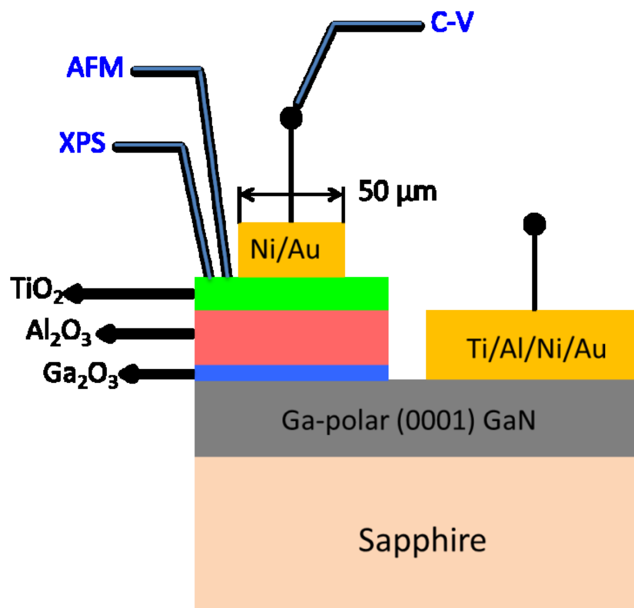

Figure 7.1 Schematic picture of GaN MOSCAP with nano-laminate gate dielectrics

Elemental compositions of the oxides were measured as a function of depth by x-ray photoelectron spectroscopy (XPS) with argon ion sputtering using a K-Alpha XPS from Thermo

Scientific. Depth profiling was carried out using 3 KV Ar-ions and was set to a known sputtering rate for SiO_2, which is 6nm/min, as calibrated on a SiO_2 standard. The thickness of Ga_2O_3 was calculated by correlating the XPS sputtering time with the SiO_2 sputtering rate while the thickness of Al_2O_3 and TiO_2 was determined by spectroscopic ellipsometry (JA Wollam M-2000U) on a silicon witness sample. Atomic force microscopy (AFM, Digital Instrument MultiMode SPM from Veeco Instruments Inc.) was used to monitor the surface morphology throughout device fabrication process. Capacitance-voltage (C-V) measurements were performed using a Keithley 4200 semiconductor characterization system operating at 100 kHz at room temperature. Hysteresis analysis was performed to assess the interface quality by holding the gate bias at accumulation for 1 second and sweeping from accumulation to depletion (A to D) and depletion to accumulation (D to A) with a sweep rate of 0.24 V/s. A current-voltage (I-V) measurement was also carried out to evaluation the gate leakage current.

Results and Discussion

Fig. 7.2 is the AFM images, comparing surface topography of the Ga-polar GaN surface and Ga_2O_3. The surface roughness increase after oxidizing for 30 min; this produced ~2 nm high bumps on the surface of the GaN. A relative low temperature (850 °C) and short reaction time (30 minutes) was used to thermally oxidize the GaN,[10] to maintain a thin smooth Ga_2O_3 surface, because a smooth oxide surface usually yields better electrical properties than a rough surface. Higher temperature for longer time produces thick oxide with rough surface,[5,11] which is detrimental for devices performance. Also, thick oxide films leads to low gate capacitance, and subsequently a low drive current. A rough surface forms interface traps and a bumpy morphology increases the local electrical field, leading to current breakdown at small voltage input.[12] The surface roughness and morphology after ALD of the Al_2O_3/ TiO_2 nano-laminate was similar to that of Ga_2O_3 which was not shown.

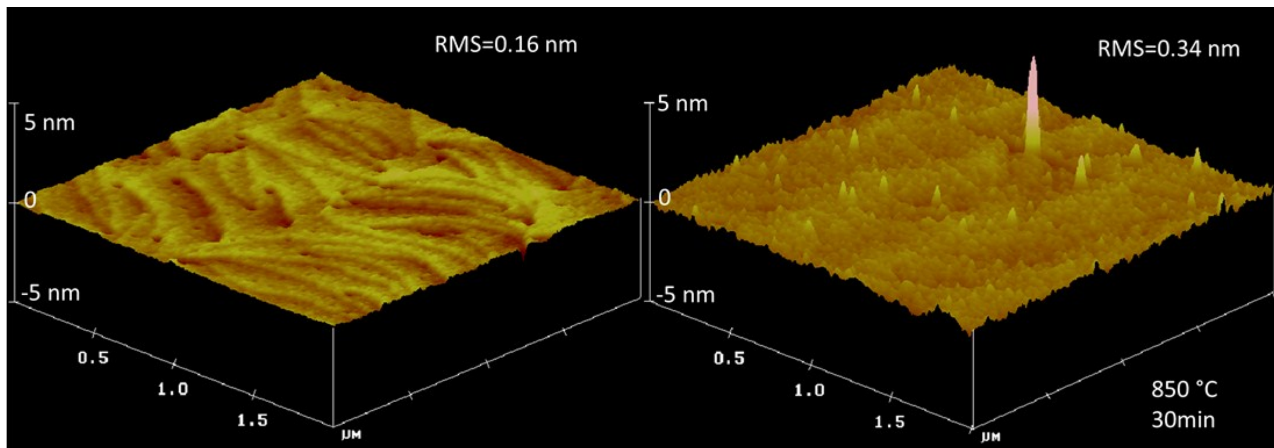

Figure 7.2 Three dimensional AFM image of (a) Ga-polar GaN surface; (b) Ga_2O_3 after thermal oxidation of 850°C for 30 min. The scanned areas were 2 × 2 µms with the Z scale of 10nm.

XPS was used to confirm the composition of nano-laminate oxide and the thermal oxide. Since XPS depth profile was destructive, it was conducted on a test GaN template. Fig. 7.3 presented the O 1s peak shift as a function of sputtering depth. The binding energy for Ti-O, Al-O and Ga-O were 529.7, 531.3 and 530.9 respectively. The binding energy of Ti-O and Ga-O were 0.2 eV and 0.1 eV off,[13] which could due to the surface charging from the Ar sputtering and X-ray shooting. But the relative position of the O 1s peaks of Ti, Al and Ga agreed well with the previous study.[13] Also, the background signal increased as the profile approaching the GaN surface. This phenomena could be explained as the bigger Ga atom has stronger scattering effect of electrons than Al and Ti, increasing the backscattered electron flux, and raising the background intensity.

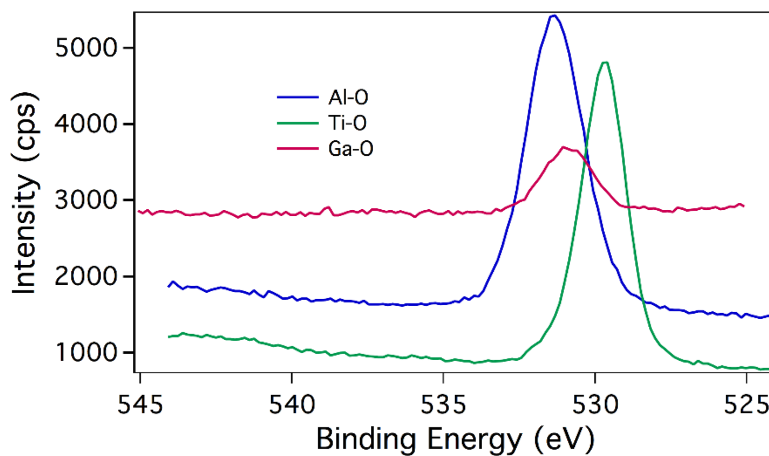

Figure 7.3 XPS spectrum of O 1s binding with Ti, Al and Ga.

The only impurities detected was carbon. (Fig 7.4 a survey). But after 5s Ar sputtering, the carbon peak signal disappeared indicating it was only due to surface contamination from the air. This agrees with the results from Wang *et al*.[14] and Fu *et al*.[15] that thermal oxidation of GaN had the advantage of limiting foreign contamination. Figure 7.4b shows the depth profile of thermal oxidation of GaN at 850°C. The concentration of oxygen disappeared after 20 sec sputtering. As the sputtering rate was ~6 nm/min on SiO_2 and the selectivity was similar on most oxide, a rough estimation of the thickness of Ga_2O_3 was 2 nm after 30 min oxidation at 850°C.

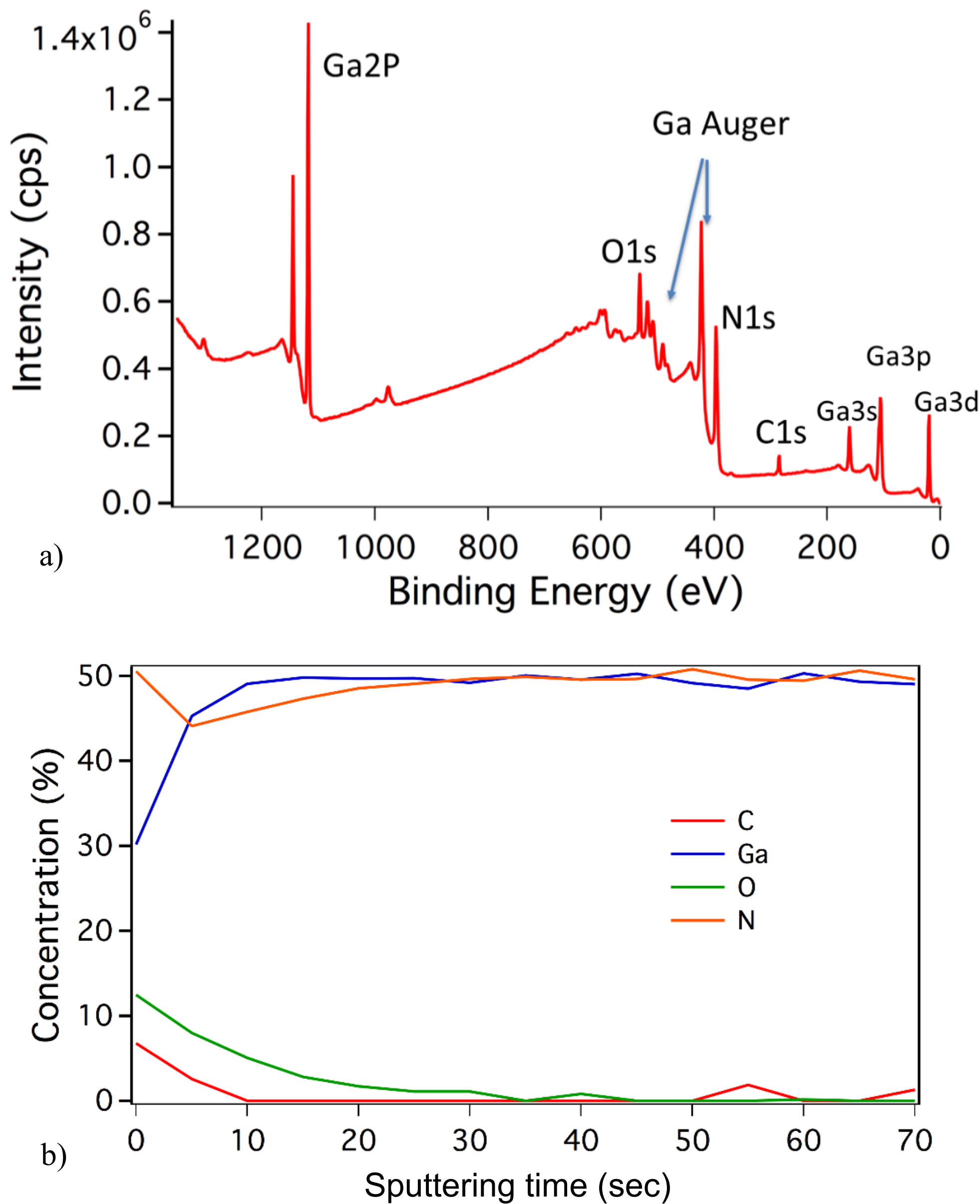

Figure 7.4 (a) XPS Survey of Ga_2O_3; (b) depth profile of Ga_2O_3

The effective dielectric constant was calculated from the accumulation capacitance based on the equation:

$$\varepsilon_{OX} = \frac{C_{OX}d}{\varepsilon_0 A}$$

Where C_{ox} is the accumulation capacitance; ε_0 is the permittivity of the vacuum; A is the area under the gate contact (1.96×10^{-5} cm^{-2}); d is the thickness of the three-layer oxide (14.2 nm) corresponding to a 2 nm Ga_2O_3, 7.1 nm Al_2O_3 and 5.1 nm TiO_2. The thickness of Al_2O_3/ TiO_2 laminates was determined on the Si witness sample by ellipsometry. With the above result, ε_{OX} was calculated to be 12.5 which is larger than that of single Al_2O_3 dielectric.

A theoretical calculation can be conducted by treating three capacitors of Ga_2O_3, Al_2O_3 and TiO_2 in series. Assuming the dielectric constant of Ga_2O_3, Al_2O_3 and TiO_2 are 10, 8.4 and 50 respectively,[12,16–18] the theoretical capacitance is 1.52×10^{-11} F determined by the following equation:

$$C_{theoretical} = \frac{1}{\frac{1}{C_{Ga_2O_3}} + \frac{1}{C_{Al_2O_3}} + \frac{1}{C_{TiO_2}}}$$

This $C_{theoretical}$ matched well with the capacitance of 1.53×10^{-11} F in the accumulation region.

Figure 7.5 presented the C-V loop for the GaN MOSCAP sweeping the voltage from A to D and returning by sweeping from D to A. A clear deep depletion behavior at negative bias voltage was observed, which was typical characteristics of wide band gap semiconductor substrate explained in the previous chapter. Quantitative analysis of total trap density (Q_T) of GaN MOSCAP was extract from the hysteresis (ΔV_{FB}) of C-V sweeps based on equation:[19]

$$Q_T = \frac{C_{ox}\Delta V_{FB}}{qA}$$

A comparison was made between the this nano-laminate oxide on Ga_2O_3/GaN and Al_2O_3 on piranha pretreated bare GaN due to similar method of calculating Q_T.[18] The nano laminate had a lower Q_T of 8.74×10^{11} cm^{-2} compare to 1.2×10^{12} cm^{-2}for the latter sample, indicating the Ga_2O_3/GaN interface quality was better. This also correlated with the contamination free interface determined by XPS.

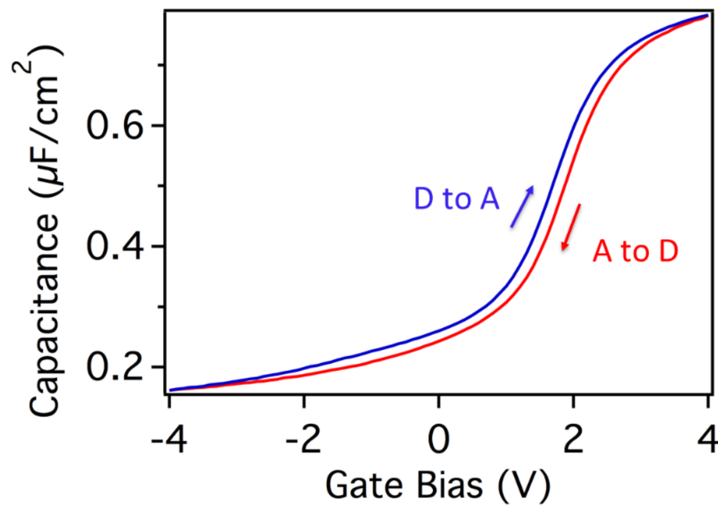

Figure 7.5 Hysteresis sweep of the GaN MOSCAP at room temperature

The $1/C^2$ characteristics of GaN MOSCAP is shown in Fig. 7.6 as a function of applied voltage from depletion to deep depletion. The $1/C^2$ curve showed good linear behavior in the bias range of 1 to 2 V indicating a consistent doping concentration distribution in the GaN.[20] From the slope of the plots, the doping density of GaN substrate was calculated to be 2.6×10^{18} cm^{-3} in reasonably good agreement to the expected value of 2×10^{18} cm^{-3}.

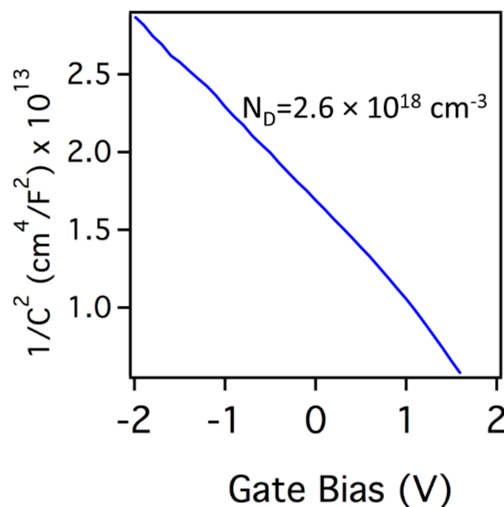

Figure 7.6 $1/C^2$ curve vs. the applied gate voltage in the depletion and depletion region. The GaN electron concentration was calculated to be 2.6×10^{18} cm^{-3}

The leakage current density ($J=2.81\times 10^{-8}$ A/cm^2) was measured at +1 V which is comparable with the $Al_2O_3/TiO_2/$ Al_2O_3 (2.5/5/2.5 nm) nano-laminates reported by Lee et al.[7] indicating good insulating characteristic of the oxide stack. The GaN MOSCAP breakdown at

4.5V corresponding to a breakdown field of 3.2 MV/cm, which is smaller than that of single Al_2O_3 oxide on GaN. The small band gap of TiO_2 leads to a smaller breakdown strength, which could be the bottleneck and affect the overall breakdown field. But the compromised breakdown field improved the effective dielectric constant and interface quality.

Conclusion

Nano-laminate Al_2O_3/ TiO_2/ Ga_2O_3 as gate dielectric was successfully fabricated on GaN MOSCAP, which combined the characters of a high effective dielectric constant, low leakage current density and low interface trap density at one device. In comparison to a simple Al_2O_3 layer, the nano-laminate offered a lower interface trap density and larger dielectric constant. It could be promising to integrate this oxide stack future GaN based devices.

Acknowledgement

This study was supported by the Office of Naval Research (ONR) with grant number N00014-09-1-1160. Device fabrication was conducted in the Center for Nanophase Materials Sciences in Oak Ridge National Laboratory with the proposal ID: CNMS2013-334.The XPS work was sponsored by the Assistant Secretary for Energy Efficiency and Renewable Energy, Office of FreedomCAR and Vehicle Technologies, as part of the High Temperature Materials Laboratory User Program, Oak Ridge National Laboratory, managed by UT-Battelle, LLC, for the U.S. Department of Energy under contract number DE-AC05-00OR22725.

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Chapter 8 - Comparison of the physical, chemical and electrical properties of ALD Al_2O_3 on *c*- and *m*-plane GaN

Abstract

This study compares the physical, chemical and electrical properties of Al_2O_3 thin films deposited on gallium polar *c*- and nonpolar *m*-plane GaN substrates by atomic layer deposition (ALD). Correlations were sought between the film's structure, composition, and electrical properties. The thickness of the Al_2O_3 films was 19.2 nm as determined from a Si witness sample by spectroscopic ellipsometry. The gate dielectric was slightly aluminum-rich (Al:O=1:1.3) as measured from x-ray photoelectron spectroscopy (XPS) depth profile, and the oxide-semiconductor interface carbon concentration was lower on *c*-plane GaN. The oxide's surface morphology was similar on both substrates, but was smoothest on *c*-plane GaN as determined by atomic force microscopy (AFM). Circular capacitors (50-300 μm diameter) with Ni/Au (20/100 nm) metal contacts on top of the oxide were created by standard photolithography and e-beam evaporation methods to form metal-oxide-semiconductor capacitors (MOSCAPs). The alumina deposited on *c*-plane GaN showed less hysteresis (0.15V) than on *m*-plane GaN (0.24V) in capacitance-voltage (CV) characteristics, consistent with its better quality of this dielectric as evidenced by negligible carbon contamination and smooth oxide surface. These results demonstrate the promising potential of ALD Al_2O_3 on *c*-plane GaN, but further optimization of ALD is required to realize the best properties of Al_2O_3 on *m*-plane GaN.

As published:

D. Wei, T. Hossain, N. Nepal, N.Y. Garces, J.K. Hite, H.M. Meyer III, C.R. Eddy, and J.H. Edgar, Physica Status Solidi (C), 11, (2014) DOI: 10.1002/pssc.201300677

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Introduction

GaN is employed for power electronics because of its ability to operate at high temperatures, high frequencies, and high power. For instance, in AlGaN high electron mobility transistors (HEMTs) high frequencies are achieved by the two dimensional electron gas (2DEG) that spontaneously forms at the AlGaN/GaN interface in the *c*-plane. These devices have a negative threshold voltage (normally-on transistor). For power applications, normally-off transistors are preferred for fail-safe operations and to minimize stand-by energy consumption.[1] As such, *m*-plane AlGaN/GaN heterostructures are promising for E-mode (normally-off) transistors due to the lack of a high-density, polarization induced 2DEG,[2] but the performance of this *m*-plane heterostructure remains largely unexplored.

By incorporating an insulated gate, the metal insulator semiconductor high electron mobility transistor (MISHEMT) has the advantages of a lower leakage current, and larger voltage swings are possible compared to the HEMT. Many studies have been conducted on the gate oxide on *c*-plane GaN;[3-5] however research of high k oxide on *m*-plane GaN is also needed to optimize the device. This is addressed in this paper. The high-k gate dielectric Al_2O_3 was deposited by atomic layer deposition (ALD) on both *c*- and *m*-plane GaN. The physical, chemical and electrical properties of the oxide were compared and correlated to the performance of the devices.

Experiments

The Ga-polar *c*-plane (0001) 2μm thick *n*-type ($1x10^{18}$ cm^{-3}) GaN film was deposited by metal oxide chemical vapor deposition (MOCVD) on *c*-plane sapphire. The non-polar GaN ($10\bar{1}0$) layer was prepared by GaN MOCVD on a pure *m*-plane GaN substrate with a 0.08 offcut angle towards the *c*-plane. The epitaxial layer was employed to ensure the surface was free of defects that might be present from substrate preparation such as chemical mechanical polishing. Both the Ga-polar and non-polar GaN surface were cleaned with a piranha solution (H_2O_2:H_2SO_4 1 : 5) at 80ºC for 10 min before ALD. Al_2O_3 was deposited using 200 ALD cycles at 280ºC on the two different substrates. The thickness of the film was estimated to be 19.2 nm by using a variable angle spectroscopic ellipsometer (VASE) on Si witness samples. The Al_2O_3 film morphology was measured by atomic force microscope (AFM, Digital Instrument MultiMode SPM from Veeco Instruments Inc.) operating in tapping mode. The composition of the ALD

oxides was determined as a function of depth by x-ray photoelectron spectroscopy (XPS) with argon ion sputtering using a K-Alpha XPS from Thermo Scientific. For depth profiling of the composition, the ALD oxides were sputtered using 3 KV Ar-ions and set to a known sputtering rate for SiO_2, which is 6nm/min, as calibrated on a SiO_2 standard. 50-μm-diameter circular capacitors with Ni/Au (20/100 nm) metal contacts on top of the oxide were created by standard photolithography and e-beam evaporation methods (Fig. 8.1).

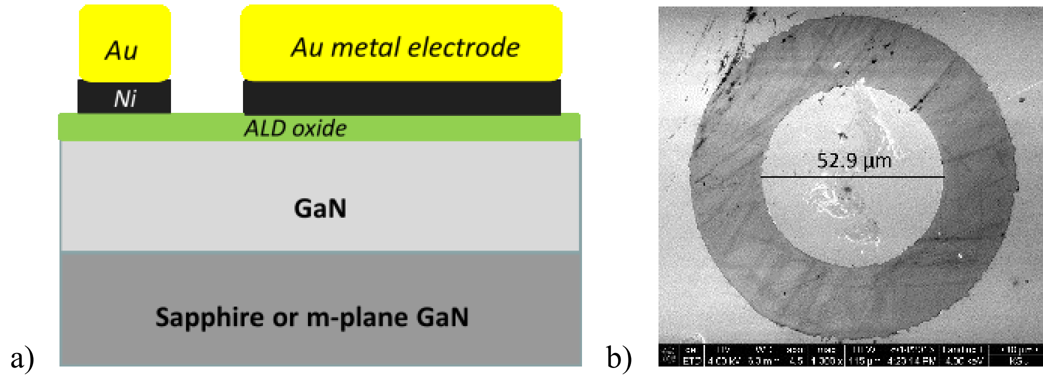

Figure 8.1 a) Schematic structure of the side view of the MOSCAP. b) Scanning electron microscopy (SEM) top view of the MOSCAP with the diameter of 52.9 μm.

The electrical properties of the gate dielectric were measured on the MOSCAPs by capacitance-voltage (C-V) measurements at room temperature. The area of the larger contact is four orders of magnitude higher than the device under test (DUT, Left MOSCAP in Fig. 1a), thus its contribution to the overall capacitance is negligible. Hysteresis sweeps were conducted with a DC bias of 4V to -6V at 1MHz with a sweep rate of 0.02V/s. Current-voltage (I-V) measurement was conducted with the large area contact as the low potential. Because of the big difference in areas, the total resistance of large area is not significant comparing to the resistance of DUT.

Results and discussion

The surface morphology of the ALD Al_2O_3 films are shown in Fig. 8.2. Based on a relative small area (1x1 μm^2) AFM scan, both Al_2O_3 films are uniform and smooth with similar morphologies on *c*- and *m*-plane GaN substrate. This indicating the piranha pretreatment yielded a favorable condition for the initiation of ALD.

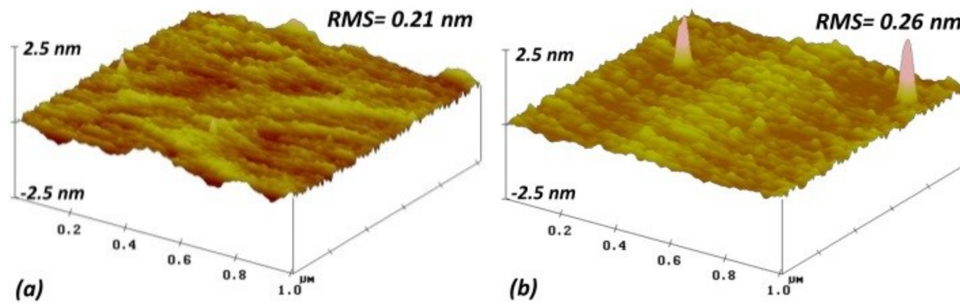

Figure 8.2 Three-dimensional AFM images of Al_2O_3 on (a) *c*-plane and (b) *m*-plane GaN. The Z height is 5 nm and scan area is 1 × 1 square micron for both images.

However, under the larger area view by optical microscopy the surface of the *m*-plane GaN was covered in steps from the epitaxial layer by MOCVD (Fig. 8.3.). This is probably due to a small offcut angle of 0.08^0 toward *c*-plane GaN. A smooth surface was reported for substrate with 2^0 offcut angle towards *c*-plane.[6,7]

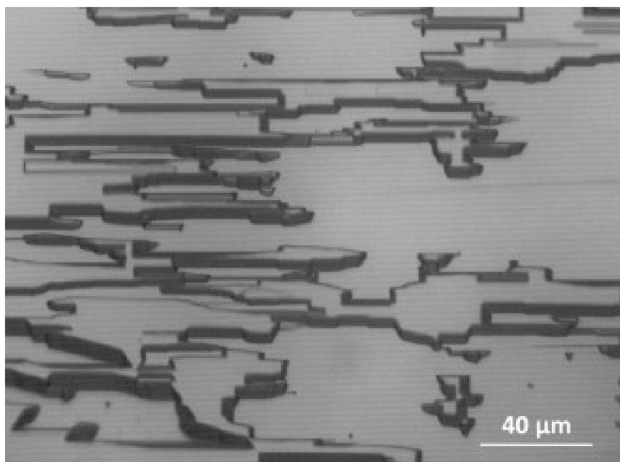

Figure 8.3 Optical microscopic image of the m-plane GaN surface. The morphology is a consequence of the epitaxial growth.

The depth profiles of the Al_2O_3 are shown in Fig. 8.4. Similar etching time of the films was observed on both *c*- and *m*-plane GaN; The gate oxides were slightly aluminum-rich with stoichiometry of Al:O=1:1.3 (~14% oxygen deficient) for the films on both *c*- and *m*-plane GaN. These proved ALD of Al_2O_3 yielded similar film composition regardless of the substrate used. The step structure on the *m*-plane GaN blocked part of the ion gun sputtering area, which led a residue signal of ~5% Al, O and 2% C. Less than 1% of fluorine was detected on the surface but disappeared after first round sputtering indicating fluorine was surface contamination.

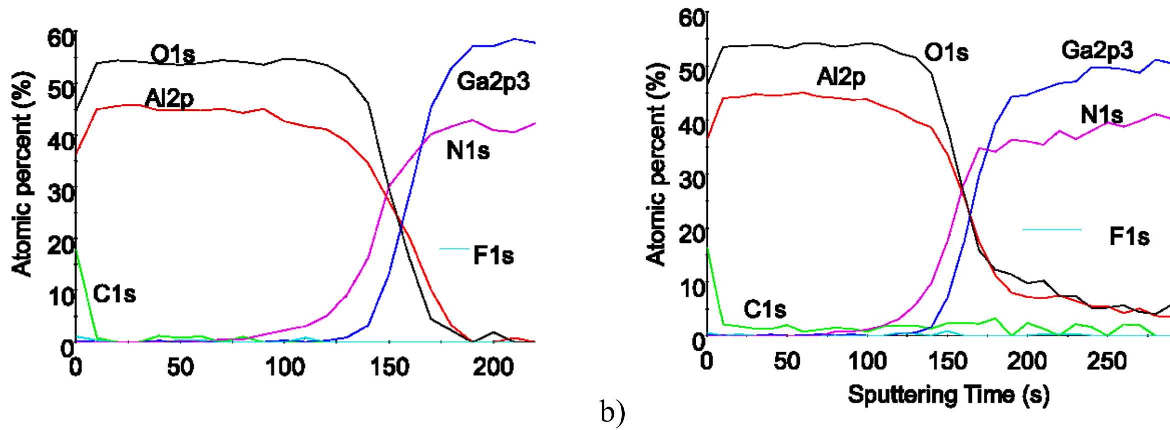

Figure 8.4 XPS depth profile of Al_2O_3 on a) *c*- and b) *m*-plane GaN.

Figure 8.5 showed hysteresis sweeps from the room temperature C-V measurement on the MOSCAPs on a) *c*- and b) *m*-plane GaN. The hysteresis was smaller on *c*-plane GaN. Also its change between the accumulation and depletion regions was sharper, indicating a lower trap density.[8] The step feature (Fig. 8.3) on the surface of the *m*-plane GaN led to overall rougher surface, which could be detrimental for the electrical performance of MOSCAP,[9] as it could form interface traps and cause a stretched-out depletion region in Fig. 8.5b.

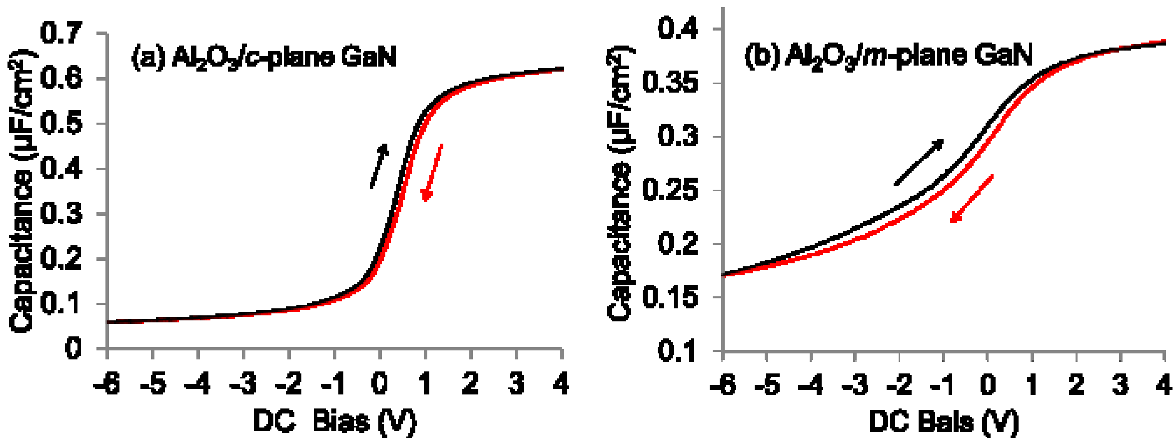

Figure 8.5 C-V measurements of the MOSCAPs on (a) *c*- and (b) *m*-plane GaN at 20 °C.

The total trapped charge was estimated by multiplying the hysteresis at the flat band voltage (V_{FB}) and the oxide capacitance (C_{ox}); V_{FB} was determined based on the flat band capacitance (C_{FB}) of the C-V measurement by:[10]

$$C_{FB} = \frac{C_{ox}\varepsilon_0\varepsilon_s A/\lambda}{\varepsilon_0\varepsilon_s A/\lambda + C_{ox}}$$

where C_{ox} is the determined from the accumulation region of the C-V curve; ε_0 is the permittivity of vacuum; ε_s is the dielectric constant of GaN (ε_s=9); A is the area of DUT; λ is the Debye length, and

$$\lambda = \sqrt{\varepsilon_s kT/q^2 N_D}$$

where k is the Boltzmann constant, and N_D is the doping concentration. The calculated results were listed in Table 8.1.

The Al_2O_3 on the *c*-plane GaN had a slightly lower trapped density: 5.68×10^{11} cm^{-2} compared to $5.83 \times 10^{11} cm^{-2}$ for Al_2O_3 on the *m*-plane. The larger hysteresis showing on the C-V of *m*-plane GaN yielding similar trapped density is because the capacitance of the MOSCAP fabricated on *m*-plane GaN is lower than *c*-plane GaN under the same DC bias in the accumulation region of the CV curve. Also, the capacitance did not reach saturation within the sweep range, possibly because the Fermi level was pinned for the *m*-plane GaN due to the high interface trap density,[11,12] which also corresponded to its stretching out C-V curve.[13] High interface traps were also observed by Hung *et al.*,[14] and could be suppressed by a 500°C post metal annealing (PMA) which was not performed in this study.

Table 8.1 Calculated oxide capacitance, flat band capacitance, hysteresis and total trapped charge density of Al_2O_3 on *c*- and *m*-plane GaN.

	C_{ox} (μF/cm^2)	C_{FB} (μF/cm^2)	Hysteresis at V_{FB} (V)	Total trapped charge ($\times 10^{11} cm^{-2}$)
c-plane GaN	0.62	0.49	0.15	5.68
m-plane GaN	0.39	0.33	0.24	5.83

The leakage current were compared at +3V, equivalent to an electric field of 1.5MV/cm (Fig. 8.6). Although, *m*-plane GaN showed a slightly lower leakage current of 0.3×10^{-12}A than *c*-plane GaN of 7.6×10^{-12}A, the ALD Al_2O_3 layers were highly insulating on both orientations.

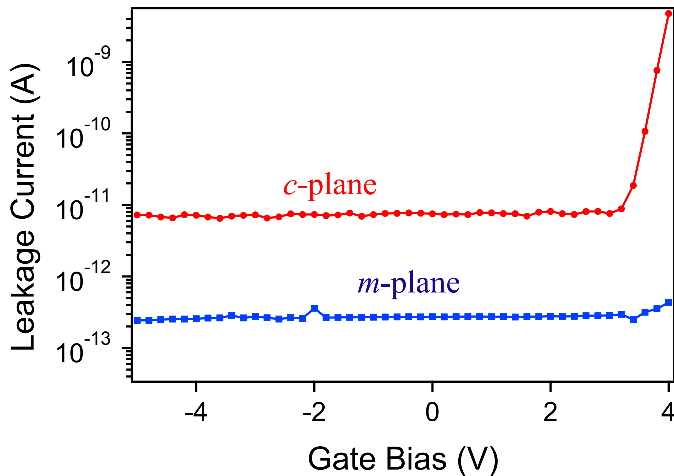

Figure 8.6 I-V measurement of the MOSCAPs on *c*- and *m*-plane GaN.

Conclusion

The oxide film shared similar thickness, surface morphology and stoichiometry regardless of substrate indicating the consistency of ALD procedure. The lower hysteresis and more abrupt change between accumulation and depletion region demonstrated better electrical properties of the ALD film on the *c*-plane than on the *m*-plane GaN. This could be improved by making smooth surface *m*-GaN with less crystal growth defects, and the performance of Al_2O_3 on low roughness *m*-GaN need to be further optimized.

Acknowledgements

This study was supported by the Office of Naval Research (ONR) with grant number N00014-09-1-1160. The XPS work was sponsored by the Assistant Secretary for Energy Efficiency and Renewable Energy, Office of FreedomCAR and Vehicle Technologies, as part of the High Temperature Materials Laboratory User Program, Oak Ridge National Laboratory, managed by UT-Battelle, LLC, for the U.S. Department of Energy under contract number DE-AC05-00OR22725.

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Chapter 9 - Conclusions and Future work

Conclusions

This project explored multiple high dielectric constant gate oxides which were deposited on different crystalline orientations and polarities of GaN by atomic layer deposition (ALD) to form metal oxide semiconductor capacitors (MOSCAPs). These devices were tested by correlating the composition, impurity concentrations, structure and morphology of gate oxides and/or GaN substrate, to the electrical properties of the device such as interface quality, leakage current density and breakdown field. These were also related to the process conditions such as deposition temperature and surface pretreatment methods under which the oxide was prepared to better control the performance of the device.

In the study of effect of surface pretreatment on N-polar GaN prior to ALD Al_2O_3, several pretreatment methods were systematically investigated and compared including etching/pre-epitaxy, oxidation and various chemical pretreatments. Due to the reactive nature of N-polar GaN, the surface morphology could be greatly changed with a small change of one parameter of pretreatments. For example, 850°C oxidation temperature produced very rough surface (RMS=1.41 nm) which showed no sign of the MOSCAP behavior in the capacitance-voltage (C-V) measurement, while 800°C oxidation yielded relative smooth surface (RMS=0.56 nm) and presented regular accumulation to deep depletion of GaN MOSCAPs during C-V sweep. We demonstrated a 14 nm thick ALD Al_2O_3 films were directly deposited on N-polar GaN without thermal or chemical pretreatments, which yield a smooth surface, small flat band voltage shift, low leakage current and good Al_2O_3/GaN interface quality. We believe this study open a new page for the future research of N-polar GaN MOSHEMTs for high frequency applications.

In the study of TiO_2- Al_2O_3 nano-laminate, a higher dielectric constant with similar insulation ability and interface quality was observed on Ga-polar GaN MOSCAPs adapting the oxide stack of TiO_2/ Al_2O_3/ Ga_2O_3 comparing to the simple Al_2O_3 on GaN. The main contribution to the rising of dielectric constant is the integration of the high dielectric constant material of TiO_2, and there is still possibility of improving the interface quality of this three oxide feature.

In this dissertation, a correlation between the surface morphology of oxides and device performance was discovered. Generally, a smooth gate dielectric and substrate offers better electrical properties such as low gate leakage, low interface traps and high breakdown field. This offers an expectation of depositing oxide films for fabricating GaN based devices.

Future work

For the surface pretreatment on N-polar GaN, although non pretreated sample demonstrate superior performance than other pretreated samples, there was hysteresis on the C-V sweep and positive flat band voltage shift indicating fix charges and traps presenting at the interface. A mild surface cleaning method with good selectivity needs to be discovered to maintain the least damage to the GaN substrate but effective enough to target and remove the carbon and hydrogen impurities.

The effective dielectric constant of oxide nano-laminates could be further increased by depositing a thinner Al_2O_3 layer and thicker TiO_2 layer. Special attentions are needed to better tune the thickness of Al_2O_3 to ensure the insulating ability of this high band gap gate dielectric. To deposit smooth oxide surface as an initial layer for later ALD deposition, different methods of growing Ga_2O_3 could be investigated rather than thermally oxidized GaN.

For wide band gap energy GaN, the electrons captured by deep-lying interface states cannot emit to the conduction band at room temperature and become fixed charges. This could be more accurately measured with UV light assisted C-V measurement. Because the minority carriers generated by the UV light could react with the deep-lying state and distort the shape of C-V curves. Quantitative measurement of the state density could be derived with respect of the change in C-V sweeps.

Appendix A - Process flow of GaN MOS capacitor with top to bottom contact

Figure A.1 Photoresist (PR) spin coating on Ga_2O_3/GaN/Sapphire 2-inch wafer. P20 was spin coated first as a primer which improves the adhesion of the PR to the surface, followed by the 955-2 µm positive photoresist. 3000 rpm spin rate was applied to both chemicals, and a pre-exposure baking of 90 °C for 90 sec was conducted to reduce the solvent concentration in the PR. This prevents the PR sticking to the mask and improves the resist adhesion.

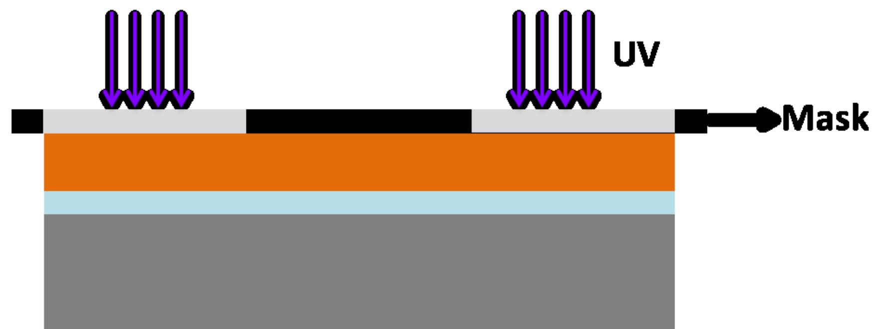

Figure A.2 Ultra-violet light exposure for 3 sec. A post exposure bake at 115°C for 90 sec was applied to further harden the PR and improving the adhesion

Figure A.3 Develop the exposed PR in CD-26 for 75 sec. The exposed PR turns into clouds in CD-26. Rule of thumb of a good development is visually observe the disappearance of clouds and wait for additional 10 sec. Wafer will subsequently rinsed by DI water and characterized under optical microscope for the quality of development. Surface Profilometer was used to monitor the thickness of PR.

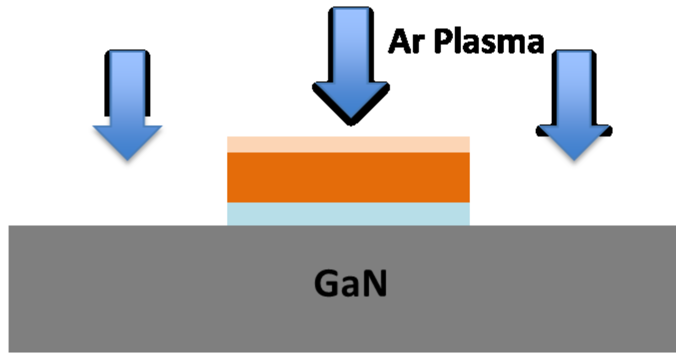

Figure A.4 Reactive ion etching (RIE). Etching process is very sensitive to the chamber condition. A 10 min pre-clean of RIE chamber was applied before loading the wafer. The exposed Ga_2O_3 on the surface of the wafer was etched by Ar ion with an RF generation power of 2500 W and DC bias of 50 W. This is a combination of descum PR and device feature developing. A 20 sec sputtering removes surface contamination, and improves the adhesion for Ohmic contact metal deposition.

Figure A.5 Metal deposition to form Ohmic contact. Metal stack of Ti/Al/Ni/Au was evaporated in order by electron beam evaporation. The thickness of each layer is 25/20/40/50 nm. The first Ti layer reacts with N in GaN forming TiN which has low band offset with GaN. Meanwhile the N vacancy increase the conductivity of GaN. Al and Ni prevent the diffusion of Ti and Au respectively. Also, 40 nm of Ni provide better adhesion for Au layer

Figure A.6 Liftoff. Wafer was immersed in an acetone and sonicated for 5mins in the dirty slurry, followed by another 5mins sonication in the clean bath.

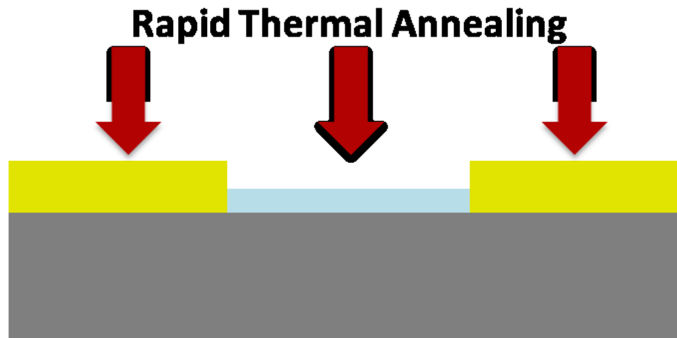

Figure A.7 Rapid thermal processing (RTP). The metal stack needs to be annealed to decrease the resistivity. RTP was ramped to 400°C within 20 sec and wafer was soaked for 3 min to let the heat evenly distribute across the wafer. Then, the system temperature was increased to 800°C within 40 sec and maintain 800°C for 25 sec. The whole thermal process was under N_2 atmosphere.

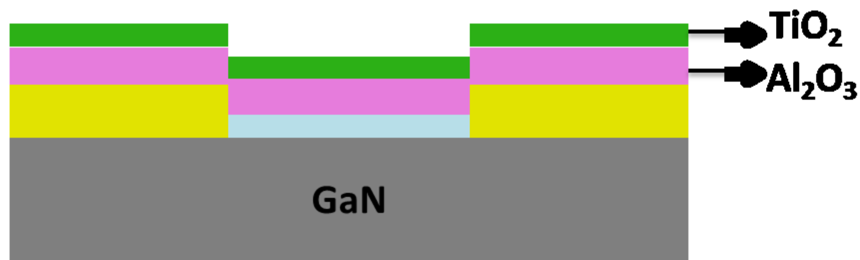

Figure A.8 ALD of high-k oxides. The cycle of Al_2O_3 includes 30 ms TMA dose followed by 1500 ms Ar purge; and 2000ms O_2 plasma dose followed by 800 ms post plasma. This yields 1.35 Å per cycle. Then TiO_2 was deposited on top of Al_2O_3 with the recipe of 1000 TTIP dose followed by 3000ms Ar purge and 3000ms O_2 plasma dose followed by 2000 ms Ar purge. This yields of 0.43 Å per cycle. The thickness of both oxide was characterized to be 7.1 nm and 5.1 nm on Si witness wafer under ellipsometry.

Figure A.9 PR spin coating. The thickness of PR is 0.7 µm with a recipe of P20 as the primer and 955-0.7 at the PR. The spin rate was 4000rpm for 45 sec.

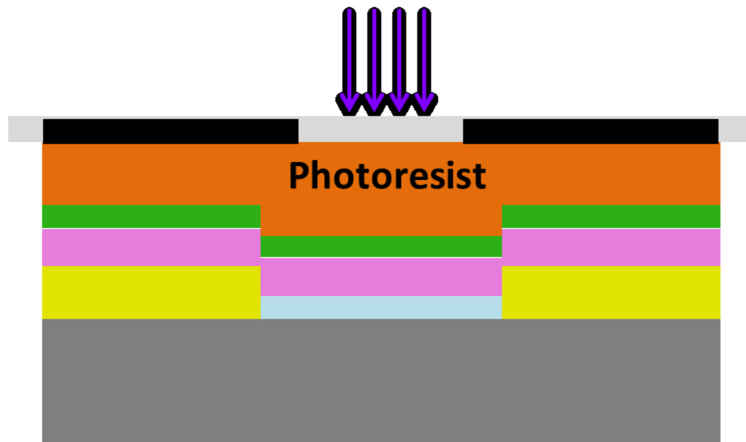

Figure A.10 Mask alignment and Exposure. The alignment mark was adjusted under microscope before a 5-seconds exposure.

Figure A.11 Develop the pattern in CD-26 for 1 min. The quality of the photolithography was monitor under the microscope and the thickness of PR was measured by surface Profilometer.

Figure A.12 Ni/Au (20/40 nm) was evaporated in order to form the gate contact.

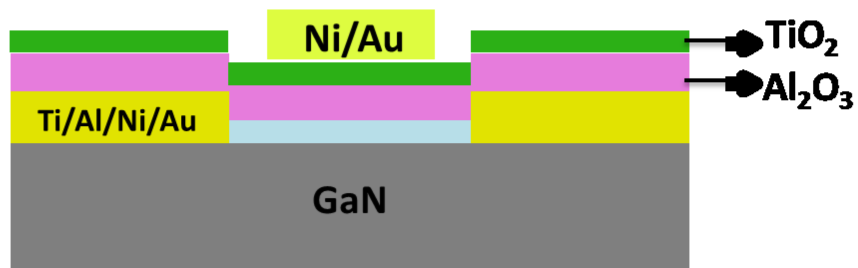

Figure A.13 Liftoff. Wafer was immersed in the acetone bath and sonicated for 5 min then transferred to clean acetone bath for another 5 min sonication. Finally, wafer was rinsed by IPA, DI water and air dry to get rid of the liftoff metal particles on the surface.