# REDUCING PHASE NOISE AND SPURIOUS TONES IN FRACTIONAL-N SYNTHESIZERS

by

DANIEL ALLEGRE

B.A., Kansas State University, 2007

A THESIS

submitted in partial fulfillment of the requirements for the degree

MASTER OF SCIENCE

Department of Electrical Engineering
College of Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

2009

Approved by:

Major Professor
BILL KUHN

# Abstract

A frequency synthesizer is a control system which employs a reference signal from a component, such as a crystal oscillator, with excellent phase and frequency stability to synthesize higher frequencies with similarly desirable characteristics. Such a control system is at the heart of many communication schemes.

Due to the digital circuitry used in frequency synthesis, it is relatively straightforward to synthesize frequencies at integer multiples of the reference signal frequency. A synthesizer which achieves this is called an integer-N frequency synthesizer. The main challenge in the design of integer-N synthesizers is to reduce phase noise introduced by circuitry while achieving a needed frequency resolution.

Noise can be spectrally spread by conversions in the loop which are non-linear, so the strategy to reduce noise is two-fold. Control-loop and circuit design techniques can be used to reduce device noise, but it is also important to make sure that the noise performance is not degraded by spectral spreading within the loop. This thesis addresses primarily the latter approach with the design and implementation of circuits targeting a specific conversion within the loop.

Frequency resolution of a synthesizer can be improved by introducing additional circuitry and complexity. This additional complexity makes it possible to multiply the reference frequency by a fractional number and thus achieve higher frequency resolution. A control system which achieves this is called a fractional-N frequency synthesizer.

The cost associated with the increased frequency resolution is a form of noise that is deterministic called spurious noise. This spurious noise can also be spread and amplified by non-linear conversions in the control loop. A quantitative understanding of the magnitude of this noise that is not readily available in the literature was developed in this research.

A comparison between several implementations of integrated frequency synthesis was also carried out in this research with the intent of providing guidelines to produce a better performing synthesizer. These implementations differ in key components of the loop where linearity is of particular importance.

# Table of Contents

# List of Figures

# Chapter 1: Synthesizer Basics

## [1.1] Integer Frequency Synthesis

A frequency synthesizer is a type of phase locked loop where a reference signal with a given frequency is employed to create signals with frequencies which are multiples of the reference signal frequency. The block diagram for a simple "integer-N" frequency synthesizer is shown in Figure 1.1.

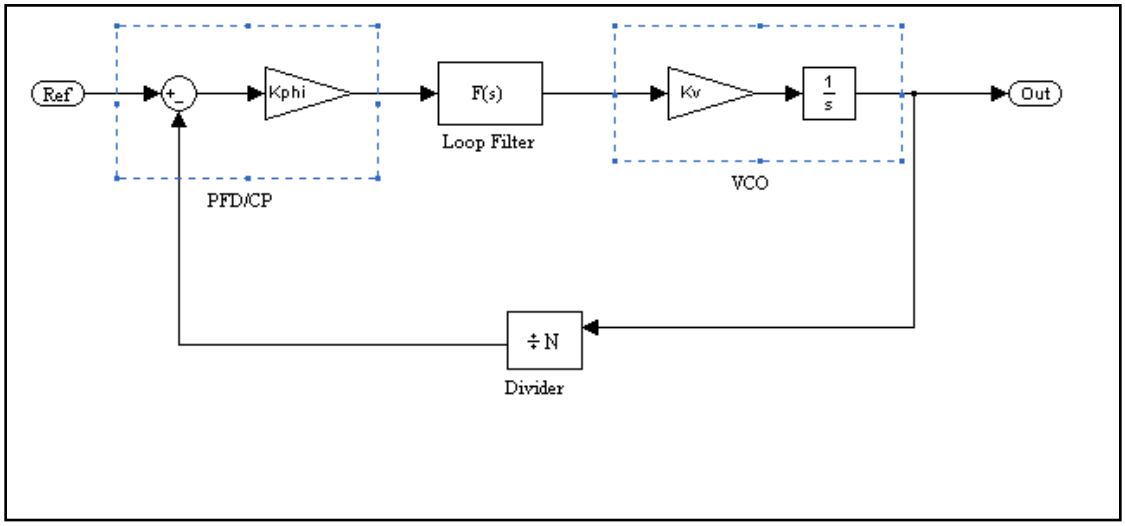


Figure 1.1: Simple Frequency Synthesizer Block Diagram

### *[1.1a] Block Diagram Description*

The reference signal is usually generated by a crystal oscillator (XO) or temperature compensated crystal oscillator (TCXO). This type of component creates a sinusoidal output signal at the physical resonant frequency of the device. The reference signal is typically characterized by excellent frequency stability and high spectral purity (low phase noise). A signal which closely approximates a sinusoidal wave in the time domain also approximates an impulse in the frequency domain. Figures 2 and 3 show plots of the time and frequency domain representations of such a signal.

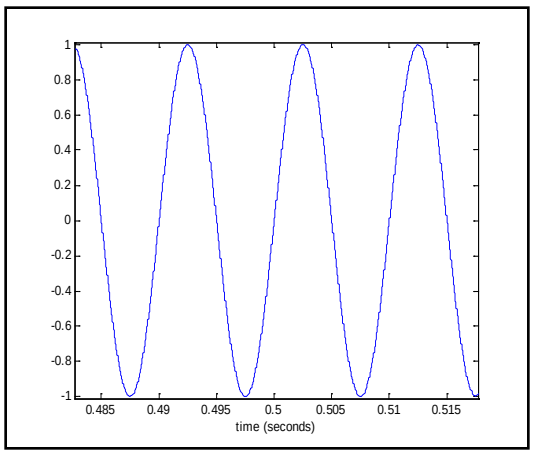


Figure 1.2: Excerpt of a Time Domain 100Hz Sinusoidal Signal

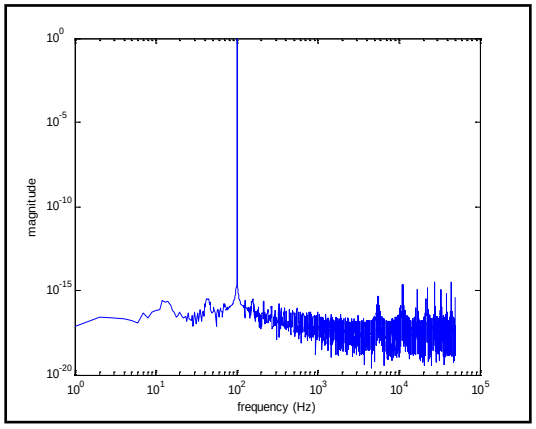


Figure 1.3: Frequency Domain Representation of Figure 1.2

The key thing to notice about Figure 1.3 is that ideally all of the information in the sinusoidal signal is contained at a single frequency. Noise in this figure is from quantization errors in the finite precision calculations in MATALB. In a physical oscillator, the primary sources are thermal noise and shot noise from active devices. If the quality factor of the resonator is very high, such as in a crystal, this noise is minimized and confined to a few Hz around the resonant frequency. Because signals generated by crystal oscillators have a nearly ideal frequency domain characteristic, this signal will, for now, be considered as a single frequency rather than a signal made up of multiple frequency components.

An experienced reader may notice that the simple frequency synthesizer of Figure 1.1 is a type of control system where an output signal is fed back and compared with an input signal. The divider block in the feedback loop represents a division in frequency. Just as the TCXO reference signal can be thought of as a single frequency, the input and output of this block can also be thought of as single frequencies where the divided signal is an integer number ("N") times lower than the frequency of the VCO. Hence the VCO is N times the frequency of the reference. It is the intent of the feedback control system to assure that this relationship holds.

In the analysis of the synthesizer, we will assume that the VCO is at or near this frequency (N times the reference frequency), and concentrate on the "phase-locked" behavior. The section of the loop labeled PFD/CP represents the phase frequency detector and charge pump. In the locked condition, this section can be thought of as a mechanism by which two phases are compared and a current is generated that is proportional to the difference between the two phases. The word "difference" is a convenient word to use here because the comparison can also be thought of as subtraction. Note that the polarity of this subtraction is such that the divider's output phase (the VCO's phase divided by N) is subtracted from the reference signal phase. The proportionality constant between the phase difference and the output current will be represented by $K_{phi}$.

The loop filter converts the current signal generated by the PFD/CP into a voltage and provides a low-pass response on the PFD/CP output. This filter can simply be thought of as an integrator and current-to-voltage converter at this point in the discussion.

The VCO or voltage controlled oscillator converts a voltage from the loop filter into a frequency with the proportionality constant $K_v$ and to a phase via an integration (which can be represented by 1/s in the Laplace domain).

### *[1.1b] Basic Operation*

With a description of the fundamental building blocks of the frequency synthesizer imparted, an explanation of the operation of the loop can be presented.

The purposes of the frequency synthesizer are to generate a frequency at the output that is a multiple of the reference frequency and to have the VCO track the reference signal's (very stable) phase behavior. In this design, the multiple is the number N. To show how this is accomplished, two cases might be considered. The first case is where the divided output signal leads the reference signal in phase and the second is where the divided output signal lags behind the reference signal in phase.

When the divided output phase is greater than the reference phase, the PDF/CP will generate a negative current at its output. The loop filter will then convert this negative current into a negative voltage. The loop filter will also integrate this negative voltage, creating a down-sloping voltage ramp at its output. This down-sloping voltage will be seen by the VCO, and since the VCO converts voltage to frequency, the frequency of the output signal will decrease.

Assuming that the VCO frequency doesn't decrease too much, the consequence of the process described above would be that the divided output's phase decreases with the VCO frequency. The two phases seen at the PFD input (the reference and the divided output) would then be closer together.

The second case to be considered is where the divided output phase is less than the reference phase. In this case, the PFD/CP will output a positive current, which will produce a positive voltage on the loop filter that will increase the output frequency from the VCO.

These two cases should illustrate for the reader that when the loop is in phase-locked operation, it will force the divided output phase to be equal to the reference phase. This

translates into the output frequency being N times the reference frequency ($f_{ref} = f_{out}/N$ or $f_{out}=Nf_{ref}$).

## [1.2] Fractional-N Synthesizers and the Problem of Spurious Signals

The simple frequency synthesizer described above can take advantage of the spectral purity of the TCXO signal to produce a spectrally clean output signal, assuming that the noise contribution from the divider, PFD/CP, loop filter and VCO are small.

In reality, of course, the noise contributions of each part of the loop degrade the spectral quality of the output signal. The purpose of this document stems in part from the fact that there are fundamental limitations to a simple frequency synthesizer as described in the previous section.

The fundamental limitation of the simple frequency synthesizer discussed in the previous section is based on a limitation in the frequency divider. The frequency divider is a digital circuit that employs counters to produce an output pulse after an integer number of input pulses. This implies that the number by which the frequency is divided must be an integer. The output frequency then is constrained to be an integer multiple of the reference frequency. It is for this reason that the simple frequency synthesizer described above is commonly referred to as an *integer-N frequency synthesizer*.

In many modern communication schemes, portions of the available electromagnetic spectrum must be divided into smaller sections, calling for frequency synthesizers with higher frequency resolution. Resolution, in this context, is a term used to describe how finely the output frequency in the loop can be tuned. In an integer-N synthesizer, the frequency resolution (or "tuning step size") is equal to the reference frequency.

As an example, if an engineer is designing a loop using a TCXO at 10MHz, he or she could employ an integer-N synthesizer to produce frequencies at integer multiples of 10MHz (20MHz, 30MHz, 40MHz, etc.). If the engineer is designing for a communication standard that calls for transmission or reception of frequencies separated by a channel spacing of 500KHz, it should be clear that the above scheme would not work without modification.

One solution which may come to mind would be to reduce the reference frequency by dividing it down before the PFD, for example. This is not an effective solution because, in addition to fine frequency resolution, many modern communications standards also call for fast acquisition times. The acquisition time of a synthesizer is the time it takes for the output frequency to converge to its programmed value ($Nf_{ref}$). Decreasing the reference frequency used by a synthesizer increases the acquisition time because it puts a constraint on the bandwidth of the loop filter. This constraint arises from the need for the loop filter to keep the reference signal from feeding through to the output signal. In general, the loop filter should have a cutoff frequency that is less than one tenth of the reference frequency.

Therefore, if the reference frequency is low, the bandwidth of the loop filter must be made appropriately narrow. A narrower loop filter bandwidth will result in a longer acquisition time. In addition, there are penalties to the output phase noise of the synthesizer if the reference frequency and therefore the loop bandwidth are significantly decreased [see section 4.3a].

### *[1.2a] Fractional Dividers*

The solution that is commonly used to simultaneously address the problems of spectral purity, acquisition time, and frequency resolution is to add additional circuitry so that the loop is multiplying the reference frequency by a non-integer number even though the frequency divider still operates under the constraint that it can divide by an integer number only [15]. This is

accomplished by rapidly modulating the divisor (N) so that, over time, the loop effectively sees a fractional frequency division at the divider. A synthesizer that employs this technique is called a *fractional-N synthesizer*.

A simple example of a fractional-N synthesizer is often used to explain how this can be possible. The frequency division number N is alternated between an integer (n) and a greater integer (n+1) each time the reference phase is compared with the divided output phase. It may be intuitive that the loop output under these conditions will not converge to the frequency ($n*f_{ref}$) or the frequency ($(n+1)*f_{ref}$), but rather the output will converge to the average of these two frequencies over several comparison cycles. The output frequency of the loop would converge to ($(n + 1/2)*f_{ref}$) in this case, and a fractional division will have been achieved. The engineer from the previous illustration could now achieve the frequency resolution required for his or her communication standard with frequency divisions of 5MHz using a 10MHz TCXO.

### *[1.2b] Spurs*

This example also provides an introduction to a problem that is addressed in this thesis. If the output frequency is being divided alternately by (n) and (n+1) with each comparison by the PFD/CP and the output frequency has converged to ($(n+1/2)*f_{ref}$), the divided output frequency fed back to the PFD will alternate between ($((n+1/2)/n)*f_{ref}$) and ($((n+1/2)/(n+1))*f_{ref}$). The frequency ($((n+1/2)/n)*f_{ref}$) is higher than the reference frequency and the frequency ($((n+1/2)/(n+1))*f_{ref}$) is lower than the reference frequency, so phase errors will occur and the PFD/CP will put out negative and positive pulses of current. Figure 4 illustrates what the time domain plots of the divided output frequency, the PFD/CP output, the loop filter voltage and the VCO output frequency might look like in this example.

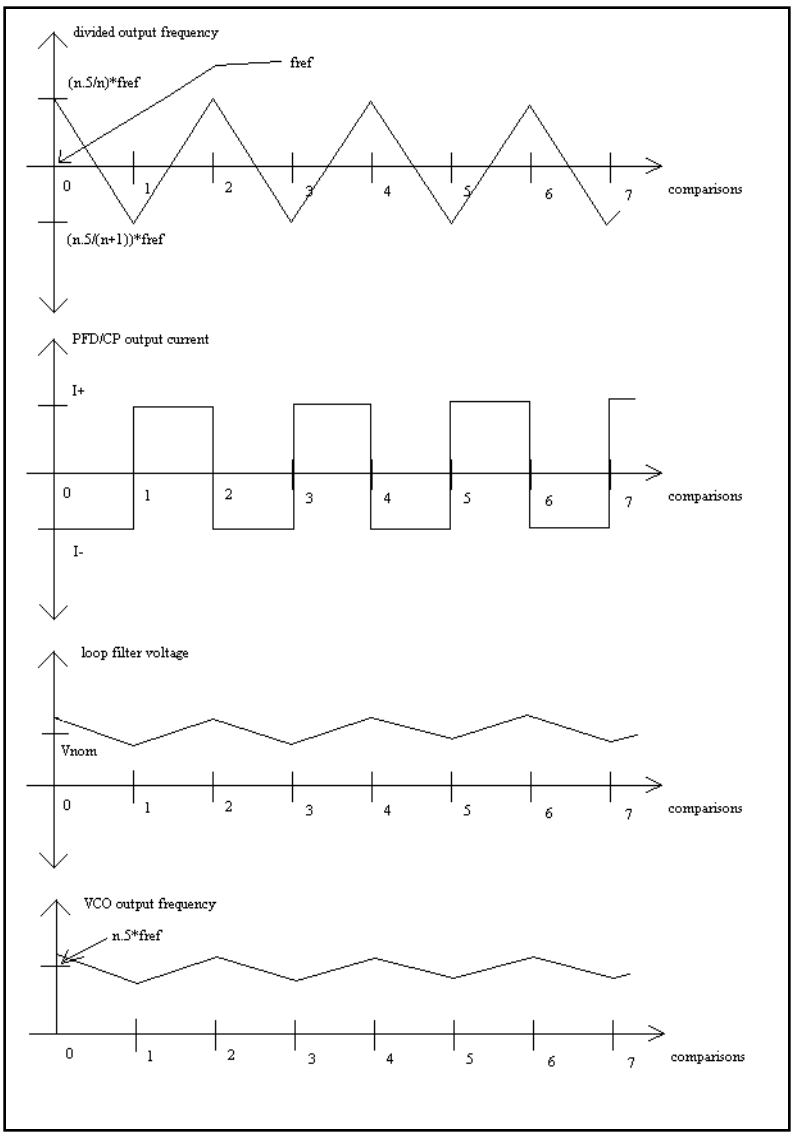


Figure 1.4: Frequency, Current and Voltage Plots for Simple N-Fractional Synthesizer

The important thing to notice in Figure 1.4 is that, when the divider is modified with each comparison, the VCO loop filter voltage and therefore the output frequency of the synthesizer is effectively modulated by a triangle wave. The output signal now can no longer be thought of as a pure sinusoidal signal, but a sinusoid that is FM modulated and therefore composed of multiple frequency components. Figure 1.5 shows the frequency domain representation of a sinusoid modulated by a triangle wave.

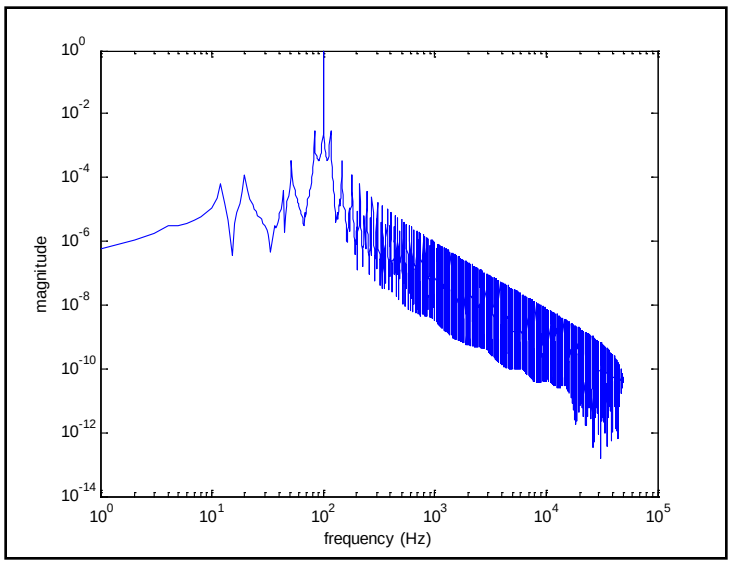


Figure 1.5: Frequency Domain Representation of a Triangle-FM-Modulated Sinusoid

This simple example illustrates why spurious signals are produced in the spectral content at the synthesizer output when the loop is made to dynamically divide by a fractional value. This example also provides the motivation to find a frequency-domain mapping from modulation of the division to the spectral content of the synthesizer output.

## [1.3] Mapping from Modulation of the Divider to Spurious Content at the Output

### *[1.3a] Closed-Loop Synthesizer Transfer Function*

To find what effect changing the value in the feedback divider will have on the output spectrum generated by the VCO, the frequency synthesizer will be considered as a control system in the Laplace domain. Figure 1.6 shows the block diagram of a synthesizer again, but with phases at different nodes in the loop labeled.

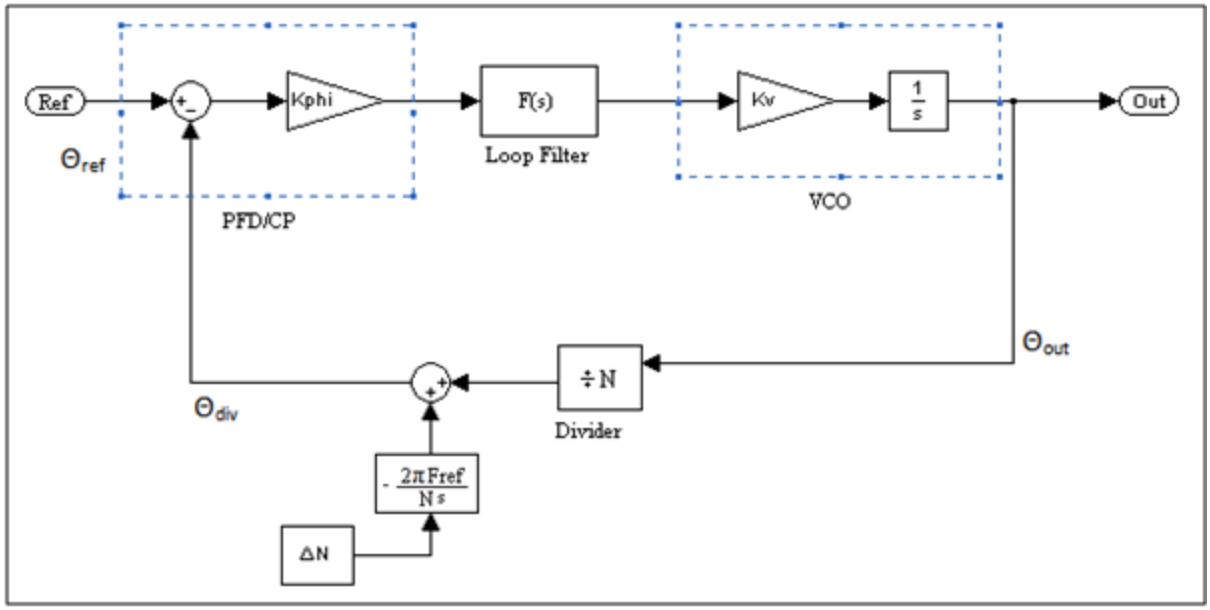


Figure 1.6: Block Diagram of a Fractional-N Synthesizer with Phases Labeled

The block diagram in Figure 1.6 describes the same system that is described by the block diagram in Figure 1.1, except that the N divider is no longer a constant. In Figure 1.6, signals are also denoted by their phases. Any change in the value of "N" results in a change in the frequency of the divided output signal. Any change in frequency will result in an accumulation of phase error at the PFD input. Therefore, in order that a change in "N" be represented as an effective change in the phase of the divided output signal, this change must be integrated before being taken into the loop because a change in frequency will cause an accumulation of change in phase. The factor $(2\pi f_{ref}/(Ns))$ required to take N into the loop is derived in section 1.3c.

To determine the closed-loop transfer function, the open-loop transfer function must first be considered. The gain of the PFD/CP, the transfer function of the loop filter and the gain of the VCO can be grouped together to form the open-loop transfer function of the synthesizer. The three transfer functions combine to form the right-hand side of Equation 1.1.

$$H_{ol}(s) = \frac{K_v K_{phi} F(s)}{s} \tag{1.1}$$

Grouping these factors together is a useful step in determining the closed-loop transfer function of the synthesizer because it puts the loop into a familiar form known to students of control systems. Figure 1.7 illustrates such a grouping.

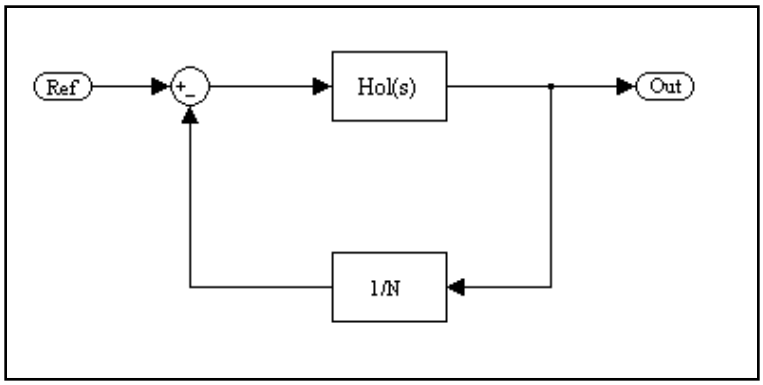


Figure 1.7: Frequency Synthesizer in Familiar Form

Using basic control systems theory [14], it can be determined that the closed-loop transfer function of the system described by the block diagram in Figure 1.7 can be represented by Equation 1.2:

$$H_{cld}(s) = \frac{H_{ol}(s)}{1 + H_{ol}(s)/N} \tag{1.2}$$

Combining Equations 1.1 and 1.2 gives the closed-loop transfer function of the frequency synthesizer from the reference to the output (Equation 1.3), which describes how non-idealities in the reference spectrum are translated into phase noise at the output.

$$H_{cl}(s) = \frac{K_{phi}K_vF(s)/s}{1 + K_{phi}K_vF(s)/Ns} \tag{1.3}$$

### *[1.3b] Closed-Loop Synthesizer Transfer Function from Divider to Output*

Since phase is the integral of frequency, a sudden change in the divided output frequency due to a sudden change in N will translate into an accumulation (or integration) of phase error at the divided output signal. A change of $\Delta N$ in the value of N will also have to be scaled by a factor of $(2\pi f_{ref}/N)$. See section 1.3c for a derivation of this scaling factor. Figure 1.8 illustrates

how this can be represented in the frequency synthesizer block diagram. Note that the phase of the reference has been taken to be zero, as the reference signal will be assumed to be ideal for this discussion.

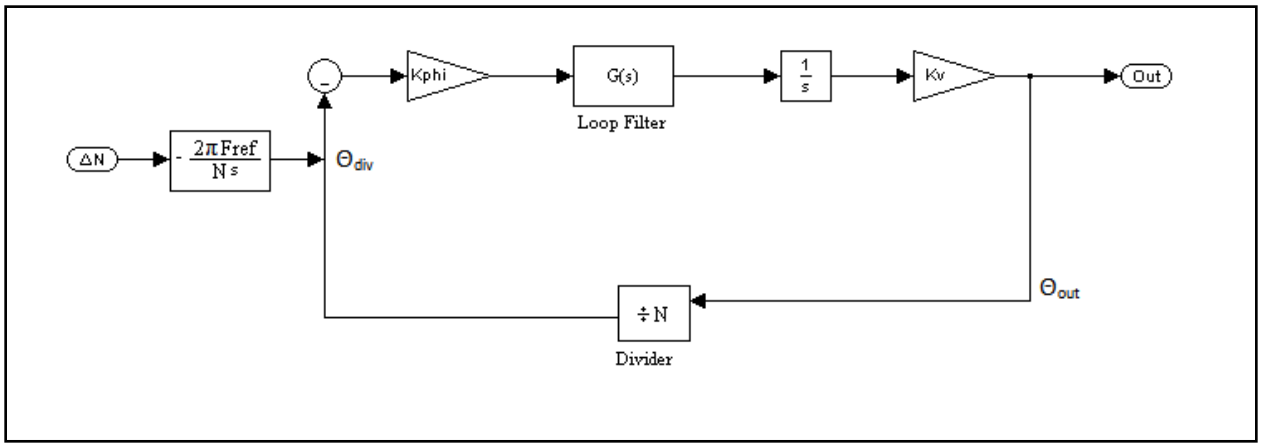


Figure 1.8: A Phase Domain Representation of Divider Modulation

The block diagram represented in Figure 1.8 can be rearranged so that the phase disturbance from the frequency divider acts on the loop in a similar manner that the reference phase acts on the loop. Figure 1.9 shows the block diagram with this modification where the reference phase has been taken to be zero (a pure TCXO signal). Note that these two systems (Figure 1.8 and Figure 1.9) are equivalent.

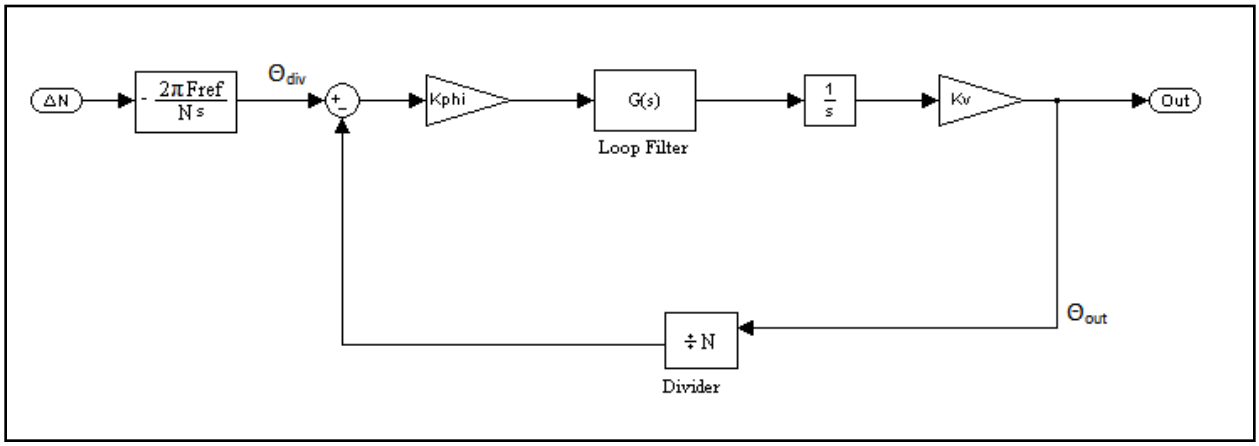


Figure 1.9: Modified Representation of Divider Modulation

The blocks in Figure 1.9 can be condensed so that the loop is in a more familiar form from which a closed-loop transfer function can be easily derived. Figure 1.10 shows the modified block diagram in this form.

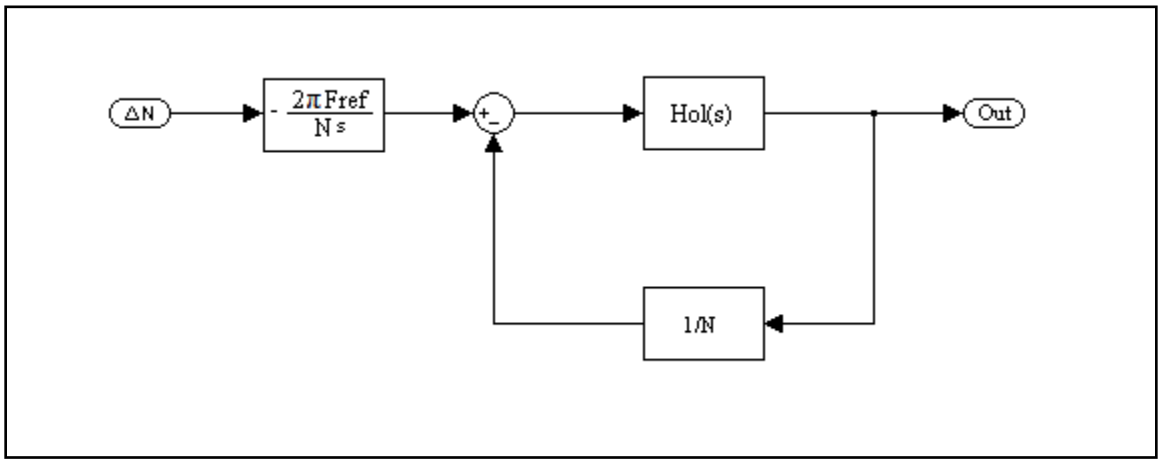


Figure 1.10: Modified Block Diagram in Simplified Form

It can easily be seen that the closed-loop phase transfer function from the input of Figure 1.10 (representing the ΔN values) to the phase output of the VCO is equal to Equation 1.4, which is similar to the transfer function from the reference to the VCO output, except for the factor of $(2\pi f_{ref}/Ns)$ preceding it.

$$H_{cld}(s) = \left(\frac{2\pi f_{ref}}{Ns}\right)\frac{-K_{phi}K_vF(s)/s}{1 + K_{phi}K_vF(s)/Ns} \tag{1.4}$$

### *[1.3c] Example Simulated Spur Levels in Fractional-N PLLs*

While it is nice to have a theoretical analysis of the effects on the VCO output phase due to modulation of the frequency divider, it is also important to have quantitative examples of the implications of this analysis. This section will describe MATLAB code which takes a modulation signal (to represent changes in "N") and filters it in the frequency domain using the previously derived transfer function (Equation 1.4).

As a check, the program also implements an algorithm to derive the frequency domain VCO output using a comparison between accumulated phase of the reference signal and accumulated phase of the frequency-divided output signal which represents the phase error seen at the PFD. This phase error is converted into a charge pump current and convolved with the inverse Fourier transform of the transfer function from the output of the PFD to the output of the VCO given by Equation 1.5. Note that the transfer function from the PFD to the VCO output is equivalent to the transfer function between the reference and the VCO output except that it is divided by the proportionality constant relating phase error at the PFD inputs to current out from the charge pump ($K_{phi}$).

$$H_{clpfd}(s) = \frac{K_v F(s)/s}{1 + K_{phi} K_v F(s)/Ns} \tag{1.5}$$

In estimating phase error seen at the input to the PFD/CP, it is important to remember that phase accumulates over time. The phase of the reference signal can be calculated by summing up the phase change accumulated during each period of the reference signal. $2\pi$ of phase change occurs during one period of the reference signal, which is ($1/f_{ref}$) seconds long. Equation 1.6 describes the reference signal phase, where the summation counter k represents the immediate phase-comparison interval (cycle), and M is the total number of cycles up to the current time.

$$\theta_{ref} = \sum_{k=0}^{M} 2\pi k \tag{1.6}$$

The phase of the divided output signal can be calculated using a similar accumulation over reference periods. For this calculation, the phase of the divided output signal is accumulated, taking into account that the divided output frequency depends upon the denominator value "N". Equation 1.7 describes how the divided output phase accumulates over reference periods:

$$\theta_{div} = \sum_{k=0}^{M} \frac{2\pi k f_{ref}}{f_{out}/(N+\Delta N)} \quad (1.7)$$

Rearranging Equation 7 so that it is in terms of the reference frequency instead of the output frequency results in Equation 1.8:

$$\theta_{div} = \sum_{k=0}^{M} \frac{2\pi k(N+\Delta N)}{(N+F)} \quad (1.8)$$

where "F" is the average value of ΔN. With expressions for the reference and divided output phases in terms of the reference frequency, the output of the PFD can be calculated by subtracting the two quantities. Equation 1.9 annotates this phase difference ($\Theta_{error}$).

$$\theta_{error} = \sum_{k=0}^{M} \frac{2\pi k(F-\Delta N)}{(N+F)} \quad (1.9)$$

Assuming that F is small relative to N and ΔN, Equation 1.9 can be approximated as Equation 1.10.

$$\theta_{error} \approx -\sum_{k=0}^{M} \frac{2\pi k \Delta N}{N} \quad (1.10)$$

The summation in equation 1.10 can be represented by integration in the continuous time domain after taking into account the frequency at which the phase comparisons are performed. This approximate continuous time domain expression is given by Equation 1.11.

$$-\int_0^t f_{ref} \frac{2\pi\Delta N}{N} d\tau \quad (1.11)$$

where the factor $f_{ref}$ is introduced within the integrand to guarantee that (1.11) equal to (1.10) after M periods, each of length $T_{ref} = 1/f_{ref}$. The Laplace domain transfer function between a change in the instantaneous divider and the phase error, therefore, can be written as Equation 1.12:

$$\frac{\theta_{error}}{\Delta N}(s) = \frac{-2\pi f_{ref}}{Ns} \quad (1.12)$$

Equation 1.12 tells us how the frequency spectrum of the delta-N sequence is translated to spurious noise at the output of the VCO. The 1/s term indicates that it is critical to minimize content at low frequencies. This issue is addressed in the following chapter.

# CHAPTER 2 - Sigma Delta Modulation

Sigma delta modulators (SDMs) are used in digital-to-analog (D/A) conversion to achieve a high analog resolution with a small number of digital states. High resolution implies low quantization errors. SDMs achieve this by pushing quantization error to high frequencies and averaging the output using a low-pass filter. This technique is commonly called noise shaping [14]. In order to explain how noise shaping will be exploited in the design of a frequency synthesizer, a discussion of the application of sigma delta modulation in D/A conversion will be presented as background. The application of these circuits in frequency synthesizers will then be shown.

## [2.1] First-Order Accumulator D-to-A Implementation

The simplest implementation of an SDM is a digital accumulator or integrator. A block diagram of a digital accumulator or first order SDM is shown in Figure 2.1. Here, the output from the converter is a simple 1-bit value from the accumulator's carry signal.

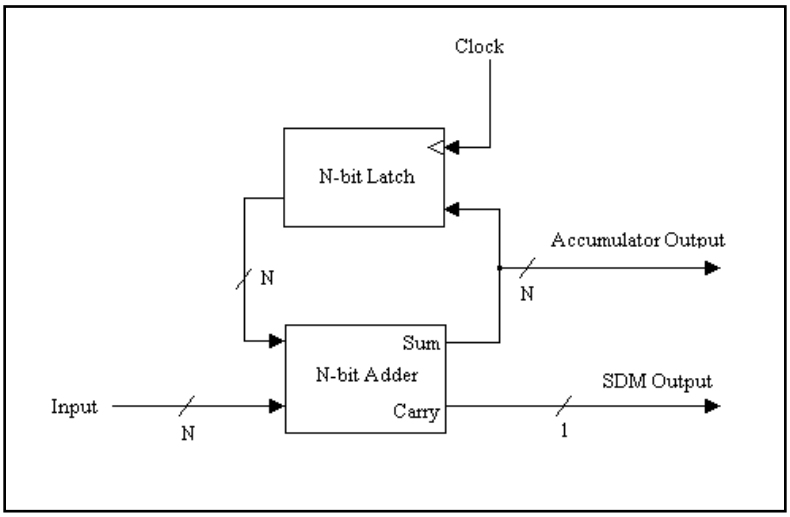


Figure 2.1: Digital Accumulator as Simple D-to-A

All digital accumulators have finite length. Finite length implies that there is a limit on the input value that the adder can operate upon and the sums it can accumulate. As an example,

a 10-bit adder could operate on values up to $2^{10}$–1 or 1023. When this limit is reached, the digital counter is reset and the carry bit is high for one clock cycle. Figure 2.2 illustrates what the accumulator (sum) and SDM (carry) outputs might look like for a 4-bit digital accumulator. In the case of a 4-bit digital accumulator, the accumulator output can be a maximum of 15.

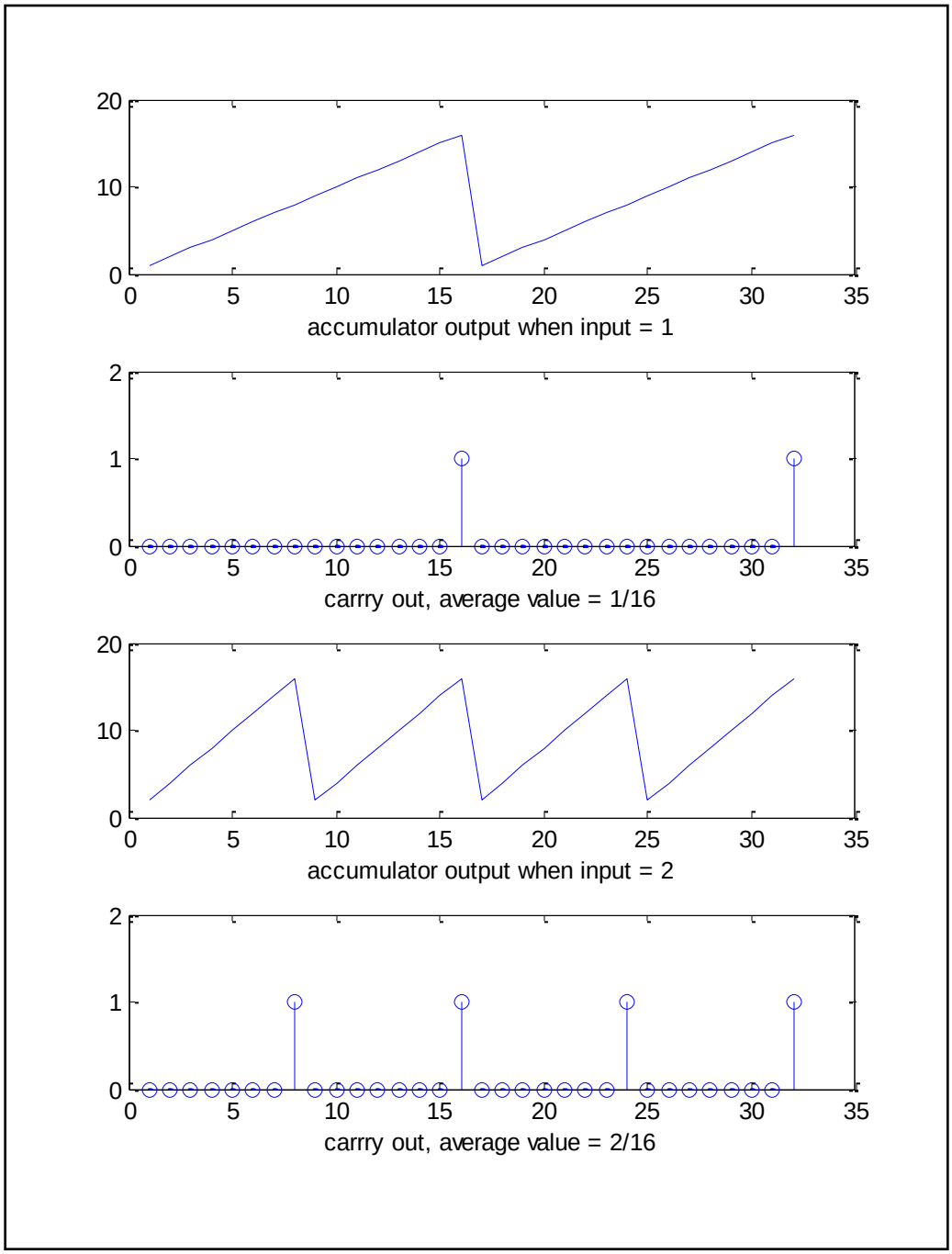


Figure 2.2: Accumulator and Carry Outputs from a 4-bit Digital Integrator

As illustrated in Figure 2.2, if the input to the accumulator is the lowest value it can be (1), the accumulator output will ramp by an increment of this value (1) with each clock cycle. When the accumulator output reaches the highest value it can (15), the accumulator resets on the next clock cycle and the carry bit is made high. Similarly, when the accumulator input is a higher value (2, for example) the accumulator output will increment by 2 with every clock cycle. If the accumulator output increments by 2 with every clock cycle, then the maximum value will be reached twice as fast as in the previous case where the input value was unity. Since the carry bit will be high every time the maximum is reached, a high carry will occur twice as often for an input of 2 than it would for an input of 1.

The reason that this simple digital accumulator can act as a D/A accumulator is based on the fact that the frequency of carry bits are directly dependent on the value of the input to the accumulator. The analog output can be represented by taking the average value of the carry over a long time scale. A long time scale, specifically, is an interval longer than several occurrences of 2^N clock cycles. For the 4-bit accumulator, for instance, the carry average would be meaningful if taken over a number of clock cycles greater than 4 or 5 times 16. Equation 2.1 equates the average carry value with the accumulator input, where $C_a$ is the average carry output, i is the accumulator input and N is the length of the accumulator [8].

$$C_a = \frac{i}{2^N} \tag{2.1}$$

In the 4-bit accumulator example (N = 4), if the input is unity, than the average carry output will be (1/(2^N)) or 1/16. If the input is 2, the average carry output will be 2/16.

Although the operation of a simple first-order accumulator-based D/A has been described for a constant input, it may not be clear to a reader who is unfamiliar with these devices how they can be used to convert digital *signals* into an analog representation. In the previous example, a

digital accumulator was used as a simple SDM with a constant (DC) input. Signals of interest are often not constant, but changing. Figure 15 illustrates what the output of a first-order SDM might look like (red) given a sinusoidal input signal (blue).

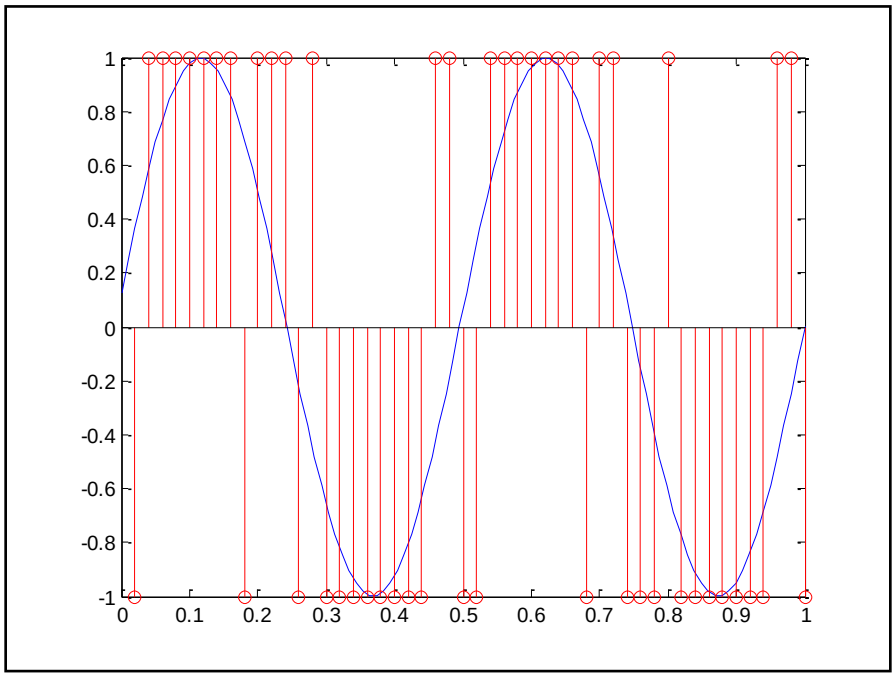


Figure 2.3: 1-bit SDM Input and Output

As shown in Figure 2.3, the average of the output of the SDM is proportional to the level of the input signal even though it is a single-bit representation of the input. This single-bit representation of a signal can be converted into an analog representation by low-pass filtering. In practice, as in many computer sound cards and audio capture devices, the SDM is clocked at a much higher rate than the sampling rate.

## [2.2] Noise Shaping with Sigma Delta Modulators

In addition to the desired analog signal in the output, quantization-error noise will also exist. Z-domain analysis of a first-order sigma delta modulator shows that the quantization error noise spectrum is shaped by the transfer function given in Equation 2.2 [12].

$$H_n(\mathrm{Z}) = 1 - Z^{-1} \tag{2.2}$$

In order to show how Equation 2.2 was derived, the first order modulator can be rearranged into a block diagram as illustrated in Figure 2.4, where the carry output is generated from the accumulator output and a source representing quantization noise. While the accumulator output is increasing, the carry out bit is low (corresponding to a zero value) so the quantization noise source represents the difference between the zero output and the desired average accumulator output value. When the accumulator overflows, the quantization noise is the difference between 1 and the average output. Thus, the quantization noise has a magnitude between zero and unity and is constantly changing. It can be represented statistically as a white noise source [11].

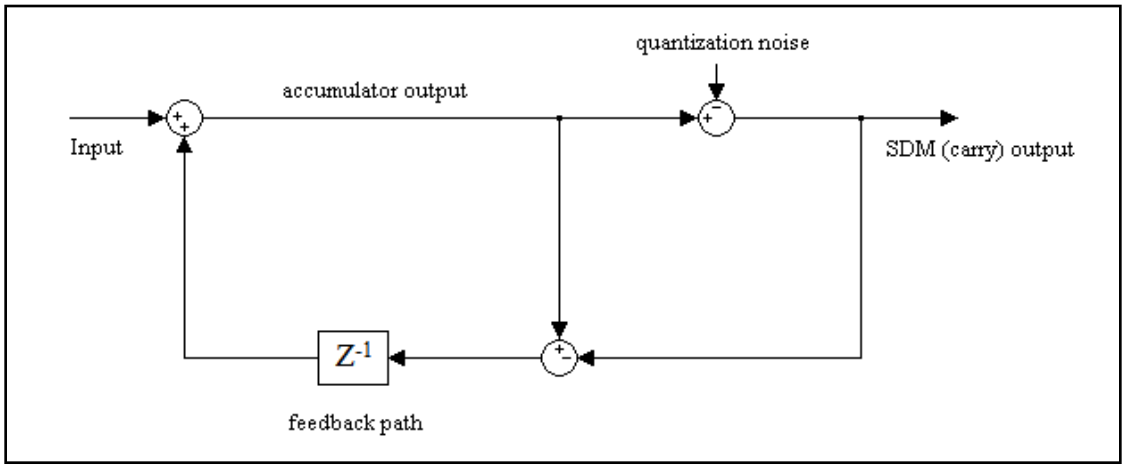


Figure 2.4: Quantization Noise Model for 1st-Order SDM [12]

The transfer function in Equation 2.2 has a single-pole high-pass response. When a MASH (Multi-Accumulator noise SHaping [12]) sigma delta modulator is used, the order of a SDM can be increased to add poles to this response. Figure 2.5 illustrates a 2nd-order MASH SDM [11], where the clock signal has been abstracted out to make the figure easier to interpret. Each of the blocks in Figure 2.5 labeled "∑Δ" represent the equivalent of the block diagram in Figure 2.4. The quantization error from this modulator is shaped by a two-pole high-pass

response. The second-order modulator is also different from the first-order modulator in that it has a three-bit output.

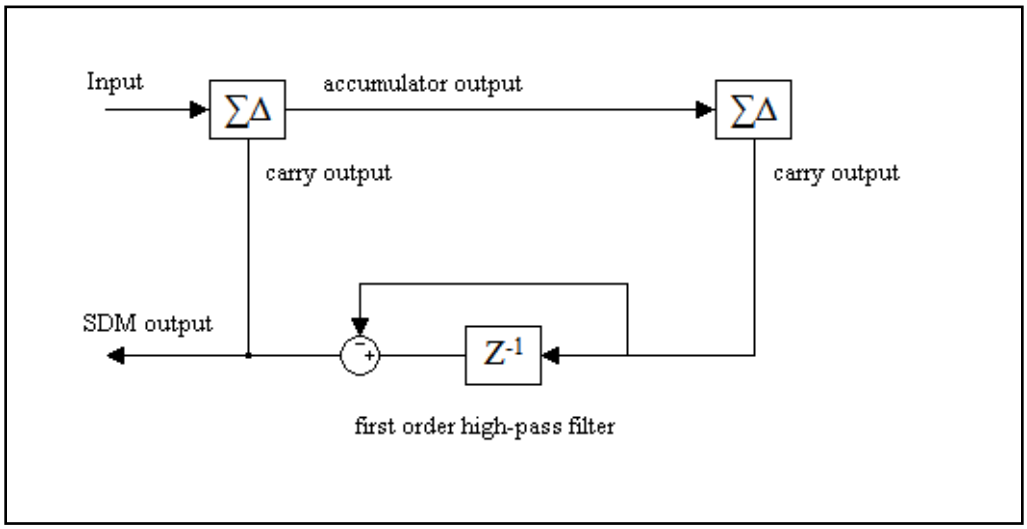


Figure 2.5: 2nd-Order MASH SDM Block Diagram

In general, the quantization error in an N$^{th}$-order SDM is transferred through an N-pole response before reaching the output of the modulator. Figure 2.6 illustrates a 3$^{rd}$-order MASH SDM, exhibiting by a 3$^{rd}$-order noise transfer function and a 5-bit output. A 4$^{th}$-order MASH SDM has a 4-pole noise transfer function and a 9-bit output.

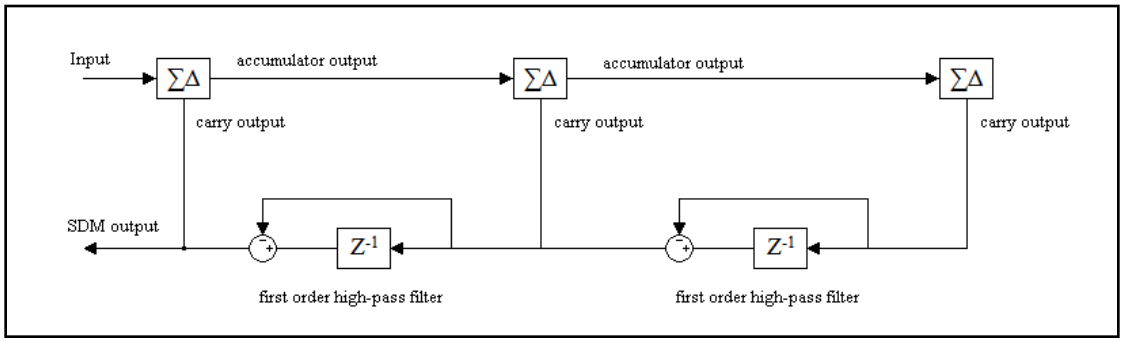


Figure 2.6: 3rd-Order MASH SDM Block Diagram

Equation 2.3 annotates the Z-domain representation of such an N-pole high-pass response.

$$H_N(z) = (1 - z^{-1})^N \tag{2.3}$$

Since the quantization error from a SDM is treated with a digital high-pass filter operation and the output must be low-pass filtered in order to represent the input signal, quantization error at both low and high frequencies is effectively attenuated. Furthermore, by running the SDM at a higher rate than the actual sampling rate and using a $4^{th}$ or $5^{th}$-order SDM, significant suppression of quantization noise in D/A conversion can be achieved.

## [2.3] SDMs in Fractional Frequency Synthesis

Frequency synthesizers use digital counters to divide frequencies and thus generate an output at a multiple of a crystal-controlled reference frequency. As stated earlier in this document, these circuits can only divide by integer numbers because they are implemented using digital counters.

A sigma delta modulator can be used to change the value of the frequency division so that, over time, the frequency is effectively divided by an average value that is fractional rather than integer. As noted in Equation 2.1, if a first-order SDM is given a constant input, then the average value of the output will be equal to the input divided by the maximum value that the digital circuitry can operate on. By dithering the number the divider counts to in a synthesizer, an integer divider can be made to divide by a fractional value equal to the average of each of the varying division values used. The resolution of these fractional values is determined by the length of the accumulators making up the SDM. A synthesizer using a 10-bit SDM and a 10MHz reference, for example, would have a frequency resolution of 10MHz divided by 2^10 or about 977Hz, whereas an additional five bits of accumulator depth would provide a frequency resolution of 15Hz.

To overcome the spurious signal generation problem illustrated in Chapter 1, a fractional frequency synthesizer can exploit noise shaping in a MASH SDM in a similar way that analog to

digital conversion utilizes this behavior. In a typical frequency synthesizer the low-pass filtering operation is carried out on the quantization noise by the loop filter.

## [2.4] MATLAB Simulation of a 3rd-Order SDM

Simulation of a 3rd-order, 10-bit SDM was carried out using MATLAB. Figure 2.7 illustrates the time-domain output from this system given an input of a constant value of 500.

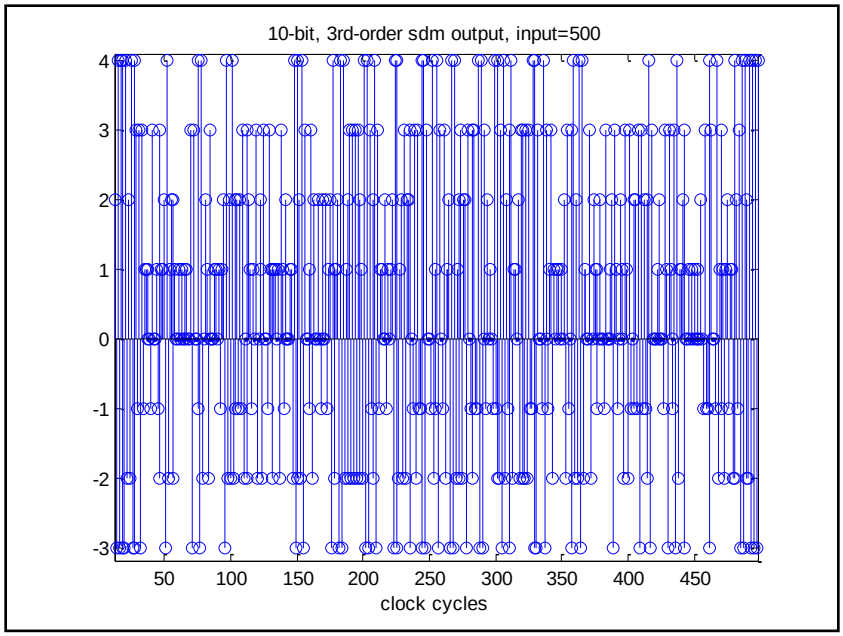


Figure 2.7: Simulated 10-bit, 3rd-Order SDM Output

Since this is a representation of the output of a 10-bit SDM with an input of 500, the average value of this signal taken over more than (2^10) or 1024 clock cycles should be equal to 500/(2^10) or 0.4883. Code was written to numerically determine the average value of this signal and it comes out to 0.4883 (the average was taken over 10,000 clock cycles).

Since the average value of this signal represents what the output should be based on the input and this signal only takes on discrete values from -3 to 4, this signal represents the quantization error plus the desired constant offset. This signal, therefore, should display a 3-pole

high-pass shape in the frequency domain (see Equation 2.3). Figure 2.8 illustrates the frequency domain representation of this signal, found by taking the FFT of Figure 2.7.

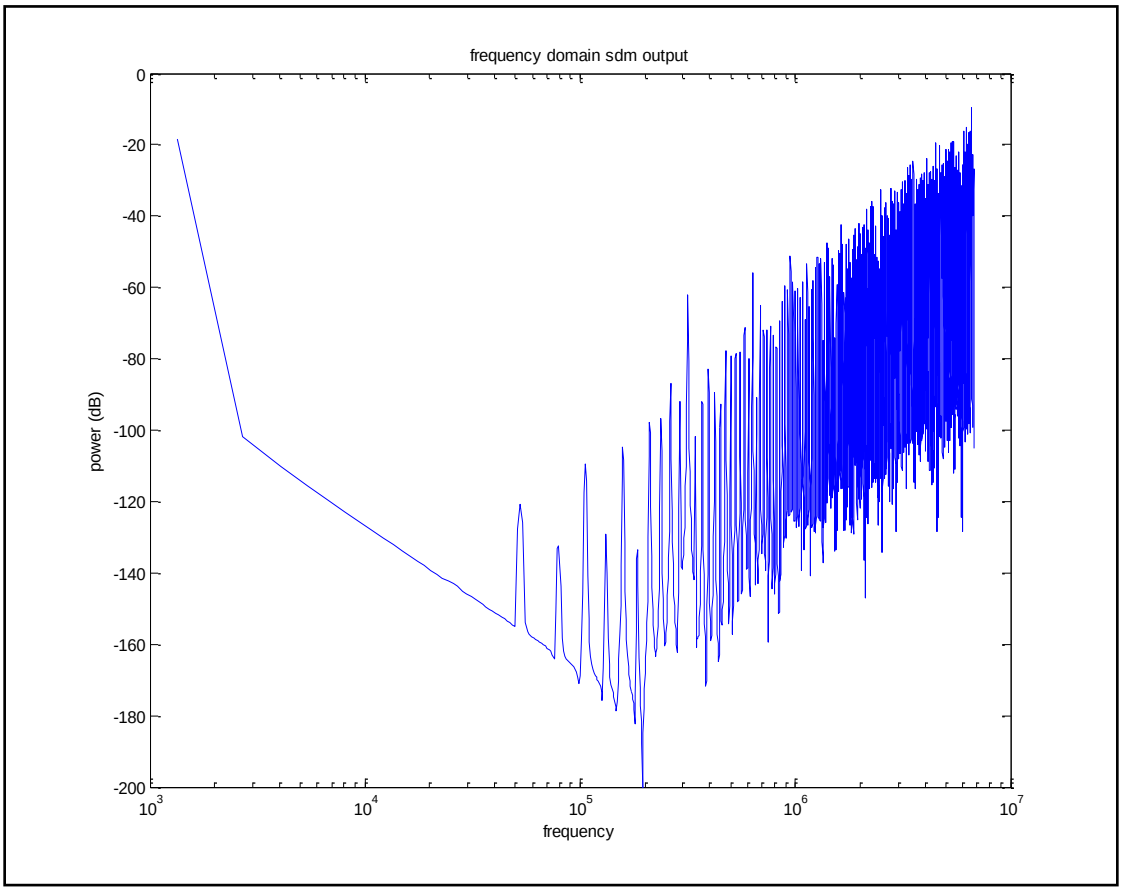


Figure 2.8: Frequency Domain Representation of 10-bit, 3rd-Order SDM Output

Note that this representation displays a high-pass shape (besides the lines to the left of the figure, which are artifacts of the FFT due to DC offset). Furthermore, from 100KHz to 1MHz, there is a -30dB difference, corresponding to a 3-pole slope.

To summarize this discussion of sigma delta modulators and how they can be used in fractional frequency synthesizers, the SDM provides density-modulated high frequency representations of fractional numbers. These signals are desirable for frequency synthesis

because high-frequency noise can be filtered out by the loop filter while low frequency noise has been suppressed by the noise transfer function in the SDM.

## [2.5] MATLAB Simulation of Spectral Spreading Caused by Non-Linearities

Spectral spreading has been mentioned as an effect that can degrade noise performance in frequency synthesizers, but a clear explanation of how non-linear conversions lead to spectral spreading has not been presented. A non-linearity was introduced to the time domain signal illustrated in Figure 2.7, where the positive numbers were amplified by a different amount than the negative numbers. This non-linearity would be similar to the mismatching effect seen in charge pump circuits as discussed in Section 3.2c. The FFT was then taken of the signal to generate Figure 2.9. Figure 2.9 illustrates the effect of "10 percent" asymmetry, where positive values from the SDM are amplified by 1.1 and negative values are amplified by unity. Comparison of Figure 2.9 with Figure 2.8 illustrates that this small amount of gain asymmetry can result in significant degradation to the desirable noise shaping characteristics that are exploited in frequency synthesis by using MASH accumulators.

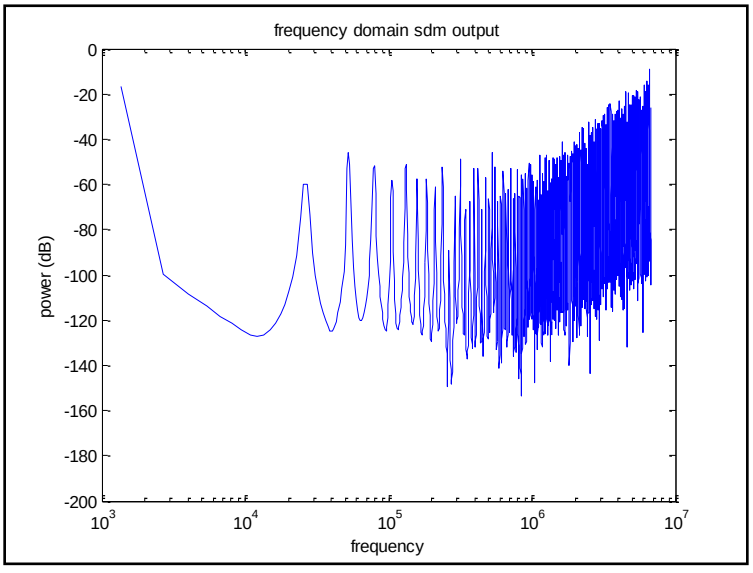


Figure 2.9: 10-bit, 3rd-Order SDM Output after 10 Percent Asymmetry

### *[2.5a] Simulation of Spurious Tones in a SDM-based Synthesizer*

Figures 2.10 and 2.11 are calculated frequency domain representations of spurious levels in dBc (dB relative to the carrier or desired output signal) at the loop output due to divider modulation for the case of a 3$^{rd}$-order sigma-delta delta-N. Figure 2.10 was generated using a modulation signal (whose frequency domain representation is illustrated in Figure 2.8) and the transfer function from frequency divider modulation to VCO output phase (as derived in section 1.3c). Figure 2.11 was generated using estimation of phase error and charge pump current and the transfer function from the charge pump to the VCO output. Note that Figures 2.10 and 2.11 are similar in terms of magnitude and frequency of spurious tones.

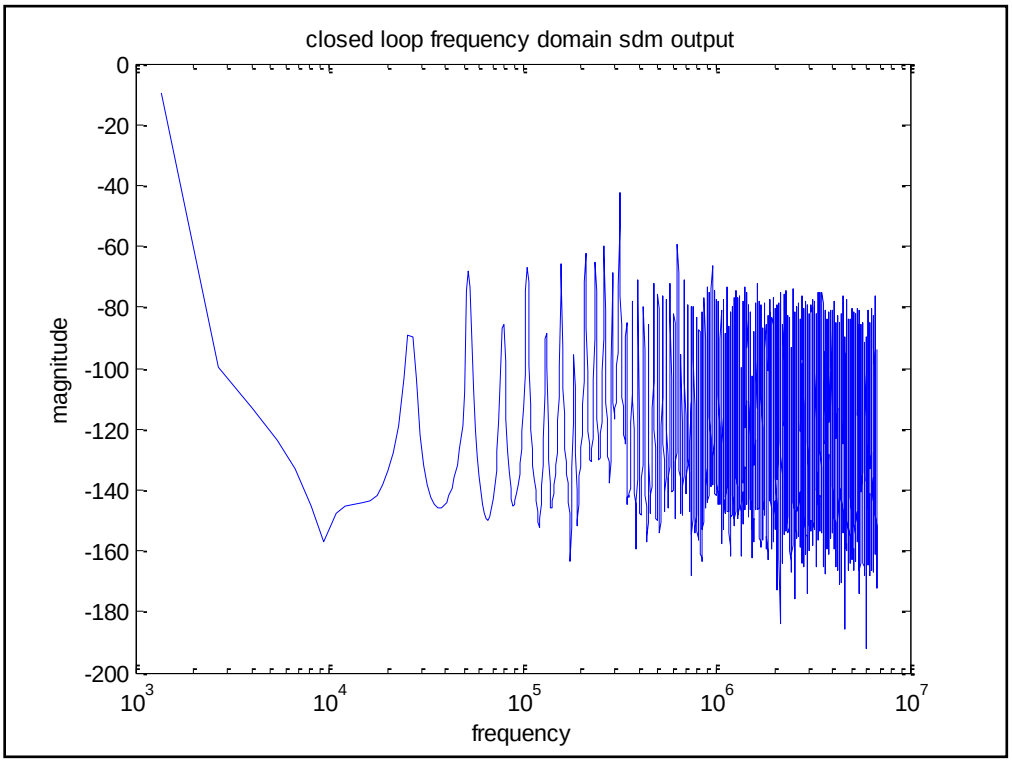


Figure 2.10: Spurious Content of VCO Output Due to N Modulation

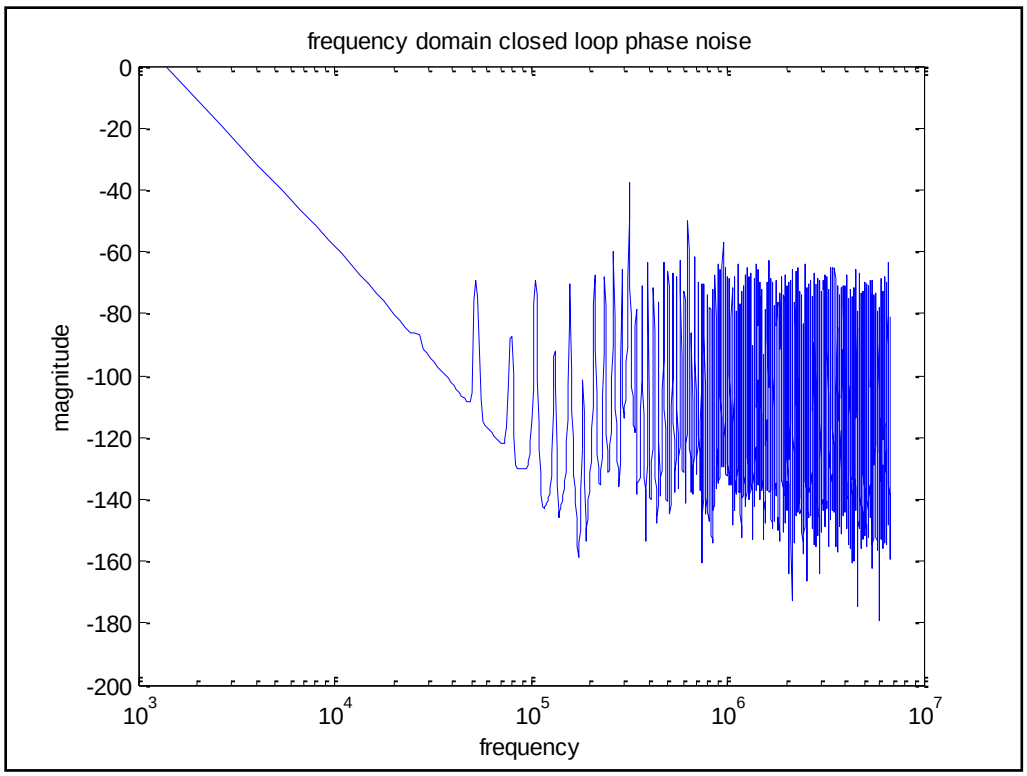


Figure 2.11: Spurious Content of VCO Output Due to N Modulation (Alternate Method)

Note that these plots represent ideal spurious content in that there are no non-linearities modeled in the loop. If such defects are present, the simulated spurious tones can be as high as -20dBc for a 10 percent gain mismatch at the charge pump.

# CHAPTER 3 – Phase-Frequency Detectors and Charge Pumps

Since non-linearities in a system can cause folding of tones from one region of a spectrum to another (e.g. from the high-noise high-frequency region into the low-noise, low-frequency region), linearity is very important in SDMs and fractional-N synthesizer implementations. There are two conversions which take place in a frequency synthesizer which should be made as linear as possible in order to achieve the lowest possible phase and spurious noise. One of these conversions is at the VCO (voltage controlled oscillator) where a control voltage at the loop filter is turned into a frequency at the synthesizer output. The other conversion is at the PFD/CP (phase frequency detector / charge pump) where a difference in phase between the divided output signal and the reference signal is converted into a charge to be deposited on the loop filter. This section will describe the latter conversion and what the two main challenges are in making this conversion as linear as possible.

## [3.1] PFD (Phase-Frequency Detector) Basics

A phase frequency detector is a mixed-signal circuit that uses digital logic circuits (flip flops and gates) to convert the phase difference between two signals into a width-modulated signal representing that phase difference [6]. In the synthesizer described in this document, digital output from the PFD controls a charge pump. Some synthesizers employ PFDs which have an analog voltage output and these designs negate the need for a charge pump. Figure 3.1 illustrates a basic PFD circuit, similar to the one used in this synthesizer.

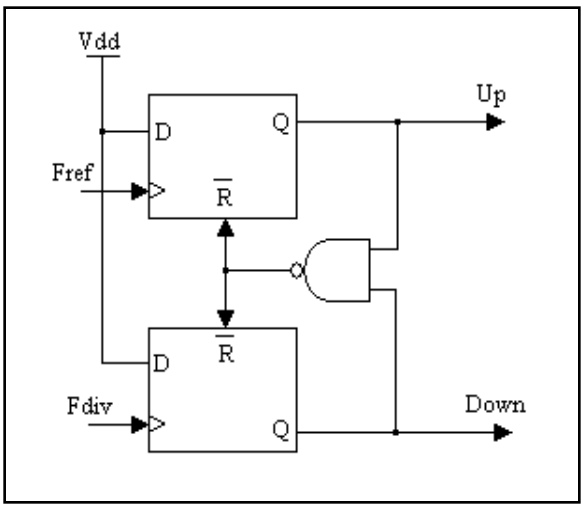


Figure 3.1: Basic PFD Circuit [13]

To get an understanding of the operation of this circuit, let us assume that the inputs labeled $F_{ref}$ and $F_{div}$ represent the reference and the divided output frequencies. Let us also assume that the outputs of the flip flops are initially low.

If the outputs of the flip flops are low, then the output of the NAND gate will be high. If the NAND gate output is high, then the flip flops will not be in reset mode and their outputs will remain low.

Now let us suppose that a rising edge occurs in the signal representing $F_{ref}$. Since the input of the flip flop driven by this signal is tied high and the flip flop is not in reset, its output will become high on the rising clock edge from $F_{ref}$. If a rising edge on the clock input to the other flip flop occurs shortly thereafter, the output to that flip flop will go high and the NAND output will become low because it has two high signals at its inputs. When the NAND output becomes low, the flip flops will be reset.

The desired effect of all of this is that the "Up" output will put out a pulse whose duration is proportional to the amount of time that the divided output lags the reference signal. This "Up" pulse will cause the charge pump to output a positive current for that amount of time and this will increase the voltage on the loop filter. When the loop filter voltage increases, the VCO

output frequency will increase and, assuming the frequency does not increase too much, the lag between the divided output and the reference signal will decrease.

Similarly, it can be seen that if the limited divided output signal issues a positive edge before the reference signal, a “Down” pulse will result. This “Down” pulse will have the effect of decreasing the frequency of the output and, again assuming the frequency is not changed too much, the divided output signal will slow down and the lag or phase difference between the two signals of interest will decrease.

The actual phase frequency detector used in the synthesizer described in this thesis is illustrated in Figure 3.2.

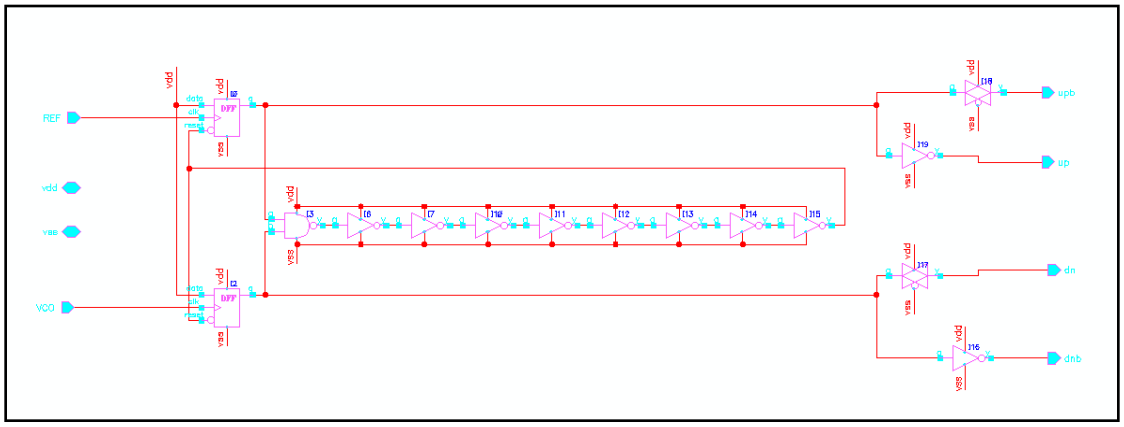


Figure 3.2: PFD Schematic

Aside from the naming conventions used on the input and output nodes, Figure 3.2 exhibits a couple of key differences from the simple PFD circuit explained earlier (Figure 3.1). First of all, the “Up” and “Down” outputs (as they were annotated earlier) are each taken through an inverter and a transmission gate. The transmission gate is simply there to minimize any time delay between the inverted and not-inverted versions of the outputs. The inversions are necessary to support the charge pump circuitry, which will be explained in the *Charge Pump* section.

The other key difference between the circuit in Figure 3.2 and the circuit in Figure 3.1 is that a chain of inverters exists between the NAND output and the resets of the flip flops. This inverter chain acts as a digital delay to make sure that the "Up and "Down" pulses coming from the PFD are not too short. The reason for this delay will also be described in the *Charge Pump* section below.

## [3.2] Charge Pumps in Frequency Synthesis

In order to address some of the PFD issues noted in the previous section, a basic understanding of what a charge pump does in a frequency synthesizer must be imparted. Figure 3.3 illustrates how an ideal charge pump could be connected to the basic PFD circuit presented in Figure 3.1. This CP is ideal in the sense that we assume there are no delays in the switches involved.

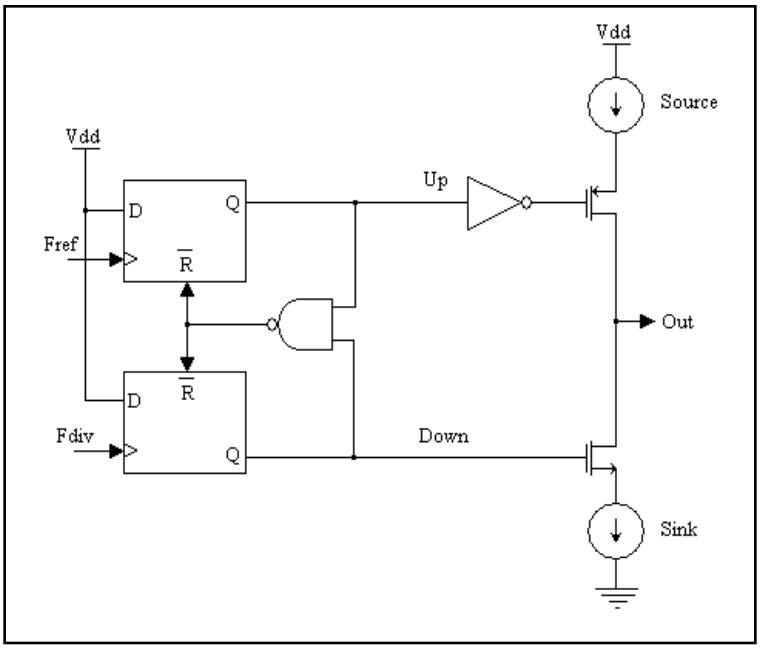


Figure 3.3: Ideal Charge Pump and PFD [6]

According to this idealized topology, when "Up" is high and "Down" is low, the PFET switch would be on and the NFET switch would be shut off. Thus current would flow into the

node labeled “out”, which would be connected to the loop filter in a synthesizer. When “Up” is low and “Down” is high, current would be pulled from the node labeled “out” and the loop filter.

### *[3.2a] Practical Charge Pump*

In practice the idealized topology in Figure 3.3 would not be practical because real current sources cannot be turned on and shut off instantaneously. This is why complementary representations of the “Up” and “Down” signals need to be generated, as in the circuit illustrated in Figure 3.2. Figure 3.4 illustrates a charge pump topology that is employed in the synthesizer. This circuit topology is one which addresses the issue of finite current source starting times. Without employing techniques such as those of Figure 3.4, FETs within the current source and sink circuits would enter the triode region of operation and fail to immediately output the desired current values when called on to do so.

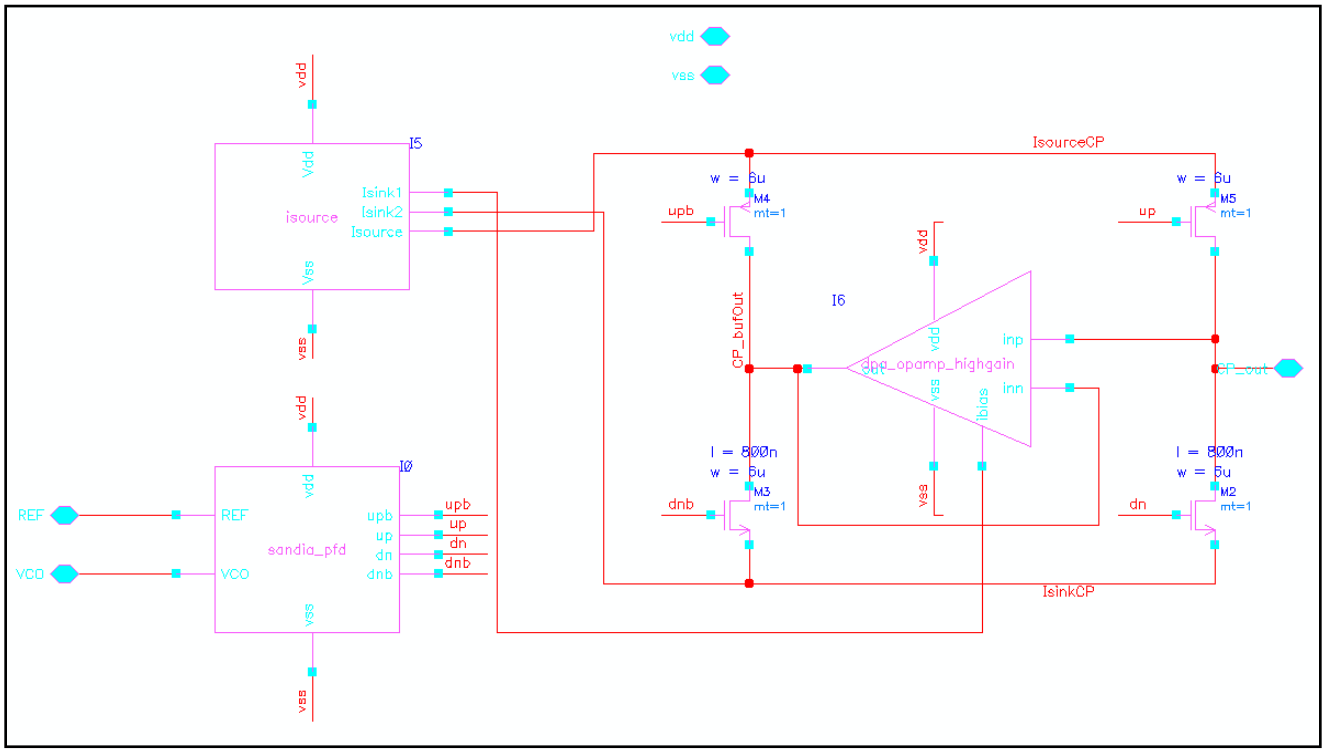


Figure 3.4: Practical Charge Pump Topology

In this circuit, the current source (represented by the block “isource”) is always sinking and sourcing current, and its FETs remain in the active region at all times. When “Up” is high, “up” is low and “upb” is high. Thus the PFET switch on the right is on and the PFET switch on the left is shut off. When the charge pump is sourcing current to the loop filter, “Down” is low and the node “dn” is also low and the node “dnb” is high. Thus the right NFET switch will be off and the left NFET switch will be on. Current for the IsourceCP sink node flows from the op-amp output.

Similarly, when the charge pump is pulling current from the loop filter in order to lower the control voltage on the VCO, the current will be pulled from the node CP_out through the right NFET switch into IsinkCP. The current source will still provide current into IsourceCP through the left PFET switch into the output of the op-amp.

When “Up” and “Down” are both low, the charge pump circuit will neither source current to nor pull current from the loop filter. The current sink and current source will still operate, however, because the left NFET and PFET switches will both be on. Therefore, under all three conditions (when the charge pump supplies the loop filter with current, when the charge pump pulls current form the loop filter, and when the charge pump neither pulls or supplies current from or to the loop filter), the current source and sink supplying the charge pump will remain in the active region and no switching-time problems will occur. Moreover, since the op-amp holds node CPbufOut at the same voltage as the loop filter, there are no voltage variations on the current source source and sink terminals, further minimizing any switching delays.

### *[3.2b] The Dead Zone Effect*

Although the above circuit solves problems of delays associated with the current-source/sink block, there are still time delays associated with the turning on and shutting off of a

FET switch. This becomes a problem in the PFD/CP of a frequency synthesizer when the phase difference between the reference signal and the divided output signal becomes very small [5]. In this case, the "Up" and "Down" pulses from the PFD become very short and the switches in the charge pump do not have enough time to switch on and supply current to or pull current from the loop filter. The dotted line in Figure 3.5 illustrates the ideal relationship between charge deposited on the loop filter and phase difference at the PFD input.

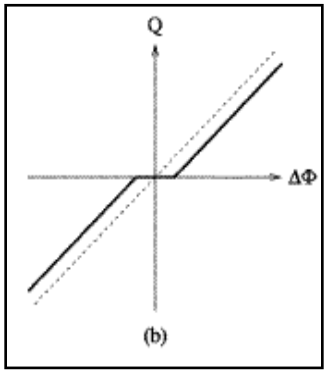


Figure 3.5: Dead Zone Effect [4]

As stated earlier, the ideal conversion between phase the difference at the PFD input and charge deposited on the loop filter is perfectly linear. Due to finite FET switching times, however, a "dead zone" effect can be observed in real charge pump circuits as illustrated by the solid line in Figure 3.5.

This effect is the reason for the chain of inverters in the PFD between the NAND gate output and the reset inputs of the flip flops. This chain of inverters acts as a digital delay so that a change in the NAND output will take some time to propagate to the flip flop resets. This delay ensures that the pulses coming from the PFD will not be too narrow for the FET switches in the charge pump, even if the reference signal and the divided output signal are very close together in phase.

To see how this delay would ensure minimum pulse duration from the PFD, the case where the reference signal provides a rising edge to the PFD very shortly before the divided output signal does could be considered. The output of the "Up" flip flop will become high, creating no change on the NAND gate output. Soon after, the "Down" flip flop output will also turn high because this flip flop has also received a rising clock edge. The output of the NAND gate will now change to low, but this change will not reach the resets of the flip flops until it has gone through the chain of inverters. Since the resets will not be toggled for the duration of the journey through the inverter chain, the "Up" and "Down" outputs will be high for this amount of time. Thus the "Up" and "Down" pulses will have a minimum duration equal to the delay introduced by the chain of inverters. The actual charge imparted to the loop filter however, will still be correct, since it is a function of the *difference* of the durations for which the N and P devices are on.

### *[3.2c] Mismatching*

An additional effect that can degrade the linearity of the conversion from phase difference to charge carried out by the PFD/CP is mismatch in the sourcing and sinking currents [7]. Ideally we would like the magnitude of the current pulled from the loop filter to be equal to the current supplied to the loop filter. In CMOS processes, however, the output resistance of FETs can create mismatches in the source and sink currents that depend on the loop filter voltage. This can make it difficult to design a current source that is perfectly matched to a current sink. Figure 3.6 illustrates the effect that mismatching can have on the linearity of the conversion from phase difference to charge. This problem is typically addressed by use of long-channel devices and/or cascading techniques within the current source circuits.

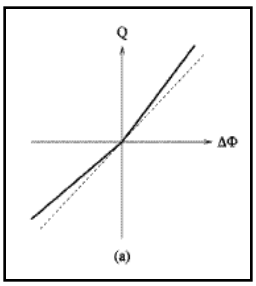


Figure 3.6: Mismatching Effect [4]

This mismatching effect is not explicitly addressed in the charge pump topology illustrated in Figure 3.4. An alternate charge pump topology is illustrated in Figure 3.7, where the sink and source currents are generated by identical circuits and the sink current is mirrored from a source current to the output via an NFET mirror [ref]. Since the sink and source current circuits are identical and it is practical to expect to NFETs to be closely matched, assuring accurate current mirroring, the sink and source currents generated by this topology should be very close to one another.

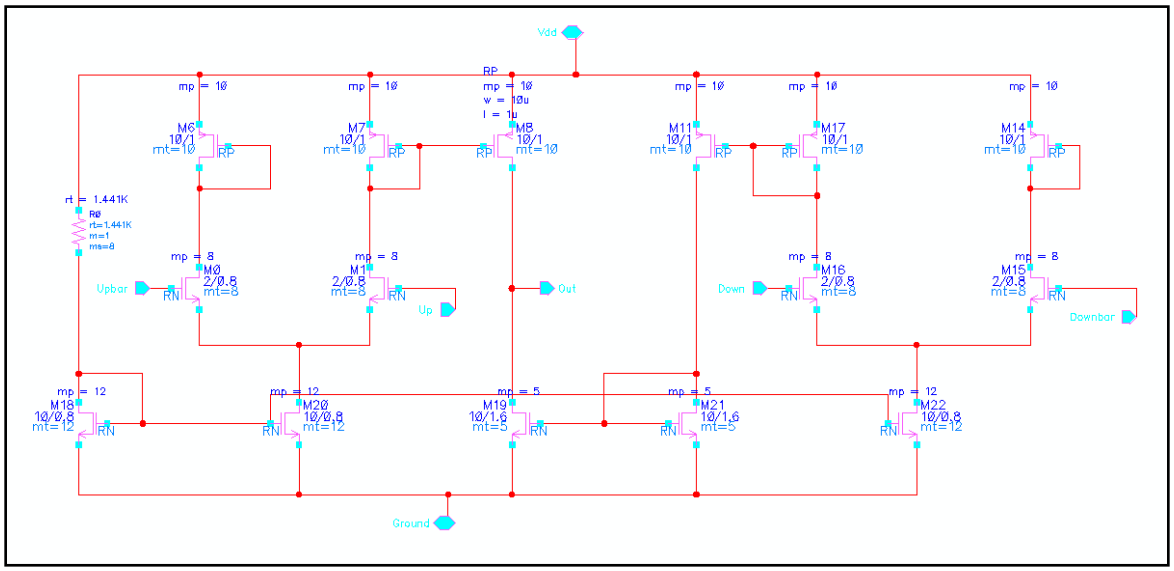


Figure 3.7: Alternate Charge Pump Topology 1

### *[3.2d] Device Noise and FET Gate Area*

In addition to introducing non-linearity into the loop in the conversion from phase to charge, the charge pump circuit also introduces active device noise into the synthesizer. The noise added by the active circuitry that we are most concerned with is low-frequency noise because high-frequency noise will be suppressed by the loop filter. Low frequency noise in FETs is usually dominated by so called flicker or 1/f noise. This noise, in addition to being inversely proportional to frequency, has been shown to be inversely proportional to the gate area (W*L) [1,3]. The penalties for an increase in gate area are increased size and an increase in gate capacitance which results in reduced switching speed [1]. With the previously mentioned imposed minimum delay seen by the PFD, switching times of up to about 500ps can be tolerated.

In order to test the proportionality between device noise added by the charge pump and gate area, two versions of the same charge pump topology were fabricated. These two versions differ only in the gate area. The width-to-length ratios were kept the same so that the two charge pumps have the same conversion gains and the loop bandwidth of the synthesizer is unaffected (see section 4.1). Figure 3.8 displays this topology [4].

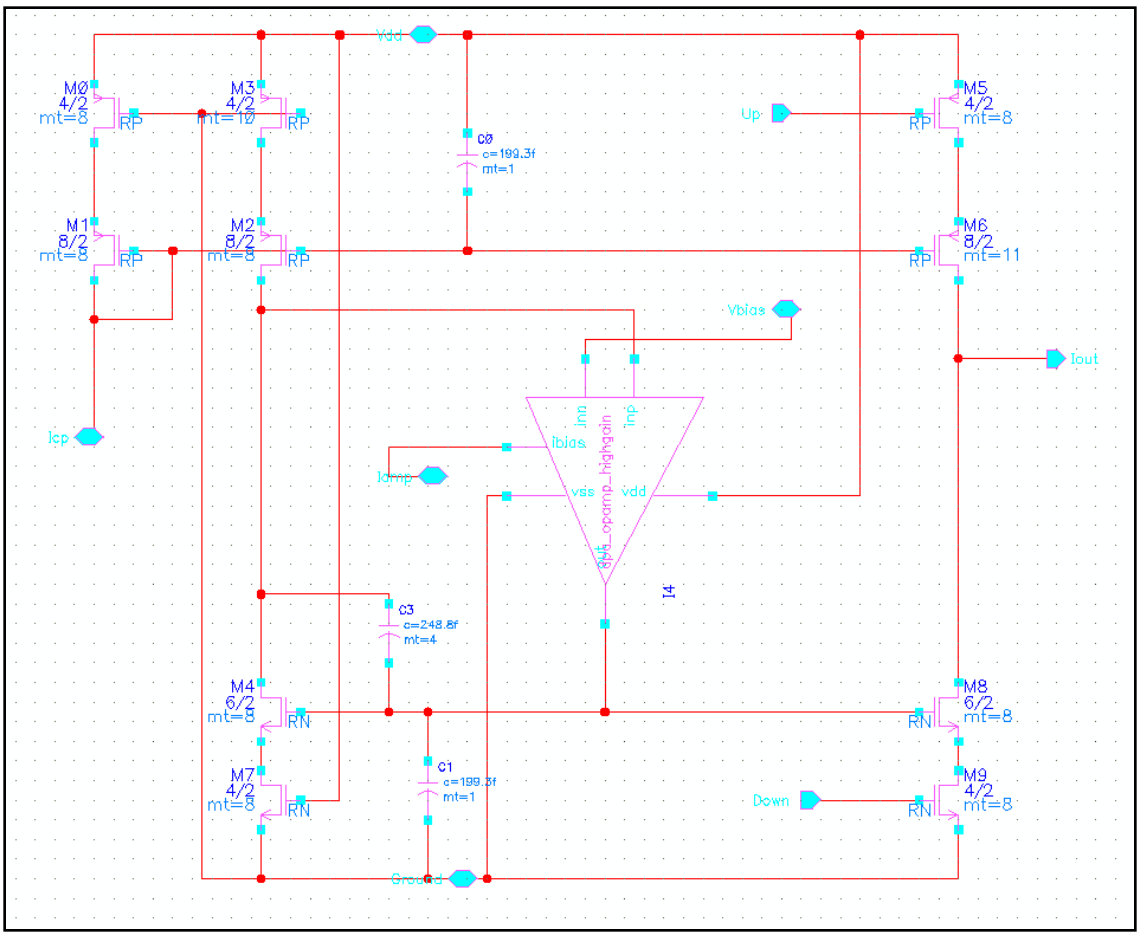


Figure 3.8: Alternate Charge Pump Topology 2 [4]

This topology is similar to the topology in Figure 3.4 in that the op-amp ensures that no rapid fluctuations in load are imposed on the current source and sink driving the charge pump. It was taken from [4]. The orientation of the amplifier may be confusing, particularly in that it appears to employ positive feedback (because the positive input is indirectly connected to the output). This is not the case, however, because M4 acts as an inverting common-source amplifier between the positive input of the op-amp and the op-amp output.

The capacitor C3 acts to compensate the effective op-amp that has been created to ensure adequate phase margin. The transistors M3 and M7 act as resistors to counter the impedance of M5 and M9 when they are switched on by the PFD. The capacitors C0 and C1 act to supplement

the action of the “shock absorbing” capacitor in the loop filter, whose operation is explained in section 4.1.

# CHAPTER 4 – Loop Filter Theory and VCO Phase Noise

There are many types of loop filters, including passive and active, but the common function of all loop filters in frequency synthesizers is to provide averaging of the PFD/CP output. The averaging function is essential to smooth out the pulsed signal from the PFD/CP so that the control voltage seen by the VCO does not vary rapidly, causing phase jitter and spurious tones at the VCO output.

As mentioned in Chapter 3, some PFDs convert phase and frequency differences into voltages which can be acted on by active or passive loop filters. The PFD in the synthesizer developed in this project sends digital signals to a charge pump circuit, which outputs current pulses of varying duration. The loop filter in this synthesizer, therefore, must convert the current pulses from the charge pump into a control voltage to drive the VCO. This conversion necessitates a capacitor-based integration operation so that the current pulses can be translated into voltage levels proportional to the pulse duration.

## [4.1] Second-Order Loop Filter

The low-pass filtering, current-to-voltage conversion and integration can all be achieved by the circuit illustrated in Figure 4.1. While this circuit only contains a single pole, it is still called a second-order filter when used in PLLs because there is an additional pole added by the loop due to the integration when converting phase to frequency at the VCO.

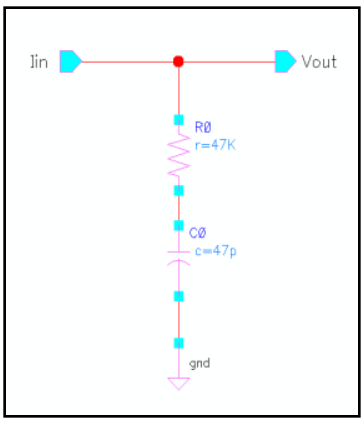


Figure 4.1: 2nd Order Passive Loop Filter Schematic

Using Ohm's law (V = IZ), the transfer function of this circuit can be determined by the series combination of the impedance of the capacitor and resistor. The transfer function for a passive 1st-order loop filter is given in Equation 4.1.

$$F(s) = \frac{V_{out}}{I_{in}} = R + \frac{1}{sC} \tag{4.1}$$

Equation 4.1 can be substituted into Equations 1.3 and 1.4 to determine the transfer functions from the reference to the output and the divider modulation to the output given a specific loop filter. Figure 4.2 illustrates the magnitude response from the reference to the output using a second-order loop filter. The pass-band gain of the closed-loop response is equal to N.

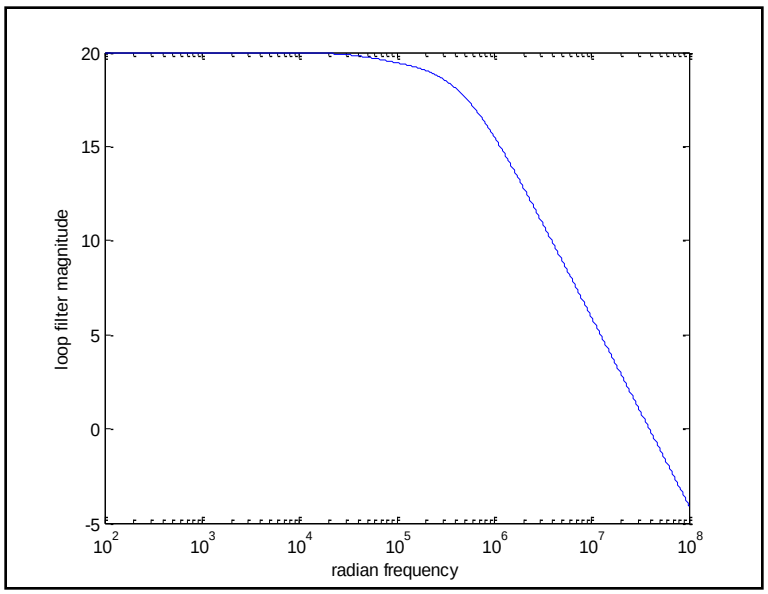


Figure 4.2: PLL Closed-loop Magnitude Response with Second-Order Loop Filter for N = 20 and a 1MHz Loop Bandwidth.

Although this result is for a second-order loop, this transfer function approximates a single-pole low-pass filter response due to the existence of a zero in the numerator of the overall response function. An important characteristic to note about this transfer function is that the -3db location, and thus the bandwidth of the synthesizer, is determined not only by the selection of the passive components in the loop filter, but also by $K_{phi}$ and $K_v$. If the magnitude of the charge pump current is altered, changing $K_{phi}$, then the loop bandwidth will also change. Figure 4.3 illustrates the inverse relationship between the loop bandwidth and charge pump current.

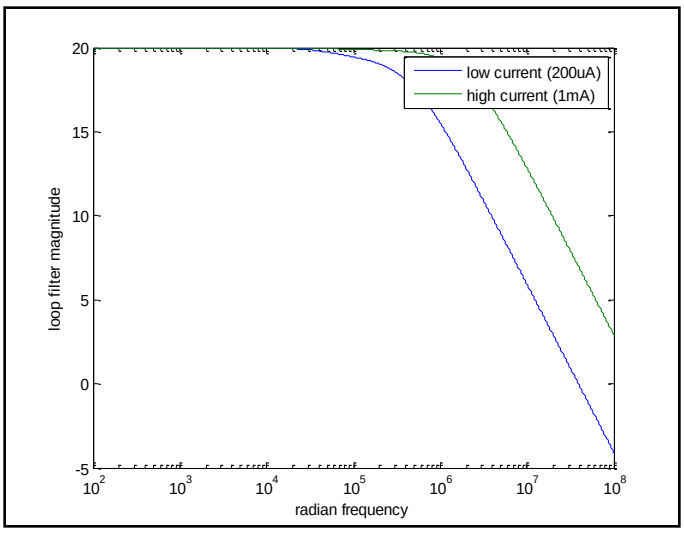


Figure 4.3: Inverse Relationship between Charge Pump Gain and Loop Bandwidth

## [4.2] Third-Order Loop Filter

One significant problem with the topology of the second-order loop filter is that the IR drop across the resistor will cause voltage spikes at the loop filter that are typically in excess of the VCO's linear range, especially for integrated synthesizers where this tuning range may be only a volt or two wide. As an example, let us assume that the capacitor is not charged so that the lower terminal (as shown in Figure 4.1) of the resistor is at a potential equal to ground.

When the loop filter receives a current pulse from the charge pump, all of the current will initially flow through the resistor. If the charge pump current is 200uA and the loop filter resistor is 47KΩ, then the voltage introduced by the resistor will be 200uA by 47KΩ which is 9.4V. Since the circuitry in our synthesizer is powered by 3.3V, 9.4V is clearly out of the linear range of operation for the VCO. This problem can be remedied by adding a second capacitor to the loop filter in order to absorb the charge from the current spike delivered by the charge pump.

The topology in Figure 4.4 represents a third-order loop filter, which mitigates the problem with the second-order filter topology discussed above.

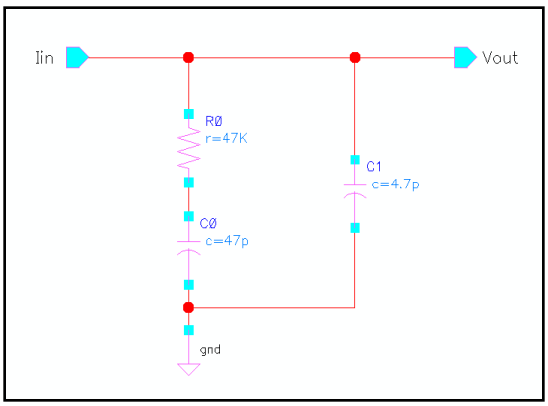


Figure 4.4: 3rd-Order Passive Loop Filter Schematic [10]

The capacitor $C_1$ acts to absorb charge during the beginning of the current pulse from the charge pump. In addition to providing this transient functionality, however, this capacitor also changes the frequency response. The frequency response of this filter topology is given in Equation 4.2.

$$F(s) = \frac{V_{out}}{I_{in}} = \frac{RC_0 + 1}{Rs(sC_1C_0 + C_0 + C_1)} \tag{4.2}$$

This response, when substituted into the loop transfer function, produces what approximates a 2nd-order low-pass filtering operation. Figure 4.5 illustrates this frequency response. It should be noted that stability considerations place significant constraints on the size of the capacitor and its ability to totally absorb the current spike. Typically the capacitor is limited to approximately 1/10th of the value of C0 [6]. Hence, for long current pulses, such as those delivered by a fractional-N loop design, the VCO may still see voltages spikes in the range of a volt or higher.

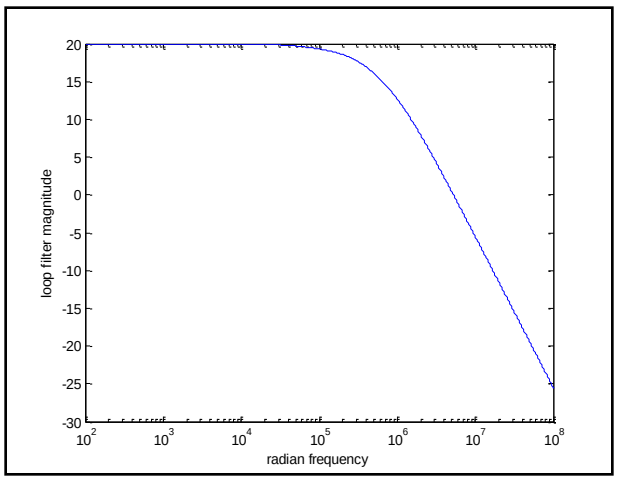


Figure 4.5: PLL Magnitude Response with 3rd-Order Loop Filter

## [4.3] VCO Phase Noise

As with the other active components in the loop (the divider and the PFD/CP), the VCO introduces phase noise which can be seen at the synthesizer output. In a synthesizer made in a MOS process, the VCO is in fact the main phase noise culprit due to large 1/f noise factors and limited Q in the VCO tank circuit. It is therefore important that we develop a Laplace domain mapping from VCO phase noise to the synthesizer output. Figure 4.6 represents the synthesizer block diagram with the VCO phase noise modeled as a source.

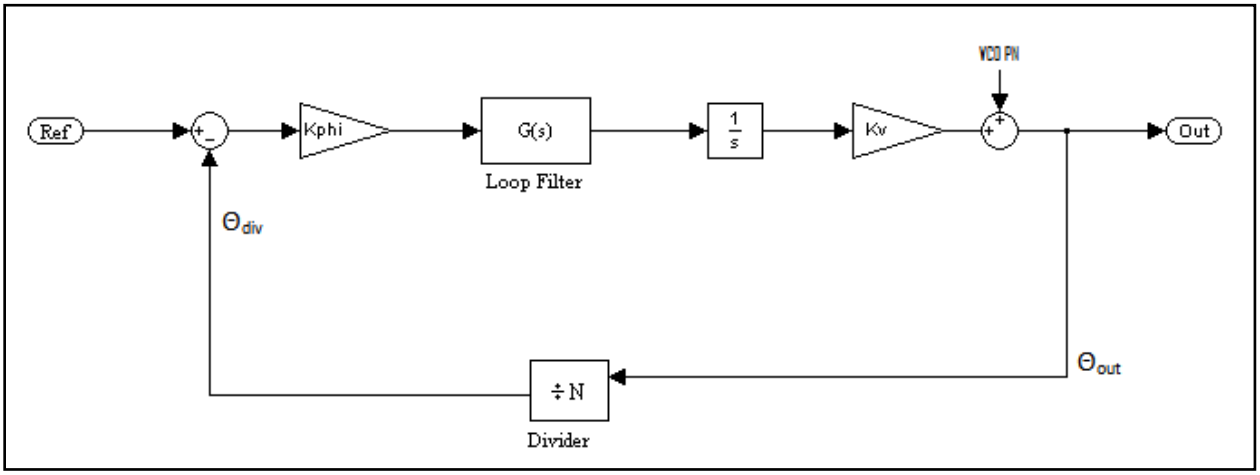


Figure 4.6: Synthesizer Block Diagram with VCO Phase Noise Source

### *[4.3a] Mapping from VCO Phase Noise to Synthesizer Output*

The mapping from modulation of the divider to the synthesizer output as described in Chapter 1 is similar to the mapping from the VCO output to the synthesizer output, except that the VCO phase noise is introduced before the output sample point instead of after it. This seemingly minor difference has a large effect on the overall result, changing the response function from a low-pass to a high-pass result. The block diagram presented in Figure 4.6 can be simplified by condensing the open-loop transfer function and assuming no phase noise from the reference. A simplified block diagram is presented in Figure 4.7.

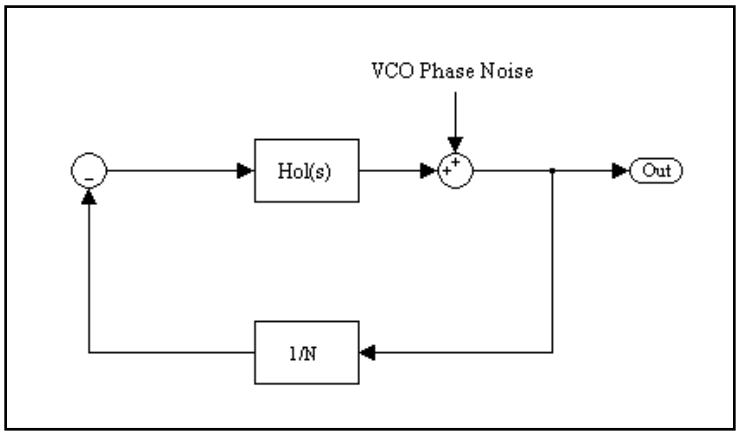


Figure 4.7: Modified Synthesizer Block Diagram with a VCO Phase Noise Source

Control system analysis on this loop shows that the transfer function from the VCO phase noise to the output is as described in Equation 4.3.

$$H_{clvco}(s) = \frac{1}{1 + H_{ol}(s)/N} = \frac{Ns}{Ns + K_{phi}K_v F(s)} \tag{4.3}$$

A very important consequence of this mapping is that, when the loop filter bandwidth is increased, the low-offset contribution to output phase noise from the VCO is decreased. This effect can easily be seen in the hardware by changing the loop bandwidth. Figure 4.8 illustrates this effect. This is the reason that the reference and loop bandwidth cannot be made arbitrarily low and the added complexity in a fractional-N synthesizer is necessary.

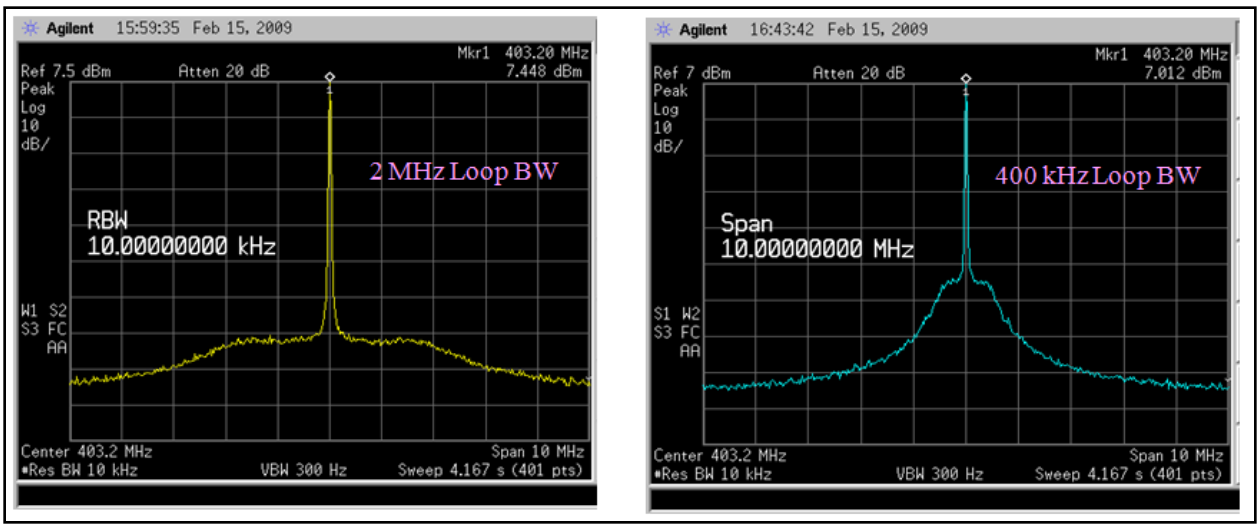


Figure 4.8: Loop Bandwidth and Low-Offset Phase Noise

### *[4.3b] VCO Phase Noise Measurements*

Using the effect described above, an approximate VCO phase noise measurement can be presented. Due to frequency jitter, true open-loop VCO phase noise cannot be measured, but by narrowing the bandwidth of the loop filter VCO phase noise can be approximated. Figure 4.8 is a measurement of VCO phase noise using a 1 kHz loop filter bandwidth.

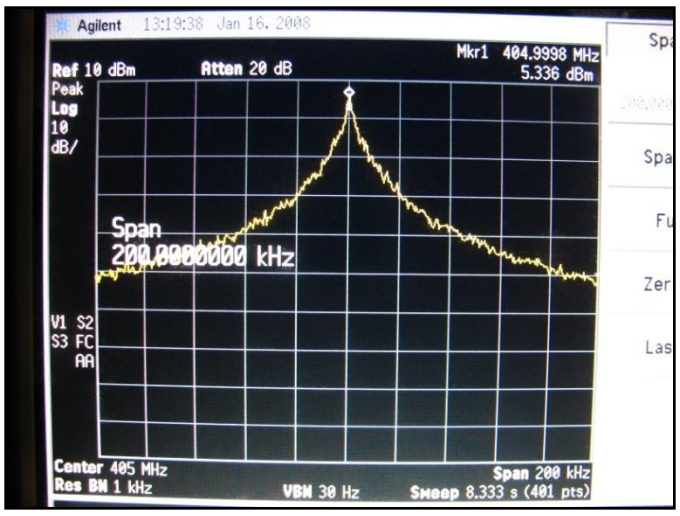


Figure 4.9: VCO Phase Noise Spectrum

A more detailed VCO phase noise measurement is presented in Figure 4.9. This measurement is recorded in dBc/Hz, where “dBc” annotates that the noise magnitude is

presented as relative to the carrier or desired output signal. The "/Hz" signifies that the resolution bandwidth of the spectrum analyzer has been taken into account when recording the measurement. For example, if the resolution bandwidth of the analyzer is set to 1KHz as it is in Figure 4.8, the phase noise is actually 30dB (power-decibel representation of 1K) less than what is observed on the screen. A closed loop measurement of the phase noise output is also presented in Figure 4.9 in order to illustrate how the loop acts to reduce phase noise at low frequency offsets.

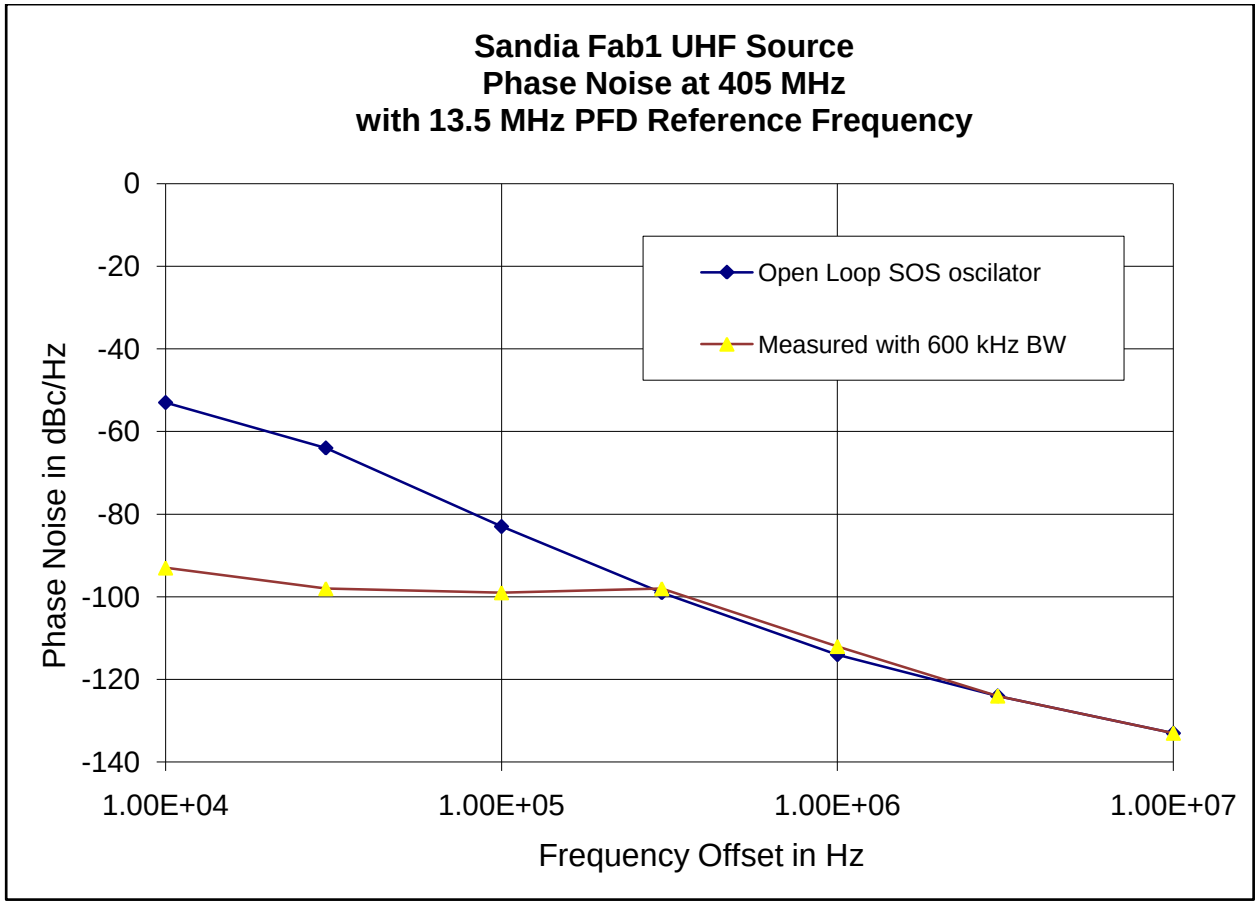


Figure 4.10: Detailed VCO Phase Noise Measurement

# CHAPTER 5 – Early K-State Synthesizer Design Discussion

The research on which this thesis is written was prompted by performance in previous integrated frequency synthesizer implementations by K-State. This performance was well below expected values and observations led us to believe that the charge pump is a critical circuit to focus on with the aim of achieving better noise levels and spurious performance. Hence, we studied the previous circuits and created several new implementations designed to improve phase noise and spur levels.

## [5.1] Charge Pump Op-Amp Design

The first frequency synthesizer chip developed by K-State was based on a 3rd-order MASH accumulator, a 3rd-order loop filter, a CMOS VCO and the charge pump circuit illustrated in Figure 5.1.

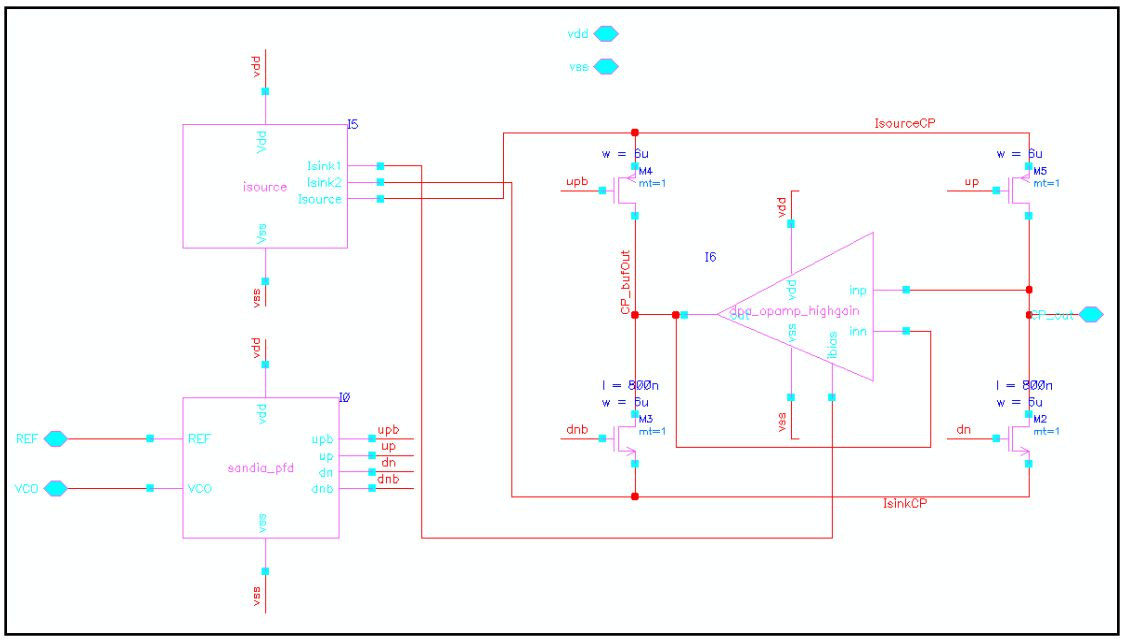


Figure 5.1: Default Charge Pump Schematic

This topology was discussed in the third chapter of this thesis. The key observation to note here is that the op-amp must be able to sink and source current levels equal to the pump

current and keep the voltage at its output constant. The op-amp implementation used in the Fab1 charge pump circuit was, unfortunately plagued by low open loop gain and low current sinking ability relative to the charge pump current. Figure 5.2 illustrates the op-amp schematic used.

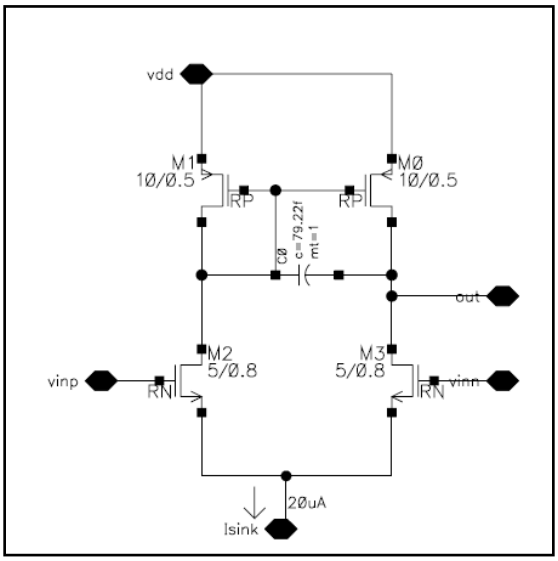


Figure 5.2: Fab1 Op-Amp Schematic

Transistors M2 and M3 form a differential pair and transistors M1 and M0 serve as an active load. C0 provides a pole in the frequency response in order to bring the open-loop gain to below unity before 180° of phase is reached, ensuring closed-loop stability. This design is appropriate for an op-amp input stage, but it falls short when used as a whole op-amp due to high output impedance and low gain.

This design also falls short in its ability to sink and source current. The charge pump in the first synthesizer design pumped 200μA of current to and from the loop filter when on. This op-amp circuit, however, is only able to sink a current equal to the bias current labeled "Isink" at the bottom of Figure 5.2. The output impedance, open-loop gain and current output were all improved by introducing the topology illustrated in Figure 5.3.

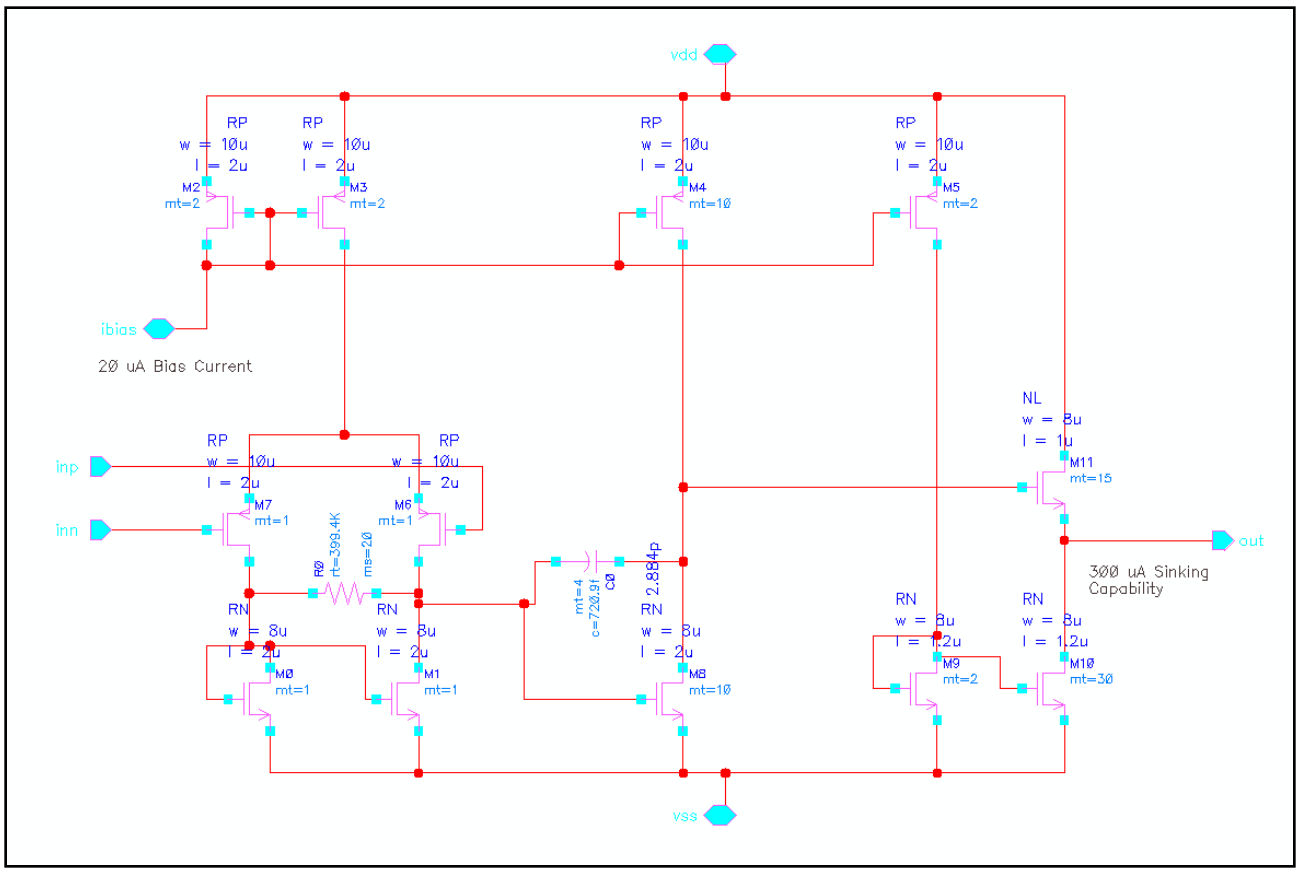


Figure 5.3: Fab4 Op-Amp Schematic

This topology comes closer to the traditional op-amp design, which includes an input stage, a voltage gain stage and an output stage. This design is somewhat minimal in that it utilizes a simple source follower (M11) as an output stage rather than a class A-B output stage as used in most op-amps.

The input stage of the op-amp illustrated in Figure 5.3 is different from the input stage illustrated in Figure 5.2 in that it is composed of PFETs instead of NFETs. This was done to extend the common-mode input voltage range down to ground, due to the expected voltage tuning range of the VCO. The compensating capacitor C0 was moved to the voltage gain stage, made of M8, in keeping with standard op-amp design practice. A source follower (M11) is used to decrease the output impedance of the amplifier and thus allow for higher current sinking and

sourcing ability at the output. Finally, the power supply current was set at 150% of the charge pump current**.**

***[5.1a] Charge Pump Op-Amp Over-ride Measurements***

So much attention was given to the op-amp in the charge pump because observations in the lab suggested that improving the op-amp design would drastically improve spurious noise performance. These observations involved using a power supply to over-ride the op-amp output via a probe pad on the synthesizer chip. The output of the op-amp was kept at a constant voltage by a power supply in order to simulate what would happen if the opamp worked properly (in which case it would hold its output node at the same voltage as the loop filter voltage value). Figure 5.3 displays spectra with the op-amp output over-ridden and left alone. The yellow spectrum shows the synthesizer output with no over-ride and the blue spectrum shows the output with over-ride.

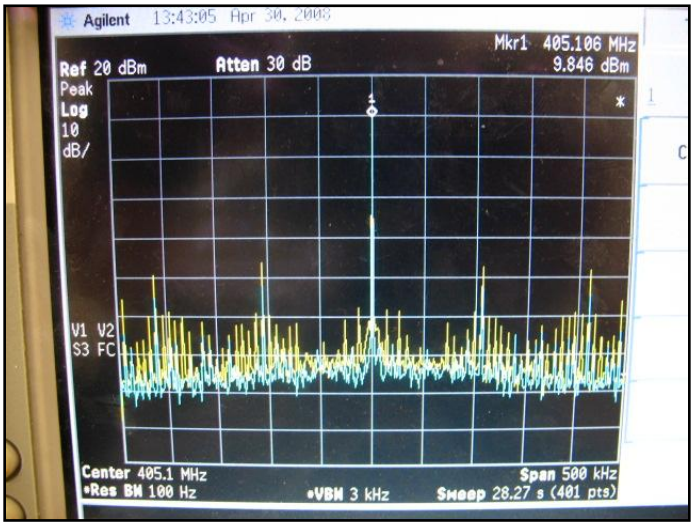


Figure 5.4: Spectra with and without Op-Amp Over-ride

According to these observations, a spectral purity improvement of as much as 15dB or more could be seen at low frequency offsets (below 200KHz) from the desired signal could be achieved by the improvement of the op-amp circuit. This is believed to be due to an effective

linearization of the charge-to-phase error transfer function discussed in Chapter 1. The new op-amp is intended to fix this problem.

# CHAPTER 6 – Improved K-State Frequency Synthesizer Measurements

To research the problems noted in the previous chapter, integrated synthesizers were developed with a 10-bit 4th-order MASH sigma delta modulator, a 3rd-order loop filter, and four alternative charge pump circuits. As expected, there are differences in noise performance between the charge pump implementations. The measurements taken for this thesis primarily focus on phase noise and spurious noise levels for the different charge pumps and loop filter configurations. Figure 6.1 is a picture of the synthesizer chip on a test board.

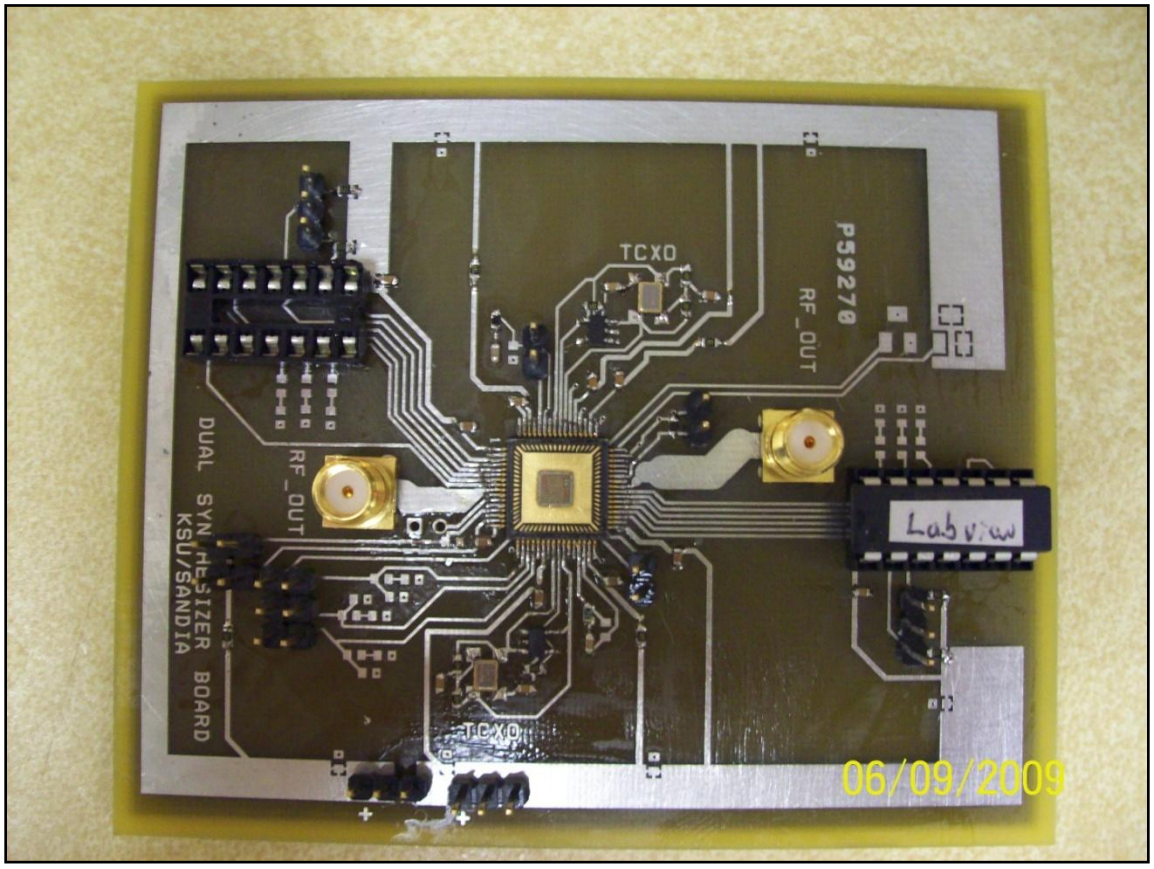


Figure 6.1: Synthesizer Chip on Test Board

The 3rd-order SDM synthesizer also has a VCO with a higher control-voltage to frequency conversion gain, which turned out to offer a significant improvement in linearity and performance.

### [6.1] Default Charge Pump

The schematic for the default charge pump is shown in Figure 6.2. This circuit was given the name "default" because it was derived from the charge pump circuits in previous fabrications of the synthesizer, but its op-amp circuit was improved over the previous versions.

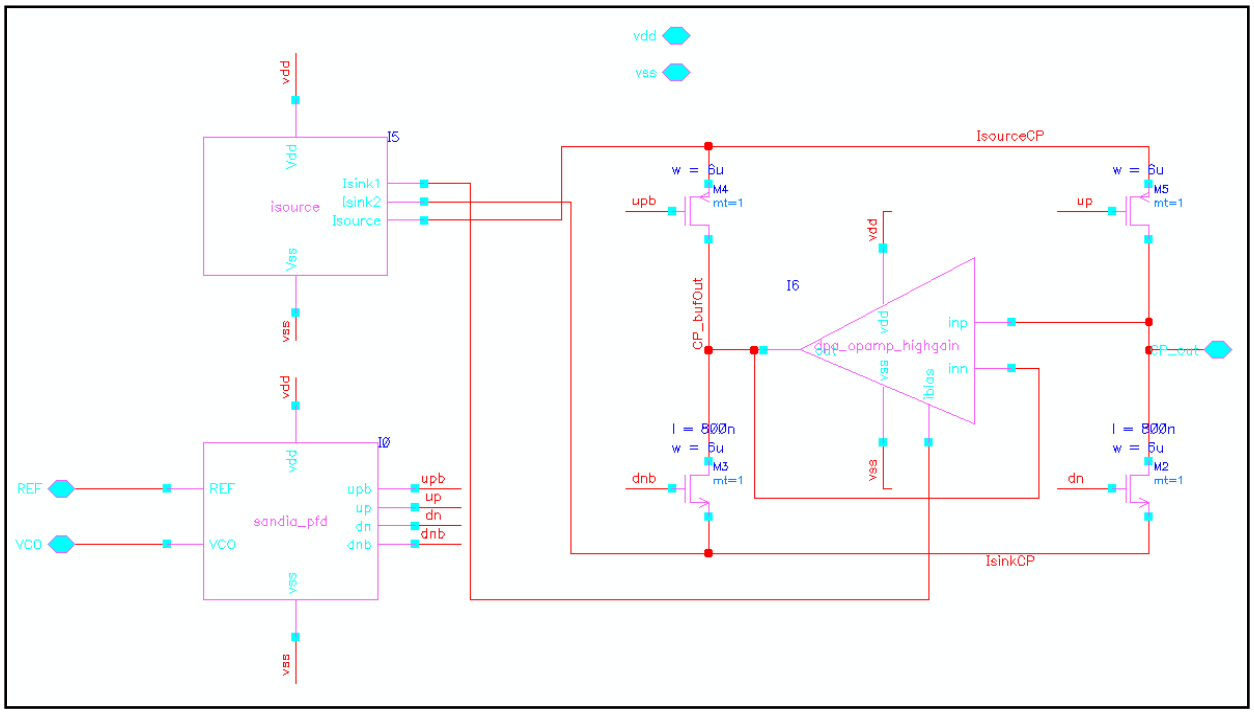


Figure 6.2: Default Charge Pump Schematic

As discussed in Chapter 5, the circuit employs an op-amp whose gain and output impedance were improved to reduce low frequency offset spurious tones at the synthesizer output. Figure 6.3 illustrates an example spectrum from the synthesizer in integer-N mode while using this charge pump.

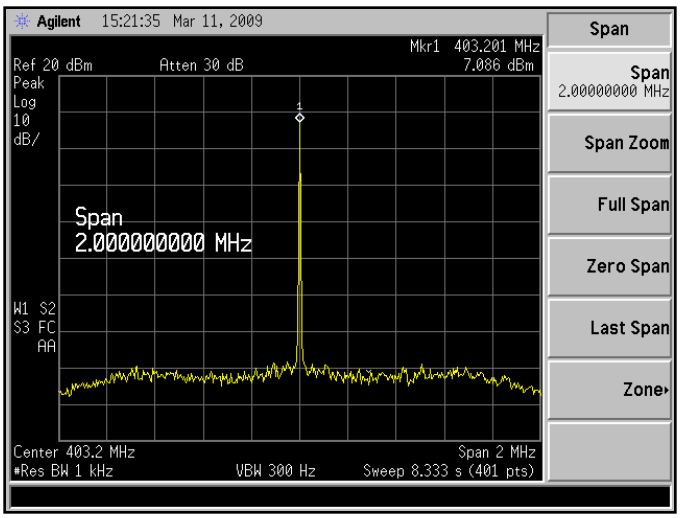


Figure 6.3: Default Charge Pump Integer Mode Spectrum

Figure 6.3 was generated using an HP E4402B spectrum analyzer. A more detailed phase noise plot was generated using the E4402B for high frequency offset measurements and a test setup including a Rhode and Schwarz SME02 oscillator, an HP 11729C carrier noise test set and an HP 3588A spectrum analyzer for low offset phase noise measurements (see Figure 6.4). The oscillator and carrier noise test set were used to beat the noise spectrum down to DC as would be done in a direct conversion receiver. A mixer in the test set and a control voltage input to the reference oscillator within the SME02 ensure that the signal from the synthesizer and the test oscillator are in sync to allow the signal be beat down to DC. Figure 6.4 shows this test setup.

Figure 6.4: Phase Noise Test Setup

Figure 6.5 presents the phase noise measurements taken with this setup. This figure also presents measurements taken from the previous synthesizer implementation, which uses the op-amp circuit with low gain and high output impedance.

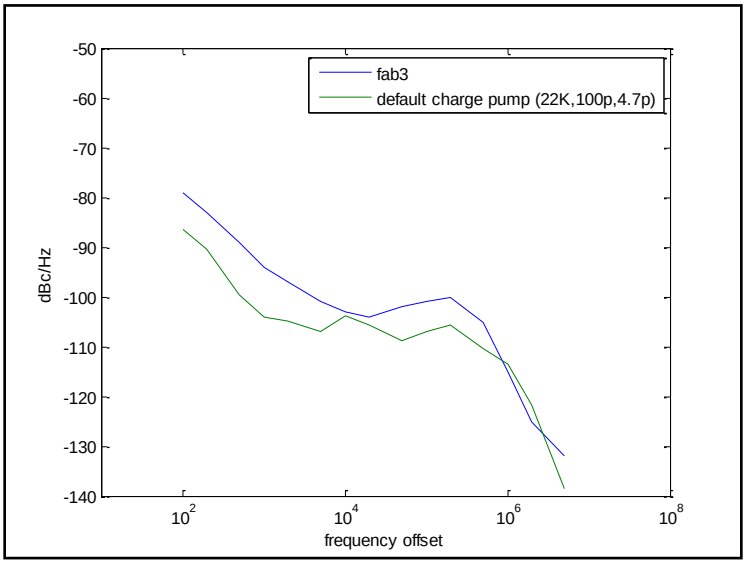


Figure 6.5: Default Charge Pump Phase Noise Measurements

From Figure 6.5, the newer synthesizer achieves approximately 10 dB better phase noise performance at low frequency offsets.

## [6.2] Alternate Charge Pump 1

To address the switching speed and non-linear effects of mismatching between the source and sink currents in the charge pump, the topology illustrated in Figure 6.6 was implemented. The output spectrum from the synthesizer with this charge pump in operation is illustrated in Figure 6.7.

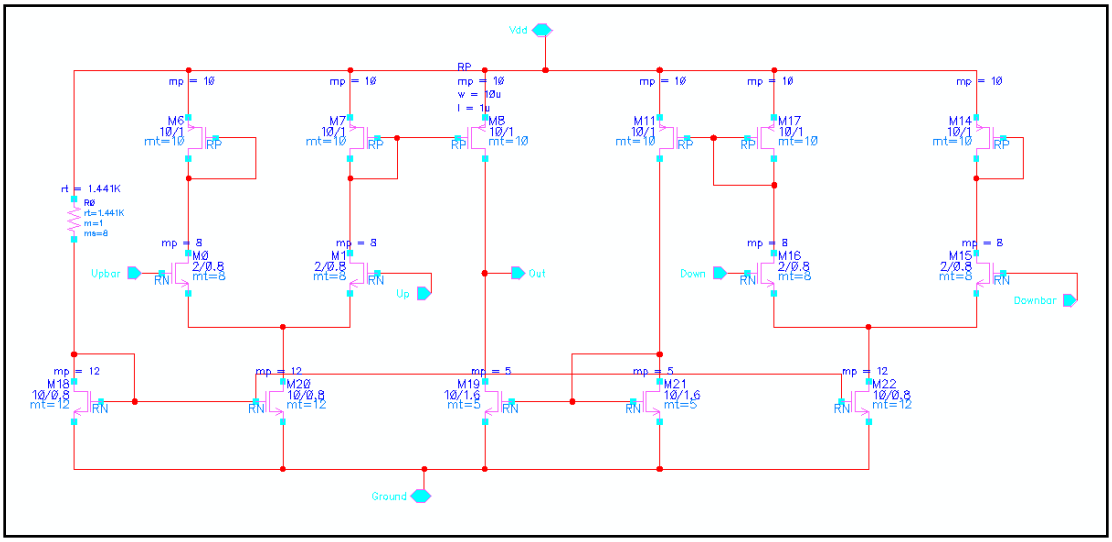


Figure 6.6: Alternate Charge Pump 1 Schematic

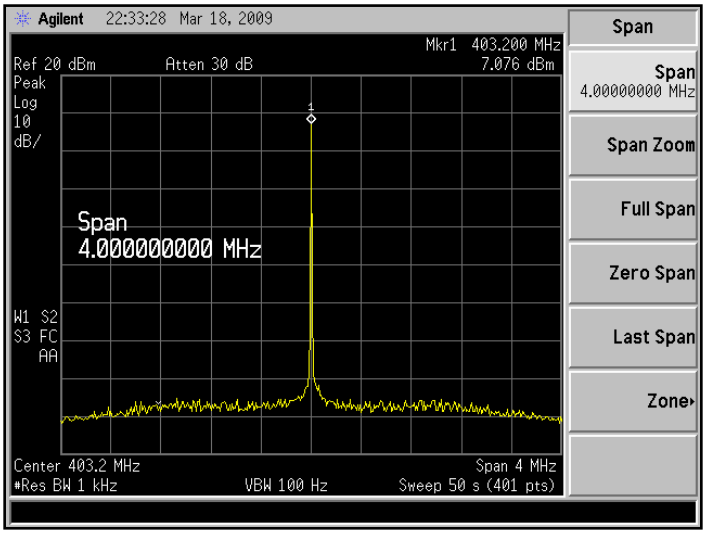


Figure 6.7: Alternate Charge Pump 1 Integer-N Spectrum

More detailed phase noise measurements were also taken of the output noise with this charge pump in operation in order that its performance be compared to the default charge pump and previous implementations of the synthesizer. Figure 6.8 illustrates this measurement.

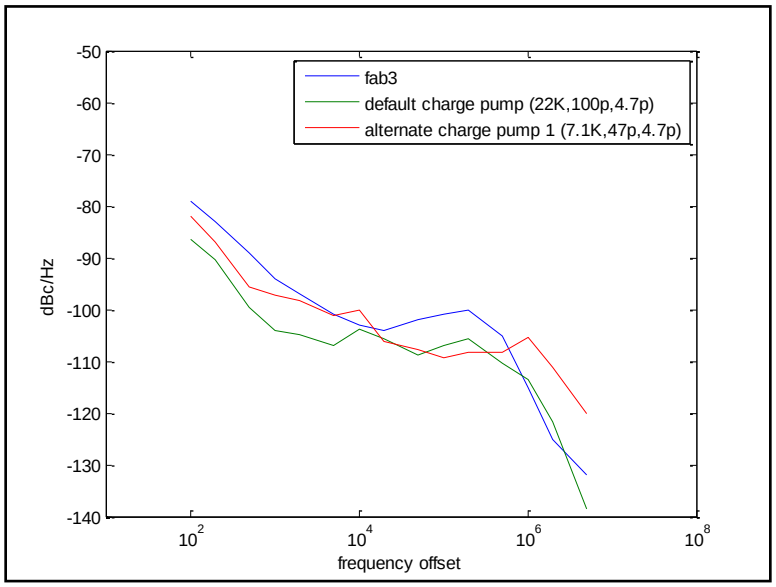


Figure 6.8: Alternate Charge Pump 1 Phase Noise Measurement

This charge pump appears to be out-performed by the default charge pump at the majority of the frequency offsets measured, but still super-cedes the phase noise of the previous synthesizer implementation. This charge pump is different from the default charge pump not only in topology, but in magnitude of charge deposited on the loop filter. This circuit is designed to sink and source 1mA of current when on, while the default charge pump sinks and sources 200uA of current.

The difference in charge pump current has an effect on phase noise performance in that a charge pump with a higher current needs to be on for a shorter amount of time. If the charge pump is on for less time, than there will be less degradation to the over-all phase noise performance of the synthesizer because the active device noise from the charge pump makes less of a contribution to the output phase noise [5].

The disappointing noise performance in this circuit can be explained by an effect that has been observed in transistors in the fully-depleted silicon on insulator (SOI) process that was used for the fabrication of the synthesizer [ref]. Figure 6.9 illustrates that the output resistance of typical FETs in this process can be lower than what Cadence simulations would predict. The low output impedance would cause a unity-gain current mirror to have a non-unity gain, which would cause a mismatching effect in the alternate charge pump 1 design.

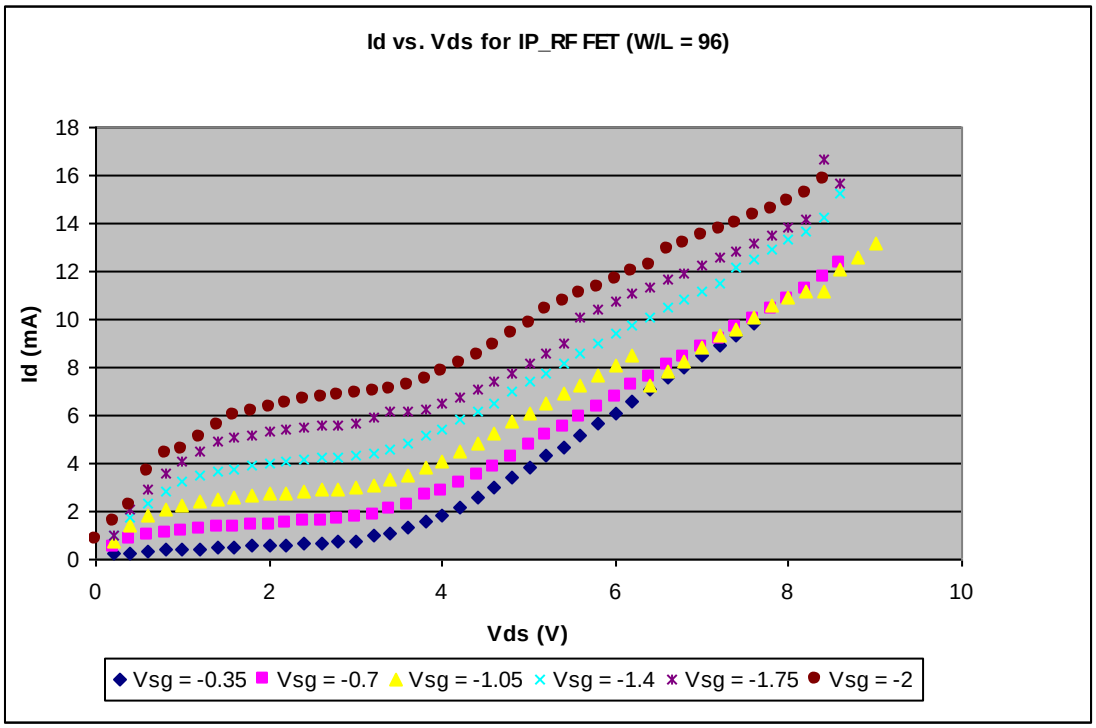


Figure 6.9: Measured FET Output Resistance Plots in Peregrine FC Process

## [6.3] Alternate Charge Pump 2

Two versions of this topology were implemented in the synthesizer. These two circuits differ only in the gate areas of the current sinking and sourcing transistors. The width-to-length ratios are all the same, however, so ideally these two circuits should pump the same amount of

charge. The schematics for these two charge pump circuits are presented in Figures 6.10 and 6.11.

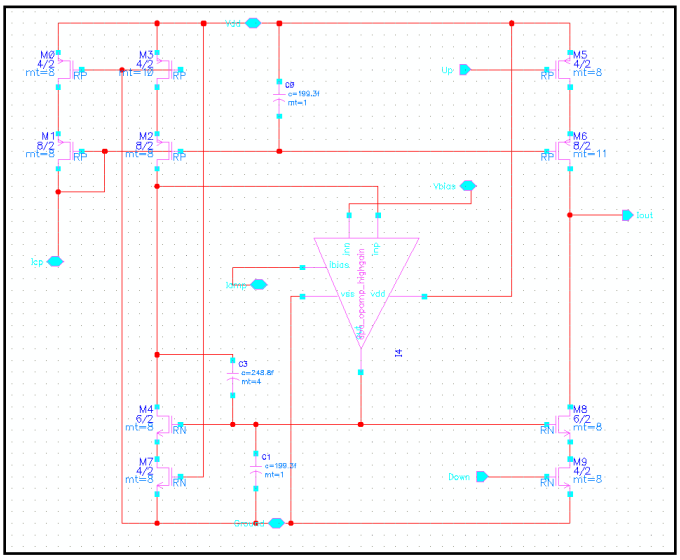


Figure 6.10: Alternate Charge Pump 2a Schematic

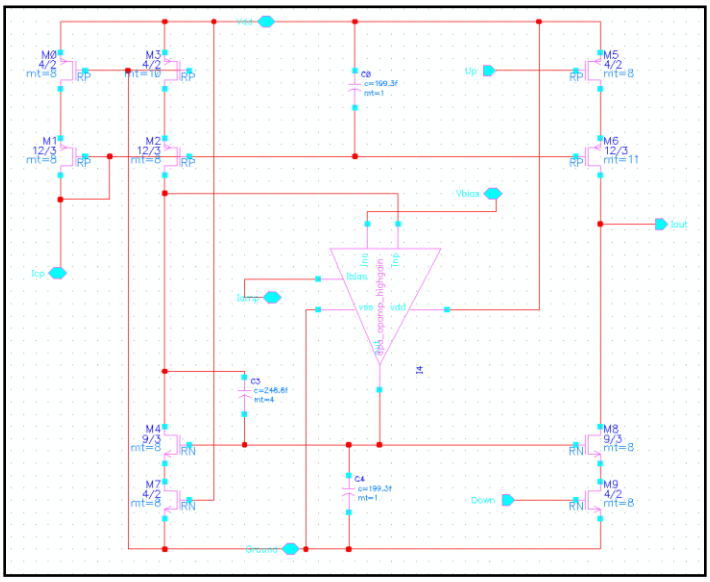


Figure 6.11: Alternate Charge Pump 2b Schematic

Figures 6.12 and 6.13 illustrate output spectra from these designs.

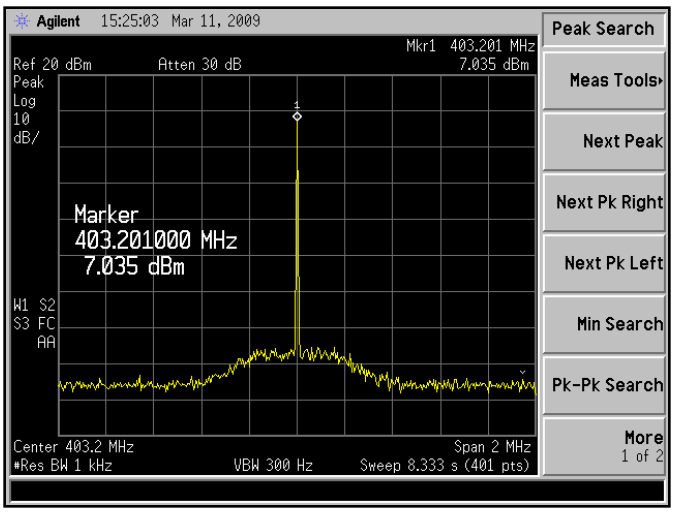


Figure 6.12: Alternate Charge Pump 2a Output Spectrum

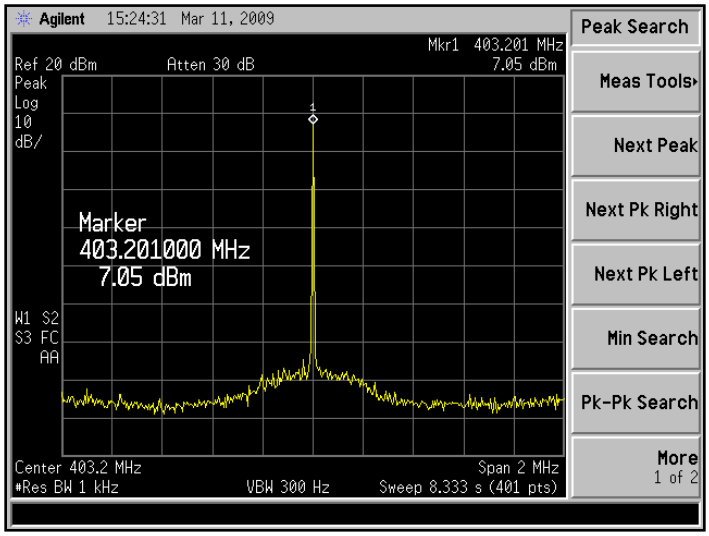


Figure 6.13: Alternate Charge Pump 2b Output Spectrum

The phase noise in the charge pump with the larger current sinking and sourcing transistors always exhibits slightly better phase noise performance than the charge pump with the smaller transistors. This is as expected given the arguments presented in Chapter 3. Figure 6.14 illustrates a more detailed comparison between the phase noise of the synthesizer using these two circuits.

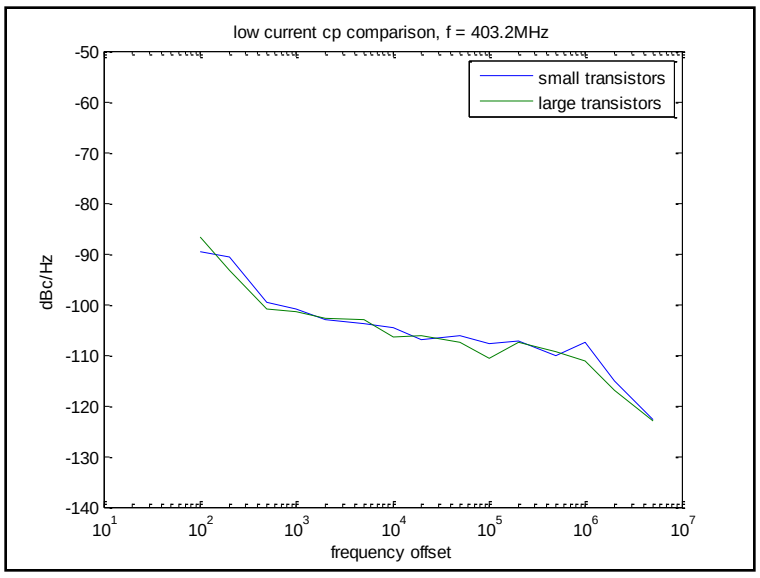


Figure 6.14: Gate Area Phase Noise Comparison

Figure 6.14 presents a comparison between this topology and the other two topologies implemented in the synthesizer chip. It can be seen that this topology results in the best low-offset phase noise performance, but does not facilitate an improvement in high-offset phase noise (as seen in Figure 6.15).

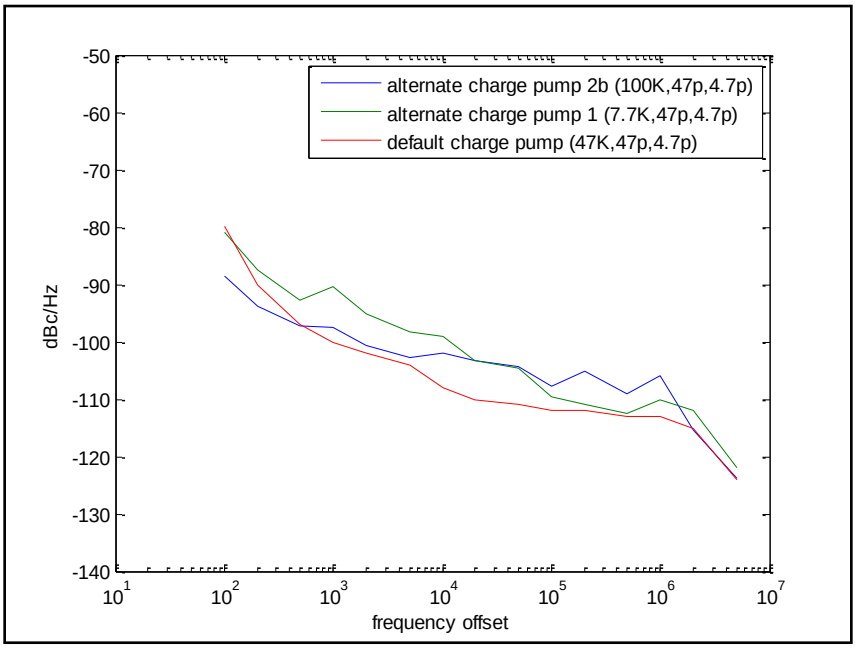


Figure 6.15: Alternate Charge Pump Phase Noise Comparison

## [6.4] VCO Gain and Linearity Measurements

The VCO converts a voltage into a frequency and, in the analysis of the loop, this conversion is assumed to be linear. In reality, however, this conversion is only approximately linear around a range of control voltages. Figure 6.16 illustrates measured conversion curves for the VCO used in this synthesizer. According to these plots, the voltage to frequency conversion is roughly linear when the control voltage is at or around 1.25V. The effects of the VCO non-linearity on output phase noise can be measured by changing the coarse tuning range while the synthesizer is programmed to synthesize a given frequency. Figure 6.17 displays phase noise plots for different average control voltages. Note that the noise is lowest when the average control voltage is around the linear range (1.21V, according to the legend).

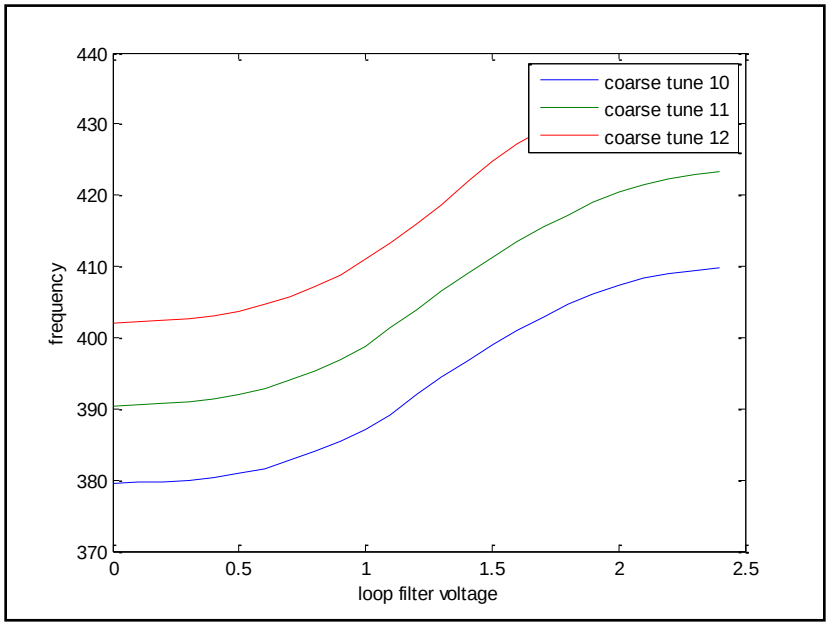


Figure 6.16: VCO Tuning Curves

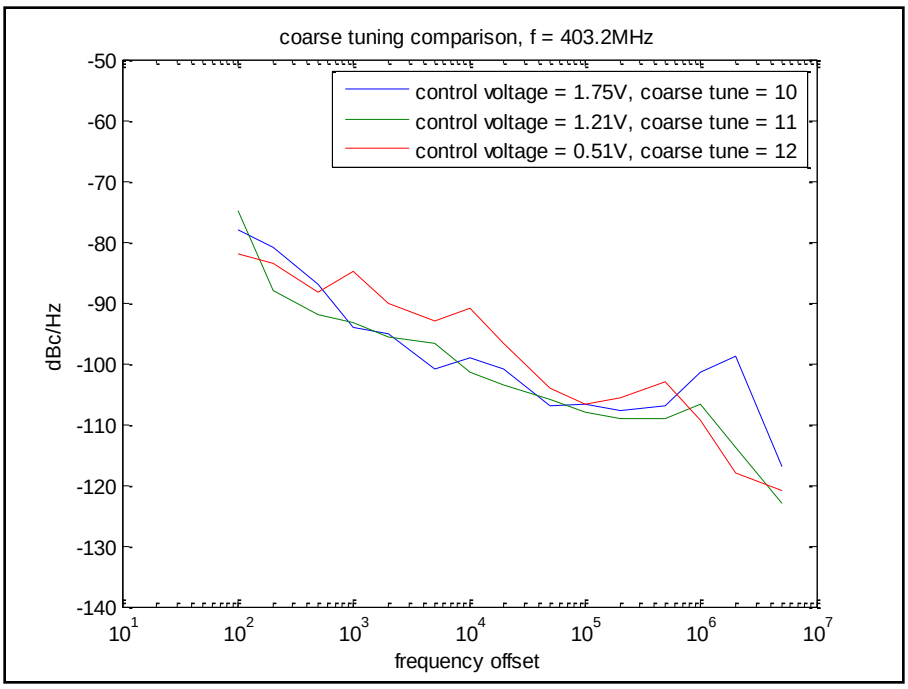


Figure 6.17: Phase Noise for Different Average Control Voltages

It can be shown that the control voltages measured for these three coarse tuning settings can be predicted using the VCO tuning curves. Figure 6.18 displays the tuning curves with the output frequency marked in order to show the corresponding control voltages. Note that for a coarse tuning of "10" the control voltage is about 0.5V. For a coarse tuning of "11" the control voltage is about 1.2V. For a coarse tuning of "12" the control voltage is about 1.8V. These voltages agree roughly with what was measured and annotated in the legend of Figure 1.17.

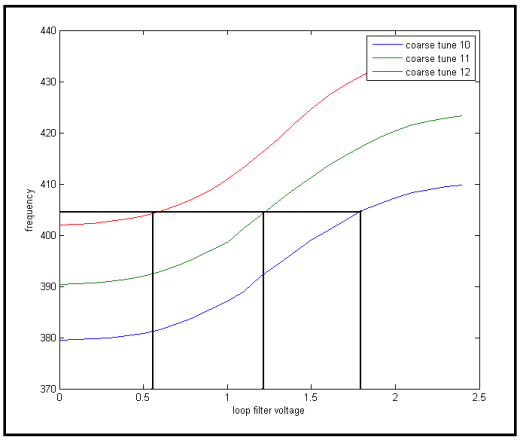


Figure 6.18: VCO Tuning Curves, 403MHz Labeled

## [6.5] 3rd-Order SDM versus 4th Order SDM Measurements

According to the noise shaping behavior of MASH sigma-delta modulation described in Chapter 2, a fractional-N synthesizer built around a 4th-order SDM should display better spurious noise performance at low frequency offsets than a synthesizer utilizing a 3rd-order SDM. This improvement with an increase in modulator complexity was, however, not realized. The chip on which the synthesizer described in this thesis was integrated also includes a synthesizer of each type. When the 4th-order synthesizer is using the default charge pump, it is identical to the 3rd-order synthesizer except that the 3rd-order synthesizer has a VCO that is roughly twice as sensitive to control voltage. Hence, its tuning range is larger and loop filter impedances must be scaled by ½ . This results in an effective improvement in linearity of the VCO tuning curve.

The synthesizer with a 3rd-order SDM has been shown to consistently produce a fractional-N spectrum that has spurious tones which are 50dB less than the carrier signal. This is approximately 10 dB better than the original synthesizer design. The 4th-order modulator, however, produces tones that are only 35dB down from the carrier signal. Figure 6.19 and 6.20 display fractional-N spectra from the 3rd and 4th-order synthesizers. The 4th-order synthesizer used the default charge pump for the measurement in Figure 6.20, which is the same charge pump circuit used in the 3rd-order synthesizer.

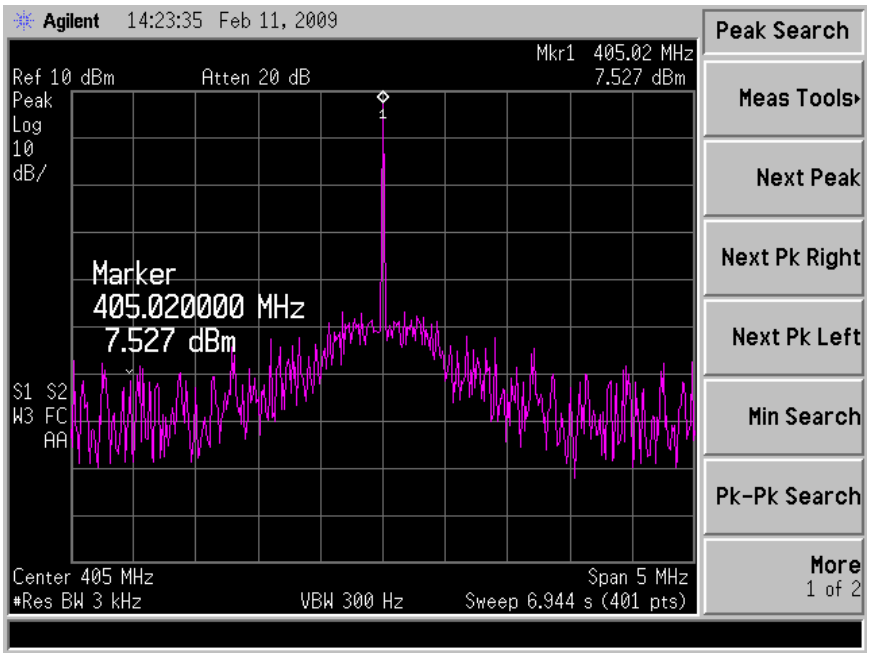


Figure 6.19: Spurious Tones in 3rd-Order Synthesizer

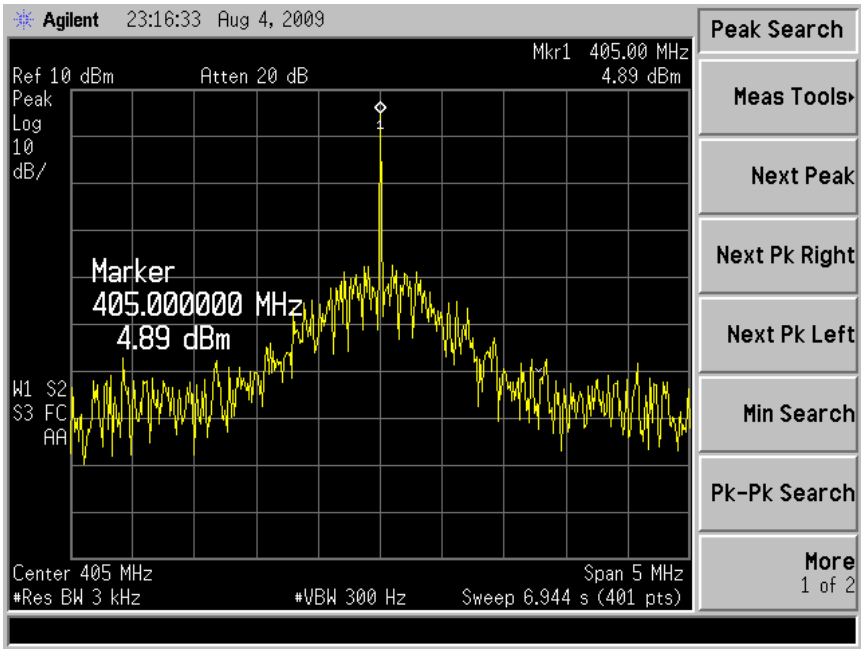


Figure 6.20: Spurious Tones in 4th-Order Synthesizer

There are two reasons why a 4th-order synthesizer could have poorer spurious noise performance than the 3rd-order synthesizer. The first reason is due to the fact that the 4th-order SDM outputs higher

values than the 3rd-order SDM by a factor of 2. This would account for a 6dB increase in spurious tones when the SDM order is increased by unity.

Another reason for the difference in spurious performance between the 3rd and 4th-order synthesizer can be attributed to the difference in the gain in the conversion at the VCO from voltage to frequency. As stated earlier in this section, the VCO gain in the 3rd-order synthesizer is twice that of the VCO gain in the 4th-order synthesizer and a larger gain at the VCO results lower loop filter impedance and lower variations in control voltage and thus improved linearity in the VCO voltage to frequency conversion.

Figure 6.21 illustrates a phase noise comparison between the 3rd and 4th-order synthesizers.

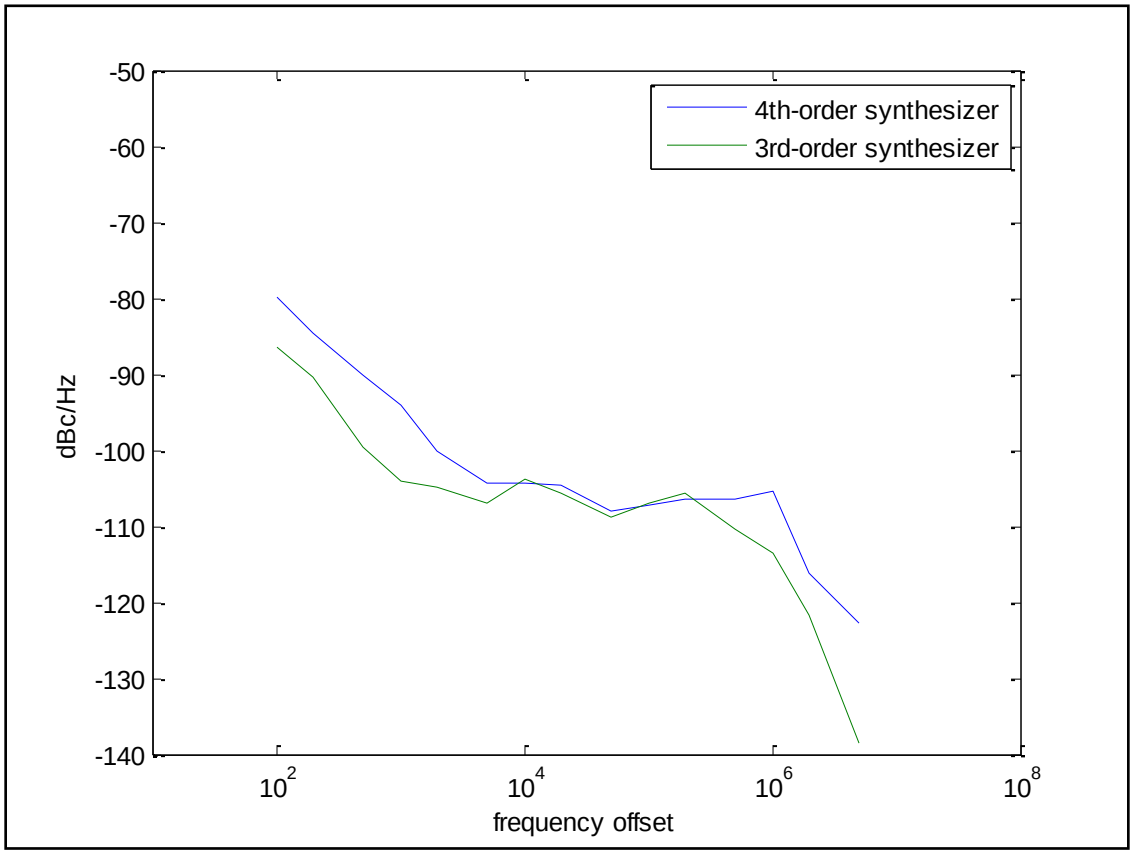


Figure 6.21: 3rd and 4th Order Synthesizer Phase Noise Comparison

# CHAPTER 7 – Conclusions

Techniques in improving phase and spurious noise performance in integer-N and fractional-N frequency synthesizer have been investigated. Some techniques, such as increasing VCO sensitivity and gate area in charge pump transistors have been shown to be effective. Other techniques, such as increasing the order of the modulator and charge pump current have not been shown to be effective.

## [7.1] Design Recommendations

In order that this thesis be useful for future research, recommendations for further improvement of integrated frequency synthesizers will be presented in this section. These recommendations will focus on the different circuits in the loop, starting with the charge pump.

### *[7.1a] Charge Pump Recommendations*

As was stated numerous times in this thesis, linearity in the conversion from phase error to charge at the PFD/CP in the loop is critical for the realization of low spurious tones and low phase noise at the output. This conversion can be made as linear as possible by ensuring that the positive and negative currents from the pump are equivalent. The circuit presented in Section 3.2c with the problem noted in figure 6.2 could be improved by using cascoding on the mirror made of transistors M19 and M21. The schematic of this charge pump is presented again in Figure 7.1 for reference.

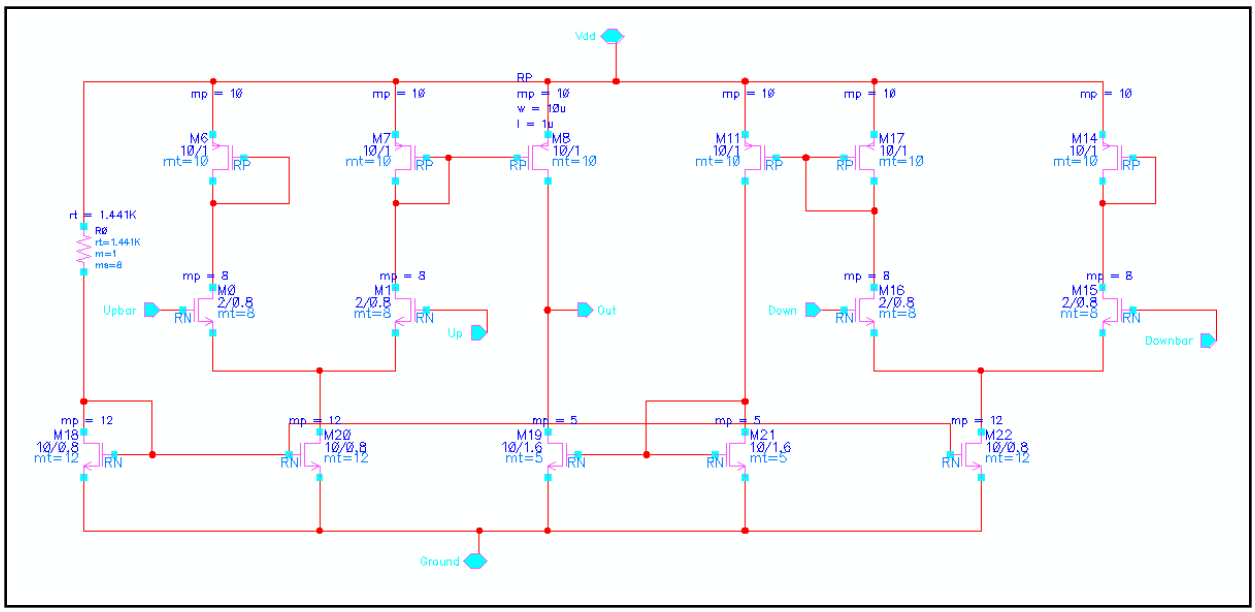


Figure 7.1: Alternate Charge Pump 1

An investigation into the effects of additive noise from the charge pump circuit was also presented using the second alternate charge pump topology. This topology was implemented twice with the two implementations differing in gate area of the current pumping transistors only. While a difference in phase noise was observed qualitatively, a quantitative measurement of the performance gain associated with gate area increase was not achievable with these circuits. This was because the difference in phase noise was smaller than the tolerance in the low frequency phase noise measurements. It could therefore be suggested that a greater difference in gate area be implemented in a future synthesizer design.

Since current magnitude from the charge pump affects $K_{phi}$, which in turn affects the impedance of the loop filter for a given bandwidth, a comparison between similar topologies providing different current magnitudes would also be beneficial.

***[7.1b] PFD Recommendations***

The phase frequency detector also has an impact on the linearity of the conversion between phase error and charge at the PFD/CP. This effect is seen primarily in the dead zone

phenomenon discussed in Section 3.2b. To ensure that this effect is properly mitigated, the delay introduced by the chain of inverters illustrated in Figure 3.2 could be increased. Simulation has suggested that this circuit does not exhibit dead zone behavior with any of the charge pump circuits presented in this thesis, conservative design would suggest that increasing this delay would be a prudent thing to do.

***[7.1c] Reference Frequency Recommendations***

Increasing the reference frequency is also recommended as a method to control spurious levels. Increasing $f_{ref}$ spreads the SDM spectrum, pushing more energy outside the loop bandwidth. The cost is degradation in resolution, although this can be overcome by increasing the SDM register depth. Another cost is added power consumption, which must be weighed against system goals. Finally, it is recommended that this method only be considered for spurious reduction after linearity issues have been fully addressed, since the loop filter cannot correct for spurious mixing within the PFD and charge pump circuits preceding it.

***[7.1d] VCO Recommendations***

Measurements taken to compare VCO gain in the course of the research presented in this thesis suggest that increasing VCO gain is beneficiary to phase noise and spurious noise performance in the synthesizer. This performance gain is due to the fact that increasing $K_v$ allows for lower loop filter impedance for a given bandwidth.

Lower loop filter impedance implies using a smaller resistor and a larger shock absorbing capacitor. These effects result in a decreased variation in the control voltage from the loop filter and better containment of this voltage into the linear range of the VCO.

Since phase noise in the CMOS VCOs is the main contributor to phase noise at the synthesizer output, techniques for reducing noise at the VCO are very important. Phase noise

from the VCO signal can be attributed to a non-infinite quality factor of the resonating elements in the circuit (primarily, the inductors) and to 1/f noise in the active devices. Thus, research into implementation of high quality factor inductors and use of lower 1/f noise devices (i.e. PMOS devices) in the process used would be beneficial.

# References


[1] E. A. M. Klumperink, S. L. J. Gierkink, A. P. Van der Wel and B. Nauta, "Reducing MOSFET 1/f Noise and Power Consumption by Switched Biasing, 995, July 2000

[2] H. Tian and A. El Gamal, "Analysis of 1/f Noise in Switched MOSFET Circuits", 152, Feb. 2001

[3] L. K. J. Vandamme, X. Li, and D. Rigaud, "1/f Noise in MOS Devices, Mobility or Number Fluctuations", 1937, Nov. 1994

[4] E. Temporiti, G. Albasini, I. Bietti, R. Castello and M. Colombo, "A 700KHz Bandwidth ∑Δ Fractional Synthesizer with Spurs Compensation and Linearization Techniques for WCDMA Applications", 1448, Sept. 2004

[5] T. Bourdi and I. Kale, *CMOS Single Chip Fast Frequency Hopping Synthesizers for Wireless Multi-Gigahertz Applications*, Dordrecht, the Netherlands: Springer, 2007

[6] B. Razavi, *Monolithic Phase-Locked Loops and Clock Recovery Circuits: theory and design*, New York: IEEE Press, 1996, 81

[7] P. Jacobs, J. Janssens, T. Geurts and J. Crols, "A .35μm CMOS Fractional-N Transmitter for 315/433/868/915 MHz ISM Applications", 3

[8] U. Meyer-B¨ase, S. Wolf, and F. Taylor, "Accumulator-Synthesizer with Error-Compensation, 885, July 1998

[9] G. Vasilescu, *Electronic Noise and Interfering Signals: principles and application*, Germany: Springer, 2004, 63

[10] H. C. Luong and G. C. T. Leung, *Low-Voltage CMOS RF Frequency Synthesizers*, UK: Cambridge, 2007

[11] A. Lacaita, S. Levantino and C. Samori, *Integrated Frequency Synthesizers for Wireless Systems*, UK: Cambridge, 2007

[12] A. Holme, "15-25MHz Fractional-N Synthesizer", 2005. [Online]. Available: http://www.holmea.demon.co.uk/Frac2/Mash.htm [Accessed: July 27, 2009]

[13] J. Rogers, C. Plett, F. Dai, *Integrated Circuit Design for High-Speed Frequency Synthesis*, Boston: Artech House 2006

[14] W. L. Brogan, *Modern Control Theory (Third Edition)*, Upper Saddle River, NJ: Prentice-Hall 1991