AN EVALUATION OF THE MC68HC11A8 SINGLE-CHIP MICROCOMPUTER AS A CONTROLLER FOR LOW-POWER, PRECISION A/D CONVERTERS

by

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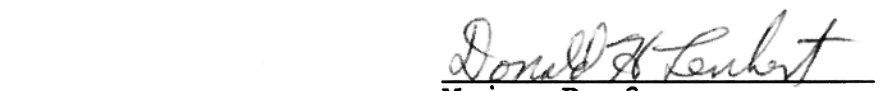

Major Professor

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I would also like to thank my parents, Duane and Glenna, who not only encouraged my curious mind, but also patiently supported my college education.

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Introduction

Graduate research at Kansas State University's Department of Electrical and Computer Engineering has demonstrated several benefits of microprocessor based analog-to-digital (A/D) conversion. Four of these advantages are:

* power reduction by power-switching analog components at low duty cycles
* increased precision by run-time error correction and auto-calibration
* increased control capability for complex hybrid conversion schemes
* increased host communication capability for versatile application

The same graduate research which demonstrated the advantages of microprocessor based A/D conversion also demonstrated the disadvantages. The two most significant disadvantages were power consumption and physical size.[1] [2] Almost in answer to these disadvantages, Motorola Corporation's Semiconductor Division recently developed the MC68HC11A8. The MC68HC11A8 is a fast, low-power, 8-bit microcomputer complete with memory, sophisticated

communication interfaces, and an 8-bit A/D converter (ADC) all fabricated on a single monolithic chip.

This thesis evaluates the MC68HC11A8 single-chip microcomputer as a controller for low-power, precision ADCs. The first section describes the MC68HC11A8, its input/output interfaces, its on-chip ADC, and its power consumption. The next section demonstrates how the MC68HC11A8 reduced the physical size of an existing ADC. Section three presents four feasible, low-power, precision A/D conversion techniques. The last section documents the MC68HC11A8's control of a new switched-capacitor sample-and-hold DAS.

Relevant schematics, parts lists, timing diagrams, and program listings for each of the two applications are provided in the appendix. In addition, a description of the MC68HC11A8 evaluation system and listings of useful software utilities used to evaluate the MC68HC11A8 and its applications are also provided in the appendix.

MC68HC11A8 Characteristics

The MC68HC11A8 is a sophisticated HCMOS 8-bit microcomputer fabricated on a single integrated circuit chip. Although fully compatible with existing 6800 and 6801 machine instructions, the MC68HC11A8 provides an additional CPU register and an extended 6800 instruction set. One 16-bit index register, Y, has been added to the MC68HC11A8. In addition, the two 8-bit accumulators can either be accessed independently as accumulators A and B or collectively as the 16-bit accumulator D (Figure 1).

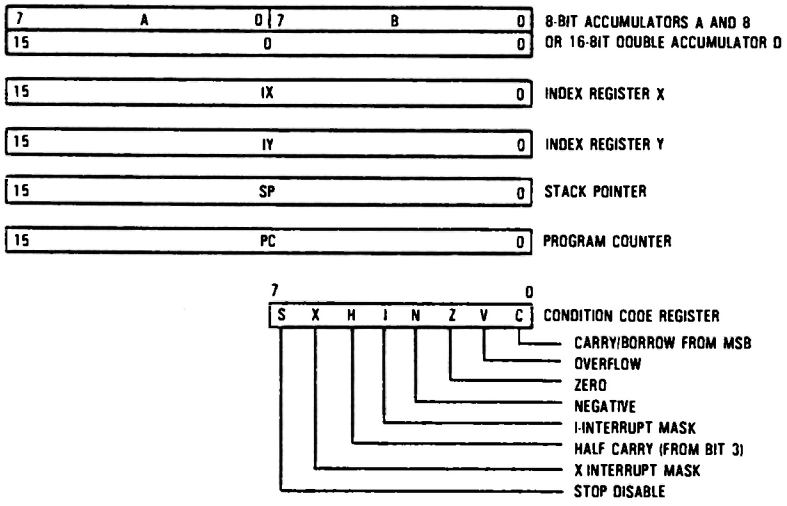


Figure 1 Graphical Representation of MC68HC11A8 CPU Registers (Courtesy of Motorola[3])

The MC68HC11A8 is called a single chip microcomputer because its on-chip memory and input/output (I/O) interfaces allow the MC68HC11A8 to execute stored programs and communicate with host or peripheral systems independently of additional support logic. The MC68HC11A8's on-chip memory includes 8K bytes of ROM, 512 bytes of EEPROM, and 256 bytes of RAM. If additional memory is required for large programs or data tables, the MC68HC11A8 can also be configured to access external memory in its expanded-memory mode.

Input/Output Interfaces

There are 40 I/O pins (36 I/O pins on the MC68HC11A8's 48 pin package) on the MC68HC11A8 assigned to five, 8-bit I/O ports. These I/O pins can be configured as either general purpose I/O lines or special purpose communication and interrupt lines (Figure 2). Port A, for instance, is used by the MC68HC11A8's elaborate timer interrupt system. The timer system has a 16-bit free running counter which is used to perform hard-wired output compares, input captures, pulse accumulations, and real-time periodic interrupts.

In single-chip mode, ports B and C can be used for strobe and handshake, parallel I/O. Port B is always configured as an 8-bit output port but port C can be configured for output, input, or latched input. In expanded-memory mode, ports B and C become the multiplexed

address and data bus for external memory. The strobe and handshake, parallel I/O ports B and C can be regained in expanded-memory mode using an MC68HC24 Port Replacement Unit.

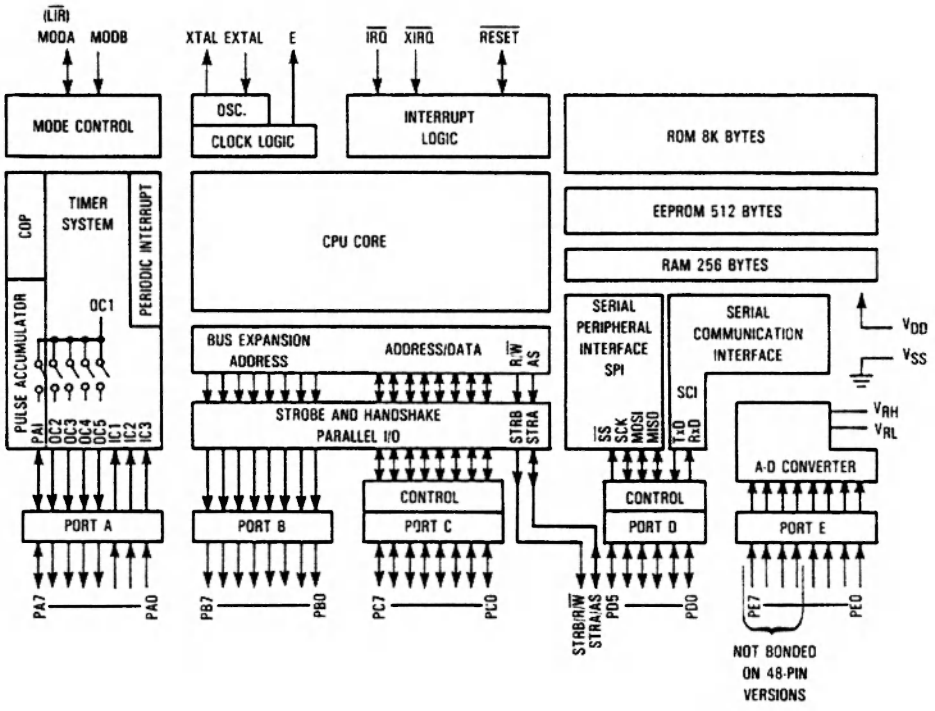


Figure 2 Functional Block Diagram of MC68HC11A8 Single-Chip Microcomputer (Courtesy of Motorola[3])

The MC68HC11A8 has both synchronous and asynchronous serial communication interfaces. The synchronous communication interface, called the serial peripheral interface (SPI), supports full duplex, three-wire synchronous transfers at up to one million bits per second in master mode or 2 million bits per second in slave mode.

The asynchronous communication interface, called the serial communication interface (SCI), provides full duplex, two-wire, NRZ compatible communication at any of 32 programmable baud rates up to 131K Baud. Both serial interfaces are accessed through six of port D's I/O pins. The remaining two pins of port D are used as the strobe and handshake control lines for parallel communication.

Port E has eight input lines on the MC68HC11A8's 52-pin version but only four input lines on the 48-pin version. These input lines can serve as either general purpose, digital input lines or as analog input channels to the MC68HC11A8's on-chip A/D converter.

On-Chip A/D Converter

Another outstanding feature of the MC68HC11A8 is its on-chip, 8-bit, unipolar ADC. The MC68HC11A8 converts either one or four of its eight analog input channels to 8-bit digital values during each 16 E-cycle A/D conversion. Its sample-and-hold input stage reduces errors caused by time varying input signals during the successive approximation conversions. In addition to eight multiplexed analog input channels, two voltage reference input lines, VRH and VRL, are used by the MC68HC11A8 to provide true ratiometric A/D conversions.

Product specifications of the MC68HC11A8's ADC claim that conversions performed within the range 0 Vdc to +5 Vdc, contain no non-monotonicities, no missing codes, and integral non-linearity of less than $\pm 1/2$ least significant bit (LSB).[3]

In an attempt to validate Motorola's claim, static ADC tests were performed on the MC68HC11A8's ADC under various operating conditions. The static ADC test method described in Doerfler's MS thesis was used to obtain 1024-point transfer function data (digital output code vs. analog input voltage).[4] The following absolute error plots were then calculated by finding the difference between the ADC's digital output code and the ideal digital output code.

Four typical absolute error plots of the MC68HC11A8's ADC are shown in Figures 3 through 6. The data for Figure 3 was obtained with a crystal frequency of f_{XTAL}= 8.0 MHz and the internal RC timer disabled (CSEL=0). The next two results represent a crystal frequency of f_{XTAL}= 4.0 MHz, with and without the RC timer disabled. The last figure (Figure 6) was obtained with a 2.0 MHz crystal frequency and the RC timer enabled.

The accuracy of the MC68HC11A8's ADC is closely related to the MC68HC11A8's operating frequency. At crystal frequencies of 4.0 MHz or below and with the RC timer enabled, the absolute error remains below ± 1 LSB but it contains missing codes and non-monotonicities. At

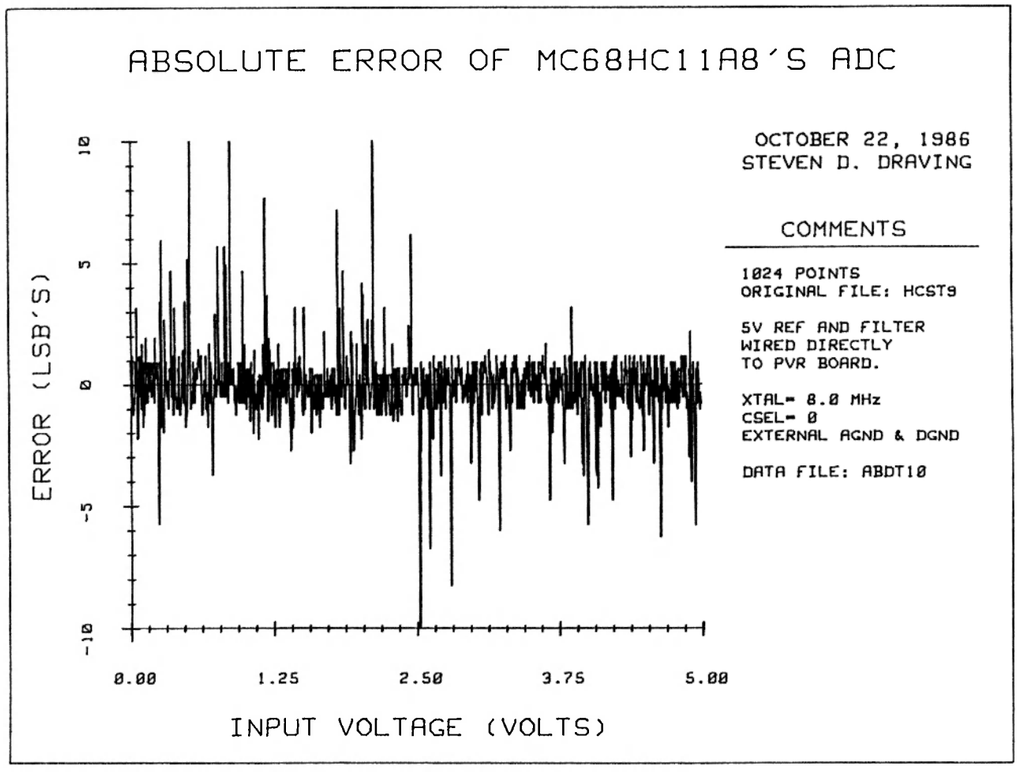


Figure 3 Plot of Absolute Error of MC68HC11A8's ADC: f_{XTAL}= 8.0 MHz, RC Timer Disabled

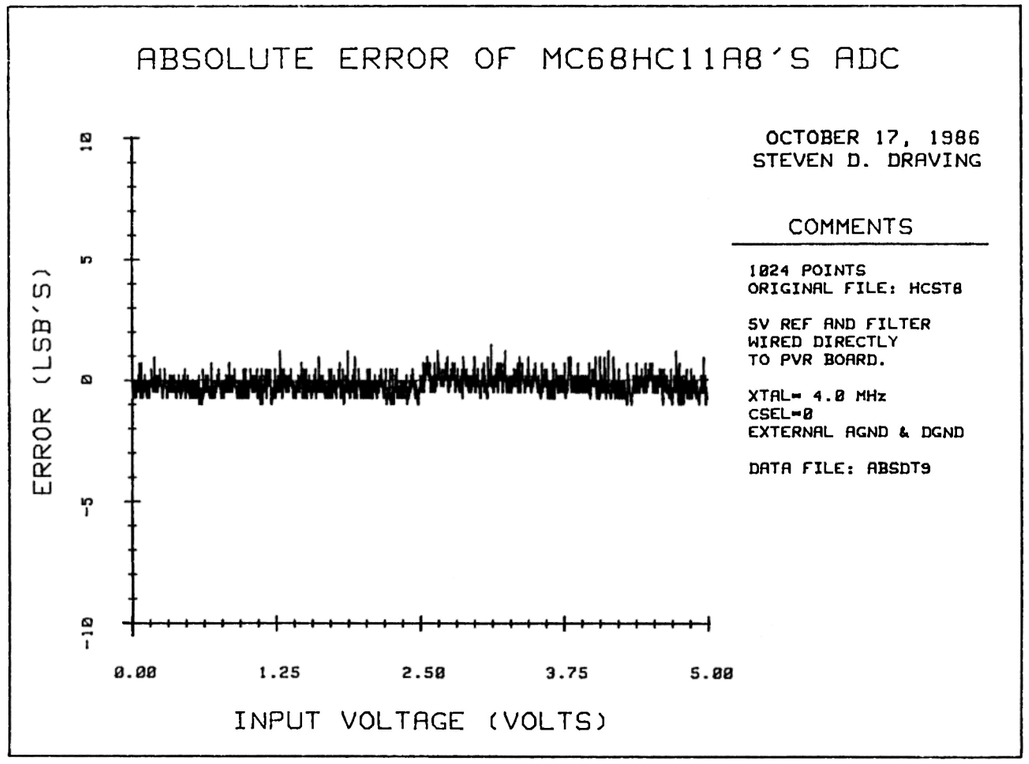


Figure 4 Plot of Absolute Error of MC68HC11A8's ADC: f_{XTAL}= 4.0 MHz, RC Timer Disabled

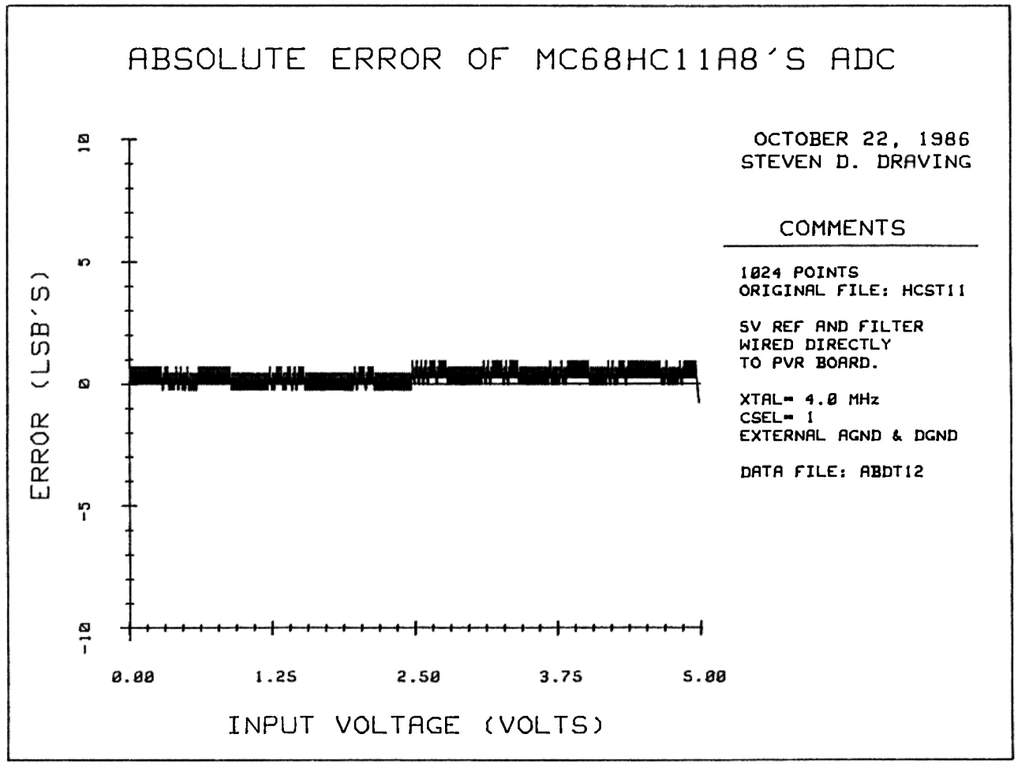


Figure 5 Plot of Absolute Error of MC68HC11A8's ADC: f_{XTAL}= 4.0 MHz, RC Timer Enabled

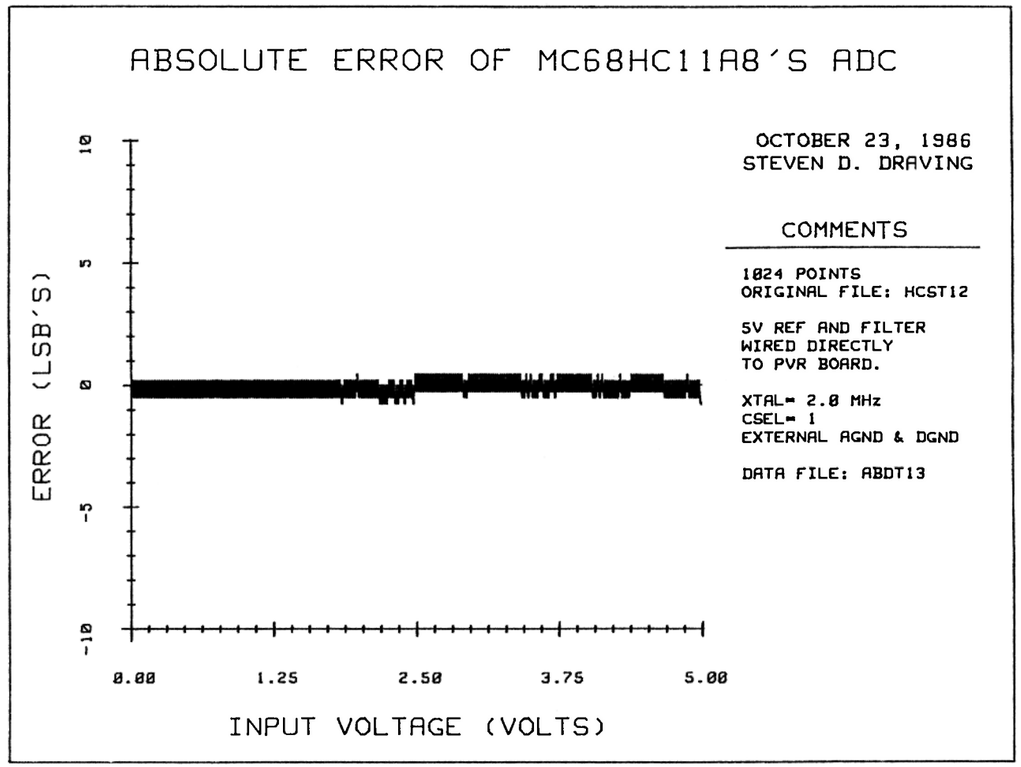


Figure 6 Plot of Absolute Error of MC68HC11A8's ADC: f_{XTAL}= 2.0 MHz, RC Timer Enabled

frequencies above 4.0 MHz and with the RC timer disabled, the absolute error increases to as high as 10 LSBs.

Unlike integrating-type ADCs, successive approximation ADCs are very susceptible to noise. Therefore, great care must be taken to shield the MC68HC11A8's ADC from its noisy microprocessor environment. All ADC tests were performed using the MC68HC11A8 evaluation system (EVS) described in Appendix A. Because the entire EVS is wire-wrapped and because the components are packed closely together, the EVS is very noisy. In fact, the EVS could be noisy enough to produce the errors observed in the four absolute error plots. But considering that the evaluation was performed on preproduction models of the MC68HC11A8, the source of the ADC's error is not obvious. In order to determine if the observed errors are caused by the MC68HC11A8's ADC or by the noisy EVS, additional static ADC tests should be performed using newer MC68HC11A8 models on a "quieter" printed-circuit version of the EVS.

Power Consumption

The MC68HC11A8's low power consumption makes it ideal for battery-powered ADC applications. The MC68HC11A8 utilizes HCMOS technology to achieve 8 MHz crystal clock frequencies with less than 100 mW average power consumption in single-chip mode.

As with all CMOS logic devices, the power consumption of HCMOS devices are directly proportional to their operating frequencies. Motorola takes full advantage of HCMOS's linear power consumption characteristics by designing the MC68HC11A8 to be completely static. As a static logic device, its crystal clock frequency can be reduced all the way to dc for ultra-low power consumption applications.

Other low-power features of the MC68HC11A8 include device disabling and programmable low-power operating modes. Power consumption can be reduced by disabling some on-chip peripheral devices such as the ADC or SPI. The wait and stop operating modes also reduce power consumption. Entering wait mode disables the timer interrupt and processor "watch dog" systems and halts program execution. Stop mode reduces power consumption even further by disabling all internal clocks and timers. In either mode, normal execution is resumed after either of the external interrupts (IRQ, XIRQ) occur.

A quantitative relationship between the MC68HC11A8's power consumption and operating frequency is not currently available from Motorola. Therefore, the test system shown in Figure 7 was constructed to determine the power/frequency relationship for a typical MC68HC11A8 device.

Simultaneous supply voltage and supply current measurements were acquired at various processor operating frequencies using a dc voltmeter and a dc ammeter. The MC68HC11A8's average power was calculated using equation 1 and then recorded.

$$P_{AVE} = I_{SUPPLY} \times V_{SUPPLY} \quad (1)$$

Power consumption tests were performed for run, wait, and stop modes of the MC68HC11A8 and the results were then graphed (Figures 8 and 9).

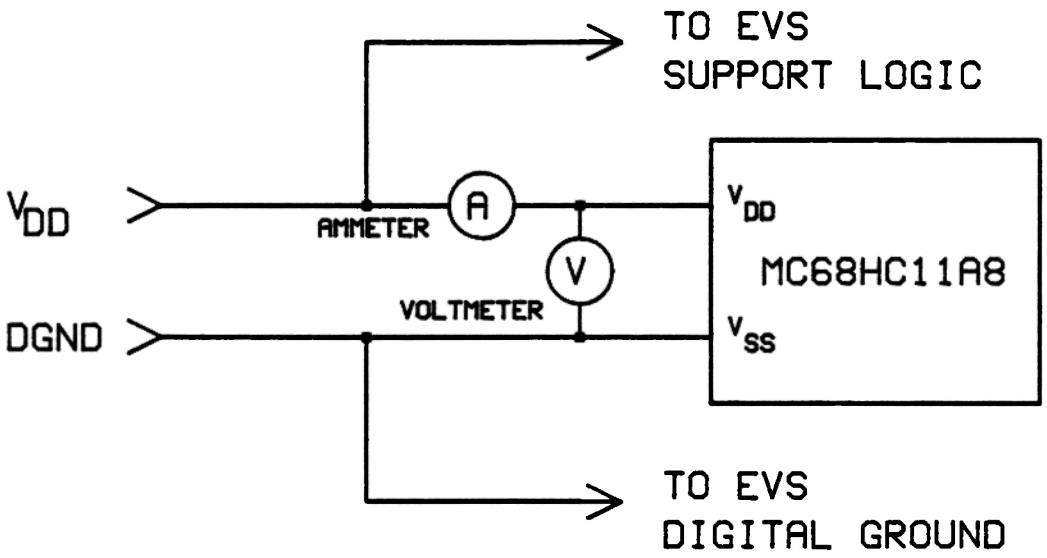


Figure 7 Functional Block Diagram of Power Consumption Test System

Figure 8 shows that the MC68HC11A8's average power consumption in wait mode is approximately half of that in

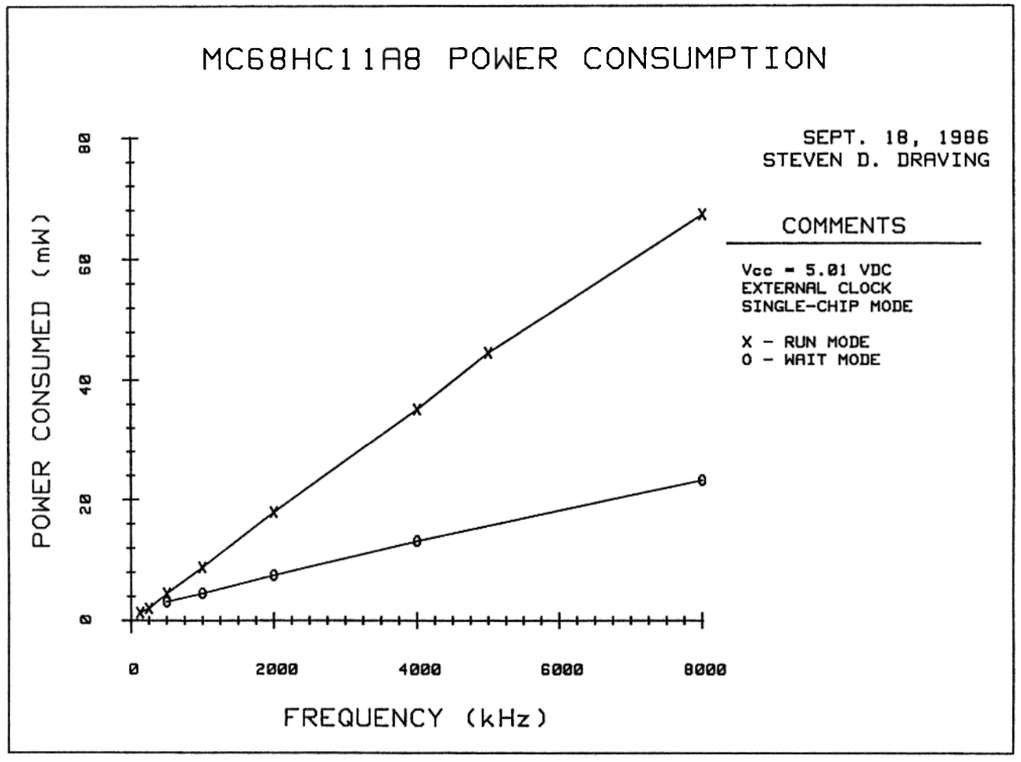


Figure 8 Plot of MC68HC11A8's Power Consumption: Wait Mode vs. Run Mode

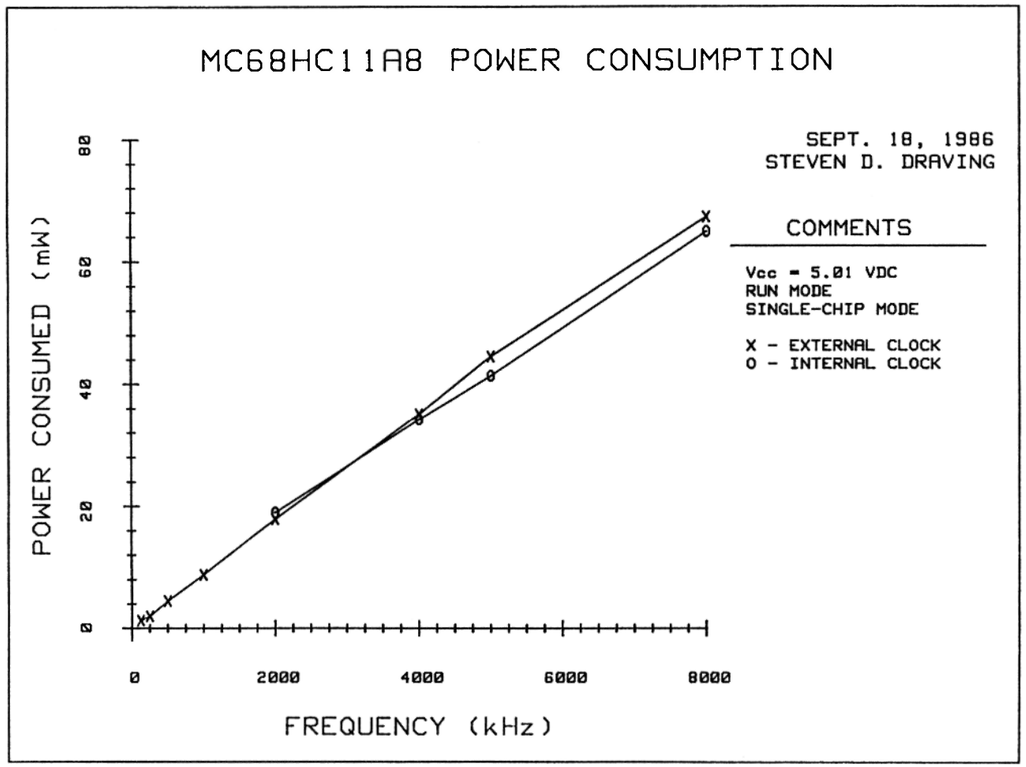


Figure 9 Plot of MC68HC11A8's Power Consumption: Internal Clock vs. External Clock

run mode. Average power consumption in stop mode (not shown in Figure 8) is approximately 0.43 mW for all external clock frequencies. Figure 9 compares the MC68HC11A8's average power consumption when operating with the internal clock circuit and when operating with an external square wave clock signal. Power measurements were also collected for the MC68HC11A8 in expanded-memory mode. The MC68HC11A8's power consumption in expanded-memory mode equaled that in single-chip mode and therefore was not graphed.

Analysis and Discussion

For control applications of any kind, the MC68HC11A8 has a definite functional advantage over other 8-bit microprocessors currently available. In single-chip mode, the MC68HC11A8 provides a significant physical size advantage over conventional microprocessor systems. The central processing unit's (CPU's) extended instruction set supports several 16-bit operations and direct bit manipulation for creating fast and efficient control programs. The interrupt timer system performs several operations such as waveform generation, pulse accumulation, and elapsed-time measurements almost independently of processor control so that several I/O operations can be performed simultaneously. The one parallel and two serial communication interfaces allow communication with many

different devices. The MC68HC11A8 can even function as a translator between two devices of differing communication methods.

Although the MC68HC11A8 may be the most powerful 8-bit single-chip microcomputer available, it could be better. If the EEPROM programming voltage was reduced from $1.8V_{DD}$ to $1.0V_{DD}$, then the MC68HC11A8 would require only one supply voltage, +5 Vdc. Another improvement would be to add a programmable clock circuit which could toggle one I/O pin independently of CPU control. This clock could be enabled and disabled to drive digital circuits at programmable frequencies.

Controlling the Existing RDB DAS

Ragsdale[1], Doerfler[4], and Bradley[2], recent MSEE graduates from Kansas State University have developed a low-power, 15-bit data acquisition system (DAS). The Ragsdale-Doerfler-Bradley (RDB) DAS, named after its designers, performs A/D conversions on two simultaneously sampled analog inputs at a rate of 128 samples/second and with a total power consumption of 36.5 mW. The RDB DAS utilizes error correction and power switching techniques to provide high resolution at low power consumption. However, the DAS's high performance is achieved at the expense of large physical size. The RDB DAS requires two, 3 1/2 in X 6 in, 6-layer printed circuit boards.[1 2 4] The following design revision attempts to reduce the existing RDB DAS's physical size by replacing its original microprocessor and control logic with the MC68HC11A8 Single-Chip Microcomputer.

Original RDB DAS

A functional block diagram of the original RDB DAS is shown in Figure 10. Figure 10 separates the DAS into four functional blocks; power supply filtering and switching network, two-channel track-and-hold, microprocessor and control logic, and 15-bit bipolar sign-magnitude successive approximation ADC.

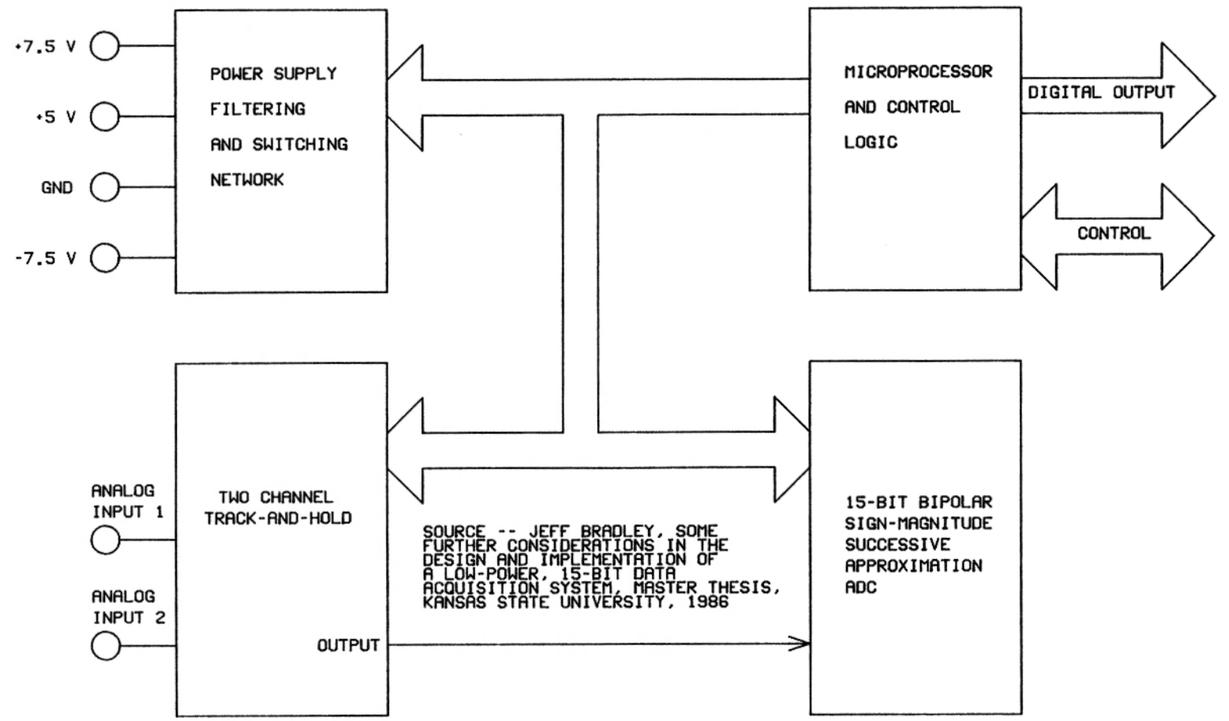


Figure 10 Functional Block Diagram of Original RDB DAS (Reproduced from Harbour's MS Thesis[5])

The power supply filtering and switching network is directly controlled by the microprocessor to supply power to the DAS's analog components only while necessary. The two-channel track-and-hold is also controlled by the microprocessor. Input signals are simultaneously sampled by the track-and-hold and then sequentially passed to the 15-bit ADC upon request by the microprocessor. For each analog input held by the track-and-hold the 15-bit ADC converts the analog voltage to an equivalent sign-magnitude digital value. Partially controlled by the microprocessor, the 15-bit ADC first determines and records the analog input's sign. The input's magnitude is then determined using a unipolar successive approximation procedure of the same polarity as the input's sign. The microprocessor converts both sign-magnitude conversion values (one from each input channel) to two's-complement form, corrects the values for errors and stores the 15-bit two's-complement results in four 8-bit output latches to be accessed by a host system.

Schematics, parts lists, and timing diagrams for the original RDB DAS are provided in Appendix B. A detailed functional description of the original RDB DAS can be found in Bradley[2].

MC68HC11A8 Controlled RDB DAS

The MC68HC11A8 controlled RDB DAS functions essentially the same as the original RDB DAS except for the method in which the SAR's output is read from the analog board. The sign bit for each MC68HC11A8 controlled conversion is passed directly to port D of the MC68HC11A8 using the dedicated data line, SIGN. The 14-bit magnitude of each MC68HC11A8 controlled conversion is passed serially to the MC68HC11A8's synchronous SPI interface using the MOSI data line. The original RDB DAS passed the SAR's output to its digital section through two octal latches, U1 and U2 (see Circuit Diagram of Original RDB DAS Analog Section, Appendix B).

Controlling the RDB DAS with the MC68HC11A8 requires only three modifications to the original RDB DAS analog board (Figure 11). The CLOCK synchronization signal used by the RDB DAS's analog section and the MC68HC11A8's synchronous SPI interface is generated by dividing the MC68HC11A8's E clock signal by two with the unused half of the RDB DAS's D-type flip-flop, U11. Since the SAR's output is now read serially, the two octal latches, U1 and U2 can be eliminated. The last RDB DAS modification requires using one of the unused exclusive NOR-gates of U23 to form the MOSI output signal from the combination of the SH and SL serial SAR outputs.

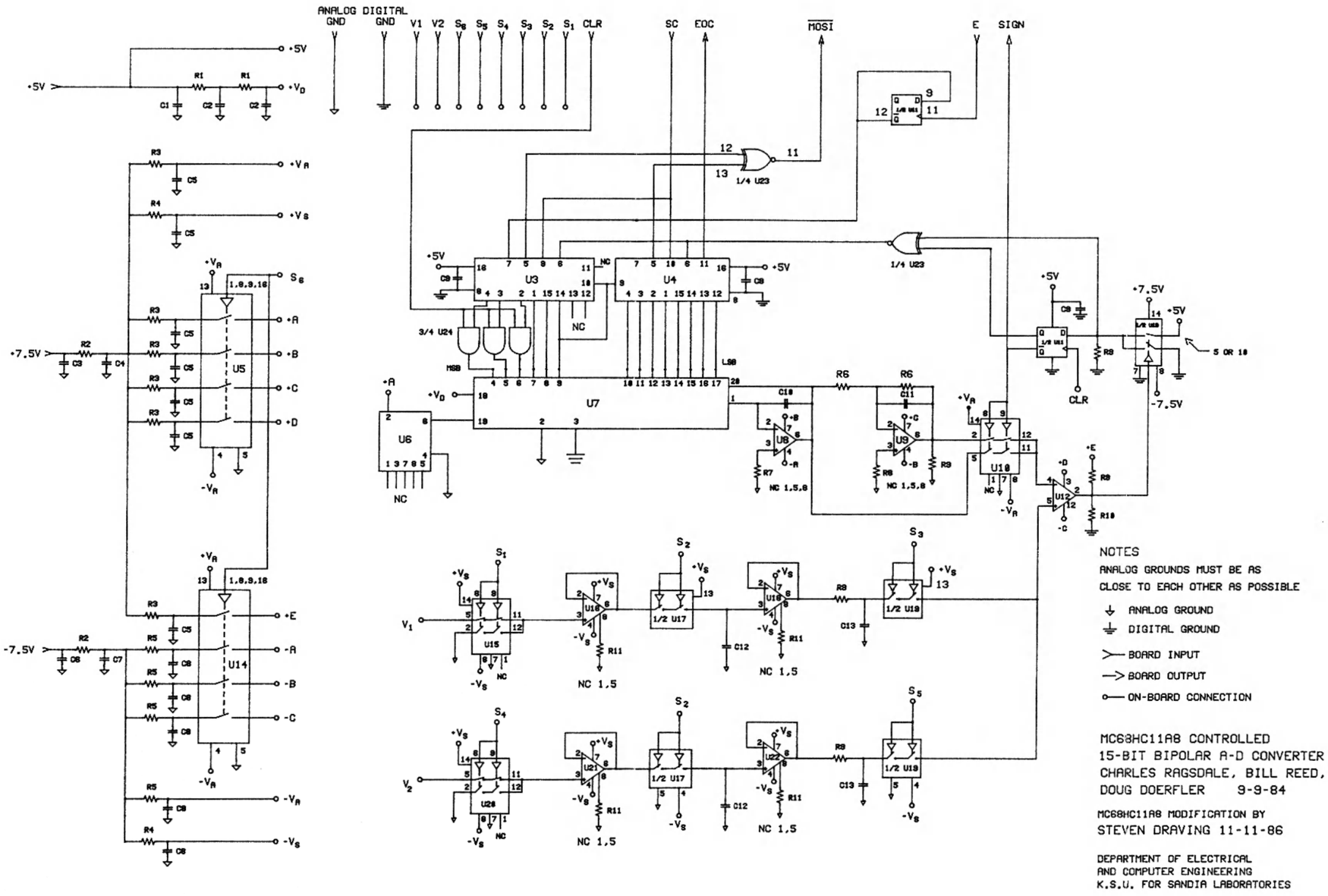


Figure 11 Circuit Diagram of MC68HC11A8 Controlled RDB DAS Analog Section

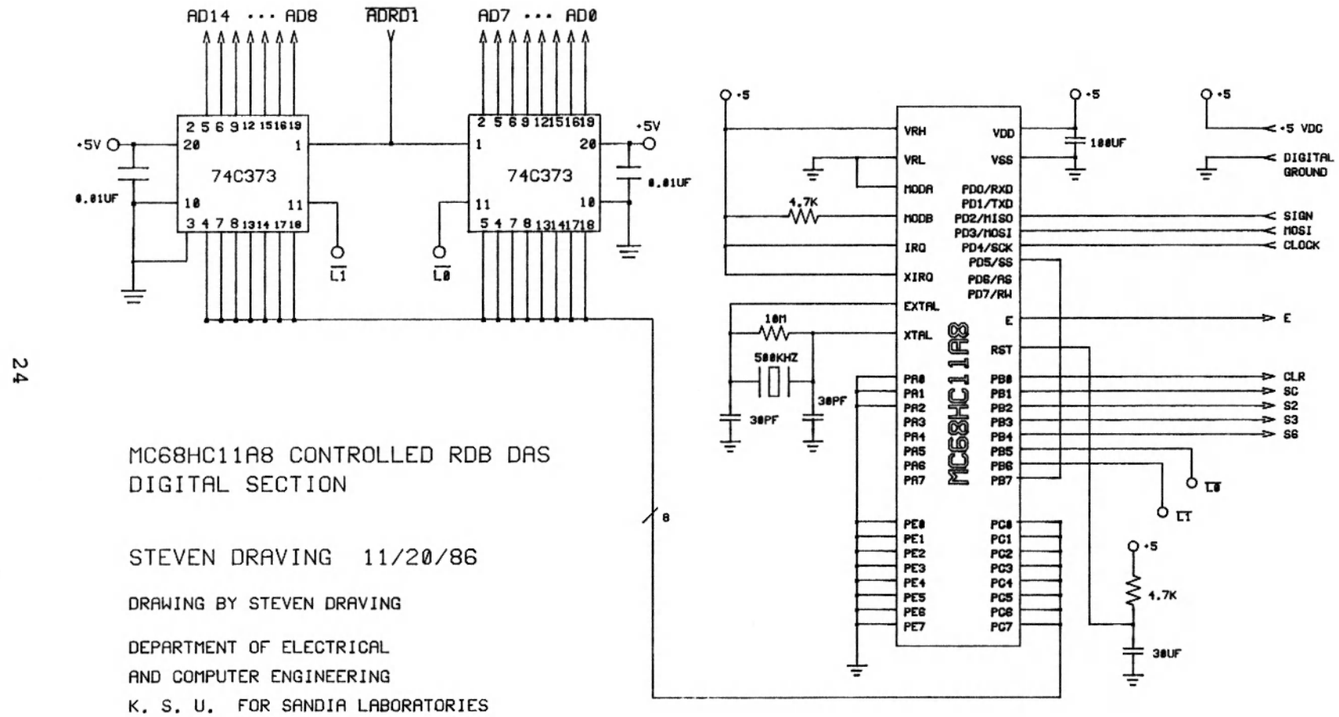


Figure 12 Circuit Diagram of MC68HC11A8 Controlled RDB DAS Digital Section

The MC68HC11A8 replaces everything on the RDB DAS's digital board except the four output latches, U1-U4 (Figure 12). Schematics, parts lists, a timing diagram and a program listing for the MC68HC11A8 controlled RDB DAS are provided in Appendix C.

Testing the MC68HC11A8 Controlled RDB DAS

The test system of Figure 13 was used to verify the MC68HC11A8's correct control of the RDB DAS. For simplicity, the MC68HC11A8 controlled RDB DAS's digital section (Figure 12) was not constructed and the MC68HC11A8 evaluation system (Figure A-1) was used to control the modified RDB DAS analog section (Figure 11). During testing, the MC68HC11A8 was configured for expanded-memory mode with ports B and C replaced by the MC68HC24 Port Replacement Unit. An external 500 kHz square-wave was used to drive the MC68HC11A8's internal processor.

The assembly language program ADCSE (source listing located in Appendix C) was written for the MC68HC11A8 to control the RDB DAS analog board during single A/D conversions and then transmit each conversion result over the MC68HC11A8's asynchronous SCI communication interface. Upon execution, ADCSE initializes all internal registers and I/O ports, performs one conversion, and then waits for keyboard input from the data terminal. Additional conversions are performed by pressing the terminal's

carriage return key. Pressing the carriage return key corresponds to sending an ASCII 13 over the serial communication line. When the carriage return key is pressed, ADCSE performs a conversion on analog input channel one and then sends the 2's-complement digital result back to the terminal over the serial interface line. ADCSE is terminated by pressing the line feed key on the data terminal or sending an ASCII 10 over the serial communication line.

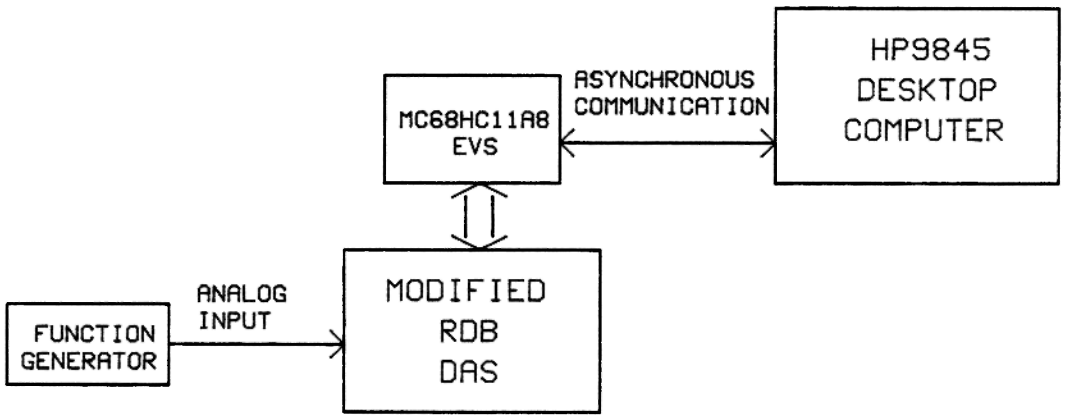


Figure 13 Functional Block Diagram of MC68HC11A8 Controlled RDB DAS Test System

Using the test system of Figure 13, several conversions were performed and the results were then compared to the conversion results from the original RDB DAS. Both RDB DAS's produced similar results, verifying the MC68HC11A8's successful control of the RDB DAS.

Analysis and Discussion

The MC68HC11A8 was shown to successfully control the RDB DAS and reduce the DAS's size by four 20-pin, one 16-pin, one 24-pin, and one 40-pin dip IC packages. Although only five IC chips remain on the MC68HC11A8 controlled RDB DAS digital board, the entire DAS will still not fit on a single 3 1/2 in X 6 in printed-circuit board (PCB). One possible way to reduce the entire DAS to a single PCB, is to replace the four MM74C373 octal output latches with one MCM68HC34 Dual-Port RAM Memory Unit. Using the MCM68HC34 as an output latch limits the output to 8-bit words but it requires only half the board space as the existing four output latches require.

Doerfler calculated the original RDB DAS optimum power consumption to be approximately 28 mW.[6] Based on similar calculations, the MC68HC11A8 controlled RDB DAS's optimum power consumption is 30 mW. The 2 mW power consumption difference can be significant for some low-power DAS applications. However, the physical size and weight differences between the two RDB DAS's may prove more significant. This MC68HC11A8 application demonstrates that the MC68HC11A8 can reduce a microprocessor controlled ADC's physical size and weight without significantly increasing its power consumption.

Low-Power, Precision ADC Techniques

The following four A/D conversion techniques demonstrate the MC68HC11A8's versatility as an ADC controller. Version 1 utilizes an 8-bit digital-to-analog converter (DAC) and the MC68HC11A8's on-chip 8-bit ADC in a two-stage, successive approximation A/D conversion process. Version 2 is similar to version 1 except that the 8-bit DAC, differential amplifier, and sample-and-hold (S/H) are replaced by an 8-bit switched-capacitor sample-and-hold (SCSH). In version 3, the MC68HC11A8 pre-scales the analog input voltage by applying a successive approximation procedure to a 4-bit SCSH. The SCSH pre-scaler effectively increases the accuracy of the "follow-up" 12-bit integrating ADC to 15 bits. Version 4 uses a 3-bit SCSH as a pre-scaling S/H for a "follow-up" 13-bit successive approximation ADC.

All four ADCs perform 15-bit conversions on analog input voltages ranging from -5 V to +5 V. Each can perform at least 1000 conversions per second with approximately 50 mW average power consumption. Although not evident from the functional block diagrams, each design uses power switching of its analog components to reduce power consumption. The power consumption of the MC68HC11A8 itself is also reduced through the careful selection of operating frequencies and use of its low-power operating

modes.

Because of the two-stage nature of each ADC technique, there is a 1-bit "overlap" between the number of bits resolved by each stage. This 1-bit overlap insures continuity between the two conversion ranges. In addition, error correction is available to each design in order to guarantee 15-bit linearity.

ADC Version 1

ADC Version 1 is a two-stage ADC which utilizes the MC68HC11A8's on-chip 8-bit ADC to perform 15-bit A/D conversions (Figure 14). Stage 1 of the conversion determines the most significant eight bits of the conversion. Stage 2 determines the remaining bits.

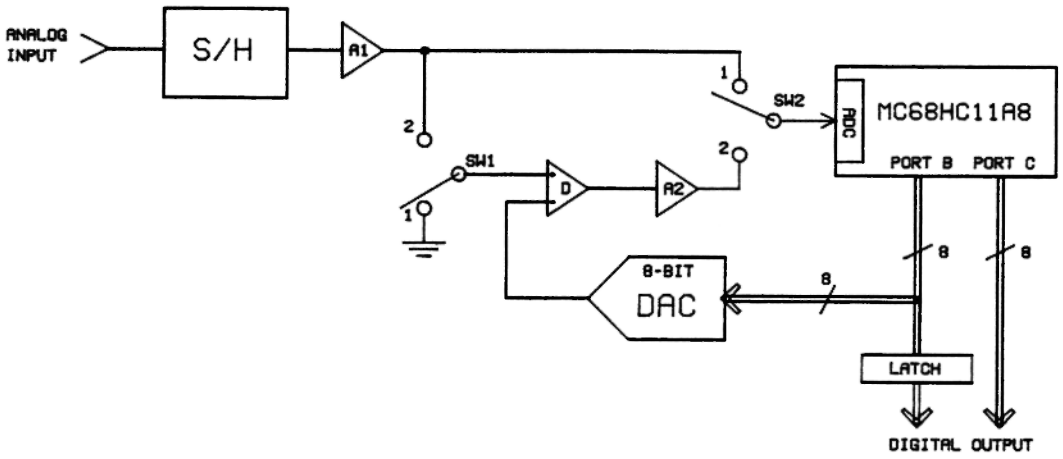


Figure 14 Functional Block Diagram of ADC Version 1

Theory of Operation. Throughout the entire conversion the analog input voltage held by the sample-and-hold (S/H) is conditioned by amplifier A1. Amplifier A1 maps the desired analog input voltage range to the MC68HC11A8's ADC input range, 0 V to 5 V. During Stage 1 of the conversion, switches SW1 and SW2 are set to position "1" and the first eight most-significant-bits (MSBs) of the 15-bit result are converted by the MC68HC11A8's ADC. During stage 2, switches SW1 and SW2 are moved to position "2" and the 8-bit digital result from stage 1 is converted back into an analog voltage by the 8-bit digital-to-analog converter (DAC). The differential amplifier, D reduces the conditioned analog input voltage by an amount equal to the first eight MSBs. The residual voltage from the differential amplifier is amplified 256 times by amplifier A2 and then converted by the MC68HC11A8's ADC. The most significant seven bits of the final result are then stored in an 8-bit D-type latch. The remaining bits are stored in port C and the MC68HC11A8 returns to one of its low-power operating modes, wait or stop. The final result is stored in the 8-bit latch and port C so that the host system can access the entire 15-bit result as a single 15-bit word. This allows the ADC to begin performing the next conversion before the result from the previous conversion has been read by the host system.

Design Considerations. ADC version 1 is a fairly simple circuit to implement providing sufficiently fast, low-noise analog components are available. Choosing the correct analog components for all four designs is very critical because power-switching requires fast settling times and high-precision (1 LSB = 0.305 mV) requires high power supply noise rejection. Components with these characteristics can be found but their power consumptions are normally very large.

Since version 1 uses several power consuming analog components, its power-switching duty cycle must be small to obtain low average power consumption. The MC68HC11A8's ADC must perform two 8-bit conversions for each 15-bit result. Each conversion requires a maximum of only 0.032 ms so the power switching duty cycle for version 1 can be kept low. In addition, the MC68HC11A8's operating frequency can be kept very low because very little control is required. This also reduces overall power consumption because the MC68HC11A8's power consumption is directly related to its operating frequency.

ADC Version 2

ADC Version 2 is also a two-stage ADC which operates very similarly to version 1 (Figure 15). The only difference between version 1 and version 2 is that version 2 holds the input voltage and subtracts the first

eight MSBs from the input voltage using an 8-bit switched-capacitor sample-and-hold (SCSH).

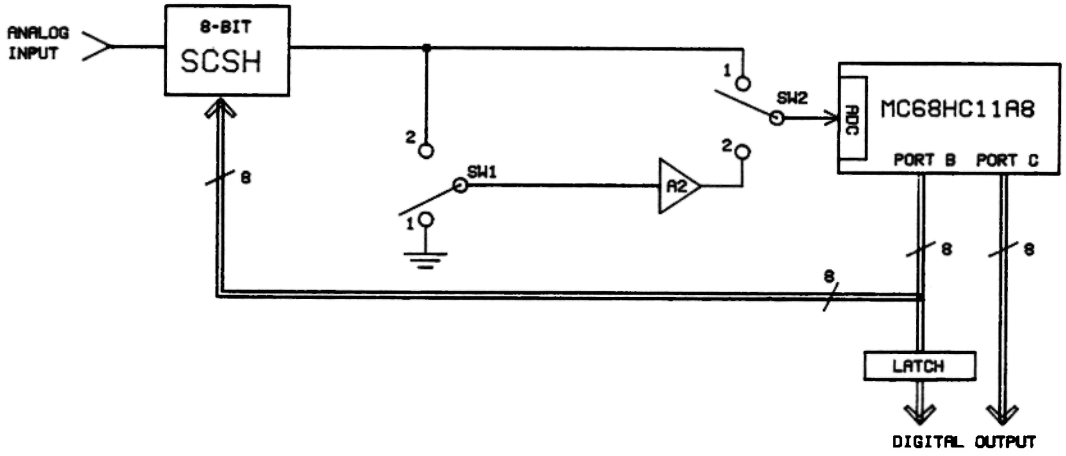


Figure 15 Functional Block Diagram of ADC Version 2

The SCSH used in three of the four ADC designs is actually a modified dual-reference version of the switched-capacitor ADC developed by McCreary and Gray.[7] The SCSH described in this thesis is a binary weighted, switched-capacitor array which samples a bipolar input voltage onto its common plate and then subtracts binary weighted voltages from the sampled voltage using charge redistribution. A detailed description of the SCSH is presented in Harbour.[5]

Design Considerations. ADC version 2 performs conversions with the same duty cycle as version 1 but using

far less analog components. Therefore the power consumption and physical size of version 2 is much less than that of version 1. Replacing the analog components with the SCSH does reduce power consumption but also requires the use of a 256 element "look-up" table for correcting the SCSH's capacitor ratio errors. This look-up table would be fast and easy to use during an actual conversion but would be very time consuming to generate for an autocalibrating ADC.

ADC Version 3

ADC version 3 can be treated as a 12-bit integrating ADC with a very small input voltage range and a 4-bit SCSH pre-scaler (Figure 16).

Theory of Operation. The MC68HC11A8 controls ADC version 3 as follows. First the analog input voltage is held by the bipolar SCSH. Then with switch SW1 set to position "1", the MC68HC11A8 controlled SCSH reduces the analog input voltage to the 12-bit integrating ADC's allowable input range using a successive approximation procedure. Switch SW1 is moved to position "2". The reduced analog input voltage is amplified to the integrating ADC's true input range and then converted to a 12-bit digital value. Finally, the 4-bit SCSH result and the 12-bit ADC result are combined, error correction is performed if necessary and the 15-bit digital result is

stored in the output data latch.

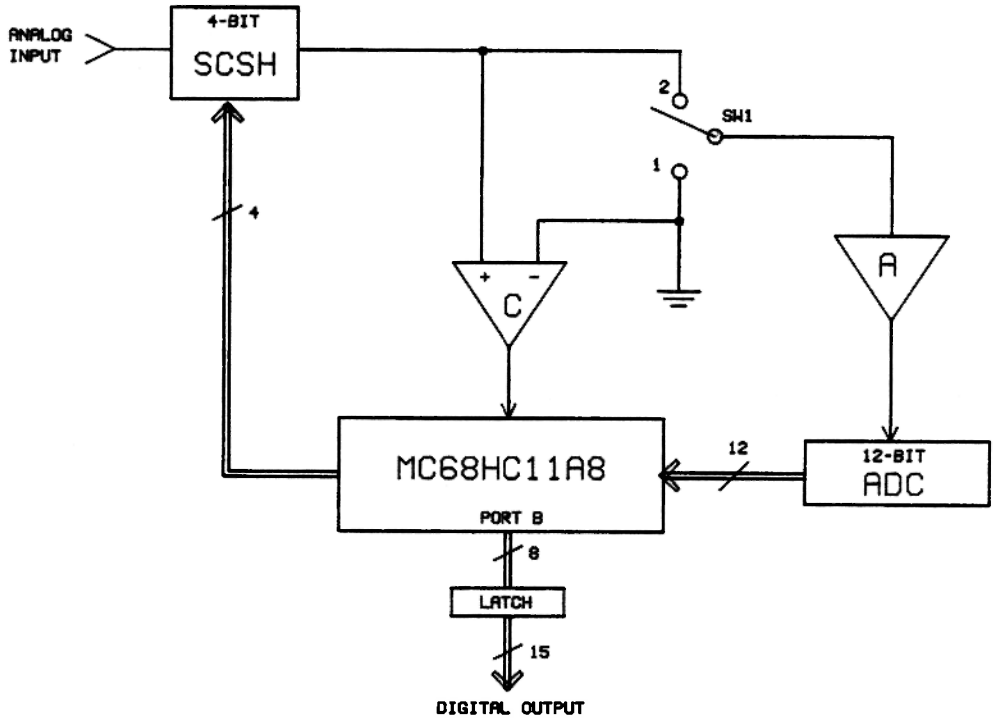


Figure 16 Functional Block Diagram of ADC Version 3

Design Considerations. The static ADC test performed on the MC68HC11A8's ADC as part of its evaluation suggested that the MC68HC11A8's ADC is very susceptible to noise. For this reason, ADC versions 3 and 4 do not use the MC68HC11A8's ADC. In addition, version 3 utilizes a self-contained integrating ADC to further reduce the effects of noise. A four bit SCSH is used in version 3 to reduce the size of the error correction look-up table and to reduce the conversion time required to determine the first four bits of the conversion. Although version 3

would be fairly easy to implement and the effects of noise are small, it requires more board space and consumes more power than the other ADC versions discussed.

ADC Version 4

ADC version 4 is similar to version 3 except that the 12-bit integrating ADC is replaced by a 13-bit successive approximation ADC and the 4-bit SCSH is reduced to three bits (Figure 17).

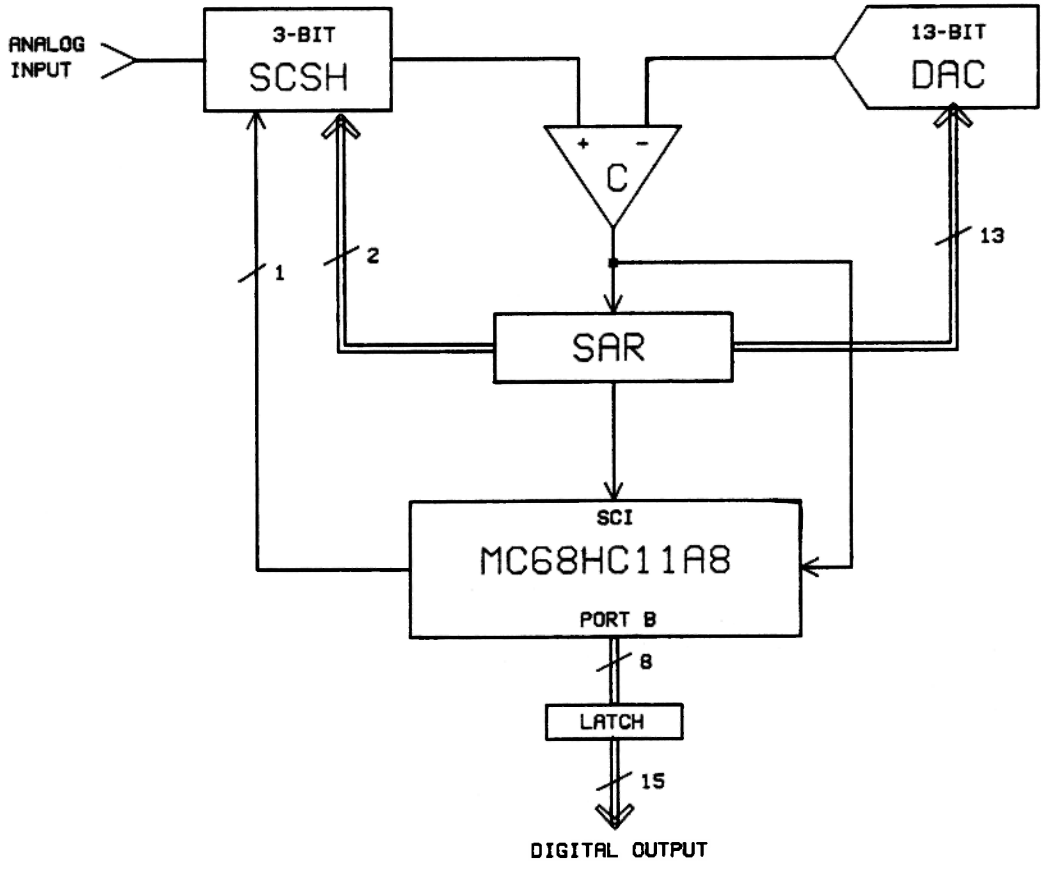


Figure 17 Functional Block Diagram of ADC Version 4

Theory of Operation. Initially, the successive approximation register (SAR) is cleared and the SCSH holds the analog input voltage. The first MSB is converted manually by the MC68HC11A8 using a successive approximation procedure and then the remaining bits are converted automatically by the SAR. The DAC's output is 0 Vdc while the SCSH's three bits are being converted. The remaining bits are then converted such that the DAC's output voltage equals the SCSH's output voltage. During the successive approximation procedure, each bit determined by the SAR is read into the MC68HC11A8 through the SPI synchronous communication interface. Error correction is performed on the resulting 15-bit value and the 15-bit digital result is stored in the output data latch.

Design Considerations. Although ADC version 4 requires a longer duty cycle than the previous versions, it has very few analog components to consume power. Since only three bits are converted by the SCSH, the error correction look-up table need only contain eight elements.

The control required by the MC68HC11A8 to perform each conversion is much more complicated than it is for the other ADC versions. However, version 4 appears to have the best chance of resolving all 15-bits with the lowest average power consumption. In fact, ADC version 4 was chosen as the next generation low-power data acquisition system to be pursued by Kansas State University's on-going

research of low-power systems. A detailed description of the SCSH DAS's design and preliminary test results is presented in the following section of this thesis.

Controlling the SCSH DAS

The ADC techniques discussed in the second section of this thesis represent a fairly new approach to A/D conversion. Each ADC technique converts several of its most significant bits into a digital value and then subtracts their analog equivalent from the input voltage. The resulting difference called a residue, is also converted to a digital value. The two results are then combined to form the final digital output value.

The four ADC schemes discussed in that section were designed and then evaluated as possible successors to the RDB DAS. The evaluation was based on the ADC technique's ability to meet even more demanding design specifications than those required of the RDB DAS. The design specifications of the second generation data acquisition system are listed below.

* -5 V to +5 V analog input voltage range
* two simultaneously sampled analog input channels
* 15-bit resolution
* $\pm 1/2$ LSB maximum differential linearity error
* ± 1 LSB maximum integral linearity error
* 200 Hz input signal bandwidth
* 500 Hz minimum conversion rate per channel
* 50 mW maximum average power consumption

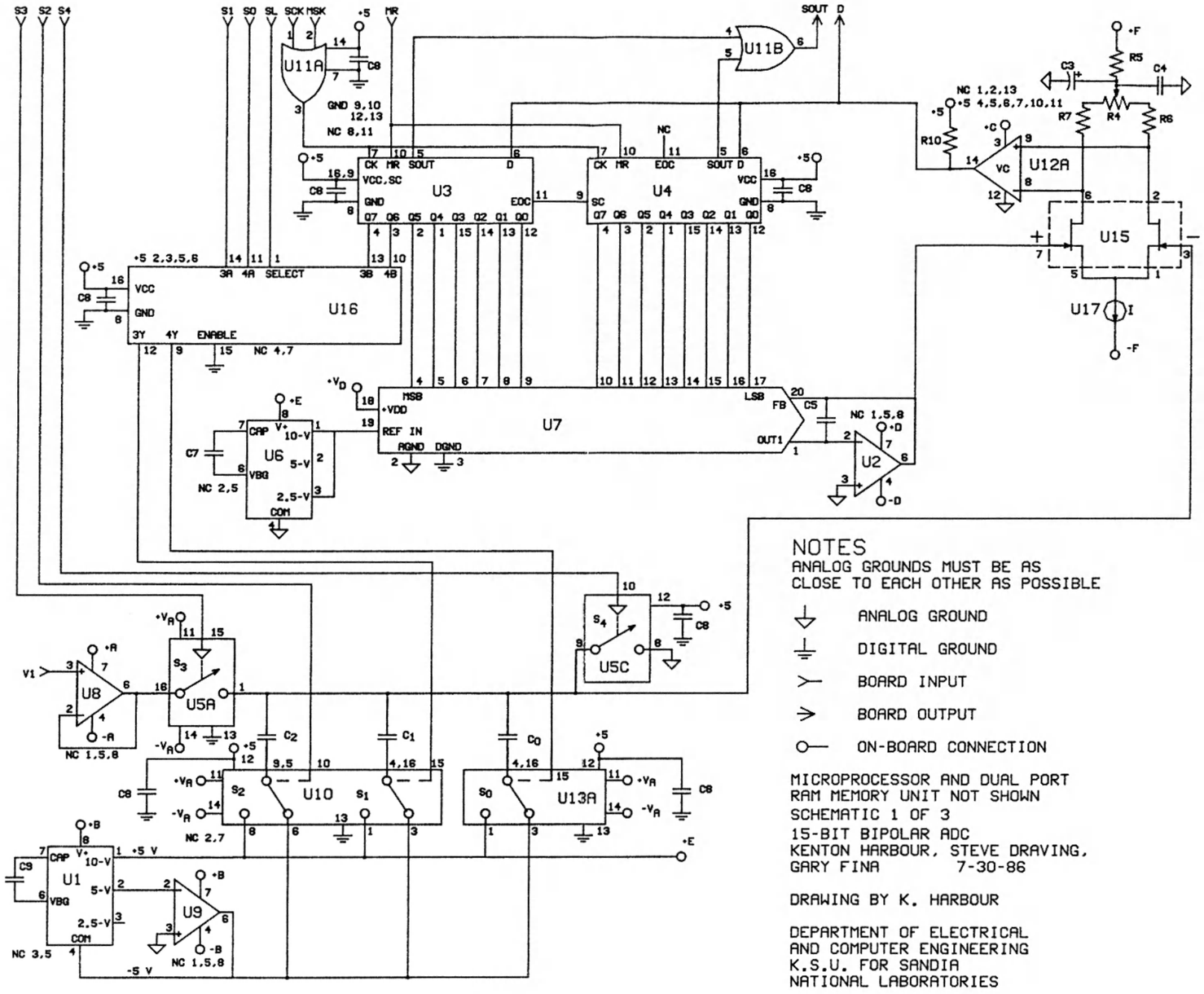
* 3" X 5" maximum required PCB board space
* fabricated from commercially available components

ADC version 4 was chosen as having the best chance of meeting all the design specifications required by the second generation DAS. As a preliminary step in the development of the new DAS, a single-channel prototype version of the switched-capacitor sample-and-hold (SCSH) data acquisition system (DAS), was constructed using the MC68HC11A8 as the controlling microcomputer. In the interest of time, only the analog portion of the SCSH DAS was constructed and the MC68HC11A8 controlled the DAS through the MC68HC11A8 evaluation system (Appendix A).

The following section of this thesis describes the SCSH DAS's operation and the MC68HC11A8's role in controlling it. A detailed description of the SCSH DAS's analog circuitry can be found in Harbour.[5]

Circuit Description

A circuit diagram of the SCSH DAS is provided in Figure 18. The analog input voltage, V1, enters the circuit through the unity gain buffer, U8. Switch S3 connects the buffered input voltage to the switched capacitor array and to the inverting input of the comparator circuit. Three switches, S0, S1 and S2, switch the SCSH capacitors between the two references. The other



NOTES

ANALOG GROUNDS MUST BE AS CLOSE TO EACH OTHER AS POSSIBLE

ANALOG GROUND

DIGITAL GROUND

BOARD INPUT

BOARD OUTPUT

ON-BOARD CONNECTION

MICROPROCESSOR AND DUAL PORT RAM MEMORY UNIT NOT SHOWN

SCHEMATIC 1 OF 3

15-BIT BIPOLAR ADC

KENTON HARBOUR, STEVE DRAVING, GARY FINA 7-30-86

DRAWING BY K. HARBOUR

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
K.S.U. FOR SANDIA NATIONAL LABORATORIES

Figure 18a Circuit Diagram of SCSH DAS Analog Section

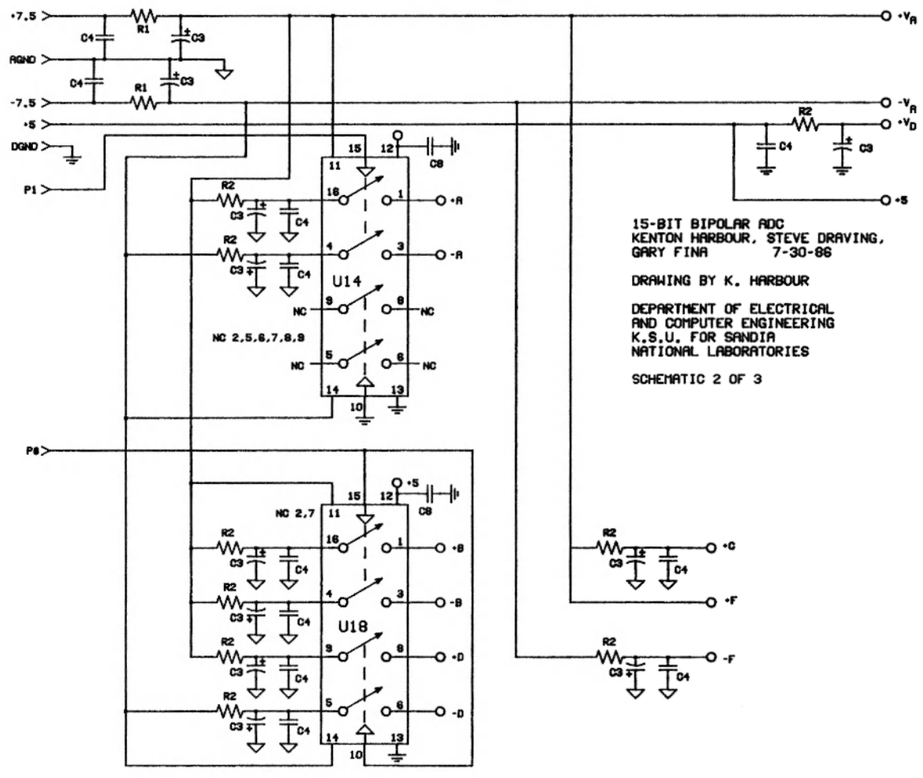


Figure 18b Circuit Diagram of SCSH DAS Power Supply Filtering and Switching Section

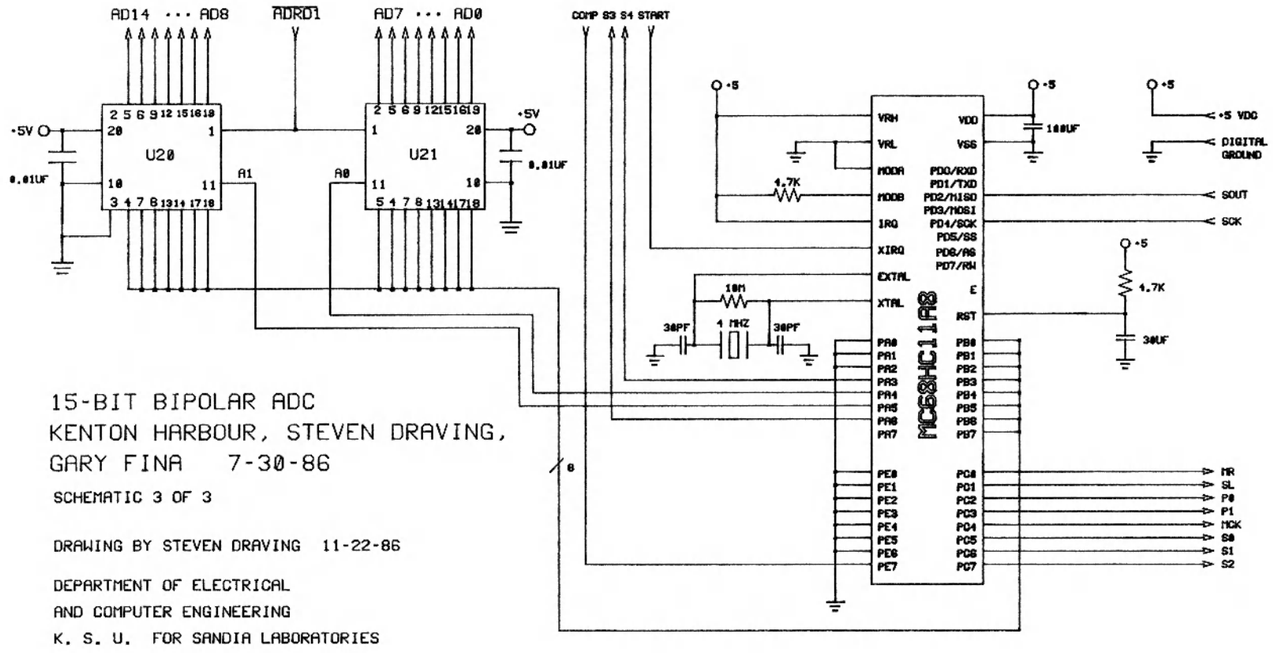


Figure 18c Circuit Diagram of SCSH DAS Digital Section

switch connected to the inverting comparator input, S4, is used only during self-calibration to ground the capacitor's common plate.

During a conversion, both the DAC and the first two LSBs of the SCSH are controlled completely by the successive approximation registers (SARs). The multiplexer, U6, allows the first two LSBs of the SCSH to be controlled directly by the MC68HC11A8 during auto-calibration but by the SARs during a normal conversion.

Two control lines, P0 and P1, are used to control the switches, U14 and U18, which connect power to the SCSH DAS's analog components (Figure 18a). P0 controls the power to the input buffer, U8, separately from all other analog components because the output buffer is used during only a small portion of the total power-switching duty cycle.

Circuit Operation

A theoretical description of the SCSH DAS's operation has already been presented in the previous section of this thesis. The following description is a detailed presentation of the control and computation required by the MC68HC11A8 to perform a single A/D conversion. Schematics of the entire SCSH DAS system are provided in Figure 18. A timing diagram of the SCSH DAS's control scheme is also

provided in Figure 19.

In order to minimize the MC68HC11A8's power consumption, the MC68HC11A8 resides in wait mode until each new conversion is requested from the host system. Conversions are requested by sending a logic low pulse to the MC68HC11A8 over the XIRQ line. A logic low XIRQ line causes the MC68HC11A8 to return from wait mode into run mode and begin executing the XIRQ interrupt service routine. The actual conversion is performed by the interrupt routine. When a conversion is complete, program execution resumes with the main program which simply returns the MC68HC11A8 to wait mode until another conversion is requested (program listing located in Appendix D).

The MC68HC11A8 begins each conversion by supplying power to all of the power-switched analog components (Figure 19). After a 6 micro-second power-up settling delay, the analog input voltage is sampled onto the common plate of the switched-capacitor array. The input voltage is sampled for 28 microseconds, switch S3 is re-opened, and then the supply power to the input buffer, U8 is removed. The output voltage of the DAC is 0 Vdc because the SARs were reset after the last conversion, so the output of the comparator (COMP line) possesses the value of the MSB for the SCSH. The MC68HC11A8 sets the MSB (S2 line) to the comparator's current output value and begins clocking the

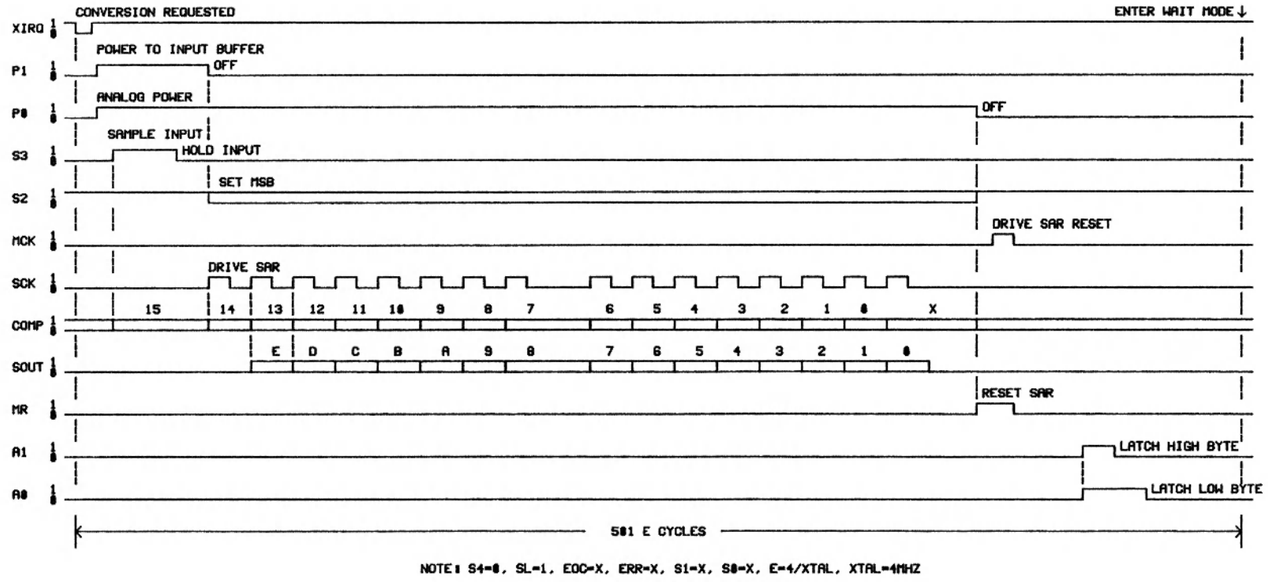


Figure 19 Timing Diagram of A Single SCSH DAS A/D Conversion

SARs through their determination of the remaining 15 bits of the conversion.

The MC68HC11A8 controls the SARs with its SPI interface. The SPI is configured for "master" mode so that it generates the SAR's driving clock signal. The SPI is also responsible for reading the SAR's serial output into the MC68HC11A8. A write to the SPI's output data register with the SPIF flag set initiates the synchronous transfer of eight data bits into the SPI's input data register. Two 8-bit transfers are required to clock the SAR's through all 15 bits of its conversion.

After all 16 bits have been loaded into the MC68HC11A8, the supply power to the remaining power-switched analog components is switched off. The SARs are then reset to all logic zeros by manually clocking the MR line's high-level state into the SARs with the manual clock (MCK) line.

In addition to controlling the analog and digital circuitry of the SCSH DAS, the MC68HC11A8 must also calculate the 15-bit digital output value from the SAR's raw output data. The final result is calculated by first appending the second 8-bit SAR result to the least significant five bits of the first 8-bit SAR result. Next, the pointer for the error correction look-up table is formed from the manually determined MSB and the two most significant bits of the first 8-bit SAR result. The error

correction pointer selects a 15-bits value to add to the 13-bit SAR result. This sum is then complemented and the resulting 15-bit, offset binary, digital output value is stored in the output data latch.

Testing the SCSH DAS

The SCSH DAS was tested using the same static ADC test procedure used to test the MC68HC11A8's ADC. A plot of the SCSH DAS's absolute error as a function of input voltage is provided in Figure 20. The stair-stepped appearance of the plot is caused by the uncorrected capacitor ratio errors of the SCSH. The capacitor ratio errors should be eliminated in future versions of the DAS when error correction is used. The "fuzzyness" of each step is caused by noise and comparator oscillation effects on the least significant six bits of each conversion.

All software errors aside, the SCSH DAS operated correctly under the MC68HC11A8's control. One problem was encountered with the analog circuit, however. The throwing of switches S0, S1 and S2 caused severe transient current demands on the bipolar voltage reference, U1. As a result, the voltage reference experiences severe voltage spikes on its positive and negative outputs. This problem was solved by placing passive RC low pass filters on each voltage reference output.

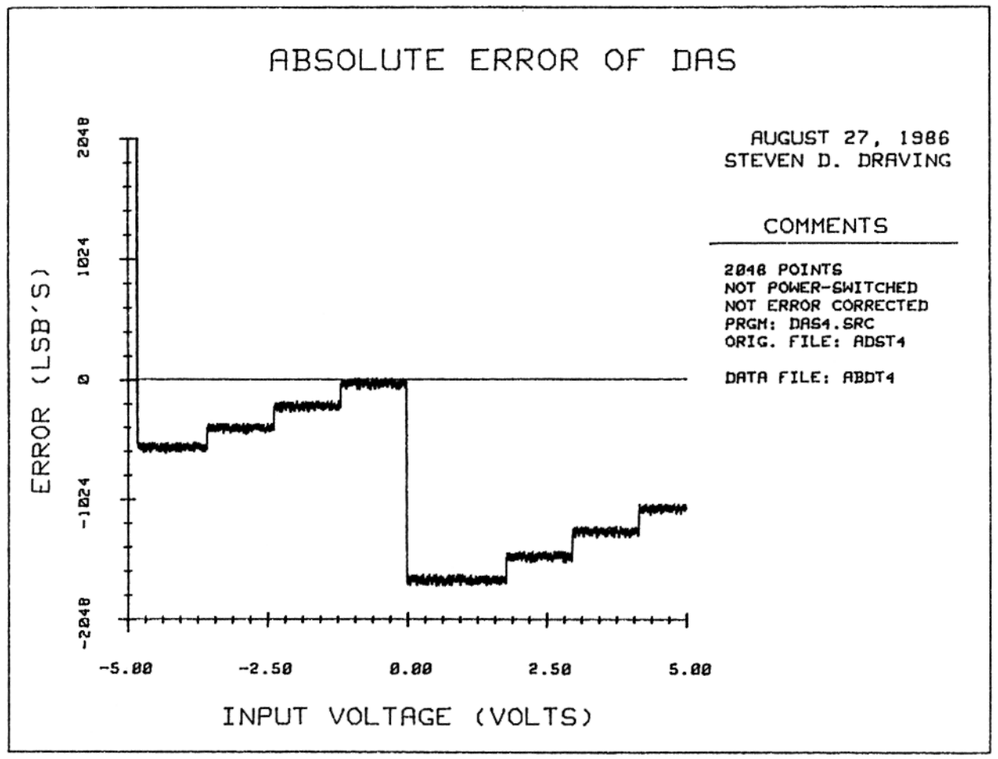


Figure 20 Plot of Absolute Error of SCSH DAS

Analysis and Discussion

A prototype SCSH DAS was constructed and preliminary tests suggest that it can meet the desired design specifications providing several modifications are performed. The output's absolute error caused be comparator oscillation and system noise are probably a result of the prototypes's wire-wrapped construction and therefore will not be discussed further. However, two design modifications which may reduce power consumption are discussed.

The first modification is very simple and could reduce the SCSH DAS's total power consumption by as much as 23%. If the host system provided a 4 MHz clock signal to the MC68HC11A8, the MC68HC11A8 could enter stop mode instead of wait mode during inactive periods of each conversion cycle. Stop mode can not be used with internal clock generation because stop mode would disable the clock and re-starting the clock requires a very long settling time.

The other suggested design modification is to remove the multiplexer, U16, and convert the first three MSBs of the conversion using the MC68HC11A8. The SARs could then be clocked twice as fast to resolve the remaining bits of the conversion. Converting these bits faster would reduce power consumption by reducing the power switching duty cycle.

Conclusion

The MC68HC11A8 Single-Chip Microcomputer's extensive memory, sophisticated interfaces, elaborate interrupt system, and 8-bit ADC make it an ideal controller for low-power precision ADCs. Though not necessary, the addition of a programmable clock circuit would improve the MC68HC11A8's control ability. The MC68HC11A8's size and power consumption advantages over existing microprocessor systems was demonstrated in the MC68HC11A8's successful control of the RDB DAS. Four A/D conversion schemes were presented which utilized different abilities of the MC68HC11A8. One of these schemes was then built and tested to demonstrate the ease with which the MC68HC11A8 can be implemented in ADC controller applications. From the evidence collected during its evaluation, the MC68HC11A8 appears to be an ideal controller not only for low-power ADCs, but for many other control applications as well.

As an extension of this evaluation, Jeff Daniels will perform extensive dynamic tests on the MC68HC11A8's on-chip ADC as part of his graduate research at Kansas State University. Also, the SCSH DAS design will continue to be refined through Jim Heise's graduate research at Kansas State University.

Appendix A: MC68HC11A8 Evaluation System

All tests and applications discussed in this evaluation of the MC68HC11A8 Single-Chip Microcomputer were performed using the customized MC68HC11A8 Evaluation System (EVS). The EVS is a small wire-wrapped microcomputer evaluation circuit which supports the MC68HC11A8 in various configurations and operating modes. In single-chip mode, the EVS provides the MC68HC11A8 chip with a quartz crystal for internal clock generation and a ±12 Vdc line driver with DB-25 connector for the SCI interface connection to a data terminal or host system. In expanded-memory mode, two additional serial communication interfaces, 2K bytes external RAM and 8K bytes external EPROM are also provided. The two general purpose parallel I/O ports, B and C, are still available in expanded-memory mode through the use of an MC68HC24 Port Replacement Unit. In both operating modes, the EVS provides convenient power supply and I/O connections to the MC68HC11A8 package.

Circuit Description

A circuit diagram of the MC68HC11A8 Evaluation System shown in Figure A.1 is a modified version of an evaluation circuit suggested in Motorola's early BUFFALO monitor documentation. An 8-pin dip-type switch is used in this

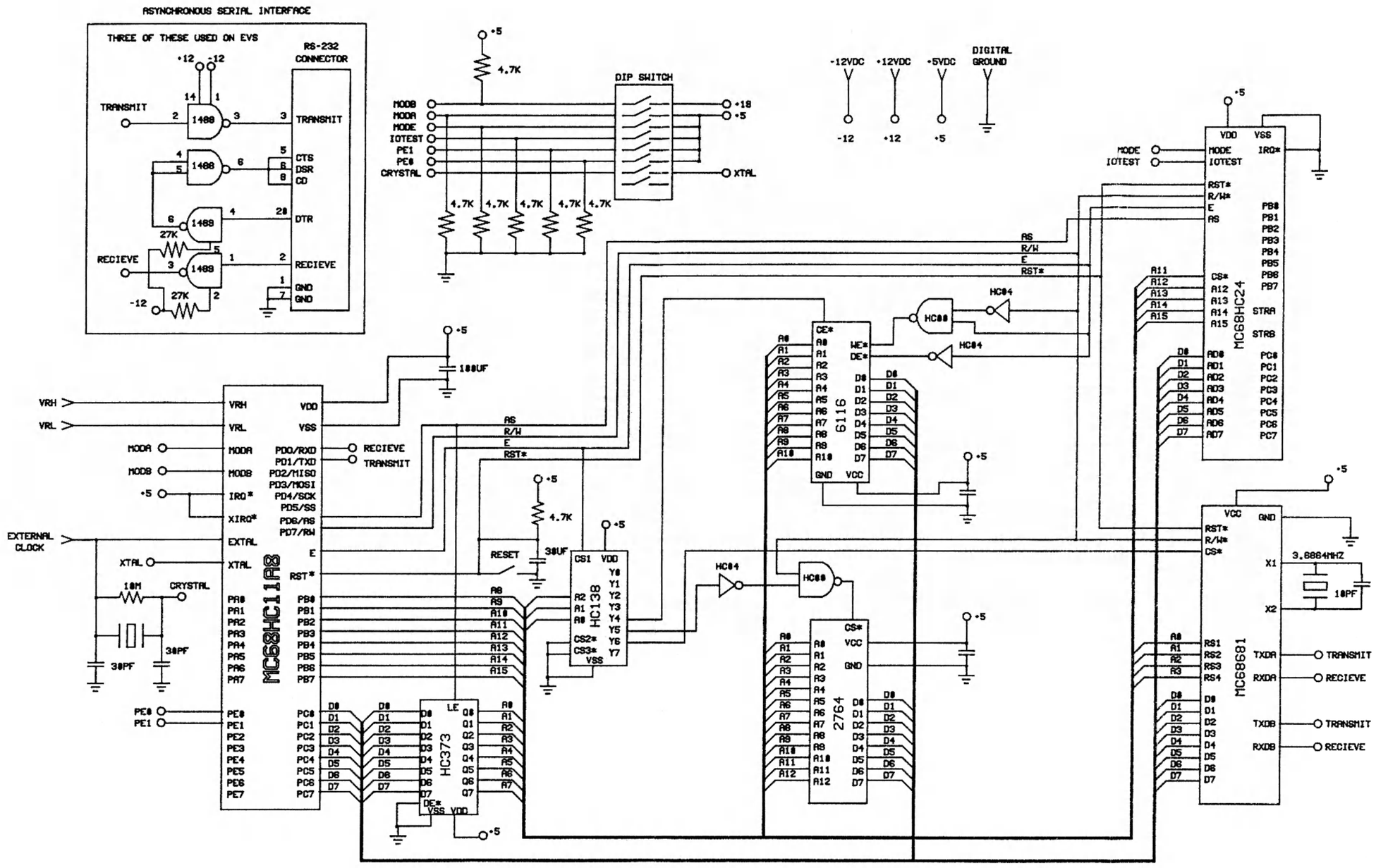


Figure A.1 Circuit Diagram of MC68HC11A8 Evaluation System
(Courtesy of Motorola)

modified version to select between various MC68HC11A8 operating modes and evaluation circuit configurations. Switch SW1 of the dip switch is used to apply a 19 Vdc EEPROM programming voltage to the MC68HC11A8's MODB pin. Switch SW2 selects between single-chip and expanded-memory modes of the MC68HC11A8. Switches SW3 and SW4 select the mode and I/O test configurations of the MC68HC24 Port Replacement Unit. Switches SW5 and SW6 are connected directly to the MC68HC11A8's PE0 and PE1 pins to select whether or not BUFFALO is executed immediately out of reset. Finally, switch SW7 connects the MC68HC11A8's XTAL pin to the clock crystal for internal clock operation.

Figure A.2 shows the MC68HC11A8 EVS's memory map. Note that the internal EEPROM and part of the external EPROM are mapped to the same location in memory. This does not cause a problem because the EPROM data lines are protected from conflicting output data within the MC68HC11A8. The EPROM can only be accessed at the conflicting address when the EEPROM is disabled.

BUFFALO Monitor

All prototype MC68HC11A8 chips tested by Kansas State University were received with the BUFFALO monitor program stored in their 8K byte on-chip ROM memory. The BUFFALO (Bit Users Fast Friendly Aid to Logical Operation) monitor is a microprocessor programming aid which performs

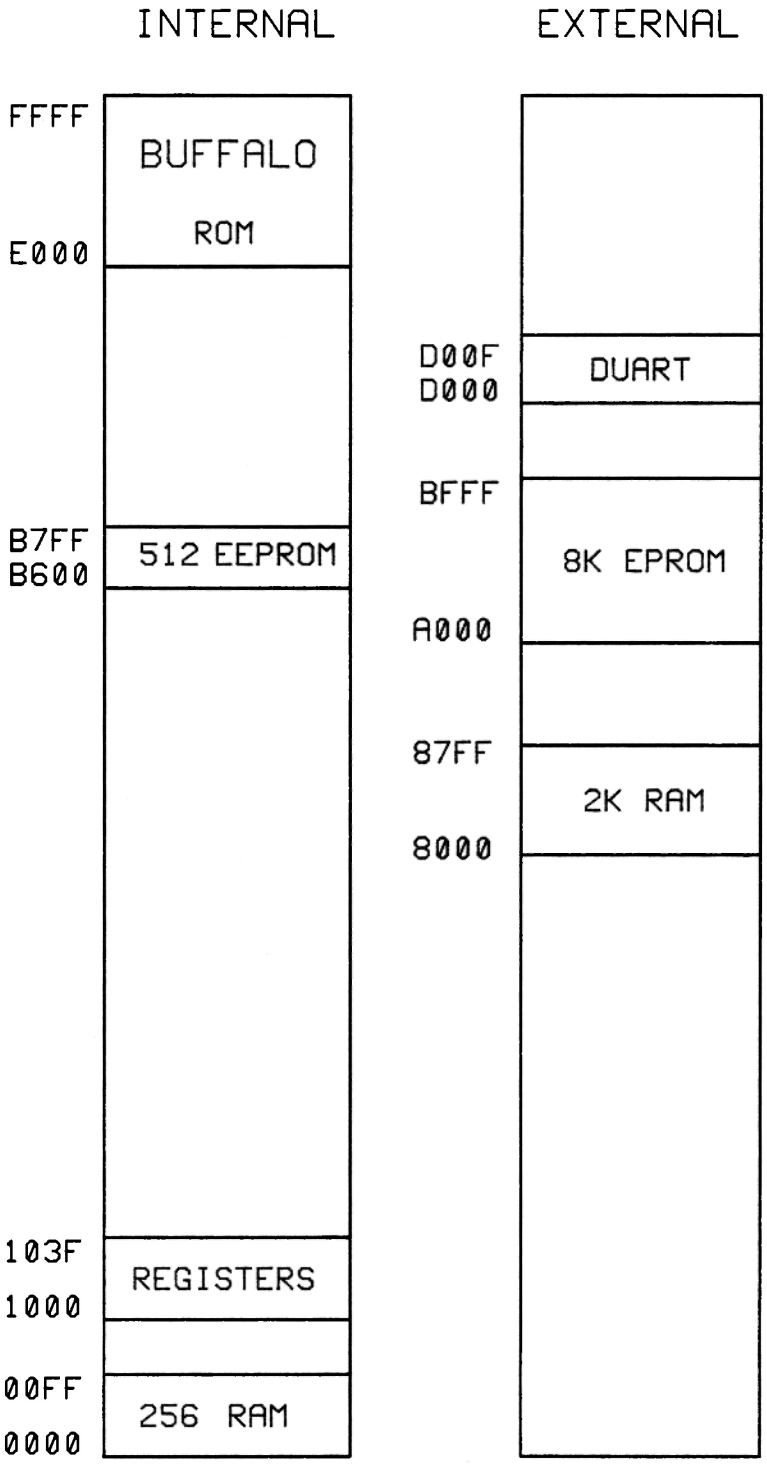


Figure A.2 Memory Map of MC68HC11A8 Evaluation System

single-line assembly and disassembly, memory and register editing, program up-loading and down-loading, and break-point editing. In addition to these functions, the BUFFALO monitor has several useful I/O routines which are made available to the user as utility subroutines.

MC68HC11A8 EVS Workstation

All user interaction with the MC68HC11A8 is conducted with VTERM, or similar terminal emulator program, on an IBM PC-XT microcomputer. Under VTERM's control, the IBM PC-XT functions as a simple data terminal and can communicate with the EVS over two of its three asynchronous serial I/O ports. With dip switches SW5 and SW6 set to logic one and zero, respectively, the EVS powers-up running the BUFFALO monitor program located in its on-chip ROM. At the time this evaluation was conducted, no cross-assembler was available for the MC68HC11A8's extended instruction set. Therefore, all source programs were written as undocumented text files and then "auto-typed" to the BUFFALO monitor's single-line assembler. Assembled programs could then be up-loaded to or down-loaded from the IBM PC-XT using VTERM. Two utility programs, UPLOAD and DNLOAD, were written to aid data transfer of programs in Motorola EXORciser (S1/S9) format.

Evolution of the EVS

Kansas State University's evaluation of the MC68HC11A8 Single-Chip Microcomputer began during the summer of 1985 with the original 64-pin dip package prototypes. Original MC68HC11A8 prototypes were not completely functional. Byte and row erase, programming voltage, and programming speed of the on-chip EEPROM were all major problems for the original MC68HC11A8s. More recent prototypes have been received with improved programming speed and voltage but byte and row erase are still not functional.

In addition, early BUFFALO monitor versions were also incomplete. Automatic EEPROM programming and line disassembly were not operational in early BUFFALO monitors. Also, the jump vector look-up table for the BUFFALO's I/O utility subroutines was not implemented. Although newer versions of the monitor have since been received, none of these functions have been made operational.

Over the 15-month evaluation period, updated versions of both the MC68HC11A8 and MC68HC24 were received and substituted for older versions. Because not all versions came in the same type of IC package, special socket adapters were made so that either quad or dip type ICs could be used. Although these socket adapters worked correctly, they increased the noise level of the EVS considerably, possibly explaining the noise problems

experienced by the MC68HC11A8's ADC.

With each new MC68HC11A8 prototype came a different version of the BUFFALO monitor. The address locations of the I/O utility subroutines varied between the monitors preventing user written programs from being completely compatible with all MC68HC11A8 prototypes.

Other MC68HC11A8 evaluation systems are available from Motorola. Two printed circuit board systems, the Evaluation Board (EVB) and the Evaluation Module (EVM) perform basically the same functions as the EVS. The EVB is a small (4 1/2 in X 7 in) board which emulates the MC68HC11A8 in single-chip mode and supports program down-loading from a host computer. The EVM (8 1/2 in X 11 in) emulates both single-chip and expanded-memory operating modes. It also supports programming of the MC68HC11A8's EEPROM. Both boards provide an additional 8K RAM and 8K EPROM for user programs.

More recent BUFFALO monitor versions are also now available. However, their capabilities have not yet been determined. Also an MC68HC11A8 cross-assembler is now available which will run on an IBM-PC or compatible computer.

Utility Programs

Source listings of the following three utility programs are provided in the following pages.

* EEPROM - Erases MC68HC11A8's entire EEPROM before copying specified memory bytes from RAM to the EEPROM.

* UPLOAD - Generates S1/S9 file and transmits it over the current serial communication port.

* DNLOAD - Accepts incoming data streams over the current serial communication port in S1/S9 format and stores them in memory.

```
*************************************************************
**                          EEPROM                         **
*************************************************************
*
*       THIS PROGRAM ERASES THE MC68HC11A8'S ENTIRE
*   EEPROM BEFORE COPYING SPECIFIED MEMORY BYTES FROM RAM
*   TO THE EEPROM.  MEMORY BYTES CAN BE COPIED WITHOUT
*   FIRST ERASEING THE EEPROM BY CALLING THE PROGRAM
*   AT ADDRESS 8020 (HEX).
*
*         BEGINNING SOURCE ADDRESS:      0000 (HEX)
*         ENDING SOURCE ADDRESS:         0002
*         BEGINNING DESTINATION ADDRESS: 0004
*
*       ALL COMMENTS AND ADDRESS LABELS MUST BE REMOVED
*   FROM THIS LISTING BEFORE IT CAN BE AUTO-TYPED TO THE
*   BUFFALO MONITOR.
*
*   STEVEN D. DRAVING                                7/8/85
*
*************************************************************
*
*
*
     A 8000          BEGIN ASSEMBLY AT ADDRESS 8000
8000 LDAB #06        SELECT BLOCK ERASE
     STAB 103B
     INC 103B        TURN ON ERASE VOLTAGE
     LDY #8000       PAUSE FOR A WHILE
800C DEY
     BNE 800C
     DEC 103B        TURN OFF ERASE VOLTAGE
     CLR 103B        SELECT NORMAL READ MODE
     BRA 8020        BRANCH TO COPYING ROUTINE

     A 8020          CONTINUE ASSEMBLY AT ADDRESS 8020
     LDAB #02        SELECT PROGRAMMING MODE
     STAB 103B
     LDX 0000        LOAD STARTING SOURCE ADDRESS
     LDY 0004        LOAD STARTING DESTINATION ADDRESS
802A LDAA 0,X        TRANSFER ONE MEMORY BYTE
     STAA 0,Y
     INC 103B        TURN ON PROGRAMMING VOLTAGE
     LDD #8000
8035 SUBD #01
     BNE 8035
     DEC 103B        TURN OFF PROGRAMMING VOLTAGE
     INX             SELECT NEXT MEMORY BYTE
     INY
     CPX 0002        ARE THERE MORE BYTES?
     BLE 802A        IF SO, THEN REPEAT
```

```
CLR 103B        SELECT NORMAL READ MODE
RTS             RETURN FROM PROGRAM
```

```
*************************************************************
**                          UPLOAD                           **
*************************************************************
*
*       THIS PROGRAM GENERATES S1/S9 OBJECT FILES AND
*  THEN TRANSMITS THEM OVER THE CURRENT SERIAL
*  COMMUNICATION INTERFACE TO A HOST SYSTEM.
*
*         BEGINNING ADDRESS:      0001 (HEX)
*         ENDING ADDRESS:         0003
*
*       ALL COMMENTS AND ADDRESS LABELS MUST BE REMOVED
*  FROM THIS LISTING BEFORE IT CAN BE AUTO-TYPED TO THE
*  BUFFALO MONITOR.
*
*  STEVEN D. DRAVING                                7/15/85
*
*************************************************************
*
*
*
*
     A 8000          BEGIN ASSEMBLY AT ADDRESS 8000
8000 LDY 0001        PUSH FIRST ADDRESS ONTO STACK
     PSHY
     BRA 800F        SKIP THE NEXT COUPLE LINES
8007 LDAA #13        SET BYTCNT = 13 (HEX)
     STAA 0000       BYTCNT
     BSR 8050        SEND AN "S1"
     BSR 8060        SEND REMAINDER OF THE LINE
800F LDD 0003        IS THERE MORE DATA TO SEND?
     ADDD #01
     SUBD 0001
     CPD #10
     BGT 8007        IF SO, SEND IT
     ADDB #03        CALCULATE BYTCNT
     STAB 0000
     BSR 8050        SEND "S1"
     BSR 8060        SEND REMAINDER OF THE LINE
     LDAA #03        STORE BYTCNT
     STAA 0000
     PULY            PULL FIRST ADDRESS FROM STACK
     STY 1
     LDAA #53        SEND "S9"
     JSR E2D3
     LDAA #39
     JSR E2D3
     BSR 8060        SEND REMAINDER OF LINE
     JSR E3D9        WAIT UNTIL ANOTHER KEY IS PRESSED
     RTS             RETURN FROM PROGRAM
```

```
     A 8050          CONTINUE ASSEMBLY AT ADDRESS 8050
8050 LDAA #53        SEND "S"
     JSR E2D3
     LDAA #31        SEND "1"
     JSR E2D3
     RTS             RETURN FROM SUBROUTINE

     A 8060          CONTINUE ASSEMBLY AT ADDRESS 8060
8060 LDX #0000
     JSR E394        SEND BYTCNT
     JSR E394        SEND CURRENT ADDRESS
     JSR E394
     LDAB 0000       CALCULATE CHKSUM
     ADDB 0001
     ADDB 0002
     LDAA #03        DOES BYTCNT = CHKSUM
8074 CMPA 0000
     BEQ 808A        IF SO, SKIP THE NEXT FEW LINES
     LDX 0001        SEND NEXT DATA BYTE
     ADDB 00,X
     JSR E394
     LDY 0001        INCREMENT CURRENT ADDRESS COUNTER
     INY
     STY 0001
     INCA
     BRA 8074        REPEAT THE ABOVE
     COMB            SEND CHKSUM
     STAB 0005
     LDX #05
     JSR E394
     JSR E3AC        SEND CARRAGE RETURN AND LINE FEED
     RTS             RETURN FROM SUBROUTINE
```

```
*************************************************************
**                          DNLOAD                         **
*************************************************************
*
*       THIS PROGRAM ACCEPTS INCOMING DATA FILES FROM
*  THE CURRENT SERIAL COMMUNICATION INTERFACE IN S1/S9
*  FORMAT AND STORES THEM IN MEMORY.  THIS PROGRAM WAS
*  MODELED FROM THE DOWN LOADING SUBROUTINE IN THE
*  BUFFALO MONITOR.
*       ALL COMMENTS AND ADDRESS LABELS MUST BE REMOVED
*  FROM THIS LISTING BEFORE IT CAN BE AUTO-TYPED TO THE
*  BUFFALO MONITOR.
*
*  STEVEN D. DRAVING                              7/31/85
*
*************************************************************
*
*
*
*
     A 8000          BEGIN ASSEMBLY AT ADDRESS 8000
8000 BSR 800E        CALL THE MAIN SUBROUTINE
     JSR E2B9        HAVE EITHER Ctrl-D OR Ctrl-G BEEN
     CMPA #04             PRESSED YET?
     BEQ 800D
     CMPA #07
     BNE 8002
800D RTS             IF SO, THEN RETURN FROM PROGRAM
800E CLR 00C1        CLEAR FLAGT1 OF BUFFALO
8011 JSR E2B9        READ TERMINAL
     TSTA
     BEQ 8011        BRANCH IF NO INPUT
     CMPA #53
     BNE 8011        BRANCH IF NOT AN "S"
801B JSR E2B9        READ TERMINAL AGAIN
     TSTA
     BEQ 80IB        BRANCH IF NO INPUT
     CMPA #39
     BNE 8036        BRANCH IF NOT A "9"
     BSR 8083
     LDAB 0099       SET BYTCNT
     BSR 8083
     DECB
     BNE 802A        REPEAT UNTIL END OF RECORD
     LDX #E4D5
     JSR E3B9        DISPLAY "done" MESSAGE
     RTS             RETURN FROM MAIN SUBROUTINE
8036 CMPA #31
     BNE 8011        BRANCH IF NOT "1"
     CLR 00C3        CLEAR CHKSUM
     BSR 8083
```

```
     LDAB 0099
     SUBB #02        SET BYTCNT
     BSR 8083
     BSR 8083
     LDX 0098        X = BASE ADDRESS
     DEX
804C BSR 8083        GET NEXT BYTE
     INX
     DECB            DOES BYTCNT = 0 ?
     BEQ 8073        IF SO, THEN CALCULATE CHKSUM
     LDAA 0099
     TST 00C1
     BNE 805C        BRANCH IF CHKSUM IS VERIFIED
     STAA 0,X
805C CMPA 0,X
     BEQ 804C        JUMP IF RAM IS OK
     STX 00BF        SAVE ERROR ADDRESS
     JSR E3AC
     LDX #E4E9       DISPLAY "ERROR ADDRESS" MESSAGE
     JSR E3B9
     LDX #00BF       DISPLAY BAD ADDRESS
     JSR E3A0
     RTS             RETURN FROM SUBROUTINE
8073 LDAA 00C3       IS CHKSUM OK?
     INCA
     BEQ 8011        BRANCH IF CHKSUM IS OK
     JSR E3AC
     LDX #E4DA       DISPLAY "CHECKSUM ERROR"
     JSR E3B9
     RTS             RETURN FROM SUBROUTINE
8083 PSHB
     PSHX
8085 JSR E2B9        READ TERMINAL
     TSTA
     BEQ 8085        WAIT FOR INPUT
     JSR E191
808E JSR E2B9        READ TERMINAL
     TSTA
     BEQ 808E        WAIT FOR INPUT
     JSR E191        CALL HEXBIN SUBROUTINE FROM BUFFALO
     LDAA 0099
     ADDA 00C3
     STAA 00C3       ADD TO CHKSUM
     PULX
     PULB
     RTS             RETURN FROM SUBROUTINE
```

Appendix B

Circuit Diagrams, Parts Lists, and A Timing Diagram for the Original RDB DAS

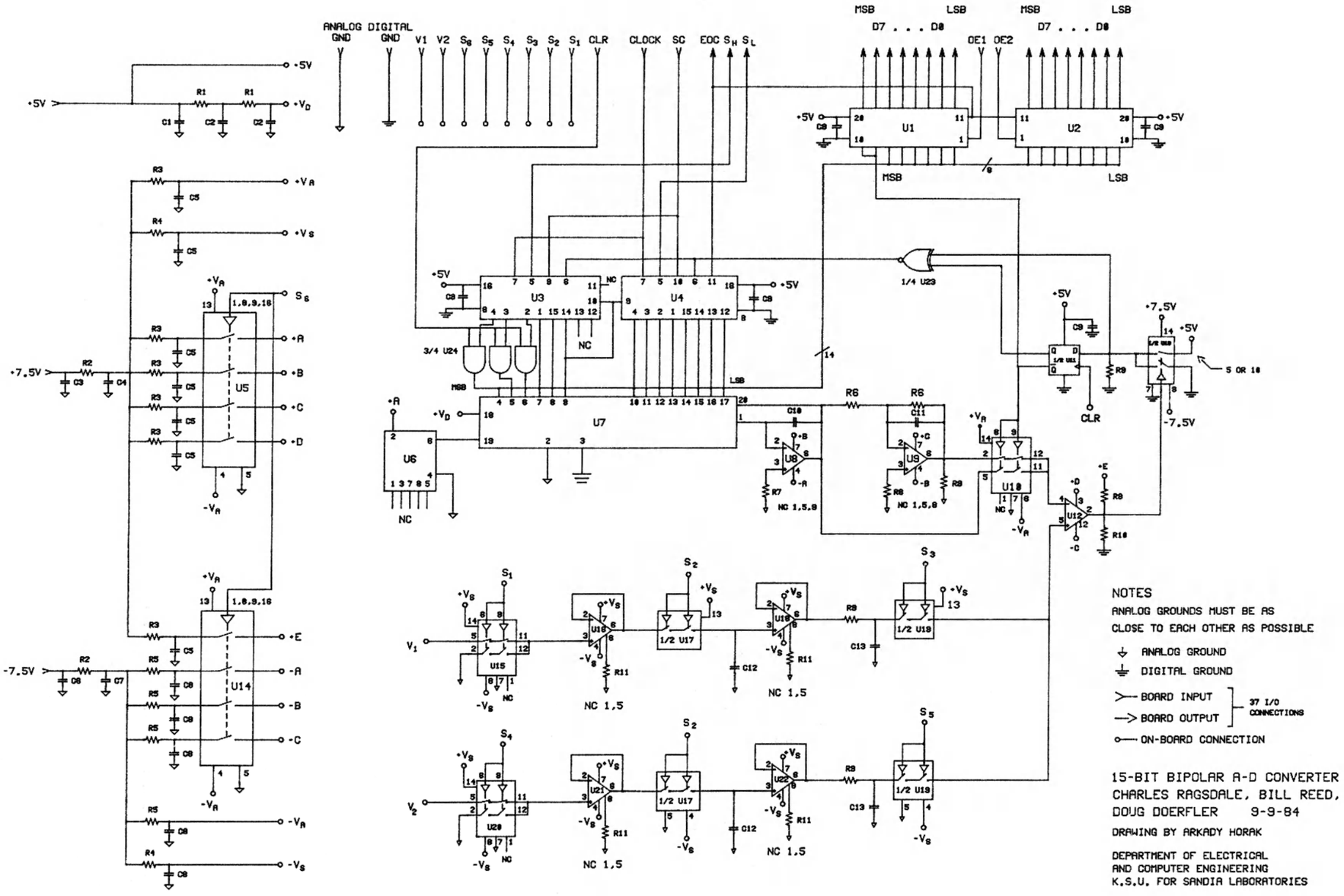


Figure B.1 Circuit Diagram of Original RDB DAS Analog Section

Parts List for the Analog Section of the Original RDB DAS

ICs

DEVICE	FUNCTION	PART#	MANUFACT.	#PINS
U1	Octal D Flip-Flop	MM74C374	Nat. Semi.	20
U2	Octal D Flip-Flop	MM74C374	Nat. Semi.	20
U3	Succ. Approx. Reg.	MC14559B	Motorola	16
U4	Succ. Approx. Reg.	MC14549B	Motorola	16
U5	SPST Analog Switch	DG308CJ	Siliconix	16
U6	+5V Voltage Ref.	REF-02EZ	PMI	8
U7	14-bit DAC	DAC-HA14B	Datel-Intersil	20
U8	Low-noise Op-Amp	OP-37EZ	PMI	8
U9	Low-noise Op-Amp	OP-37EZ	PMI	8
U10	SPDT Analog Switch	DG307BP	Siliconix	14
U11	Dual D Flip-Flop	MM74C74	Nat. Semi.	14
U12	Quad Comparator	CMP-04FP	PMI	14
U13	SPDT Analog Switch	DG307BP	Siliconix	14
U14	SPST Analog Switch	DG308CJ	Siliconix	16
U16	Micropower Op-Amp	OP-22EZ	PMI	8
U17	SPST Analog Switch	DG309CJ	Siliconix	16
U18	Micropower Op-Amp	OP-22EZ	PMI	8
U19	SPST Analog Switch	DG308CJ	Siliconix	16
U20	SPDT Analog Switch	DG307BP	Siliconix	14
U21	Micropower Op-Amp	OP-22EZ	PMI	8
U22	Micropower Op-Amp	OP-22EZ	PMI	8
U23	Quad 2 I/P EX-NOR	MM74HC266	Nat. Semi.	14
U24	Quad 2 I/P AND	MM74C08	Nat. Semi.	14

Resistors

DEVICE	FUNCTION	PART#	MANUFACT.	#USED	
R1	10 ohm discrete res.	*		2	
R2	1 ohm discrete res.	*		2	
R3	22 ohm resistor net.	108A	Allen-Bradley	2	$
R4	100 ohm discrete res.	*		2	
R5	22 ohm discrete res.	106A	Allen-Bradley	2	$
R6	10 kohm resistor net. matched to 0.005%	300190	Vishay	1	
R7	10 kohm 1% discr. res.	*		1	
R8	5 kohm 1% discr. res.	*		1	
R9	10 kohm resistor net.	108B	Allen-Bradley	2	#
R10	1 Mohm discrete res.	*		1	
R11	2 Mohm discrete res.	*		4	
R13	10 kohm discrete res.	*		1	

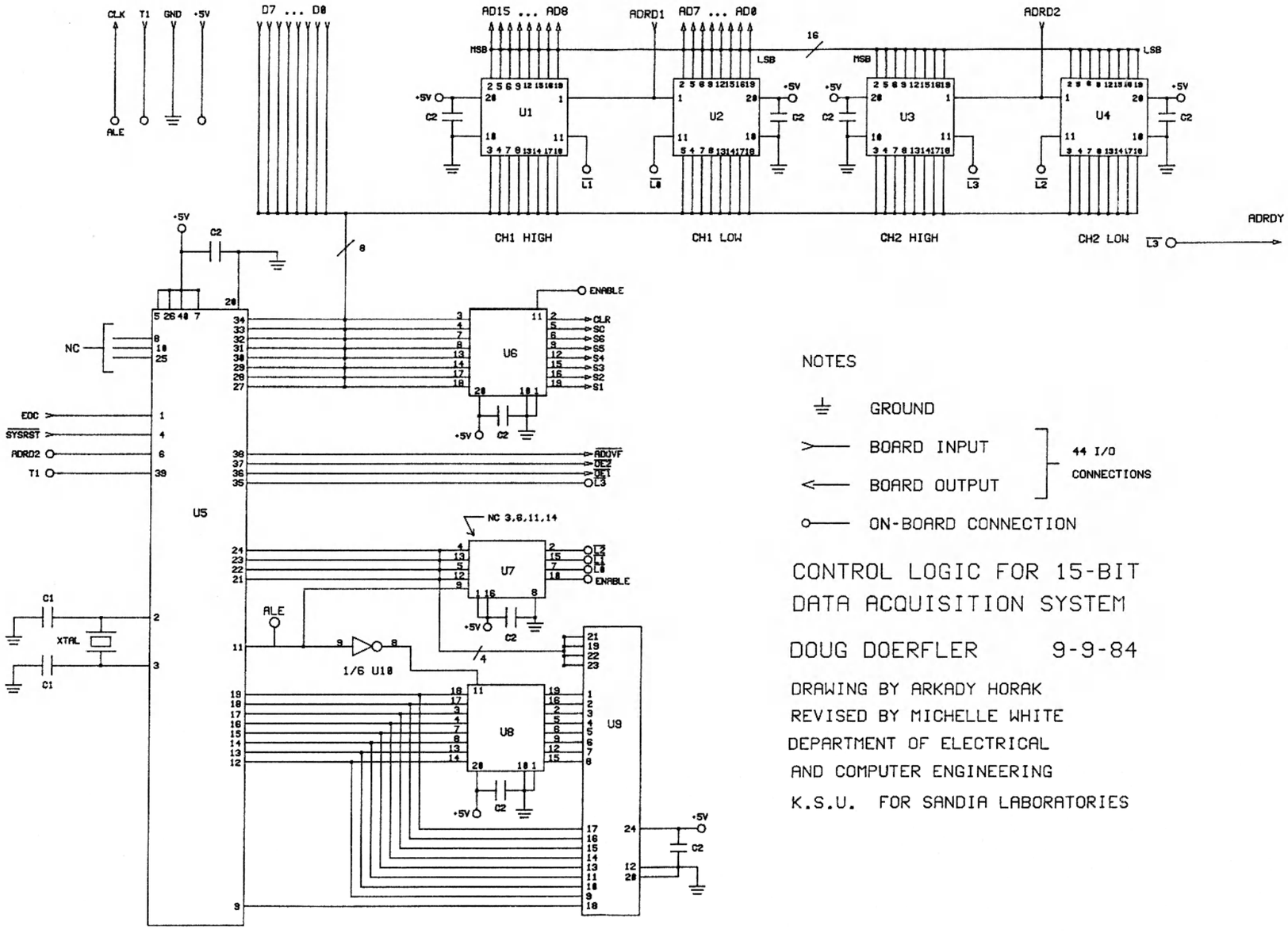
* use Allen-Bradley 1/4 watt, 5% or equivalent
$ R3 and R5 are packaged in 8 pin and 6 pin SIPs respectively, two SIPs are placed in parallel to achieve an 11 ohm value.
\# R9 is packaged in an 8 pin SIP

Capacitors

DEVICE	FUNCTION	#USED
C1	0.1 uF Ceramic	1
C2	10 uF Tantalum	2
C3	0.1 uF Ceramic	1
C4	10 uF Tantalum	1
C5	10 uF Tantalum	7
C6	0.1 uF Ceramic	1
C7	10 uF Tantalum	1
C8	10 uF Tantalum	5
C9	0.01 uF Ceramic	6
C10	59 pF Ceramic	1
C11	10 pF Ceramic	1
C12	0.01 uF Teflon	2
C13	0.001 uF Ceramic	2

All Ceramic capacitors are Panasonic disc ceramic caps or equivalent.

All Tantalum capacitors are Panasonic SQ resin dipped solid tantalum caps or equivalent.



NOTES

GROUND

BOARD INPUT

BOARD OUTPUT

44 I/O CONNECTIONS

ON-BOARD CONNECTION

CONTROL LOGIC FOR 15-BIT DATA ACQUISITION SYSTEM

DOUG DOERFLER 9-9-84

DRAWING BY ARKADY HORAK
REVISED BY MICHELLE WHITE
DEPARTMENT OF ELECTRICAL
AND COMPUTER ENGINEERING
K.S.U. FOR SANDIA LABORATORIES

Figure B.2 Circuit Diagram of Original RDB DAS Digital Section

Parts List for the Digital Section of the Original RDB DAS

ICs

DEVICE	FUNCTION	PART#	MANUFACT.	#PINS
U1	Octal D-type Latch	MM74C373	Nat. Semi.	20
U2	Octal D-type Latch	MM74C373	Nat. Semi.	20
U3	Octal D-type Latch	MM74C373	Nat. Semi.	20
U4	Octal D-type Latch	MM74C373	Nat. Semi.	20
U5	8-bit Microcomputer	80C39-7	Intel	40
U6	Octal D-type Latch	MM74C373	Nat. Semi.	20
U7	Quad D Flip-Flop	MM74C175	Nat. Semi.	16
U8	Octal D Flip-Flop	MM74C374	Nat. Semi.	20
U9	32k UV CMOS EPROM	MMC27C32	Nat. Semi.	24
U10	Hex Inverter	MM74C04	Nat. Semi.	14

Capacitors

DEVICE	FUNCTION	# USED	
C1	20 pF Ceramic	10	Panasonic disc ceramic caps or equivalent.
C2	0.01 uF Ceramic	2	

Crystal

DEVICE	FUNCTION	
XTAL	1.0 MHz crystal	series resonant, AT cut, HC33 package

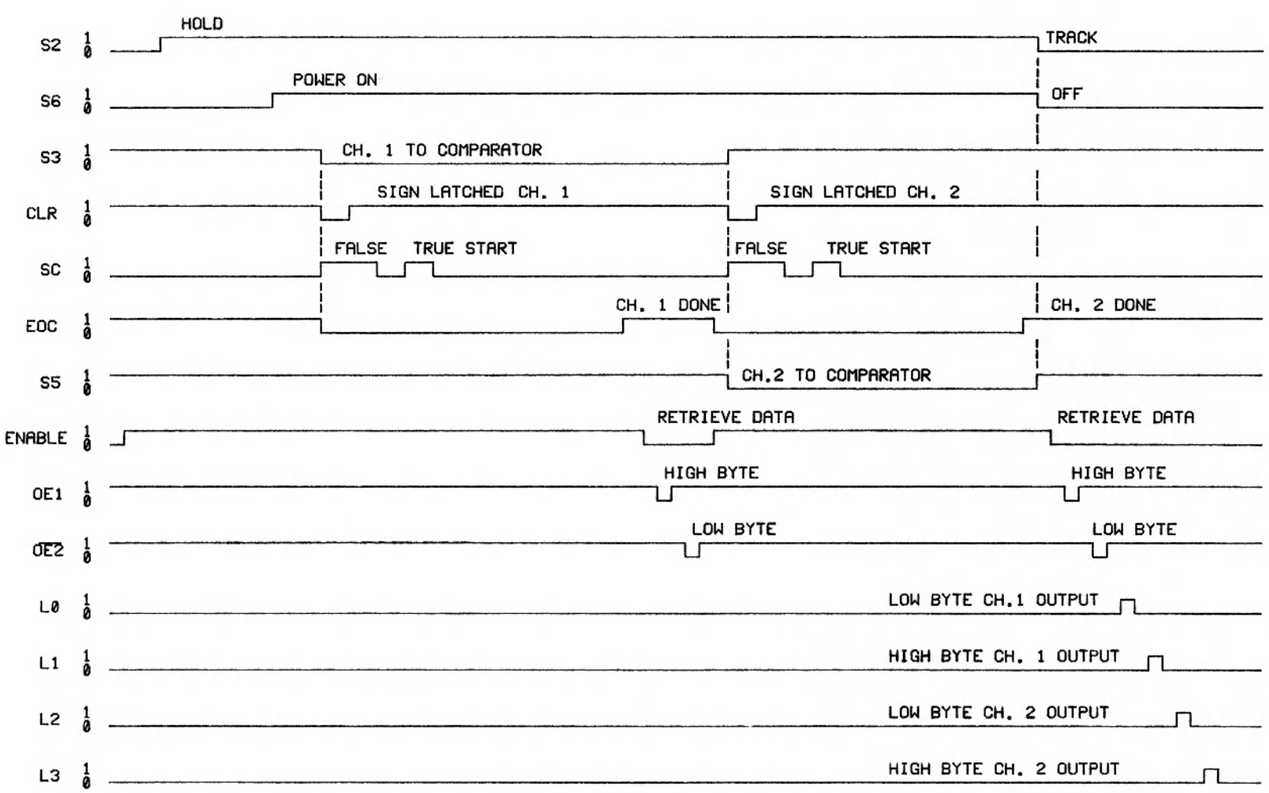


Figure B.3 Timing Diagram of A Single, Two-Channel Original RDB DAS A/D Conversion

Appendix C

Circuit Diagrams, Parts Lists, A Timing Diagram and A Program Listing for the MC68HC11A8 Controlled RDB DAS

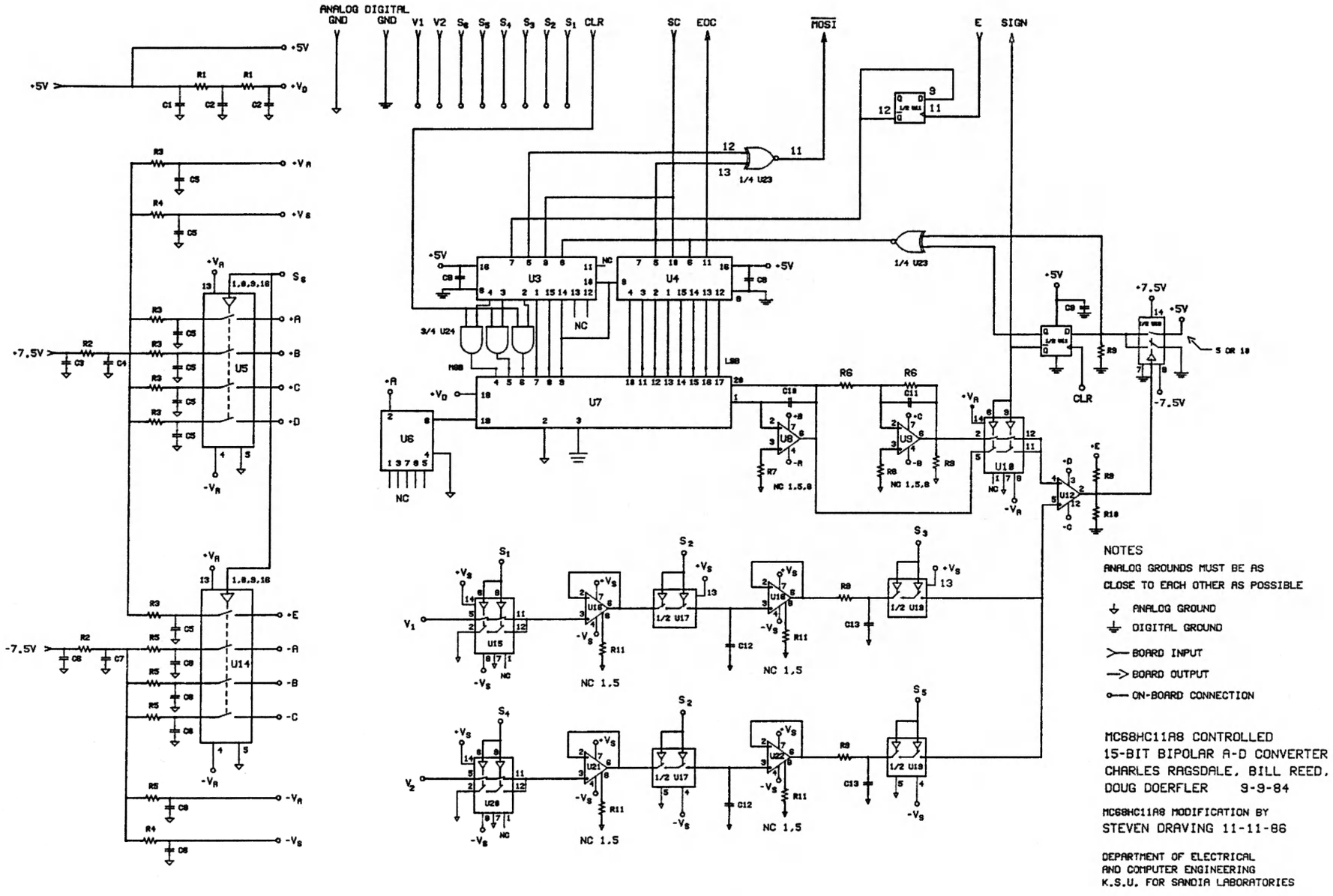


Figure C.1 Circuit Diagram of MC68HC11A8 Controlled RDB DAS Analog Section

Parts List for the Analog Section
of the MC68HC11A8 Controlled RDB DAS

ICs

DEVICE	FUNCTION	PART#	MANUFACT.	#PINS
U3	Succ. Approx. Reg.	MC14559B	Motorola	16
U4	Succ. Approx. Reg.	MC14549B	Motorola	16
U5	SPST Analog Switch	DG308CJ	Siliconix	16
U6	+5V Voltage Ref.	REF-02EZ	PMI	8
U7	14-bit DAC	DAC-HA14B	Datel-Intersil	20
U8	Low-noise Op-Amp	OP-37EZ	PMI	8
U9	Low-noise Op-Amp	OP-37EZ	PMI	8
U10	SPDT Analog Switch	DG307BP	Siliconix	14
U11	Dual D Flip-Flop	MM74C74	Nat. Semi.	14
U12	Quad Comparator	CMP-04FP	PMI	14
U13	SPDT Analog Switch	DG307BP	Siliconix	14
U14	SPST Analog Switch	DG308CJ	Siliconix	16
U16	Micropower Op-Amp	OP-22EZ	PMI	8
U17	SPST Analog Switch	DG309CJ	Siliconix	16
U18	Micropower Op-Amp	OP-22EZ	PMI	8
U19	SPST Analog Switch	DG308CJ	Siliconix	16
U20	SPDT Analog Switch	DG307BP	Siliconix	14
U21	Micropower Op-Amp	OP-22EZ	PMI	8
U22	Micropower Op-Amp	OP-22EZ	PMI	8
U23	Quad 2 I/P EX-NOR	MM74HC266	Nat. Semi.	14
U24	Quad 2 I/P AND	MM74C08	Nat. Semi.	14

Resistors

DEVICE	FUNCTION	PART#	MANUFACT.	#USED	
R1	10 ohm discrete res.	*		2	
R2	1 ohm discrete res.	*		2	
R3	22 ohm resistor net.	108A	Allen-Bradley	2	$
R4	100 ohm discrete res.	*		2	
R5	22 ohm discrete res.	106A	Allen-Bradley	2	$
R6	10 kohm resistor net. matched to 0.005%	300190	Vishay	1	
R7	10 kohm 1% discr. res.	*		1	
R8	5 kohm 1% discr. res.	*		1	
R9	10 kohm resistor net.	108B	Allen-Bradley	2	#
R10	1 Mohm discrete res.	*		1	
R11	2 Mohm discrete res.	*		4	
R13	10 kohm discrete res.	*		1	

* use Allen-Bradley 1/4 watt, 5% or equivalent
$ R3 and R5 are packaged in 8 pin and 6 pin SIPs respectively, two SIPs are placed in parallel to achieve an 11 ohm value.
\# R9 is packaged in an 8 pin SIP

Capacitors

DEVICE	FUNCTION	#USED
C1	0.1 uF Ceramic	1
C2	10 uF Tantalum	2
C3	0.1 uF Ceramic	1
C4	10 uF Tantalum	1
C5	10 uF Tantalum	7
C6	0.1 uF Ceramic	1
C7	10 uF Tantalum	1
C8	10 uF Tantalum	5
C9	0.01 uF Ceramic	6
C10	59 pF Ceramic	1
C11	10 pF Ceramic	1
C12	0.01 uF Teflon	2
C13	0.001 uF Ceramic	2

All Ceramic capacitors are Panasonic disc ceramic caps or equivalent.

All Tantalum capacitors are Panasonic SQ resin dipped solid tantalum caps or equivalent.

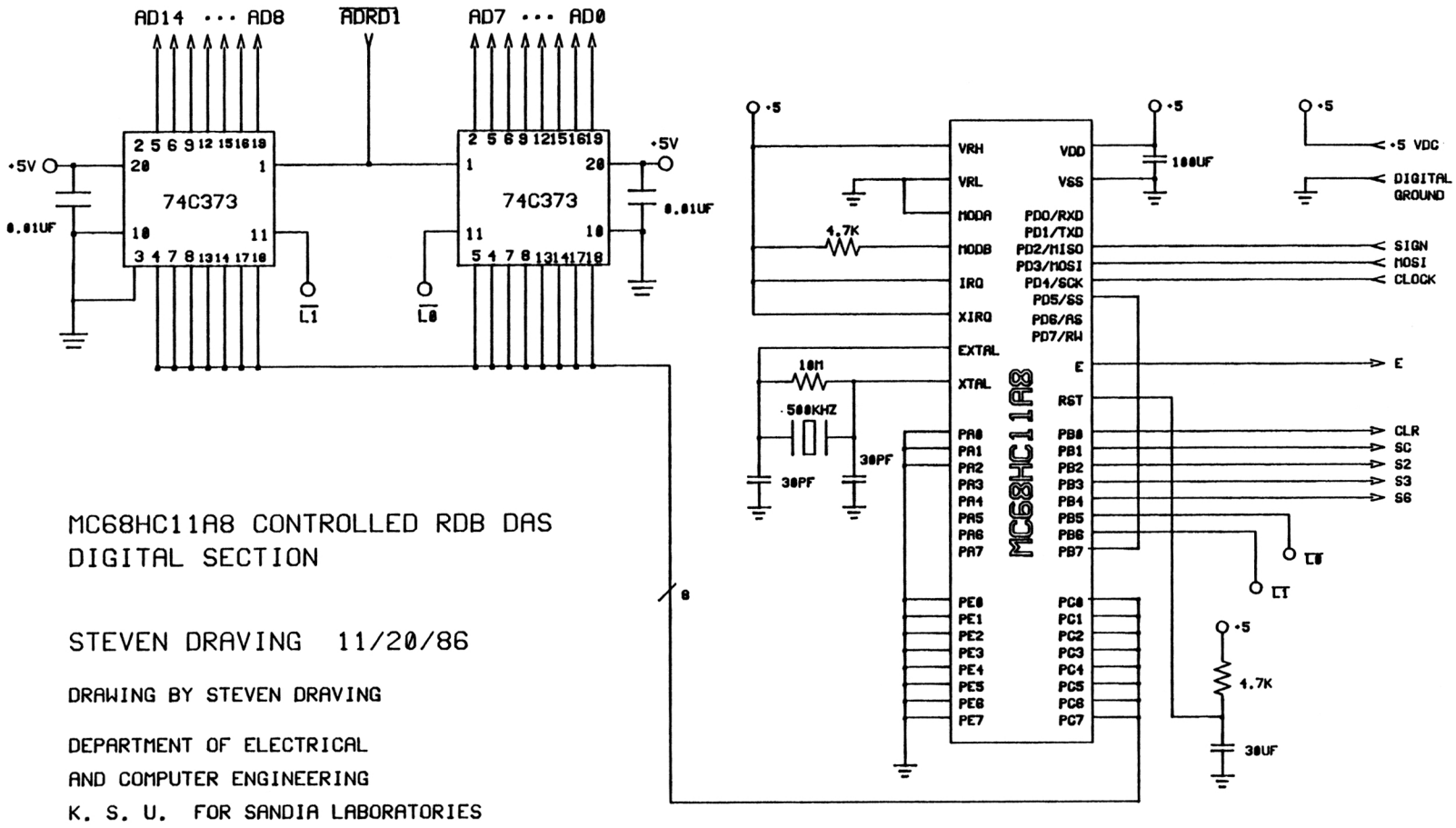


Figure C.2 Circuit Diagram of MC68HC11A8 Controlled RDB DAS Digital Section

Parts List for the Digital Section of the MC68HC11A8 Controlled RDB DAS

ICs

DEVICE	FUNCTION	PART#	MANUFACT.	#PINS
U1	Octal D-type Latch	MM74C373	Nat. Semi.	20
U2	Octal D-type Latch	MM74C373	Nat. Semi.	20
U3	8-bit Microcomputer	MC68HC11A8	Motorola	52

Capacitors

DEVICE	FUNCTION	#USED	
C1	30 pF Ceramic	2	Panasonic disc
C2	0.01 uF Ceramic	2	ceramic or
C3	30 uF Ceramic	1	equivalent.
C4	100 uF Electrolytic	1	

Crystal

DEVICE	FUNCTION	
XTAL	4.0 MHz crystal	series resonant, AT cut, HC33 package

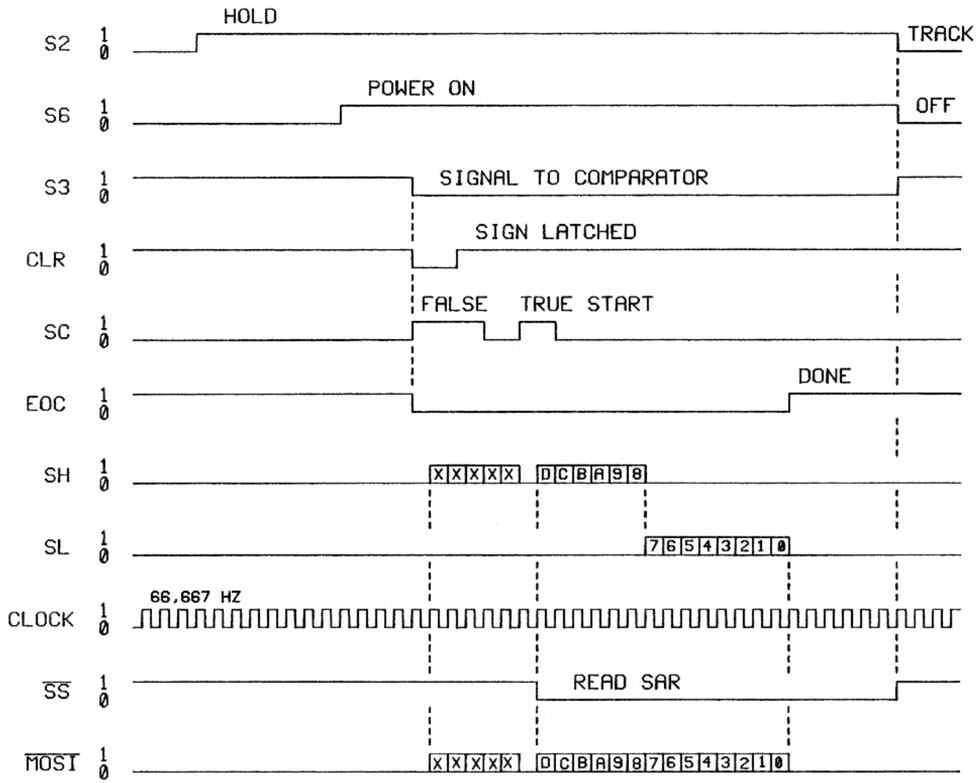


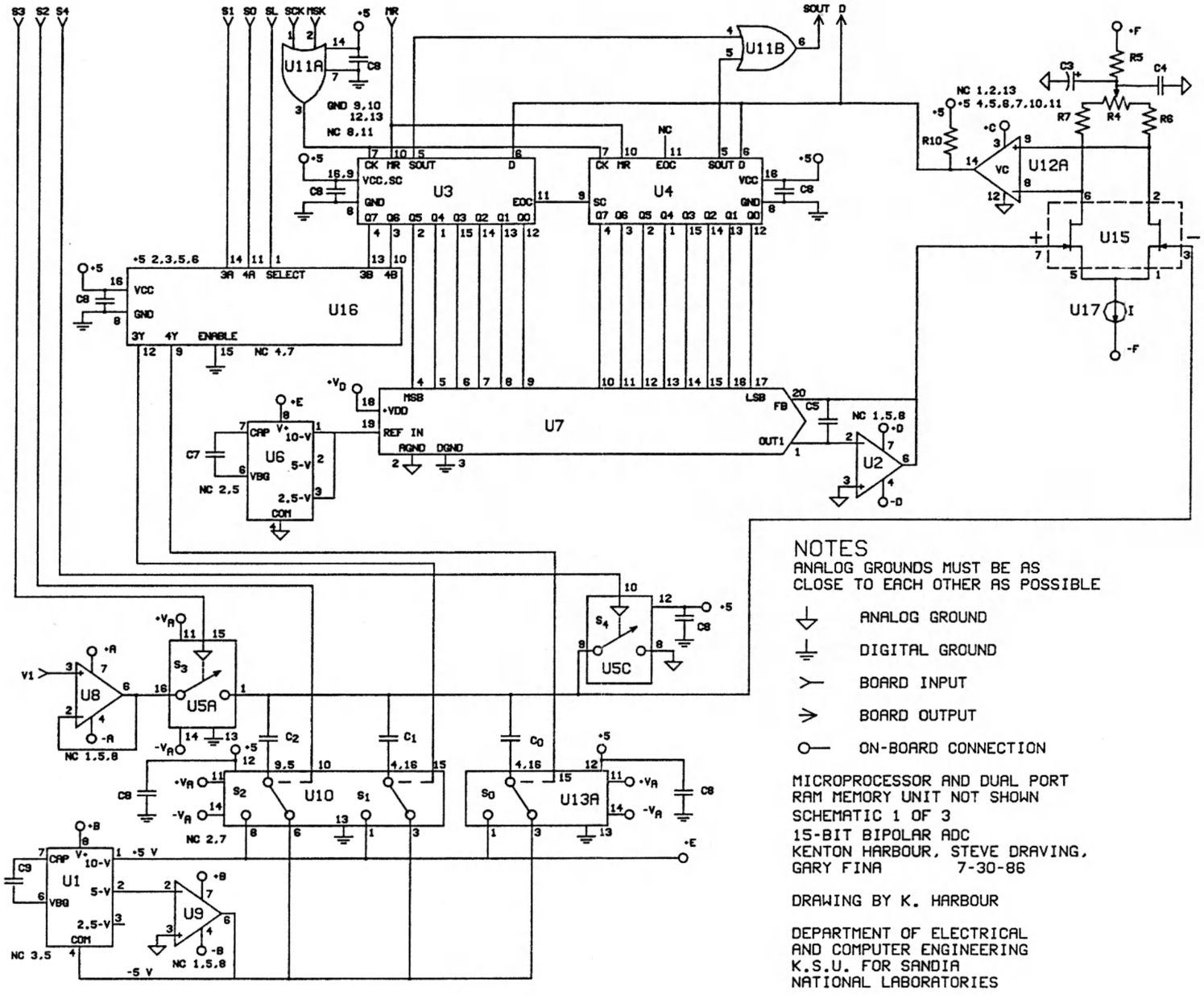
Figure C.3 Timing Diagram of A Single MC68HC11A8 Contolled RDB DAS A/D Conversion

```
*************************************************************
**                          ADCSE                          **
*************************************************************
*
*       THIS PROGRAM CONTROLS THE RDB DAS ANALOG SECTION
*  THROUGH SINGLE CONVERSIONS OF A SINGLE INPUT CHANNEL.
*  EACH CONVERSION IS INITIATED BY THE RECEPTION OF AN
*  ASCII 0D (HEX) OVER THE HC11'S SCI INTERFACE.  THE
*  RESULT OF EACH CONVERSION IS ALSO SENT BACK TO THE
*  HOST SYSTEM OVER THE SCI INTERFACE.
*
*  STEVEN D.DRAVING                                9/10/85
*
*************************************************************

         ORG $8000          LOCATE PROGRAM AT $8000

INIT     CLR $1009          DATA DIRECTION PORT D
         LDAA #$FF
         STAA $1000         INIT. PORT A
         STAA $1007         INIT. PORT C
         LDX #$1000
         LDAA #$4C
         STAA $1028         INIT. SPI CONTROL REG.
         LDAA #$E9
         STAA $1004         INIT. PORT B

START    LDAA $1029         CLEAR SPIF FLAG
         LDAA $102A
         BSET $04  $04,X    HOLD (S2=1)
         BSET $04  $10,X    POWER ON (S6=1)

         LDAA #$F6
         STAA $1004         FALSE CONV. (S3=0,CLR=0,SC=1)
         INC $1004          LATCH SIGN (CLR=1)
         LDAB #$F5
         STAB $1004         END FALSE CONVERSION (SC=0)
         ANDB #$7F

         LDAA #$77
         STAA $1004         TRUE CONVERSION (SC=1,SS=0)
         STAB $1004         (SC=0)
         LDAA $1000         PAUSE 16 E-CYCLES
         LDAA $1000
         LDAA $1000
         LDAA $1000
         LDAA $1029         CLEAR SPIF FLAG
         LDAA $102A
         STAA $1018         STORE HIGH BYTE
         LDAA $1000         PAUSE 4 E-CYCLES
         LDAA $1029         CLEAR SPIF FLAG
```

```
        LDAA $102A
        STAA $1019          STORE LOW BYTE
        BSET $04  $80,X     DISABLE SPI INTERFACE (SS=1)
        LDAA #$E9
        STAA $1004          END CONV. (S2=0,S6=0,S3=1)

        LDAA $1018          COMPLIMENT SAR OUPUT
        COMA
        ANDA #$3F           MASK FIRST 2 MSB
        STAA $1018
        COM $1019

        LDAA $1008          READ SIGN (PIN PD2)
        RORA
        RORA
        RORA
        BCC OUTPUT          TEST SIGN BIT

        COM $1019           PERFORM 2'S-COMPLIMENT
        COM $1018
        LDY $1018
        INY
        STY $1018

OUTPUT  LDX #$1018
        JSR $E3A0           DISPLAY HIGH BYTE OF RESULT
        JSR $E3AC           DISPLAY LOW BYTE OF RESULT
        LDX #$1000

READ    JSR $E2B9           WAIT FOR TERMINAL INPUT
        CMPA #$0D           TEST FOR CARRAGE RETURN
        BNE AGAIN
        JMP START           RUN ANOTHER CONVERSION
AGAIN   CMPA #$0A           TEST FOR LINE FEED
        BNE READ            REPEAT
        RTS
```

Appendix D

Circuit Diagrams, Parts Lists, A Timing Diagram and A Program Listing for the SCSH DAS



NOTES
ANALOG GROUNDS MUST BE AS
CLOSE TO EACH OTHER AS POSSIBLE

ANALOG GROUND

DIGITAL GROUND

BOARD INPUT

BOARD OUTPUT

ON-BOARD CONNECTION

MICROPROCESSOR AND DUAL PORT
RAM MEMORY UNIT NOT SHOWN
SCHEMATIC 1 OF 3
15-BIT BIPOLAR ADC
KENTON HARBOUR, STEVE DRAVING,
GARY FINA 7-30-86

DRAWING BY K. HARBOUR

DEPARTMENT OF ELECTRICAL
AND COMPUTER ENGINEERING
K.S.U. FOR SANDIA
NATIONAL LABORATORIES

Figure D.1 Circuit Diagram of SCSH DAS Analog Section

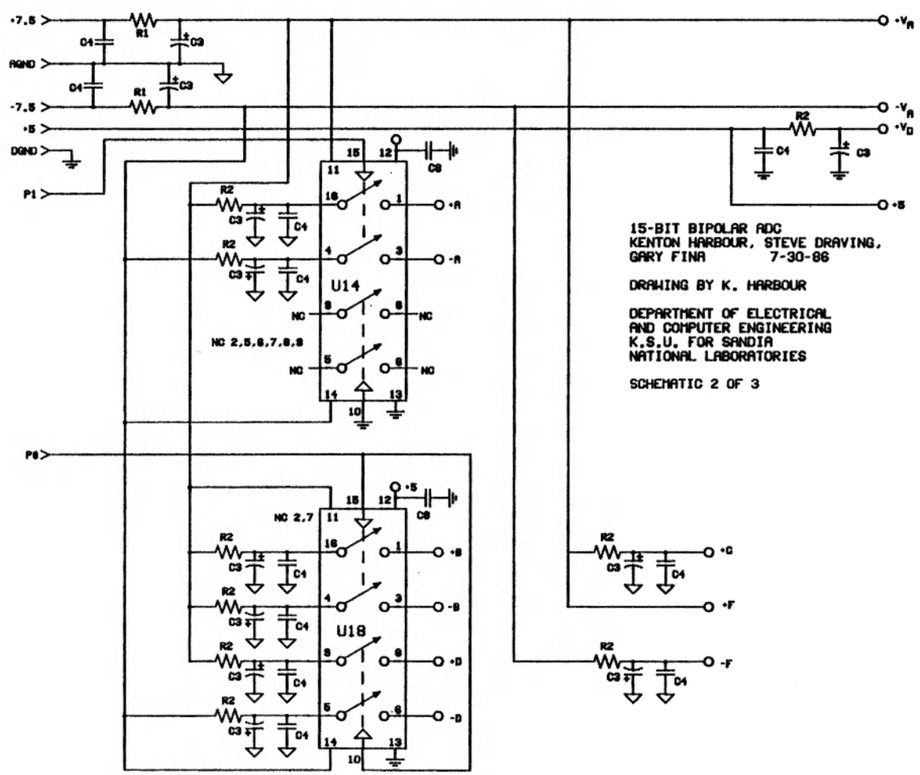


Figure D.2 Circuit Diagram of SCSH DAS Power Supply Filtering and Switching Section

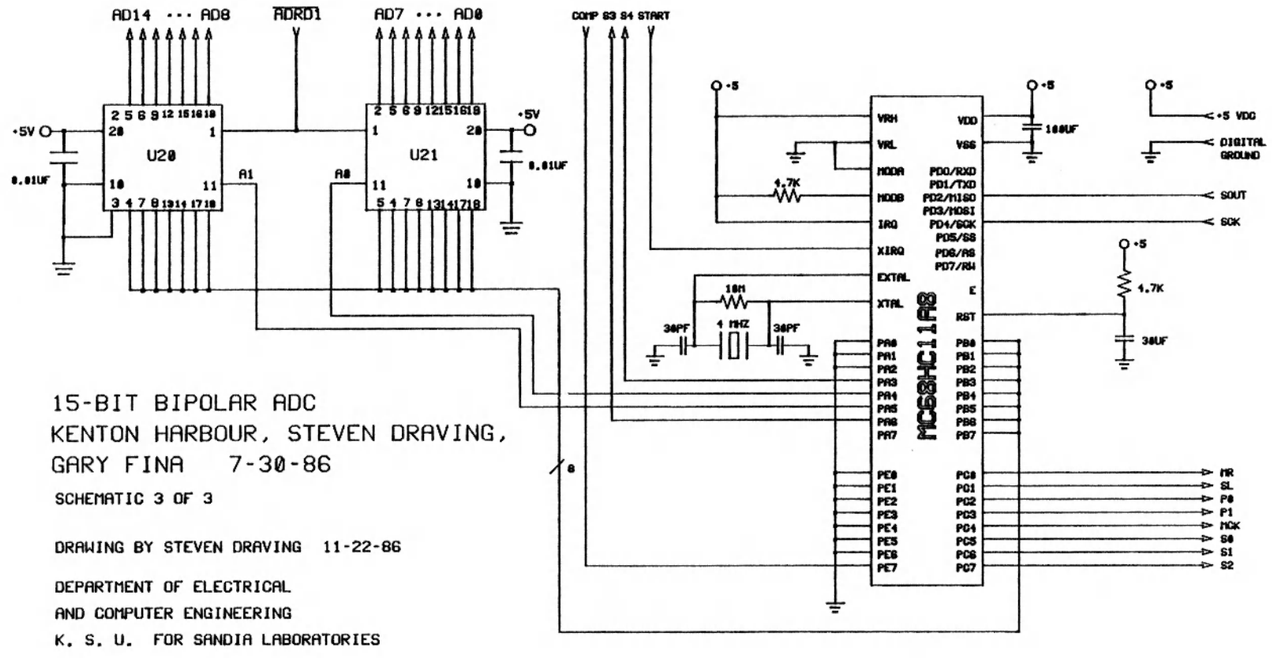


Figure D.3 Circuit Diagram of SCSH DAS Digital Section

Parts List for Entire SCSH DAS

Integrated Circuit Components

DEVICE	FUNCTION	PART#	MFG.	#PINS
U1	Voltage Reference	AD584	Analog Devices	8
U2	Low-Noise Op Amp	OP-37	PMI	8
U3	SAR	MC14549	Motorola	16
U4	SAR	MC14549	Motorola	16
U5	Dual DPST Switch	DG5145	Siliconix	16
U6	Voltage Reference	AD584	Analog Devices	8
U7	CMOS 14 Bit DAC	DAC-HA14B	Datel-Interstil	20
U8	Low-Noise Op Amp	OP-27	PMI	8
U9	BIFET Op Amp	AD547	Analog Devices	8
U10	Dual SPDT Switch	DG5143	Siliconix	16
U11	Quad 2-Input OR	MM74HC32	Nat. Semi.	14
U12	Quad Comparator	CMP-04	PMI	14
U13	Dual SPDT Switch	DG5143	Siliconix	16
U14	Dual DPST Switch	DG5145	Siliconix	16
U15	Monolithic Dual JEFT	U401	Siliconix	6
U16	Quad 2-Input Mux	MM74HCT157	Nat. Semi.	16
U17	Current Regulator Diode	CR022	Siliconix	2
U18	Dual DPST Switch	DG5145	Siliconix	16
U20	Octal Latch	MM74HC373	Motorola	20
U21	Octal Latch	MM74HC373	Motorola	20
U22	Microprocessor	MC68HC11A8	Motorola	48
			Total no. of pins	312

* Not shown on schematic

Resistors

DEVICE	VALUE (ohms)	DESCRIPTION	QTY.
R1	1	5% Carbon	2
R2	10	5% Carbon	9
R4	500	Multiturn Pot.	1
R5	20K	1% Metal Film	1
R6	10.2K	1% Metal Film	2
R10	100K	5% Carbon	1

Capacitors

DEVICE	VALUE (uF)	DESCRIPTION	QTY.
C0	0.0011	Teflon*	1
C1	0.0022	Teflon	1
C2	0.005	Teflon	1
C3	10	Tantalum	12
C4	0.01	Ceramic	12
C5	59 pF	Ceramic	1
C7	0.01	Ceramic	1
C8	0.01	Ceramic	9
C9	0.001	Ceramic	1

* obtained by placing two 0.0022 uF capacitors in parallel

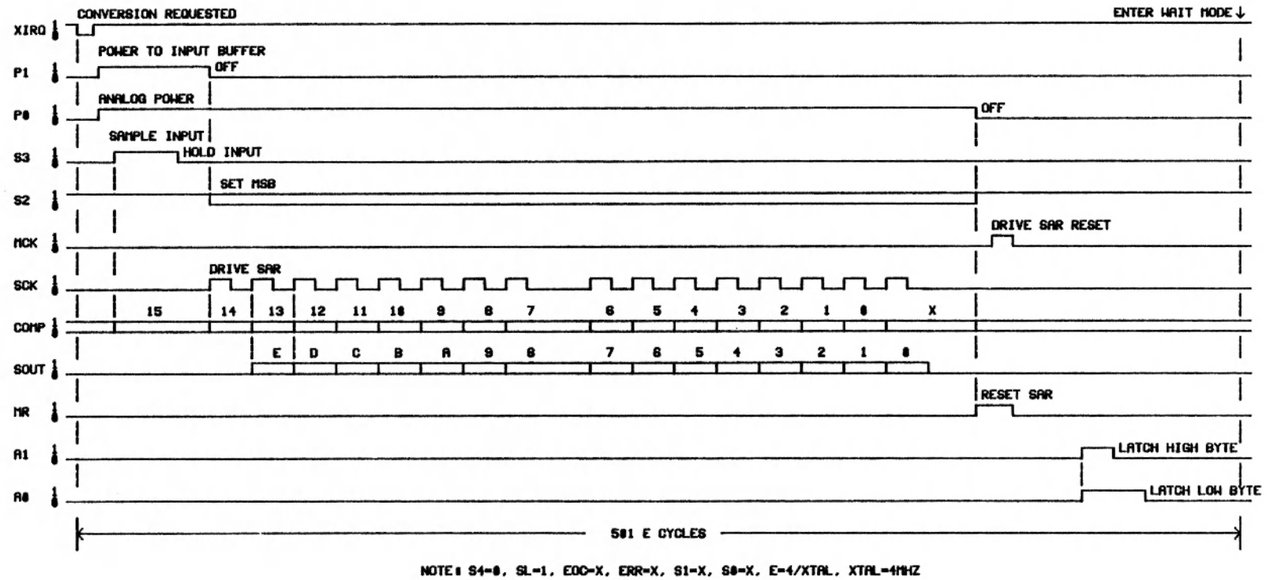


Figure D.4 Timing Diagram of A Single SCSH DAS A/D Conversion

```
*************************************************************
**                          SCSHDAS                        **
*************************************************************
*
*       THIS PROGRAM CONTROLS THE SCSH DAS ANALOG SECTION
*   THROUGH SINGLE CONVERSIONS OF A SINGLE INPUT CHANNEL.
*   THE PROGRAM RESIDES IN WAIT MODE UNTIL A CONVERSION
*   IS REQUESTED FROM THE HOST SYSTEM (HP9845 COMPUTER
*   EXECUTING THE PROGRAM "ADC1_2").  EACH CONVERSION IS
*   INITIATED BY THE OCCURANCE OF AN XIRQ INTERRUPT.  THE
*   CONVERSION RESULT IS STORED IN AN OUTPUT LATCH THROUGH
*   PORT D BEFORE THE PROGRAM RETURNS TO THE WAIT MODE.
*
*       ALL COMMENTS AND ADDRESS LABELS MUST BE REMOVED
*   FROM THIS LISTING BEFORE IT CAN BE AUTO-TYPED TO THE
*   BUFFALO MONITOR.
*
*   STEVEN D. DRAVING                              8/25/85
*
*************************************************************
*
*
*
     A 8000          BEGIN ASSEMBLY AT ADDRESS 8000
8000 LDAA #7E        INITIALIZE XIRQ JUMP VECTOR
     STAA F1
     LDX #806F
     STX F2
     LDAA #00        CONFIGURE PARALLEL HANDSHAKE PORTB
     STAA 1002
     LDAA #00        CLEAR PORT A
     STAA 1000
     LDAA #FF        SELECT OUTPUT PORT C
     STAA 1007
     LDAA #82        SET DATA PORT C
     STAA 1003
     LDAA #F2        SET DATA DIRECTION PORT D
     STAA 1009
     LDAA #00        CLEAR PORT D
     STAA 1008
     LDAA #56        CONFIGURE SPI INTERFACE
     STAA 1028
     LDAA 1029       CLEAR SPIF FLAG
     LDAA 102A
     LDX #0000       GENERATE ERROR CORRECTION TABLE
     STX 0000
     LDX #2000
     STX 0002
     LDX #4000
     STX 0004
     LDX #6000
```

```
     STX 0006
     LDX #8000
     STX 0008
     LDX #A000
     STX 000A
     LDX #C000
     STX 000C
     LDX #E000
     STX 000E
     LDY #1000       SET POINTER TO PORT A
     LDAB #8E
     TPA             ENABLE XIRQ INTERRUPT
     ANDA #BF
     TAP
806C WAI             ENTER WAIT MODE
     BRA 806C        GOTO BACK TO SLEEP

     A 806F
806F STAB 1003       POWER-UP ANALOG COMPONENTS
     LDAA #40
     STAA 1000       BEGIN SAMPLING, S3=1
     LDAA 1000       PAUSE 16 E CYCLES, 16uS IF XTAL=4MHz
     LDAA 1000
     LDAA 1000
     LDAA 1000
     LDAA #00
     STAA 1000       END SAMPLING, S3=0
     LDAB #06        MASK DATA FROM PORT E
     ORAB 100A       READ MSB FROM PORT E BIT 7
     STAB 1003       P1=0, S2=MSB
     STAB 102A       BEGIN CLOCKING SARS WITH SCK
     LDX #17         PAUSE 164 E CYCLES
8096 DEX
     BNE 8096
     LDAA 1029       CLEAR SPIF FLAG
     STAA 102A       CONTINUE CLOCKING SARS
     ANDB #80        MASK ALL BUT MSB
     STAB 101E       REMEMBER ACC. B
     LDAB 102A       READ HIGH BYTE OF DAC FROM SPI
     ANDB #7F        INSERT CORRECT MSB
     ORAB 101E
     LDX #0011       PAUSE 121 E CYCLES
80AF DEX
     BNE 80AF
     PSHB            PUSH HIGH BYTE ON STACK
     LSRB            CALCULATE POINTER FOR ERROR CORRECTION
     LSRB
     LSRB
     LSRB
     LSRB
     LSLB
```

```
LDX #0000
ABX
LDAA #83
LDAB 1029       CLEAR SPIF FLAG
LDAB 102A       READ LOW BYTE OF DAS FROM SPI
STAA 1003       P0=0, S2=1, MR=1
LDAA #93        CLOCK SAR RESET, MCK=1
STAA 1003
LDAA #82        MCK=0, MR=0
STAA 1003
PULA            RECALL HIGH BYTE FROM STACK
ANDA #1F        STRIP OFF FIRST THREE MSB'S
LSLD            PERFROM ERROR CORRECTION
ADDD 00,X
COMA            INVERT AND SHIFT RESULT
COMB                 TO GET POSITIVE OFFSET BINARY
LSRD
BSET 00,Y 30    OUTPUT HIGH BYTE TO LATCH
STAA 1004
BCLR 00,Y 20    OUTPUT LOW BYTE TO LATCH
STAB 1004
BCLR 00,Y 10
LDAB #8E        PREPARE FOR NEXT CONVERSION
RTI             RETURN FROM INTERRUPT
```

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AN EVALUATION OF THE MC68HC11A8 SINGLE-CHIP MICROCOMPUTER AS A CONTROLLER FOR LOW-POWER, PRECISION A/D CONVERTERS

by

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Abstract

The MC68HC11A8 Single Chip Microcomputer is evaluated as a controller for low-power, precision A/D converters. Performance tests of the MC68HC11A8's power consumption and on-chip ADC were performed and their results are discussed. A functional description of the MC68HC11A8's I/O interfaces are also presented.

Physical size and power consumption advantages of the MC68HC11A8 over an existing microprocessor system are demonstrated in an Ragsdale-Doerfler-Bradley (RDB) data acquisition system (DAS) control application. Details of the MC68HC11A8's control of the RDB DAS and the verification tests performed are discussed.

Four, low-power, precision analog-to-digital conversion (ADC) techniques are presented which utilize the MC68HC11A8 to perform switch control and error correction. These four ADC techniques are compared and one, the switched-capacitor sample-and-hold (SCSH) DAS, is selected as the RDB DAS's successor. A single-channel prototype of the SCSH DAS is then presented which uses the MC68HC11A8 for control. The correct control of the SCSH DAS is verified by the SCSH DAS's preliminary test results.