DIGITALLY PROGRAMMABLE DELAY GENERATOR

by

MAULIN I. PATEL

B.S., Sardar Patel University, Gujarat, India, 1985

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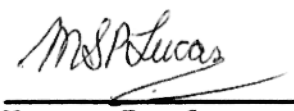
Approved by:



Major Professor

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Finally, my thanks are due to my family whose support and inspiration has helped me throughout my graduate study.

1.0 INTRODUCTION:

A Voltage Step Generator(VSG) was designed and developed at the National Bureau of Standards(NBS). The VSG was designed for use in automated test systems to characterize the transient response of waveform recorders, oscilloscopes, and other instruments. The VSG was designed to output programmable pulses with one well defined transition per period with known beginning and terminating levels of transitions [1].

The heart of the design of the NBS VSG is its control unit, which performs and controls the above mentioned functions. An attempt was made to redesign the timing circuit of the control unit to achieve the same goals, but with different hardware configuration. Hence a digitally programmable delay generator chip, AD9500 of the Analog Devices was used for the timing control functions of the NBS VSG control unit.

The AD9500 can be used in different configurations such as minimum configuration, extended pulse-width configuration, ring oscillator configuration etc. For each configuration extensive tests were made and results were recorded. The section 3.3 of this report describes these configurations briefly. Finally the ring oscillator configuration was selected for the above mentioned purpose. Thus the AD9500 was

characterized for different configurations using the Analog Devices products specification literature. In order not to constrict the flow of presenting the required material for this report, specifications of AD9500 are in Appendix A [3].

This report contains all the technical information and experimental results obtained in the attempt to use the AD9500 for the timing control functions of the NBS VSG control unit.

2.0 Introduction to the NBS Voltage Step Generator [1]:

The NBS Voltage Step Generator(VSG) was designed to output programmable voltage pulses, with one well-defined transition per period, with known beginning and terminating levels of transitions. The VSG consists of the output circuit and the control unit.

The output circuit is a test-head which connects directly to the input terminals of the device under test. The control unit provides the power, precision dc voltage levels, polarity selection pulses and timing pulses necessary to control the parameters of the voltage steps generated in the output circuit. Fig. 1 shows the VSG in an automated test system.

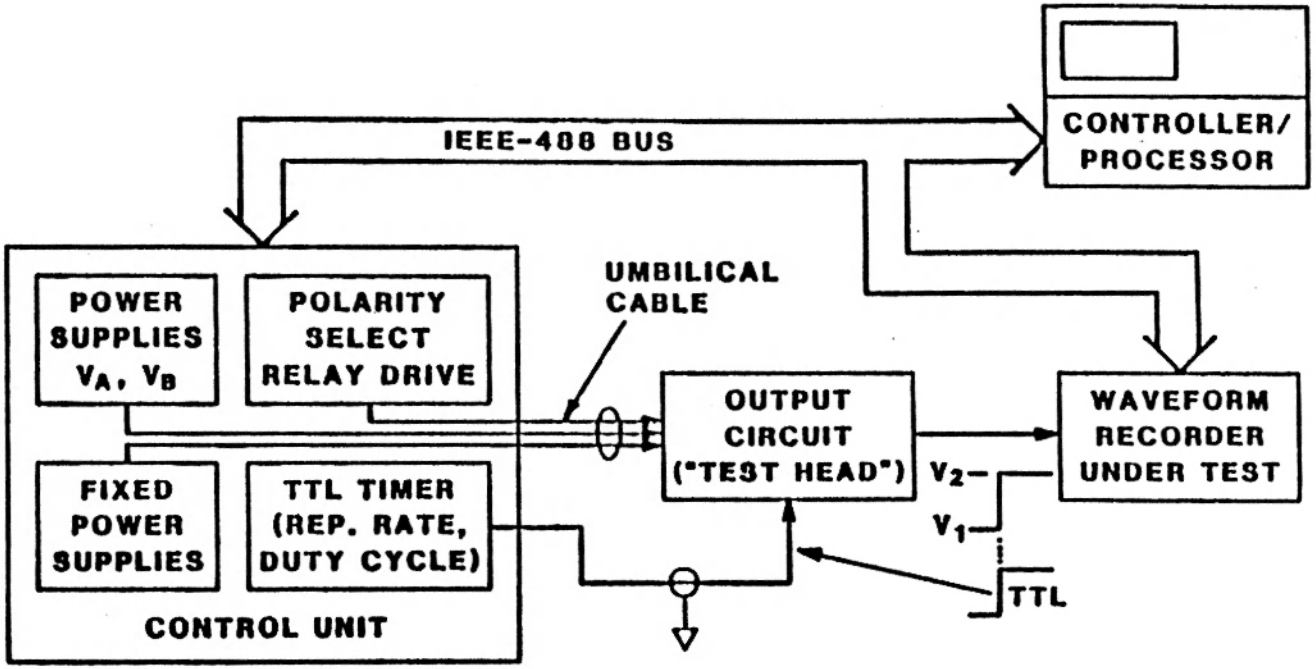


Fig. 1 Automated test system with VSG
[H. K. Schoenwetter et. al, 'A Precision Programmable Step Generator for Use in Automated Test Systems', NBS Technical Note 1230, Dec. 1986, p.10 [1]]

2.1 VSG Requirements [1]:

The minimum requirements of the NBS VSG are as follows:

1) The initial and the final levels of the voltage transitions should be independently adjustable, and each should have a range of at least +5V or -5V for high impedance loads and a range of +1V or -1V for range of 50 ohms loads.

2) The transition duration(10-90% Rise time) of the voltage steps should be less than 7 ns.

3) The voltage step should settle to within ±0.1% and ±0.02% of final level voltage in less than 22 ns and 27 ns, respectively, measured from the 10% amplitude point.

4) The output impedance of the VSG should be resistive for frequencies ranging from dc to several times the upper cut off(-3 dB) frequency of the test instrument.

5) The VSG output circuit should be directly connectable to avoid losses and pulse distortion from a connecting cable.

6) The pulse width and pulse repetition rate should be independently selectable, with pulse widths ranging from 50 ns to 5 ms and repetition rates upto 5 MHz.

7) All pulse parameters should be programmable, so that the VSG may be used in automatic test systems.

2.2 VSG Control Unit [1]:

The Fig. 2 shows a complete block diagram of the control unit. The IEEE-488 bus is used to provide overall control. The bus interface drives a system bus to distribute data for controlling the operating parameters of the VSG output circuit. The parameters are: the pulse repetition rate, pulse length, voltage step polarity, and the initial and final voltage levels of the step. The respective ranges for each pulse parameters are as follows:

- pulse repetition rate: 153 Hz to 5 MHz
- pulse length: 20 ns to @ 6 ms
- duty cycle: approximately 5% to 95%
- initial and final voltage levels: +5V or -5V
- polarity of transition: either + or -

The whole control unit contains the following boards(modules):

1) IEEE-488 interface
2) TTL Timing board
3) DAC/OA board
4) Output board
5) All the required power supplies

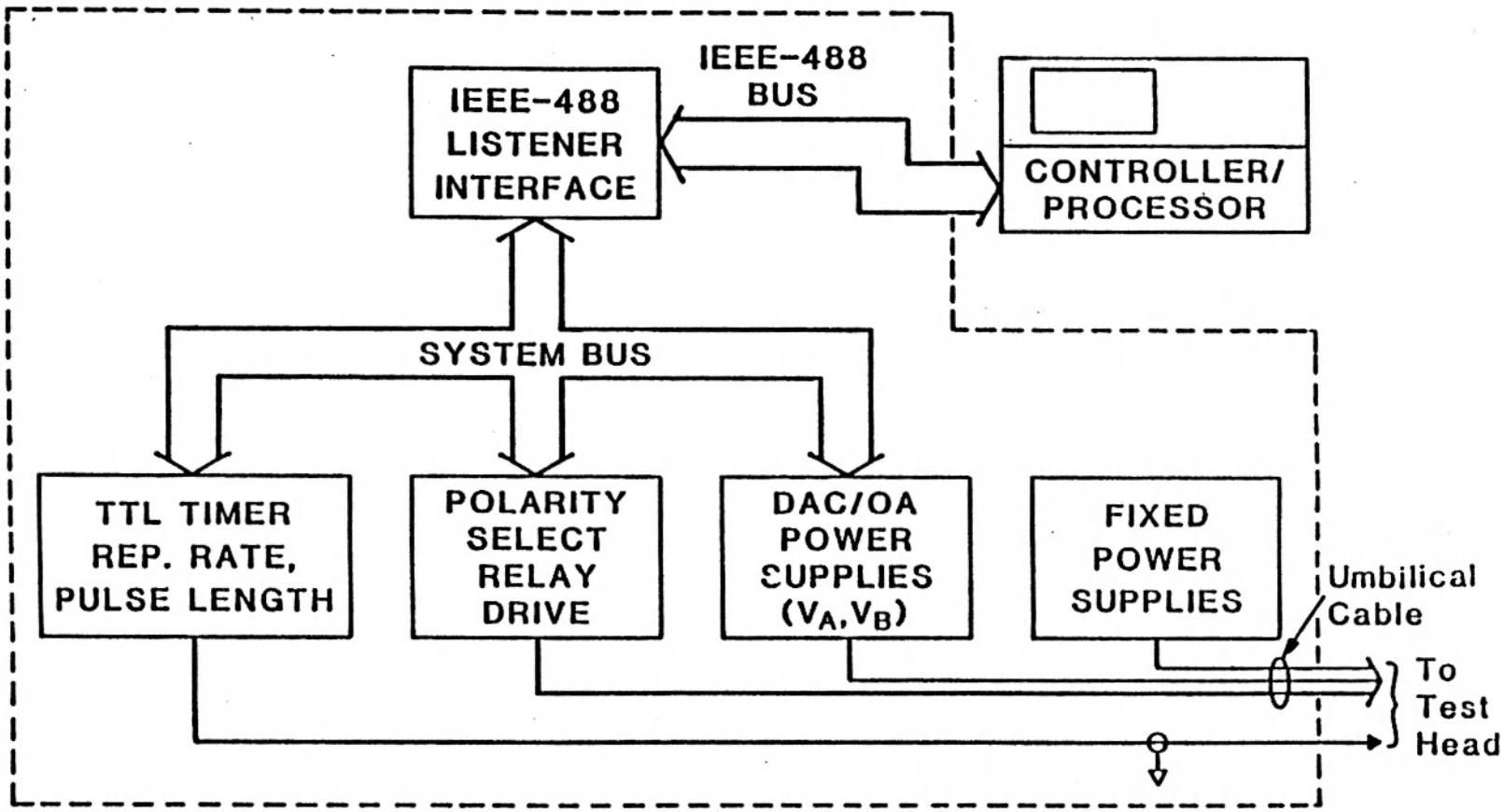


Fig. 2 Complete Block Diagram of the NBS VSG Control Unit
[H. K. Schoenwetter et. al, 'A Precision Programmable Step Generator for Use in Automated Test Systems', NBS Technical Note 1230, Dec. 1986, p.18 [1]]

Fig. 3 shows the timing board circuit, which controls the pulse repetition period and the pulse length of the voltage steps as well as the internal/external clock choice. A brief explanation of the circuit in the Fig. 3 is as follows:

The inputs to the chip address decoder U11 are obtained from outputs of the board address decoder of the IEEE-488 interface board. 4-bit data words from the board data bus are sequentially loaded into registers U1 through U10, with change in the input code by 1 bit.

The data words(codes) that have been latched into registers U3-U10 are preset into counters U21-U28. The pulse repetition period of the step generator is determined by the code value present into counters U21 through U24, and equals the complement of this code times the(10 MHz) clock period. The code values in counters U25-U28 are used to control the pulse length. A D-type flipflop with clear and preset, a delay chip and a dual 4-line to 1-line MUX are used to achieve the above mentioned timing functions.

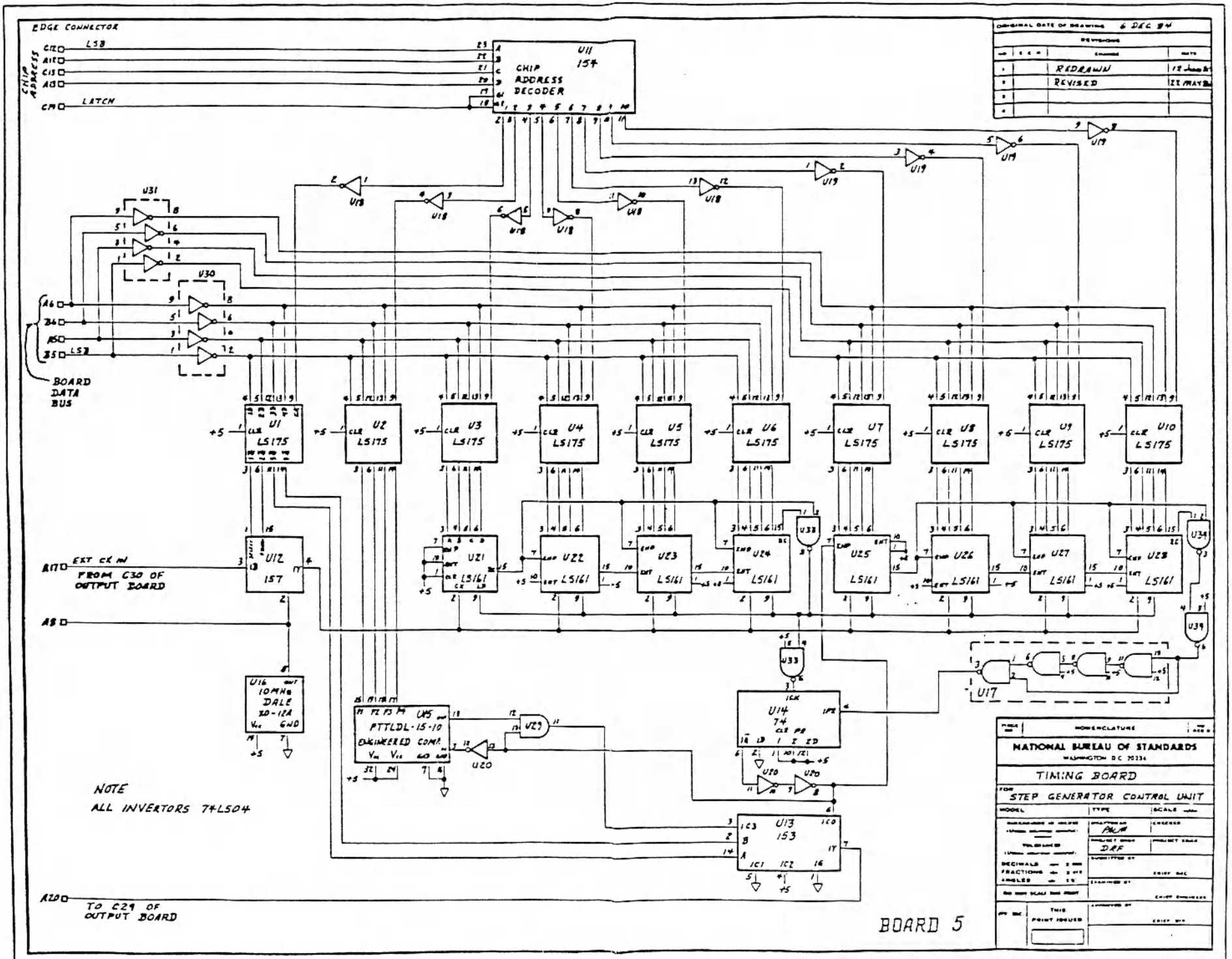


Fig. 3 Timing board circuit of the NBS VSG [p.37 1]

This circuit uses the TTL logic levels only. Hence a new approach to gain the control over pulse repetition period and the pulse length was attempted using Analog Devices digitally programmable delay generator chip AD9500, which is discussed in the following sections.

3.0 Digitally Programmable Delay Generator Chip : AD9500

3.1 Introduction [3] [4]:

The AD9500 is a digitally programmable delay generator which includes virtually all the circuits needed for generating time delays for digital pulses. It provides 256 programmed delays in a user-specified full scale range which can be varied from 2.5 ns to 100 us and more. The 2.5 ns scale can resolve increments as small as 10 picoseconds.

The output of the AD9500 is delayed from the input trigger pulse by a time proportional to the 8-bit digital input code. In addition, the AD9500 is ECL compatible and usable with analog as well as TTL input levels. A full scale delay range is very flexible and can be set externally by using a proper R-C combination.

Fig. 4, shows the pin configurations of the AD9500. For a detailed description of each pin, please refer to the Appendix-A.

The AD9500 has trigger and reset inputs which are differential and are designed primarily for ECL signal levels, but they can also function with analog and TTL input levels. An on-board ECL reference midpoint allows both the inputs to be driven by either single-ended or differential ECL circuits. The output of the AD9500 is a complementary ECL stage, which also provides

a parallel output($\overline{Q}_R$) circuit to facilitate reset timing implementations. The maximum triggering rate for the input of the AD9500 is 100 MHz. The digital input code is passed to the AD9500 through a transparent latch which is controlled by the LATCH ENABLE signal. In the transparent mode, the internal DAC of the AD9500 will attempt to follow changes at the input, otherwise LATCH ENABLE is used to strobe the digital data into the AD9500 latches.

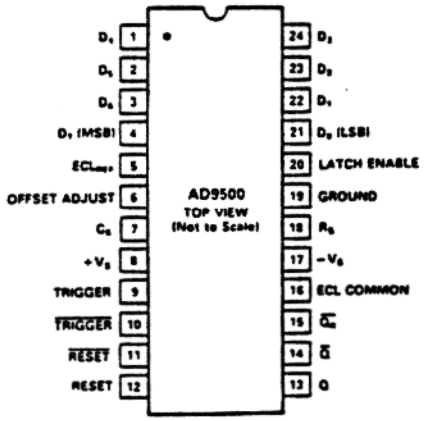


Fig. 4 Pin configurations of the AD9500
["Digitally Programmable Delay Generator", A technical literature by Analog Devices [3], p.1]

3.2 How it works [3] [4]:

The heart of the AD9500 is the linear ramp generator. The initiation of a ramp cycle is done by any triggering event at the input of the AD9500. An internal Digital to Analog Converter(DAC) sets up the threshold voltage and hence as the ramp voltage falls down, eventually it will definitely fall below the threshold level. These levels (linear ramp and DAC threshold) both are monitored by a comparator. The output of the AD9500 is the output of this comparator stage. The time interval between the trigger and the output transition is the total delay time generated by the AD9500.

Fig. 5 shows the functional block diagram of the AD9500. The important functional modules are the reference and the timing-control circuit-which form an analog integrator; an 8-bit DAC, set by the 8-bit digital control input(code); and a high-speed precision comparator with complementary ECL outputs. The trigger and the reset inputs are differential and the triggering rate cannot be greater than 100 MHz for the AD9500.

The timing diagram in Fig. 6, shows that the programmed delay is initiated when the trigger input goes high. It initiates a falling ramp from the integrator and when it crosses the threshold level set by the 8-bit DAC, the comparator output is changed which

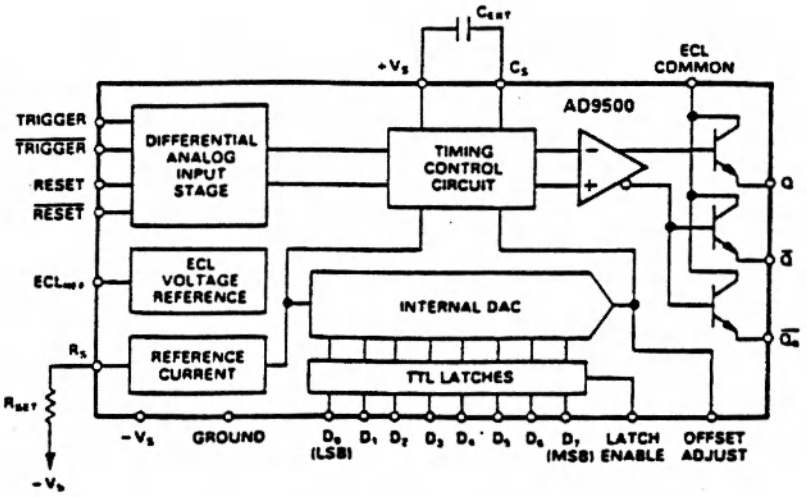


Fig. 5 Functional block diagram of the AD9500
["Digitally Programmable Delay Generator", A technical literature by Analog Devices [3], p.4]

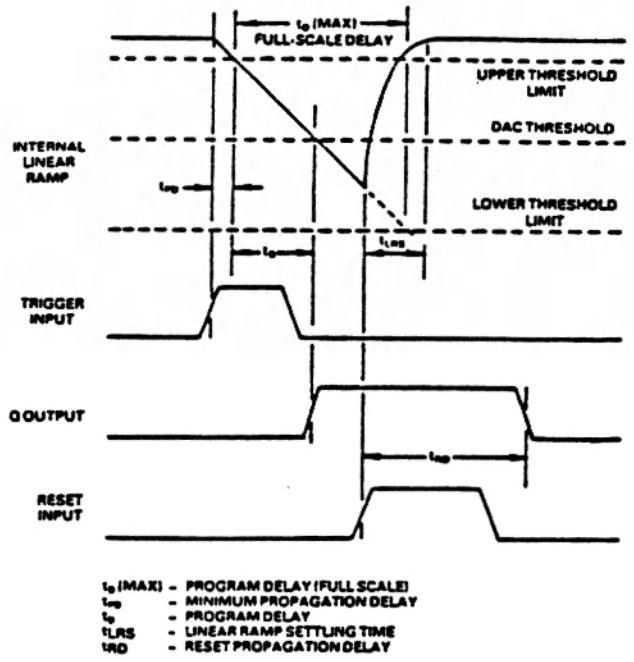


Fig. 6 Timing diagram for the AD9500
["Digitally Programmable Delay Generator", A technical literature by Analog Devices [3], p.7]

produces the required delay outputs (Q and $\bar{Q}$). A parallel $\bar{Q}_R$ output is also made available on the AD9500, to control the driving of its own reset input.

The total delay through the AD9500 is made up of the two major components:

1) the programmed delay(t_D) - a function of the selectable RC time constant and the precision threshold set by the DAC.

2) the propagation delay(t_{PD}).

Fig. 7 shows some typical values of the programmed delay ranges as a function of resistance and capacitance, with the digital input = 255 or $FF(hex).

The actual programmed delay is directly related to both of the digital input data and the RC time constant established by R_{SET} and C_{EXT}. The relationship is as follows:

Total Delay = Minimum propagation delay + Programmed delay

$$= t_{PD} + (\text{digital input}/256)R_{SET}(C_{EXT} + 10pF)$$

The LATCH ENABLE control pin is active LOW. In the logic "LOW" state, the latch is transparent, and the internal DAC will attempt to follow the changes at the digital data inputs. Both the LATCH ENABLE control and the digital data inputs are TTL compatible.

A pulse of appropriate width applied at the reset input resets the integrator and the Q output. This

is due to discharging of the ramp voltage held in the timing capacitor(C_{EXT} + 10 pF). After the reset input goes low, the AD9500 is ready for the next trigger. The reset and the trigger inputs of the AD9500 are differential and must be driven relative to one another.

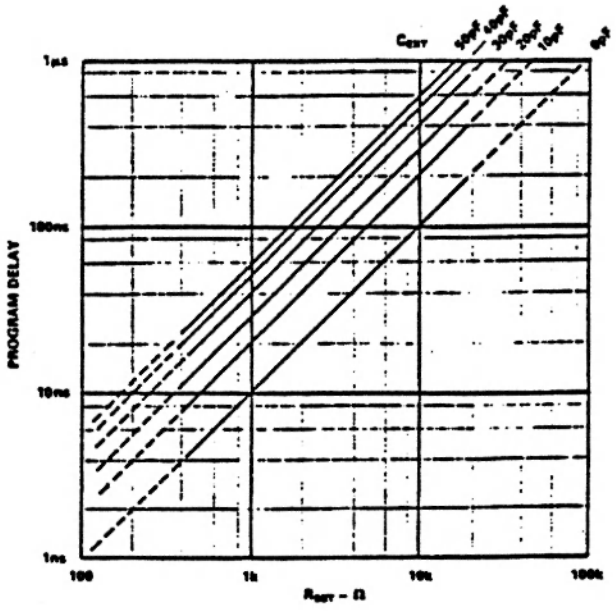


Fig. 7 Typical programmed delay ranges
["Digitally Programmable Delay Generator", A technical literature by Analog Devices[3], p.7]

3.3 Different Configurations [3] [4]:

The versatility of the AD9500 allows it to be configured for a number of different applications. As the trigger and the reset inputs can be treated as single-ended or as differential, the AD9500 can be operated with a wide range of signal sources. There are number of possible configurations for the AD9500. Some of them are minimum, extended output pulse width, ring oscillator, multichannel de-skewing, measurement of unknown delays, measuring high-speed AC waveforms. Only the ones which are useful for the purpose of this report, are discussed in the following sections. For information about the non-discussed ones, please refer to the references [3] and [4].

3.3.1 Minimum configuration:

In this configuration only one of the trigger inputs is used. The other is connected to the ECL reference midpoint, ECL_{REF}. The parallel output $\bar{Q}_R$ is grounded and $\bar{Q}$ is used to drive the reset input. Once the triggering event occurs, the Q output will go into logic "HIGH" state and the $\bar{Q}$ into "LOW" after the programmed delay. As the AD9500 is reset using $\bar{Q}$, the result is a delayed output pulse which is only as wide as the reset propagation delay (t_{RD}). Fig. 8 shows the circuit diagram for this configuration and Fig. 9 shows

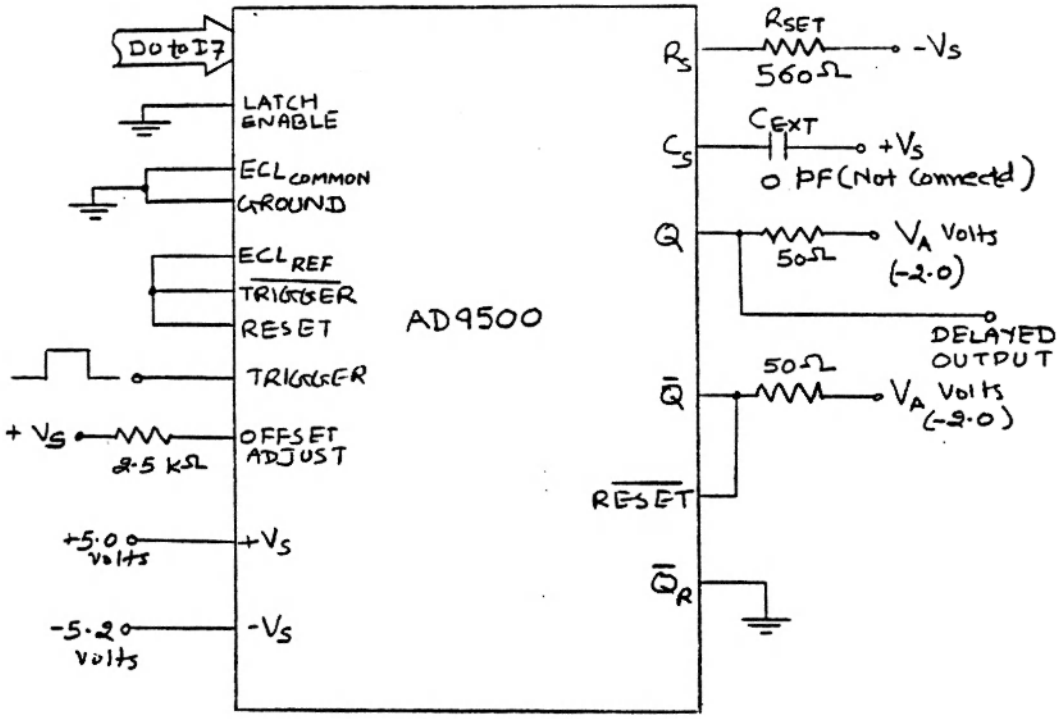


Fig. 8 Minimum configuration of the AD9500

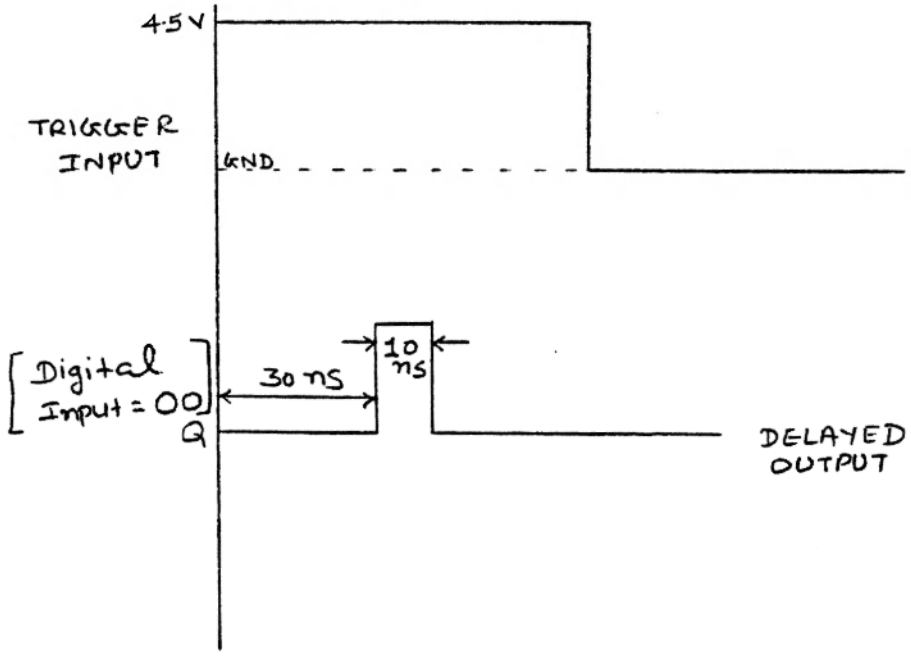


Fig. 9 Output obtained using the Minimum configuration

the output. It shows the delay achieved with the digital input = 00 and with the OFFSET ADJUST pin tied to $+V_S$ through a resistor(>220 ohms) value of 2500 ohms.

Note that in the Fig. 9 , the minimum delay with the zero(00) digital input, can be reduced further by not using the pin OFFSET ADJUST. By not using OFFSET ADJUST, a delay of about 8 ns was obtained which is the minimum delay we can have in this configuration with R_{SET} and C_{EXT} as in Fig 8. This was confirmed by the application engineer at the Analog Devices(Appendix-B).

3.3.2 Extended Output Pulse Width [3] [4]:

This configuration of the AD9500 is almost the same as the minimum configuration, except the output pulse width is extended in this case. Triggering the AD9500 is also the same but there is a functional difference in the resetting circuit.

In this case the output $\bar{Q}_R$ is used to drive the reset input through a resistor-capacitor(R_D - C_D) charging network. Due to this network, the signal at the reset input will fall more slowly which causes the output pulse width to be extended. The important advantage of this configuration is that the both Q and $\bar{Q}$ outputs are independent and are completely free for other uses.

Fig. 10 shows the circuit diagram for this

configuration. The total reset time contributed due to R_D and C_D is as follows:

Reset time = $t_{RD} + (R_D C_D / 1.85)$

[Note: please refer to the Appendix-B for the derivation of the term $R_D C_D / 1.85$]

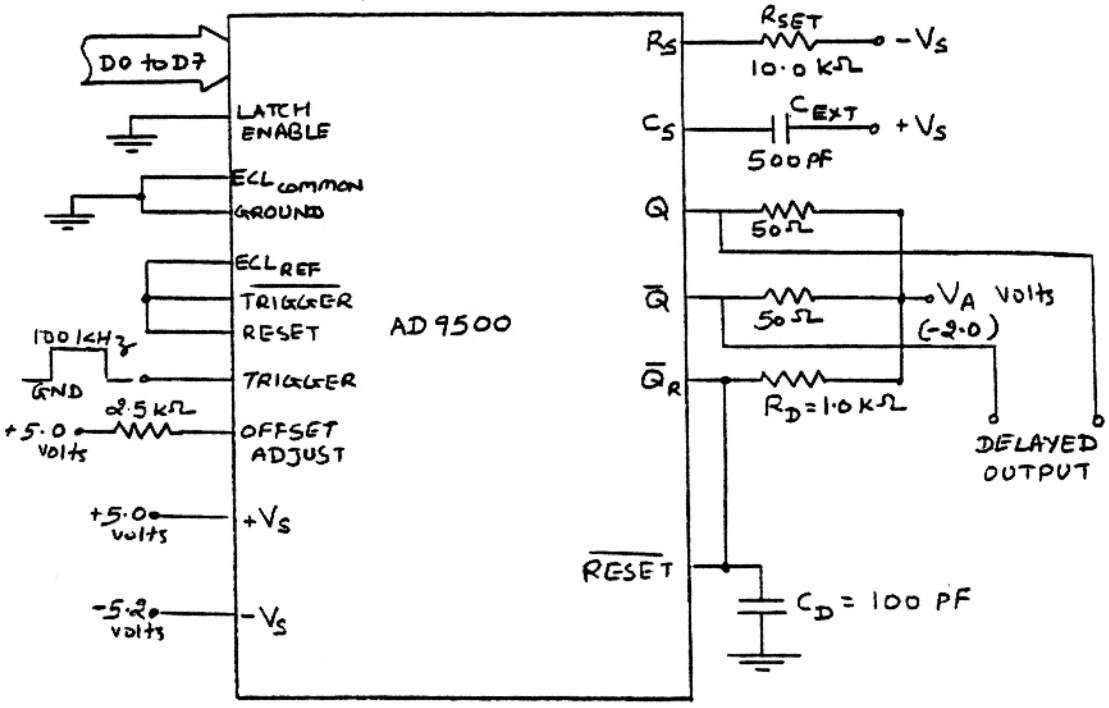


Fig. 10 Extended output pulse width configuration

Fig. 11 shows the output of the circuit shown above, with the values of R_D = 1000 ohms and C_D = 100 pF and the triggering rate of 100 kHz. In the Fig. 11, please note the following:

1) minimum delay value with the digital input = 00
2) change in pulse width with the increased digital input.

The above results are naturally not the obvious ones i.e one should expect a very low value of delay value with the digital input = 00 and the pulse width should not change(reduce in this case) with the higher value of the digital input. The questions concerning these results were asked to the application engineer at the Analog Devices and are discussed in the Appendix-B.

It was found that by simply changing the values of R_D and C_D appropriately, the output pulse width was changing accordingly i.e. one can control the duty cycle of the output pulse by controlling the R_D and C_D .

In both the configurations discussed above(minimum and extended pulse width), the frequency of the output pulse depends on the rate at which the AD9500 is triggered. That means to change the output pulse frequency, one has to change the triggering rate externally everytime. This is eliminated in the ring oscillator(programmable oscillator) configuration as in

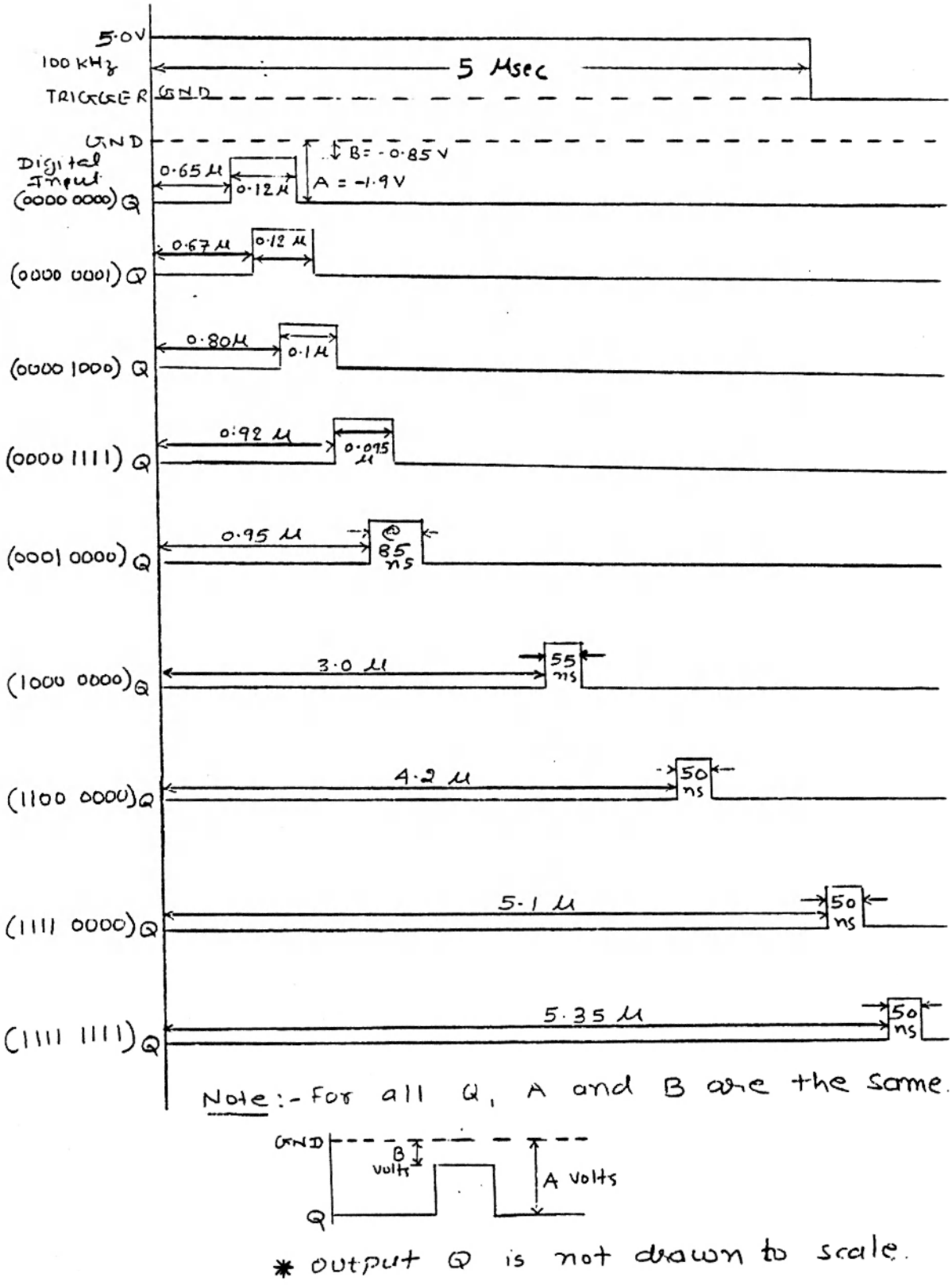


Fig. 11 Output of the extended pulse width configuration

this configuration the output pulse frequency is determined by the digital input data. Also the output pulse width can be controlled by applying the output of this configuration to a simple logic circuit (e.g. Set-Reset flipflop).

3.3.3 Ring oscillator configuration [3] [4]:

The ring oscillator configuration or the programmable oscillator configuration is one of the most interesting and important use of the AD9500. As mentioned in the section 3.3.2, this configuration can control both the frequency and the duty cycle, of the output pulse of the AD9500.

Fig. 12 shows the block diagram for this configuration. Two AD9500s are used for this configuration. The delayed output of the first AD9500 is used to drive the trigger input of the second AD9500. The output of the second AD9500, in turn, is used to drive the trigger input of the first AD9500. Because of cascading these two AD9500s in such a back-to-back configuration, together the two devices will alternately trigger each other creating two pulse chains (trains) on the outputs.

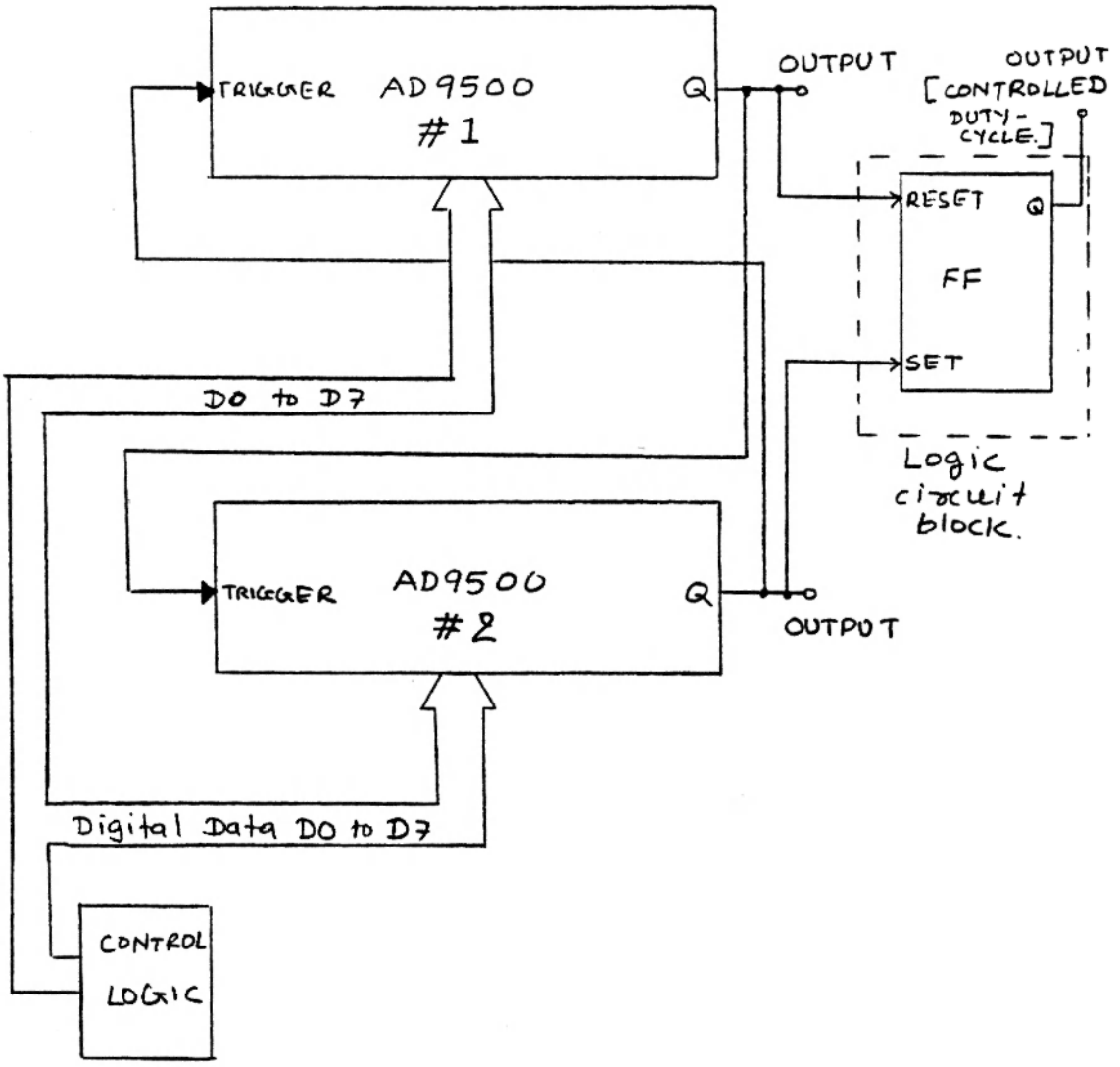


Fig. 12 Block diagram of the ring oscillator configuration

The total delay through both the AD9500s combined, determines the period of the oscillation and hence the frequency. By using the outputs of both the AD9500s to drive the Set and the Reset inputs of a (S-R) flipflop, the duty cycle of the output pulse can be controlled. The total delay through the first AD9500

will control the flipflop logic LOW output pulse width, and the second AD9500 will control the flipflop logic HIGH output pulse width.

Thus in this configuration, as both the pulse repetition rate and the pulse length of the output, are controlled effectively by the digital input to the AD9500, this configuration was used for the timing circuit design of the NBS Voltage Step Generator(VSG).

4.0 Timing control circuit for VSG using the AD9500:

4.1 Introduction:

One of the basic requirement for the NBS VSG is to have an independent control over the output pulse frequency and the duty cycle. As discussed in the previous section, in the ring oscillator (programmable oscillator) configuration of the AD9500, it is possible to have an effective control over the output pulse repetition rate(frequency) and the pulse length(duty cycle). Hence an attempt was made to use the AD9500 in the ring oscillator configuration, which can be used for the timing control circuit for the NBS VSG.

Fig. 13 shows the block diagram of the timing control circuit for the VSG using the AD9500, where the AD9500 is used in the ring oscillator configuration.

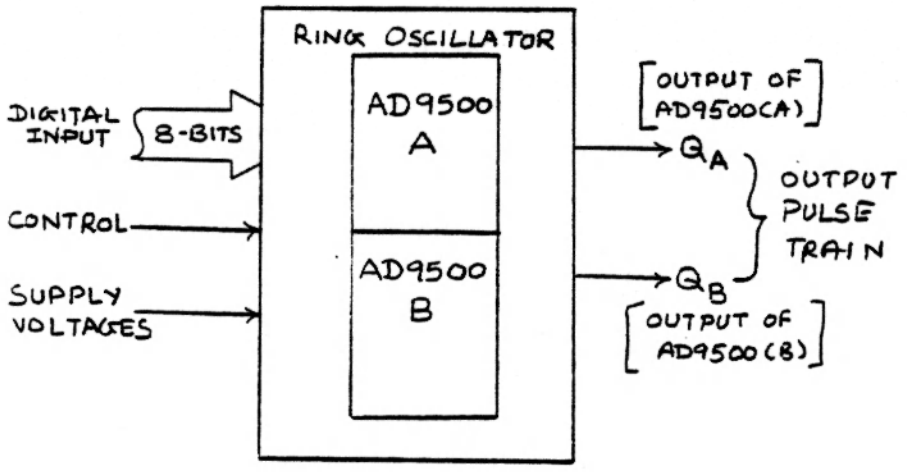


Fig. 13 Block diagram of the timing circuit for VSG using the AD9500.

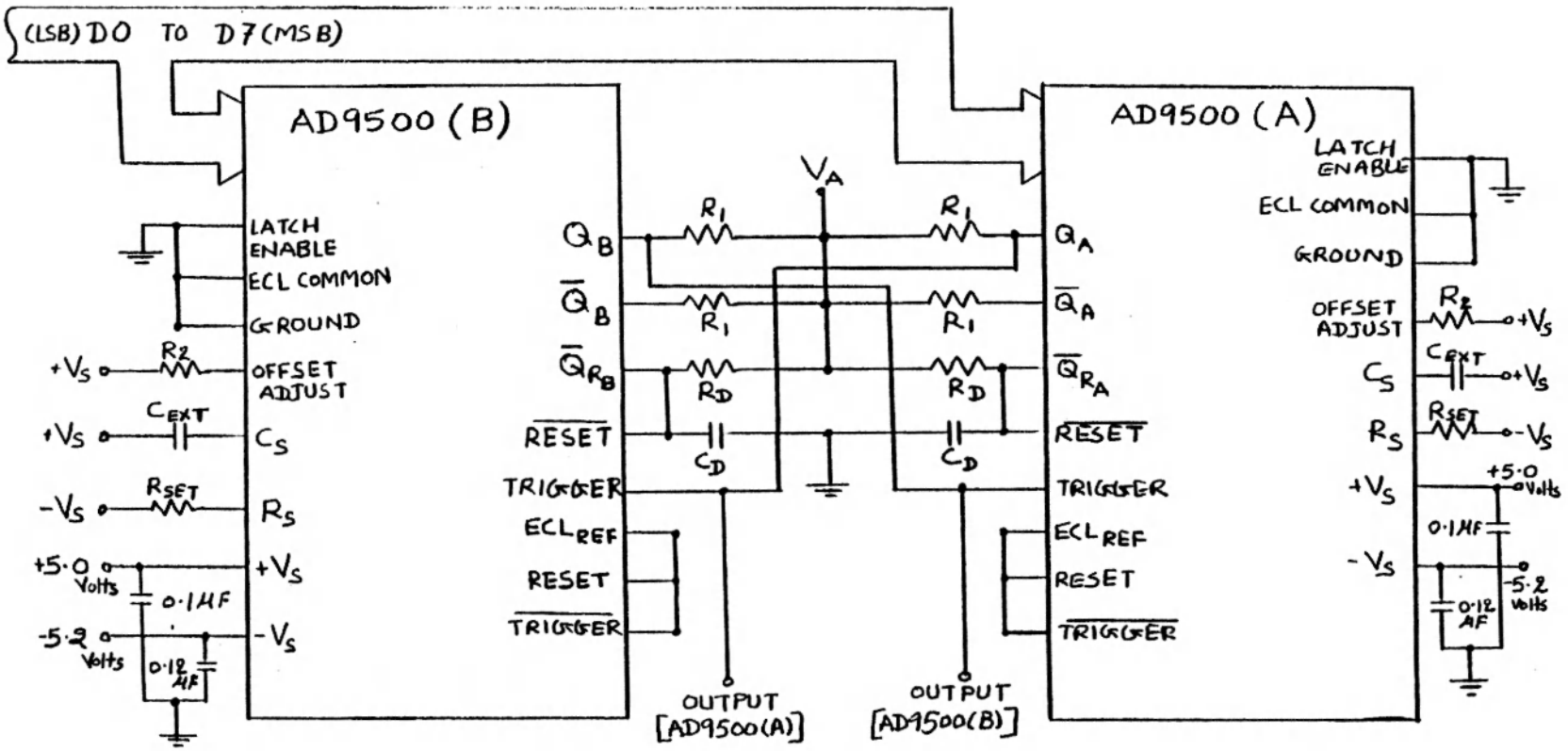


Fig. 14 Complete circuit diagram of the timing circuit for VSG using the AD9500

Fig. 14 shows the complete circuit diagram of the system shown in fig. 13. In fig. 14, there are two AD9500s connected in the ring oscillator configuration. The output (Q_A) of the first AD9500(A) is used to trigger the second AD9500(B) and viceversa. As both the AD9500s are triggering each other alternately, a pulse train(chain) is created at the outputs (Q_A, $\bar{Q}_A$, Q_B and $\bar{Q}_B$). For simplicity, only Q_A and Q_B outputs are used while taking the readings of the experiment, for this report.

R_D and C_D are used to delay the resetting of the output of the respective AD9500. R_{SET} and C_{EXT} are used to extend the full scale delay. As the full-scale delay is increased, a component of the minimum propagation delay (t_{PD}) also increases. To reduce this propagation delay, an offset is introduced in the internal DAC threshold level by injecting some current through the pin OFFSET ADJUST of the AD9500. This is done by connecting OFFSET ADJUST to $+V_S$ through a resistor of 4700 ohms.

The delay through each AD9500 is determined by the digital input. The total delay through each AD9500 combined determines the output pulse repetition rate. Hence by changing the digital input to the system, we can change the pulse repetition rate and hence the output frequency.

The circuit in the fig. 14 was constructed on a bread-board. To avoid the high frequency noise problems and to have a common ground base, only one power supply was used to power the whole circuit. The circuit requires regulated voltages of the magnitude 5.0 V, -5.2 V and -2.6 V. Hence the regulators with the above mentioned output voltages were used for the circuit in the Fig. 14. The Following section describes briefly the circuit and related design calculations of each regulator, with the required output.

4.2 Voltage Regulators [5]:

Three voltage regulators with the output voltages of 5.0 V, -5.2 V and -2.6 V, were required.

[1] Voltage Regulator with output = 5.0 V :

Fig. 15 shows the circuit diagram for this regulator. The LM340-TS (5.0 V, 1.0 A) regulator is readily available for this purpose.

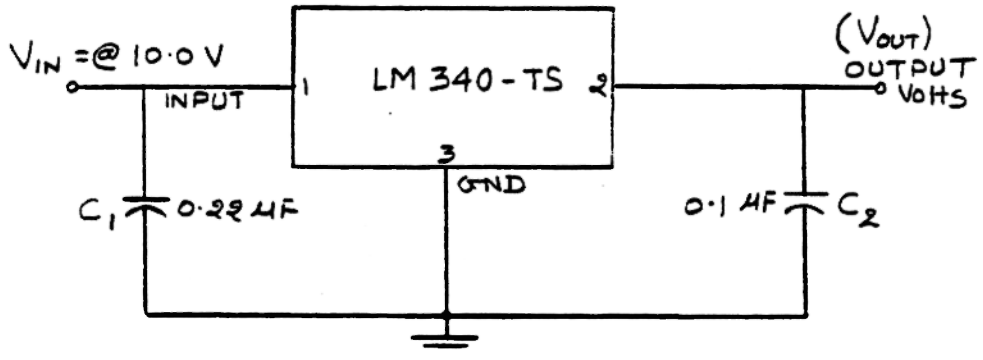


Fig. 15 Voltage Regulator with output = 5.0 V

In the Fig. 15, C_1 is used as it helps to reduce the noise at the input, if the regulator is far from the main power supply. Also, C_2 is used as it improves the transient response.

[2] Voltage Regulator output = -5.2 V :

The LM337T is a programmable -ve output(@0.5A) regulator, hence it was used to obtain an output voltage of -5.2 Volts. Fig. 16 shows the circuit diagram for this regulator.

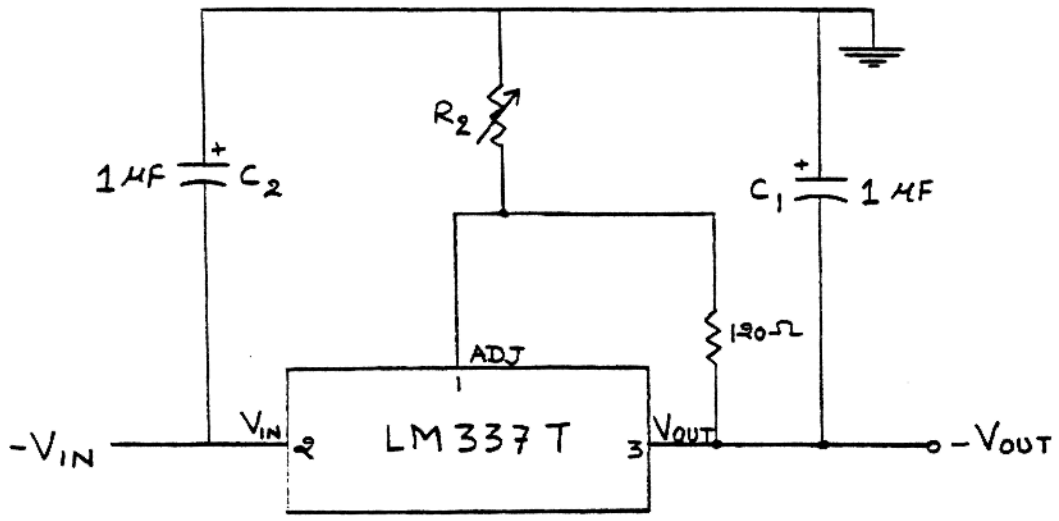


Fig. 16 Voltage Regulator with output = -5.2 Volts

$C_1 = C_2 = 1$ uF (solid tantalum). These are used for the noise reduction and the stability of the regulator. In the Fig. 16, to find the appropriate value of R the following equation was used:

$$-V_{OUT} = -1.25(1 + (R_2/120\text{ohms})) \quad \ldots\ldots\ldots\ldots\ldots (A)$$

We have, $-V_{OUT}$ = -5.2 Volts; therefore;

$$-5.2 = -1.25(1 + R_{\ell}/120\text{ohms}))$$

$$\Rightarrow R_{\ell} = @\ 379\ \text{ohms}$$

Hence a potentiometer(pot) of the value of 1.0 Kohms was used and the output was set exactly to -5.2 Volts.

Similarly for the regulator with output = -2.6 V, the same configuration as in the Fig. 16, was used. Only the value of R_{ℓ} was changed accordingly. If we follow the equation (A) with V_{OUT} = -2.6 V, then the calculated value of the R_{ℓ} = @ 130 ohms. Hence a pot of 1.0 Kohms was used to set the output exactly equal to -2.6 Volts.

4.3 Experimental Setup:

The circuit shown in Fig. 14, was constructed on a single bread-board(of the type A.C.E. 236), with a common ground plane. Fig. 17 shows the block diagram of the experimental setup.

The HP-6236B (triple-output power supply) was used to power the whole circuit. The HP-1720A, an oscilloscope with 275 MHz bandwidth, was used to observe the output of the circuit in Fig. 14. Also the HP-3466A; digital multimeter; was used to measure the required voltage levels during the experiment.

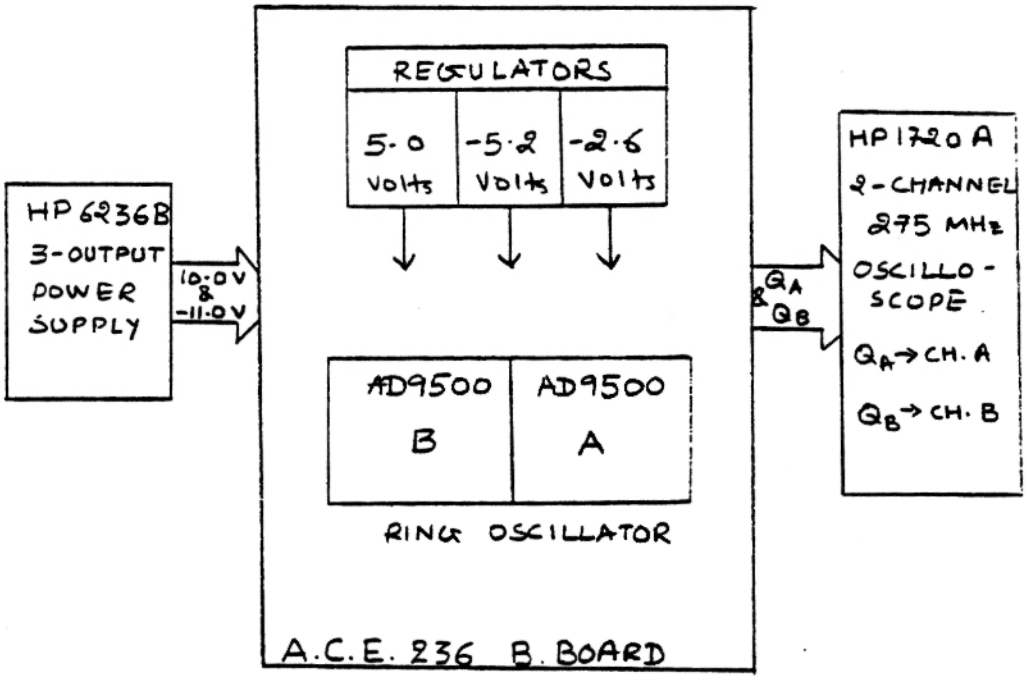


Fig. 17 The block diagram of the experimental setup

4.3.1 **Experimental Results:**

The circuit in Fig. 14 generated the pulse trains at the outputs. The frequency of these pulses was dependent on the digital input of the system. Though it was not possible to obtain good pulse outputs at lower digital inputs, the circuit generated very good pulse outputs for the value of the digital input greater than 0000 1100(hex). (Please refer to the section 4.4 for the difficulties during the experiment).

Table 1 and the Table 2 show the results obtained from the circuit shown in Fig. 14. Table 1 shows the relevent parameters for the first AD9500(A) and Table 2 shows the same for the second AD9500(B).

The resistors and the capacitors used in the circuit of Fig. 14 are responsible for the results in Table 1 and Table 2. The respective values of the resistors and the capacitors are as follows:

* R_1 = 50 ohms
* R_2 = 4700 ohms
* R_D = 1000 ohms
* C_D = 470 pF
* R_{SET}= 8200 ohms
* C_{EXT}= 500 pF

Also, for the readings in the Table 1 and the Table 2, refer to Fig. 18, showing the output of the circuit shown in Fig. 14. (Fig. 18 shows the symbolic

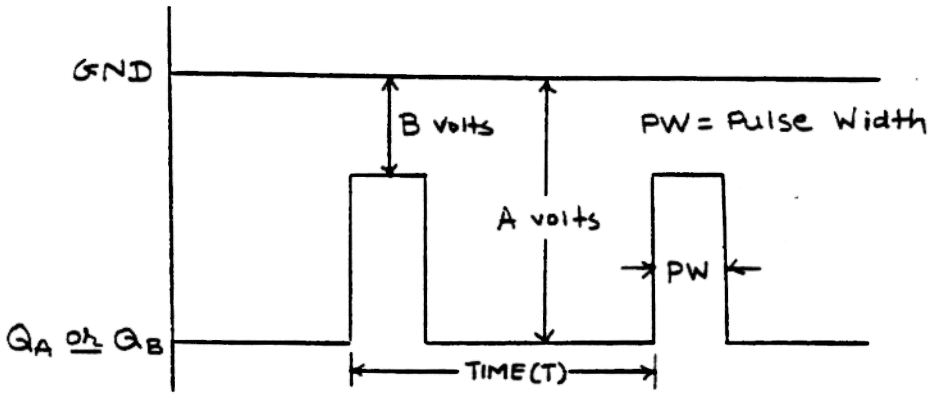


Fig. 18 Output of the circuit shown in the Fig. 14

output of the circuit while refering to the Table 1 and the Table 2)

Refering to the Fig. 18, for the Table 1 and Table 2, we have following for all the readings:

* A = -2.0 Volts
* B = -1.0 Volts
* V_A = -2.6 Volts (Fig. 14)
* V_S = 5.0 Volts (Fig. 14)
* $-V_S$ = -5.2 Volts (Fig. 14)

For the results in the Table 1 and the Table 2, the digital input was supplied as the voltage levels, as shown below:

For, logic HIGH (1) = 5.0 Volts

logic LOW (0) = 0.0 Volts (ground)

The current drawn by the circuit in the Fig. 14, including the voltage regulators, is as follows: (for max. digital input = 255 or $FF(hex))

* 10.0 Volts @ 100 mA , and
* -11.0 Volts @ 200 mA

[Note:- The HP 6236B was used as the main power supply.]

Digital Input 8-bits	Time(T) microsec	Pulse width	V_{Q_A} volts	$V_{\bar{Q}_A}$ volts	$V_{\bar{Q}_{RA}}$ volts
0000 1101	1.05 us	0.20 us	-1.780	-1.500	-1.140
0000 1110	1.10 us	0.20 us	-1.760	-1.500	-1.140
0000 1111	1.15 us	0.25 us	-1.740	-1.500	-1.120
0001 0000	1.20 us	0.20 us	-1.770	-1.500	-1.130
0001 1000	1.55 us	0.20 us	-1.825	-1.100	-0.978
0001 1111	1.85 us	0.20 us	-1.850	-1.080	-0.967
0010 1000	2.15 us	0.20 us	-1.860	-1.050	-0.957
0010 1111	2.40 us	0.20 us	-1.870	-1.020	-0.952
0100 1000	3.20 us	0.20 us	-1.950	-1.010	-0.950
0100 1111	3.40 us	0.20 us	-1.893	-0.994	-0.940
1000 1000	5.20 us	0.20 us	-1.913	-0.975	-0.936
1000 1111	5.40 us	0.20 us	-1.915	-0.961	-0.934
1111 1111	8.80 us	0.20 us	-1.925	-0.948	-0.928

Table 1 : Output of the AD9500(A) in the circuit of the fig. 14

Digital Input 8-bits	Time (T) microsec	Pulse width	V_{Q_B} volts	$V_{\bar{Q}_B}$ volts	$V_{\bar{Q}_{R_B}}$ volts
0000 1101	1.10 us	0.25 us	-1.728	-1.520	-1.320
0000 1110	1.15 us	0.25 us	-1.728	-1.520	-1.320
0000 1111	1.15 us	0.25 us	-1.710	-1.500	-1.120
0001 0000	1.20 us	0.20 us	-1.750	-1.500	-1.130
0001 1000	1.55 us	0.20 us	-1.800	-1.100	-0.967
0001 1111	1.85 us	0.20 us	-1.826	-1.080	-0.954
0010 1000	2.15 us	0.20 us	-1.840	-1.040	-0.942
0010 1111	2.40 us	0.20 us	-1.850	-1.030	-0.936
0100 1000	3.20 us	0.20 us	-1.880	-1.000	-0.933
0100 1111	3.40 us	0.20 us	-1.879	-0.987	-0.924
1000 1000	5.20 us	0.20 us	-1.902	-0.962	-0.919
1000 1111	5.40 us	0.20 us	-1.901	-0.956	-0.917
1111 1111	8.80 us	0.20 us	-1.914	-0.940	-0.910

Table 2 : Output of the AD9500(B) in the circuit of the fig. 14

It can be concluded from the readings in the Table 1 and the Table 2 that it is possible to change the pulse repetition rate at the output of the AD9500 by a corresponding change at the digital input.

In the circuit of the Fig. 14, by changing R_D or C_D or both, it is possible to have variation in the pulse width of the output (i.e with the increase in R_D or C_D ,

the pulse width increases and viceversa). This is the control over the duty cycle of the output. There is one more efficient way to achieve an effective control over the duty cycle. This is achieved by using the outputs Q_A and Q_B of the circuit in the Fig. 14, to drive the RESET and the SET inputs of a (RS)flipflop. The block diagram and the output of that circuit is shown in the Fig. 19.

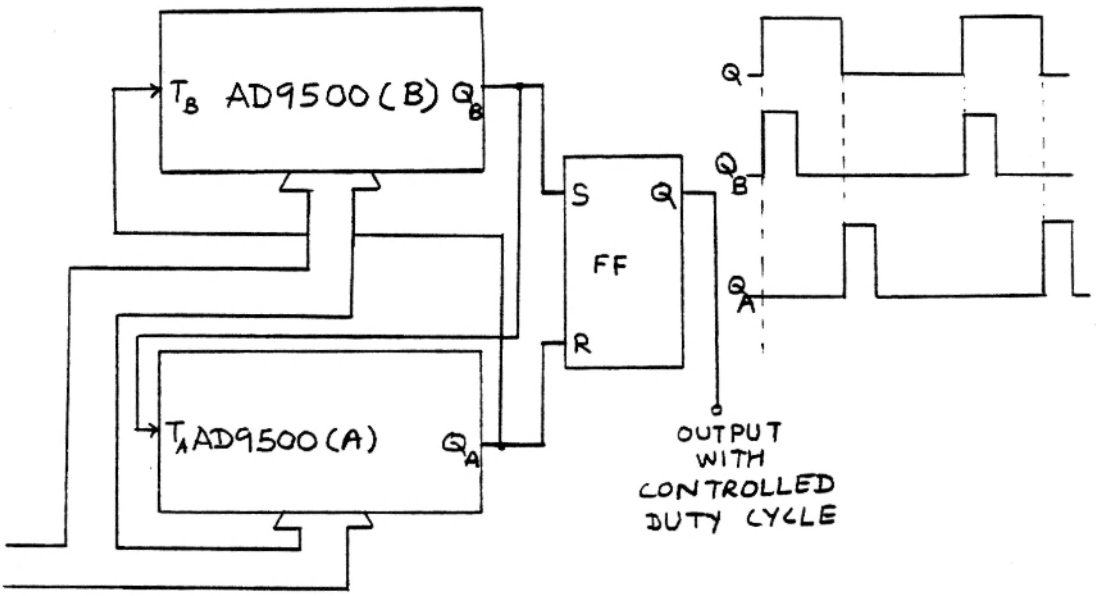


Fig. 19 Controlled duty cycle using a RS-flipflop

[Note:- By applying a positive(@5.0V) voltage at the ECL COMMON pin of the AD9500, the output pulses at Q_A and Q_B can be shifted above the ground level]

The output at Q in the Fig. 19 is the required output with the controlled duty cycle. Moreover, by simply changing the digital input to both the AD9500s, the frequency of the output pulses(Q_A and Q_B) can be

controlled, and hence the frequency of the output at Q, in the Fig. 19. Hence, an effective control over the output frequency and the duty cycle is possible.

4.4 Difficulties:

From the results in the table-1 and the table-2, it is obvious that the AD9500 was not able to output a good pulse train for a digital input between 0000 0000 to 0000 1100. For these inputs, it was possible to get output pulses , BUT, all the pulses were associated with constant high frequency oscillations. All the pulses were following the change in the digital input and the pulse repetition rate was also changing accordingly. Different values of R_{SET} , C_{EXT} and by-pass capacitors (associated with $+V_S$ and $-V_S$) were tried, with the above range of the digital inputs, but the output pulses were always associated with constant oscillations. Digital inputs of the TTL levels, using a MUX , were also tried, but the output was not changed.

Finally, it was found that by reducing the values of R_1 , in the circuit of the Fig. 14, it was possible to get a good output pulse train for some of the digital inputs of the above mentioned range, but not all. Too much reduction in the value of R_1 is not desirable as it can damage the output section of the AD9500 and also the -2.6 Volts regulator was getting

extremely hot due to the reduction in R_1 .

These problems were discussed with the application engineer of the AD9500 and some of them were answered. They are discussed in the Appendix-B.

5.0 Conclusions:

The digitally programmable generator chip, the AD9500, by Analog Devices, was characterized and tested for the three types of configurations, as explained in the section 3.3. The ring oscillator configuration was chosen in the design of a timing control circuit, which can be used for the NBS Voltage Step Generator control unit.

Using the two AD9500s, a circuit was designed and tested to generate two output pulse trains, whose frequency can be controlled by the digital input to the system. From the results in the Table 1 and the Table 2, it was concluded that the output pulse repetition rate (i.e. the frequency) was controlled by the digital input to the two AD9500s. Also, an effective control over the duty cycle of the output is possible by using a RS-flipflop, as discussed in the section 4.3.1.

It was found that the system of the Fig. 14, was not able to generate a good output pulses for the digital inputs in the range from 0000 0000 to 0000 1100. The output, with the the digital inputs from the above range, was associated with the constant, high frequency oscillations. Inspite of a hard effort, these oscillations could not be eliminated from the output pulses. The application engineer for the AD9500 was

informed with the all detailed technical information, about the above mentioned problem.

Finally, in the AD9500 technical literature (published by the Analog Devices), some technical errors were found and they were discussed with the application engineer for the AD9500. The engineer acknowledged those errors and provided some useful information about the functioning of the AD9500.

6.0 References:

[1] H. K. Schoenwetter, D. R. Flach, T. M. Souders and B. A. Bell, "A precision Programmable Step Generator for Use in Automated Test Systems", National Bureau of Standards Technical Note 1230, December 1986.

[2] J. R. Andrews, B. A. Bell and E. E. Baldwin, "Reference Flat Pulse Generator", National Bureau of Standards Technical Note, October 1983.

[3] "Digitally Programmable Delay Generator", A Technical Literature by Analog Devices.

[4] "Monolithic Digitally Programmable Delay Generator", Analog Dialogue, Volume 22, November 1, 1988, p. 14-15.

[5] Voltage Regulator Handbook, 1980, p.10-60 to 10-64 and p.10-78 to 10-85, National Semiconductor Corporation, Santa Clara, California 95051.

[6] The TTL Data book, Volume 2, 1985, Texas Instruments, Dallas, Texas 75265.

APPENDIX-A

Specifications of the AD9500

Digitally Programmable Delay Generator

FEATURES
- 10ps Delay Resolution
- 2.5ns to 100μs+ Full-Scale Range
- Fully Differential Inputs
- Separate Trigger and Reset Inputs
- Low Power Dissipation – 310mW

APPLICATIONS
- ATE
- Pulse Deskewing
- Arbitrary Waveform Generators
- High-Stability Timing Source
- Multiple Phase Clock Generators

GENERAL DESCRIPTION

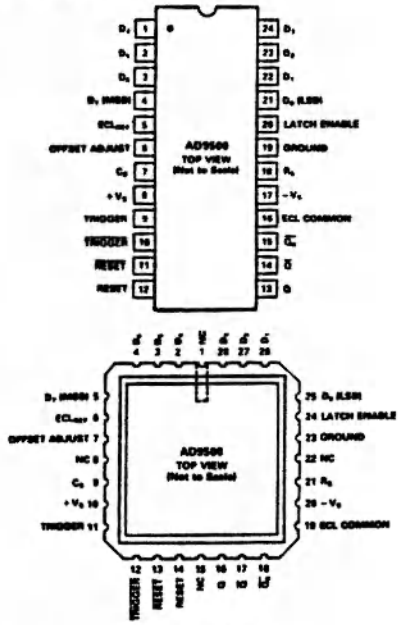
The AD9500 is a digitally programmable delay generator, which provides programmed delays, selected through an 8-bit digital code, in resolutions as small as 10ps. The AD9500 is constructed in a high-performance bipolar process, designed to provide high-speed operation for both digital and analog circuits.

The AD9500 employs differential TRIGGER and RESET inputs which are designed primarily for ECL signal levels but function with analog and TTL input levels. An on-board ECL reference midpoint allows both of the inputs to be driven by either single ended or differential ECL circuits. The AD9500 output is a complementary ECL stage, which also provides a parallel $\overline{Q_R}$ output circuit to facilitate reset timing implementations.

The digital control data is passed to the AD9500 through a transparent latch controlled by the LATCH ENABLE signal. In the transparent mode, the internal DAC of the AD9500 will attempt to follow changes at the inputs. The LATCH ENABLE is otherwise used to strobe the digital data into the AD9500 latches.

The AD9500 is available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both grades are packaged in a 24-pin ceramic "Skinny" DIP (0.3" package width), as well as 28-pin surface mount packages. Contact the factory for MIL-STD-883, revision C, qualified devices.

PIN CONFIGURATIONS



ORDERING INFORMATION

Device	Temperature Range	Description	Price (100s)
AD9500BP	−25°C to +85°C	28-Pin PLCC (Plastic), Industrial Temperature	$16.50
AD9500BQ	−25°C to +85°C	24-Pin "Skinny" DIP, Industrial Temperature	$16.00
AD9500TE	−55°C to +125°C	28-Pin LCC, Extended Temperature	$40.00
AD9500TQ	−55°C to +125°C	24-Pin "Skinny" DIP, Extended Temperature	$36.00

One Technology Way; P. O. Box 9106; Norwood, MA 02062-9106
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 714/641-9391 Midwest 312/980-0300 Texas 214/231-5094

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$)	+7V
Negative Supply Voltage ($-V_S$)	−7V
ECL COMMON to Ground Differential	−2.0V to +5.0V
Digital Input Voltage Range	−3.5V to +5.0V
Trigger/Reset Input Voltage Range	±5.0V
Trigger/Reset Differential Voltage	5.0V
Minimum R_{SET}	220Ω
Digital Output Current (Q and $\overline{Q}$)	30mA
Digital Output Current ($\overline{Q_R}$)	2mA
Offset Adjust Current (Sinking)	4mA
Power Dissipation (+25°C Free Air)[2]	2.62W
Operating Temperature Range	
AD9500BP/BQ	−25°C to +85°C
AD9500TE/TQ	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+175°C
Lead Soldering Temperature (10sec)	+300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages $+V_S = +5.0V$, $-V_S = -5.2V$; $C_{EXT} = 0pF$; $R_{SET} = 500\Omega$, unless otherwise stated)

Parameter	Mil[3] Sub Group	Temp	Industrial −25°C to +85°C AD9500BP/BQ Min	Typ	Max	Military −55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
RESOLUTION			8			8			Bits
ACCURACY[4]									
Differential Linearity	7	+25°C			0.5			0.5	LSB
Integral Linearity	7	+25°C			1.0			1.0	LSB
Monotonicity	7	+25°C		Guaranteed			Guaranteed		
DIGITAL INPUT									
Logic "1" Voltage	7, 8	Full	2.0←			2.0			V
Logic "0" Voltage	7, 8	Full			0.8←			0.8	V
Logic "1" Current	1, 2, 3	Full			5			5	µA
Logic "0" Current	1, 2, 3	Full			5			5	µA
Digital Input Capacitance	12	+25°C			5.5			5.5	pF
Data Setup Time[5]	12	+25°C		0.4	0.75		0.4	0.75	ns
Data Hold Time[6]	12	+25°C		0.4	0.75		0.4	0.75	ns
Latch Pulse Width (t_{LPW})	12	+25°C	3.0			3.0			ns
RESET/TRIGGER INPUTS[7]									
TRIGGER Input Voltage Range		Full		−2.5; 4.5			−2.5; 4.5		V
RESET Input Voltage Range		Full		−2.5; 2.0			−2.5; 2.0		V
Differential Switching Voltage	7, 8	Full		40	300		40	300	mV
Input Bias Current	1	+25°C		40	50		40	50	µA
	2, 3	Full			75			75	µA
Input Resistance		+25°C		4			4		kΩ
Input Capacitance	12	+25°C		6.5	7.25		6.5	7.25	pF
Minimum Input Pulse Width (t_{TPW}, t_{RPW})		+25°C		2.0			2.0		ns
DYNAMIC PERFORMANCE[8]									
Maximum Trigger Rate	12	+25°C	100			100			MHz
Minimum Propagation Delay (t_{PD})[9]	4	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Minimum Propagation Delay TC[10]		Full		7.5			7.5		ps/°C
Full-Scale Range TC		Full		0.5			0.5		ps/°C
Delay Uncertainty (Jitter)		+25°C		10			10		ps
Reset Propagation Delay (t_{RD})[11]	4	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Reset-to-Trigger Holdoff (t_{THO})[12]	4	+25°C	0.2	0		0.2	0		ns
Trigger-to-Reset Holdoff (t_{RHO})[13]	4	+25°C	2.0	1.5		2.0	1.5		ns
Minimum Output Pulse Width		+25°C		3.3			3.3		ns
Output Rise Time	12	+25°C			2.0			2.0	ns
Output Fall Time	12	+25°C			2.0			2.0	ns
Delay Coefficient Settling Time (t_{DAC})[14]		+25°C		29			29		ns
Linear Ramp Settling Time (t_{LRS})		+25°C		22			22		ns

Parameter	Mil[3] Sub Group	Temp	Industrial −25°C to +85°C AD9500BP/BQ Min	Typ	Max	Military −55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
SUPPORT FUNCTIONS									
ECL_{REF}	1	+25°C	−1.4	−1.3	−1.2	−1.4	−1.3	−1.2	V
ECL_{REF} Voltage Drift[15]		Full		1.1			1.1		mV/°C
Offset Adjust Range		Full		−2			−2		mA
DIGITAL OUTPUTS[8]									
Logic "1" Voltage	1, 2, 3	Full	−1.1			−1.1			V
Logic "0" Voltage	1, 2, 3	Full			−1.5			−1.5	V
POWER SUPPLY[16]									
Positive Supply Current (+5.0V)	1	+25°C		24	28		24	28	mA
	2, 3	Full			30			30	mA
Negative Supply Current (−5.2V)	1	+25°C		37	42		37	42	mA
	2, 3	Full			44			44	mA
Nominal Power Dissipation		+25°C		312			312		mW
Power Supply Rejection Ratio[17]									
Full-Scale Range Sensitivity	7	+25°C		70	300		70	300	ps/V
Minimum Propagation Delay Sensitivity	7	+25°		150	500		150	500	ps/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance

24-Pin Ceramic $\theta_{JA} = 56°C/W$; $\theta_{JC} = 16°C/W$

28-Pin PLCC (Plastic) $\theta_{JA} = 60°C/W$; $\theta_{JC} = 22°C/W$

28-Pin Ceramic LCC $\theta_{JA} = 69°C/W$; $\theta_{JC} = 25°C/W$

[3]Military subgroups apply to military qualified devices only.

[4]R_{SET} = 10kΩ. (Full-scale delay = 100ns).

[5]The digital data inputs must remain stable for the specified time prior to the LATCH ENABLE signal.

[6]The digital data inputs must remain stable for the specified time after the LATCH ENABLE signal.

[7]The TRIGGER and RESET inputs are differential and must be driven relative to one another. Both of these inputs are ECL compatible, but can also be used with TTL logic families in a limited fashion.

[8]Outputs terminated through 50Ω resistors to −2.0V.

[9]Program Delay = 0.0ps (Digital Data = 00_H). In Operation, any programmed delays are in addition to the Minimum Propagation Delay.

[10]Measured from the 50% transition point of the reset signal input, to the 50% transition point of the resetting output.

[11]Minimum time from falling edge of RESET to triggering input, to insure a valid output event.

[12]Change in total delay through AD9500, exclusive of changes in minimum-propagation delay t_{PD}.

[13]Minimum time from triggering event to rising edge of RESET, to insure a valid output event.

[14]Measured from the LATCH ENABLE input to the point when the AD9500 becomes 8-bit accurate again, after a full-scale change in the programmed delay.

[15]Standard 10K and 10KH ECL families operate with a 1.1mV/°C drift by design.

[16]Supply voltages should remain stable within ±5% for normal operation.

[17]Measured at ±5% of $-V_S$ and $+V_S$.

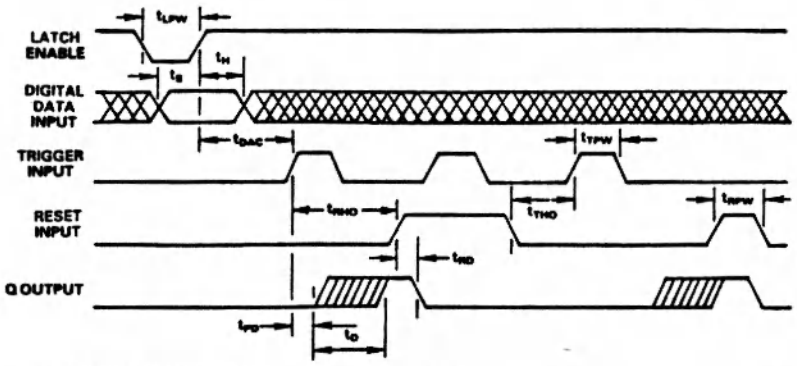
Specifications subject to change without notice.

EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated operating temp.
Subgroup 3 – Static tests at min rated operating temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated operating temp.
Subgroup 6 – Dynamic tests at min rated operating temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated operating temp.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated operating temp.
Subgroup 11 – Switching tests at min rated operating temp.
Subgroup 12 – Periodically sample tested.

FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
D_6–D_0	– One of eight digital inputs used to set the programmed delay.
D_7(MSB)	– One of eight digital inputs used to set the programmed delay. D_7 (MSB) is the most significant bit of the digital input word.
ECL_{REF}	– ECL midpoint reference, nominally −1.3V. Use of the ECL_{REF}, allows either of the TRIGGER or the RESET inputs to be configured for single-ended ECL inputs.
OFFSET ADJUST	– The OFFSET ADJUST is used to adjust the minimum propagation delay (t_{PD}), by pulling or pushing a small current out of or into the pin.
C_S	– C_S allows the full-scale range to be extended by using an external timing capacitor. The value of C_{EXT}, connected between C_S and $+V_S$, may range from 0pF to 0.1μF+. See R_S ($C_{INTERNAL}$ = 10pF).
$+V_S$	– Positive supply terminal, nominally +5.0V.
TRIGGER	– Noninverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The TRIGGER input must be driven in conjunction with the $\overline{\text{TRIGGER}}$ input.
$\overline{\text{TRIGGER}}$	– Inverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The $\overline{\text{TRIGGER}}$ input must be driven in conjunction with the TRIGGER input.
$\overline{\text{RESET}}$	– Inverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The RESET input must be driven in conjunction with the $\overline{\text{RESET}}$ input.
RESET	– Noninverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The $\overline{\text{RESET}}$ input must be driven in conjunction with the RESET input.
Q	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic HIGH on the Q output. A "resetting" event at the inputs will produce a logic LOW on the Q output
$\overline{Q}$	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q}$ output.
$\overline{Q_R}$	– $\overline{Q_R}$ output is parallel to the $\overline{Q}$ output. The $\overline{Q_R}$ output is typically used to drive delaying circuits for extending output pulse widths. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q_R}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q_R}$ output.
ECL COMMON	– The collector common for the ECL output stage. The collector common may be tied to +5.0V, but normally it is tied to the circuit ground for standard ECL outputs.
$-V_S$	– Negative supply terminal, nominally −5.2V.
R_S	– R_S is the reference current setting terminal. An external setting resistor, R_{SET}, connected between R_S and $-V_S$ determines the internal reference current. See C_S ($250\Omega \leq R_{SET} \leq 50k\Omega$).
GROUND	– The ground return for the TTL and analog inputs.
LATCH ENABLE	– Transparent TTL latch control line. A logic HIGH on the LATCH ENABLE freezes the digital code at the logic inputs. A logic LOW on the LATCH ENABLE allows the internal current levels to be continuously updated through the logic inputs D_0 thru D_7.
D_0(LSB)	– One of eight digital inputs used to set the programmed delay. D_0 (LSB) is the least significant bit of the digital input word.
D_3–D_1	– One of eight digital inputs used to set the programmed delay.

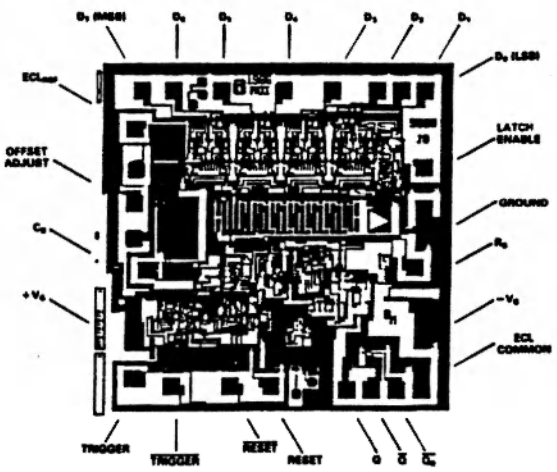


t_S – DIGITAL DATA SETUP TIME
t_H – DIGITAL DATA HOLD TIME
t_{LPW} – LATCH ENABLE PULSE WIDTH
t_{DAC} – INTERNAL DAC SETTLING TIME
t_{PD} – MINIMUM PROPAGATION DELAY
t_{RD} – RESET PROPAGATION DELAY
t_D – PROGRAMMED DELAY
t_{TPW} – TRIGGER PULSE WIDTH
t_{RPW} – RESET PULSE WIDTH
t_{THO} – RESET-TO-TRIGGER HOLDOFF
t_{RHO} – TRIGGER-TO-RESET HOLDOFF

NOTE
A TRIGGERING EVENT MAY OCCUR AT ANY TIME WHILE THE INTERNAL DAC (PROGRAMMED DELAY) IS BEING CHANGED. TRIGGERING EVENTS DURING THE INTERNAL DAC SETTLING TIME MAY NOT GENERATE AN ACCURATE PULSE DELAY.

System Timing Diagram

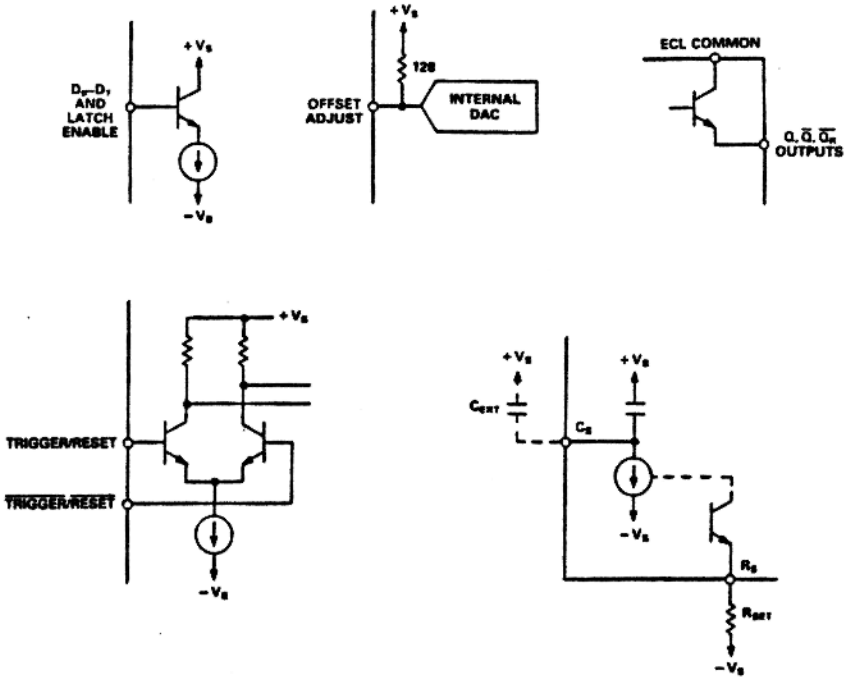
DIE LAYOUT



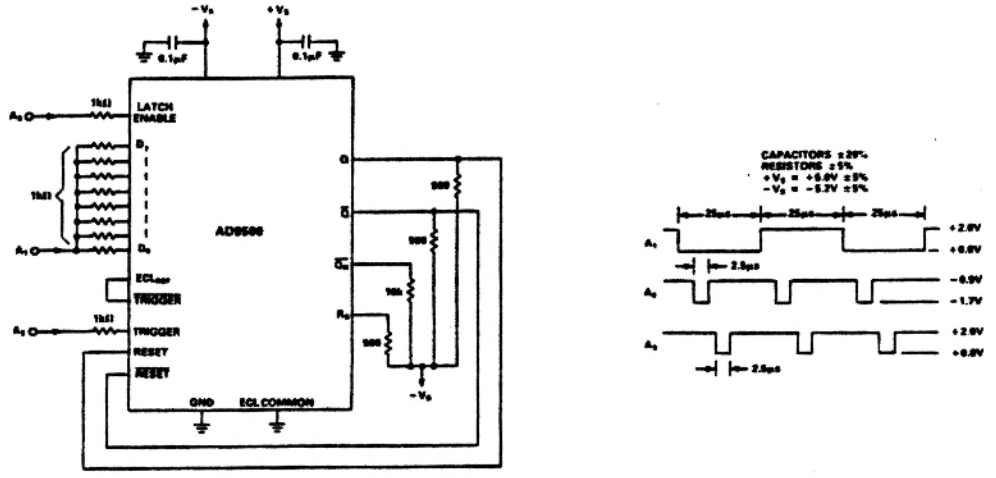
MECHANICAL INFORMATION

Die Dimensions	104 × 103 × 18 (max) mils
Pad Dimensions	4 × 4 (min)mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold; Gold Ball Bonding

Input/Output Circuits



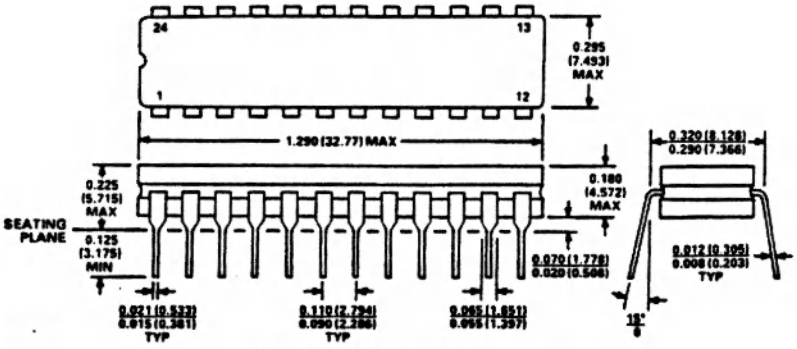
Burn-In Circuit



OUTLINE DIMENSIONS

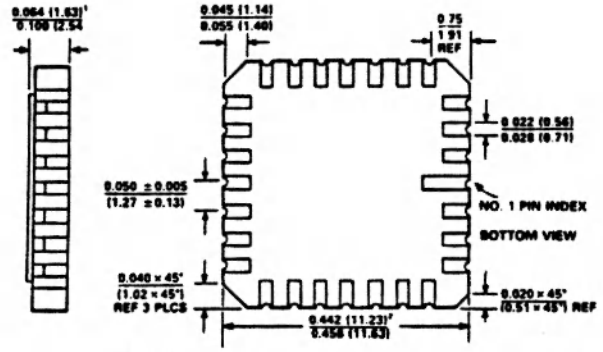
Dimensions shown in inches and (mm).

24-Pin Ceramic "Skinny" DIP



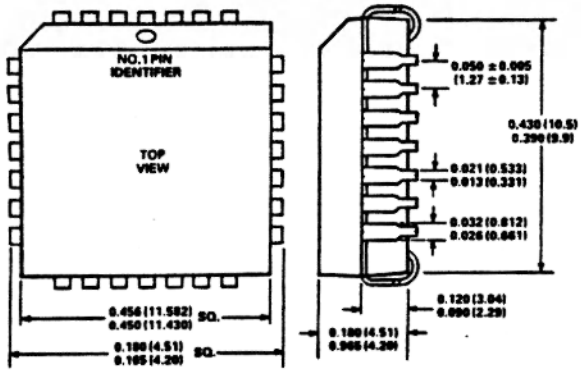
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Pin LCC



NOTES
1. THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2. APPLIES TO ALL FOUR SIDES.
3. ALL TERMINALS ARE GOLD PLATED.

28-Pin PLCC



APPENDIX-B

Discussion with the Application Engineer of the AD9500

APPENDIX-B

Discussion with the Application Engineer of the AD9500

The digitally programmable delay generator chip AD9500, was successfully used in the circuit, to generate the output pulse train. The frequency of the output pulse train was controlled by the digital input to the AD9500.

During the phase of testing the AD9500 for the different configurations (section 3.3 of this report) and testing the circuit which can be used as a part of the NBS Voltage Step Generator control unit (section 4.0 of this report), there were instances where the functioning of the AD9500 was doubted. All the questions and doubts concerning the AD9500 were discussed with Mr. Jim Surber, Marketing(Application) Engineer at the Analog Devices, on the phone as well as on paper(mail). [Mr. Jim Surber, Marketing Engineer, Computer Labs Division, 7910 Triad Center Drive, Greensboro, NC 27409-9605; Phone:(919) 668-9511]

Some corrections were suggested for the technical literature for the AD9500, published by the Analog Devices (reference [3]). They are as follows:

* The literature should specify which configuration of the AD9500 is used for the electrical characteristic table.

* It does not clearly indicate whether the ECL_{REF}

is an output pin or an input pin. In reality, it is an output of -1.3 volts D.C.

* Actually, the AD9500 has 8-bit digital input but in all the diagrams, in the literature, it is shown as D0 to D8! (i.e 9-bit input !)

* During the discussion of the ring oscillator, in the literature, it is shown that two pulse trains are produced at the OUTPUT and $\overline{\text{OUTPUT}}$ (corresponding to Q_A and Q_B of Fig. 14), but in reality both are OUTPUT. There cannot be $\overline{\text{OUTPUT}}$ in that diagram.

* In the graph of "some typical programmed delay ranges" (Fig. 7 of this report), it is not stated what is the corresponding digital input for the all delays shown on that graph. Actually those delays correspond to the digital input of 255 or $FF(hex).

There were some technical questions concerning the AD9500; and they are as follows:

* The first time the minimum configuratir (section 3.3.1) was tested, with a digital input = 00; a programmed delay of @ 30 ns was produced which is not logical. This was referred to Mr. Surber and he suggested not to use the OFFSET ADJUST pin in that configuration, as it is used while extending the full scale delay only. The reading for the programmed delay were taken again, without any connection to the OFFSET ADJUST pin, and a delay of @ 8 ns was obtained which is correct and was confirmed with Mr. Surber.

* Fig. 11 of this report, shows that the output pulse width reduces with the increase in the digital input. Why? No satisfactory answer yet!

* It was found that in the ring oscillator configuration (circuit in the Fig. 14 of this report), the AD9500 was unable to work satisfactorily when a digital input of 0000 1100 or less is applied. The output pulse train with this inputs, was associated with the constant, high frequency oscillations. Why? No satisfactory answer yet!

* In the calculation of the Reset Time (page 20 of this report), the following expression was used:

$$\text{Reset Time} = t_{RD} + (R_D\ C_D\ /1.85)$$

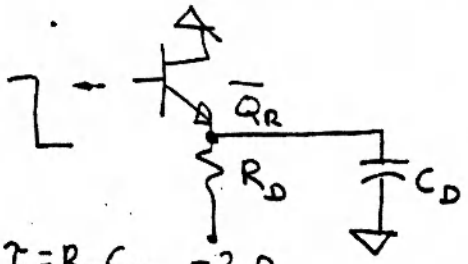
Why the term "$(R_D\ C_D\ /1.85)$" is used as the RC-time constant? A copy of the answer provided by Mr. Surber, is attached at the end of this Appendix.

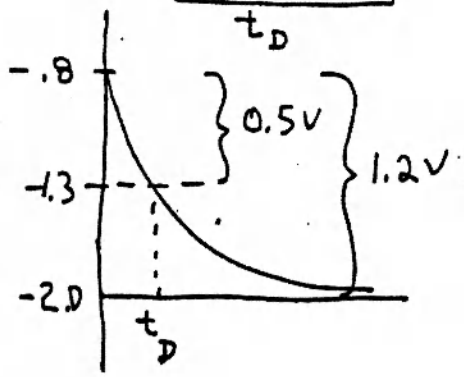
Mr. Surber was called quite frequently, for the above problems and he has been extremely helpful in providing the required information. He was very happy with the results and the technical information sent to him, regarding the above problems. He also suggested that, it is important to have the test circuit built up on a circuit board with a low impedance ground plane and all ground pin connections should be tied to the common ground plane as well as a ground connection for each power supply. Unfortunately, due to the time constraint, all the questions regarding the functioning of the AD9500, were not answered completely.

AD-9500 - Use of $\overline{Q_R}$ 10-24-08

Formula in data sheet is (p.8)

$$\text{RESET TIME} = t_{RD} + \underbrace{\frac{1}{8} \cdot R_D C_D}_{t_D}$$





$$1 - e^{-t_D/\tau} = \frac{0.5}{1.2} = 0.4166$$

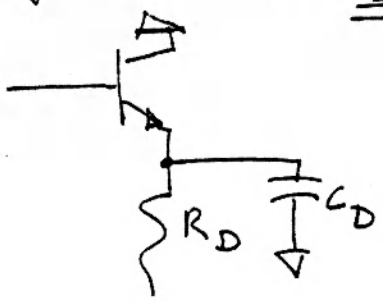
$$e^{-t_D/\tau} = .5833$$

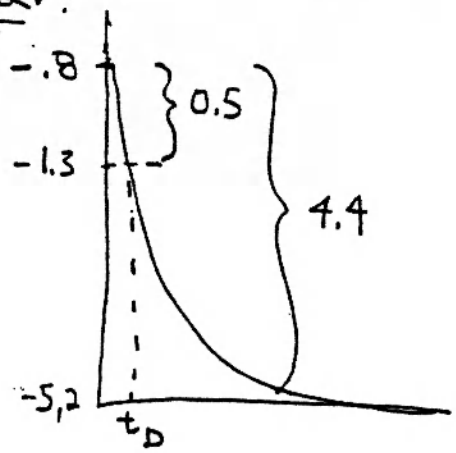
$$-t_D/\tau = -.54,$$

$$\boxed{t_D = .54\,\tau}$$

↓ CORRECT FOR -2.0 V Termination

If terminated to -5.2V:





$$1 - e^{-t_D/\tau} = \frac{0.5}{4.4} = .1136$$

$$e^{-t_D/\tau} = .8864$$

$$-t_D/\tau = -.121$$

$$\boxed{t_D = 0.121\,\tau \approx \tau/8}$$

∴ Formula in data sheet assumes -5.2V termination

DIGITALLY PROGRAMMABLE DELAY GENERATOR

by

MAULIN I. PATEL

B.S., Sardar Patel University, Gujarat, India, 1985

AN ABSTRACT OF A MASTER'S REPORT

submitted in partial fulfillment of the

requirements for the degree

MASTER OF SCIENCE

Department of Electrical and Computer Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

1989

ABSTRACT

A Voltage Step Generator(VSG) was designed and developed at the National Bureau of Standards(NBS). The VSG was designed to output programmable pulses. An attempt was made to redesign the timing circuit of the control unit of the VSG, to achieve the same goals, but with different hardware configuration. The digitally programmable delay generator chip, AD9500 of the Analog Devices was used for the above purpose.

The AD9500 was characterized and tested for all the possible configurations. The ring oscillator configuration was chosen for the design of the timing circuit. The circuit was built and tested using the AD9500 and the results were recorded. There were some difficulties due to improper behavior of the AD9500. The application engineer at the Analog Devices was asked questions concerning the functioning of the AD9500.