A 2.4 GHZ RECEIVER IN SILICON-ON-SAPPHIRE

by

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Abstract

From 2004 to 2008, Kansas State University's Electrical and Computer Engineering (ECE) department, along with the NASA Jet Propulsion Laboratory and Peregrine Semiconductor, researched design techniques for producing a low-power, 400 MHz micro-transceiver suitable for future use on Mars scout missions. In 2012, Dr. Kuhn's Digital Radio Hardware Design class, ECE765, adapted the K-State circuit designs from this research project to investigate the possibility of producing a 2.4 GHz micro-transceiver in Peregrine Semiconductor's newer 0.25 µm Silicon on Sapphire process.

This report expands upon the work completed in the Digital Radio Hardware Design (ECE765) course. The schematics and layout of the subsections of the receiver portion of the micro-transceiver chip, consisting of a transmit/receive switch, low-noise amplifier, mixer, intermediate-frequency amplifiers, and an analog-to-digital converter are described. Circuits designed to date require a total of 15 mW to operate. This report is intended as a guide for future students who will take over this project, make modifications, adapt the transmit portion of the micro-transceiver from previous work, and finish layout before fabrication of a full 2.4 GHz prototype chip.

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Introduction

This project will be fabricated using Peregrine Semiconductor's 0.25 μm GC process. This is a scaled-down version of the 0.5 μm FC commercial process used for the 400 MHz radio [1]. Parasitic capacitance is reduced in the GC process, and intrinsic threshold devices allow transistors to be cascoded on the lower 2.5 V supply, making it a good candidate for researching a 2.4 GHz transceiver design.

The block diagram of the transceiver chip in Figure 1 shows gain and impedances of the 2.4 GHz system. This report covers the section highlighted in red.
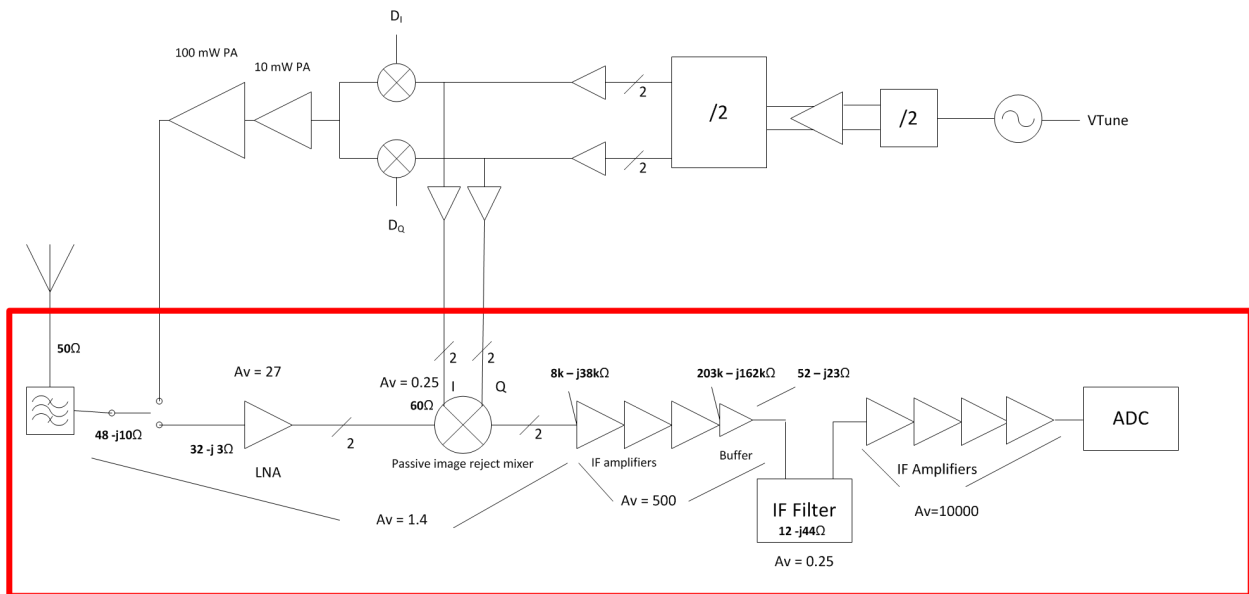
Figure 1: Block diagram of micro-transceiver

LNA and Transmit / Receive Switch

The LNA is preceded by a resonant transmit/receive switch intended to match the LNA's input impedance to 50 ohms in receive mode and to present a high impedance in transmit mode to ensure the transmitted signal reaches the antenna instead of the LNA. [1]

An inductively degenerated common-source, cascode architecture was used for the first stage of the LNA. The output node of this stage has programmable capacitance added in order to tune the resonant frequency. It is followed by a differential amplifier with one input shorted to ground through a capacitor to convert to a differential output. Figures 3, 6, and 8 show closer views of the LNA schematic.

20 dB of voltage gain is provided with a bandwidth of 180 MHz.

LNA
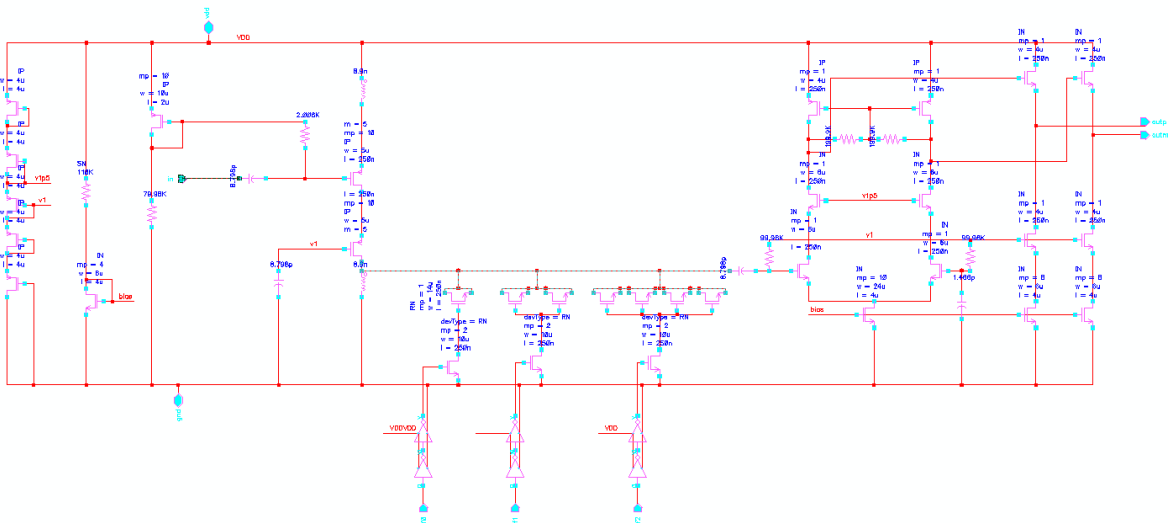
Figure 2: Schematic of LNA
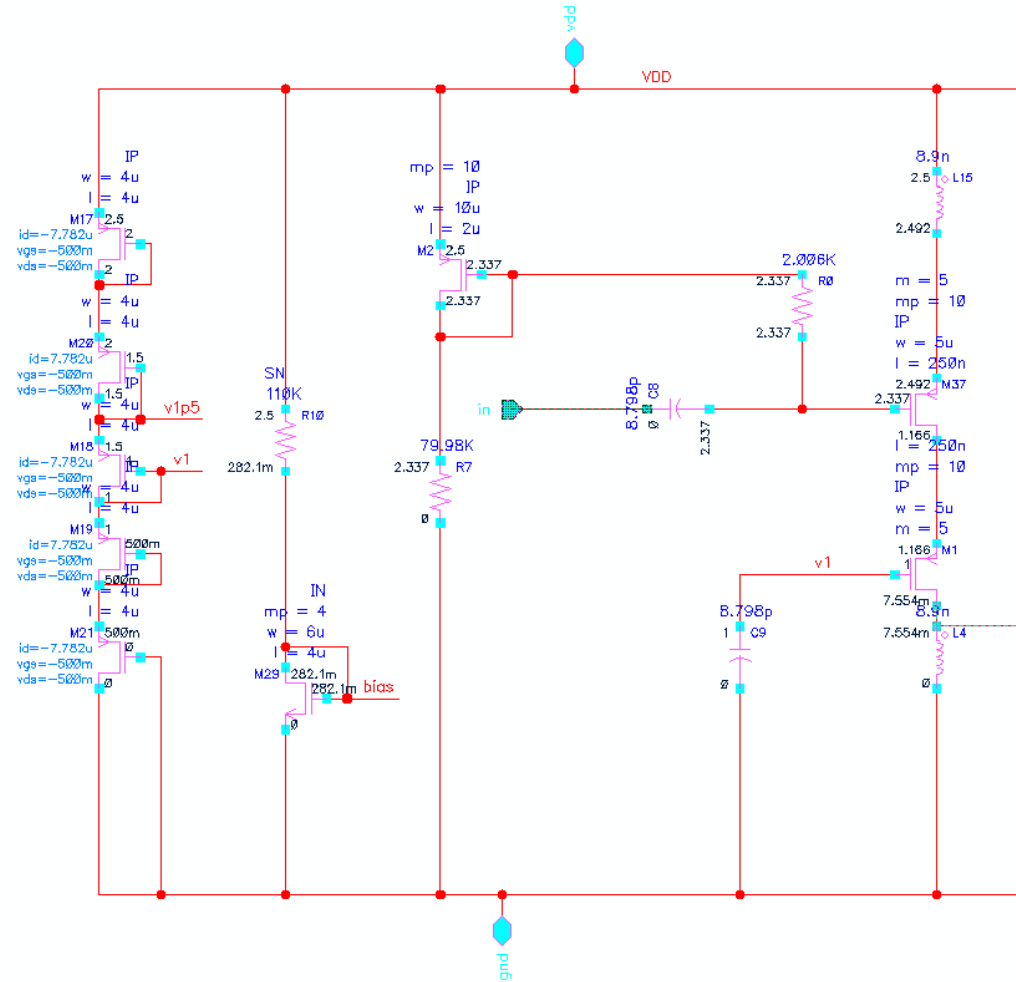
Figure 3: Schematic of common source, cascoded, input stage of the LNA

The input stage of the LNA is shown in Figure 3. Intrinsic PFETs were used instead of NFETs as a precaution in case signal is fed through during transmission. PFETs have a higher breakdown voltage in Peregrine Semiconductor's GC process. The DC bias simulation failed to converge from the extracted view. From simulation done from schematics, the two FETs are biased at 1.4 mA. Their overdrive voltage was set to roughly 100 mV to protect against process variations: The top PFET V_{gs} is 155 mV; the lower PFET V_{gs} is 165 mV.

The gain is approximately $-g_m$ (R || r_o), thus mainly dependent on the parallel equivalent impedance of the tank circuit at the drain of M1. This inductor had to be lowered to 9.8 nH after the tuning stage was added and parasitic capacitance was simulated in order to keep the frequency centered at 2.4 GHz.

The test bench in Figure 4 was used to simulate gain and tuning of the LNA unloaded. Voltage gain is 28.7 dB for the entire LNA at 2.4 GHz. Almost all of this is realized in the first stage. The voltage level at

the drain of transistor M1 is 24.5 times levels at the input. Bandwidth is 100 MHz with the LNA simulated alone.
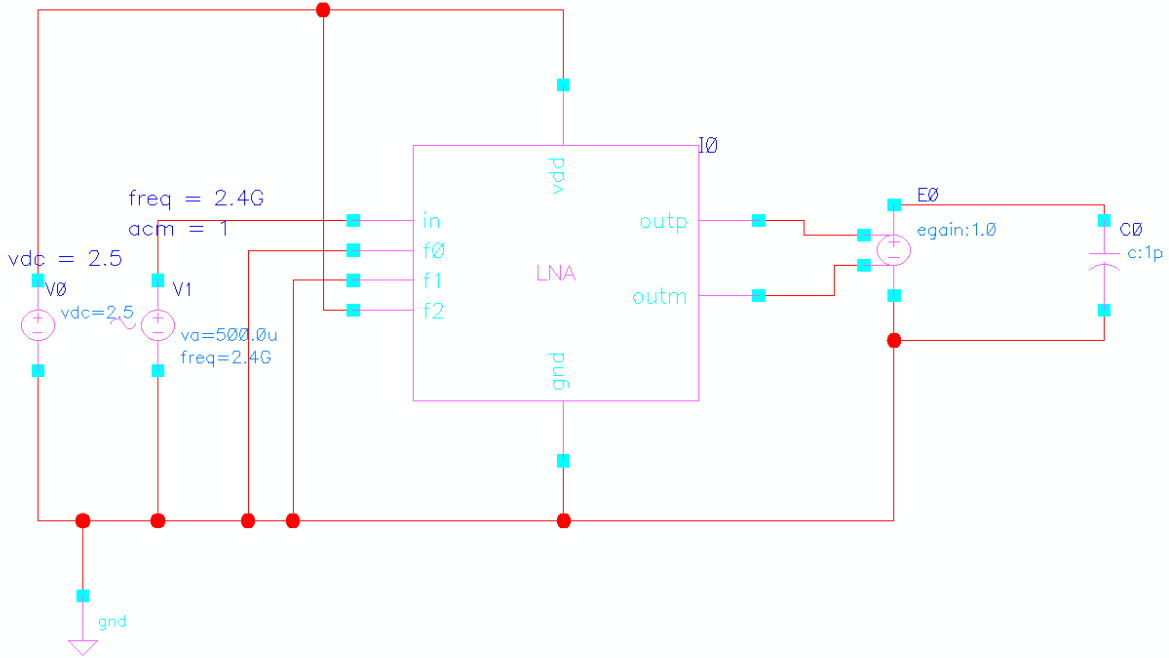
Figure 4: LNA AC test bench
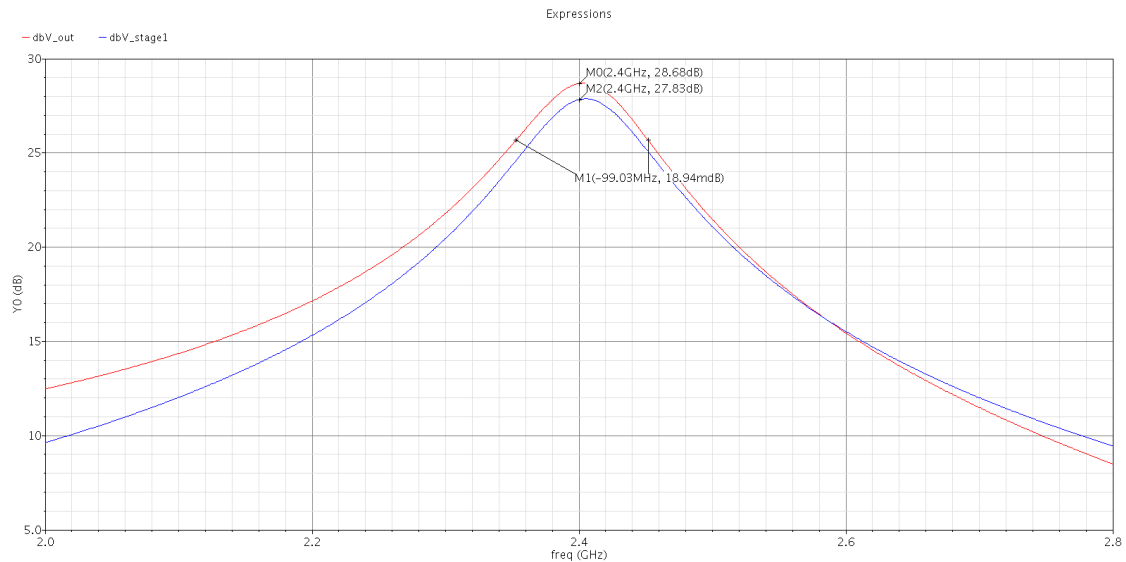
Figure 5: LNA AC simulation results of the voltage at the drain of M1 and the differential output

Simulated parasitic capacitance cannot be trusted to be completely accurate, so frequency tuning had to be added to the LNA. Transistors M50 to M56 in Figure 6 provide added capacitance for tuning. Replacing these with MIM capacitors would result in more reliable performance.

Tuning should be provided in eight steps of 90 MHz (half the bandwidth when simulated with the TR switch), however, this stage still needs more work. As currently laid out, the LNA's center frequency is tunable from 2.35 GHz to 2.52 GHz in steps of 20 to 30 MHz.
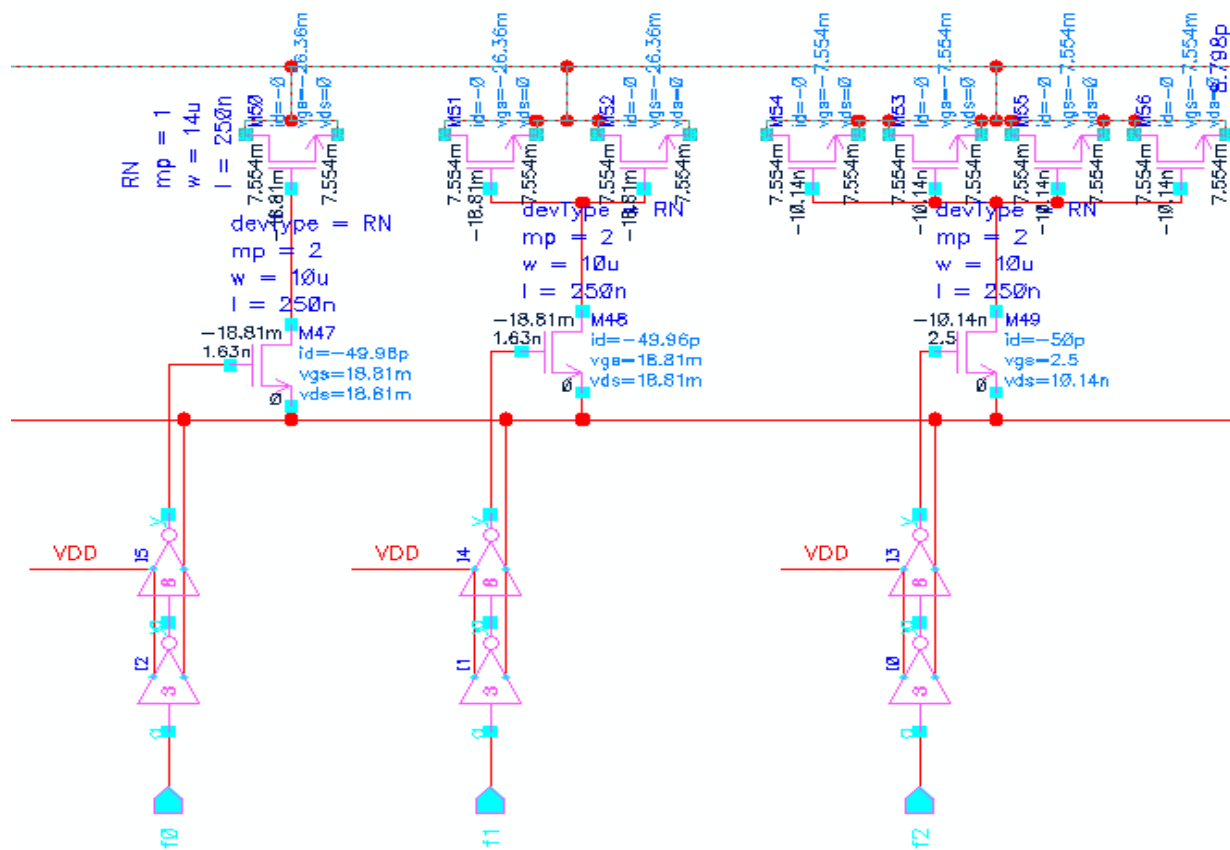
Figure 6: Schematic of LNA frequency tuning

In order to increase each tuning step's Q, a FET with W/L of 20µm / 250nm is switched by inverters INV3 and INV8. These PSC cells are designed for high fanout and provide smaller resistance than INV1. Total capacitance at the extracted output node was calculated to be about 400 fF before adding the tuning
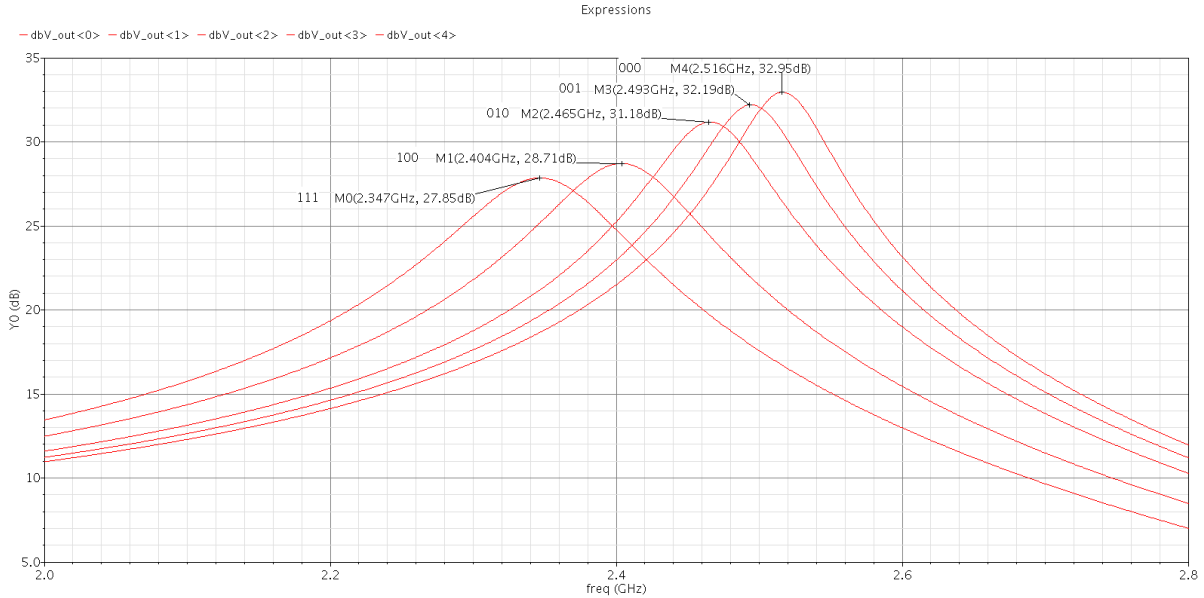
Figure 7: Differential output of LNA with various frequency tuning

stage. Resistance and capacitance from each leg were simulated from the schematic level. When switched on, each of the three legs has a resistance of 20 ohms and capacitances of 22 fF, 43 fF, and 86 fF, respectively. When switched off, the capacitances are 10 fF, 14 fF, and 17 fF.

The on-resistance needs to be decreased to prevent such a large reduction in gain as seen in Figure 7.

The differential amplifier in figure 8 converts the single ended output to differential for increased noise immunity for the rest of the circuit stages. Gain of 1 is provided. Each side of the differential pair is biased at 110 μA and the two common drain outputs are biased at 40 μA.

AC simulation with 1 A of current into the output node was used to measure output impedance as shown.

Z_{out} = 3.5 kΩ – j 1.9 kΩ

The output common drain FETs should be resized and rebiased to lower the output impedance to better match the mixer's input impedance.

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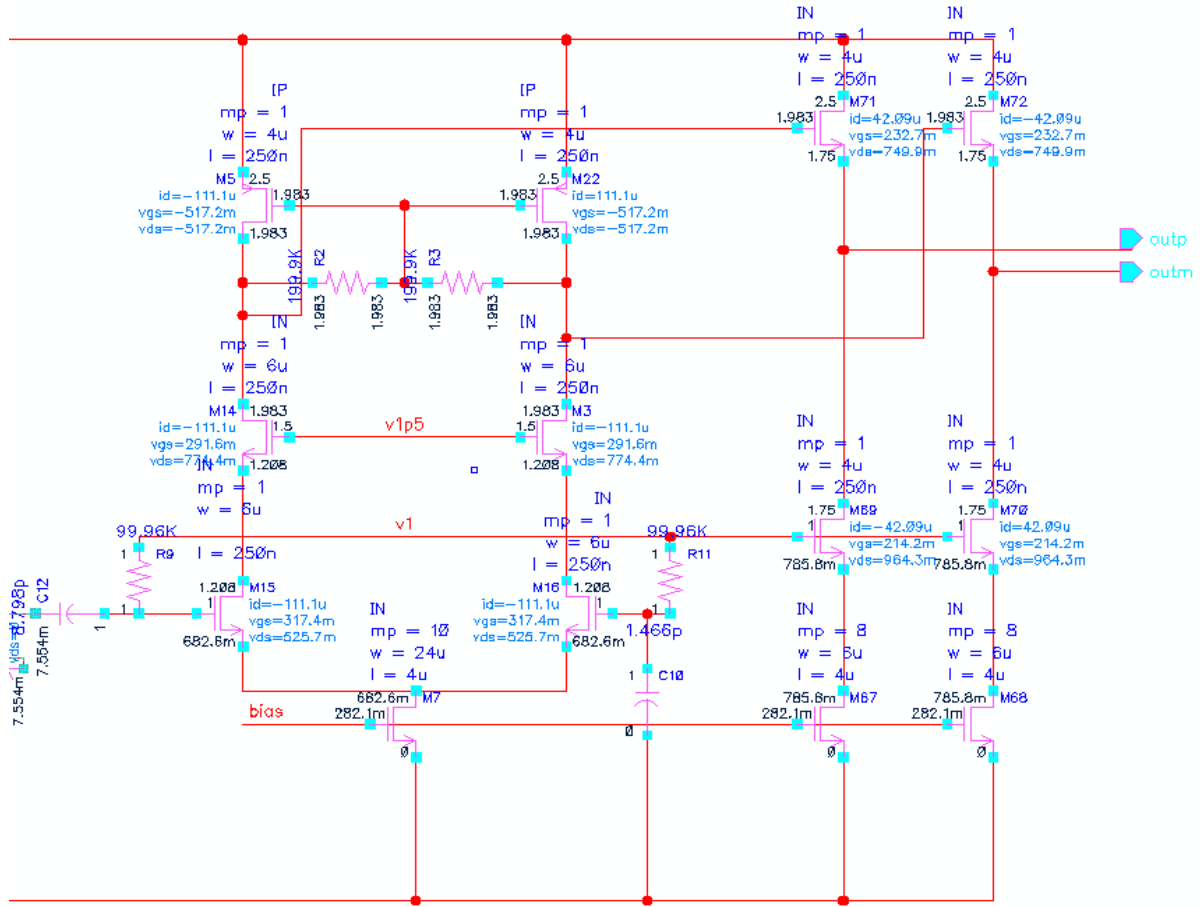
Figure 8: Schematic of single-to-differential stage of LNA
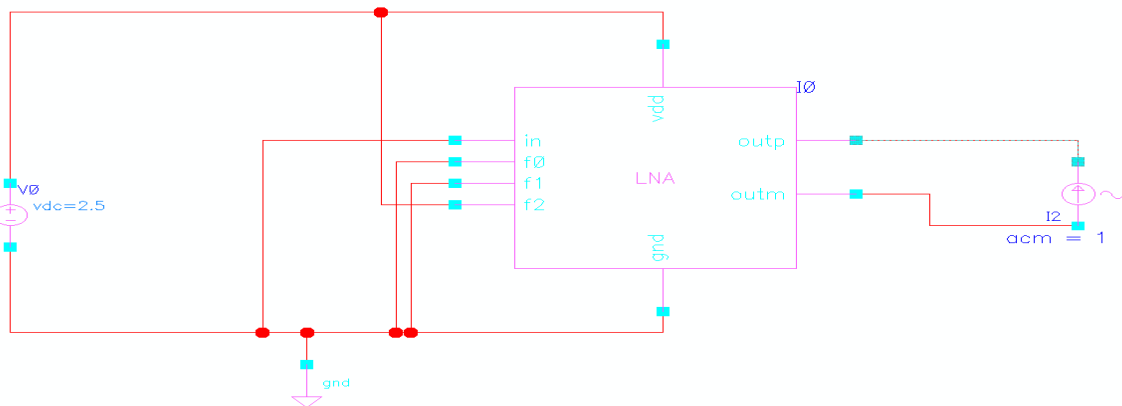
Figure 9: Test bench used to determine the LNA's output impedance
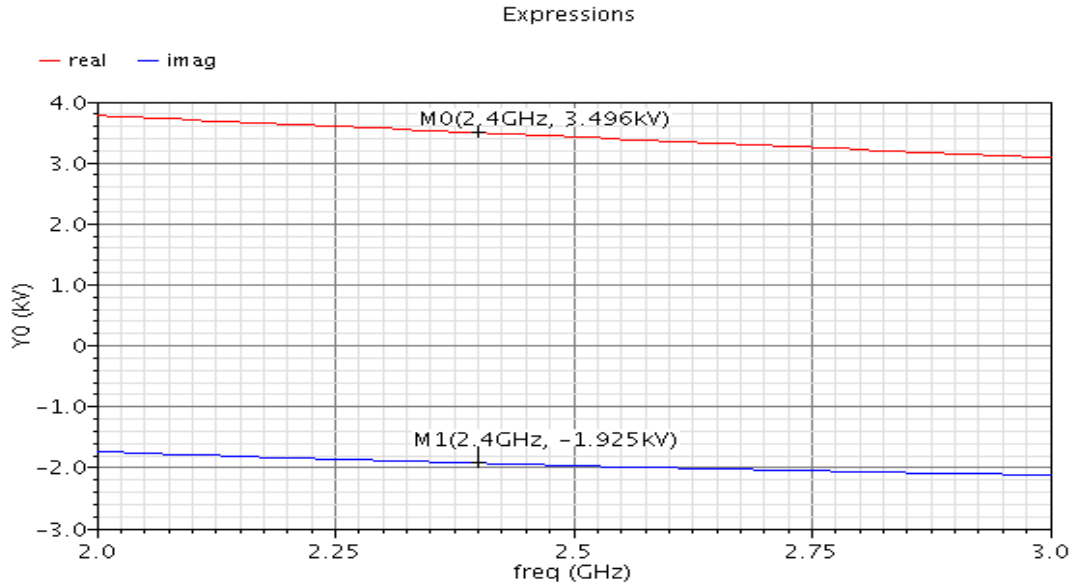
Figure 10: LNA output impedance: Plot of (V$_{outp}$ – V$_{outn}$) for 1A test current

Transmit / Receive Switch

The transmit/receive switch pin is pulled low for receive mode. This matches the input impedance to the antenna at 50 Ω. When pulled high, the switch should have very high impedance when looking from the antenna. A path to ground is also provided to protect the LNA from high voltage signals.
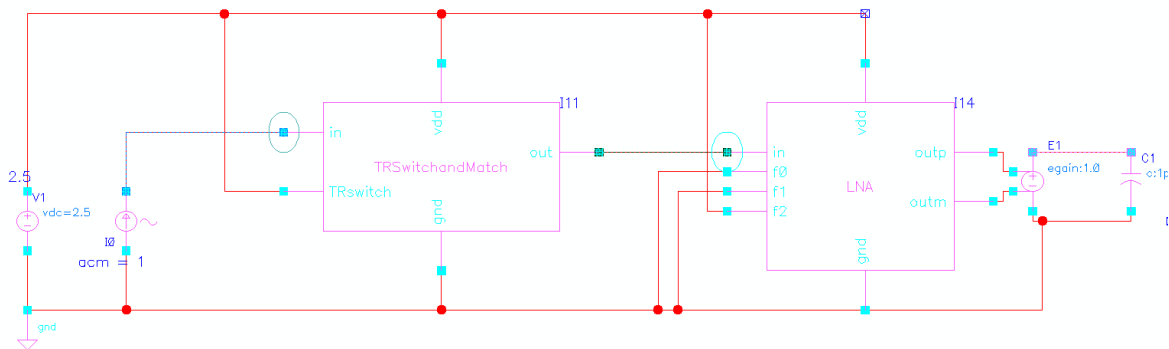
Figure 11: Test bench used to determine TR switch and LNA input impedance

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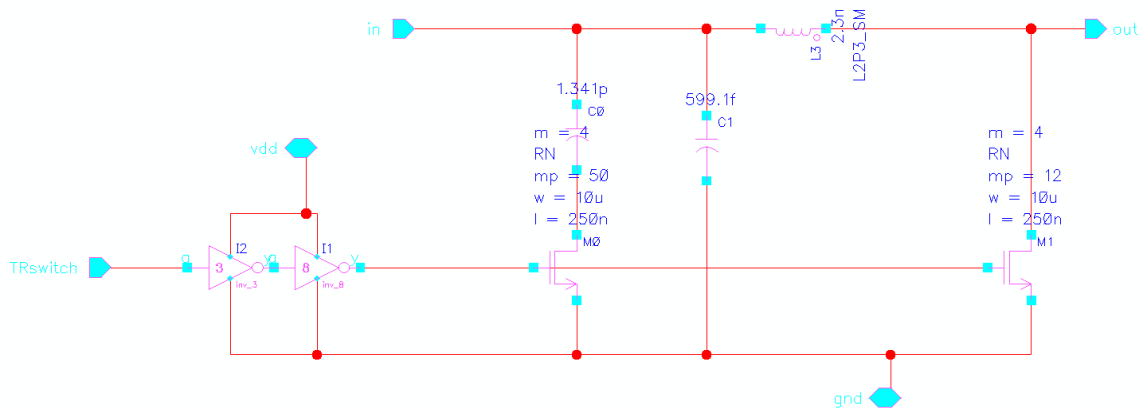
Figure 12: Schematic of TR switch

L3 and C1 provide matching to 50 Ω from the LNA in receive mode. When the TR switch pin is high, M0 and M1 are switched on. M0 is very large to provide a high Q for C0. From schematic level simulations, M0's on resistance is 1 Ω. M1's on resistance is 4Ω.
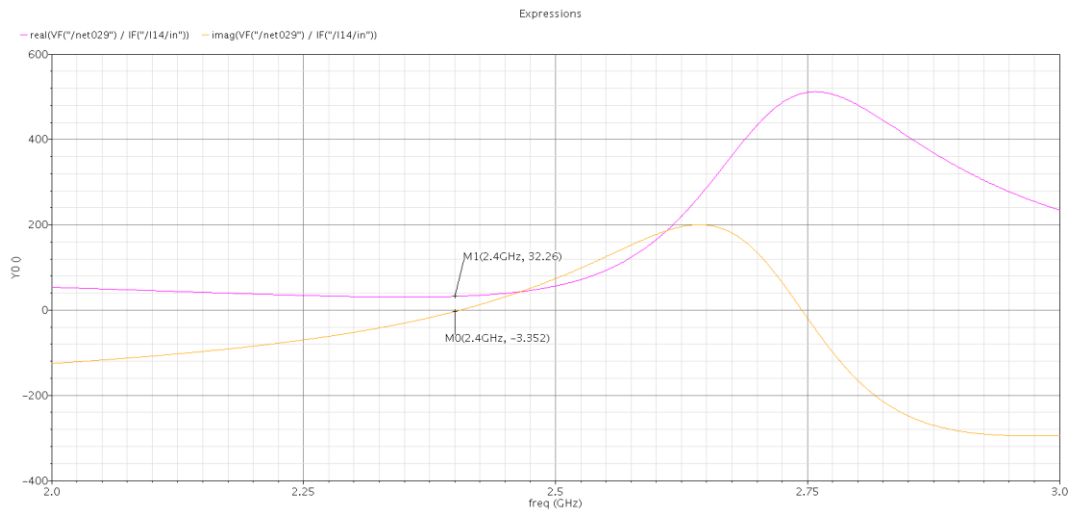
Figure 13: LNA block input impedance: 32 – j 3 Ω

The TR switch input impedance in transmit mode is 162 – j 10 Ω. This is not acceptable. This results in a reflection coefficient of 0.52 looking into the TR switch from the antenna. The input impedance of the LNA alone is 32 – j 3 Ω. The input impedance to the LNA needs to be increased by increasing the inductor at the source of M37 before the design is committed to fabrication. This will allow the inductor in the TR switch to be increased, resulting in a higher impedance in transmit mode.

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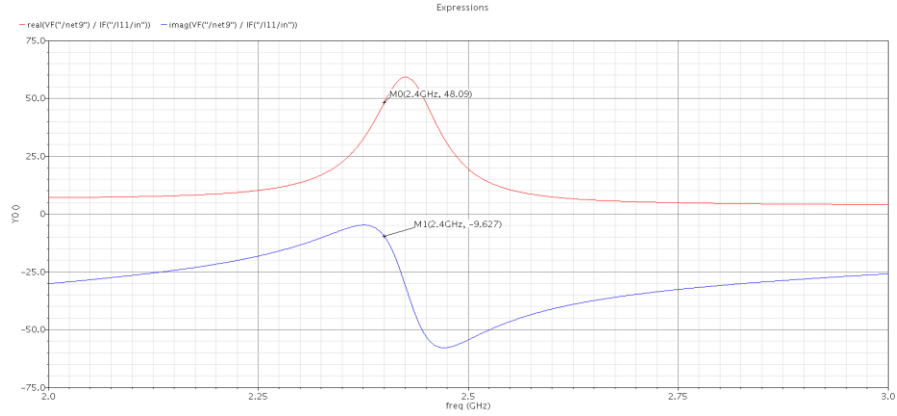
Figure 14: Receive-mode TR switch input impedance: 48 – j 10 Ω
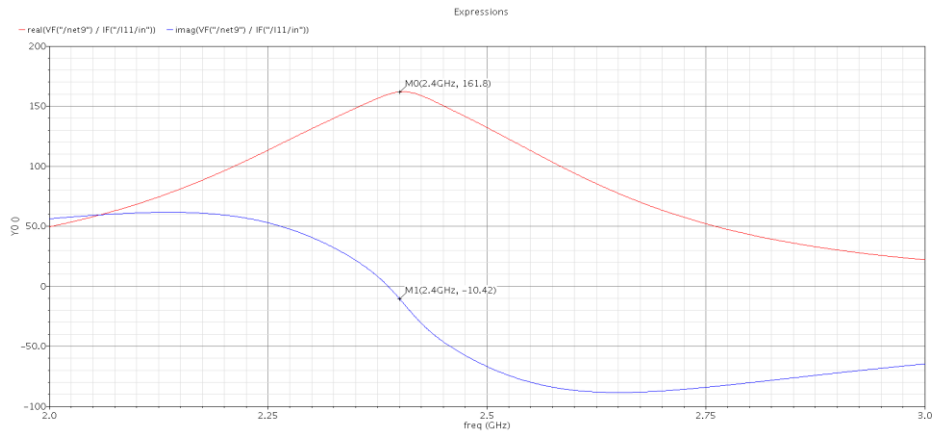
Figure 15: Transmit-mode TR switch input impedance: 162 – j 10 Ω

Figure 16: TR switch and LNA test bench

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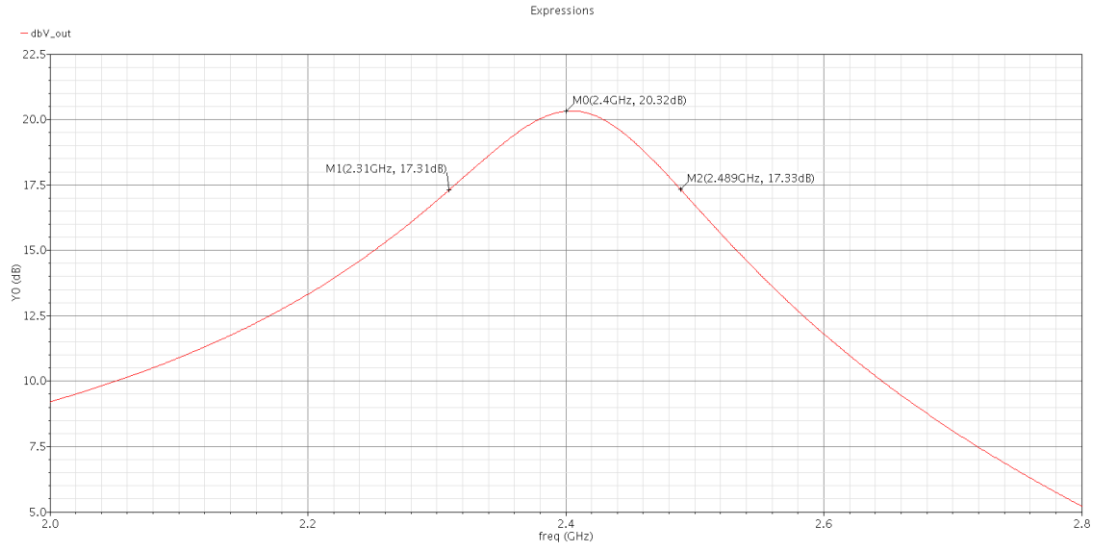
Figure 17: AC simulation of TR switch and LNA in receive-mode

With the TR switch and LNA simulated together, gain from the vsin source to the output is 20.3 dB, 8 dB less than simulated with the LNA alone. With the antenna impedance of 50 Ω, gain from the source is expected to drop 6 dB to from 28.7 dB to 22.7 dB. The other 2 dB is lost between the source resistance and the LNA input as the result of an imperfect switch and low input impedance on the LNA.

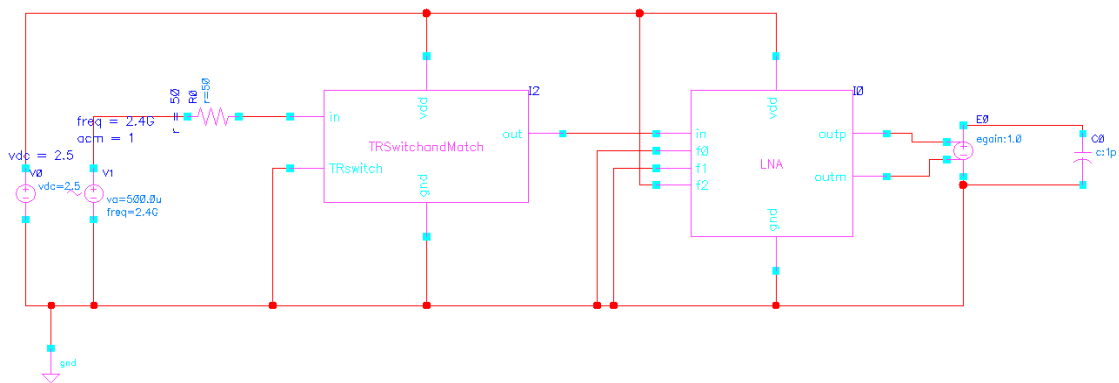With a transient simulation the gain dropped to 19.3 dB with the vsin source set to 44 mV peak to peak. The signal is measured as 17 mV peak to peak at the input of the LNA. The 1 dB compression point could probably be improved by increasing V_{gs} of the bias FET and therefore the input PFET.
The LNA consumed 1.77 mA of current in this simulation, or 4.4 mW of power.

I used Cadence's noise simulator to plot then integrate VN2() at the LNA's output over the 3dB bandwidth of 180 MHz. This gave a value of 63.37E-9 V^2.
Using 10 log ((S_{in}/N_{in})/(S_{out}/N_{out})) to calculate noise figure:
S_{in} at the TR switch port = 0.497 mV ^2 / 50 Ω
N_{in} = kTB = 1.38065E-23 * 290K * 180MHz
S_{out} / N_{out} = 10.38 mV ^2 / 63.37E-9.
This gives a noise figure of the TR switch and LNA of 6dB. This should improve after increasing the source inductor in the LNA and the inductor in the TR switch.

Layouts
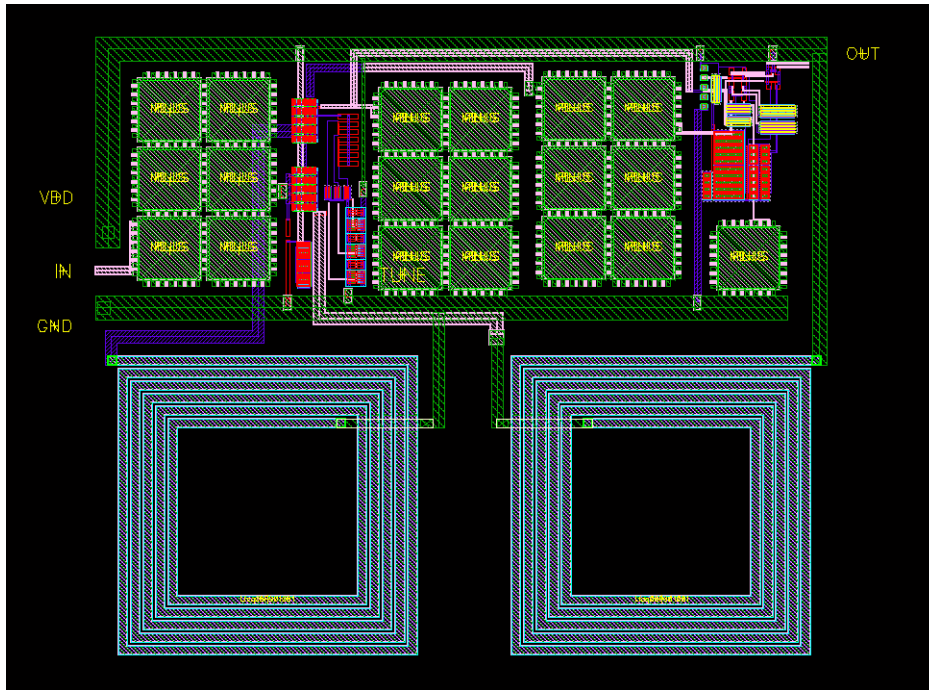
Figure 18: Layout of LNA
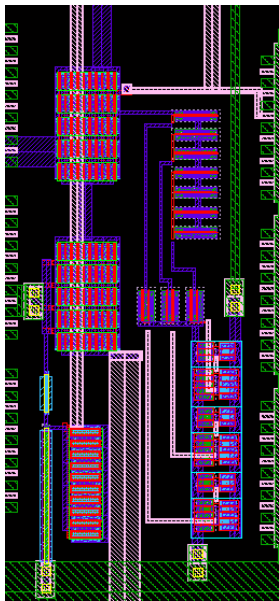
**Figure 19: LNA
stage 1 and tuning**
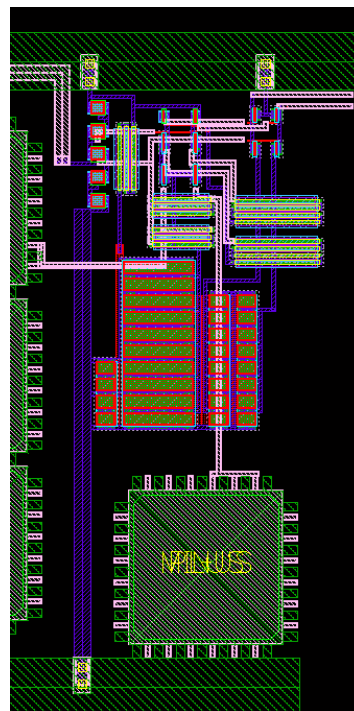
**Figure 20: LNA single to
differential stage**
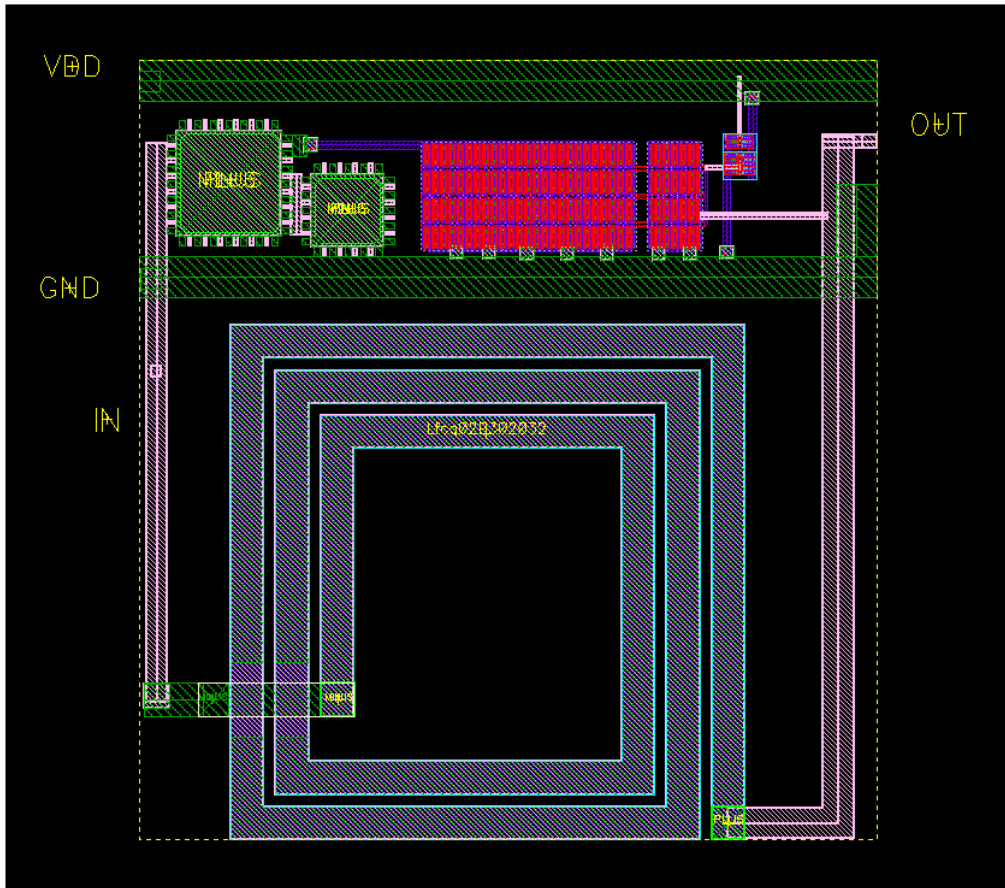
Figure 21: Layout of TR switch

The layout shown in Figure 22 of the pads, TR switch, and LNA takes up 685 x 1280 µm, including space left near the bottom for routing to the IF section. Routes for frequency tuning were added to the composite layout; in the LNA layout these pins are accessible through the metal 1 layer over the center block of 6 MIM caps.

Figure 22: Layout of input, TR switch, and LNA

Mixer

A passive image reject mixer is used to down convert the incoming signal to 110.6 MHz so that it is easier to filter and amplify before reaching the ADC. A passive mixer was designed as an alternative to the traditional Gilbert cell style in order to reduce power consumption and increase linearity, however this mixer's performance is entirely dependent on LO power. Conversion gain and input impedance change with LO signal levels. Only 20 µA of current is consumed from V_{DD} for biasing.

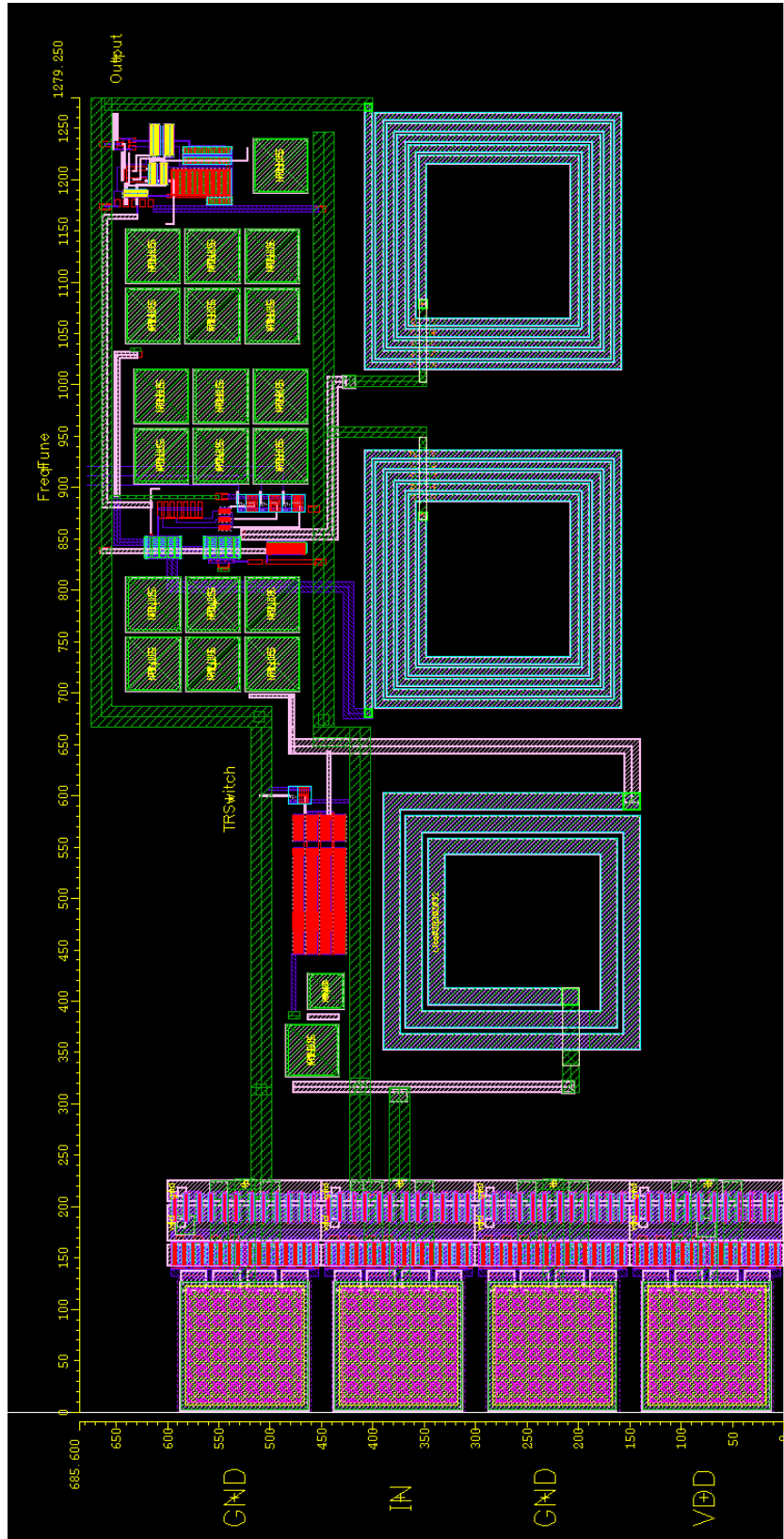The image reject mixer in figure 23 has differential inputs for RF, LO_Q and LO_I. The RF and LO_Q signal are fed to the top mixer block and the RF and LO_I signals to the lower block. The LO signals cause the HN FETs to switch on and off. These switching FETS are biased about 100 mV below the threshold level for HN FETs. Simulations showed this Vgs level resulted in higher conversion gain as the FETs start conducting in triode region slightly below the threshold level, but it may be better to modify the biasing to be slightly higher as the threshold will vary with manufacturing.

After mixing, the outputs from the two blocks are phase shifted. The RF signal mixed with LO_Q, which has a phase shift of -90 degrees pre-mixing, is phase shifted another -45 degrees with a 1 pole low pass filter. The RF signal mixed with LO_I is phase shifted +45 degrees with a 1 pole high pass filter. These 2 signals are then summed simply by connected them together at the inputs of the IF amplifier circuit, which is later. In schematic level simulations before layout and extraction, the mixer was tested with an IF amplifier block placed in each signal path before summation, after the high or low pass filters. More gain is achieved with these IF blocks placed after the summation node.

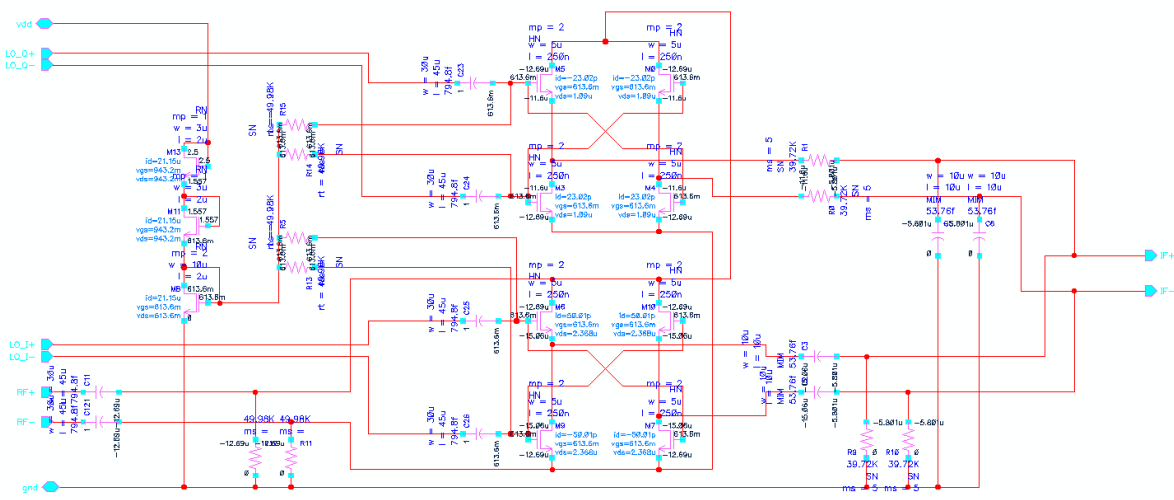Simulated image rejection is 18 dB in this design.

Figure 23: Passive image reject mixer schematic

The mixer was first connected to an ideal RF source for simulation as shown in the following test bench. Input LO signal levels are 1 V differential peak to peak. The Q LO signal is delayed by 109.1989 ps from the I LO signal (90 degrees).
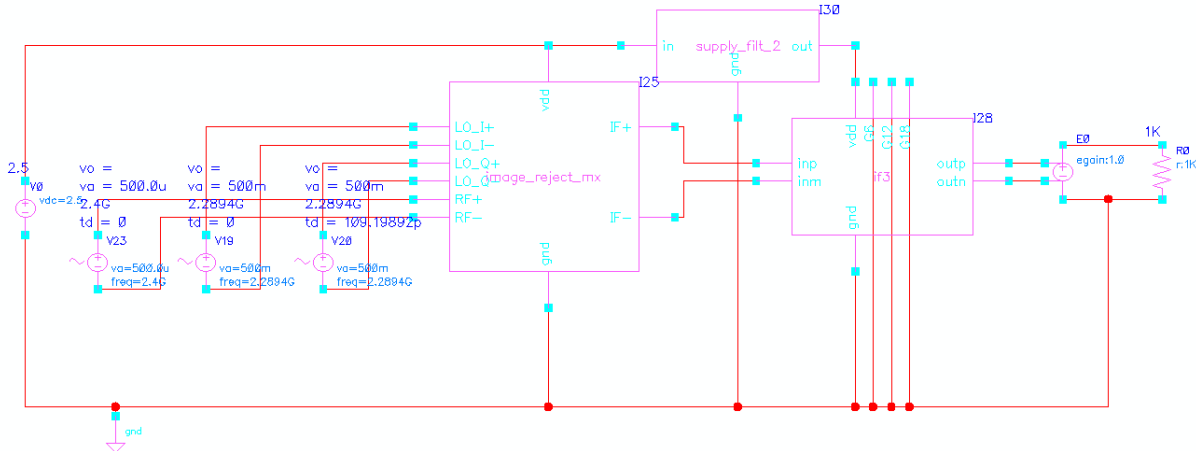
Figure 24: Mixer test bench with 1mV$_{PP}$ RF and 1V$_{PP}$ LO inputs

This passive mixer has limited isolation between ports, and the LO signal feed through to the output is significant, so several IF amplifiers between the mixer and off chip buffer are necessary for low pass filtering in addition to gain. Figure 25 plots the differential output between the IR mixer and IF amplifier. 1 mV of LO signal feedthrough is shown. The 110.6 MHz signal can be seen with an amplitude of 270μV, which corresponds to a conversion loss of 11 dB.

Figure 25: IR mixer output before summation with the IF block

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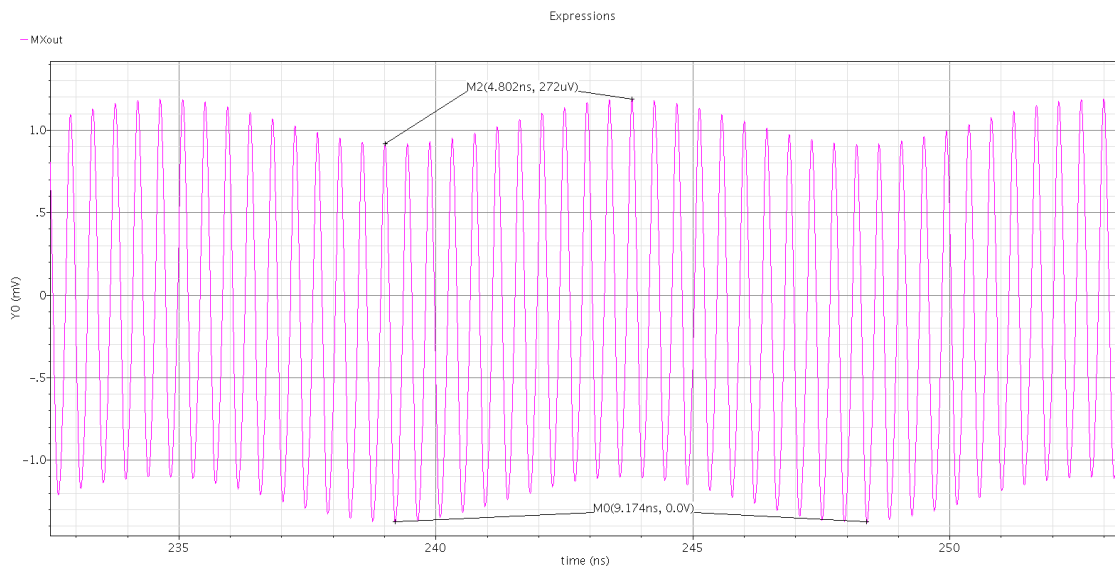The differential output after one IF amplifier is shown in figure 26. LO signal is still present.
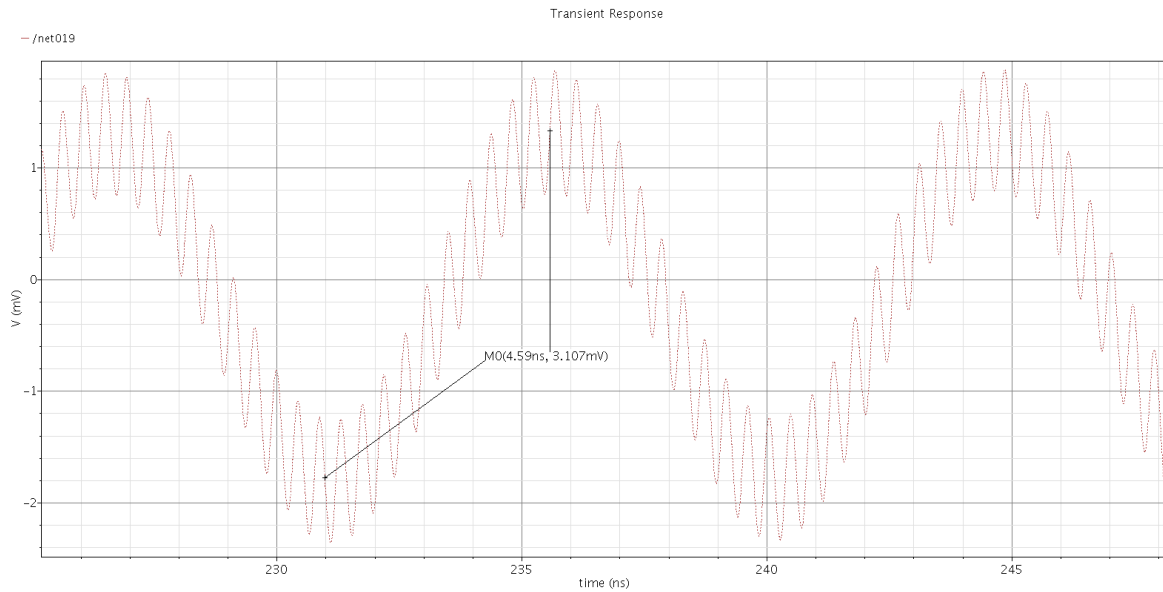
Figure 26: Output after mixer and one IF stage with RF source at 2.4 GHz

A second IF block was added to the test bench before simulating image rejection. The voltage after two IF blocks with a 2.4 GHz input signal is 27.2 mV. The RF input source was then changed to 2.1788 GHz. The output voltage dropped to 3.3 mV, showing image rejection of 18 dB.
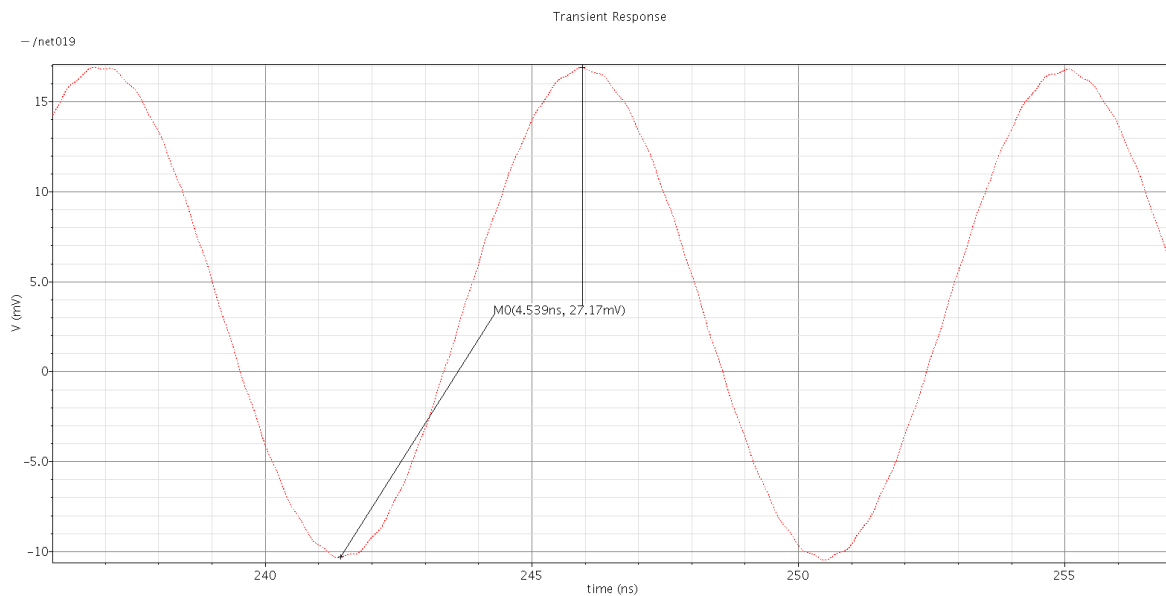
Figure 27: Output after mixer and two IF stages with RF source at 2.4 GHz: 27.2 mV
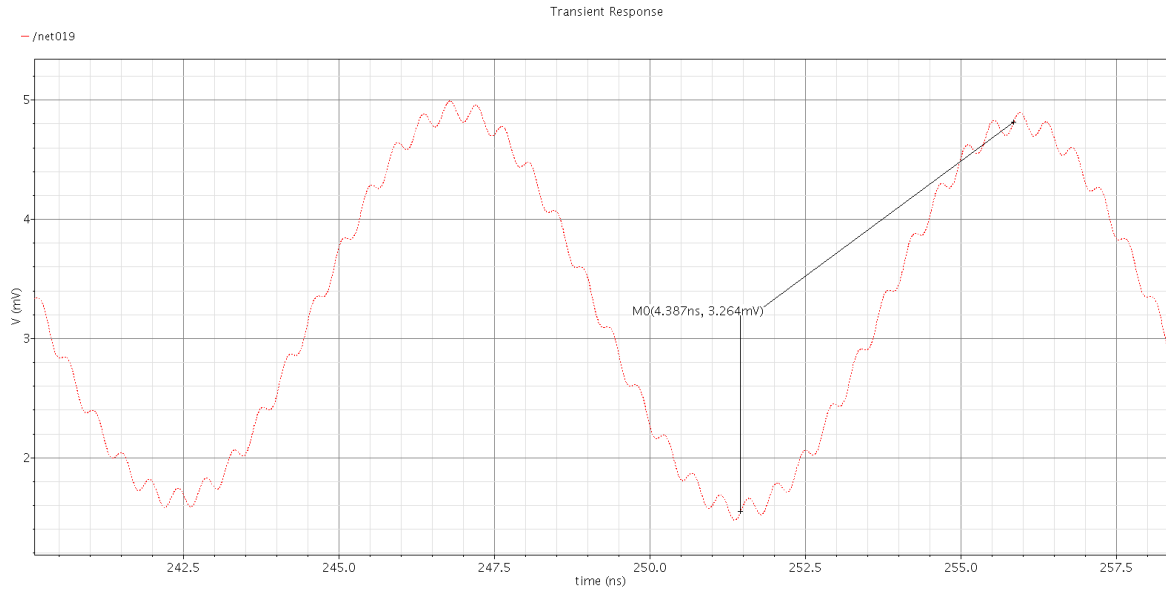
Figure 28: Output after mixer and two IF stages with RF source at 2.1788 GHz: 3.3 mV

The voltage and current at the RF port was plotted to determine input impedance. The 1 V differential LO signal causes these ports to float by about 10 mV. Input impedance averages approximately 60 Ω.
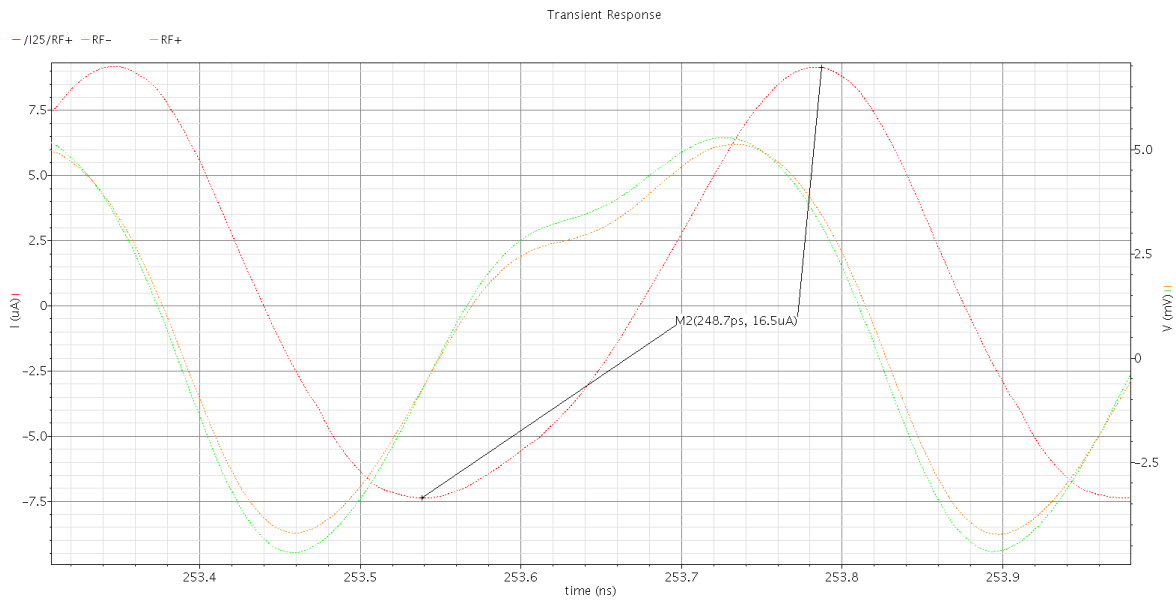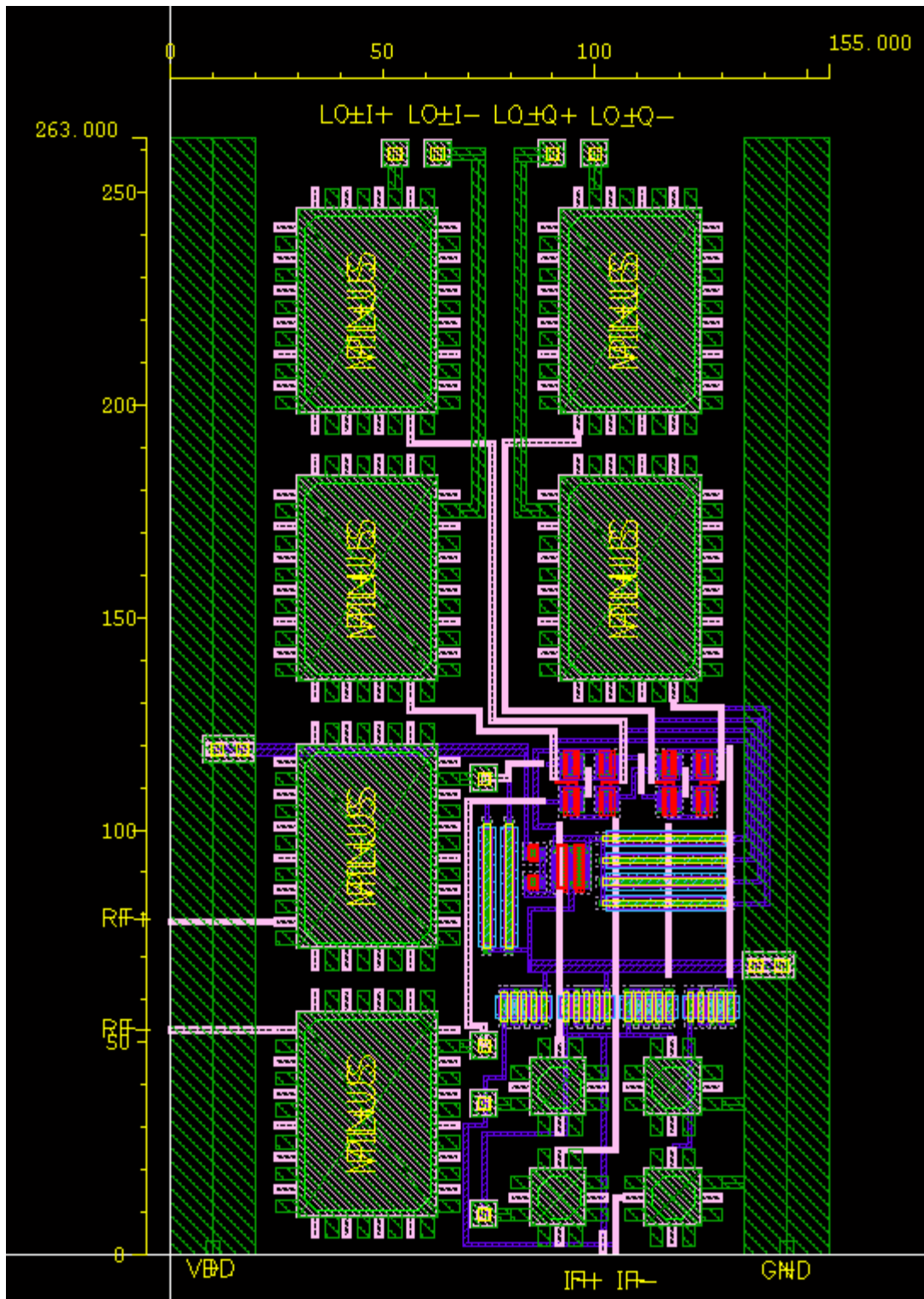

Figure 29: RF port input

Figure 30: Layout of mixer

Supply Filters

Figure 31: Schematic of supply filter

Supply filtering is necessary to remove noise on the power supply line to the IF circuits. Noise on the ground line is reduced by running separate grounds for each section of the chip [1]. The design for this supply filter was taken from [2]. This filter causes about 425 mV of supply voltage drop with a 350 μA current draw, like seen from the IF amplifiers, while providing 45 dB of attenuation to signals up to around 100mV in amplitude at 110 MHz. Transistors M0 and M1 act as capacitors with a value of approximately 25 pF. This supply filter's output impedance is about 60Ω. This is mostly seen through capacitor M0 to ground.

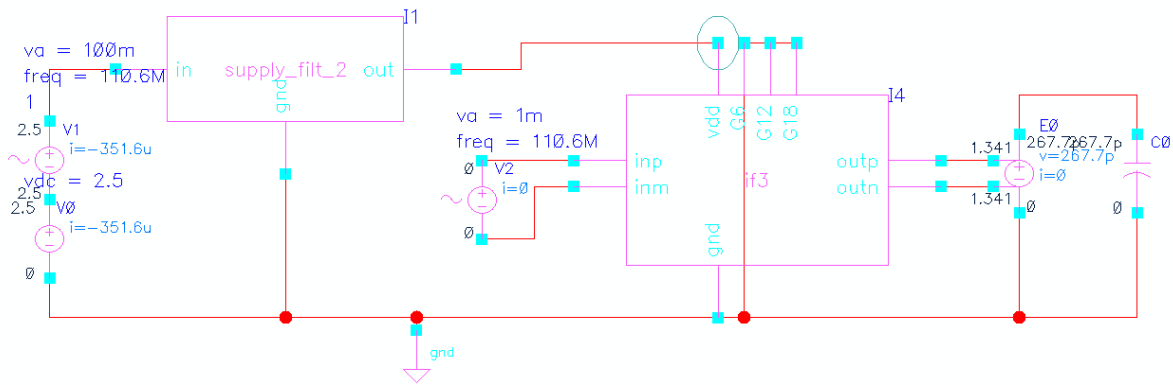A test bench with one IF amplifier was set up to test the filter's performance.

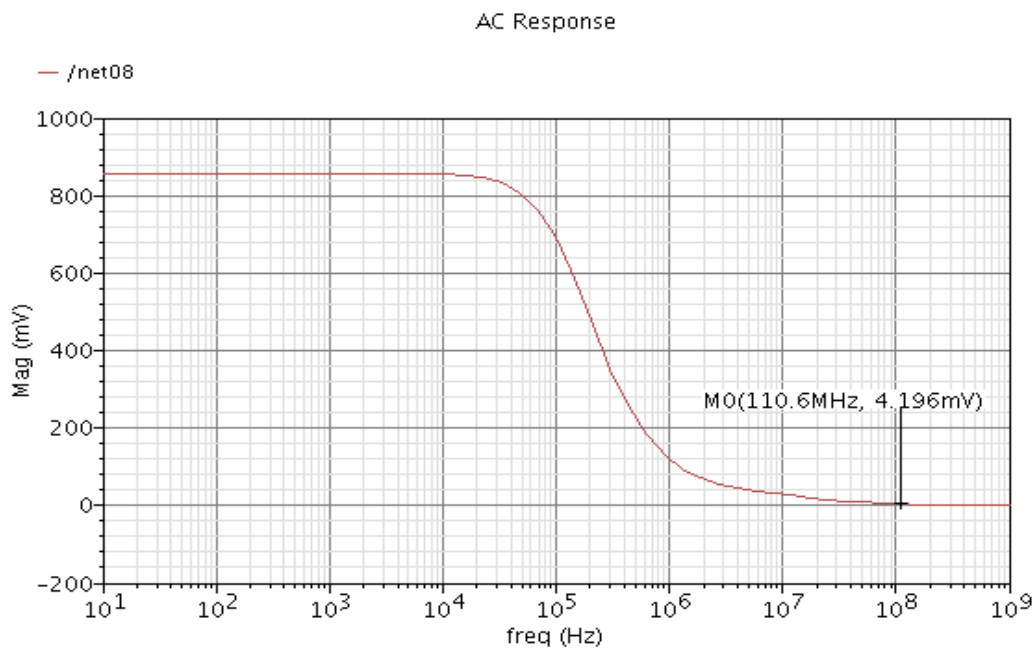**Figure 32: Supply filter test bench**

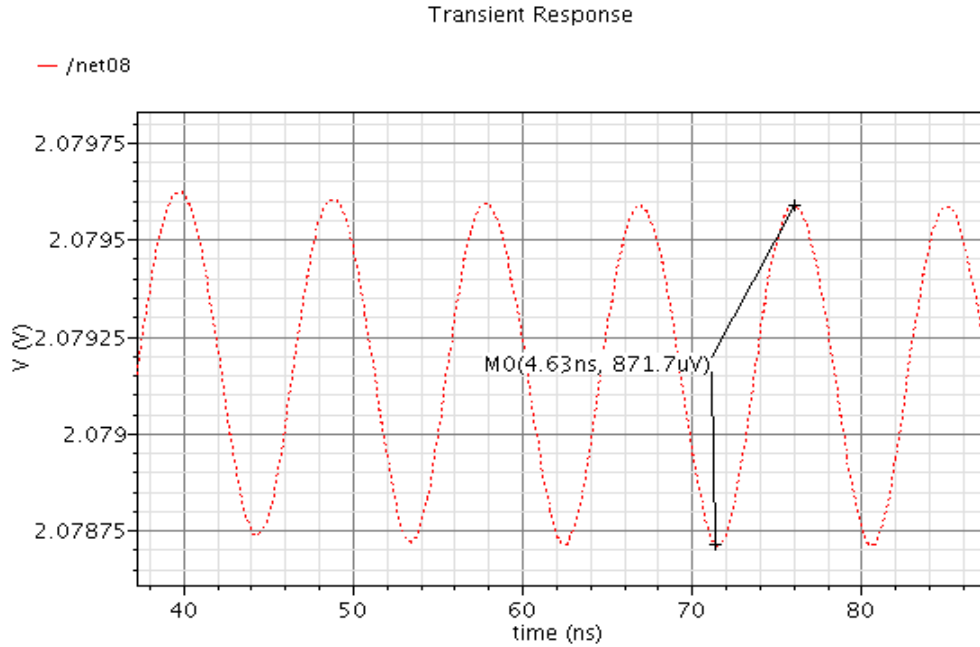**Figure 33: AC simulation with 1V input noise on supply line**

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Figure 34: Transient simulation with 200mV$_{PP}$ signal at 110 MHz on the supply line

In the simulation shown in Figure 35, the source with 500 mV$_{PP}$ is turned on at 30 ns. Attenuation is 40 dB.
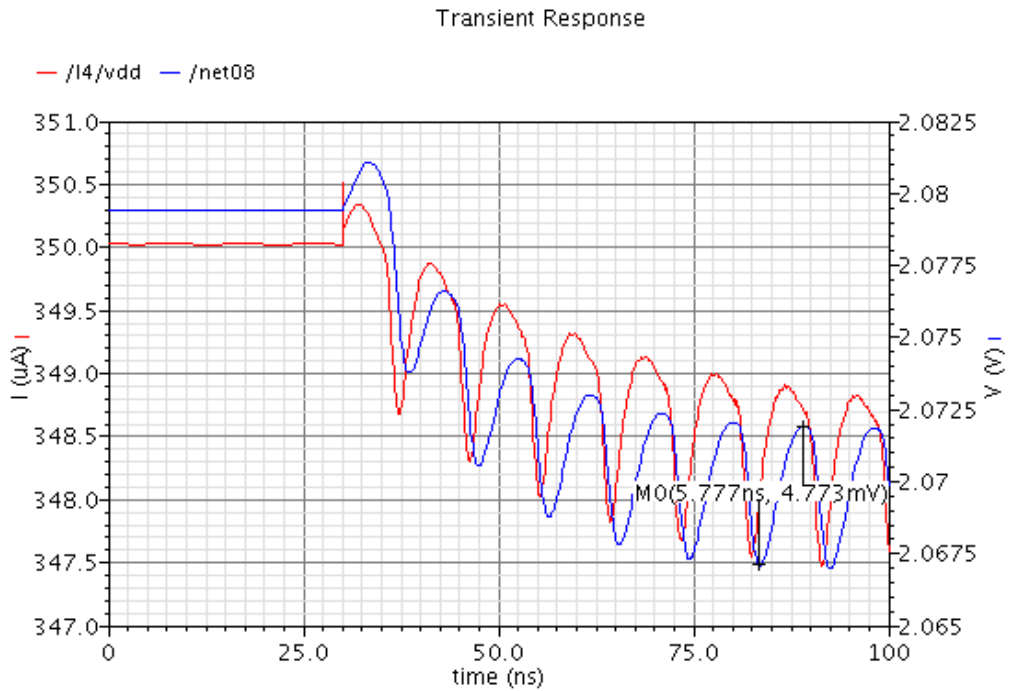

Figure 35: Transient simulation with 500mV$_{PP}$ signal at 110 MHz on the supply line
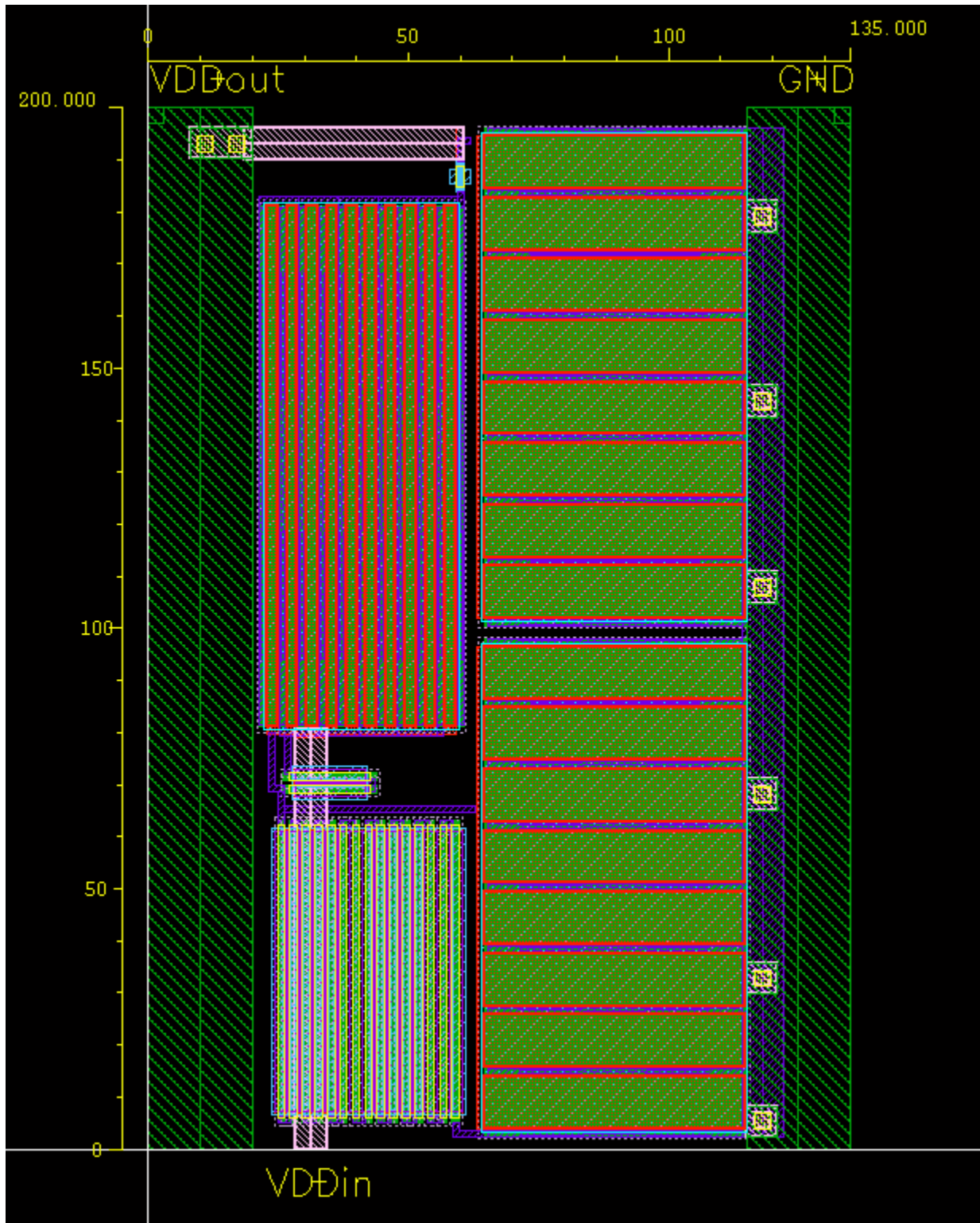
Figure 36: Layout of supply filter

IF Amplifier and Off-Chip Buffer

Cascaded differential amplifiers are used to increase the voltage level of the mixer output up to the 100 mV level required by the ADC. Each stage draws 350 µA from the power supply. 20 dB of voltage gain is provided per stage with all of the gain controls grounded, or G6, G12, and G18 can be pulled high to drop gain by approximately 6, 12, and 18 dB respectively so the amplifiers do not become saturated. The cascode load from previous versions of this schematic was replaced by a single PFET due to lower headroom with a 2.5V supply. As shown in simulations on the following page, the corner frequency is still slightly below 110 MHz.
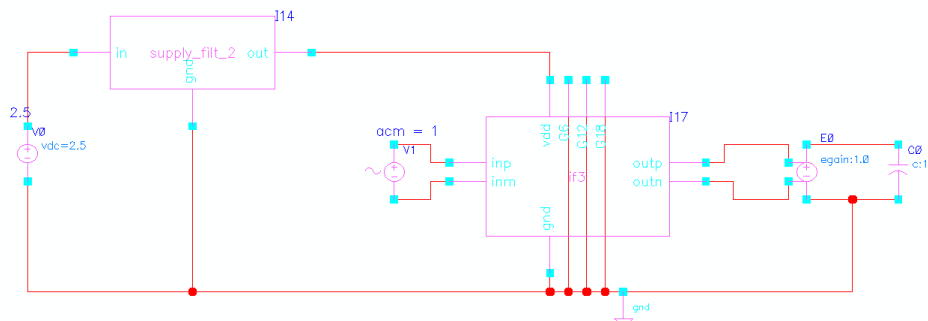

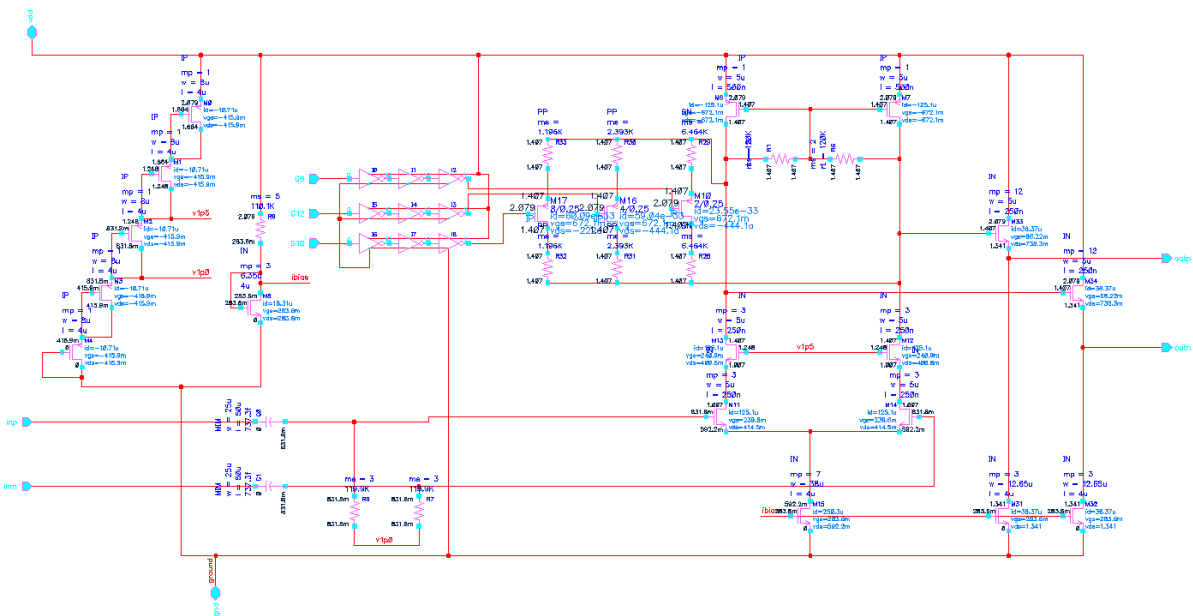
Figure 37: IF amplifier test bench

Figure 38: Schematic of IF amplifier

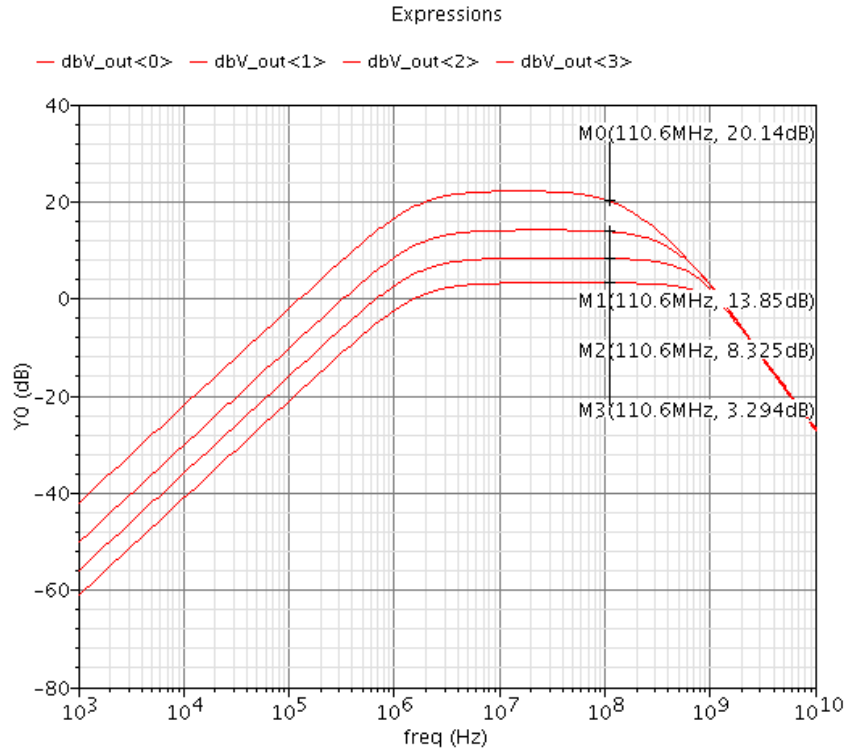# IF Amplifier Simulations

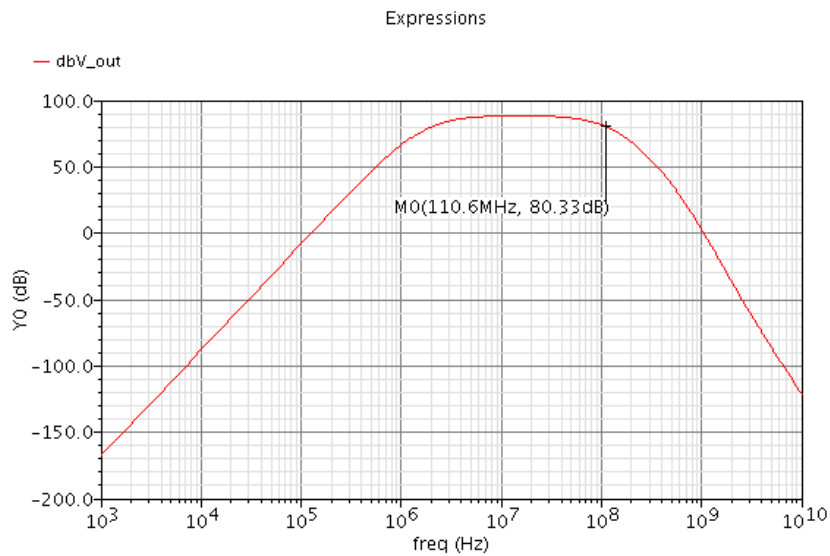**Figure 39: IF AC simulation at 4 gain settings**

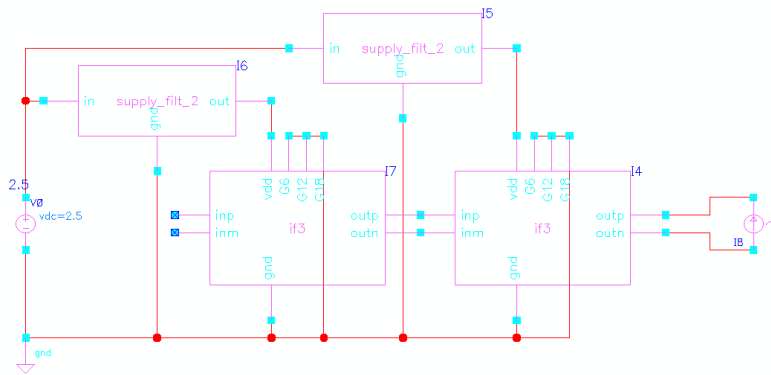**Figure 40: IF AC simulation with 4 IF stages**

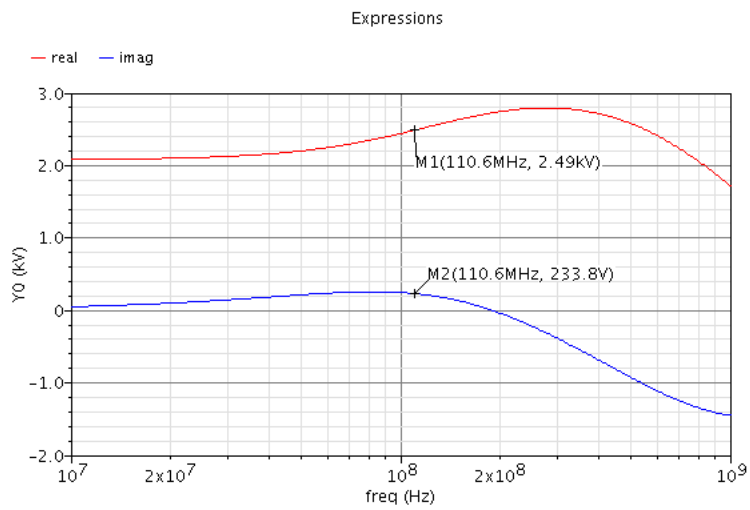**Figure 41: IF amplifier output impedance test bench**

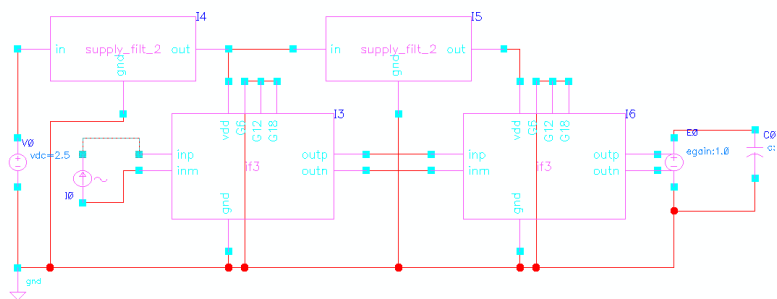**Figure 42: IF amplifier output impedance: 2.5k + j 230 Ω**

Figure 43: IF amplifier input impedance test bench
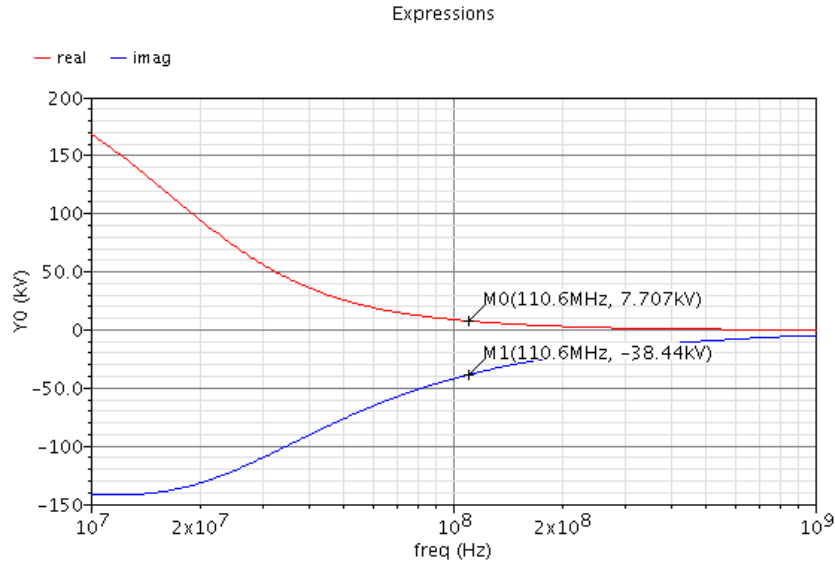
Figure 44: IF amplifier input impedance: 7.7k - j 38.4k Ω

A transient simulation was also run to show how the IF amplifier performs when compressed and to show the need for gain control. A 1 V$_{PP}$ differential signal was input to two IF stages. Output is 3 V$_{PP}$ differential with the peak at about 1.9 V and trough at 400 mV. The left graph shows both positive and negative outputs while the right shows their difference. The output is not perfectly symmetrical. The differential output is below zero for a slightly longer duration than above zero.

Figure 45: IF amplifier transient simulation with 1 V$_{PP}$ input

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Figure 46: Layout of IF amplifier

IF Buffer

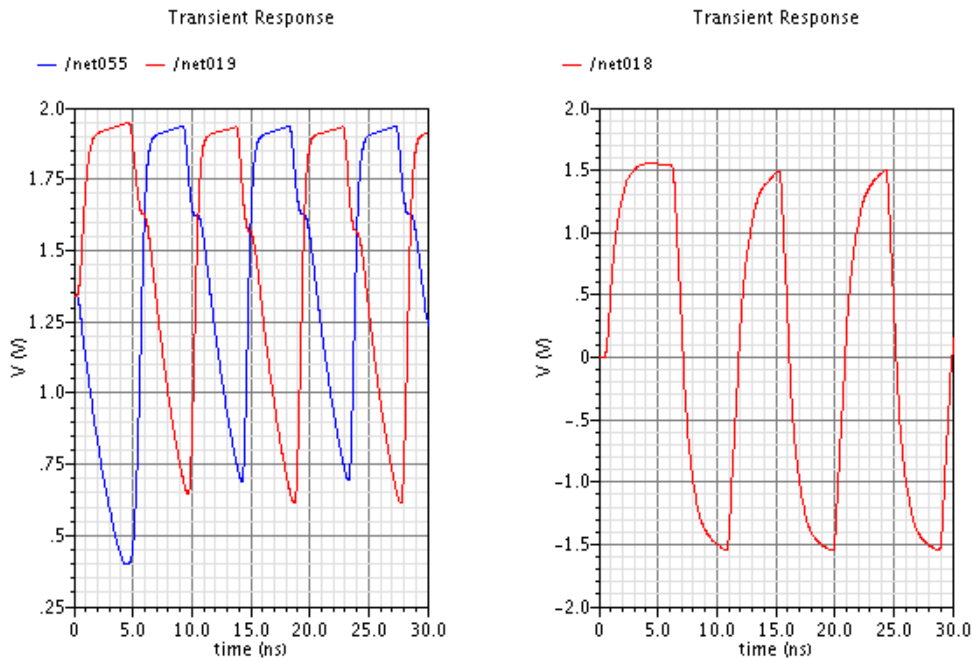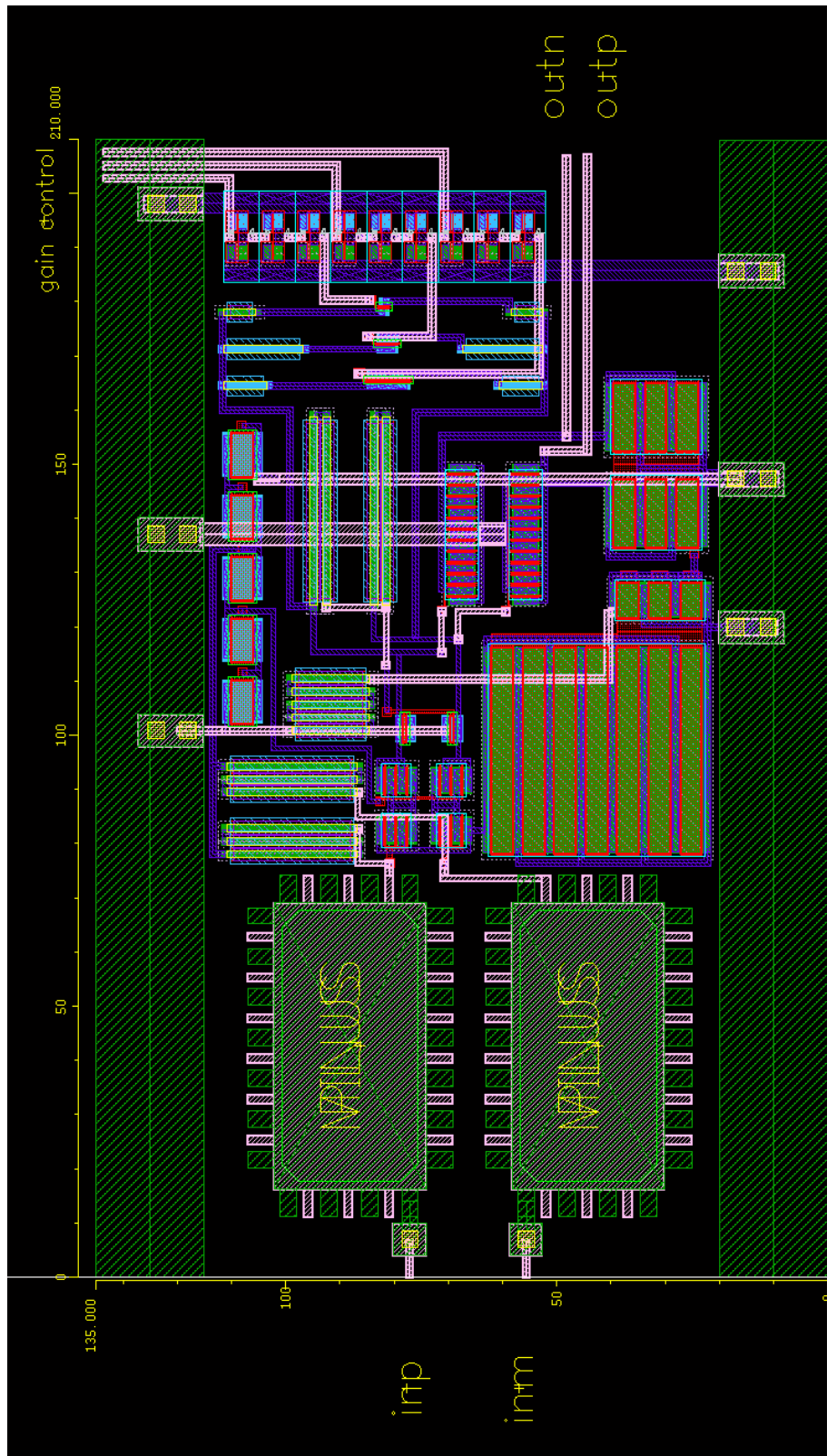An off chip buffer is used for the IF filtering. An Epcos model B39111B4542H310 filter provides a 1.1 MHz bandwidth at 110.6 MHz with an insertion loss of 12 dB in a 5 x 7 mm package. However, its input and output impedance are 170 Ω in parallel with a 30 pF capacitor. This is equal to 12 − j 44 Ω series impedance, or a magnitude of about 50 Ω. The current design requires 1 A to drive 50 Ω load. The supply filter design is not capable of supplying 1 A without dropping the supply voltage too low. The W/L ratio of M14 needs to be greatly increased so that this circuit can drive 50 Ω while using less current.
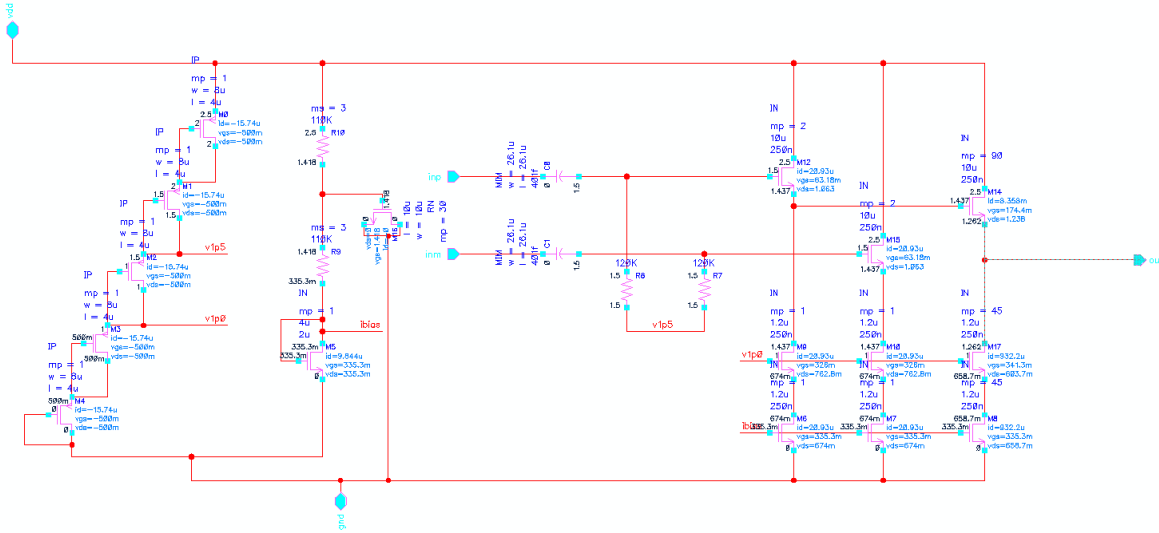
Figure 47: Schematic of buffer

The design for this buffer was taken from the previous 400 MHz chip, described in [3]. Biasing is similar to the IF amplifier with an extra bypass capacitor added to the current reference. From [3], "The buffer itself is configured as two cascaded source-followers. The differential input signal is fed to two identical low-power followers to maintain balance. One of these follower outputs is left open while the other feeds a larger follower which drives the filter."

Figure 48: Buffer test bench with supply filter unconnected

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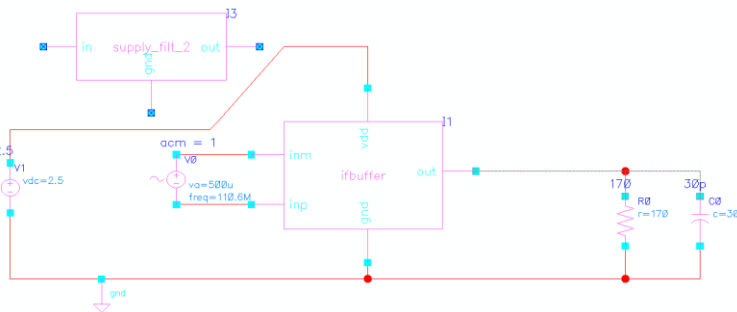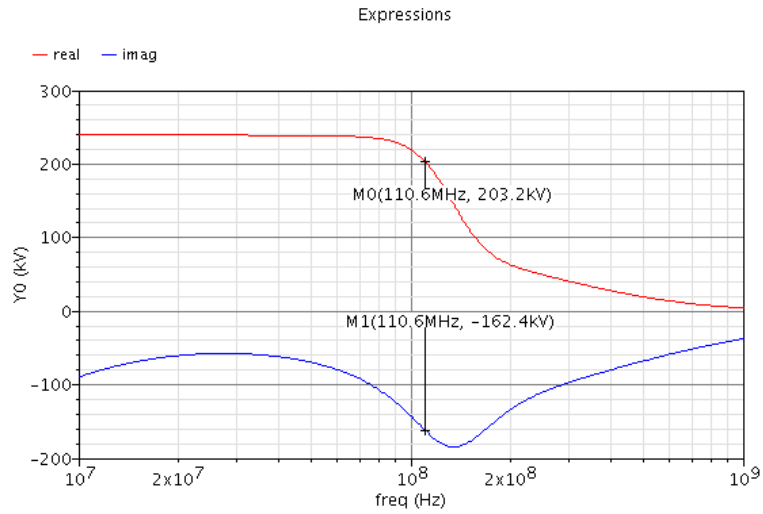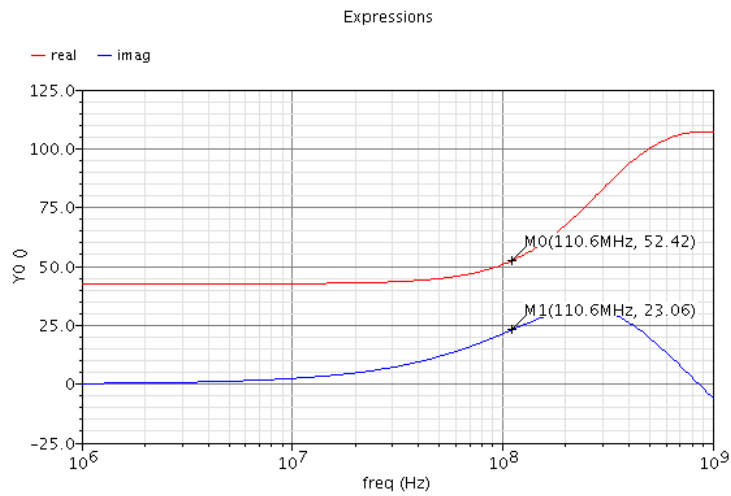**Figure 49: Buffer input impedance: 203 k - j 162k Ω**

Figure 50: Buffer output impedance: 52 - j 23 Ω
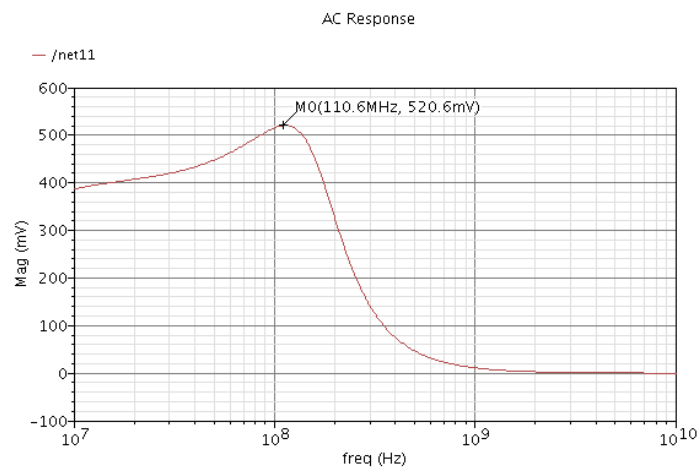

Figure 51: AC simulation of buffer

1 bit ADC

A comparator based on the sense amplifier from Baker was implemented. M0, M1, M8, and M9 form a cross-coupled inverter, or latch.   W/L ratios for the inverters were set to center the switching point: 2.8/0.25 µm for the PFETs and 2.8/0.35µm for the NFETs. M18 and M19 set the inputs to this latch, steering current to one side depending on which input voltage to the comparator is higher. The outputs to the latch feed a set-reset latch made with NAND gates. When the clock is low, M0 and M3 pull the both inputs to the SR latch high. The outputs of the SR latch are now held. M4 and M5 are also turned off with the clock low so that there is no connection between VDD and ground through the latch and no current flows. When the clock goes high, M4 and M5 are turned on and positive feedback allows the input signals to the comparator to be compared and the inputs to the SR latch to go to ground and VDD. The SR latch allows the output to switch only on the rising edge of the clock.   If the biasing were removed from this circuit, the comparator would fail to operate with high signal levels.   [4]
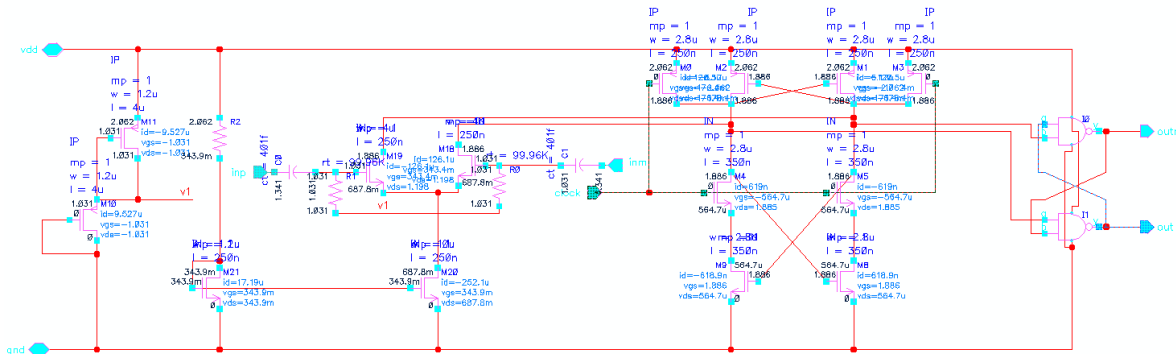

Figure 52: Schematic of ADC

RMS supply current for the comparator is 450 µA. Biasing on the input FETs was set to 250 µA total. Input impedance is 30k – j 74k Ω.
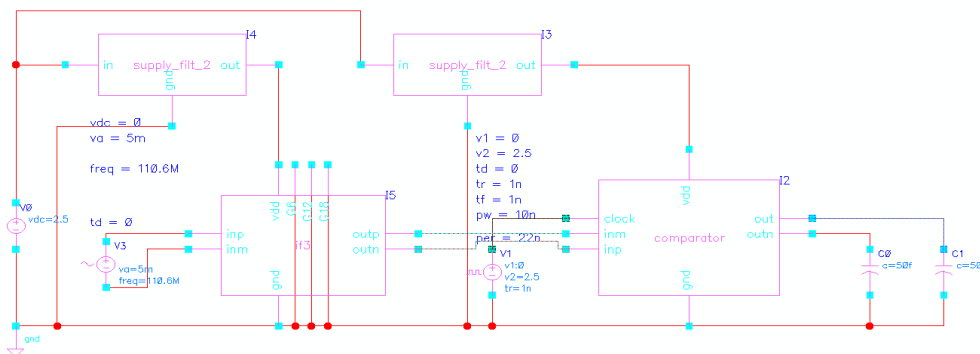

Figure 53: ADC test bench with a 10mV$_{PP}$, 110.6 MHz signal input to an IF amplifier preceding the comparator

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Propagation delay while rising and rise times are both less than 1 ns. Falling propagation delay and fall times are approximately 1.75 ns. The following simulation was done with 100 mV$_{PP}$ input signal with no noise. At 155 ns, the output rises to approximately 400 mV before falling again. In this case, the output differential signal went positive at 154.8 ns as the clock was halfway risen. Ripples in the output high level are caused by the supply voltage dipping slightly as the supply filter provides more current.
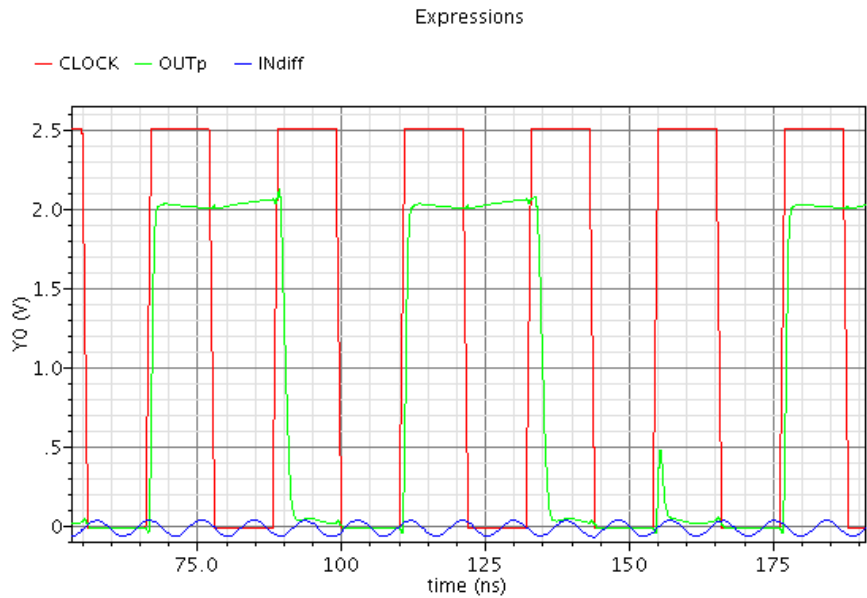

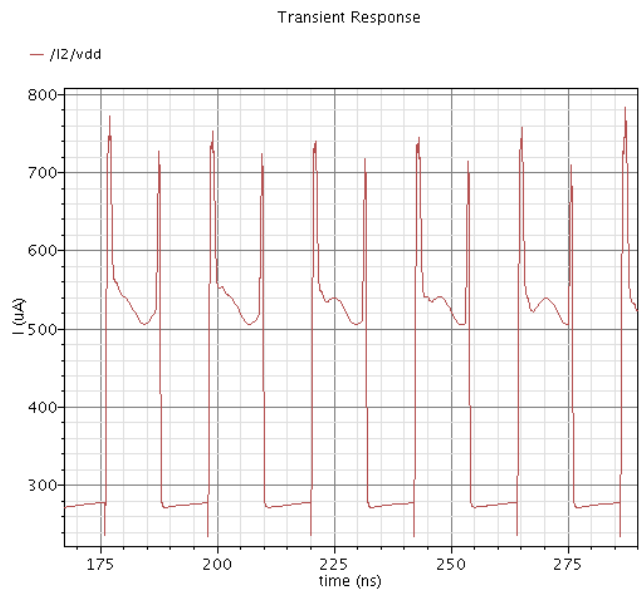**Figure 54: Transient simulation with 100 mV$_{PP}$ input signal**

Figure 55: Transient simulation showing supply current to ADC

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The comparator should be made more robust before fabrication. The input source to the test bench in Figure 53 was reduced to 5 mV$_{PP}$ and several instances where the comparator did not perform as expected were recorded when the output was high before a rising clock edge.
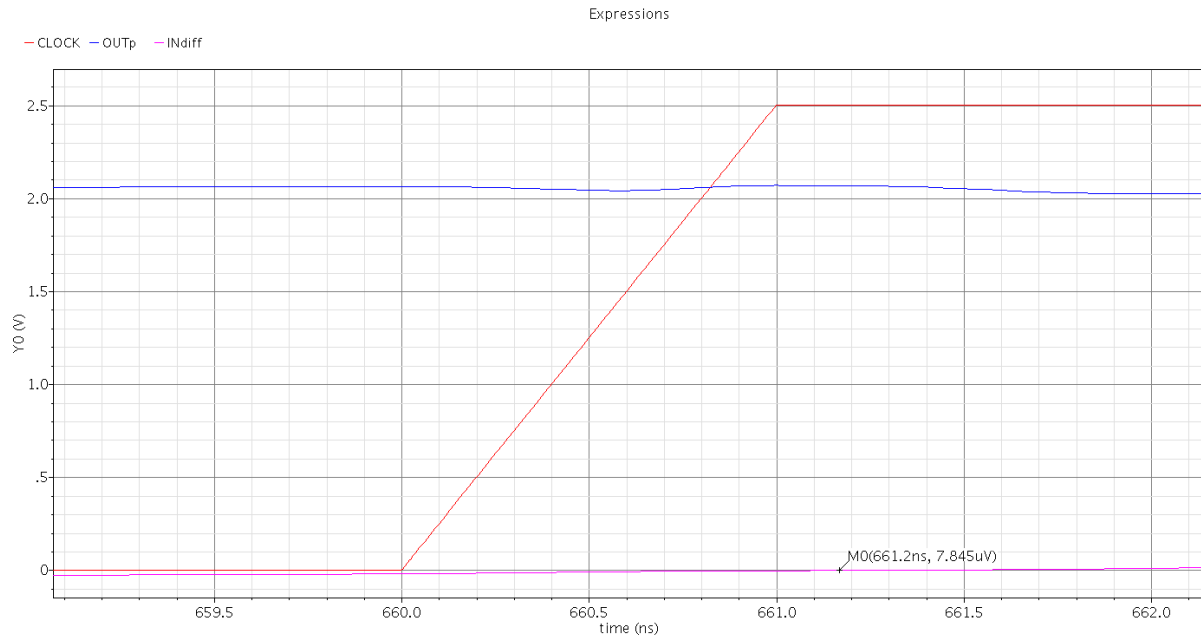

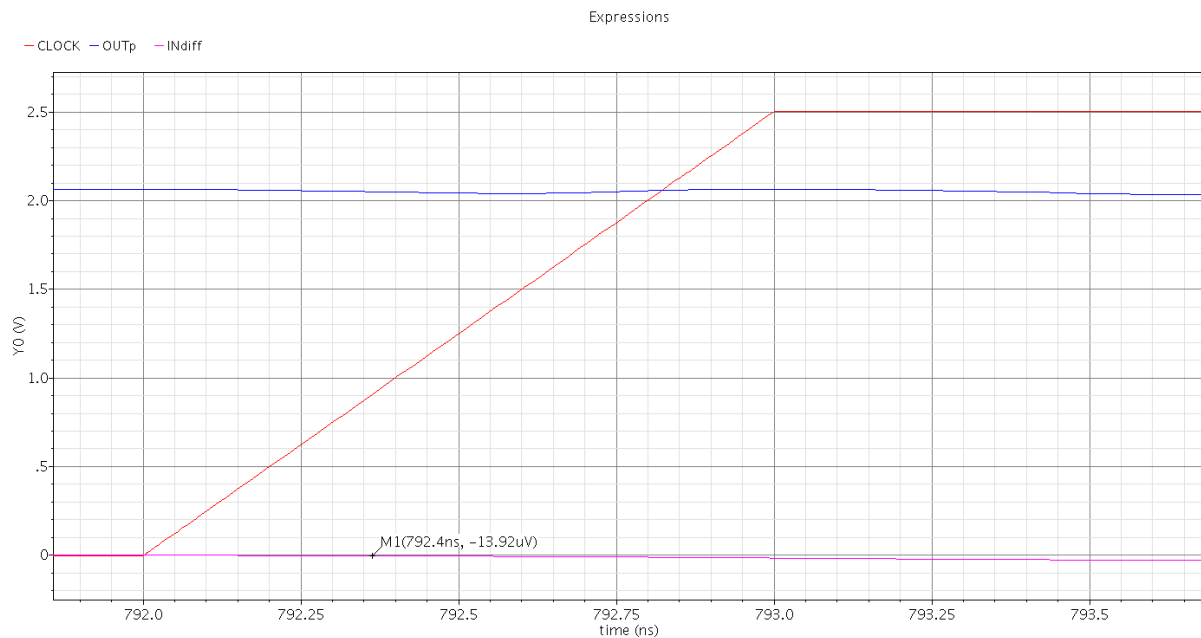**Figure 56: Comparator output failing to fall low when the input went high 200 ps after the end of a rising clock edge**

Figure 57: Comparator output failing to fall low when the input went low 200 ps after the start of a rising clock edge
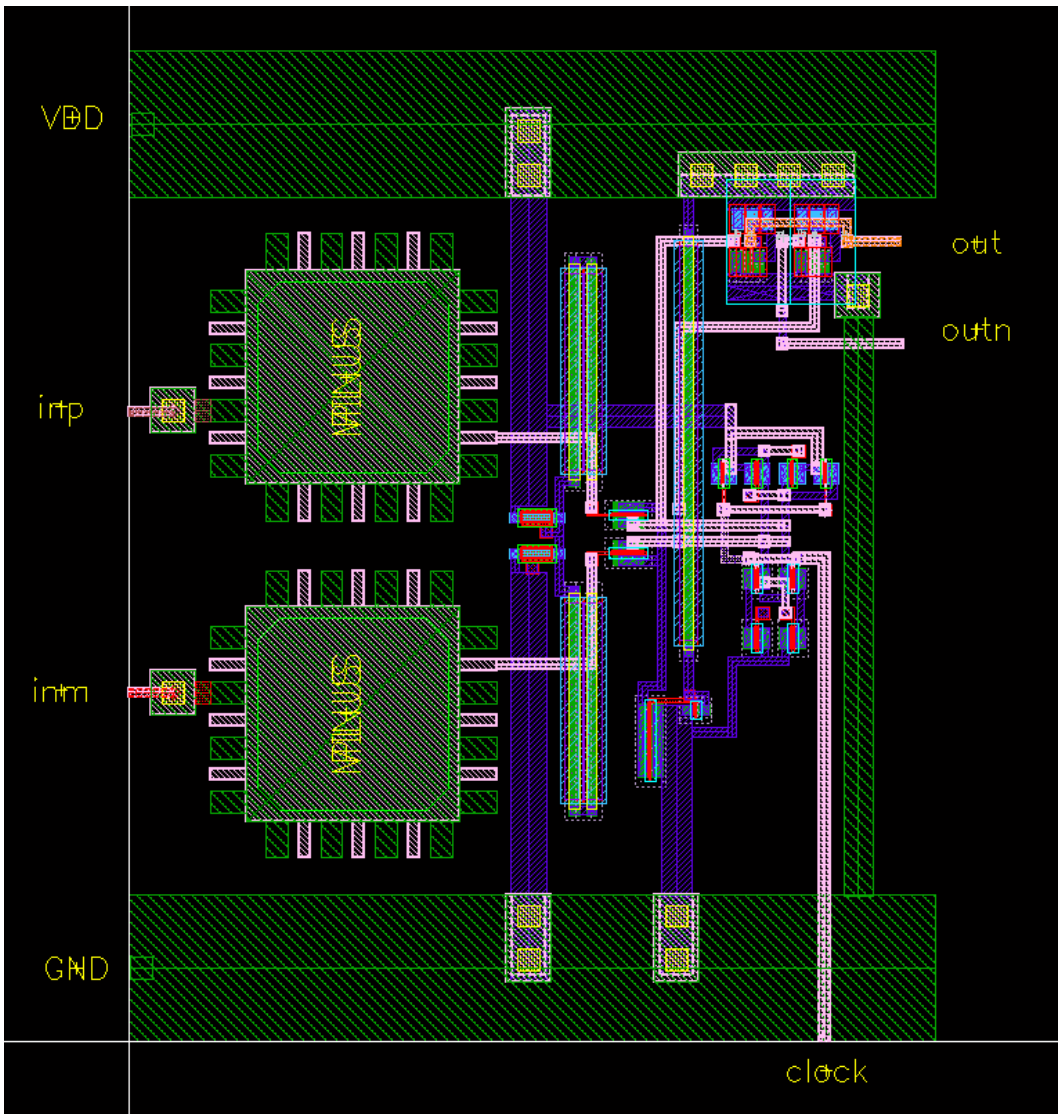
Figure 58: Layout of ADC

System Simulations and Conclusion

The front end was connected together in the following test bench. A 1 mV 2.4 GHz source with 50 Ω resistance feeds the TR switch, LNA, mixer, and three IF blocks. The differential output of the mixer, before summation, is 680 µV. Mixer conversion gain could be increased slightly with larger LO signals. After three IF stages, the signal level is 700 mV. With an input voltage level of 70 nV (-130 dBm into a 50 Ω antenna), this would result in a 25 µV signal into the off chip filter, assuming gain of 0.5 from the buffer. To get to a mV level signal before going off chip, gain of at least 40 is still needed in this chain. This could be provided by increasing the input impedance to the LNA and improving the transmit/receive chip so it acts as a step-up matching network.   2.8 mA is supplied from VDD for all the circuits shown below.

After returning on chip, 4 IF stages would be needed before the ADC to get the voltage up to 100 mV$_{PP}$, assuming filter loss of 12 dB. 4 additional IF amplifier stages and the ADC will consume another 2.2 mA of current from the supply. With 1 mA allocated for the off-chip buffer if necessary, this sums to 6 mA for the lower half of the transceiver chip, or 15 mW of power consumption, not including the necessary VCO for reception.
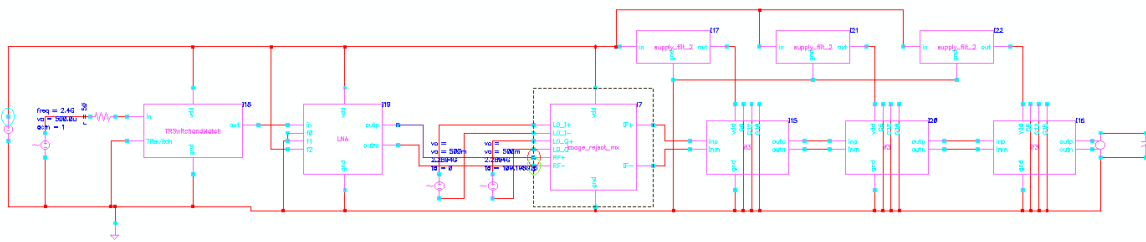

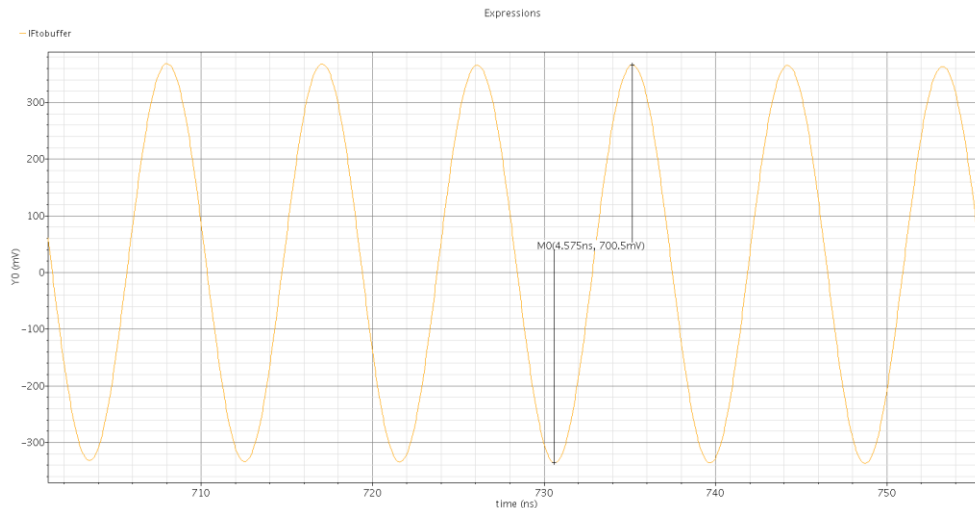**Figure 59: Front-end test bench**

Figure 60: Output of test bench with 1 mV$_{PP}$ input

References

[1]   W. B. Kuhn, et al., "A Micro-transceiver for UHF Proximity Links Including Mars Surface-to-Orbit Applications", *Proceedings of the IEEE*, Vol. 95, No. 10, October 2007.

[2]   W. B. Kuhn, *Supply Filter, Measurements,* ECE 765 Fall 2012 class notes.

[3]   W. B. Kuhn, *IF Amp Buffer*, ECE 765 Fall 2012 class notes.

[4]   R. Baker, *CMOS Circuit Design, Layout, and Simulation, 3rd Edition,* Hoboken: Wiley, 2010, pp. 450-*451,918-919.*

[5]   M. Clewell, A. Fund, S. Khamis, M. Peters, *2.4 GHz Micro-Transceiver Design*, ECE 765 Fall 2012 class report.